MAD2402

Data Sheet

Version: 1.00

Features

❖ Delta Sigma ADC

- **ADC Resolution 24 Bits**
- **Data Output Rates up to 1280 SPS**
  - Selectable 10SPS or 40SPS output data rate by PD_SCK clock number
  - Programmable output rates from 10SPS to 1280 SPS by ADC command mode
- **Input Multiplexer with two Differential Inputs**
  - One external differential input AIN0 and AIN1
  - One internal differential input for DVDD and AVDD supply voltage difference measurement
- **Chopper-Stabilized Input Buffer**
- **Low-Noise PGA with programmable gain up to 128**
  - Chip default gain of 128
  - Programmable gain of 1, 2, 4, 8, 16, 32, 64, 128 by ADC command mode

❖ Power

- **Built-in a power management controller with Power-Down and wakeup control**
- **Support Normal mode and Power-Down mode control by PD_SCK pin**

❖ Reset

- **Built-in embedded POR (power-on reset) circuit**
- **Provide software register force reset**

❖ Clock

- **Built-in embedded IHRCO (internal high frequency RC oscillator)**

❖ Communication

- **Two-wire serial port for ADC data output**
- **Support simple ADC conversion mode by PD_SCK clock number**
  - Three fixed conversion mode: 10-SPS/PGA=128, 40-SPS/PGA=128, 40-SPS/DVDD-AVDD
  - One user configure conversion mode
- **Support ADC command mode for register setting**

❖ Operating

- **Analog Supply range: 2.5V to 5.5V**
- **Digital Supply range: 2.5V to 5.5V**
- **Operating temperature range -40℃ ~ 85℃ (**1)**

❖ Package Types

- **SOP8 / DIP8**

(**1): Tested by sampling.

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1. General Description

The chip is embedded a precision 24-bit analog-to-digital converter and designed to provide high-resolution measurement solutions for the most applications. The converter is implemented a low-noise input buffer, a low-noise programmable gain amplifier (PGA), a 2nd-order delta-sigma (ΔΣ) modulator and a digital filter. It's designed to easy use for weigh scales and other applications by connecting directly with the external bridge sensor. The chip is packaged in an SOP-8 or DIP-8.

A flexible input multiplexer handles differential signals input. The selectable input buffer can enable to increases the input impedance. The PGA provides gains from 1 to 128. The digital filter can optimize a resolution of up to 24 bits and a data rate of up to 1280 samples per second (SPS).

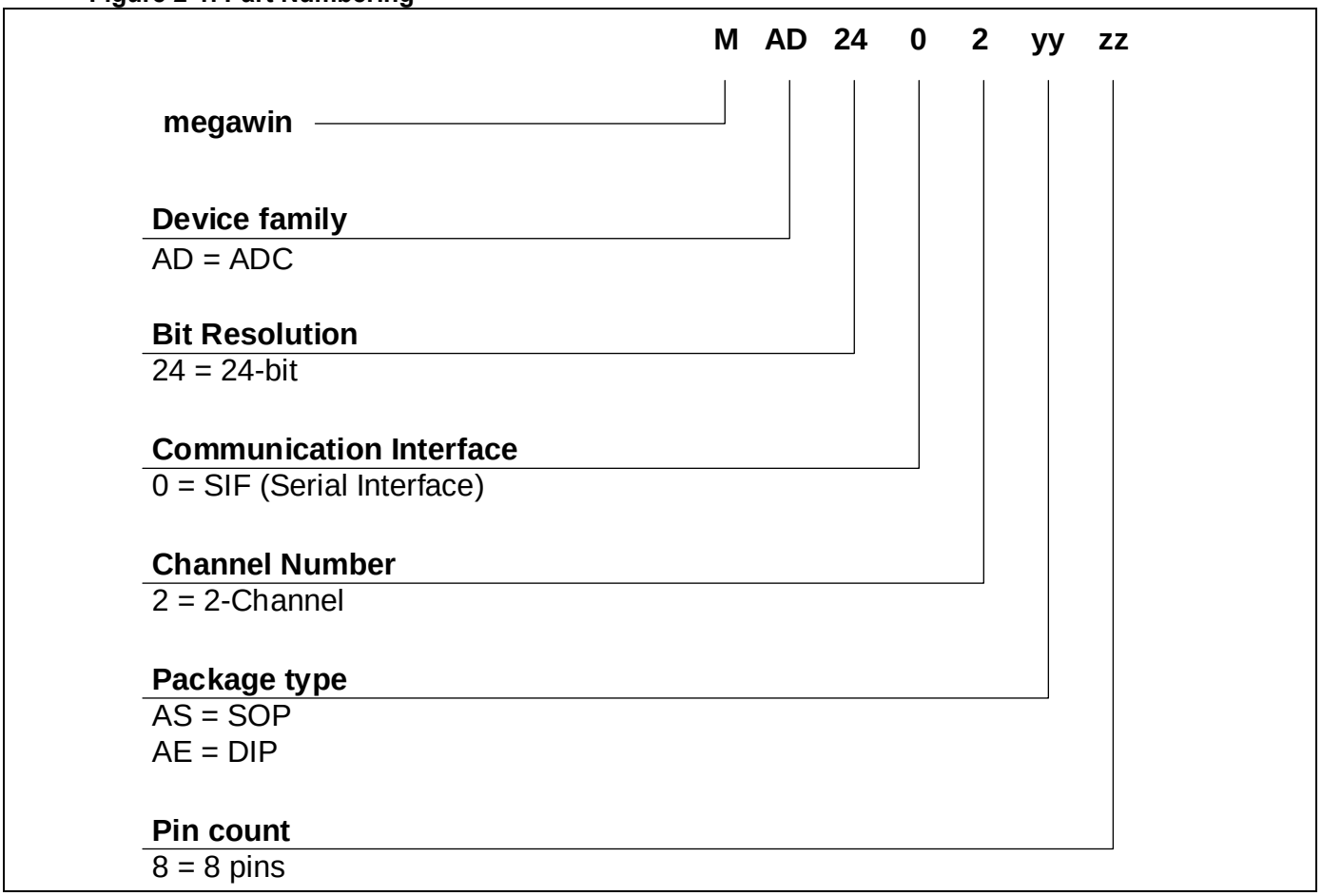
The chip is built-in embedded Power-On Reset (POR) circuit to generate internal hardware reset signal to reset the chip. For power management and reset control, the chip is built-in a power supervisor for power down control and wakeup control. Also the chip is embedded a high precision internal oscillator (IHRCO) as internal clock sources.

The communication is handled by a 2-wire serial interface to get ADC code and control the ADC settings from external MCU device. There is no programming needed for the internal registers to operate three designed fixed ADC conversion modes, (1) 10 SPS with PGA=128 (2) 40 SPS with PGA=128 (3) 40 SPS for DVDD and AVDD supply voltage difference measurement.

2. Order Information

Please contact the megawin sales for available options (package, …) and more information about this device.

Figure 2-1. Part Numbering



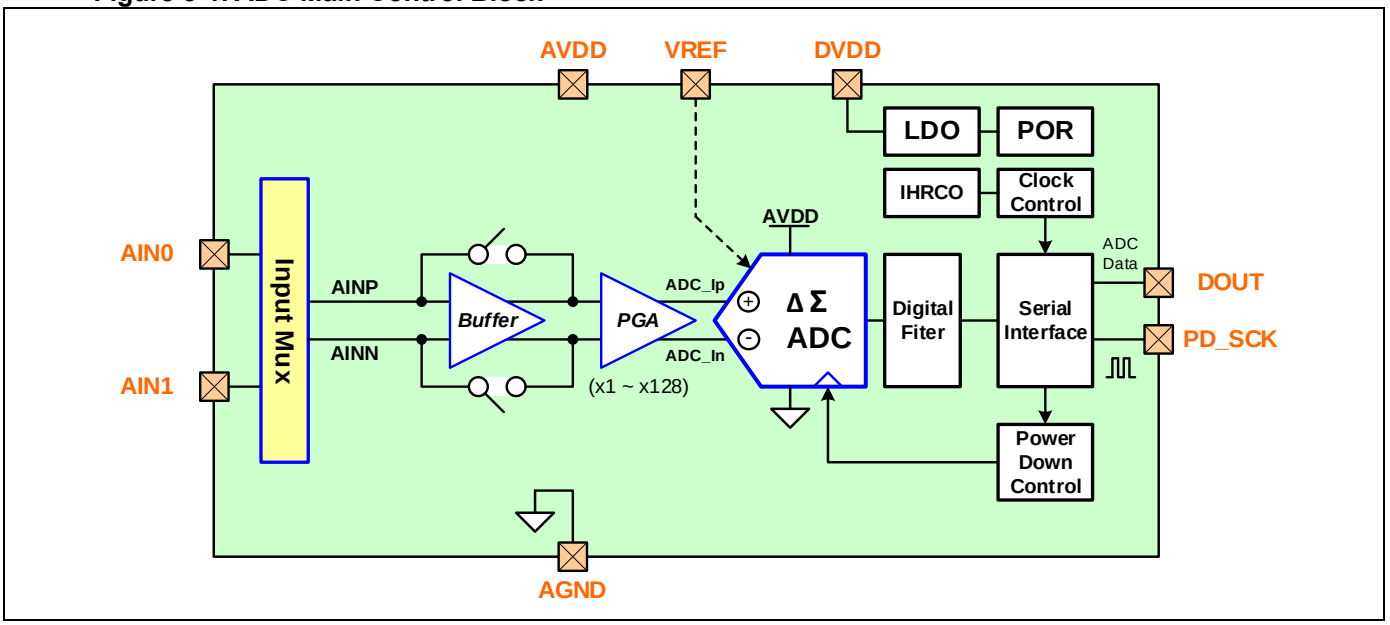
- **Part Number List**
  - **MAD2402AS8 : SOP-8 (150 mil)**
  - **MAD2402AE8 : DIP-8 (300 mil)**

3. Block Diagram

3.1. ADC Main Block

The following figure is showing the ADC control block diagram. It is embedded a precision 24-bit analog-to-digital converter with a 2nd-order delta-sigma (ΔΣ) modulator and a digital filter, analog input multiplexer with two differential inputs, a low-noise input buffer, a low-noise programmable gain amplifier (PGA) and a serial interface control block.

Figure 3-1. ADC Main Control Block

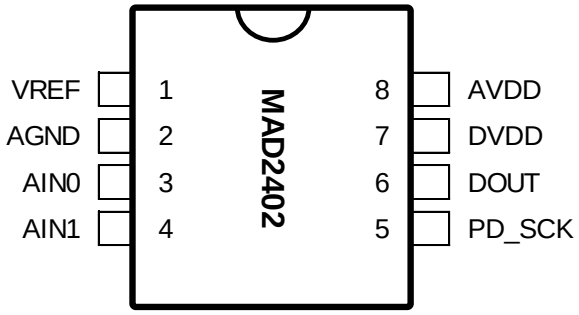


4. Pin Description

4.1. Pin Outline

4.1.1. SOP8/DIP8 Package Pinout

Figure 4-1. SOP8/DIP8 Package Pinout



4.2. Pin Definition

Table 4-1. Abbreviations for pin definition

IO Type		IO Structure	
P	Power/Ground pin	I	Digital Input
B	Bidirectional	P	Output Push-pull capability
I	Input	A	Analog I/O (Digital I/O disable)
O	Output		
A	Analog I/O		

Table 4-2. Pin Descriptions

Pin Name	Pin Number		IO Type	Default		IO Structure	Alternate Functions	Description
	SOP8	DIP8		Type	Value			
AVDD	8	8	P					ADC analog power supply
AGND	2	2	P					ADC analog ground
VREF	1	1	A	A		A		ADC VREF (VREF <= AVDD)
AIN0	3	3	A	A		A		ADC analog input
AIN1	4	4	A	A		A		ADC analog input
DVDD	7	7	P					ADC digital power supply (DVDD >= AVDD)
DOUT	6	6	B	O		I,P		Serial data output
PD_SCK	5	5	I	I		I		Power down control and serial clock input

5. Functional Description

5.1. Serial Interface

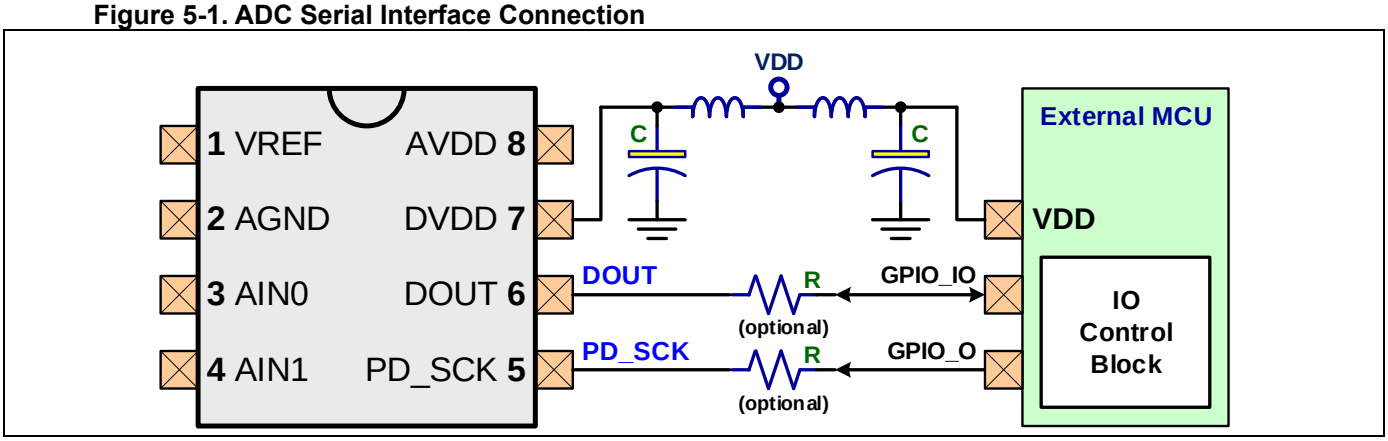
The communication is handled by a 2-wire serial interface to get ADC code and control the ADC settings from external MCU device. There are two pins of **PD_SCK** and **DOUT** those are used for the communication. These two pins are used for data retrieval, input selection, output data rate selection and power down controls.

The chip supports both simple ADC conversion mode by setting **PD_SCK** clock number for user easy control which is maximum 32 clocks and ADC command mode to directly set registers for user configuration.

The ADC serial 24-bit data output is generated from **DOUT** pin when each time the ADC is converted completely and the first data bit is most significant bit. For actual application request, user can enable the internal pull high resister of **DOUT** pin by setting **SADC_DOUT_PU** register through ADC command mode.

The following figure is showing the ADC serial interface connection diagram.

Figure 5-1. ADC Serial Interface Connection



5.2. Power and Reset

5.2.1. Chip Power

The chip power is implemented by separated analog power supply **AVDD** and digital power supply **DVDD**. It is embedded one capless LDO to supply the internal core logic power. The chip supports one power controller to manage power-on reset (POR) circuit, power down control and wakeup control.

The **AVDD** power can be connect to the same power voltage source of external sensor, like as load-cell. The **DVDD** power can be connect to the same power voltage source of external MCU device.

5.2.2. Chip Reset

The chip support multiple reset source those include power-on reset and software reset. During chip reset, all internal registers are set to their initial values. MCU firmware can read the reset events' flag to recognize the reset occurred source through ADC command mode.

The chip is embedded a Power-On Reset (POR) circuits which is always active.

- **Power-On Reset**

There is one PORF (**SADC_PORF**) flag to indicate this reset event source. Power-on reset is generated by internally hardware RC and voltage detection circuits and is no software enable control bit.

The POR circuit will generate the reset signal to reset the chip during chip power up period. When the chip is powered up, the internal RC reset circuit will be active at the voltage threshold about 0.7 volt (variant 0.6~0.8 volt by chip) of DVDD. During power on state, the RC reset circuit needs to be restarted when DVDD power drops below 0.3 volt and powers up again.

- **Software Reset**

User can trigger the chip to restart by the software reset function, which is writing "1" to **SADC_RST_SW** register bit through ADC command mode. There is one SWF (**SADC_SWF**) flag to indicate this reset event

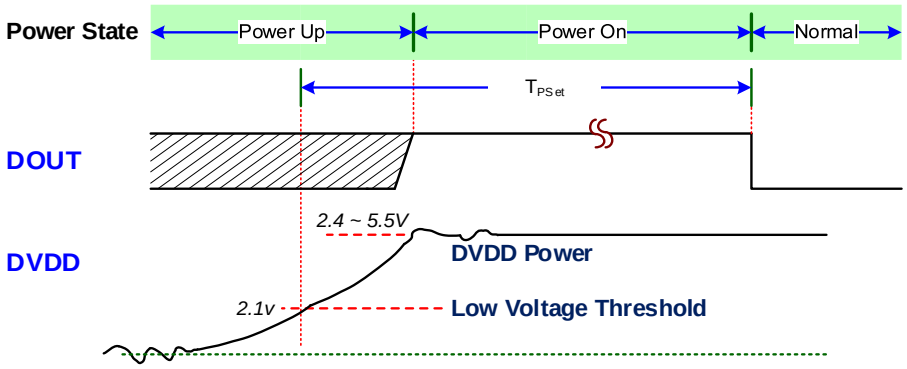
source.

5.2.3. Power-On

When the chip is powered up, the ADC must wait the power-on ADC conversion settling time (T_{PSet} in following timing figure) and ready to doing the first ADC conversion. After the ADC conversion settling time, the chip can use full power to do normally ADC operation.

The following figure is showing the ADC conversion settling time diagram during chip power on. Refer the table of "AC Timing Characteristics" about the AC timing parameters.

Figure 5-2. Power-On ADC Settling Time



<Note> T_{PSet} = Power On ADC conversion settling time

5.2.4. Power-Down and Wakeup Timing

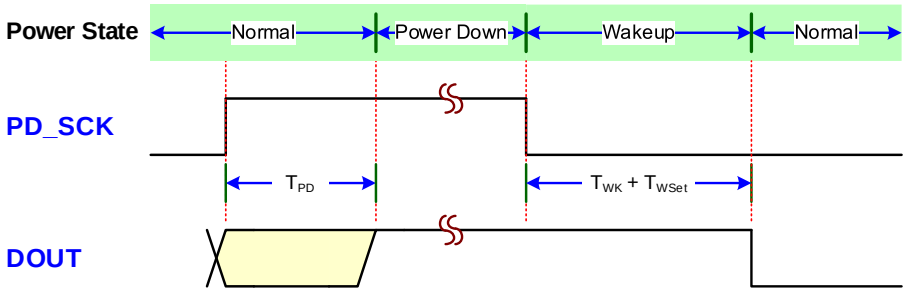
The chip is supported the ***Power Down*** mode to save current consumption. For power management and reset control, the chip is built-in a power supervisor for power down control and wakeup control. When chip is entering ***Power Down*** mode, the chip will be action follows.

1. ADC modulator is disabled.
2. Digital filter is disabled.
3. Internal IHRCO oscillator is power down.
4. POR is operated continuously.

When chip is waked up from ***Power Down*** mode, the internal IHRCO oscillator is active at first. Following, ADC modulator is enabled. Then digital filter is active.

The following figure is showing the power-down and wakeup timing diagram. T_{PD} is ADC Power Down detect time. T_{WK} and T_{WSet} are ADC wakeup time and wakeup ADC conversion settling time. Refer the table of "AC Timing Characteristics" about the AC timing parameters.

Figure 5-3. Power-Down and Wakeup Timing



<Note> T_{PD} = ADC Power Down detect time
T_{WK} = ADC Wakeup time, T_{WSet} = Wakeup ADC conversion settling time

5.3. Clock

5.3.1. Chip Clock

The chip is built-in an embedded IHRCO (internal high frequency RC oscillator). This **CK_IHRCO** clock is used to support ADC with a maximum conversion rate of 1280 SPS. The **CK_IHRCO** clock will be divided by 32*64 to do as the ADC conversion clock source. User can set the ADC conversion rate by setting **SADC_SPS** register through ADC command mode.

The ADC conversion rate is calculate by following formula. **CK_IHRCO** is the IHRCO clock frequency and **OSR** is the ADC data over sampling rate 2 ~ 256.

$$SPS = \frac{CK\_IHRCO}{32 * 64 * OSR}$$

5.4. ADC

5.4.1. Delta-Sigma ADC

The chip is embedded a precision 24-bit analog-to-digital converter and designed to provide high-resolution measurement solutions for the most applications. The converter is implemented a low-noise input buffer, a low-noise programmable gain amplifier (PGA), a 2nd-order delta-sigma (ΔΣ) modulator and a digital filter. It's designed to easy use for weight scales and other applications by connecting directly with the external bridge sensor.

A flexible input multiplexer handles differential signals input. The selectable input buffer can enable to increases the input impedance. User can enable the low-noise input buffer for weak ADC input voltage by setting **SADC_BUF_EN** register through ADC command mode. The PGA provides gains from 1 to 128. Also user can set the PGA gain ratio by setting **SADC_GAIN_PGA** register through ADC command mode. The digital filter can optimize a resolution of up to 24 bits and a data rate of up to 1280 samples per second (SPS).

5.4.2. Analog Mux

The chip is built-in the analog input multiplexers with two external differential inputs, internal DVDD and AGND inputs and VREF voltage source multiplexer. The VREF voltage source multiplexer is one analog multiplexer to select internal ADC voltage reference source which is coming from **VREF** pin or **AVDD** pin input.

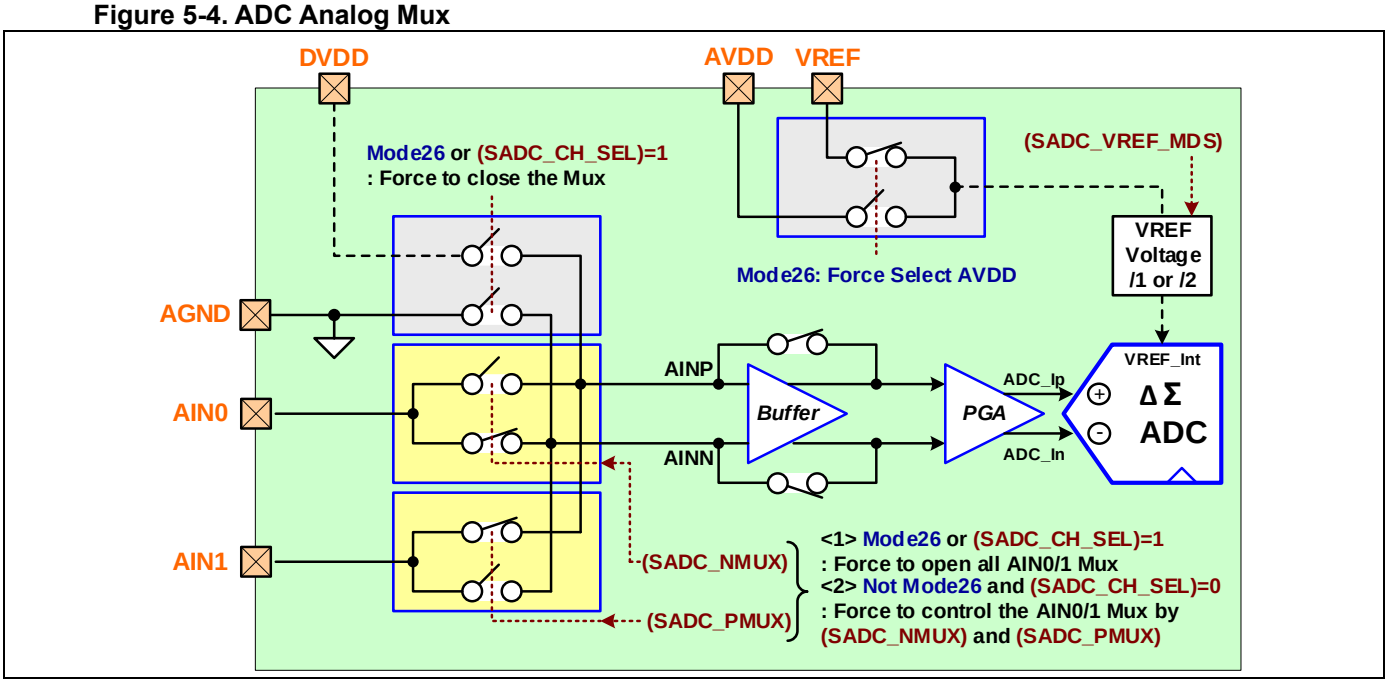
The analog multiplexer selects the inputs to the ADC to be measured in differential mode. When user configures the conversion Mode25 or Mode27, the ADC inputs are coming from external differential input pins of AIN0 and AIN1. Normally, the default ADC analog differential inputs are plus signal inputs from **AIN0** pin and minus signal inputs from **AIN1** pin. Also user can swap the **AIN0** and **AIN1** input signals by setting **SADC_NMUX** and **SADC_PMUX** registers through ADC command mode timing. When user configures the conversion Mode26, the ADC inputs are coming from internal differential input of DVDD divided voltage and AGND voltage. Also the VREF voltage source multiplexer will be selected to AVDD by chip control. Please refer the section of "ADC Conversion Mode Setting" about Mode25, Mode26 and Mode27.

When user configures the user conversion Mode28, the ADC input multiplexers are controlled by internal registers through ADC command mode timing. Please refer the section of "ADC Conversion Mode Setting" about Mode28. The analog input multiplexer is able to select from external pins input of **AIN0** and **AIN1** or internal input of DVDD divided voltage and analog ground by setting **SADC_CH_SEL** register.

The chip is built-in one VREF input voltage divided by 2 function and the chip default is divided by 2. User can set the internal ADC reference voltage divided by 2 or not by setting **SADC_VREF_MDS** register.

The following figure is showing the ADC analog multiplexer block diagram.

Figure 5-4. ADC Analog Mux

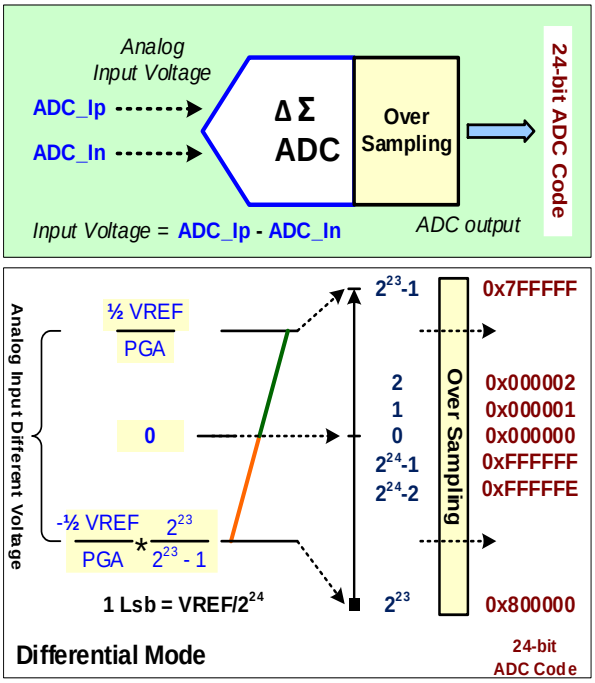


5.4.3. ADC Input Voltage Range

The ADC analog differential input voltage is the delta voltage of pin (**AIN1** - **AIN0**). The ADC output code is 24 bits in binary 2s' complement format. When the input delta voltage is 0 volt, it gets an ADC output code of 0x000000. A positive full-scale input voltage gets an ADC output code of 0x7FFFFF and the negative full-scale input voltage gets an ADC output code of 0x800000.

The following figure is showing the ADC analog differential input voltage range diagram.

Figure 5-5. ADC Input Voltage Range



The following formulas are listed the ADC full scale range (FSR) and analog input voltage range.

Full Scale Range

$$FSR = \frac{VREF * K}{PGA}$$

Input Range

$$\frac{0.5*K*VREF}{PGA} \sim \frac{-0.5*K*VREF}{PGA} * \frac{2^{23}}{2^{23} - 1}$$

VREF: ADC reference voltage from **VREF** pin

PGA: PGA gain ratio

K: =1 if (**SADC_VREF_MDS** register=0, default); =2 if (**SADC_VREF_MDS** register=1)

5.4.4. ADC Output Code

The ADC can convert the analog differential input voltage from **AIN0** and **AIN1** pins and output ADC 24-bit binary code to **DOUT** pin. Also the chip can measure **DVDD** and **AVDD** supply voltage difference by setting ADC conversion mode. User can calculate ADC conversion output code by following formulas.

ADC Output Code

$$BCD = \frac{VIN * PGA * (2^{23}-1)}{VREF * 0.5 * K}$$

DVDD-AVDD Output Code

$$BCD = \frac{DVDD * 3.2 * (2^{24}-1)}{59.2 * AVDD}$$

VIN: analog input differential (**AIN1** - **AIN0**) voltage

VREF: ADC reference voltage from **VREF** pin

PGA: PGA gain ratio

K: =1 if (**SADC_VREF_MDS** register=0, default); =2 if (**SADC_VREF_MDS** register=1)

5.4.5. ADC ENOB and Noise Free Bits

The following formulas are used to calculate the ADC Effective-Number-of-Bits (ENOB) and Noise-Free Bits (NFB).

ENOB

$$ENOB = \frac{\ln(FSR / RMS\ Noise)}{\ln(2)}$$

Noise Free Bits

$$Bits = \frac{\ln(FSR / P\text{-}P\ Noise)}{\ln(2)}$$

FSR: ADC full scale range

P-P Noise: Peak-to-Peak noise

The RMS noise and Peak-to-Peak noise can be calculated in following formulas.

Noise (Voltage)

$$RMS\ Noise = \frac{P\text{-}P\ Noise}{6.6}$$

P-P (Peak-to-Peak) Noise = $(V_{Max} - V_{Min}) / PGA$

5.5. Simple ADC Conversion Mode

The chip supports simple ADC conversion mode by setting **PD_SCK** clock number for user easy control which is maximum 32 clocks.

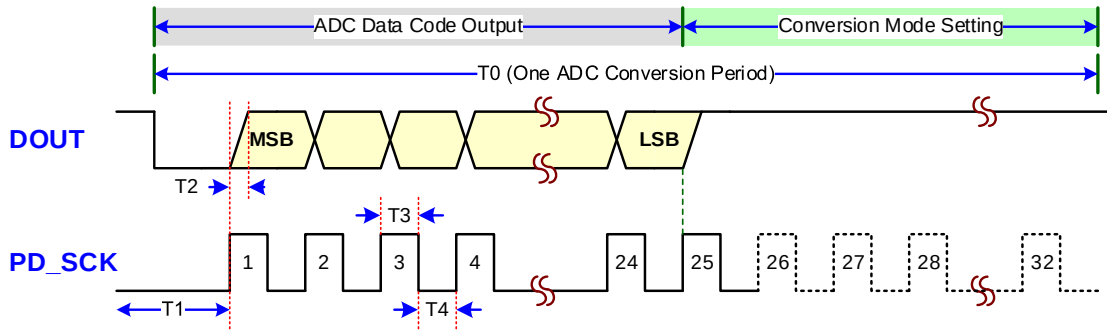
5.5.1. ADC Conversion

The chip is automatically to convert the ADC analog input voltage from **AIN0** and **AIN1** pins. After the ADC conversion is complete, the ADC will output the serial bits of ADC code to **DOUT** pin when the ADC data shift clock is receiving from **PD_SCK** pin.

The ADC serial 24-bit data output is generated from on **DOUT** pin when each time the ADC is converted completely and the first data bit is most significant bit.

The following figure is showing the ADC conversion data output timing diagram. Refer the table of "AC Timing Characteristics" about the AC timing parameters.

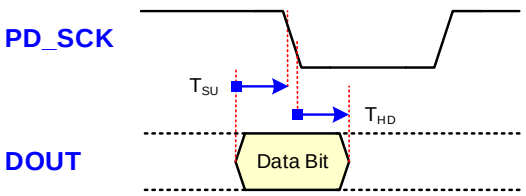
Figure 5-6. ADC Conversion Data Output Timing



<Note> T0 = ADC conversion mode settling time = Previous setting "One ADC Conversion Period"
(For example previous setting is 10 SPS, T0 is equal 100ms.)
T1 = Data ready DOUT falling edge to PD_SCK rising edge, T2 = PD_SCK rising edge to DOUT data ready
T3 = PD_SCK high time, T4 = PD_SCK low time

The following figure is showing the ADC data output setup time and hold time timing for **DOUT** signal. Refer the table of "AC Timing Characteristics" about the AC timing parameters.

Figure 5-7. ADC DOUT Setup Time and Hold Time Timing



<Note> T_{SU} = ADC Data setup time
T_{HD} = ADC Data hold time

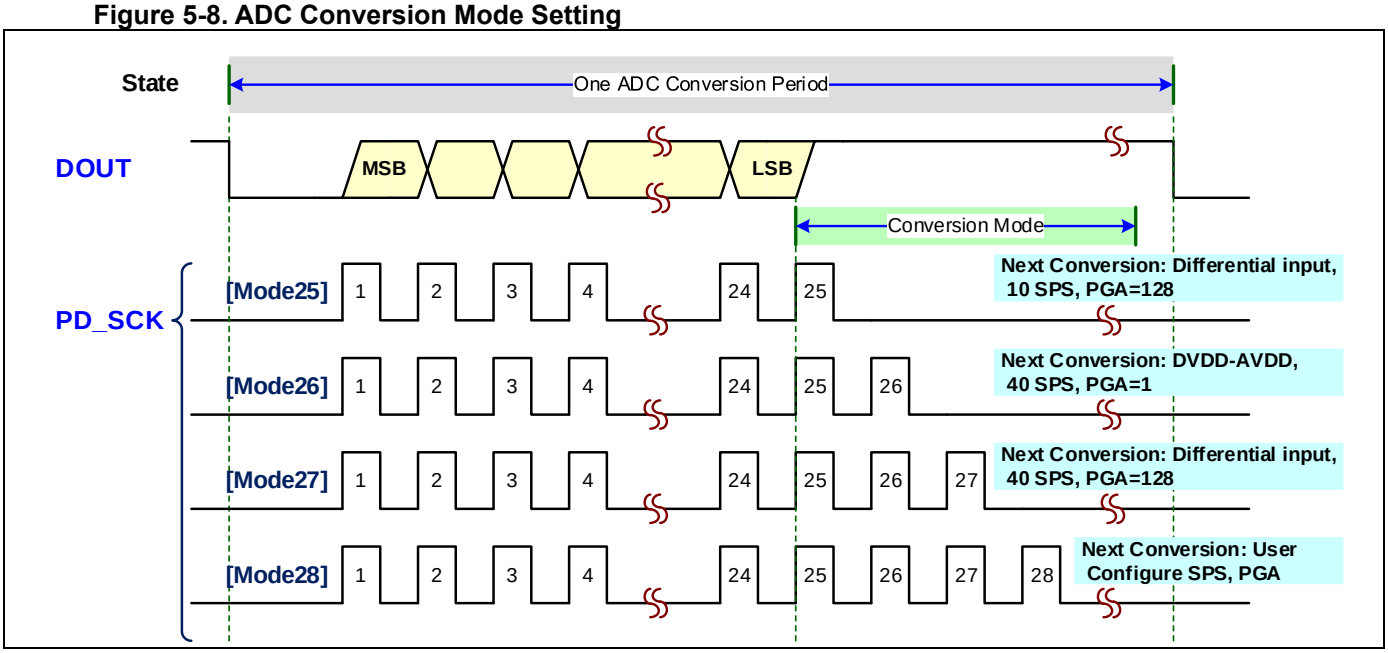
5.5.2. ADC Conversion Mode Setting

There is no programming needed for the internal registers to operate three designed fixed ADC conversion modes (Mode25, Mode26, Mode27) by setting the fixed 25, 26 and 27 of clock number of **PD_SCK** in one previous ADC conversion period. When the clock number is 25, the ADC conversion mode is set 10 SPS with PGA 128. When the clock number is 27, the ADC conversion mode is set 40 SPS with PGA 128. When the clock number is 26, the ADC conversion mode is set 40 SPS for DVDD and AVDD supply voltage difference measurement. It must be notice that the first ADC conversion data needs to be skipped after changing conversion mode. Please refer the section of "Analog Mux" about more information of analog multiplexer control for Mode25, Mode26 and Mode27.

Specially, the chip supports one user configure conversion mode (Mode28) which the clock number of **PD_SCK** must be set between 28 and 32.

The following figure is showing the ADC conversion mode setting timing diagram.

Figure 5-8. ADC Conversion Mode Setting

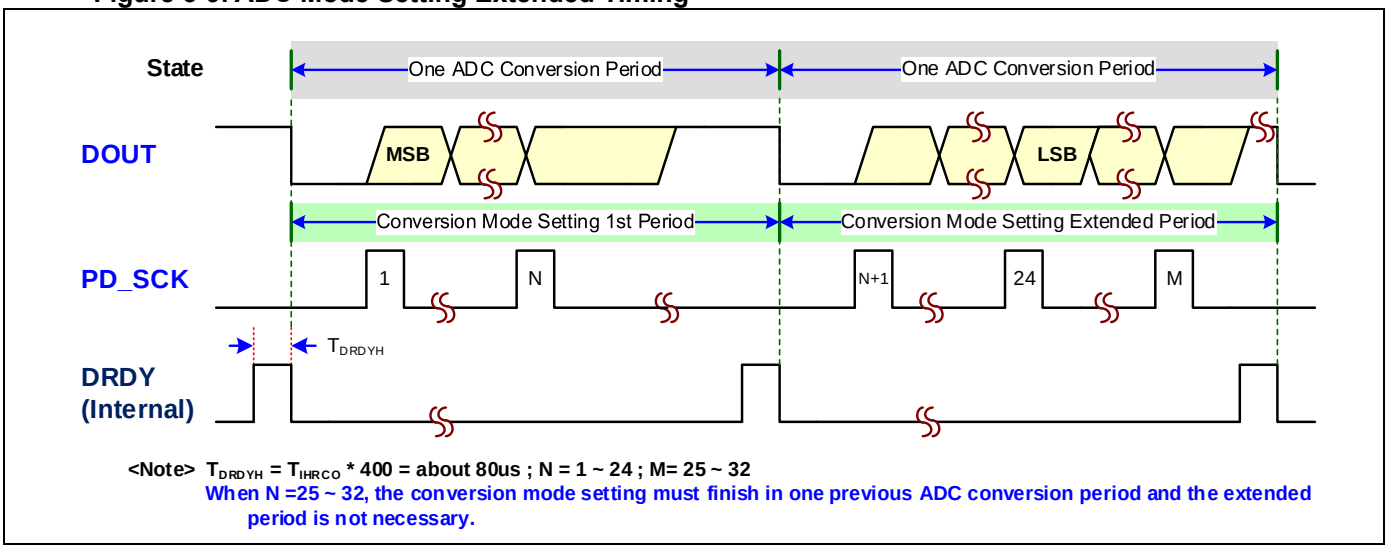


For external MCU firmware control issues, sometime the ADC mode setting does not finish in one previous ADC conversion period. Then user can separate to two mode setting periods. The clock number of **PD_SCK** must be less than 25 for the first mode setting period. The second mode setting period is the extended mode setting period which user can set the remained clocks of **PD_SCK** to get ADC data bits or set ADC conversion mode.

When the total clock number of ADC conversion mode setting is between 25 and 32, the conversion mode setting must finish in one previous ADC conversion period and the extended period is not necessary.

The following figure is showing the ADC mode setting extended timing.

Figure 5-9. ADC Mode Setting Extended Timing



<Note> $T_{DRDYH} = T_{IHRCO} * 400$ = about 80us ; N = 1 ~ 24 ; M= 25 ~ 32
When N =25 ~ 32, the conversion mode setting must finish in one previous ADC conversion period and the extended period is not necessary.

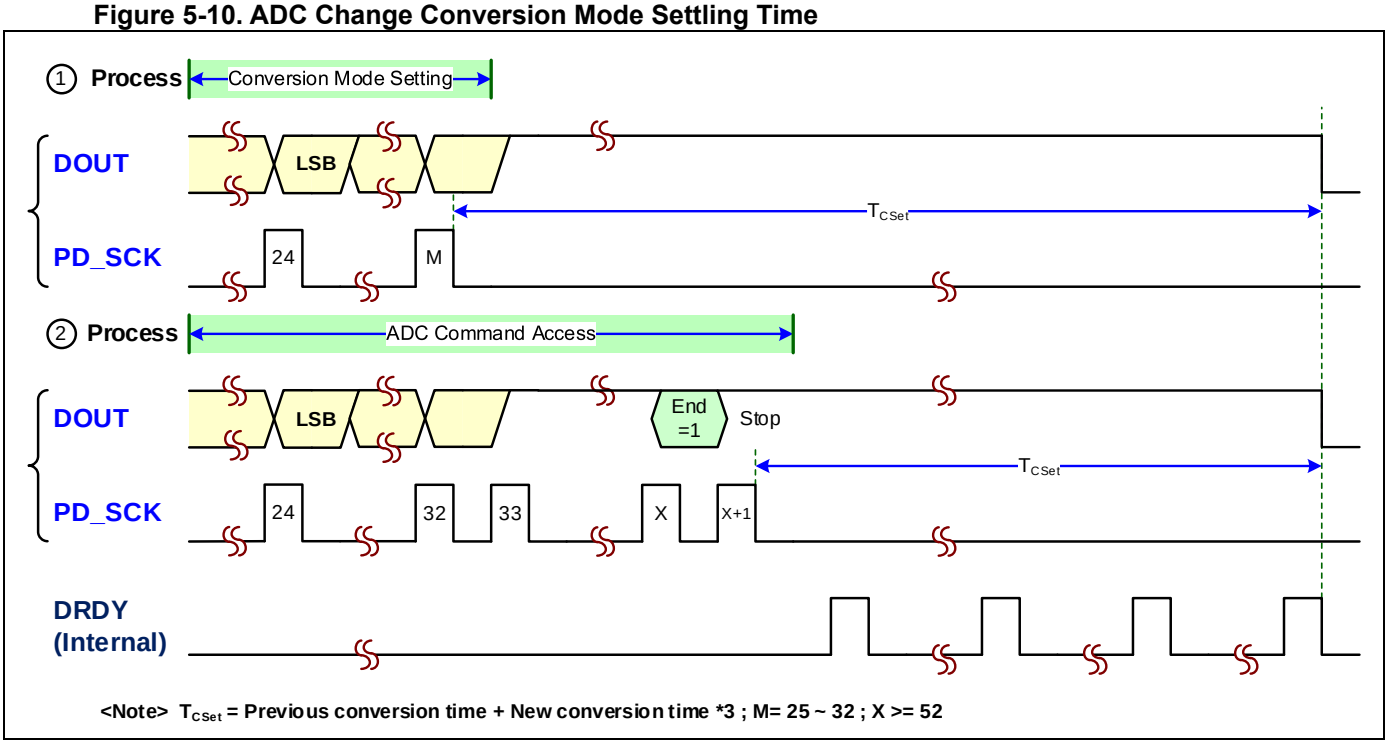
5.5.3. ADC Change Conversion Mode Settling Time

After the ADC conversion rate, PGA gain ratio or analog input selection are changed by simple ADC conversion mode or ADC command mode setting, the next ADC conversion must be normal and ready with a settling time (T_{CSet} in following timing figure). For application, suggest to skip the front of 3 ADC conversion

samples.

The following figure is showing the ADC change conversion mode settling time timing. Refer the table of "AC Timing Characteristics" about the AC timing parameters.

Figure 5-10. ADC Change Conversion Mode Settling Time



<Note> T_{CSet} = Previous conversion time + New conversion time *3 ; M= 25 ~ 32 ; X >= 52

5.5.4. ADC User Configure Conversion Mode

Specially, the chip supports one user configure conversion mode (Mode28) which the clock number of **PD_SCK** must be set between 28 and 32. At first, user must configure the user configure conversion mode through ADC command mode timing to set the internal registers. And user can run the new user configure conversion mode (Mode28) through the ADC conversion mode timing to get new ADC data.

The chip will record these register setting for the user configure conversion mode and does not destroy until next time the related setting register is updated by ADC command mode.

User can set and record the ADC conversion rate in **SADC_SPS** register, PGA gain ratio in **SADC_GAIN_PGA** register and ADC input multiplexer internal or external selection in **SADC_CH_SEL** register.

5.6. ADC Command Mode

The chip supports both simple ADC conversion mode by setting **PD_SCK** clock number and ADC command mode for register access. User can directly set the registers for user configuration.

5.6.1. ADC Command Mode Timing

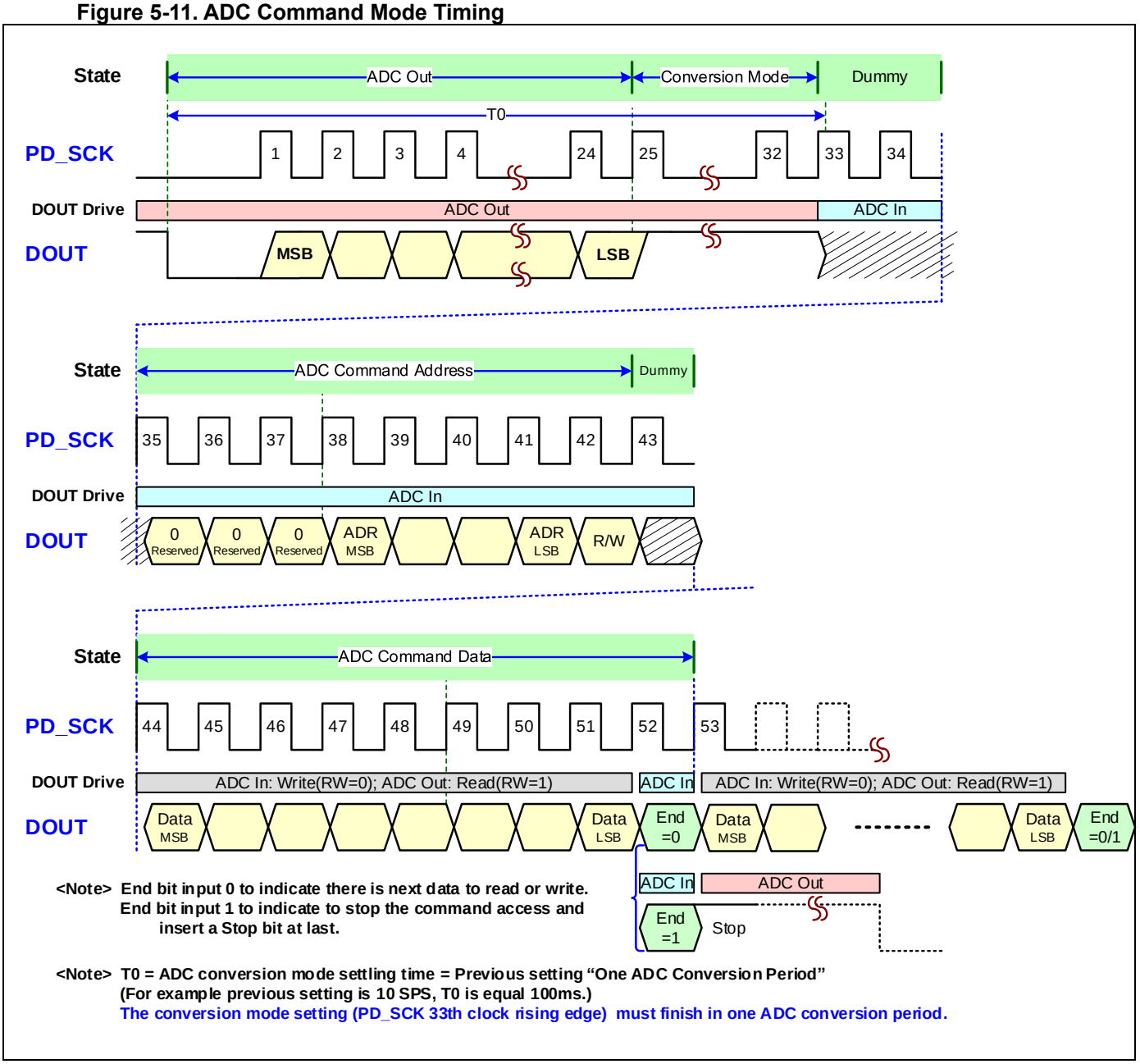
The chip supports simple ADC conversion mode by setting **PD_SCK** clock number which is maximum 32 clocks. When the clock number is over 32, the chip will escape the simple ADC conversion mode. When the chip detects the clock number 35th, the chip is entering ADC command mode.

At first, the period of clock number 38th to 41th is used to set the register address. The clock number 42th is used to set read or write for register access. Following, the period of clock number 44th to 51th is used as access 8-bit register data.

At last, the clock number 52th is end bit. If the end is 1, it indicates that the register access procedure is complete and MCU needs to send the 53th clock to end for hardware request. If the end is 0, it indicates that the register access procedure is continuous with next 8-bit data. Following the 8-bit data is next end bit and use this end bit to decide that the register access procedure is end or continuous again.

The following figure is showing the ADC command mode timing.

Figure 5-11. ADC Command Mode Timing



<Note> End bit input 0 to indicate there is next data to read or write.
End bit input 1 to indicate to stop the command access and insert a Stop bit at last.

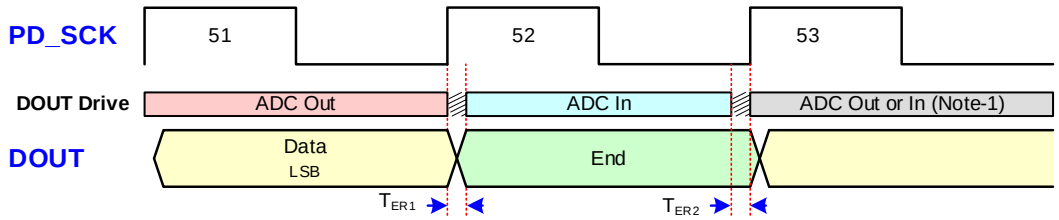
<Note> T0 = ADC conversion mode settling time = Previous setting "One ADC Conversion Period"
(For example previous setting is 10 SPS, T0 is equal 100ms.)
The conversion mode setting (PD_SCK 33th clock rising edge) must finish in one ADC conversion period.

5.6.2. End Bit Timing

For the ADC command mode, the end bit is driving by external MCU on **DOUT** signal. If the ADC command procedure is read access and previous bit of end bit is driving by ADC chip, MCU must delay a time of T_{ER1} to drive the end bit from the rising edge of end bit clock on **PD_SCK** signal. If the ADC command procedure is read access and the end bit is 0 to process continuously with next register, MCU must release the signal early with a time of T_{ER2} from the rising edge of next clock of end bit on **PD_SCK** signal.

The following figure is showing the ADC change conversion mode settling time timing. Refer the table of "AC Timing Characteristics" about the AC timing parameters.

Figure 5-12. ADC End Bit Timing



<Note-1> (1) When End bit is inputted 0, it indicates there is next data to read or write.
DOUT is outputted or inputted by previous R/W bit setting of ADC command address.
(2) When End bit is inputted 1, it indicates to stop the command access.
DOUT is inputted.

<Note-2> T_{ER1} , T_{ER2} = DOUT End bit released time by ADC, External MCU

6. Function Registers

6.1. SADC Control Registers

SADC Control	(SADC) Delta-Sigma ADC Control Module
Base Address :	0x5B040000

6.1.1. SADC status register

SADC_STA	SADC status register		
Offset Address :	0x00	Reset Value :	0x23

7	6	5	4	3	2	1	0
SADC_ID[3:0]				SADC_DRDYF	SADC_SWF	Reserved	SADC_PORF

Bit	Attr	Bit Name	Description	Reset
7..4	r	SADC_ID	ADC version ID. It is fixed 0x02.	0x02
3	r	SADC_DRDYF	ADC data ready output status. 0 = No : data not ready 1 = Ready : data ready	0x00
2	rw	SADC_SWF	Software forced reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
1	-	Reserved	Reserved	0x01
0	rw	SADC_PORF	Power-on reset flag. Software write 1 to clear and is no effect by writing 0. This bit reset by POR reset and set after POR reset. 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x01

6.1.2. SADC input channel multiplexer register

SADC_MUX	SADC input channel multiplexer register		
Offset Address :	0x01	Reset Value :	0x10

7	6	5	4	3	2	1	0
SADC_CH_SEL	Reserved		SADC_PMUX	Reserved			SADC_NMUX

Bit	Attr	Bit Name	Description	Reset
7	rw	SADC_CH_SEL	ADC input channel Mux external or internal channel selection. When selects EXT, the input Mux is mapping to external channel. When selects INT, the input Mux is mapping to internal DVDD-AVDD channel. 0 = EXT : external channel 1 = INT : internal channel	0x00
6..5	-	Reserved	Reserved	0x00
4	rw	SADC_PMUX	ADC positive-ended input channel Mux selection. 0x0 = AIN0 0x1 = AIN1	0x01
3..1	-	Reserved	Reserved	0x00
0	rw	SADC_NMUX	ADC negative-ended input channel Mux selection. 0x0 = AIN0 0x1 = AIN1	0x00

6.1.3. SADC control register 0

SADC_CR0	SADC control register 0		
Offset Address :	0x02	Reset Value :	0x40

7	6	5	4	3	2	1	0
Reserved	Reserved			Reserved	SADC_DOUT_PU	SADC_BUF_EN	Reserved

Bit	Attr	Bit Name	Description	Reset
7	-	Reserved	Reserved	0x00
6..4	-	Reserved	These bits are for internal using, it must be 0x04.	0x04
3	-	Reserved	Reserved	0x00
2	rw	SADC_DOUT_PU	DOUT pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
1	rw	SADC_BUF_EN	ADC input buffer enable. 0 = Disable 1 = Enable	0x00
0	-	Reserved	Reserved	0x00

6.1.4. SADC control register 1

SADC_CR1	SADC control register 1		
Offset Address :	0x03	Reset Value :	0x70

7	6	5	4	3	2	1	0
Reserved	SADC_GAIN_PGA[2:0]			Reserved	SADC_SPS[2:0]		

Bit	Attr	Bit Name	Description	Reset
7	-	Reserved	Reserved	0x00
6..4	rw	SADC_GAIN_PGA	ADC input PGA gain adjust bits. 0x0 = X1 : multiplied by 1 0x1 = X2 : multiplied by 2 0x2 = X4 : multiplied by 4 0x3 = X8 : multiplied by 8 0x4 = X16 : multiplied by 16 0x5 = X32 : multiplied by 32 0x6 = X64 : multiplied by 64 0x7 = X128 : multiplied by 128	0x07
3	-	Reserved	Reserved	0x00
2..0	rw	SADC_SPS	ADC data output sampling rate per second select. 0x0 = SPS10 : SPS 10Hz 0x1 = SPS20 : SPS 20Hz 0x2 = SPS40 : SPS 40Hz 0x3 = SPS80 : SPS 80Hz 0x4 = SPS160 : SPS 160Hz 0x5 = SPS320 : SPS 320Hz 0x6 = SPS640 : SPS 640Hz 0x7 = SPS1280 : SPS 1280Hz	0x00

6.1.5. SADC control register 2

SADC_CR2	SADC control register 2		
Offset Address :	0x04	Reset Value :	0x30

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SADC_SHORT_EN

Bit	Attr	Bit Name	Description	Reset
7	-	Reserved	Reserved	0x00
6	-	Reserved	This bit is for internal using, it must be 0x00.	0x00
5	-	Reserved	This bit is for internal using, it must be 0x01.	0x01
4	-	Reserved	This bit is for internal using, it must be 0x01.	0x01
3	-	Reserved	This bit is for internal using, it must be 0x00.	0x00
2	-	Reserved	Reserved	0x00
1	-	Reserved	Reserved	0x00
0	rw	SADC_SHORT_EN	ADC input shorting to common voltage enable. 0 = Disable 1 = Enable	0x00

6.1.6. SADC control register 3

SADC_CR3	SADC control register 3		
Offset Address :	0x05	Reset Value :	0x00

7	6	5	4	3	2	1	0
Reserved			Reserved	Reserved		SADC_VREF_MDS	Reserved

Bit	Attr	Bit Name	Description	Reset
7..5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	SADC_VREF_MDS	ADC internal VREF mode selection. When selects 'Normal', the ADC internal VREF input voltage will be divided by 2. When selects 'X1', the ADC internal VREF input voltage will be not divided. 0 = Normal 1 = X1 : internal VREF input	0x00
0	-	Reserved	Reserved	0x00

6.1.7. SADC reset control register

SADC_RST	SADC reset control register		
Offset Address :	0x0F	Reset Value :	0x00

7	6	5	4	3	2	1	0
Reserved						SADC_RST_SW	Reserved

Bit	Attr	Bit Name	Description	Reset
7..2	-	Reserved	Reserved	0x00
1	rw	SADC_RST_SW	System software forced reset enable for whole chip reset 0 = No operation 1 = Generate reset	0x00
0	-	Reserved	Reserved	0x00

7. Application Notes

7.1. ADC Application Circuit

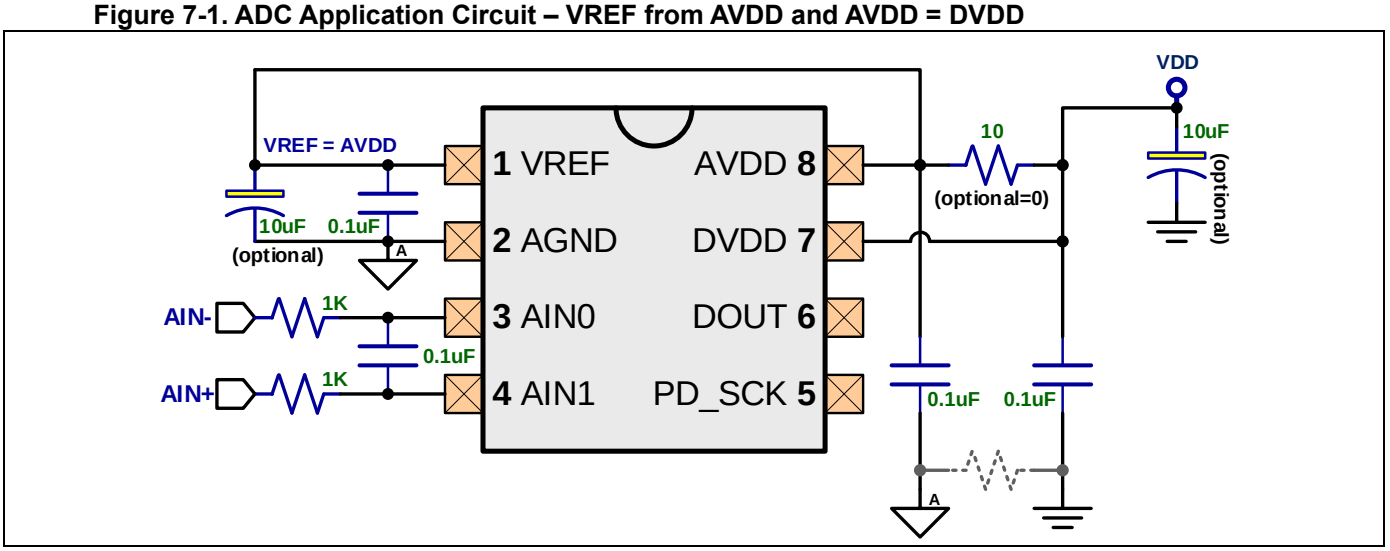
The ADC reference voltage source can be from (1) VDD power by connecting **VREF** pin to **AVDD** pin directly (2) external quiet reference voltage source. Suggests to separate analog and digital ground areas on PCB to reduce the digital signals' interference to analog ADC. User can connect these two ground areas through a resister or a ferrite bead. Please place the related components of **VREF**, **AVDD**, **AIN0** and **AIN1** pins on analog ground area. Please place the related components of **DVDD**, **PD_SCK** and **DOUT** pins on digital ground area.

7.1.1. Use AVDD as Reference Voltage

When uses the VDD power as the ADC reference voltage, it must connect **VREF** pin trace to the point which is at current flow behind the power capacitor(s).

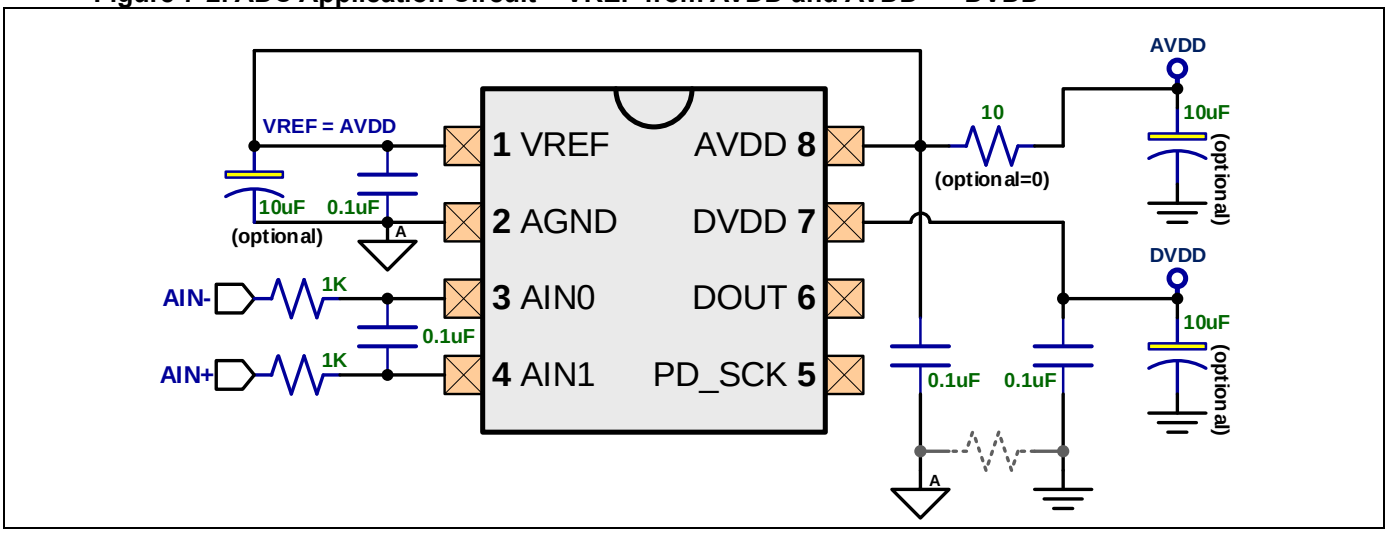
The following figure is showing the ADC application circuit when VREF voltage is directly coming from AVDD. AVDD voltage is coming from DVDD by through a ferrite bead or resister.

Figure 7-1. ADC Application Circuit – VREF from AVDD and AVDD = DVDD



The following figure is showing the ADC application circuit when VREF voltage is directly coming from AVDD. AVDD voltage and DVDD voltage can come from independent voltage source.

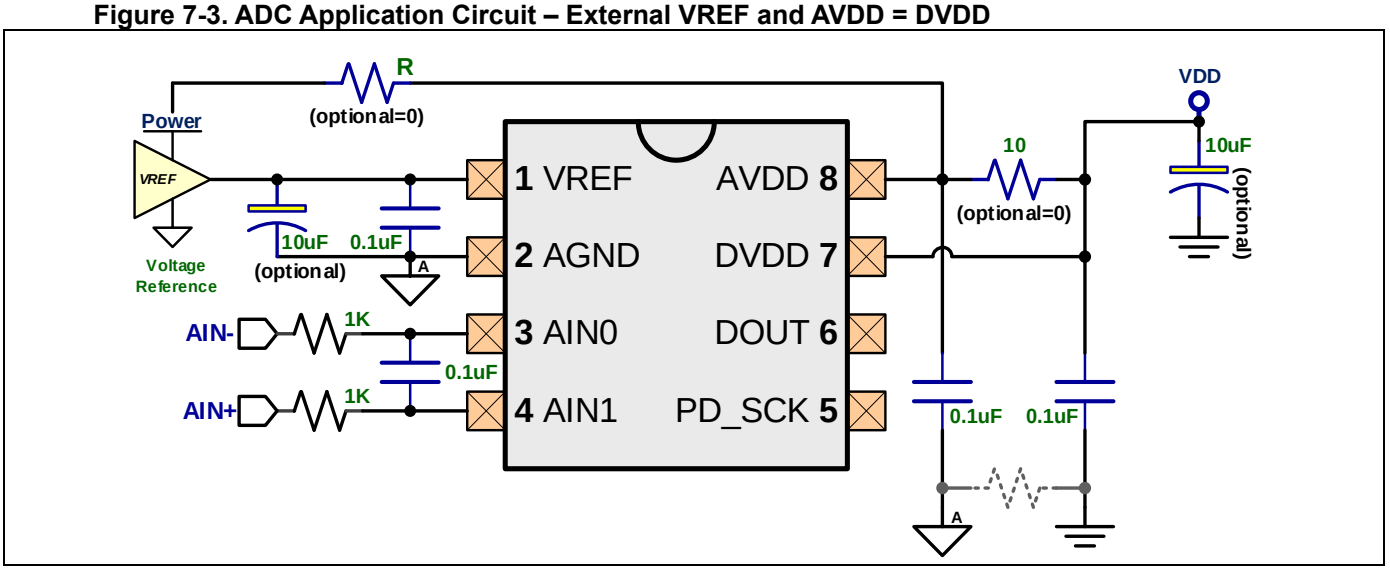
Figure 7-2. ADC Application Circuit – VREF from AVDD and AVDD <= DVDD



7.1.2. Use External Reference Voltage Device

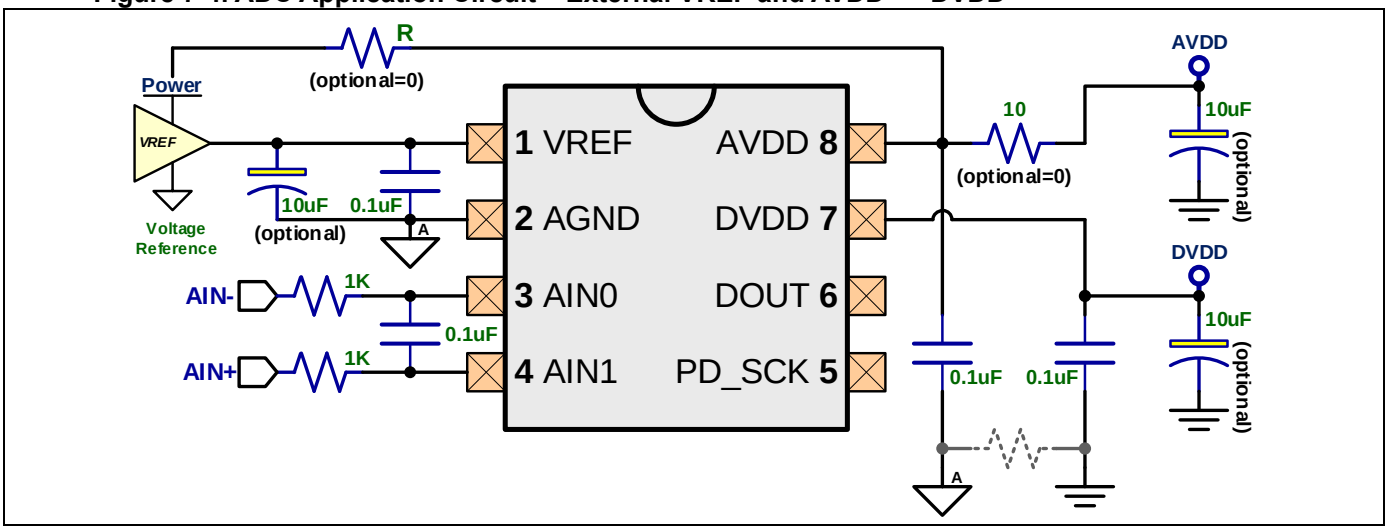
When uses the external quiet reference voltage source as the ADC reference voltage, it must add some bypass and decoupling capacitors, as shown in following figure. AVDD voltage is coming from DVDD by through a ferrite bead or resister.

Figure 7-3. ADC Application Circuit – External VREF and AVDD = DVDD



The following figure is showing the ADC application circuit when VREF voltage is coming from external voltage reference source. AVDD voltage and DVDD voltage can come from independent voltage source.

Figure 7-4. ADC Application Circuit – External VREF and AVDD <= DVDD



8. Electrical Characteristics

8.1. Parameter Glossary

Table 8-1. Parameter Glossary

Symbol	Definition	Descriptions
Abbreviations for electrical characteristics		
Min	Minimum value	Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value.
Max	Maximum value	Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value.
Typ	Typical value	Unless otherwise specified, the value is based on TA=25 °C, AVDD=DVDD=5V.
AVDD DVDD	Power supply voltage	The voltage range is specified in characteristics table or conditions column.
AGND	Power reference voltage	Unless otherwise specified, all voltages are referred to AGND.
TA	Ambient temperature	The temperature range is specified in characteristics table or conditions column.

8.2. Absolute Maximum Rating

Table 8-2. Absolute Maximum Rating

Parameter	Rating	Unit
Ambient temperature under bias	-40 ~ +105	**°C**
Storage temperature	-65 ~ + 150	**°C**
Voltage on any Port I/O Pin or RST with respect to AGND	-0.5 ~ DVDD + 0.5	**Volt**
Voltage on DVDD with respect to AGND	-0.5 ~ +6.0	**Volt**
Maximum output current sunk by any I/O pin	10	**mA**

Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

8.3. ADC Characteristics

Table 8-3. ADC Characteristics

DVDD=5.0V±10%, AVDD=5.0V±10%<=DVDD, VREF=AVDD, AGND=0V, TA = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
AVDD	Analog Supply Voltage		2.5		5.5	Volt
DVDD	Digital Supply Voltage		2.5		5.5	Volt
TEMP	Operation Temperature		-40		85	°C
ADC Parameters						
Bits	Output Resolution			24		bits
F_{Conv}	Output Conversion Rate		10		1280	SPS
PGain	PGA Gain Ratio		1		128	.
V_{REF}	Reference Input Voltage		1.8		AVDD	Volt
V_{Diff}	Full Scale Differential Input Range	AIN1-AIN0 voltage	-VREF /(2*PGA)		+VREF /(2 *PGA)	Volt
V_{CM}	Common Mode Input Range (Absolute Input Range)	Buffer Off, PGA=128	AGND+0.1		AVDD-1	Volt
		Buffer On, PGA=128	AGND+0.1		AVDD-1.5	Volt
R_{InDiff}	Input Resistance for differential input	Buffer Off		150K		Ohm
		Buffer On		100M		Ohm
ENOB	Effective Number Of Bits	10 SPS, PGA=128		17.0		bits
		40 SPS, PGA=128		16.5		bits
NFB	Noise-Free Bits	10 SPS, PGA=128		14.3		bits
		40 SPS, PGA=128		13.8		bits
INL	Integral nonlinearity (INL)			1.5		LSB
Current Consumption						
I_{AVDD}	Analog Current	10 SPS, PGA =128		560		uA
		10 SPS, PGA =1		130		uA
		Power-Down Mode		0.08		uA
I_{DVDD}	Digital Current	10 SPS, PGA =128		275		uA
		10 SPS, PGA =1		275		uA
		Power-Down Mode		9.3		uA
IO Characteristics						
V_{IH}	Input High voltage (DOUT)	DVDD =5.0V		1.82		Volt
		DVDD =3.3V		1.29		Volt
	Input High voltage (PD_SCK)	DVDD =5.0V		2.21		Volt
		DVDD =3.3V		1.60		Volt
V_{IL}	Input Low voltage (DOUT)	DVDD =5.0V		1.74		Volt
		DVDD =3.3V		1.25		Volt
	Input High voltage (PD_SCK)	DVDD =5.0V		1.34		Volt
		DVDD =3.3V		0.98		Volt
I_{OH}	Output High current (DOUT)	DVDD =5.0V, V_{PIN} = 2.4V		18.40		mA
		DVDD =3.3V, V_{PIN} = 2.4V		5.90		mA
I_{OL}	Output Low current (DOUT)	DVDD =5.0V, V_{PIN} = 0.4V		9.10		mA
		DVDD =3.3V, V_{PIN} = 0.4V		6.60		mA
TR1	IO rising time (DOUT)	DVDD =5.0V, C load=30pF		25.4		ns
		DVDD =3.3V, C		31.6		ns

		load=30pF				
TF1	IO falling time (DOUT)	DVDD =5.0V, C load=30pF		7.5		ns
		DVDD =3.3V, C load=30pF		11.1		ns
R_{PU}	IO pin pull-high resistance (DOUT)	DVDD =5.0V		93.6		Kohm
		DVDD =3.3V		157.6		Kohm

8.4. AC Timing Characteristics

Table 8-4. AC Timing Characteristics

DVDD=5.0V±10%, AGND=0V, TA = 25°C (unless otherwise specified)

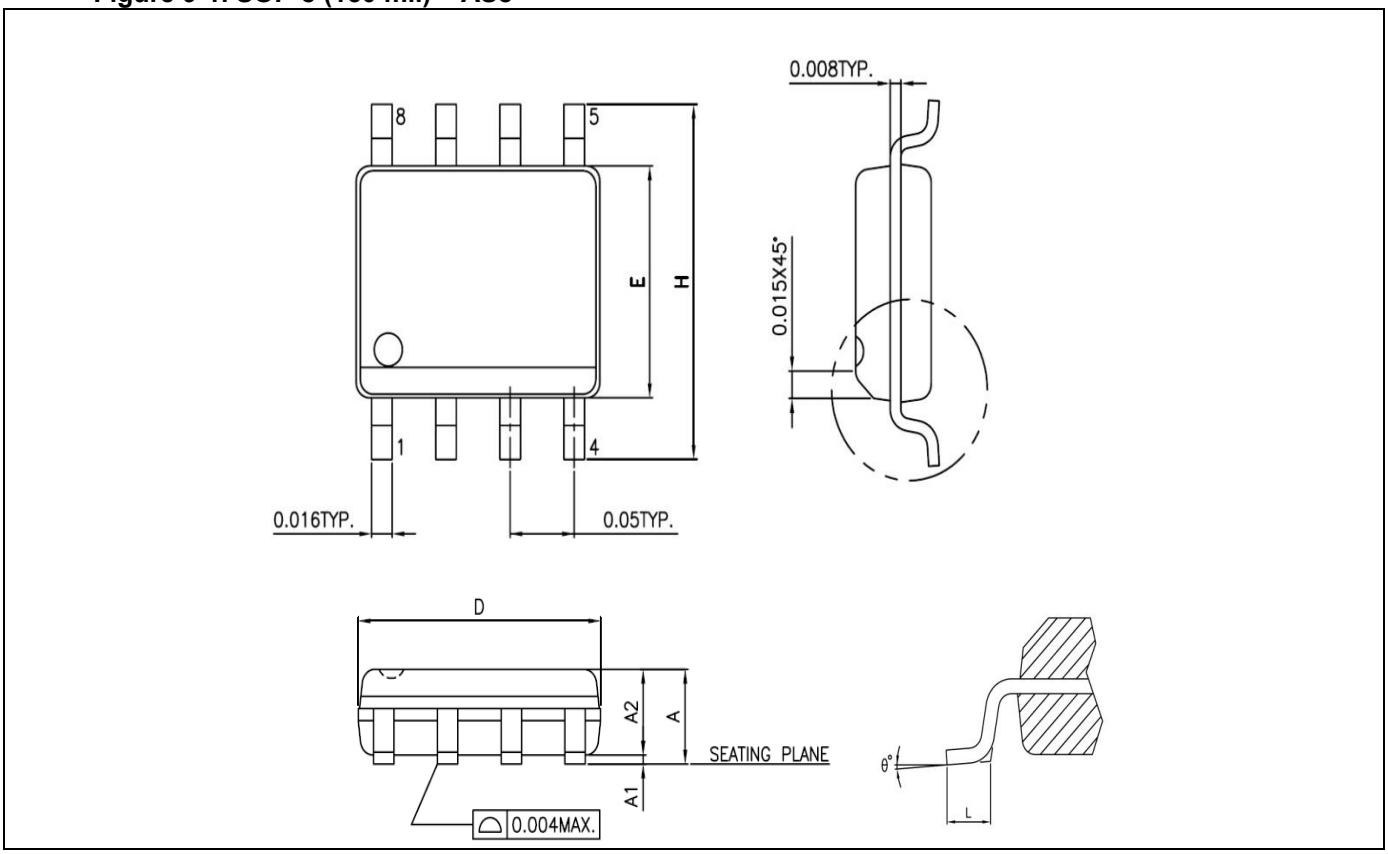
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
ADC Data Output						
T0	ADC conversion mode settling time				1	T_{Conv}
T1	Data ready DOUT falling edge to PD_SCK rising edge		0.1			us
T2	PD_SCK rising edge to DOUT data ready				0.1	us
T3	PD_SCK high time		0.2	1	50	us
T4	PD_SCK low time		0.2	1		us
T_{SU}	ADC Data setup time		40			ns
T_{HD}	ADC Data hold time		40			ns
T_{CSet}	Change Mode ADC conversion settling time				Tp + Tn*3	
ADC Power On						
T_{PSet}	Power On ADC conversion settling time (Time start from DVDD >2.1V to ADC conversion ready)		305			ms
Power Down and Wakeup						
T_{PD}	ADC Power Down detect time		60			us
T_{WK}	ADC Wakeup time			10		ms
T_{WSet}	Wakeup ADC conversion settling time		3			T_{Conv}
ADC Command Mode						
T_{ER1}	DOUT End bit released time by ADC		40			ns
T_{ER2}	DOUT End bit released time by external MCU		40			ns

T_{Conv} : ADC conversion time, Tp: Previous conversion time, Tn: New conversion time

9. Package Dimension

9.1. SOP-8

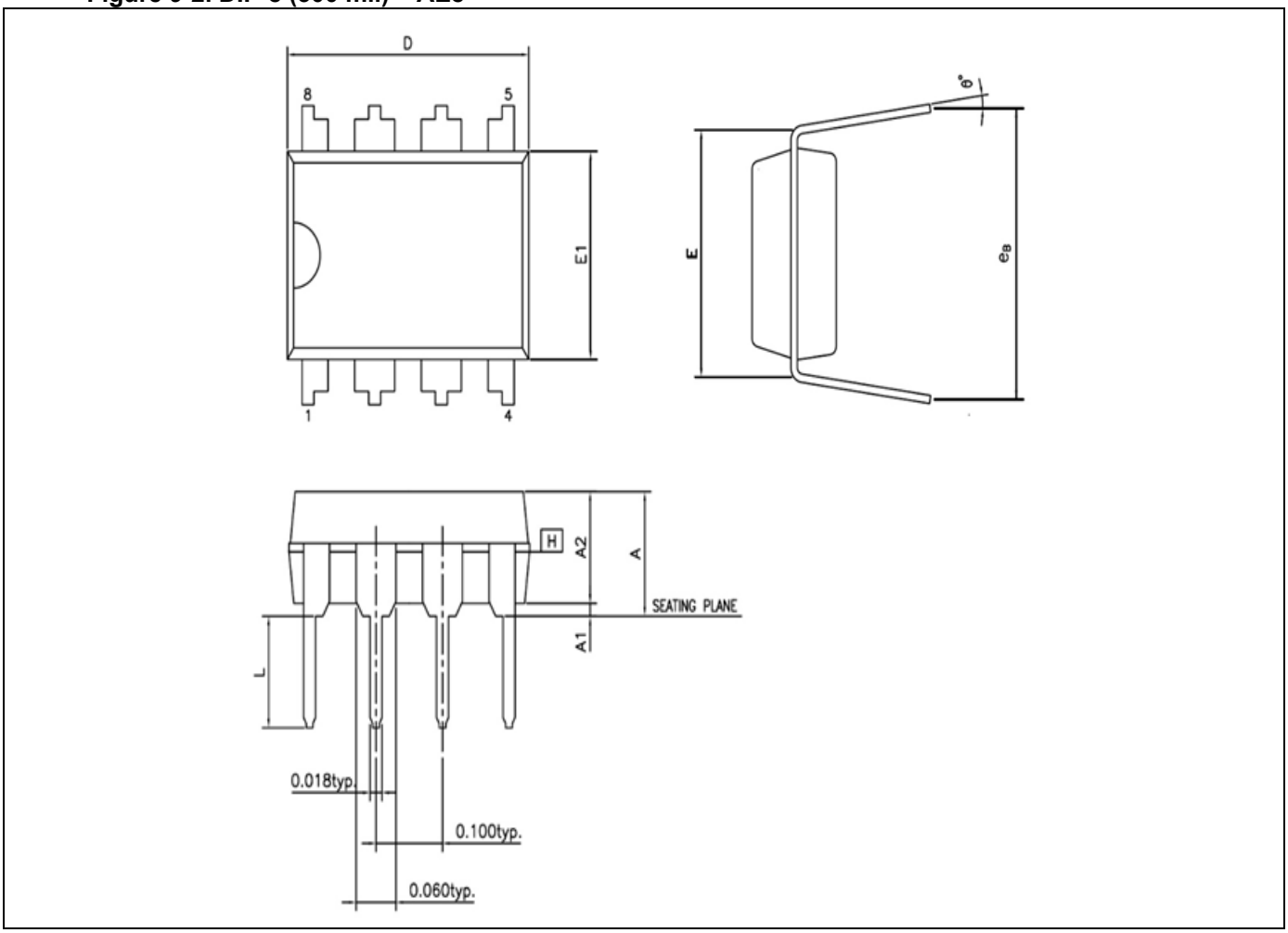
Figure 9-1. SOP-8 (150 mil) ~ AS8



Unit	mm		inch	
Symbols	Min.	Max.	Min.	Max.
A	1.346	1.753	0.053	0.069
A1	0.102	0.254	0.004	0.01
A2	1.346	1.499	0.053	0.059
D	4.801	4.978	0.189	0.196
E	3.810	3.988	0.15	0.157
H	5.791	6.198	0.228	0.244
L	0.406	1.270	0.016	0.05
ɵ	0˚	8˚	0	8

9.2. DIP-8

Figure 9-2. DIP-8 (300 mil) ~ AE8



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	----	----	5.334	----	----	0.210
A1	0.381	----	----	0.015	----	----
A2	3.175	3.302	3.429	0.125	0.130	0.135
D	9.017	9.271	10.16	0.355	0.365	0.400
E	7.62 BSC			0.300 BSC		
E1	6.223	6.35	6.477	0.245	0.250	0.255
L	2.921	3.302	3.81	0.115	0.130	0.150
e_B	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0	7	15	0	7	15

10. Revision History

Revision V1.00 (2025_0825)		Chapter
1	Change “4th-order delta-sigma” to “2nd-order delta-sigma”.	1 3.1 5.4.1
2	Update the figure of “Figure 5-8. ADC Conversion Mode Setting” about Mode26 gain ratio.	5.5.2
3	Update the table of “Table 8-3. ADC Characteristics” about V_{CM}, I_{AVDD}, I_{DVDD}.	8.3
Revision V0.30 (2025_0610)		**Chapter**
1	Update the figure of “Figure 2-1. Part Numbering” .	2
2	Add the descriptions of T_{PSet}.	5.2.3
3	Add the descriptions of T_{PD} , T_{WK} and T_{WSet}.	5.2.4
4	Add the descriptions about ADC output code format and range.	5.4.3
5	Add the descriptions of T_{CSet}.	5.5.3
6	Change the register reset value format from 32-bit to 8-bit in the section of “6.1. SADC Control Registers”.	6.1
7	Change the register reset value of SADC_STA to 0x23.	6.1.1
8	Update the table of “Table 8-3. ADC Characteristics” about ENOB, NFB, I_{AVDD} and I_{DVDD}.	8.3
Revision V0.20 (2025_0321)		**Chapter**
1	Update the descriptions of VREF and DVDD in the table of “Table 4-2. Pin Descriptions”.	4.2
2	Add the descriptions of SADC_VREF_MDS register and update the figure of “Figure 5-4. ADC Analog Mux”.	5.4.2
3	Update the figure of “Figure 5-5. ADC Input Voltage Range” and the related formula.	5.4.3
4	Update the ADC output BCD formula.	5.4.4
5	Add SADC control register 3 and update the description of SADC control register 2 in the section “6.1. ADC Control Registers”.	6.1
6	Add ground connection descriptions and change the ground connection of DVDD pin bypass capacitor to digital ground in the figures of section of “7.1. ADC Application Circuit”.	7.1
7	Update the table of “Table 8 3. ADC Characteristics”.	8.3
Revision V0.10 (2025_0219)		**Chapter**
1	Preliminary version	

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