

Medium-density performance line ARM-based 32-bit MCU with up to 256KB Flash, up to 36KB SRAM, USB, 7 timers, 12-bit ADC, 11 communication interfaces.

Features

- Core: ARM 32-bit Cortex™-M3 CPU
 - 96 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance
 - 64 Byte cache for instruction and data bus support 0 wait state memory access
 - Single-cycle multiplication and hardware division
- Memories
 - 256Kbytes of Flash memory
 - 36 Kbytes of SRAM
- Clock, reset and supply management
 - 2.0 to 3.6 V application supply and I/Os
 - POR, PDR, and programmable voltage detector (PVD)
 - 4-to-16 MHz crystal oscillator
 - Internal 8 MHz factory-trimmed RC
 - Internal 48 MHz factory-trimmed RC
 - Internal 32 kHz RC
 - PLL for CPU clock
 - 32 kHz oscillator for RTC with calibration
- Low power
 - Sleep, Stop and Standby modes
 - VBAT supply for RTC and backup registers
 - Run mode: ~100uA/MHz
 - Stop mode: ~18.5uA @3.3V
 - Standby mode: ~4.5uA @3.3V
 - VBAT with RTC: ~1.1uA @3.3V
- 12-bit mode ADC
 - Max convert rate: 1Msps
 - Up to 16 A/D channels
 - Flexible sample and converter modes.
 - Temperature sensor
- Comparator
 - 2 independent comparators
- Each with 4 positive and 4 negative input channels
- LED driver unit
 - Capable of drive 56 LEDs or 8 Seven-segment LEDs
- 51 fast I/O ports
 - 51, 37,25 I/Os, all mappable on 16 external interrupt vectors
- Debug mode
 - Serial wire debug (SWD) interface
- 7 timers
 - Three 20-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
 - 20-bit, motor control PWM timer with dead-time generation and emergency stop
 - 2 watchdog timers (Independent and Window)
 - SysTick timer: a 24-bit downcounter
- Up to 11 communication interfaces
 - 2 x I2C interfaces (SMBus/PMBus)
 - 3 UARTs (IrDA capability, modem control)
 - 3 SPI interfaces, 1 QSPI interface
 - I2S interface
 - USB 2.0 full-speed device interface
- 2 DMA controller, triggered by Timers, ADC, SPIs, I2Cs, UARTs
- CRC calculation unit, 96-bit unique ID
- RNG generate Random number
- Packages are ECOPACK®

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Chapter 1 Introduction

1.1 Description

The MG32F104xx performance line family incorporates the high-performance ARM®Cortex™-M3 32 bit RISC core operating at 96MHz maximum frequency, Memory up to 256KB FLASH, 36KB SRAM, One advanced-controltimer, Three general-purpose timers, Two watchdog timers (Independent and Window), Three SPI and one QSPIinterfaces, Two I2C interfaces, Three UART interfaces, One I2S interface, One USB2.0 Full Speed interface, One 12-bit SAR ADC converter, One LED driver, Two comparators, One RTC.

1.2 Features

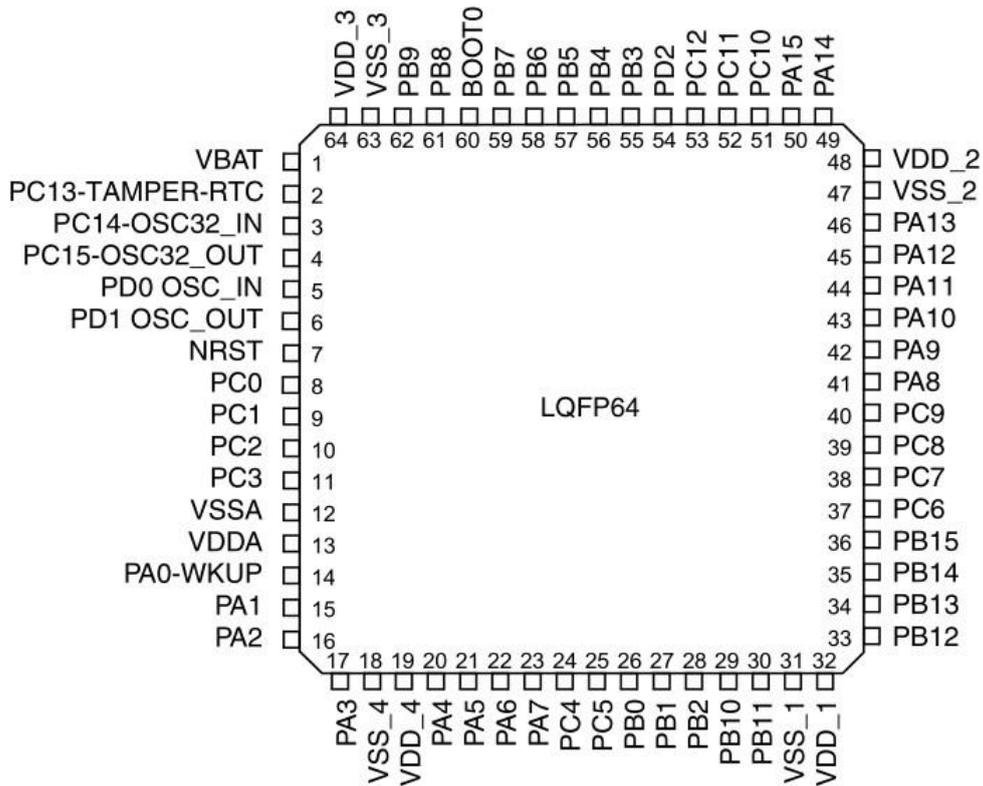
- Supply Management
 - Main supply voltage (VDD): 2.0V - 3.6V
 - Battery supply voltage (VBAT): 1.8V - 3.6V
 - VBAT for RTC and 84 Byte backup registers
- Low Power
 - Sleep, Stop and Standby modes
 - Run mode: 160uA/MHz
 - Stop mode: 18.5uA @3.3V
 - Standby mode: 4.5uA @3.3V
 - VBAT with RTC: 1.1uA @3.3V
- Operation temperature
 - Industrial temperature range (-40°C ~ +85°C)
- Reset
 - NRST reset
 - Power On reset
 - Software reset
 - Watchdog (IWDT and WWDT) reset
 - Low power mode reset
- Programmable Voltage Detector (PVD)
 - Adjustable 8 detect levels

- Configurable rising/falling detect edges
- Clock
 - 4 -16 MHz crystal oscillator, typical 8MHz (HSE)
 - 32 kHz oscillator for RTC with calibration (LSE)
 - Internal 8 MHz factory-trimmed RC (MHSI)
 - Internal 48 MHz factory-trimmed RC (FHSI)
 - Internal 32 kHz RC (LSI)
 - PLL for CPU clock
- High performance 32-bit ARM CPU Core
 - Up to 96MHz ARM Cortex™-M3 Core
 - 64 Byte cache for instruction and data bus, support 0 wait state memory access
 - Configurable system clock frequency
 - Nestable interrupt vector controller
 - Single-cycle multiplication and hardware division
 - 24-bit System Tick down-counter
- Flash
 - 256KB Flash
- SRAM
 - 36KB SRAM
- 12-bit SAR A/D converter
 - Up to 16 A/D input channels
 - Max convert rate: 1Msps
 - Continuous sample and converter mode.
 - Software or Hardware triggered A/D converter mode.
 - Temperature sensor connect to A/D channel 16.
- Comparator
 - 2 independent comparators
 - 4 positive and 4 negative input channels for each comparator
- Debug Port
 - Serial wire debug (SWD)
 - Cortex-M3 Instrumentation Trace Macrocell (ITM)
- Communication interfaces
 - Up to 3 UART interfaces
 - 3 SPI interfaces, 1 QSPI interface
 - 2 I2C interfaces, support SMBus 2.0/PMBus
 - 1 USB2.0 Full Speed interface
 - 1 I2S interface
- Timers
 - Three 20-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental)encoder input
 - 20-bit, motor control PWM timer with dead-time generation and emergency stop

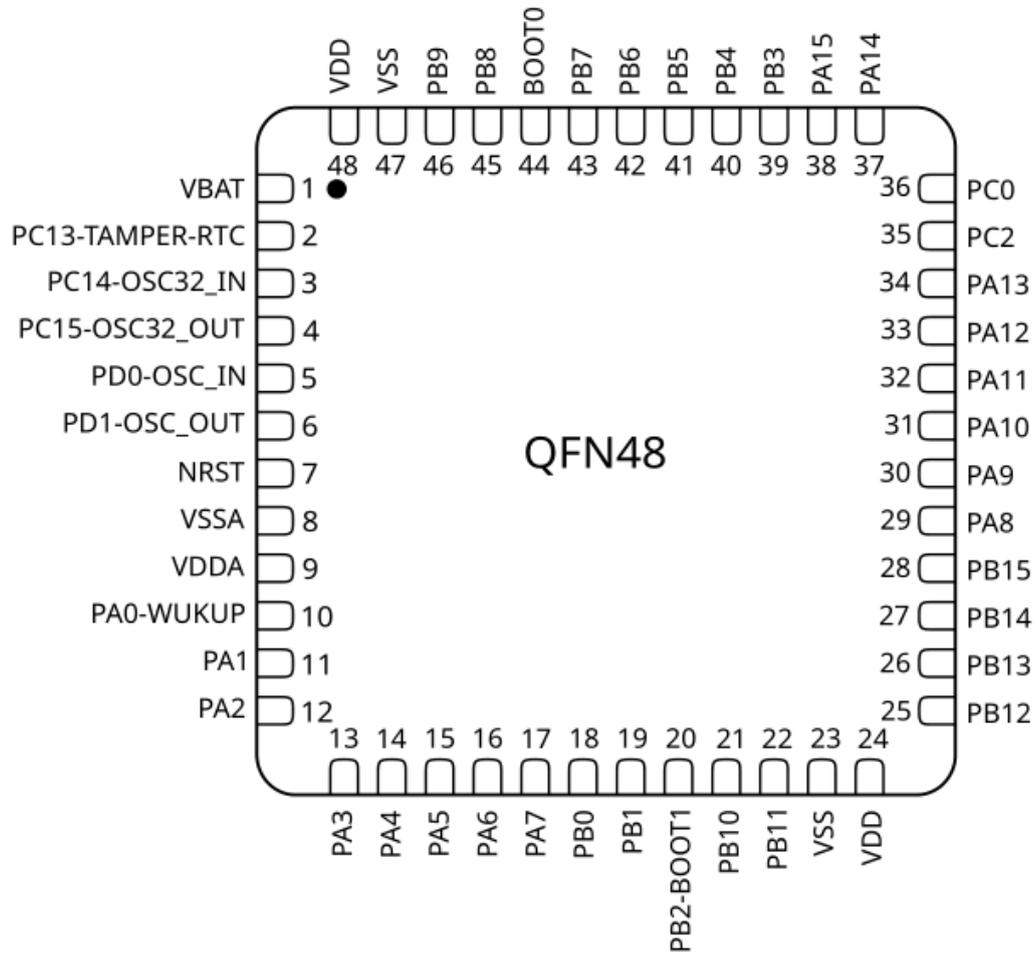
- 20-bit PWM counter (Timer 1 ~ 4)
 - Trigger A/D convertor
- General purpose IOs
 - 64-pin production has 51 GPIOs, 48-pin production has 37 GPIOs, 32-pin production has 25 GPIOs
 - All GPIO mappable on 16 external interrupt vectors
 - Up to 16mA drive current
- Mult-channel DMA controller, can be triggered by Timers, ADC, SPIs, I2Cs, UARTs
- CRC calculation unit, support 8/ 16/ 32 bit CRC algorithms.
- RNG Unit, generate Random number
- LED driver unit, support up to 56 LEDs or 8 Seven-segment LEDs.
- Real-time clock counter (RTC)
- Support ISP(In-System Programming) and IAP(In-Application Programming)
- Support QFN32, QFN48, LQFP64 packages

Chapter 2 Package

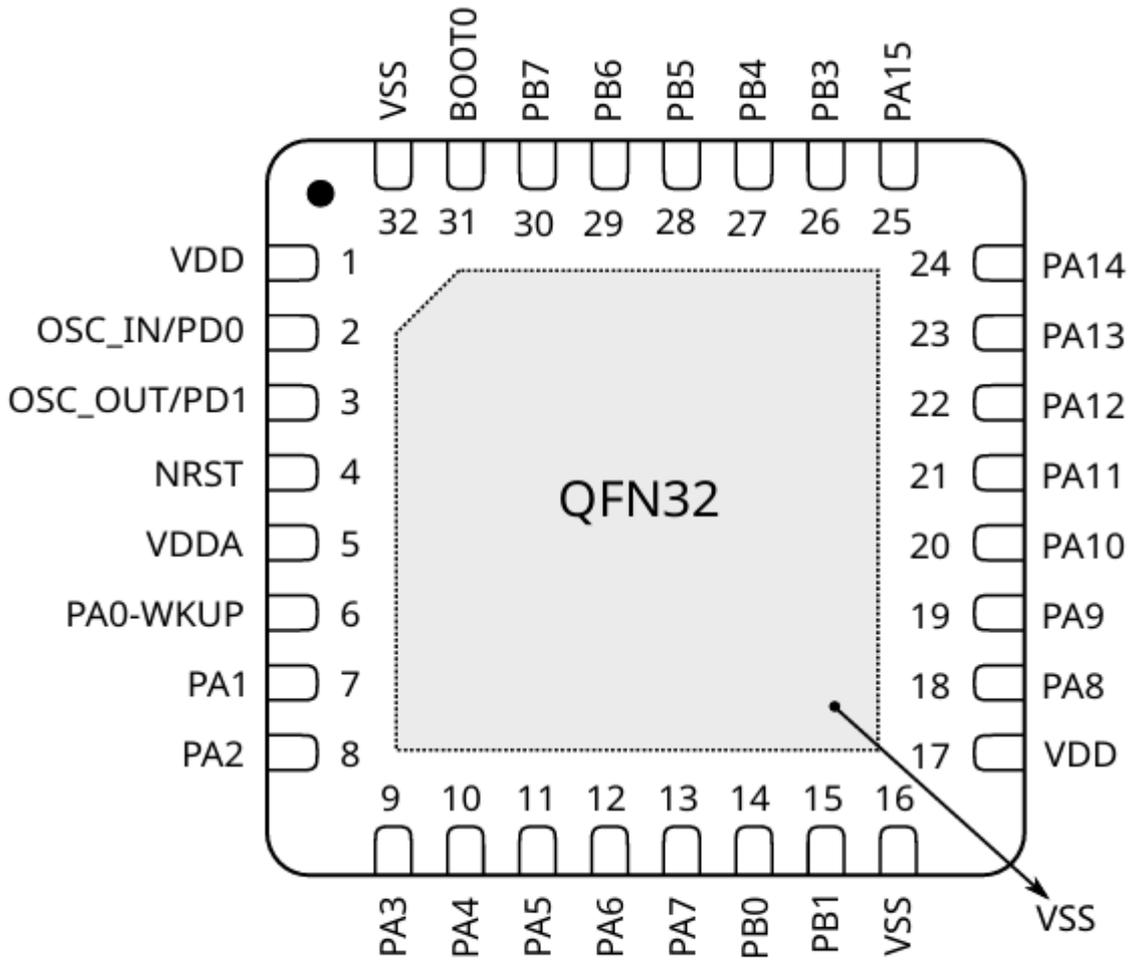
2.1 LQFP64 package



2.2 QFN48 package



2.3 QFN32 package



2.4 Pinouts and pin description

Table 2.1: Pinout description

Pin No.			Pin Name	Type	Main Function	Alternate Function	Analog Function
QFN32	QFN48	LQFP64					
-	1	1	VBAT	S	VBAT		
-	2	2	PC13	I/O	PC13	TAMPER/RTC	
-	3	3	PC14	I/O	PC14		OSC32_IN
-	4	4	PC15	I/O	PC15		OSC32_OUT
2	5	5	PD0	I/O	PD0		OSC_IN
3	6	6	PD1	I/O	PD1		OSC_OUT
4	7	7	NRST	I/O	NRST		
-	36	8	PC0	I/O	PC0	I2S_WS/SPIM2_NSS0/SPIS2_NSS	ADC_IN10
-	-	9	PC1	I/O	PC1	I2S_SCLK/SPIM2_SCK/SPIS2_SCK	ADC_IN11
-	35	10	PC2	I/O	PC2	I2S_SD0/SPIM2_MI/SPIS2_SO	ADC_IN12
-	-	11	PC3	I/O	PC3	I2S_SD1/SPIM2_MO/SPIS2_SI	ADC_IN13
-	8	12	VSSA	S	VSSA		
5	9	13	VDDA	S	VDDA		
6	10	14	PA0	I/O	PA0/WKUP	TIM2_CH1_ETR/UART2_CTS/WKUP	ADC_IN0
7	11	15	PA1	I/O	PA1	TIM2_CH2/UART2_RTS	ADC_IN1
8	12	16	PA2	I/O	PA2	TIM2_CH3/UART2_TX	ADC_IN2
9	13	17	PA3	I/O	PA3	TIM2_CH4/UART2_RX	ADC_IN3
-	-	18	VSS_4	S	VSS_4		
-	-	19	VDD_4	S	VDD_4		
10	14	20	PA4	I/O	PA4	QSPI_NSS0/SPIS1_NSS/UART2_CK	ADC_IN4
11	15	21	PA5	I/O	PA5	QSPI_SCK/SPIS1_SCK	ADC_IN5
12	16	22	PA6	I/O	PA6	TIM1_BKIN/TIM3_CH1/QSPI_MI_IO1/SPIS1_SO	ADC_IN6
13	17	23	PA7	I/O	PA7	TIM1_CH1N/TIM3_CH2/QSPI_MO_IO0/SPIS1_SI	ADC_IN7
-	-	24	PC4	I/O	PC4	TRACECK	ADC_IN14
-	-	25	PC5	I/O	PC5	SPIM2_NSS2/TRACED0	ADC_IN15
14	18	26	PB0	I/O	PB0	TIM1_CH2N/TIM3_CH3/I2S_MCLK/QSPI_IO2	ADC_IN8
15	19	27	PB1	I/O	PB1	TIM1_CH3N/TIM3_CH4/QSPI_IO3	ADC_IN9
-	20	28	PB2	I/O	PB2/BOOT		
-	21	29	PB10	I/O	PB10	TIM2_CH3/TIM4_CH1/I2C2_SCL/QSPI_NSS2/UART3_TX	
-	22	30	PB11	I/O	PB11	TIM2_CH4/I2C2_SDA/SPIM2_NSS1/UART3_RX	
16	23	31	VSS_1	S	VSS_1		
17	24	32	VDD_1	S	VDD_1		
-	25	33	PB12	I/O	PB12	TIM1_BKIN/I2S_WS/LED4/SPIM2_NSS0/SPIS2_NSS/UART3_CK	
-	26	34	PB13	I/O	PB13	TIM1_CH1N/I2S_SCLK/LED5/SPIM2_SCK/SPIS2_SCK/UART3_CTS	
-	27	35	PB14	I/O	PB14	TIM1_CH2N/LED6/SPIM2_MI/SPIS2_SO/UART3_RTS	
-	28	36	PB15	I/O	PB15	TIM1_CH3N/LED7/SPIM2_MO/SPIS2_SI	
-	-	37	PC6	I/O	PC6	TIM3_CH1/I2S_MCLK/LED0	
-	-	38	PC7	I/O	PC7	TIM3_CH2/I2S_MCLK/LED1	
-	-	39	PC8	I/O	PC8	TIM3_CH3/LED2	
-	-	40	PC9	I/O	PC9	TIM3_CH4/LED3/TRACED1	
18	29	41	PA8	I/O	PA8	TIM1_CH1/LED0/UART1_CK/MCO	CMPA_P0
19	30	42	PA9	I/O	PA9	TIM1_CH2/LED1/UART1_TX	CMPA_N0
20	31	43	PA10	I/O	PA10	TIM1_CH3/LED2/UART1_RX	
21	32	44	PA11	I/O	ISOCLK	TIM1_CH4/LED3/UART1_CTS	USBDM
22	33	45	PA12	I/O	ISODA	TIM1_ETR/UART1_RTS	USBDP
23	34	46	PA13	I/O	SWDIO	QSPI_NSS1	CMPA_P3
32	-	47	VSS_2	S	VSS_2		
1	-	48	VDD_2	S	VDD_2		
24	37	49	PA14	I/O	SWDCLK	QSPI_NSS2	CMPA_N3
25	38	50	PA15	I/O	PA15	TIM2_CH1_ETR/I2S_WS/I2C1_SMBAL/SPIS1_NSS	CMPB_P3
-	-	51	PC10	I/O	PC10	LED4/UART3_TX/TRACED2	CMPB_P1
-	-	52	PC11	I/O	PC11	LED5/UART3_RX/TRACED3	CMPB_P2

Pin No.			Pin Name	Type	Main Function	Alternate Function	Analog Function
QFN32	QFN48	LQFP64					
-	-	53	PC12	I/O	PC12	TIM4_ETR/LED6/UART3_CK	CMPB_N0
-	-	54	PD2	I/O	PD2	TIM3_ETR/LED7	CMPB_P0
26	39	55	PB3	I/O	PB3	SWD_SWO/TIM2_CH2/I2S_SCLK/QSPI_SCK/SPIS1_SCK	CMPB_N3
27	40	56	PB4	I/O	PB4	TIM3_CH1/QSPI_MI_IO1/SPIS1_SO	CMPA_P1
28	41	57	PB5	I/O	PB5	TIM3_CH2/I2S_SD1/I2C1_SMBAL/QSPI_MO_IO0/SPIS1_SI	CMPA_P2
29	42	58	PB6	I/O	PB6	TIM4_CH1/I2C1_SCL/QSPI_NSS1/UART1_TX	CMPA_N1
30	43	59	PB7	I/O	PB7	TIM4_CH2/I2C1_SDA/SPIM2_NSS1/UART1_RX	CMPA_N2
31	44	60	BOOT0	I	BOOT0		
-	45	61	PB8	I/O	PB8	TIM4_CH3/I2C1_SCL/SPIM2_NSS2/UART1_CTS	CMPB_N1
-	46	62	PB9	I/O	PB9	TIM4_CH4/I2C1_SDA/UART1_RTS	CMPB_N2
-	47	63	VSS_3	S	VSS_3		
-	48	64	VDD_3	S	VDD_3		

MG32F104xx performance line GPIO function selection:

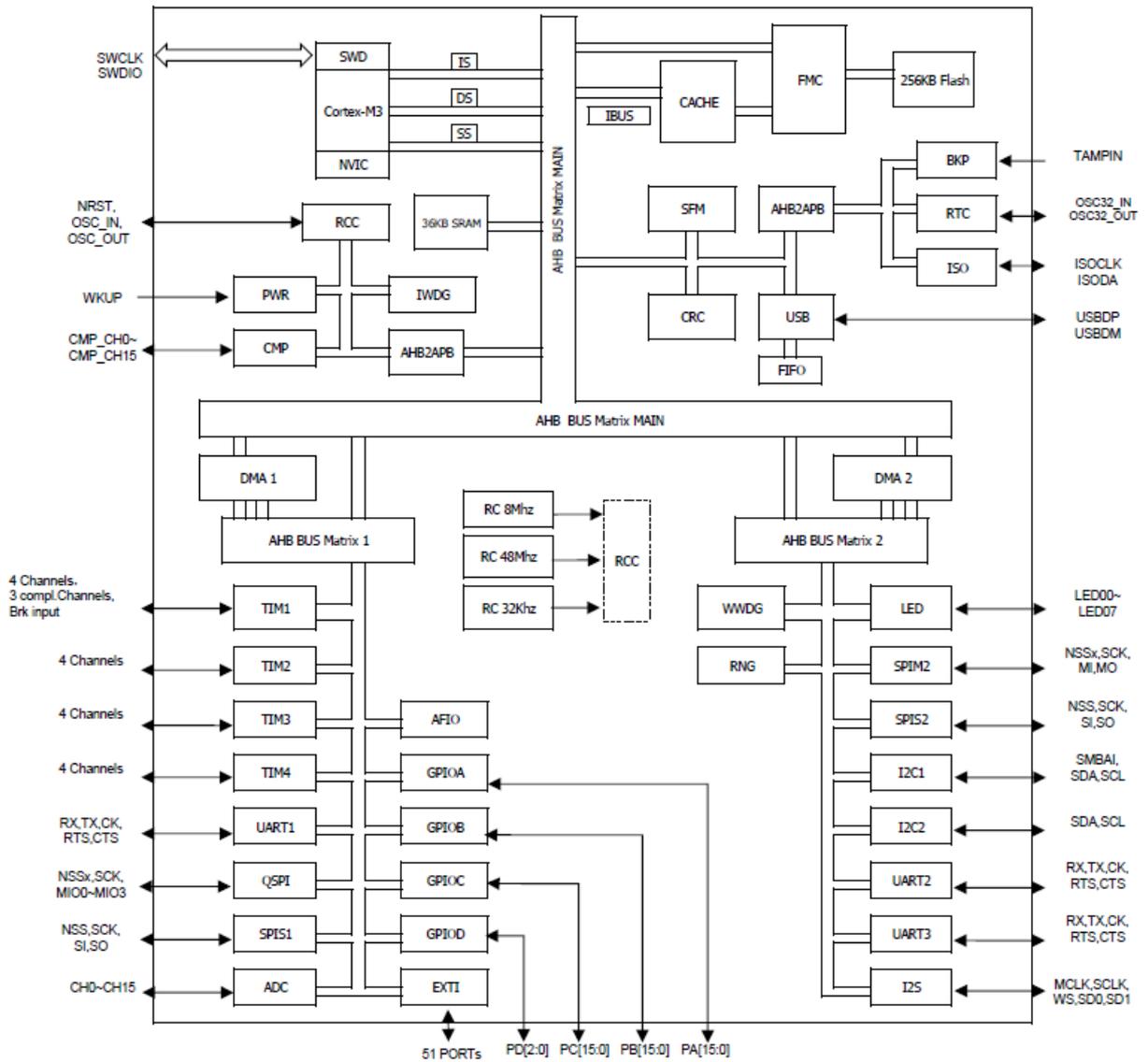
Table 2.2: Pin func selection

AFR[3:0]	0	1	2	3	4	5	6	7
PORT A	PA0	WKUP	TIM2_CH1_ETR					UART2_CTS
	PA1		TIM2_CH2					UART2_RTS
	PA2		TIM2_CH3					UART2_TX
	PA3		TIM2_CH4					UART2_RX
	PA4						QSPI_NSS0	SPIS1_NSS
	PA5						QSPI_SCK	SPIS1_SCK
	PA6		TIM1_BKIN	TIM3_CH1			QSPI_MI_IO1	SPIS1_SO
	PA7		TIM1_CH1N	TIM3_CH2			QSPI_MO_IO0	SPIS1_SI
	PA8	MCO	TIM1_CH1			LED0		UART1_CK
	PA9		TIM1_CH2			LED1		UART1_TX
	PA10		TIM1_CH3			LED2		UART1_RX
	PA11		TIM1_CH4			LED3		UART1_CTS
	PA12		TIM1_ETR					UART1_RTS
	PA13	SWD_DIO					QSPI_NSS1	
	PA14	SWD_CLK					QSPI_NSS2	
PA15		TIM2_CH1_ETR		I2S_WS	I2C1_SMBAI	QSPI_NSS0	SPIS1_NSS	
PORT B	PB0		TIM1_CH2N	TIM3_CH3	I2S_MCLK		QSPI_IO2	
	PB1		TIM1_CH3N	TIM3_CH4			QSPI_IO3	
	PB2	BOOT1						
	PB3	SWD_SWO	TIM2_CH2		I2S_SCLK		QSPI_SCK	SPIS1_SCK
	PB4			TIM3_CH1			QSPI_MI_IO1	SPIS1_SO
	PB5			TIM3_CH2	I2S_SD1	I2C1_SMBAI	QSPI_MO_IO0	SPIS1_SI
	PB6			TIM4_CH1		I2C1_SCL	QSPI_NSS1	
	PB7			TIM4_CH2		I2C1_SDA	SPIM2_NSS1	UART1_TX
	PB8			TIM4_CH3		I2C1_SCL	SPIM2_NSS2	UART1_RX
	PB9			TIM4_CH4		I2C1_SDA		UART1_CTS
	PB10		TIM2_CH3	TIM4_CH1		I2C2_SCL	QSPI_NSS2	UART3_TX
	PB11		TIM2_CH4			I2C2_SDA	SPIM2_NSS1	UART3_RX
	PB12		TIM1_BKIN		I2S_WS	LED4	SPIM2_NSS0	SPIS2_NSS
	PB13		TIM1_CH1N		I2S_SCLK	LED5	SPIM2_SCK	SPIS2_SCK
	PB14		TIM1_CH2N			LED6	SPIM2_MI	SPIS2_SO
PB15		TIM1_CH3N		I2S_SD0	LED7	SPIM2_MO	SPIS2_SI	
PORT C	PC0				I2S_WS		SPIM2_NSS0	SPIS2_NSS
	PC1				I2S_SCLK		SPIM2_SCK	SPIS2_SCK
	PC2				I2S_SD0		SPIM2_MI	SPIS2_SO
	PC3				I2S_SD1		SPIM2_MO	SPIS2_SI
	PC4	TRACECK						
	PC5	TRACED0					SPIM2_NSS2	
	PC6			TIM3_CH1	I2S_MCLK	LED0		
	PC7			TIM3_CH2	I2S_MCLK	LED1		
	PC8			TIM3_CH3		LED2		
	PC9	TRACED1		TIM3_CH4		LED3		
	PC10	TRACED2				LED4		UART3_TX
	PC11	TRACED3				LED5		UART3_RX
	PC12			TIM4_ETR		LED6		UART3_CK
	PC13	TAMPER_RTC						
	PC14	OSC32_IN						
PC15	OSC32_OUT							
PORT D	PD0	OSC_IN						
	PD1	OSC_OUT						
	PD2			TIM3_ETR		LED7		

Chapter 3 Block Diagram

MG32F104XX performance line block diagram:

Figure 3.1: MG32F104XX block diagram



Chapter 4 System description

4.1 Device Overview

Table below show MG32F104xx device features and peripherals:

Table 4.1: MG32F104XX device features and peripheral counts

Peripheral		MG32F104KCU6	MG32F104CCU6	MG32F104RCT6
Flash(KB)		256		
SRAM(KB)		36		
Timers	General-purpose	3		
	Advanced-Control	1		
Communication	QSPI(Master)	1		
	SPIM	0	1	1
	SPIS	1	2	2
	I ² C	1	2	2
	UART	2	3	3
	USB	1		
	I ² S	0	1	1
GPIOs		25	37	51
ADC	12-bit ADC	1		
	ADC channels	10	10	16
Comparators	Number	2		
	CMP channel	10	12	16
CPU frequency		96MHz		
Operating voltage		2.0V ~ 3.6V		
Operating temperatures		Industrial temperature -40°C ~ +85°C Junction temperature -40°C ~ +125°C		
Packages		QFN32	QFN48	LQFP64

4.2 ARM Cortex™-M3 core

Cortex™ M3 is a 32-bit RISC processor core with three levels pipeline. It includes the AMBA-Lite interface and is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), which is a low cost but high performance MCU platform. It has optional hardware debugging function, can execute Thumb-2 instruction, and is compatible with other Cortex-M series. MG32F104xx performance line family incorporates the ARM ©Cortex™-M3 processor core, so it is compatible with all ARM tools and software.

4.3 Memory map

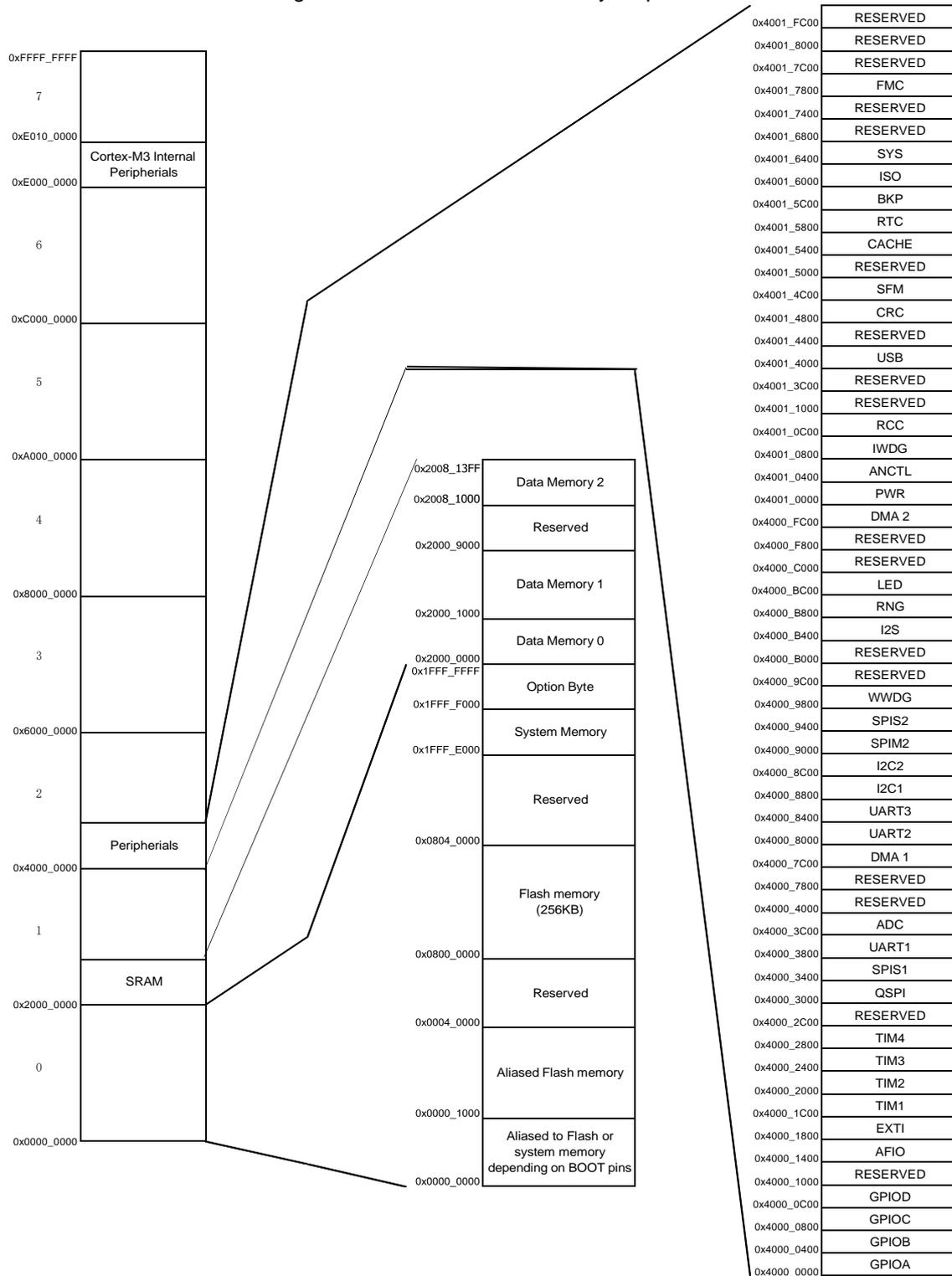
Program memory, data memory, system memory and AHB/APB peripherals are organized within the same linear 4-GB address space. The addressable memory space is divided into 8 main blocks, each of 512 MB.

AHB peripheral address space is 64KB, can support up to 64 peripherals. APB peripheral address space is 64KB, each peripheral can use up to 1KB address space. APB peripheral only support word access, byte and half-word accesses are not supported.

System memory address space is 4KB and reserved for ISP

program. The MG32F104xx memory map is organized below:

Figure 4.1: MG32F104xx memory map



4.4 System reset

System reset can be triggered by the sources below:

- POR reset (POR)
- NRST
- WDG reset (IWDG and WWDG)
- CPU Software reset
- Exiting standby mode

Any source above can trigger the system reset. When the working voltage is proper, the MHSI will be turned on and kept active. When NRST is asserted to high level, the oscillator will start running, and the flash controller will finish the device initialization.

4.5 NVIC

Cortex™-M3 is tightly coupled with the Nested Vectored Interrupt Controller (NVIC). This hardware block provides flexible interrupt management features with minimal interrupt latency.

The main features include:

- low latency interrupt processing
- handle the system exceptions/faults and peripheral interrupts/events
- support up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3)
- four programmable levels for the interrupt priority
- generate the software interrupt
- configurable Non Maskable Interrupt (NMI).

4.6 EXTI

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests.

4.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock, internal RC 48 MHz oscillator or clock output from PLL can be selected as system clock. When an external 4-16 MHz clock is used, it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC 8 MHz oscillator. A software interrupt is generated if enabled.

Several prescalers allow the configuration frequency of the AHB, APB1 and APB2 domains. The maximum frequency of the AHB, APB1 and APB2 is 96 MHz, and the frequency of them can be configured independently.

4.8 Boot mode

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

4.9 Power supply schemes

- VDD = 2.0~3.6V: external power supply for I/Os and the internal regulator. Provided externally through VDD pins.
- VDDA = 2.4~3.6V: external analog power supplies for ADC, and the minimum voltage should be 2.4 V when the ADC is used.
- VBAT = 1.8~3.6V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present.

Note: VDDA must be the same potential as VDD. It is recommended to power VDD and VDDA from the same source.

4.10 DMAC

Two general-purpose DMACs, each have 3 channels and up to 16 hardware DMA requests (16 requests for DMAC0 and 12 requests for DMAC1) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers have internal arbiter to arbitrate the priority of DMA requests.

Each channel can be configured with hardware DMA requests, or also support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I2C, I2S, UART, TIMx and ADC.

4.11 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on VDD supply when present or through the VBAT pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

4.12 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

4.13 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

4.14 System Tick

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Clock source is fixed to 1/8 of CPU frequency

4.15 General-purpose timers

There are up to 3 synchronizable general-purpose timers (TIM2, TIM3 and TIM4) embedded in the MG32F104XX performance line devices. These timers are based on a 20-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output.

This gives up to 16 input captures / output compares / PWMs on the largest packages.

The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

4.16 Advanced-control timer

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 20-bit timer, it has the same features as the TIMx timer. If configured as the 20-bit PWM generator, it has full modulation capability (0-100%). In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers which have the same architecture. The advanced-control timer can therefore work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

4.17 I2C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard ($\leq 100\text{Kb/s}$), fast mode ($\leq 400\text{Kb/s}$) and high speed mode ($\leq 3.4\text{Mb/s}$).

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and They support SMBus 2.0/PMBus.

4.18 Inter-integrated sound (I2S)

One standard I2S interface is available, it is operated in master mode. The interface can be configured to operate with 16/32 bit resolution, as input or output channels. The master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

4.19 Universal asynchronous receiver transmitters (UART)

Up to three universal asynchronous receiver transmitters (UART1, UART2 and UART3), These three interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode.

UART1, UART2 and UART3 interfaces are able to communicate at speeds of up to 6.0 Mbit/s. They also provide hardware management of the CTS and RTS signals.

All interfaces can be served by the DMA controller.

4.20 Serial peripheral interface (SPI)

Two SPIs are able to communicate up to 18 Mbits/s in slave modes in full-duplex and simplex communication modes. One SPI and one QSPI are able to communicate up to 24 Mbits/s in master modes in full-duplex and simplex communication modes. The frame can be configurable to 4bits, 8 bits, 16 bits or 32bits.

Both SPIs and QSPI can be served by the DMA controller.

4.21 USB

One USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

4.22 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

4.23 ADC

One 12-bit analog-to-digital converters is embedded into MG32F104XX performance line devices and the ADC support up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

VDDA supply power for ADC, range from 2.4V-3.6V, ADC convert input voltage from 0V to VDDA.

The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

4.24 Comparators

Up to 2 voltage comparators, each of them has 4 positive input channels and 4 negative input channels.

4.25 Random number generator

One Random number generator, used to generate 8/16/32 bit Random number.

4.26 LED Driver

One LED driver, support up to 56 LEDs or 8 Seven-segment LEDs.

4.27 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from an 8/16/32-bit data word and a fixed generator polynomial.

4.28 Embedded SRAM and Flash memory

Up to 256 Kbytes of embedded Flash is available for storing programs and data.

Up to 36 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

4.29 Power supply supervisor

The device has an integrated power-on reset (POR) /power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2.0V. The device remains in reset mode when VDD is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the VDD /VDDA power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when VDD /VDDA drops below the V_{PVD} threshold and/or when VDD /VDDA is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

4.30 Low-power modes

MG32F104XX supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the MHSI RC, the FHSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the MHSI, the FHSI and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

4.31 SWD Debug Port

The ARM SWJ-DP Interface is embedded, and is a serial wire debug port that enables a serial wire debug to be connected to the target.

Chapter 5 Electrical characteristics

5.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 5.1: Voltage characteristics, Table 5.2: Current characteristics, and Table 5.3: Thermal characteristics may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5.1.1 Voltage characteristics

Table 5.1: Voltage characteristics

Symbol	Ratings	Min	Max	Unit
VDD-VSS	External main supply voltage (including VDDA and VDD)	-0.5	3.6	V
V _{in}	Input voltage on pins	VSS-0.3	VDD+0.5	
ΔV_{DDx}	Variations between different VDD power pins	-	50	mV
$V_{SSx} - V_{SS}$	Variations between all the different ground pins	-	50	

5.1.2 Current characteristics

Table 5.2: Current characteristics

Symbol	Ratings	Max	Unit
I _{VDD}	Total current into VDD/VDDA power lines (source)	60	mA
I _{VSS}	Total current out of VSS ground lines (sink)	60	
I _{IO}	Output current sunk by any I/O and control pin	16	
	Output current source by any I/Os and control pin	-16	
I _{INJ(PIN)}	Injected current on any pin	± 5	
$\sum I_{INJ(PIN)}$	Total injected current	± 25	

Note1: All main power (VDD , VDDA) and ground (VSS , VSSA) pins must always be connected to the external power supply, in the permitted range.

Note2: Negative injection disturbs the analog performance of the device

Note3: A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$, $I_{INJ(PIN)}$ must never be exceeded.

Note4: When several inputs are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.1.3 Thermal characteristics

Table 5.3: Thermal characteristics

Symbol	Rating	Value	Unit
T_{STG}	Storage temperature range	-45 ~ +150	°C
T_J	Maximum junction temperature	100	

5.2 Operating conditions

5.2.1 General operating conditions

Table 5.4: General operating conditions

Symbol	Parameter	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	96	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	96	
f_{PCLK2}	Internal APB2 clock frequency	-	96	
VDD	Standard operating voltage	2	3.6	V
VDDA	Analog operating voltage	2	3.6	V
VBAT	Backup operating voltage	1.8	3.6	V
T	Ambient temperature	-40	85	°C

Note1: It is recommended to power VDD and VDDA from the same source. A maximum difference of 300 mV between VDD and VDDA can be tolerated during power-up and operation

Note2: When ADC is used, VDDA operation voltage is 2.4V~3.6V.

5.2.2 Embedded reset and power control block characteristics

Table 5.5: Power on Reset characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{delay}	RSTN establish time	-	-	40	-	us
$V_{POR/PDR}$	Power on reset threshold	rising edge	-	1.92	-	V
		falling edge	-	1.88	-	V

Table 5.6: PVD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector select rising edge	PLS[2:0] = 000	-	2.25	-	V
		PLS[2:0] = 001	-	2.35	-	
		PLS[2:0] = 010	-	2.45	-	
		PLS[2:0] = 011	-	2.55	-	
		PLS[2:0] = 100	-	2.65	-	
		PLS[2:0] = 101	-	2.75	-	
		PLS[2:0] = 110	-	2.85	-	
		PLS[2:0] = 111	-	2.95	-	
	Programmable voltage detector select falling edge	PLS[2:0] = 000	-	2.14	-	
		PLS[2:0] = 001	-	2.24	-	
		PLS[2:0] = 010	-	2.34	-	
		PLS[2:0] = 011	-	2.44	-	
		PLS[2:0] = 100	-	2.54	-	
		PLS[2:0] = 101	-	2.64	-	
		PLS[2:0] = 110	-	2.74	-	
		PLS[2:0] = 111	-	2.84	-	

5.2.3 Supply current characteristics

Table 5.7: Supply current characteristics

Mode	Conditions	VDD@25°C			Unit
		2.0V	2.5V	3.6V	
Run Mode ¹	HCLK=96MHz,Execute from Flash,APB clock enable	12.43	12.92	12.3	mA
	HCLK=96MHz,Execute from Flash,APB clock disable	8.0	8.22	7.73	mA
	HCLK=48MHz(FHSI),Execute from Flash,APB clock enable	9.83	9.55	10.04	mA
	HCLK=48MHz(FHSI),Execute from Flash,APB clock disable	6.96	6.41	6.89	mA
	HCLK=8MHz(HSE),Execute from Flash,APB clock enable	3.35	2.78	3.41	mA
	HCLK=8MHz(HSE),Execute from Flash,APB clock disable	2.84	2.37	2.87	mA
	HCLK=8MHz(MHSI),Execute from Flash,APB clock enable	3.11	2.54	2.79	mA
	HCLK=8MHz(MHSI),Execute from Flash,APB clock disable	2.54	1.91	2.28	mA
Sleep Mode	HCLK=96MHz, APB clock disable	3.23	2.79	3.04	mA
	HCLK=8MHz(MHSI), APB clock disable	1.68	0.93	1.12	mA
Stop Mode	LDO normal mode,HSE/HSI/LSE OFF	240	264	296	uA
	LDO Low power mode,HSE/HSI/LSE OFF	15.98	17.34	20.8	uA
Standby Mode	LSI and IWDG running	4.29	4.52	5.14	uA
VBAT Mode	RTC and LSE running	0.78	1.05	1.25	uA

Note1: Cache is enabled.

Note2: Internal voltage pump is turned on when VDD lower than 2.5V.

Note3: Add an additional power consumption of 0.8 mA in 12-bit mode ADC for the analog part.

5.2.4 External clock source characteristics

Table 5.8: High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HSE_{ext}}$	User external clock source frequency	-	-	8	16	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7VDD	-	VDD	V
V_{HSEL}	OSC_IN input pin low level voltage		VSS	-	0.3VDD	
$T_{W(HSE)}$	OSC_IN high or low time		16	-	-	ns
$T_{r(HSE)}$	OSC_IN rise or fall time		-	-	5	
$T_{f(HSE)}$						
$C_{in(HSE)}$	OSC_IN input capacitance		-	-	5	-
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%

Note1:Based on simulation and avt test results, not tested in production.

Table 5.9: Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LSE_{ext}}$	User external clock source frequency	-	-	32.768	-	KHz
V_{LSEH}	OSC_IN input pin high level voltage		0.7VDD	-	VDD	V
V_{LSEL}	OSC_IN input pin low level voltage		VSS	-	0.3VDD	
$T_{W(LSE)}$	OSC_IN high or low time		450	-	-	ns
$T_{r(LSE)}$	OSC_IN rise or fall time		-	-	50	
$T_{f(LSE)}$			-	-	50	
$C_{in(LSE)}$	OSC_IN input capacitance	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
$T_{SU(LSE)}$	startup time	VDD is stabilized	-	2	-	s

Note 1: Based on simulation and avt test results, not tested in production.

5.2.5 Internal clock source characteristics

Table 5.10: High-speed internal (MHSI) RC oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MHSI}	Frequency	-	-	8	-	MHz
$DuCy_{(MHSI)}$	Duty cycle	-	45	-	55	%
$ACC_{(MHSI)}$	Accuracy of the MHSI oscillator	$T_A = -40$ to 85°C	TBD	-	TBD	%
		$T_A = 0$ to 85°C	TBD	-	TBD	%
		$T_A = 25^\circ\text{C}$	TBD	-	TBD	%
$T_{SU(MHSI)}$	MHSI oscillator startup time	$VSS \leq V_{in} \leq VDD$	1	-	2	us
$I_{DD(MHSI)}$	MHSI oscillator power consumption	-	-	25	-	uA

Table 5.11: High-speed internal (FHSI) RC oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{FHSI}	Frequency	-	-	48	-	MHz
$DuCy_{(FHSI)}$	Duty cycle	-	45	-	55	%
$ACC_{(FHSI)}$	Accuracy of the FHSI oscillator	$T_A = -40$ to 85°C	TBD	-	TBD	%
		$T_A = 0$ to 85°C	TBD	-	TBD	%
		$T_A = 25^\circ\text{C}$	TBD	-	TBD	%
$T_{SU(FHSI)}$	FHSI oscillator startup time	$V_{SS} \leq V_{in} \leq V_{DD}$	200	-	500	ns
$I_{DD(FHSI)}$	FHSI oscillator power consumption	-	-	55	-	μA

Table 5.12: Low-speed internal (LSI) RC oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	20	-	40	KHz
$T_{SU(LSI)}$	LSI oscillator startup time	-	-	-	85	μs
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	250	-	nA

5.2.6 PLL characteristics

Table 5.13: PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock	-	1	8	16	MHz
	PLL input clock duty cycle	-	40	-	60	%
f_{PLLOUT}	PLL multiplier output clock	-	-	96	-	MHz
T_{LOCK}	PLL lock time	-	-	-	200	μs
Jitter	Cycle-to-cycle jitter	-	-	-	300	ps

Note 1: Based on simulation and avt test results, not tested in production.

5.2.7 Memory characteristics

Table 5.14: Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	Page program time	-	2.1	-	ms
T_{ERASE}	Page erase time	-	6.4	-	ms
	Mass erase time	-	25.6	-	ms
IDD_{PROG}	Page program current	-	-	2	mA
IDD_{ERASE}	Page erase current	-	-	1.5	mA
IDD_{READ}	Read current@48MHz	-	-	4.7	mA
	Read current@24MHz	-	-	2.5	mA
N_{END}	Endurance	100	-	-	kcycles
t_{RET}	Data retention	10	-	-	year

5.2.8 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size is either 3 parts (cumulative mode) or 3 parts \times (n + 1) supply pins (non-cumulative mode). The human body model (HBM) can be simulated. The tests are compliant with JESD22-A114/C101 standard.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O

pinThese tests are compliant with ANSI/ESDA/JEDEC IC latch-up

standard.

Table 5.15: ESD absolute maximum ratings

Symbol	Parameter	Condition	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = +25\text{ }^\circ\text{C}$, compliant with JEDEC JS-001-2017	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	$T_A = +25\text{ }^\circ\text{C}$, compliant with JEDEC JS-002-2018	500	V
I_{LU}	Static latch-up class	$T_A = +25\text{ }^\circ\text{C}$, compliant with JEDEC 2016	200	mA

5.2.9 EFT Characteristics

Table 5.16: EFT Characteristics

Symbol	Standard	Voltage	Class
EFT to IO	(IEC61000-4-4)	2KV	Class:4
EFT to Power	(IEC61000-4-4)	4KV	Class:4

Software suggestion

Software flow must contain code to prevent CPU run away, for example □

- Crashed Program Counter.
- Unpredicted Reset
- Crashed important data in control register

Increase driven strength of IOs improve the capability of EFT

5.2.10 IO characteristics

Table 5.17: IO static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	-	0.65VDD	-	VDD+0.5	V
V_{IL}	Input low level voltage	-	-0.5	-	0.3VDD	V
V_{hys}	Schmitt trigger voltage hysteresis	-	5%VDD	-	-	V
I_{lkg}	Input leakage current	$V_{SS} \leq V_{in} \leq V_{DD}$	-	-	± 1	μA
R_{pu}	Weak pull-up equivalent resistor	$V_{in}=V_{SS}$	30	40	50	$k\Omega$
R_{pd}	Weak pull-down equivalent resistor	$V_{in}=V_{DD}$	30	40	50	$k\Omega$
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Table 5.18: Input/output AC characteristics

Speed	Parameter	Conditions	Min	Typ	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency	$C_L=50pF, V_{DD}=2V \text{ to } 3.6V$	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	125	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125	ns
x1	$f_{max(IO)out}$	Maximum frequency	$C_L=50pF, V_{DD}=2V \text{ to } 3.6V$	-	50	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25	ns

5.2.11 TIM characteristics

Table 5.19: TIM characteristics

Symbol	Conditions	Min	Max	Unit
$T_{res(TIM)}$	Timer resolution time	1	-	$T_{TIMxCLK}$
FEXT	Timer external clock frequency on CH1 to CH4	0	$T_{TIMxCLK}/2$	MHz
RESTIM	Timer resolution	-	20	bit
$T_{counter}$	16-bit counter clock period when internal clock is selected	1	65536	$T_{TIMxCLK}$
T_{MAX_COUNT}	Maximum possible count	1	1048576×65536	$T_{TIMxCLK}$

Note1: $T_{TIMxCLK} = 96\text{MHz}$

5.2.12 USB DC electrical characteristics

Table 5.20: USB DC electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
VDD	USB operating voltage		3.0	3.6	V
V_{DI}	Differential input sensitivity	I(USBDP, USBDM)	0.2		V
V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	2.5	V
V_{SE}	Single ended receiver threshold		1.3	2.0	V
V_{OL}	Static output level low	R_L of 1.5 kom to 3.6 V		0.3	V
V_{OH}	Static output level low	R_L of 15 kom to VSS V	2.8	3.6	V

Note1: To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kom resistor to a 3.0-to-3.6 V voltage range.

Note2: Based on simulation and avt test results, not tested in production.

Note3: R_L is the load connected on the USB drivers.

Figure 5.1: USB timings: definition of data signal rise and fall time

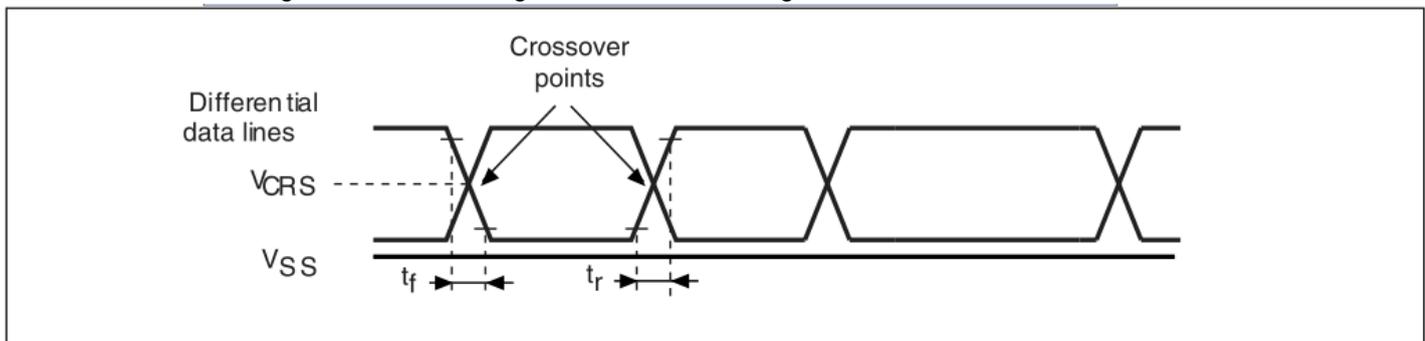


Table 5.21: USB Full-speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time	$C_L = 50 \text{ pF}$	4	20	ns
t_f	Fall time	$C_L = 50 \text{ pF}$	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

Note 1: Based on simulation and avt test results, not tested in production.

5.2.13 CMP characteristics

Table 5.22: CMP characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{in}	Input voltage	0.6	-	VDD-0.3	V
V_{HYST}	Hysteresis	-	2	5	mV
V_{OFF}	Input Offset voltage	-	5	15	mV
$TPGD$	Propagation Delay	-	-	200	nS
I_q	Operation Current	-	-	8.5	uA

5.2.14 ADC characteristics

Table 5.23: ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Power supply	-	2.4	-	3.6	V
f_s	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}	External trigger frequency	$f_{ADC}=14\text{MHz}$	-	-	823	KHz
V_{AIN}	Conversion voltage range	-	0	-	VDDA	V
R_{AIN}	External input impedance	-	-	-	200	Ω
C_{AIN}	External capacitor	-	-	TBD	-	pF
I_{lkg}	Injection current on Analog input	-	-	-	10	uA
R_{ADC}	Sampling switch resistance	-	-	-	1.4	k Ω
C_{ADC}	Internal sample and hold capacitor/12-bit	-	-	15.5	-	pF

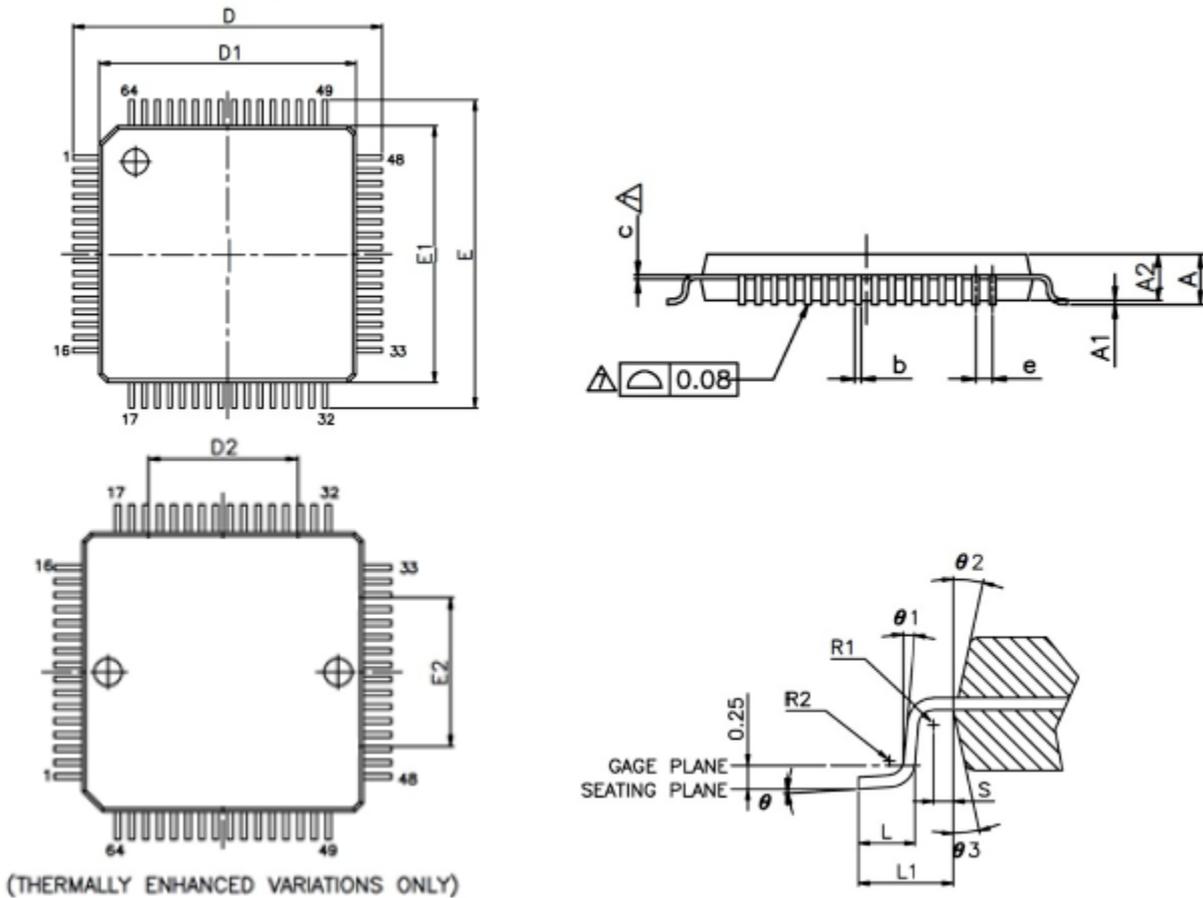
Table 5.24: ADC Conversion time

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{AD}	ADC clock frequency	-	62.5	-	-	ns
T_{CONV}	Conversion time	12-bit	-	$13T_{AD}$	-	ns
F_{CONV}	Sampling rate	12-bit	-	-	940	KSPS
T_{SAMP}	Sampling time	12-bit	$3T_{AD}$	-	-	ns
t_{DIS}	Dis-charge time	-	-	$0.5T_{AD}$	-	ns
t_{DPU}	Power-up time	-	-	-	20	us

Chapter 6 Package characteristics

6.1 LQFP64 10X10mm

Figure 6.1: LQFP64 10X10mm, 0.5mm pitch and Recommended footprint



Note1: Drawing is not to scale.

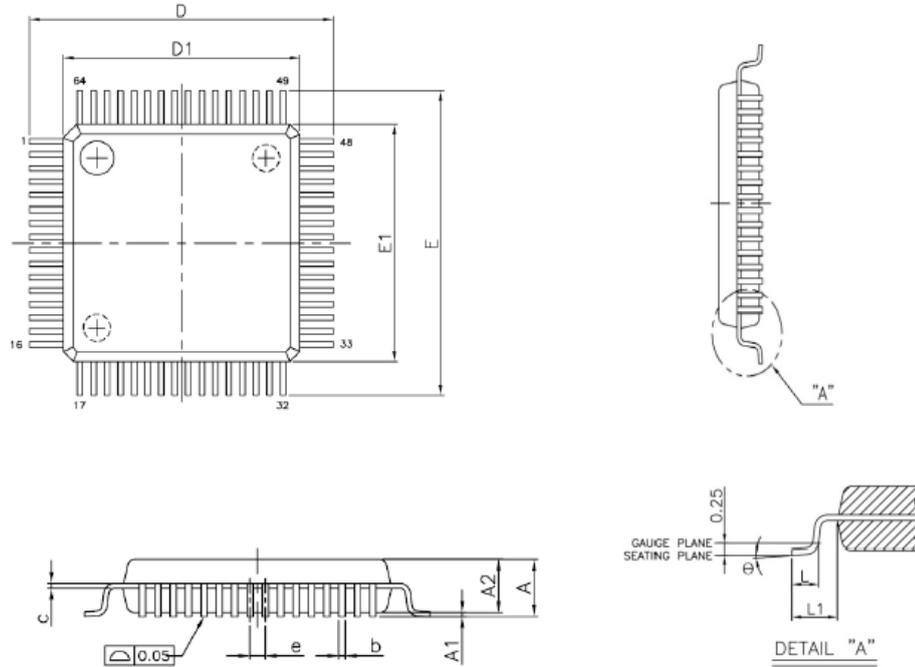
Figure 6.2: LQFP64 10X10mm, 64 pin package parameters

Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	1.60	---	---	0.062
A1	0.05	---	0.15	0.001	---	0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.006	0.008	0.010
c	0.09	---	0.20	0.003	---	0.007
D	11.75	12.00	12.25	0.462	0.472	0.482
D1	9.90	10.00	10.10	0.389	0.393	0.397
E	11.75	12.00	12.25	0.462	0.472	0.482
E1	9.90	10.00	10.10	0.389	0.393	0.397
e	0.50 BSC			0.019 BSC		
L	0.45	0.6	0.75	0.017	0.023	0.029
L1	1.00 REF			0.039 REF.		
S	0.20 REF			0.007 REF.		
ϵ	3.5° REF			0.137 REF.		
ϵ1	5.0° REF			0.196 REF.		
ϵ2	12° REF			0.472 REF.		
ϵ3	12° REF			0.472 REF.		
R1	0.16 REF			0.006 REF.		
R2	0.15 REF			0.005 REF.		

PAD SIZE	E2		D2	
	Min.	Max.	Min.	Max.
165*16E	3.99	4.19	3.99	4.19
210*21E	4.27	5.33	4.27	5.33
260*26E	5.28	6.60	5.28	6.60

6.2 LQFP64 7X7mm

Figure 6.3: LQFP64 7X7mm, 0.4mm pitch and Recommended footprint



Note1: Drawing is not to scale.

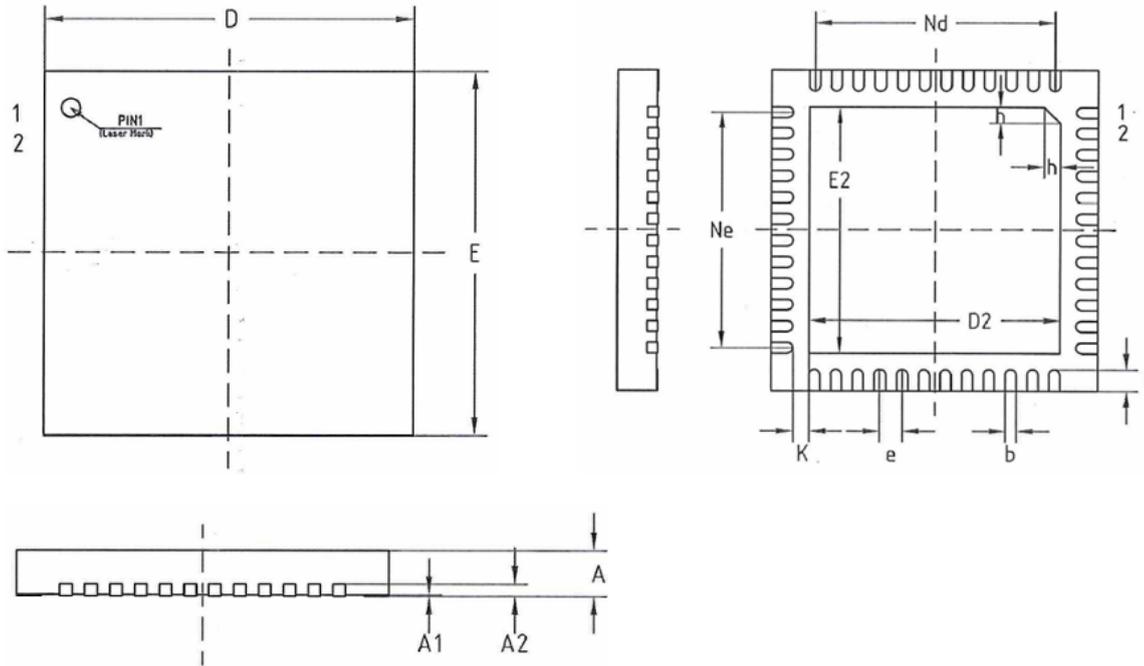
Figure 6.4: LQFP64 7X7mm, 64 pin package parameters

Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	1.60	---	---	0.063
A1	0.05	---	0.15	0.002	---	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
c	0.09	---	0.20	0.004	---	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
e	0.40 BSC			0.016 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

6.3 QFN48 6X6mm

Figure 6.5: QFN48 6X6mm, 48 pin package parameters

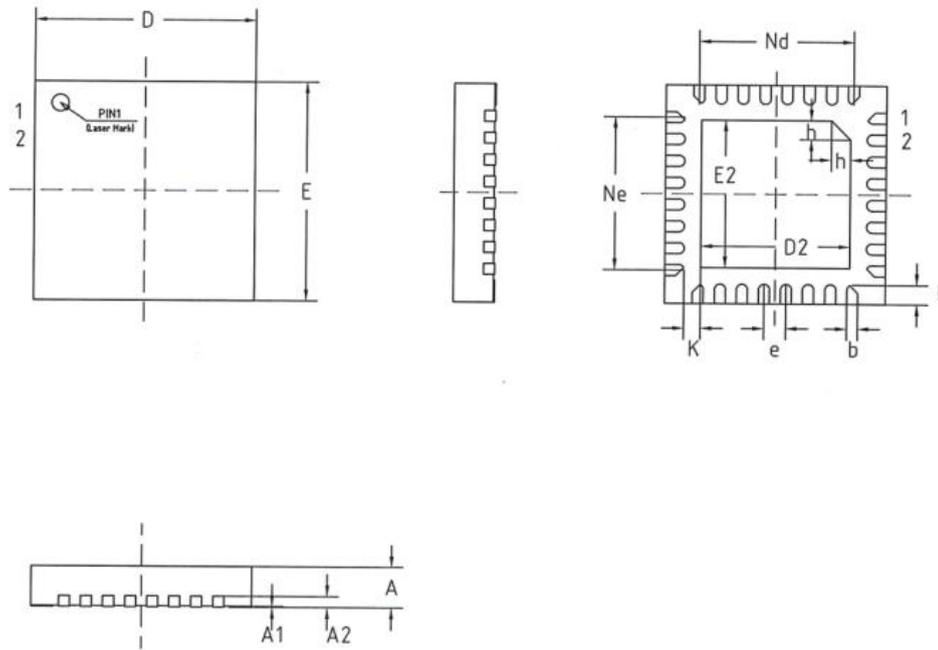
QFN-48 (6×6×0.75mm)



Unit	mm			inch		
JEDEC	MO-220			MO-220		
PKG	WQFN(X648)			WQFN(X648)		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
D2/E2	4.55	4.60	4.65	0.179	0.181	0.183
e	0.40 BSC			0.016 BSC		
K	0.25	0.30	0.35	0.009	0.011	0.013
L	0.35	0.40	0.45	0.014	0.016	0.018
h	0.25	0.30	0.35	0.009	0.011	0.013
Ne/Nd	4.40 BSC			0.173 BSC		

6.4 QFN32 4X4mm

Figure 6.6: QFN32 4X4mm, 0.4mm pitch and Recommended footprint



Note1: Drawing is not to scale.

Figure 6.7: QFN32 4X4mm, 32 pin package parameters

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.70	0.75	0.80	0.276	0.295	0.315
A1		0.02	0.05		0.008	0.020
A2	0.203 REF			0.080 REF		
b	0.15	0.20	0.25	0.059	0.079	0.098
D	3.90	4.00	4.10	1.535	1.575	1.614
D2	2.65	2.70	2.75	1.043	1.063	1.083
E	3.90	4.00	4.10	1.535	1.575	1.614
E2	2.65	2.70	2.75	1.043	1.063	1.083
e	0.40 BSC					
K	0.25	0.30	0.35	0.098	0.118	0.138
L	0.30	0.35	0.40	0.118	0.138	0.157
h	0.30	0.35	0.40	0.118	0.138	0.157
Ne	2.80 BSC			1.102 BSC		
Nd	2.80 BSC			1.102 BSC		

Chapter 7 Product selection

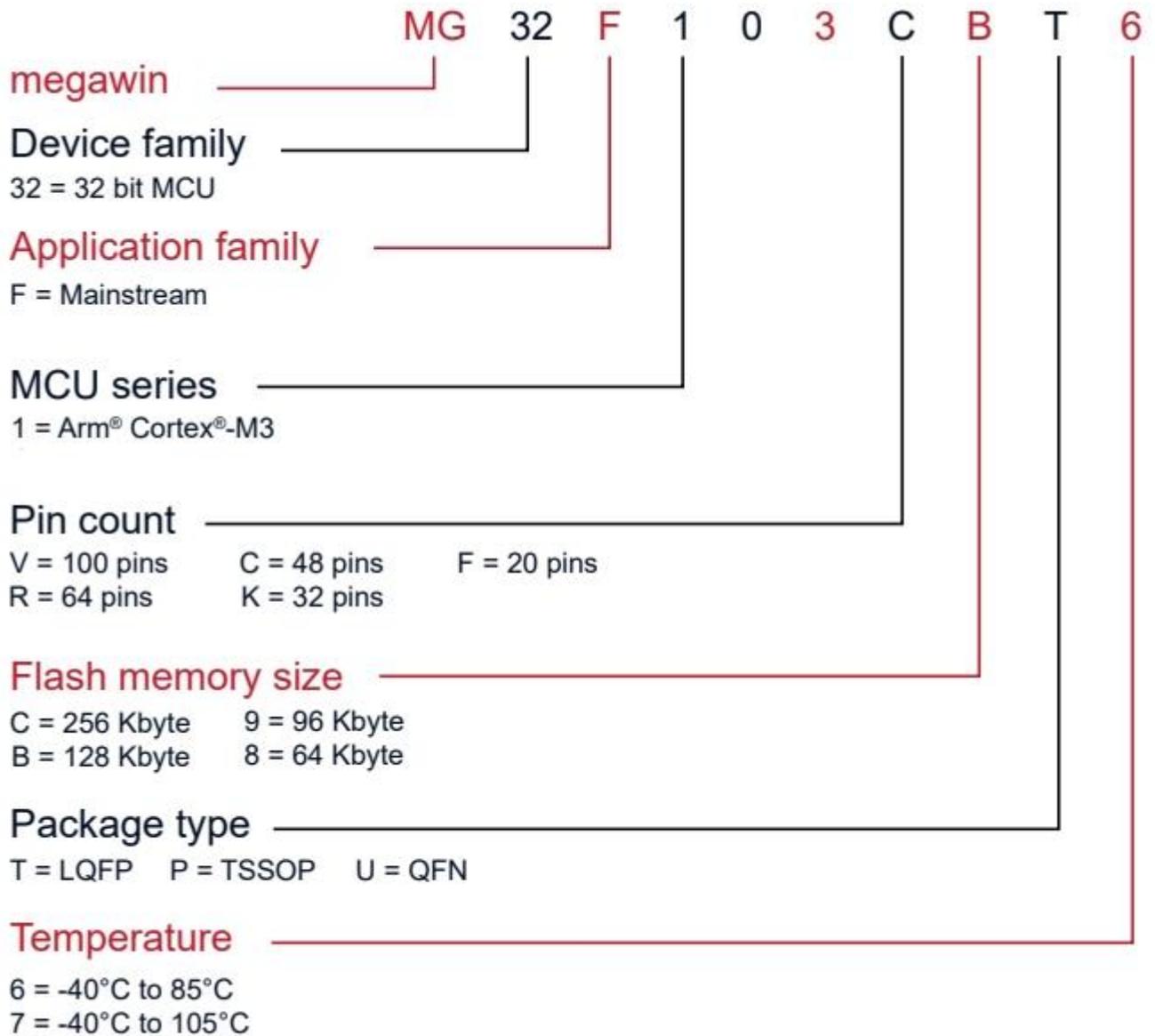
MG32F104x

ARM® Cortex®-M3 Performance MCU

Commercial Product Code	Frequency (MHz)	Core	Flash (Kbytes)	Ram (Kbytes)	Package Name	IONb	Vmin	Vmax	Nb Timer (20bit)	Nb Motor Control Timer	Nb ADC 10/12 bit Cell	Nb ADC Channels	Nb COMP	Nb COMP Channels	Quad SPI (M)	SPI (M)	SPI (S)	I2S	I2C	UART	USB	Nb Segment LCD pins	
	MG32F104RCT6	96	Cortex-M3	256	36	LQFP64	51	2	3.6	3	1	1	16	2	16	1	1	2	1	2	3	1	8
	MG32F104CCU6	96	Cortex-M3	256	36	QFN48	37	2	3.6	3	1	1	10	2	12	1	1	2	1	2	3	1	8
	MG32F104KCU6	96	Cortex-M3	256	36	QFN32	25	2	3.6	3	1	1	10	2	10	1	0	1	0	1	2	1	4

Chapter 8 Ordering information

Figure 8.1: MG32F104XX Ordering Information



Chapter 9 Revision History

Revision	Date	Author	Modify
01.07	20260305	zy.yao	Modify QFN48 package size
01.06	20260224	zy.yao	Modify QFN48 package
01.05	20251203	zy.yao	Add QFN48 package
01.04	20240408	zy.yao	Add QFN32 package
01.03	20240813	zy.yao	Modify update Table 4.1 to MG32F104RCT6
01.02	20220609	zy.yao	Modify update statement in Chapter 1.2
01.01	20220328	zy.yao	Draft version