CGH001A

8Bit Single-Chip Microcontroller

Data Sheet

Version: 0.1

Features

Motor Driving Engine (MDE)

- Space Vector PWM (SVPWM)
- Supports Sine-Wave and Square-Wave Solutions
- Supports Hall Latch Input
- Supports Digital OCP and Analog OCP (Over Current Protection)
- Programmable Dead Band
- Programmable Angle Shift Control (-59° to 59° in 128 steps)
- Frequency Generator (FG)

Embedded MCU

- MCS®-51 Compatible
- 1T 8052 Central Processing Unit
- 4.5V to 5.5V Operation Range
- 4 Level Priority Interrupt
- 14 Interrupt Sources
- 1 External Interrupts (INT1N)
- Memory Size:
- 8KB Flash Program Memory
- 256 x 8-bit IRAM
- 256 x 8-bit XRAM
- Up to 22 General-Purpose Input / Output (GPIO) Pins
- Three 16-bit Timer/Counters
- Watchdog (WD) Timer
- Channel 16-bit Capture
- 8-Channel 10-bit Analog-to-Digital Converter (ADC)
- General Operational Amplifier
- Full Duplex UART Serial Channel
- Fast Multiplication-Division Unit (MDU): 16*16,32/16, 16/16, 32-bit L/R shifting and 32-bit normalization

List of Contents

1. Description

The CGH001A is a 3-phase BLDC motor controller which supports the hall-latch interfaces. The CGH001A supports both the six-phase-drive for torque intensive application and sine-wave-drive to effectively suppress motor vibration and with the built-in, innovated speed control mechanism; an ultra-high RPM can be achieved.

The OCP protection circuitry to prevent motor damage and enhance system reliability is built-in as well. The block diagram is shown in Figure 2.1

2. Block Diagram

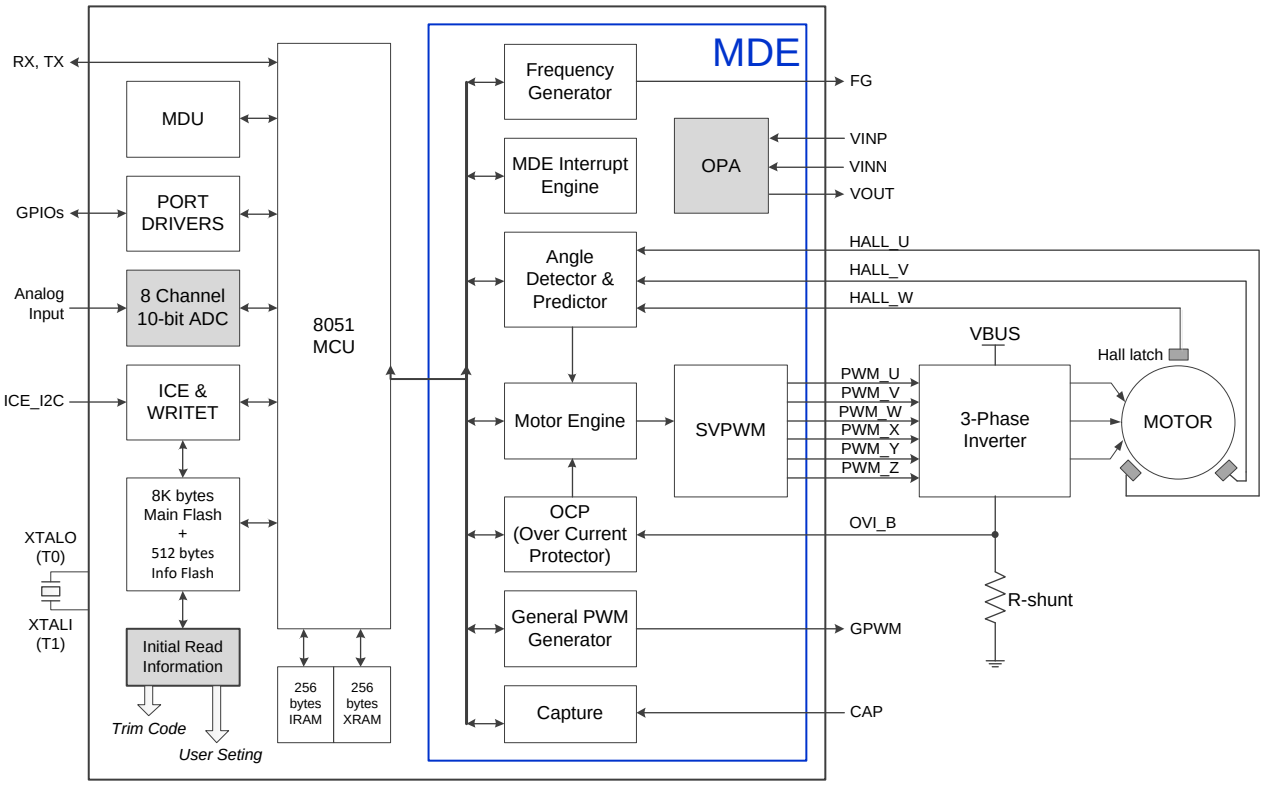


Figure 2.1 CGH001A BLDC motor controller block diagram

3. Pin Assignments

3.1 SSOP-28(AL28)

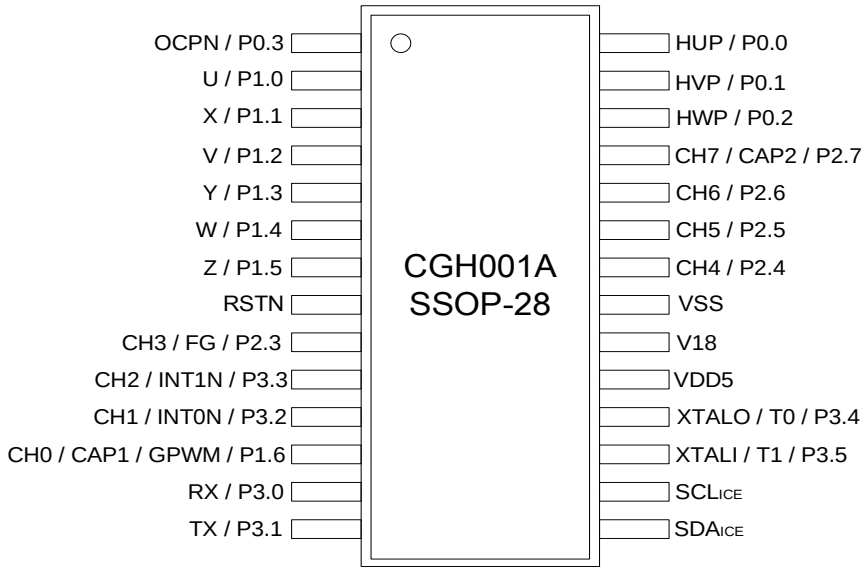


Figure 3.1 SSOP-28(AD4)

3.2 QFN32-4x4mm (AZ32)

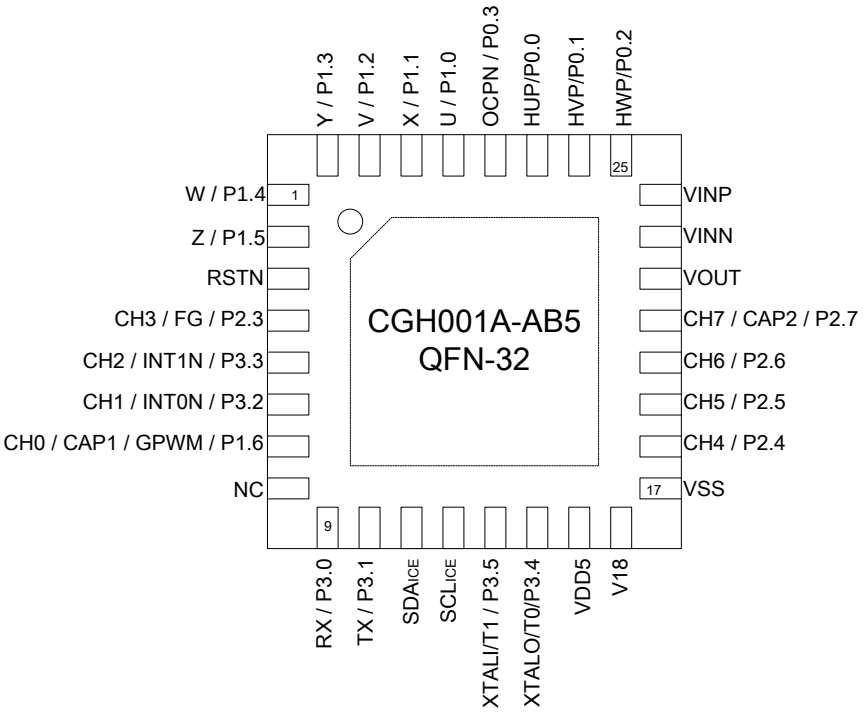


Figure 3.2 QFN32 4X4 (AB5)

4. Pin Definitions

Table 4.1 Pin Definitions

SSOP28	QFN32			
PIN #		Name	Type	Description
8	3	RSTN	I	System Reset.
25	21	CH7	I	Analog Input Ch7.
		CAP2	I	Capture Input 2
		P2.7	I/O	Bit 7 of Port 2.
24	20	CH6	I	Analog Input Ch6.
		P2.6	I/O	Bit 6 of Port 2.
23	19	CH5	I	Analog Input Ch5.
		P2.5	I/O	Bit 5 of Port 2.
22	18	CH4	I	Analog Input Ch4.
		P2.4	I/O	Bit 4 of Port 2.
9	4	CH3	I	Analog Input Ch3.
		FG	O	Frequency Generator Output
		P2.3	I/O	Bit 3 of Port 2.
13	9	RX	I	Serial Data Transmit (UART)
		P3.0	I/O	Bit 0 of Port 3.
14	10	TX	O	Serial Data Receive (UART)
		P3.1	I/O	Bit 1 of Port 3.
15	11	SDA_{ICE}		For ICE (In Circuit Emulator).
16	12	SCL_{ICE}		For ICE (In Circuit Emulator).
17	13	XTALI	I	Crystal input pin. Connect the crystal 12MHz between this pin and XTALO and a 22pF capacitor to VSS.
		T1	I	TIMER1 External Input.
		P3.5	I/O	Bit 5 of Port 3.
18	14	XTALO	O	Crystal output pin. Connect the crystal 12MHz between this pin and XTALI and a 22pF capacitor to VSS.
		T0	I	TIMER0 External Input.
		P3.4	I/O	Bit 4 of Port 3.
---	8	NC		No connect.
19	15	VDD5	Power	5.0V Voltage Input. A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS.
20	16	V18	O	1.8V Voltage Output. A 0.1uF and 1uF (minimum) capacitor should be connected between this pin and VSS.
21	17	VSS	Ground	Power Ground.

12	7	CH0	I	Analog Input Ch0.
		CAP1	I	Capture Input 1
		GPWM	O	General PWM output.
		P1.6	I/O	Bit 6 of Port 1.
11	6	CH1	I	Analog Input Ch1.
		INT0N	I	External Interrupt 0. Low level trigger or falling edge trigger.
		P3.2	I/O	Bit 2 of Port 3.
10	5	CH2	I	Analog Input Ch2.
		INT1N	I	External Interrupt 1. Low level trigger or falling edge trigger.
		P3.3	I/O	Bit 3 of Port 3.
26	25	HWP	I	Hall Latch input (HALL W)
		P0.2	I/O	Bit 2 of Port 0.
27	26	HVP	I	Hall Latch input (HALL V)
		P0.1	I/O	Bit 1 of Port 0.
---	22	VOUT	O	OPA output
---	23	VINN	I	OPA input (-)
---	24	VINP	I	OPA input (+)
28	27	HUP	I	Hall Latch input (HALL U)
		P0.0	I/O	Bit 0 of Port 0.
1	28	OCPN	I	Over current protection. Active-low.
		P0.3	I/O	Bit 3 of Port 0.
2	29	U	O	PWM output. High-side PWM of phase U.
		P1.0	I/O	Bit 0 of Port 1.
3	30	X	O	PWM output. Low-side PWM of phase U.
		P1.1	I/O	Bit 1 of Port 1.
4	31	V	O	PWM output. High-side PWM of phase V.
		P1.2	I/O	Bit 2 of Port 1.
5	32	Y	O	PWM output. Low-side PWM of phase V.
		P1.3	I/O	Bit 3 of Port 1.
6	1	W	O	PWM output. High-side PWM of phase W.
		P1.4	I/O	Bit 4 of Port 1.
7	2	Z	O	PWM output. Low-side PWM of phase W.
		P1.5	I/O	Bit 5 of Port 1.

5. Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Item	Min.	Typ.	Max.
VDD5 Supply Voltage	V_{SS}-0.3V		V_{SS}+6.0V
VDD5 Input Voltage	V_{SS}-0.3V		V_{DD}+0.3V
Θ_{JA} Thermal Resistance, Junction-to-ambient (SSOP-28L)		82℃/W	
Θ_{JA} Thermal Resistance, Junction-to-ambient (QFN32-4x4)		30℃/W	
Storage Temperature	-50℃		150℃
Operating Temperature	-20℃		105℃
I_{OH} Total		-80mA	
I_{OL} Total		80mA	
Total Power Dissipation		500mW	
Electrostatic Discharge Capability – Human Body Mode		2000 (KV)	
Electrostatic Discharge Capability – Machine Mode		200 (V)	

6. D.C. Characteristics

Table 6.1 D.C. Characteristics

Ta=25℃

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	f_{sys}=48MHz	4.5	5.0	5.5	V
V_{18}	V_{18} Output Range	—	Load Current < 10mA	1.62	1.80	1.98	V
I_{DD}	Operating Current	5V	No load, f_{sys}=48Mhz, ADC off, MDE off	—	9	12	mA
V_{IL}	Input Low Voltage for I/O Ports.	—	—	0	—	0.3 V_{DD}	V
V_{IH}	Input High Voltage for I/O Ports.	—	—	0.7 V_{DD}	—	V_{DD}	V
V_{OL}	Output Low Voltage for I/O Ports.	5V	I_{OL}=5mA	—	—	0.5	V
V_{OH}	Output High Voltage for I/O Ports.	5V	I_{OH}=-3.8mA	4.5	—	—	V
R_{PU}	Pull-up Resistance for I/O Ports	5V	—	10	35	50	KΩ
R_{PD}	Pull-down Resistance for I/O Ports	5V	—	10	35	50	KΩ

7. A.C. Characteristics

Table 7.1 A.C. Characteristics

Ta=25℃

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS}	System Frequency	4.5V~5.5V	Ta=-40℃ to 125℃	TBD	48.0	TBD	MHz
			Ta=-20℃ to 85℃	TBD	48.0	TBD	MHz
			Ta=25℃	-1%	48.0	+1%	MHz
f_{TIMER}	Timer Input Pin Frequency	—	—	—	—	4	fsys
t_{INT}	Interrupt Pulse Width	—	—	1	5	10	tsys
t_{V18}	V_{18} Stable Time	—	—	60	120	240	us
t_{RSDT}	System Reset Delay Time(Power On Reset)	—	—	25	50	100	ms

8. OPA Characteristics

Table 8.1 OPA Characteristics

Ta=25℃, V_{DD}= 5V, V_{SS}=GND

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CRM}	Common Mode Input Range		V_{SS}-0.3	—	V_{DD}+0.3	V
V_{OS}	Input Offset Voltage	V_{CM}=V_{SS}	-4.5		4.5	mV
A_{OL}	DC Open-Loop Gain	V_{OUT}=0.3V~V_{DD}-0.3V V_{CM}=V_{SS}	88	112		dB
GBWP	Gain Bandwidth Product	R_L=10KΩ C_L=60 pF		1		MHz
SR	Slew Rate	C_L=60 pF		0.6		V/us

9. A/D Converter Characteristics

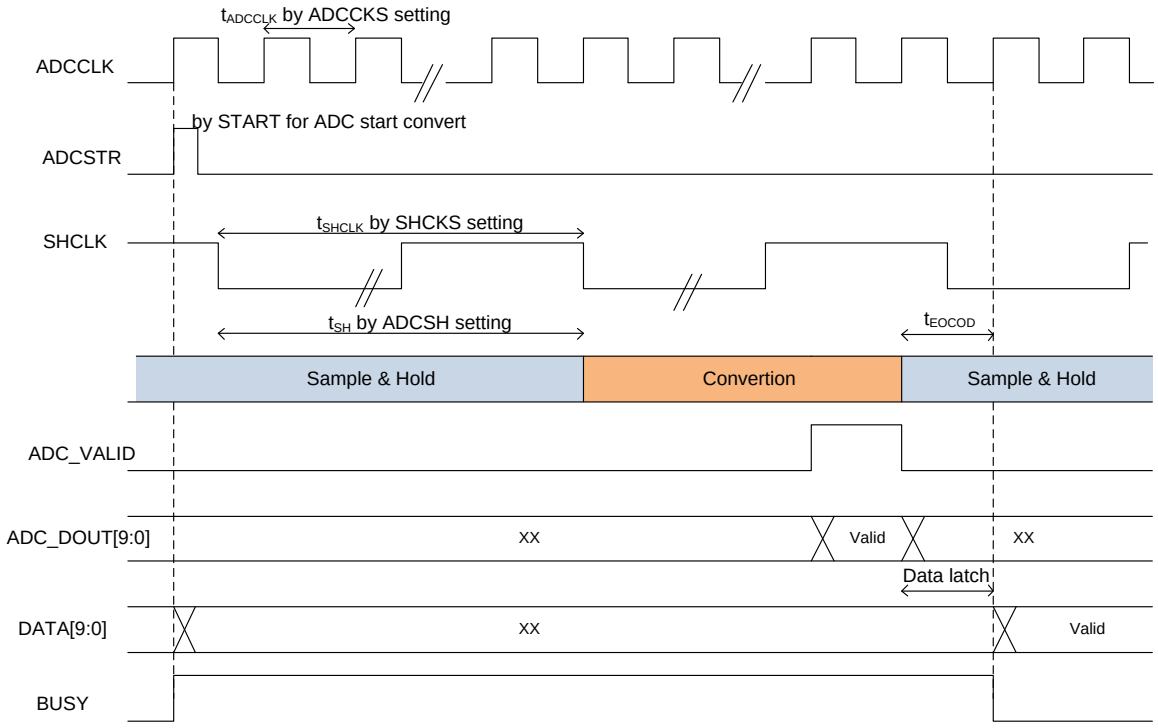


Figure 9.1 A/D Converter Characteristics

Table 9.1 A/D Converter Characteristics

Ta=25℃

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{AD}	Additional Power Consumption if A/D Converter is Used	5V	—	—	4.5	—	mA
I_{ADSTB}	A/D Converter Standby Current	—	Load Current < 10mA	—	—	4	uA
t_{ADCCLK}	A/D Converter Clock Time	—	4MHz	—	0.25	—	us
		—	2MHz	—	0.5	—	us
t_{CONV}	A/D Conversion Time	—	4MHz	—	3.25	—	us
		—	2MHz	—	6.5	—	us
t_{SHCLK}	A/D Sample and Hold Clock Time	—	1MHz	—	1	—	us
		—	500KHz	—	2	—	us
		—	400KHz	—	2.5	—	us
		—	333KHz	—	3	—	us
t_{SH}	A/D Sample and Hold Time	—	1MHz	1	—	2	us
		—	500KHz	2	—	4	us
		—	400KHz	2.5	—	5	us

		—	333KHz	3	—	6	us
DNL	Differential Non-linearity	4.5V	No load, t_{CONV}=2.5us	-1	—	+3	LSB
		5.5V		-1	—	+3	LSB
		4.5V	No load, t_{CONV}=5us	-1	—	+3	LSB
		5.5V		-1	—	+3	LSB
INL	Integral Non-linearity	4.5V	No load, t_{CONV}=2.5us	-4	—	+4	LSB
		5.5V		-4	—	+4	LSB
		4.5V	No load, t_{CONV}=5us	-4	—	+4	LSB
		5.5V		-4	—	+4	LSB
G_{ERR}	Gain Error	—	—	-10	—	+10	LSB

10. Special Function Registers (SFR)

10.1 SFRs Memory Map

Table 10.1 SFRs Memory Map

	8	9	A	B	C	D	E	F	
F8	PINCONG 1	PINCONG2	PINCONG3	PINCONG4	PINCONG5	PINCONG6	RSTS	TAKEY	FF
F0	B	PINSET1	PINSET2	PINSET3	PINSET4	PINSET5	PINSET6	PINSET7	F7
E8	ASUD1_1	ASUD1_2	ASUD1_3	ASUD1_4	ASUD2_1	ASUD2_2	ASUD2_3	ASUD2_4	EF
E0	ACC	AS_MD_CON T	MD0	MD1	MD2	MD3	MD4	MD5	E7
D 8	CAPCONT	VRHALL	SVPWMAMPF T	MD_CONT	ASUR1	ASUR2	ASUR3	ASUR4	D F
D 0	PSW	PFCON	ADCCONT	ADCSTR	-----	ADCD1	ADCD2	SYNC	D7
C 8	T2CON	CAPT_H	CAPT_L	CAPH_H	CAPH_L	-----	-----	-----	C F
C 0	IRCON1	SVPWMANGL	SVPWMANGH	SVPWMAMPL	SVPWMAMPH	FG_CTRL	-----	-----	C7
B8	IEN1	IP1	GPWMCONT	GPWMMAXL	GPWMMAXH	GPWMDYL	GPWMDYH	MIN_DUTY	BF
B0	P3	MPWMCONT1	MPWMCONT2	MPWMINV	TL2	TH2	WDTC	WDTK	B7
A8	IEN0	IP0	MPWMDYVL	MPWMDYVH	MCONT3	MPWMDYWL	MPWMDYWH	IMPMISC_FUN	AF
A0	P2	OCPCONT	MCONT2	MPWM_CYC_ L	MPWM_CYC_ H	MPWMDYUL	MPWMDYUH	MPWMDT	A7
98	SCON	SBUF	SRELL	SRELH	HALLDBT	MCONT1	AOCPCONT	IMPMISC_KEY	9F
90	P1	HALLSET1	HALLSET2	HALLSET3	HALLST	ONE_HALLSE T	ROTORSPEED L	ROTORSPEED H	97
88	TCON	TMOD	TL0	TL1	TH0	TH1	AUX	AS	8F
80	P0	SP	DP0L	DP0H	DP1L	DP1H	RCON	PCON	87
	0	1	2	3	4	5	6	7	

10.2 CGH001A SFRs and Reset Value

Table 10.2 CGH001A SFRs and Reset Value

SYMBOL	DESCRIPTION	DIRECT ADDRESS	RESET VALUE
ACC	Accumulator	E0H	00H
ADCCONT	ADC Control Register	D2H	80H
ADCD1	ADC Data Register 1	D5H	00H
ADCD2	ADC Data Register 2	D6H	00H
ADCSTR	ADC Start Convert and Setting Register	D3H	00H
AOCPCONT	Analog OCP Control Register	9EH	0FH
AS	Angle Shift Control Register	8FH	00H
AS_MD_CONT	ASU and MDU Control Register	E1H	10H
ASUD1_1	ASU Data 1 byte 1	E8H	00H
ASUD1_2	ASU Data 1 byte 2	E9H	00H
ASUD1_3	ASU Data 1 byte 3	EAH	00H
ASUD1_4	ASU Data 1 byte 4	EBH	00H
ASUD2_1	ASU Data 2 byte 1	ECH	00H
ASUD2_2	ASU Data 2 byte 2	EDH	00H
ASUD2_3	ASU Data 2 byte 3	EEH	00H
ASUD2_4	ASU Data 2 byte 4	EFH	00H
ASUR1	ASU Result Register 1	DCH	00H
ASUR2	ASU Result Register 2	DDH	00H
ASUR3	ASU Result Register 3	DEH	00H
ASUR4	ASU Result Register 4	DFH	00H
AUX	Auxiliary	8EH	11H
B	B Register	F0H	00H
CAPCONT	Capture Control Register	D8H	03H
CAPH_H	Capture High-level Count High	CBH	00H
CAPH_L	Capture High-level Count Low	CCH	00H
CAPT_H	Capture Total Count High	C9H	00H
CAPT_L	Capture Total Count Low	CAH	00H
DPTR0:	Data Pointer (2 bytes)		
DP0H	Data Pointer 0 High	83H	00H
DP0L	Data Pointer 0 Low	82H	00H
DPTR1:	Data Pointer 1 (2 bytes)		
DP1H	Data Pointer 1 High	85H	00H
DP1L	Data Pointer 1 Low	84H	00H
FG_CTRL	Frequency Generator Control Register	C5H	00H

GPWMCONT	General PWM Control Register	BAH	00H
GPWMDYH	General PWM Duty Register High	BEH	FFH
GPWMDYL	General PWM Duty Register Low	BDH	FFH
GPWMMAXH	General PWM Max Register High	BCH	00H
GPWMMAXL	General PWM Max Register Low	BBH	02H
HALLDBT	Hall De-bounce Time Register	9CH	0EH
HALLSET1	Hall Setting Register 1	91H	45H
HALLSET2	Hall Setting Register 2	92H	26H
HALLSET3	Hall Setting Register 3	93H	13H
HALLST	Hall Status Register	94H	XXH
IEN0	Interrupt Enable Register 0	A8H	00H
IEN1	Interrupt Enable Register 1	B8H	00H
IMPMISC_FUN	Improve Miscellaneous Function Setting Register	AFH	10H
IMPMISC_KEY	Improve Miscellaneous Function Turn On Key Register	9FH	00H
IP0	Interrupt Priority Register 0	A9H	00H
IP1	Interrupt Priority Register 1	B9H	00H
IRCON1	Interrupt Request Register 1	C0H	00H
MCONT1	Motor Control Register 1	9DH	X0110000B
MCONT2	Motor Control Register 2	A2H	00H
MCONT3	Motor Control Register 3	ACH	03H
MD_CONT	MDU Control Register	DBH	00H
MD0	Multiplication Division Register 0	E2H	00H
MD1	Multiplication Division Register 1	E3H	00H
MD2	Multiplication Division Register 2	E4H	00H
MD3	Multiplication Division Register 3	E5H	00H
MD4	Multiplication Division Register 4	E6H	00H
MD5	Multiplication Division Register 5	E7H	00H
MIN_DUTY	Minimum Duty Limit Register	BFH	00H
MPWMCONT1	MPWM Control Register 1	B1H	00H
MPWMCONT2	MPWM Control Register 2	B2H	00H
MPWMDT	Motor PWM Dead-Time Register	A7H	00H
MPWMDYUH	Motor PWM Duty Register U High (Phase U)	A6H	07H
MPWMDYUL	Motor PWM Duty Register U Low (Phase U)	A5H	FFH
MPWMDYVH	Motor PWM Duty Register V High (Phase V)	ABH	07H
MPWMDYVL	Motor PWM Duty Register V Low (Phase V)	AAH	FFH
MPWMDYWH	Motor PWM Duty Register W High (Phase W)	AEH	07H
MPWMDYWL	Motor PWM Duty Register W Low (Phase W)	ADH	FFH
MPWMINV	MPWM Inverse Selection Register	B3H	00H

MPWM_CYC_H	Motor PWM_CYC High Byte	A4H	00H
MPWM_CYC_L	Motor PWM_CYC Low Byte	A3H	02H
OCPCONT	OCP Control Register	A1H	04H
ONE_HALLSET	One Hall Setting Register	95H	04H
P0	Port 0	80H	FFH
P1	Port 1	90H	FFH
P2	Port 2	A0H	FFH
P3	Port 3	B0H	FFH
PCON	Power Control Register	87H	00H
PFCON	Peripheral Frequency Control Register	D1H	00H
PINCONG1	Pin Configure Register 1	F8H	AAH
PINCONG2	Pin Configure Register 2	F9H	AAH
PINCONG3	Pin Configure Register 3	FAH	A0H
PINCONG4	Pin Configure Register 4	FBH	AAH
PINCONG5	Pin Configure Register 5	FCH	AAH
PINCONG6	Pin Configure Register 6	FDH	A0H
PINSET1	Pin I/O Setting Register 1	F1H	AAH
PINSET2	Pin I/O Setting Register 2	F2H	AAH
PINSET3	Pin I/O Setting Register 3	F3H	0AH
PINSET4	Pin I/O Setting Register 4	F4H	00H
PINSET5	Pin I/O Setting Register 5	F5H	80H
PINSET6	Pin I/O Setting Register 6	F6H	2AH
PINSET7	Pin I/O Setting Register 7	F7H	FFH
PSW	Program Status Word Register	D0H	00H
RCON	Internal RAM Control Register	86H	F0H
ROTORSPEEDH	Rotor Speed Count Register High	97H	FFH
ROTORSPEEDL	Rotor Speed Count Register Low	96H	FFH
RSTS	Reset Source Register	FEH	0AH
SBUF	Serial Port Data Buffer	99H	00H
SCON	Serial Port Control Register	98H	00H
SP	Stack Pointer	81H	07H
SRELH	Serial Port Reload Register High	9BH	00H
SRELL	Serial Port Reload Register Low	9AH	00H
SVPWMAMPFT	SVPWM Amplitude Fine-Tune Register	DAH	00H
SVPWMAMPH	SVPWM Amplitude Register High	C4H	00H
SVPWMAMPL	SVPWM Amplitude Register Low	C3H	00H
SVPWMANGH	SVPWM Angular Register High	C2H	00H
SVPWMANGL	SVPWM Angular Register Low	C1H	00H

SYNC	MDE Sync Register	D7H	00H
T2CON	Timer2 Control Register	C8H	00H
TAKEY	Time Access Key Register	FFH	00H
TCON	Timer 0/1 Control Register	88H	00H
TH0	Timer0 High byte	8CH	00H
TH1	Timer1 High byte	8DH	00H
TH2	Timer2 High byte	B5H	00H
TL0	Timer0 Low byte	8AH	00H
TL1	Timer1 Low byte	8BH	00H
TL2	Timer2 Low byte	B4H	00H
TMOD	Timer 0/1 Mode Register	89H	00H
VRHALL	Virtual Hall Register	D9H	05H
WDTC	Watchdog Timer Control Register	B6H	04H
WDTK	Watchdog Timer Refresh Key	B7H	00H

11. Memory

CGH001A memory structure follows the general 8052 structures.

There are three memory areas: Program Memory (Flash), External Data Memory (XRAM) and Internal Data Memory (IRAM). In addition, **CGH001A** integrates 8Kbytes Flash, 256bytes IRAM and 256bytes XRAM.

11.1. Program Memory

CGH001A contains 8Kbytes of on-chip Flash memory for program storage.

11.2. Data Memory

CGH001A contains 256bytes of general internal data memory (IRAM) and 256 bytes of external data memory (XRAM).

11.2.1 Data Memory (IRAM)(00H~FFH)

The lower 128 bytes of IRAM may be accessed through both direct and indirect addressing. The upper 128 bytes of IRAM and the 128 bytes of SFR registers share the same address space. The upper 128 bytes of data memory may only be accessed using indirect addressing. The SFR registers can only be accessed through direct addressing. The lowest 32 bytes (00H -1FH) of data memory are grouped into 4 banks of 8 registers each. The **RS0** and **RS1** bits (**PSW**.3 and**PSW**.4) select which register bank is in use. Instructions using register addressing will only access the currently specified bank.

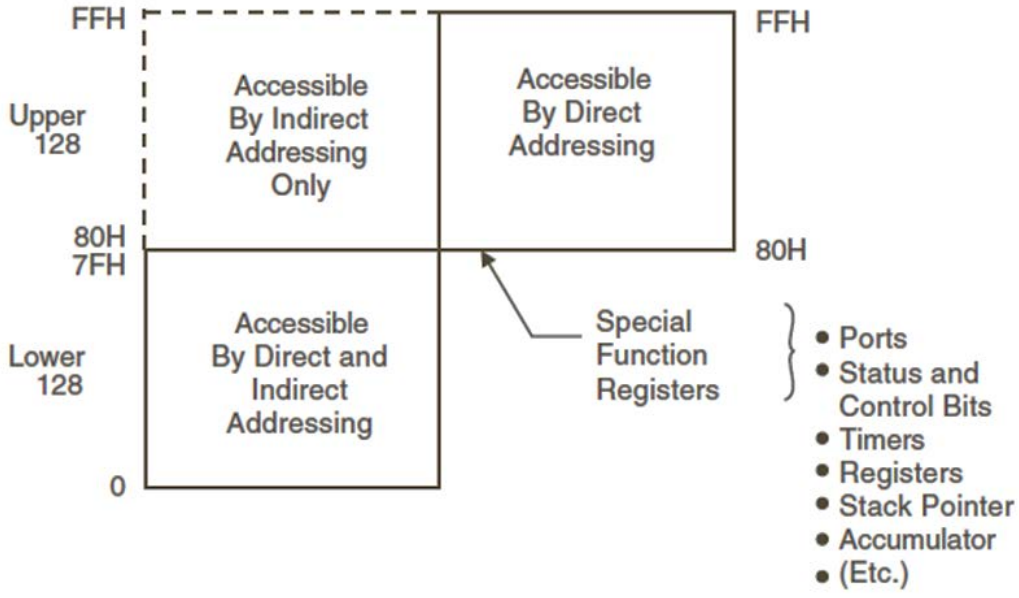


Figure 11.2.1 Data Memory (IRAM)(00H~FFH)

11.2.2 Data Memory (XRAM)(F000H~F0FFH)

External addresses F000H to F0FFh contain the on-chip expanded SRAM. This memory can be accessed via external direct addressing mode (with **MOVX** instructions). The address space of instruction **MOVX** @Ri, A (i=0,1) is determined by **RCON** [7:0] of SFR 86H**RCON**(internal RAM control register). The default setting of **RCON** [7:0] is F0h (page0). One page of XRAM is 256 bytes.

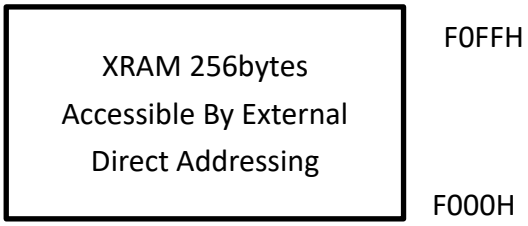


Figure 11.2.2 Data Memory (XRAM)(F000H~F0FFH)

12. Instruction Set

CGH001A is fully binary compatible with the MCS-51 instruction set.

Table 12.1 Instruction Set

Arithmetic operations	Description	Bytes	Cycles	Hex Code
ADD A,Rn	Add register to accumulator	1	1	0x28-0x2F
ADD A,direct	Add directly addressed data to accumulator	2	2	0x25
ADD A,@Ri	Add indirectly addressed data to accumulator	1	2	0x26-0x27
ADD A,#data	Add immediate data to accumulator	2	2	0x24
ADDC A,Rn	Add register to accumulator with carry	1	1	0x38-0x3F
ADDC A,direct	Add directly addressed data to accumulator with carry	2	2	0x35
ADDC A,@Ri	Add indirectly addressed data to accumulator with carry	1	2	0x36-0x37
ADDC A,#data	Add immediate data to accumulator with carry	2	2	0x34
SUBB A,Rn	Subtract register from accumulator with borrow	1	1	0x98-0x9F
SUBB A,direct	Subtract directly addressed data from accumulator with borrow	2	2	0x95
SUBB A,@Ri	Subtract indirectly addressed data from accumulator with borrow	1	2	0x96-0x97
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2	0x94
INC A	Increment accumulator	1	1	0x04
INC Rn	Increment register	1	2	0x08-0x0F
INC direct	Increment directly addressed location	2	3	0x05
INC @Ri	Increment indirectly addressed location	1	3	0x06-0x07
INC DPTR	Increment data pointer	1	1	0xA3
DEC A	Decrement accumulator	1	1	0x14
DEC Rn	Decrement register	1	2	0x18-0x1F
DEC direct	Decrement directly addressed location	2	3	0x15
DEC @Ri	Decrement indirectly addressed location	1	3	0x16-0x17

MUL AB	Multiply A and B	1	5	0xA4
DIV	Divide A by B	1	5	0x84
DA A	Decimally adjust accumulator	1	1	0xD4

Logic operations	Description	Bytes	Cycles	Hex Code
ANL A,Rn	AND register to accumulator	1	1	0x58-0x5F
ANL A,direct	AND directly addressed data to accumulator	2	2	0x55
ANL A,@Ri	AND indirectly addressed data to accumulator	1	2	0x56-0x57
ANL A,#data	AND immediate data to accumulator	2	2	0x54
ANL direct,A	AND accumulator to directly addressed location	2	3	0x52
ANL direct,#data	AND immediate data to directly addressed location	3	4	0x53
ORL A,Rn	OR register to accumulator	1	1	0x48-0x4F
ORL A,direct	OR directly addressed data to accumulator	2	2	0x45
ORL A,@Ri	OR indirectly addressed data to accumulator	1	2	0x46-0x47
ORL A,#data	OR immediate data to accumulator	2	2	0x44
ORL direct,A	OR accumulator to directly addressed location	2	3	0x42
ORL direct,#data	OR immediate data to directly addressed location	3	4	0x43
XRL A,Rn	Exclusive OR register to accumulator	1	1	0x68-0x6F
XRL A,direct	Exclusive OR directly addressed data to accumulator	2	2	0x65
XRL A,@Ri	Exclusive OR indirectly addressed data to accumulator	1	2	0x66-0x67
XRL A,#data	Exclusive OR immediate data to accumulator	2	2	0x64
XRL direct,A	Exclusive OR accumulator to directly addressed location	2	3	0x62
XRL direct,#data	Exclusive OR immediate data to directly addressed location	3	4	0x63
CLR A	Clear accumulator	1	1	0xE4
CPL A	Complement accumulator	1	1	0xF4
RL A	Rotate accumulator left	1	1	0x23
RLC A	Rotate accumulator left through carry	1	1	0x33
RR A	Rotate accumulator right	1	1	0x03
RRC A	Rotate accumulator right through carry	1	1	0x13
SWAP A	Swap nibbles within the accumulator	1	1	0xC4

Data transferoperations	Description	Bytes	Cycles	Hex Code
MOV A,Rn	Move register to accumulator	1	1	0xE8-0xEF
MOV A,direct	Move directly addressed data to accumulator	2	2	0xE5
MOV A,@Ri	Move indirectly addressed data to accumulator	1	2	0xE6-0xE7
MOV A,#data	Move immediate data to accumulator	2	2	0x74

MOV Rn,A	Move accumulator to register	1	2	0xF8-0xFF
MOV Rn,direct	Move directly addressed data to register	2	4	0xA8-0xAF
MOV Rn,#data	Move immediate data to register	2	2	0x78-0x7F
MOV direct,A	Move accumulator to direct	2	3	0xF5
MOV direct,Rn	Move register to direct	2	3	0x88-0x8F
MOV direct1,direct2	Move directly addressed data to directly addressed location	3	4	0x85
MOV direct,@Ri	Move indirectly addressed data to directly addressed location	2	4	0x86-0x87
MOV direct,#data	Move immediate data to directly addressed location	3	3	0x75
MOV @Ri,A	Move accumulator to indirectly addressed location	1	3	0xF6-0xF7
MOV @Ri,direct	Move directly addressed data to indirectly addressed location	2	5	0xA6-0xA7
MOV @Ri,#data	Move immediate data to in directly addressed location	2	3	0x76-0x77
MOV DPTR,#data16	Load data pointer with a 16-bit immediate	3	3	0x90
MOVC A,@A+DPTR	Load accumulator with a code byte relative to DPTR	1	3	0x93
MOVC A,@A+PC	Load accumulator with a code byte relative to PC	1	3	0x83
MOVX A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	3	0xE2-0xE3
MOVX A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	3	0xE0
MOVX @Ri,A	Move accumulator to external RAM (8-bit addr.)	1	4	0xF2-0xF3
MOVX @DPTR,A	Move accumulator to external RAM (16-bit addr.)	1	4	0xF0
PUSH direct	Push directly addressed data onto stack	2	4	0xC0
POP direct	Pop directly addressed location from stack	2	3	0xD0
XCH A,Rn	Exchange register with accumulator	1	2	0xC8-0xCF
XCH A,direct	Exchange directly addressed location with accumulator	2	3	0xC5
XCH A,@Ri	Exchange indirect RAM with accumulator	1	3	0xC6-0xC7
XCHD A,@Ri	Exchange low-order nibbles of indirect and accumulator	1	3	0xD6-0xD7

Program branches	**Description**	**Bytes**	**Cycles**	**Hex Code**
ACALL addr11	Absolute subroutine call	2	6	xxx10001b
LCALL addr16	Long subroutine call	3	6	0x12
RET	Return from subroutine	1	4	0x22
RETI	Return from interrupt	1	4	0x32
AJMP addr11	Absolute jump	2	3	xxx00001b

LJMP addr16	Long jump	3	4	0x02
SJMP rel	Short jump (relative address)	2	3	0x80
JMP @A+DPTR	Jump indirect relative to the DPTR	1	2	0x73
JZ rel	Jump if accumulator is zero	2	3	0x60
JNZ rel	Jump if accumulator is not zero	2	3	0x70
JC rel	Jump if carry flag is set	2	3	0x40
JNC	Jump if carry flag is not set	2	3	0x50
JB bit,rel	Jump if directly addressed bit is set	3	4	0x20
JNB bit,rel	Jump if directly addressed bit is not set	3	4	0x30
JBC bit,rel	Jump if directly addressed bit is set and clear bit	3	4	0x10
CJNE A,direct,rel	Compare directly addressed data to accumulator and jump if not equal	3	4	0xB5
CJNE A,#data,rel	Compare immediate data to accumulator and jump if not equal	3	4	0xB4
CJNE Rn,#data,rel	Compare immediate data to register and jump if not equal	3	4	0xB8-0xBF
CJNE @Ri,#data,rel	Compare immed. to ind. and jump if not equal	3	4	0xB6-0xB7
DJNZ Rn,rel	Decrement register and jump if not zero	2	3	0xD8-0xDF
DJNZ direct,rel	Decrement directly addressed location and jump if not zero	3	4	0xD5
NOP	No operation	1	1	0

Boolean manipulation	**Description**	**Bytes**	**Cycles**	**Hex Code**
CLR C	Clear carry flag	1	1	0xC3
CLR bit	Clear directly addressed bit	2	3	0xC2
SETB C	Set carry flag	1	1	0xD3
SETB bit	Set directly addressed bit	2	3	0xD2
CPL C	Complement carry flag	1	1	0xB3
CPL bit	Complement directly addressed bit	2	3	0xB2
ANL C,bit	AND directly addressed bit to carry flag	2	2	0x82
ANL C,/bit	AND complement of directly addressed bit to carry	2	2	0xB0
ORL C,bit	OR directly addressed bit to carry flag	2	2	0x72
ORL C,/bit	OR complement of directly addressed bit to carry	2	2	0xA0
MOV C,bit	Move directly addressed bit to carry flag	2	2	0xA2
MOV bit,C	Move carry flag to directly addressed bit	2	3	0x92

13. MCU

13.1 8051 Engine

Table 13.1 8051 Engine

SFR	Description	address	Reset value
ACC	Accumulator	E0H	00H
B	B Register	F0H	00H
PSW	Program Status Word Register	D0H	00H
SP	Stack Pointer	81H	07H
DP0H	Data Pointer 0 High	83H	00H
DP0L	Data Pointer 0 Low	82H	00H
DP1H	Data Pointer 1 High	85H	00H
DP1L	Data Pointer 1 Low	84H	00H
AUX	Auxiliary	8EH	11H
RCON	Internal RAM Control Register	86H	F0H

13.1.1 ACC (Accumulator)

The most important of all special function registers, that's the first comment about **Accumulator** which is also known as **ACC** or **A.** The **Accumulator** (sometimes referred to as Register A also) holds the result of most of arithmetic and logic operations.

Table 13.1.1 ACC (Accumulator)

ACC Address = E0H Reset Value = 00000000B

Accumulator

	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.1.2 B (B Register)

The **B** register is used during multiplying and division instructions. It can also be used as a scratch-pad register to hold temporary data.

Table 13.1.2 B Register

B Address = F0H Reset Value = 00000000B

B Register

	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.1.3 PSW (Program Status Word Register)

The **PSW** register contains status bits that reflect the current state of the CPU. Note that the Parity bit can only be modified by hardware upon the state of **ACC** register.

Table 13.1.3.1 PSW

PSW				Address = D0H		Reset Value = 00000000B		
Program Status Word Register								
	CY	AC	F0	RS1	RS0	OV	F1	P
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

CY	Carry flag : Carry bit in arithmetic operations and accumulator for Boolean operations.
AC	Auxiliary Carry flag : Set if there is a carry-out from third bit of Accumulator in BCD Operations.
F0	General purpose Flag0 : General purpose flag available for user.
RS1	Register bank select control bit 1, used to select working register bank.
RS0	Register bank select control bit 0, used to select working register bank.
OV	Overflow flag : Set in case of overflow in Accumulator during arithmetic operations.
F1	General purpose Flag 1 : General purpose flag available for user.
P	Parity flag : Reflects the number of ‘1’s in the Accumulator. P = ‘1’ if Accumulator contains an odd number of ‘1’s P = ‘0’ if Accumulator contains an even number of ‘1’s

The state of **RS1** and **RS0** bits selects the working register bank as follows:

Table 13.1.3.2 RS1

RS1	**RS0**	**Selected Register Bank**	**Location**
0	0	Bank 0	00H – 07H
0	1	Bank 1	08H – 0FH
1	0	Bank 2	10H – 17H
1	1	Bank 3	18H – 1FH

13.1.4 SP (Stack Pointer)

This register points to the top of stack in internal data memory space. It is used to store the return address of program before executing interrupt routine or subprograms. The **SP** is incremented before executing **PUSH** or **CALL** instruction and it is decremented after executing **POP** or **RET(I)** instruction (it always points the top of stack). A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08.

Table 13.1.4 Stack Pointer

SP	Address = 81H					Reset Value = 00000111B		
Stack Pointer								
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.1.5 DP0 (Data Pointer 0)

These registers are intended to hold 16-bit address in the indirect addressing mode used by **MOVX** (move external memory), **MOVC** (move program memory) or **JMP** (computed branch) instructions. They may be manipulated as 16-bit register or as two separate 8-bit registers. **DP0H** holds higher byte and **DP0L** holds lower byte of indirect address.

It is generally used to access external code or data space, e.g.:

MOVCA,@**A**+**DPTR** (code space)

MOVA,@**DPTR** (data space)

Table 13.1.5 DP0 (Data Pointer 0)

DP0H	Address = 83H					Reset Value = 00000000B		
Data Pointer 0 High								
	DP0H[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DP0L	Address = 82H					Reset Value = 00000000B		
Data Pointer 0 Low								
	DP0L[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.1.6 DP1 (Data Pointer 1)

The dual data pointer accelerates the movement of block data. The standard **DPTR** is a 16-bit register that is used to address external memory, or peripherals. The standard data pointer is called **DPTR0** and the second data pointer is called **DPTR1**. The data pointer select bit chooses the active pointer. The data pointer select bit (**DPS**) is located in the LSB of **AUX** register (AUX.1).

The user switches between **DPTR0** and **DPTR1** by toggling the **DPS** bit. All DPTR-related instructions use the currently selected **DPTR** for any activity.

Table 13.1.6 DP1 (Data Pointer 1)

DP1H			Address = 85H		Reset Value = 00000000B			
Data Pointer 1 High								
	DP1H[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DP1L			Address = 84H		Reset Value = 00000000B			
Data Pointer 1Low								
	DP1L[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.1.7 AUX (Auxiliary Register)

Table 13.1.7 AUX(Auxiliary Register)

AUX			Address = 8EH		Reset Value = 00010001B		
Auxiliary Register							
	-----	-----	-----	ITS	SMOD	BRS	DPS	CP
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R/W	R/W	R/W	R/W	R

ITS	MCU instruction timing select. : 0:1T 1:2T
SMOD	Serial Port (UART) baud rate select.
BRS	Serial Port (UART) baud rate generator select.
DPS	Data pointer register select : 0 : Select DPTR Register DP0H, DP0L 1 : Select DPTR Register DP1H, DP1L
CP	Code protect : 0 : Non-protect 1: Protect

13.1.8 RCON (Internal RAM Control Register)

256 bytes of on-chip expanded RAM are provided and can be accessed by external memory addressing method only (instruction **MOVX**). The address space of instruction **MOVX** @Ri, **A** (i= 0,1) is determined by **RCON** [7:0] of **RCON**. The default setting of **RCON** [7:0] is F0H.

Table 13.1.8 RCON (Internal RAM Control Register)

RCON			Address = 86H			Reset Value = 11110000B	
Internal RAM Control Register							
	RCON[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.2 GPIO

Four I/O ports are available: **Port0**, **Port1**, **Port2**, and **Port3**.

All 25port pins on **CGH001A** can configure to one of four modes : quasi-bidirectional (standard 8051 port outputs),push-pull output, open drain output, or input-only. All port pins default to input-only mode after reset.

Two configuration registers (**PINSETx**, **PINCONFGx**) for each port select the output mode for each port pin.

Table 13.2 GPIO

SFR	Description	address	Reset value
P0	Port 0	80H	FFH
P1	Port 1	90H	FFH
P2	Port 2	A0H	FFH
P3	Port 3	B0H	FFH
PINCONG1	Pin Configure Register 1	F8H	AAH
PINCONG2	Pin Configure Register 2	F9H	AAH
PINCONG3	Pin Configure Register 3	FAH	A0H
PINCONG4	Pin Configure Register 4	FBH	AAH
PINCONG5	Pin Configure Register 5	FCH	AAH
PINCONG6	Pin Configure Register 6	FDH	A0H
PINSET1	Pin I/O Setting Register 1	F1H	AAH
PINSET2	Pin I/O Setting Register 2	F2H	AAH
PINSET3	Pin I/O Setting Register 3	F3H	0AH
PINSET4	Pin I/O Setting Register 4	F4H	00H
PINSET5	Pin I/O Setting Register 5	F5H	80H
PINSET6	Pin I/O Setting Register 6	F6H	2AH
PINSET7	Pin I/O Setting Register 7	F7H	FFH

13.2.1 Port

Table 13.2.1 Port

P0 Address = 80H Reset Value = 11111111B

Port 0

	-----	-----	-----	-----	P0.3	P0.2	P0.1	P0.0
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	R/W	R/W	R/W	R/W

P1 Address = 90H Reset Value = 11111111B

Port 1

	-----	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P2 Address = A0H Reset Value = 11111111B

Port 2

	P2.7	P2.6	P2.5	P2.4	P2.3	-----	-----	-----
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	X	X	X

P3 Address = B0H Reset Value = 11111111B

Port 3

	-----	-----	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

13.2.2 PINCONG (Pin Configure Register)

Table 13.2.2 PINCONG (Pin Configure Register)

PINCONG1 Address = F8H Reset Value = 10101010B

Pin Configure Register 1

	CH4CONG[1:0]		CH5CONG[1:0]		CH6CONG[1:0]		CH7CONG[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)

01 : Push-pull output

10 : Input-only (High impedance)

11 : Open drain output

PINCONG2 Address = F9H Reset Value = 10101010B

Pin Configure Register 2

	CH0CONG[1:0]		CH1CONG[1:0]		CH2CONG[1:0]		CH3CONG[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)
01 : Push-pull output
10 : Input-only (High impedance)
11 : Open drain output

PINCONG3 Address = FAH Reset Value = 10100000B

Pin Configure Register 3

	XCONG[1:0]		UCONG[1:0]		XTALOCONG[1:0]		XTALICONG[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)
01 : Push-pull output
10 : Input-only (High impedance)
11 : Open drain output

PINCONG4 Address = FBH Reset Value = 10101010B

Pin Configure Register 4

	ZCONG[1:0]		WCONG[1:0]		YCONG[1:0]		VCONG[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)
01 : Push-pull output
10 : Input-only (High impedance)
11 : Open drain output

PINCONG5 Address = FCH Reset Value = 10101010B

Pin Configure Register 5

	OCPNCONG[1:0]		HWPCONG[1:0]		HVPCONG[1:0]		HUPCONG[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)
01 : Push-pull output
10 : Input-only (High impedance)
11 : Open drain output

PINCONG6 Address = FDH Reset Value = 00000000B

Pin Configure Register 6

	---	---	---	---	RXCONG[1:0]		TXCONG[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	R/W	R/W	R/W	R/W

00 :	Quasi-bidirectional(standard 8051 port outputs)
01 :	Push-pull output
10 :	Input-only (High impedance)
11 :	Open drain output

13.2.3 PINSET (Pin I/O Setting Register)

Table 13.2.3 PINSET (Pin I/O Setting Register)

PINSET1 Address = F1H Reset Value = 10101010B

Pin I/O Setting Register 1

	CH4SET[1:0]		CH5SET[1:0]		CH6SET[1:0]		CH7SET[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	X	X	R/W	R/W	X	X

00 : No pull

01 : Pull down

10 : Pull up

11 : No pull

PINSET2 Address = F2H Reset Value = 10101010B

Pin I/O Setting Register 2

	CH0SET[1:0]		CH1SET[1:0]		CH2SET[1:0]		CH3SET[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	X	X	R/W	R/W	X	X

00 : No pull

01 : Pull down

10 : Pull up

11 : No pull

PINSET3 Address = F3H Reset Value = 00001010B

Pin I/O Setting Register 3

	XSET[1:0]		USET[1:0]		XTALOSET[1:0]		XTALISET[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : No pull

01 : Pull down

10 : Pull up

11 : No pull

PINSET4 Address = F4H Reset Value = 00000000B

Pin I/O Setting Register 4

	ZSET[1:0]		WSET[1:0]		YSET[1:0]		VSET[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : No pull

01 : Pull down

10 : Pull up

11 : No pull

PINSET5 Address = F5H Reset Value = 10000000B

Pin I/O Setting Register 5

	OCPNSET[1:0]		HWPSET[1:0]		HVPSET[1:0]		HUPSET[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : No pull

01 : Pull down

10 : Pull up

11 : No pull

PINSET6 Address = F6H Reset Value = 00101010B

Pin I/O Setting Register 6

	-----	-----	MDES	GPWMS	RXSET[1:0]		TXSET [1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

TXSET[1:0], RXSET[1:0], HUNSET[1:0]

00 : No pull

01 : Pull down

10 : Pull up

11 : No pull

GPWMS: GPWM Port Select

0 : CH0 is GPIO or AD

1 : CH0 is GPWM

MDES: Motor Driving Engine Port Select

0 : U, V, W, X, Y, Z, HUP, HVP, HWP, and OVI_B are GPIO

1 : U, V, W, X, Y, Z, HUP, HVP, HWP, and OVI_B are MDE interface

PINSET7 Address = F7H Reset Value = 11111111B

Pin I/O Setting Register 7

	OCPNDBT[1:0]		HWPDBT[1:0]		HVPDBT[1:0]		HUPDBT[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PIN De-bounce time

00 : 0nS

01 : 250nS

10 : 500nS

11 : 1000nS

13.3 Clock Structure

The clock source of CGH001A uses an internal oscillator. The internal clock source (on-chip oscillator) is run at 12MHz. The choice of internal, clock source is setting by **Writer**.

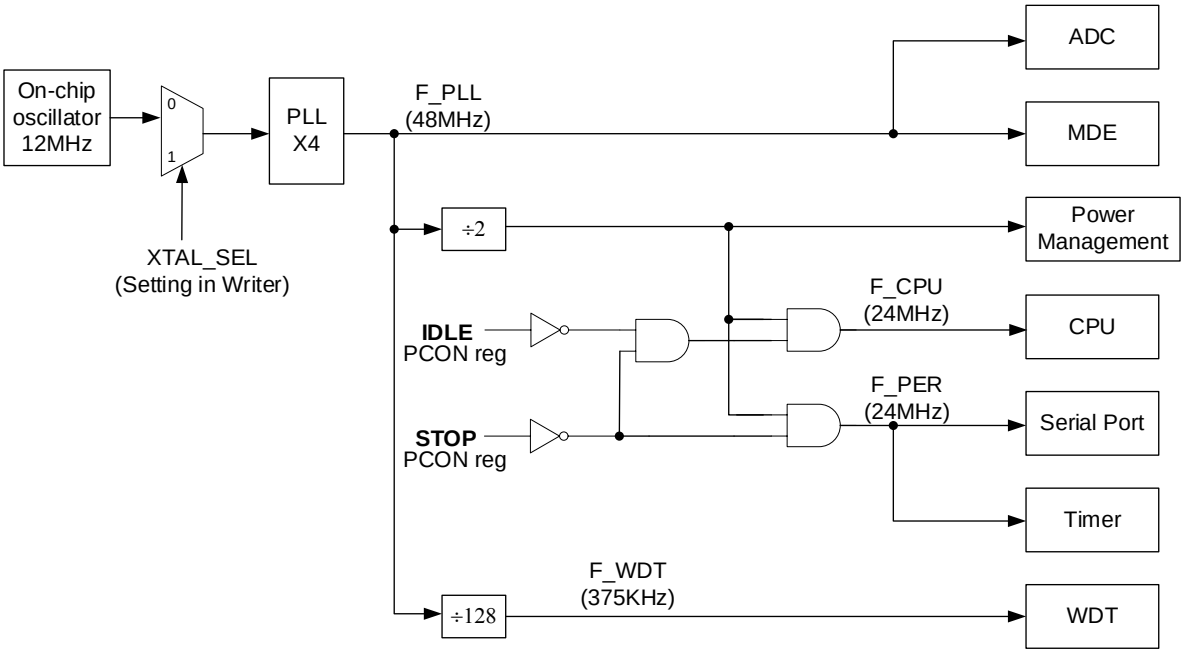


Figure 13.3 Clock Structure

13.4 Timer

The **CGH001A** has three 16-bit timer/counter registers: **Timer0**, **Timer1** and **Timer2**. All can be configured for counter, or timer, operations.

In addition to the “timer” or “counter” selection, **Timer0** and **Timer1** have four operating modes from which to select which are selected by bit-pairs (**M1**, **M0**) in **TMOD**. Modes 0, 1,and 2 are the same for both timer/counters. Mode 3 is different.

Table 13.4.1 Timer Modes

	Timer0	**Timer1**	**Timer2**
Mode 0	13-bit timer/counter	13-bit timer/counter	13-bit timer/counter
Mode 1	16-bit timer/counter	16-bit timer/counter	16-bit timer/counter
Mode 2	8-bit auto-reload timer/counter	8-bit auto-reload timer/counter	8-bit auto-reload timer/counter
Mode 3	two independent 8-bit timers/counters	stop	8-bit timers/counters

Two Special Function registers (**TMOD** and **TCON**) are used to select the appropriate mode.

Table 13.4.2 Timer Related SFR

SFR	**Description**	**address**	**Reset value**
PFCON	Peripheral Frequency Control Register	D1H	00H
TMOD	Timer 0/1 Mode Register	89H	00H
TCON	Timer 0/1 Control Register	88H	00H
T2CON	Timer2 Control Register	C8H	00H
TH0	Timer0 High byte	8CH	00H
TL0	Timer0 Low byte	8AH	00H
TH1	Timer1 High byte	8DH	00H
TL1	Timer1 Low byte	8BH	00H
TH2	Timer2 High byte	B5H	00H
TL2	Timer2 Low byte	B4H	00H

13.4.1 PFCON (Peripheral Frequency Control Register)

Table 13.4.1.1 PFCON (Peripheral Frequency Control Register)

PFCON Address = D1H Reset Value = 00000000B

Peripheral Frequency Control Register

	-----	-----	SRELPS[1:0]		T1PS[1:0]		T0PS[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

SRELPS[1:0]	Serial port (UART) Prescaler select : 00 :F_PER/64 01 :F_PER/32 10 :F_PER/16 11 :F_PER/8
T1PS[1:0]	Timer1(T1) Prescaler select : 00 :F_PER/12 01 :F_PER 10 :F_PER/96 11 :-----
T0PS[1:0]	Timer0(T0) Prescaler select : 00 :F_PER/12 01 :F_PER 10 :F_PER/96 11 :-----

13.4.2 TMOD (Timer 0/1 Mode Register)

TMOD register is used in configuration of MCU**Timer0** and **Timer1**.

Table 13.4.2 TMOD (Timer 0/1 Mode Register)

TMOD Address = 89H Reset Value = 00000000B

Timer 0/1 Mode Register

	GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

GATE1	Timer1 gate control : If set, enables external gate control (pin **INT1N**) for Counter1. When **INT1N** is high, and TR1 bit is set, the Counter1 is incremented every falling edge on **INT1N** input pin
C/T1	Timer1 counter/timer select : 0 : Timer 1 : Counter
GATE0	Timer 0 gate control : If set, enables external gate control (pin **INT0N**) for Counter0. When **INT0N** is high, and TR0 bit is set, the Counter0 is incremented every falling edge on**INT0N** input pin
C/T0	Timer0 counter/timer select : 0 : Timer 1 : Counter

T1M1 /T0M1	T1M0 /T0M0	Mode	Function
0	0	Mode0	13-bit Counter/Timer, with 5 lower bits in TL0 (TL1) register and 8 bits in TH0 (TH1) register (for Timer0 or Timer1, respectively). The 3 high-order bits of TL0 (TL1) are zeroed whenever Mode 0 is enabled. (Not auto-reload)
0	1	Mode1	16-bit Counter/Timer. (Not auto-reload)
1	0	Mode2	8 -bit auto-reload Counter/Timer. The reload value is kept in TH0 (TH1), while TL0 (TL1) is incremented every clock cycle. Reloaded from TH0 (TH1) at overflow.
1	1	Mode3	For Timer1: Timer1 is stopped. For Timer0: Timer0 acts as two independent 8 bit Timers / Counters – TL0, TH0. (Not auto-reload)

13.4.3 TCON (Timer 0/1Control Register)

TCON register is used to control operation of these modules.**CGH001A** includes two external digital interrupt sources **INT0N** and **INT1N**), with dedicated interrupt sources. **INT0N** and **INT1N** are configurable as falling edge or low level. The **IT0** and **IT1** bits in **TCON** select level- or edge-sensitive.**IE0** and **IE1** in the **TCON** register serve as the interrupt-pending flags for the **INT0N**and **INT1N** external interrupts, respectively.

Table 13.4.3 TCON (Timer 0/1Control Register)

TCON Address = 88H Reset Value = 00000000B

Timer 0/1 Control Register

	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TF1	Timer1 overflow flag : Bit set by hardware when Timer1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR1	Timer1 run control : 0 : Stop 1 : Run
TF0	Timer0 overflow flag : Bit set by hardware when Timer1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR0	Timer0run control : 0 : Stop 1 : Run
IE1	External interrupt 1 flag : Set by hardware, when External interrupt (**INT1N**) is observed. Cleared by hardware when interrupt is processed.
IT1	External interrupt 1 type control : 0 : External interrupt 1 is activated at low level on input pin 1 : External interrupt 1 is activated at falling edge on input pin
IE0	External interrupt 0 flag : Set by hardware, when External interrupt (**INT0N**) is observed. Cleared by hardware when interrupt is processed.
IT0	External interrupt 0 type control : 0 : External interrupt 0 is activated at low level on input pin 1 : External interrupt 0 is activated at falling edge on input pin

The **TF0**, **TF1** (**Timer0** and**Timer1** overflow flags), **IE0** and **IE1** (External interrupt 0 and 1 flags) will be automatically cleared by hardware when the corresponding service routine is called.

13.4.4 T2CON (Timer2 Control Register)

T2CON is used to control **Timer2**run/stop, mode, prescaler.

Table 13.4.4 T2CON (Timer2 Control Register)

T2CON Address = C8H Reset Value = 00000000B

Timer2 Control Register

	-----	-----	TF2	TR2	T2M1	T2M0	T2PS1	T2PS0
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

TF2	Timer2 overflow flag : Bit set by hardware when Timer2 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR2	Timer2run control : 0 : Stop 1 : Run
T2PS[1:0]	Timer2(T2) Prescaler select : 00 :F_PER/12 01 : F_PER 10 : F_PER/96 11 :-----

T2M1	T2M0	Mode	Function
0	0	Mode0	13-bit Timer, with 5 lower bits in TL2 register and 8 bits in TH2 register.(Not auto-reload)
0	1	Mode1	16-bit Timer. (Not auto-reload)
1	0	Mode2	8 -bit auto-reload Timer. The reload value is kept in TH2, while TL2 is incremented every clock cycle. Reloaded from TH2 at overflow.
1	1	Mode3	8 bit Timers. (Not auto-reload)

13.4.5 Timer0 Mode 0

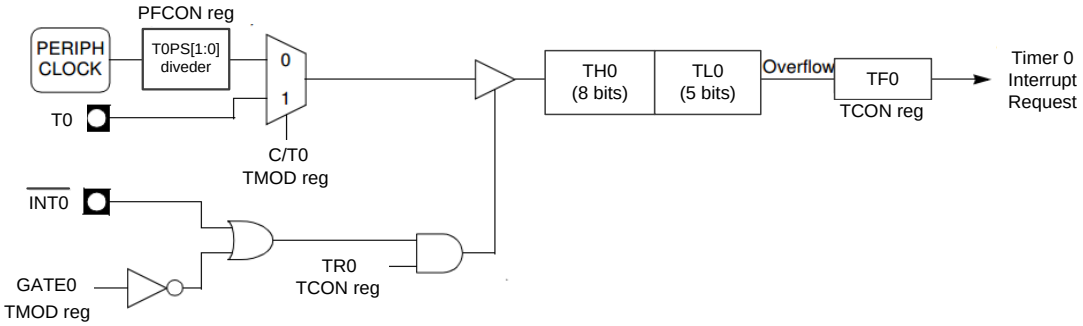


Figure 13.4.5 Timer0 Mode 0

13.4.6 Timer0 Mode 1

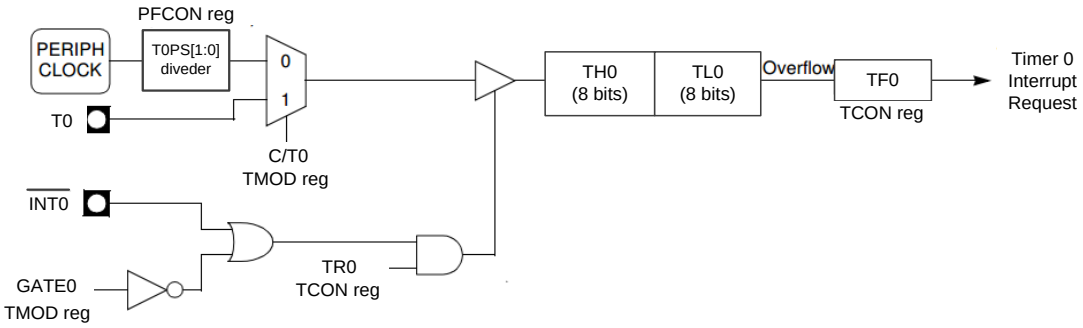


Figure 13.4.6 Timer0 Mode 1

13.4.7 Timer0 Mode 2

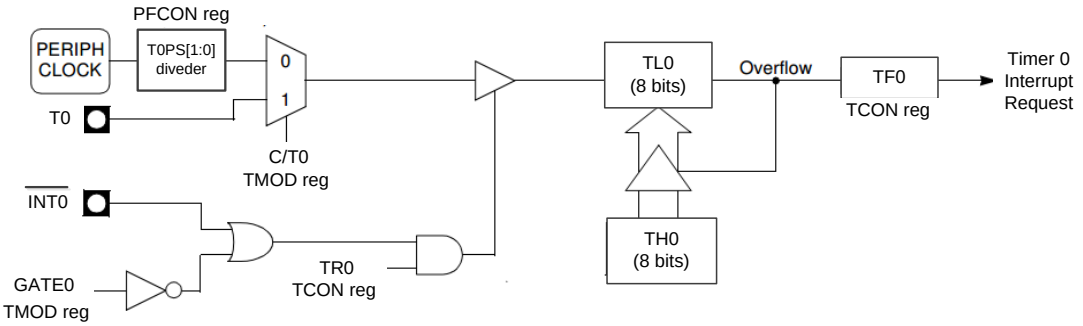


Figure 13.4.7 Timer0 Mode 2

13.4.8 Timer0 Mode 3

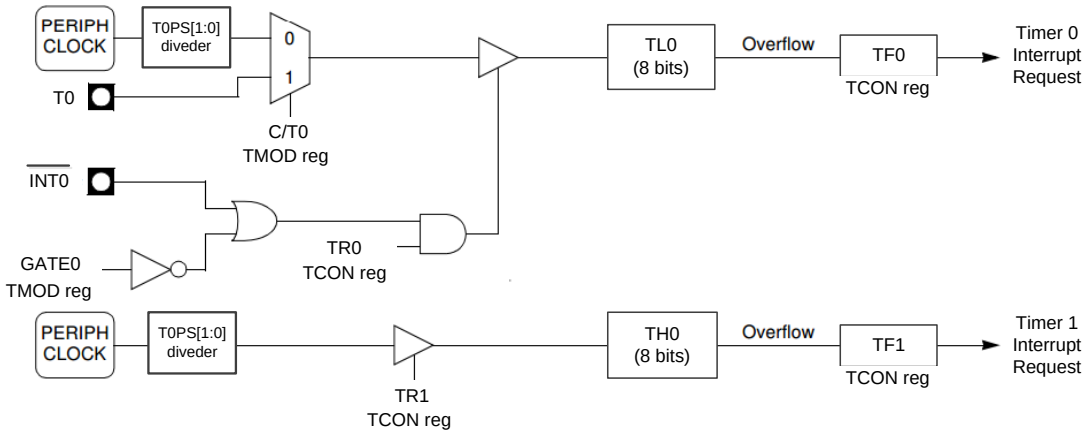


Figure 13.4.8 Timer0 Mode 3

13.4.9 Timer1 Mode 0

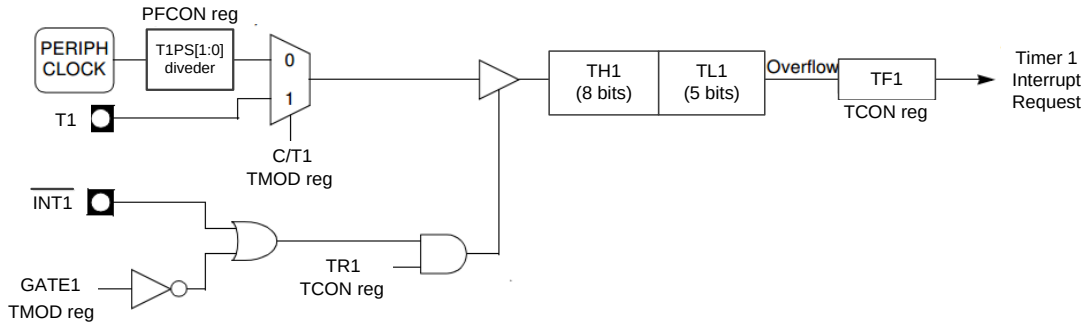


Figure 13.4.9 Timer1 Mode 0

13.4.10 Timer1 Mode 1

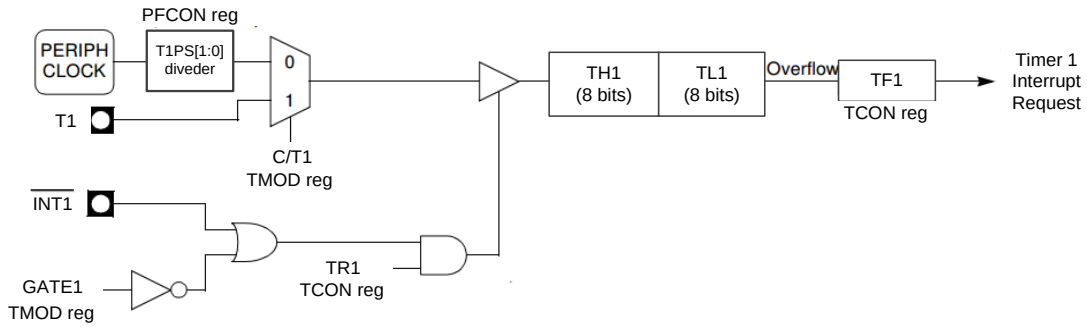


Figure 13-4.10 Timer1 Mode 1

13.4.11 Timer1 Mode 2

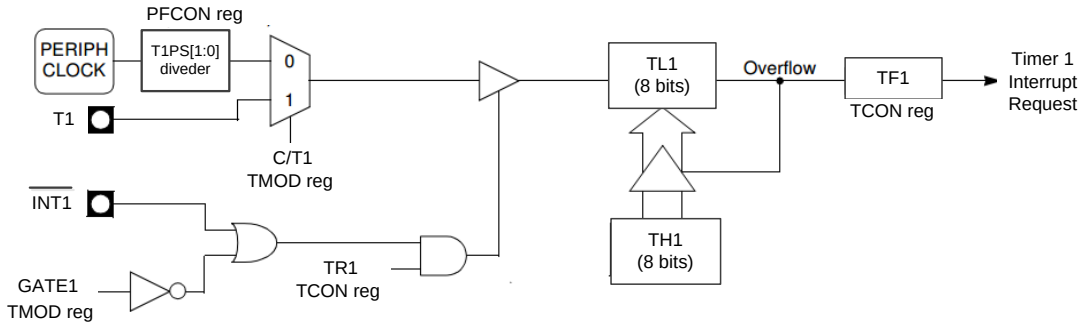


Figure 13.4.11 Timer1 Mode 2

13.4.12 Timer2 Mode 0

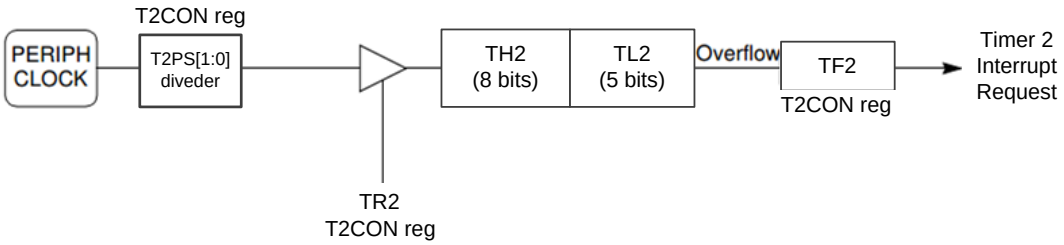


Figure 13.4.12 Timer2 Mode 0

13.4.13 Timer2 Mode 1

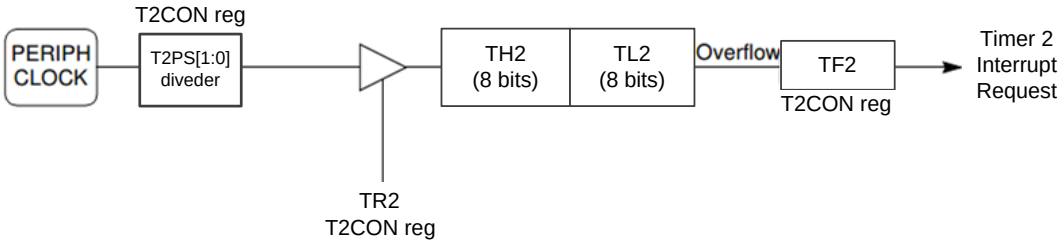


Figure 13.4.13 Timer2 Mode 1

13.4.14 Timer2 Mode 2

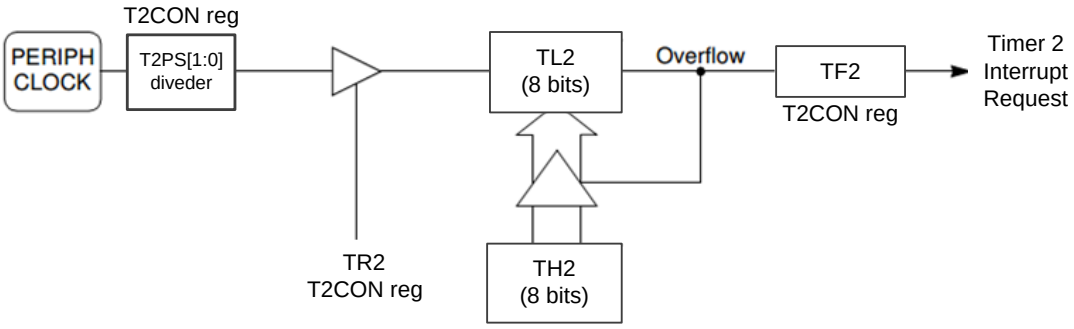


Figure 13.4.14 Timer2 Mode 2

13.4.15 Timer2 Mode 3

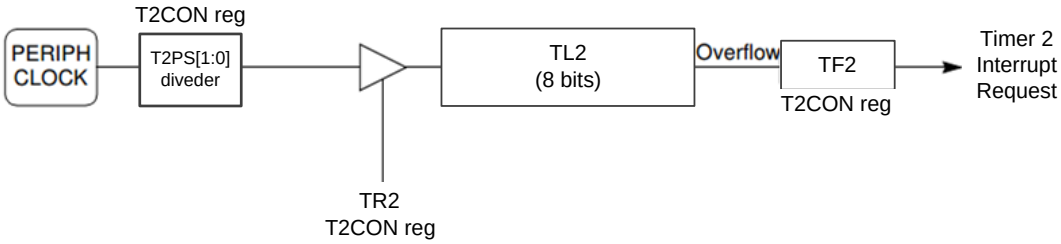


Figure 13.4.15 Timer2 Mode 3

13.5 Watchdog Timer

The Watchdog Timer (**WDT**) is a8-bit free-running counter that generates a reset signal or interrupt (**WDTC**.6) if it over flows. It can help the application software to recover from an abnormal condition. The **WDT** is independent from **Timer0**, **Timer1**, or **Timer2**. The **F_WDT** is 375KHz, it is from on-chip RC oscillator.

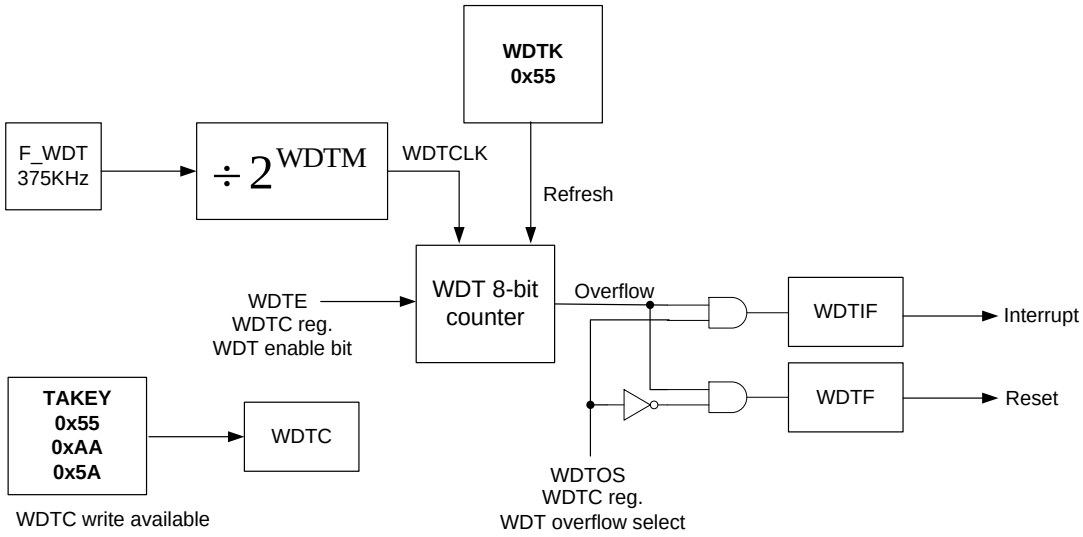


Figure 13.5 Watchdog Timer

$$WDTCLK = F\_WDT \times \frac{1}{2^{WDTM}}$$

WDT (8-bit counter) overflow time = 256/WDTCLK

Table 13.5 Watchdog Related SFR

SFR	Description	address	Reset value
RSTS	Reset Source Register	FEH	0AH
TAKEY	Time Access Key Register	FFH	00H
WDTC	Watchdog Timer Control Register	B6H	04H
WDTK	Watchdog Timer Refresh Key	B7H	00H

RSTS				Address = FEH		Reset Value = 00001010B	
Reset Source Register							
	-----	-----	-----	WDTRF	PINRF[1:0]		PORF[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R/W	R/W	R/W	R/W	R/W

WDTRF	Watchdog timer reset flag. This flag is set to 1 if the Watchdog Timer Reset caused the reset.
PINRF[1:0]	RSTN pin reset flag. This flag is set to 10b if the RSTN pin caused the reset. Clear by firmware.
PORF[1:0]	POR reset flag. This flag is set to 10b if the POR caused the reset. Clear by firmware.

13.5.1 WDTC (Watchdog Timer Control Register)

Table 13.5.1 WDTC (Watchdog Timer Control Register)

WDTC				Address = B6H		Reset Value = 00000100B	
Watchdog Timer Control Register							
	-----	WDTOS	WDTE	-----	WDTM[3:0]			
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	X	R/W	R/W	R/W	R/W

WDTOS	Watchdog timer overflow select : 0 : When WDT overflow, enable WDT reset. 1 : When WDT overflow, enable WDT interrupt.
WDTE	Watchdog timer enable : 0 : Disable WDT. 1 : Enable WDT.
WDTM[3:0]	WDT clock divider : WDTCLK = $375KHz \times \frac{1}{2^{WDTM}}$ (default is 375KHz / 16)

13.5.2 TAKEY (Time Access Key Register)

Table 13.5.2 TAKEY (Time Access Key Register)

TAKEY				Address = FFH			Reset Value = 00000000B	
Time Access Key Register								
	TAKEY[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WDTC default is read only, must write three specific values 55H, AAH and 5AH to the TAKEY enable the WDTC write available.
The sequence is:
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah								

13.5.3 WDTK (Watchdog Timer Refresh Key)

Table 13.5.3 WDTK (Watchdog Timer Refresh Key)

WDTK				Address = B7H			Reset Value = 00000000B	
Watchdog Timer Refresh Key								
	WDTK[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
The application must write 0x55 into the WDTK register, for the Watchdog timer to be cleared.								

For example, enable the watchdog with a time-out reset period of 5.461ms.

Following write sequence:

MOV TAKEY, #55h

MOV TAKEY, #AAh

MOV TAKEY, #5Ah ; WDTC write is available.

MOV WDTC, #23h ; WDTM [3:0] = 0011b. WDTE =1 to enable the WDT.

MOV WDTK, #55h ;Refresh WDT.

13.6 Serial Port (UART)

The Serial Port provides a flexible full-duplex synchronous/asynchronous receiver/transmitter, called **UART**. The communication rate can be set by configuring the baud rate in **SFRs**. The two serial buffers consist of two separate registers, a transmit buffer and a receive buffer. Writing data to the SFR **SBUF**, transfers the data to the serial output buffer and starts the transmission. Reading from the **SBUF**, reads data from the serial receive buffer. The serial port can simultaneously transmit and receive data. It can also buffer 1 byte at receive, which prevents the receive data from being lost if the CPU reads the second byte before the transmission of the first byte is completed.

Table 13.6 Serial Port (UART) Related SFR

SFR	Description	address	Reset value
AUX	Auxiliary	8EH	11H
PFCON	Peripheral Frequency Control Register	D1H	00H
SCON	Serial Port Control Register	98H	00H
SBUF	Serial Port Data Buffer	99H	00H
SRELH	Serial Port Reload Register High	9BH	00H
SRELL	Serial Port Reload Register Low	9AH	00H

AUX Address = 8EH Reset Value = 00010001B

Auxiliary Register

	LVD_EN	LVD	-----	ITS	SMOD	BRS	DPS	CP
Bit	7	6	5	4	3	2	1	0
Type	R/W	R	X	R/W	R/W	R/W	R/W	R

LVD_EN	Low voltage detect enable : 1: Enable
LVD	Low voltage detect status. : 1: Low voltage occur
ITS	MCU instruction timing select. : 0:1T 1:2T
SMOD	Serial Port (UART) baud rate select.
BRS	Serial Port (UART) baud rate generator select.
DPS	Data pointer register select : 0 : Select DPTR Register DP0H, DP0L 1 : Select DPTR Register DP1H, DP1L
CP	Code protect : 0 : Non-protect 1: Protect

PFCON Address = D1H Reset Value = 00000000B

Peripheral Frequency Control Register

	-----	-----	SRELPS[1:0]		T1PS[1:0]		T0PS[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

SRELPS[1:0] Serial port (UART) Prescaler select :

00 :F_PER/64

01 :F_PER/32

10 :F_PER/16

11 :F_PER/8

T1PS[1:0] Timer1(T1) Prescaler select :

00 :F_PER/12

01 :F_PER

10 :F_PER/96

11 :-----

T0PS[1:0] Timer0(T0) Prescaler select :

00 : F_PER/12

01 : F_PER

10 : F_PER/96

11 :-----

13.6.1 SCON (Serial Port Control Register)

The **SCON** register controls the function of Serial Port (**UART**).

Table 13.6.1 SCON (Serial Port Control Register)

SCON Address = 98H Reset Value = 00000000B

Serial Port Control Register

	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SM0	SM1	Mode	Description	Baud Rate	
0	0	Mode 0	Shift register	F_PER/12	
0	1	Mode 1	8bit UART	Variable	
1	0	Mode 2	9bit UART	Depends on SMOD (AUX.3)	
				SMOD	Baud Rate
				0	F_PER/64
				1	F_PER/32
1	1	Mode 3	9bit UART	Variable	

SM2	Multiprocessor communication enable
REN	Serial reception enable : 0 : Serial reception at Serial Port is disabled. 1 :Serial reception at Serial Port is enabled.
TB8	Transmitter bit 8 : This bit is used while transmitting data through Serial Port in Modes 2 and 3. The state of this bit corresponds with the state of the 9th transmitted bit (e.g. parity check or multiprocessor communication). It is controlled by software.
RB8	Received bit 8 : This bit is used while receiving data through Serial Port 0 in Modes 2 and 3. It reflects the state of the 9th received bit. In Mode 1, if multiprocessor communication is enabled (sm2 = 0), this bit is the stop bit that was received. In Mode 0 this bit is not used.
TI	Transmit interrupt flag : (completion of a serial transmission) It is set by hardware at the end of bit 8 in mode 0 or at the beginning of a stop bit in other modes. It must be cleared by software.
RI	Receive interrupt flag : (It must be cleared by software.) It is set by hardware after completion of a serial reception at Serial Port 0. It is set by hardware at the end of bit 8 in mode 0 or in the middle of a stop bit in other modes.

Serial Port working in modes 1 or mode 3:

When BRS = 0 (AUX.2)

TIPS[1:0] = 00b

$$\text{baud rate} = \frac{2^{SMOD}}{32\times(256-TH1)} \times \frac{F\_PER}{12}$$

TIPS[1:0] = 01b

$$\text{baud rate} = \frac{2^{SMOD}}{32\times(256-TH1)} \times F\_PER$$

TIPS[1:0] = 10b

$$\text{baud rate} = \frac{2^{SMOD}}{32\times(256-TH1)} \times \frac{F\_PER}{96}$$

When BRS = 1 (AUX.2)

SRELPS[1:0] = 00b

$$\text{baud rate} = \frac{2^{SMOD}}{2^{10}-SREL[H,L]} \times \frac{F\_PER}{64}$$

SRELPS [1:0] = 01b

$$\text{baud rate} = \frac{2^{SMOD}}{2^{10}-SREL[H,L]} \times \frac{F\_PER}{32}$$

SRELPS [1:0] = 10b

$$\text{baud rate} = \frac{2^{SMOD}}{2^{10}-SREL[H,L]} \times \frac{F\_PER}{16}$$

SRELPS [1:0] = 11b

$$\text{baud rate} = \frac{2^{SMOD}}{2^{10}-SREL[H,L]} \times \frac{F\_PER}{8}$$

13.6.2 SBUF (Serial Port Data Buffer)

Writing data to this register sets data in serial output buffer and starts the transmission through Serial Port. Reading from the **SBUF**, reads data from the serial receive buffer.

Table 13.6.2 SBUF (Serial Port Data Buffer)

SBUF	Address = 99H				Reset Value = 00000000B			
Serial Port Data Buffer								
	SBUF[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.6.3 SREL (Serial Port Reload Register)

Serial Port Reload Register is used for Serial Port baud rate generation. Only 10 bits are used, where 8 bits from the **SRELL** as lower bits and 2 bits from the **SRELH** (SRELH.1, SRELH.0) as higher bits.

Table 13.6.3 SREL (Serial Port Reload Register)

SRELH	Address = 9BH					Reset Value = 00000000B		
Serial Port Reload Register High								
	-----	-----	-----	-----	-----	-----	SREL.9	SREL.8
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	X	R/W	R/W

SRELL	Address = 9AH					Reset Value = 00000000B		
Serial Port Reload Register Low								
	SREL[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.7 Power Management

The Power Control Register (**PCON**) is used to control the **CGH001A STOP** and **IDLE** power management modes.

Table 13.7 Power Management

PCON			Address = 87H			Reset Value = 00000000B	
Power Control Register							
-----	-----	-----	-----	-----	-----	STOP	IDLE
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	X	R/W	R/W

STOP	Stop mode bit. Setting this bit activates STOP operation. (read as 0)
IDLE	Idle mode bit. Setting this bit activates IDLE mode operation. (read as 0)

13.7.1 STOP MODE

Setting the **STOP** Mode Select bit (**PCON**.1) causes the controller core to enter **STOP** mode as soon as the instruction that sets the bit completes execution. In **STOP** mode the CPU, GPIO, UART, and Timers are stopped, but the ADC, MDE, and WDT is still work.

STOP mode can terminate by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

The assertion of an enabled interrupt will cause the **STOP** Mode Selection bit (**PCON**.1) to be cleared and the CPU to resume operation.

13.7.2 IDLE MODE

Setting the **IDLE** Mode Select bit (**PCON**.0) causes the hardware to halt the CPU and enter **IDLE** mode as soon as the instruction that sets the bit completes execution.

In **IDLE** mode only the CPU is stop. All internal registers and memory maintain their original data.

IDLE mode can terminate by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

The assertion of an enabled interrupt will cause the **IDLE** Mode Selection bit (**PCON**.0) to be cleared and the CPU to resume operation.

13.8 Reset

The reset logic is used to place the device into a known state.

CGH001A provides Power-on Reset flag, External Reset **RSTN** flag and Watchdog timer Reset flag to monitor reset status. The source of the reset can be monitor.

13.8.1 RSTS (Reset Source Register)

Table 13.8.1 Reset

RSTS Address = FEH Reset Value = 00001010B

Reset Source Register

	-----	-----	-----	WDTRF	PINRF[1:0]		PORF[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R/W	R/W	R/W	R/W	R/W

WDTRF	Watchdog timer reset flag. This flag is set to 1 if the Watchdog Timer Reset caused the reset.
PINRF[1:0]	**RSTN** pin reset flag. This flag is set to 10b if the **RSTN** pin caused the reset. Clear by firmware.
PORF[1:0]	POR reset flag. This flag is set to 10b if the POR caused the reset. Clear by firmware.

13.9 Interrupt Controller

The **ISR** - Interrupt Service Routine unit, is a subcomponent responsible for interrupt handling. It receives up to **14**interrupt requests. Each interrupt source has its own request flag that is located in devices which is a source of interrupt. No interrupt request flags are located directly in **ISR**. All interrupts are requested by high level on correspondent inputs to **ISR**. Each of the interrupt sources can be individually enabled or disabled by corresponding enable flag in **IEN0**, **IEN1**SFR registers. Additionally all interrupts can be globally enabled or disabled by the —**EA** flag in the **IEN0** SFR. All interrupt sources are divided into 6 interrupts groups. Each of the interrupt groups can have one of four interrupt priority levels assigned. The interrupt priority level is defined by flags located in the **IP0** and **IP1** SFR registers.

Table 13.9.1 Interrupt vectors

Interrupt Number (use Keil C Tool)	**Interrupt Vector Address**	**Interrupt Request Flags**
0	0003H	IE0 – External interrupt 0
1	000BH	TF0 – Timer0 interrupt
2	0013H	IE1 – External interrupt 1
3	001BH	TF1 – Timer1 interrupt
4	0023H	SPIF(TI, RI)– Serial port interrupt
5	002BH	TF2 – Timer2 interrupt
6	0033H	-----
7	003BH	CAPIF – Capture interrupt
8	0043H	OCPSIF – OCP Short interrupt
9	004BH	HALLIF – HALL interrupt
10	0053H	MPWMMINIF–MPWM MIN interrupt
11	005BH	MPWMMAXIF–MPWM MAX interrupt
12	0063H	GPWMMAXIF – GPWM MAX interrupt
13	006BH	-----
14	0073H	WDTIF – Watchdog timer interrupt
15	007BH	OCPLIF – OCP Limit interrupt

Table13.9.2 Interrupt vectors

Group priority	**Interrupt Group**	**Highest priority in group**		**Lowest priority in group**
Highest	Group0	-----	IE0	-----
	Group1	WDTIF	TF0	-----
	Group2	OCPSIF	HALLIF	IE1
	Group3	MPWMMINIF	MPWMMAXIF	TF1
	Group4	GPWMMAXIF	SPIF(TI, RI)	-----
Lowest	Group5	OCPLIF	TF2	CAPIF

Table 13.9.3 Interrupt Related SFR

SFR	Description	address	Reset value
IEN0	Interrupt Enable Register 0	A8H	00H
IEN1	Interrupt Enable Register 1	B8H	00H
IRCON1	Interrupt Request Register 1	C0H	00H
IP0	Interrupt Priority Register 0	A9H	00H
IP1	Interrupt Priority Register 1	B9H	00H

13.9.1 IEN0 (Interrupt Enable Register 0)

Table 13.9.1.1 IEN0 (Interrupt Enable Register 0)

IEN0				Address = A8H		Reset Value = 00000000B		
Interrupt Enable Register 0								
	EA	-----	ET2	ESP	ET1	EX1	ET0	EX0
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	R/W	R/W	R/W	R/W	R/W	R/W

EA	Interrupts enable : 0: Disable all interrupts. 1: Enable interrupt.
ET2	Timer2 interrupt enable: 0: Disable Timer2 overflow interrupt. 1: When EA = 1, enable Timer2 overflow interrupt.
ESP	Serial port interrupt enable: 0: Disable Serial port interrupt. 1: When EA = 1, enable Serial port interrupt.
ET1	Timer1 interrupt enable: 0: Disable Timer1 overflow interrupt. 1: When EA = 1, enable Timer1 overflow interrupt.
EX1	External interrupt 1 enable: 0: Disable External interrupt 1. 1: When EA = 1, enable External interrupt 1.
ET0	Timer0 interrupt enable: 0: Disable Timer0 overflow interrupt. 1: When EA = 1, enable Timer0 overflow interrupt.
EX0	External interrupt 0 enable: 0: Disable External interrupt 0. 1: When EA = 1, enable External interrupt 0.

13.9.2 IEN1 (Interrupt Enable Register 1)

Table 13.9.2.1 IEN1 (Interrupt Enable Register 1)

IEN1 Address = B8H Reset Value = 00000000B

Interrupt Enable Register 1

	OCPLIE	WDTIE	-----	GPWMIE	MPWMMAXIE	MPWMMINIE	HALLIE	OCPSIE
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	-----	R/W	R/W	R/W	R/W	R/W

OCPLIE	OCP (Over current protect) Limit interrupt enable: 0: Disable OCP Limit interrupt. 1: When EA = 1, enable OCP Limit interrupt.
WDTIE	Watchdog timer interrupts enable : 0: Disable WDT interrupt. 1: When EA = 1 and WDTOS = 1, enable WDT overflow interrupt.
GPWMIE	GPWM interrupt enable: 0: Disable GPWM interrupt. 1: When EA = 1, enable GPWM interrupt.
MPWMMAXIE	MPWM maximum interrupt enable: 0: Disable MPWM maximum interrupt. 1: When EA = 1, enable MPWM maximum interrupt.
MPWMMINIE	MPWM minimum interrupt enable: 0: Disable MPWM minimum interrupt. 1: When EA = 1, enable MPWM minimum interrupt.
HALLIE	HALL interrupt enable: 0: Disable HALL interrupt. 1: When EA = 1, enable HALL interrupt.
OCPSIE	OCP (Over current protect) Short interrupt enable: 0: Disable OCP Short interrupt. 1: When EA = 1, enable OCP Short interrupt.

13.9.3 IRCON1 (Interrupt Request Register 1)

Table 13.9.3.1 IRCON1 (Interrupt Request Register 1)

IRCON1				Address = C0H		Reset Value = 00000000B		
Interrupt Request Register 1								
	OCPLIF	WDTIF	-----	GPWMIF	MPWMMAXIF	MPWMMINIF	HALLIF	OCPSIF
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	----	R/W	R/W	R/W	R/W	R/W

OCPLIF	OCP Limit interrupt flag.
WDTIF	Watchdog timer interrupts flag.
GPWMIF	GPWM interrupt flag.
MPWMMAXIF	MPWM maximum interrupt flag.
MPWMMINIF	MPWM minimum interrupt flag.
HALLIF	HALL interrupt flag.
OCPSIF	OCP Short interrupt flag.

13.9.4 IP (Interrupt Priority Register)

The 14interrupt sources are grouped into 6 priority groups. For each of the groups, one of four priority levels can be selected. It is achieved by setting appropriate values in **IP0** and **IP1** registers. The contents of the Interrupt Priority Registers define the priority levels for each interrupt source according to the tables below.

Table 13.9.4.1 IP (Interrupt Priority Register)

IP0				Address = A9H			Reset Value = 00000000B	
Interrupt Priority Register 0								
	-----	-----	G5IP0	G4IP0	G3IP0	G2IP0	G1IP0	G0IP0
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

G5IP0	Group5 interrupt priority bit 0
G4IP0	Group4 interrupt priority bit 0
G3IP0	Group3 interrupt priority bit 0
G2IP0	Group2 interrupt priority bit 0
G1IP0	Group1 interrupt priority bit 0
G0IP0	Group0 interrupt priority bit 0

IP1 Address = B9H Reset Value = 00000000B

Interrupt Priority Register 1

Bit	7	6	5	4	3	2	1	0
	-----	-----	G5IP1	G4IP1	G3IP1	G2IP1	G1IP1	G0IP1
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

G5IP1	Group5 interrupt priority bit 1
G4IP1	Group4 interrupt priority bit 1
G3IP1	Group3 interrupt priority bit 1
G2IP1	Group2 interrupt priority bit 1
G1IP1	Group1 interrupt priority bit 1
G0IP1	Group0 interrupt priority bit 1

Table 13.9.4.2 Priority Level

Level	**Priority**	**GxIP1**	**GxIP0**
Level 0	Lowest	0	0
Level 1		0	1
Level 2		1	0
Level 3	Highest	1	1

14. 10-bit Analog-to-Digital Converter (ADC)

The **CGH001A** provides eight channels 10-bit ADC. The result of the conversion is provided at **ADCD** [9:0].

Table 14.1 10 bit Analog-to-Digital Converter (ADC)

SFR	Description	address	Reset value
ADCCONT	ADC Control Register	D2H	80H
ADCSTR	ADC Start Convert and Setting Register	D3H	00H
ADCD1	ADC Data Register 1	D5H	00H
ADCD2	ADC Data Register 2	D6H	00H

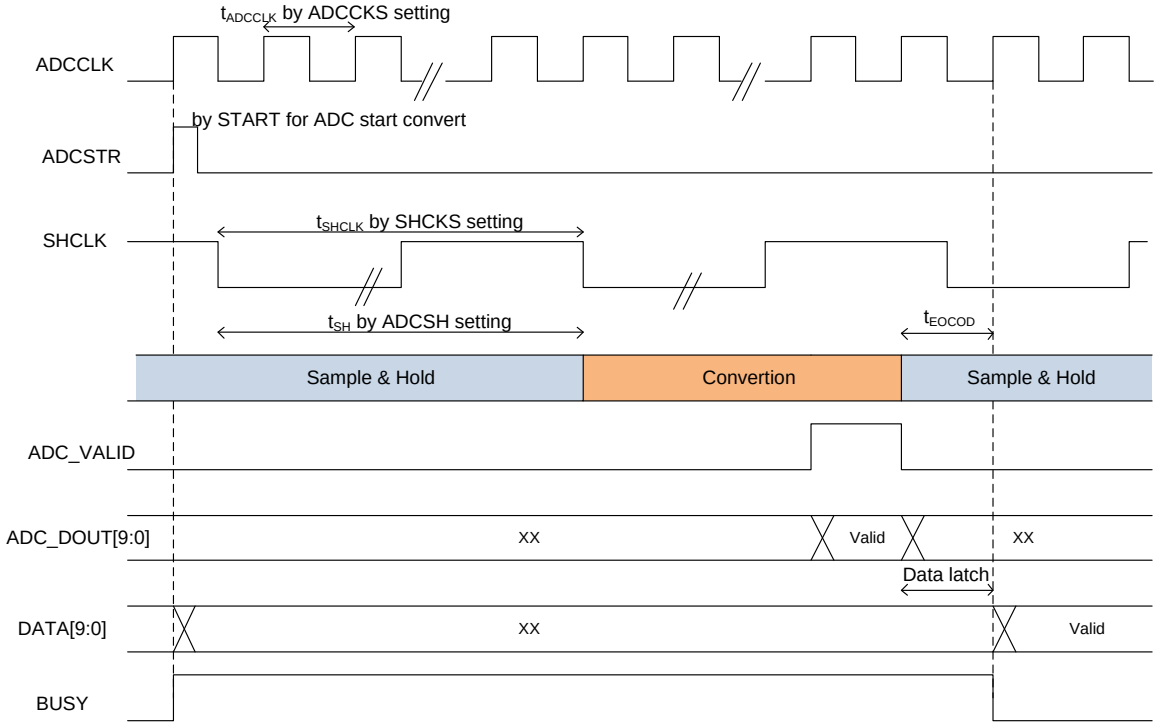


Figure14.1 ADC conversion timing

14.1 ADCCONT (ADC Control Register)

Table 14.1.1 ADCCONT (ADC Control Register)

ADCCONT Address = D2H Reset Value = 1000000B

ADC Control Register

Bit	7	6	5	4	3	2	1	0
	ADCPD	ADCSH[1:0]		ADCDS	ADCCKS	ADDCH[2:0]		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ADCPD ADC power down control register :

0 : Normal

1 : Power down

ADCSH[1:0] ADC sample and hold time : (base on SHCLK)

00 : 1 clock

01 : 2 clock

10 : 3 clock

11 : 4 clock

ADCDS ADC data select :

	MSB	10 bit result		LSB
0 :	ADCD2[7:0]		ADCD1.1	ADCD1.0
1 :	ADCD1.1	ADCD1.0	ADCD2[7:0]	

ADCCKS ADC conversion clock select : (ADCCLK)

0 : 4MHz

1 : 2MHz

ADCCH[2:0] ADC conversion channel select :

000:CH0	100:CH4
001: Reserve	101: Reserve
010:CH2	110:CH6
011 : Reserve	111 :Reserve

14.2 ADCSTR (ADC Start Convert and Setting Register)

Table 14.2.1 ADCCONT (ADC Control Register)

ADCSTR			Address = D3H		Reset Value = 0000000B		
ADC Start Convert and Setting Register							
	SHCKS[1:0]	-----	BUSY	-----	-----	-----	START
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	X	R	X	X	X	W

SHCKS[1:0]	ADC sample and hold clock select : (SHCLK) 00 : 1MHz 01 : 500KHz 10 : 400KHz 11 : 333KHz
BUSY	ADC conversion busy flag : 0 : ADC conversion finish 1 : ADC conversion busy
START	ADC start conversion register : (write 1 only) 1 : ADC start conversion

14.3 ADCD1 (ADC Data Register 1)

Table 14.3.1 ADCD1 (ADC Data Register 1)

ADCD1			Address = D5H			Reset Value = 00000000B	
ADC Data Register 1							
	-----	-----	-----	-----	-----	-----	ADCD1.1	ADCD1.0
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

14.4 ADCD2 (ADC Data Register 2)

Table 14.4.1 ADCD2 (ADC Data Register 2)

ADCD2			Address = D6H			Reset Value = 00000000B	
ADC Data Register 2							
	ADCD2[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

15. General PWM (GPWM)

CGH001A have one16-bit general PWM output (**PINSET6**.4 = ‘1’) and six 11-bit PWM (compensation with Dead-Time) for Motor Controller.

GPWM is count up and down timer.(fixed)

Table 15.1 General PWM (GPWM)

SFR	Description	address	Reset value
GPWMCONT	General PWM Control Register	BAH	00H
GPWMMAXH	General PWM Max Register High	BCH	00H
GPWMMAXL	General PWM Max Register Low	BBH	02H
GPWMDYH	General PWM Duty Register High	BEH	FFH
GPWMDYL	General PWM Duty Register Low	BDH	FFH

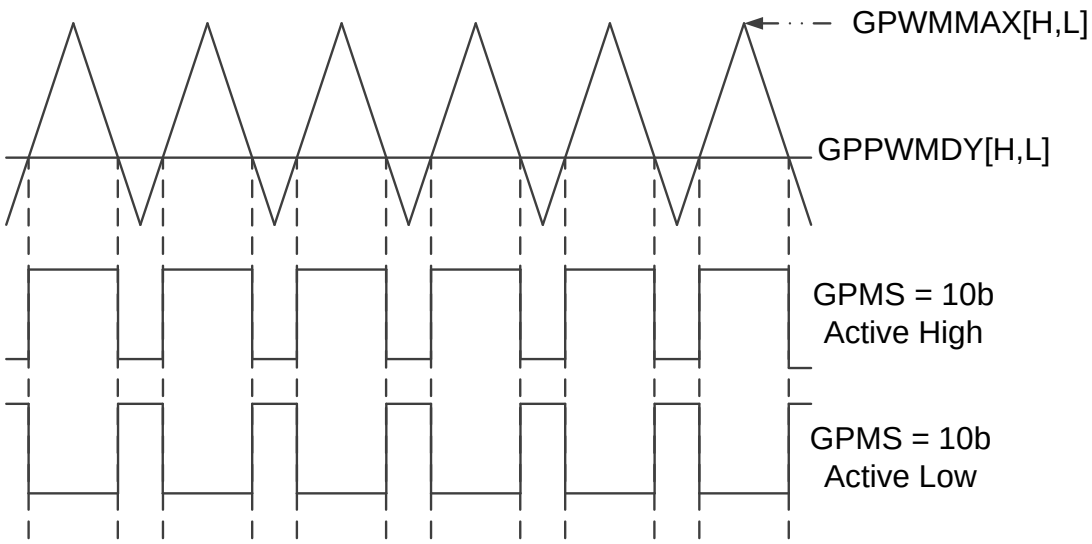


Figure 15.1 General PWM (GPWM)

15.1 GPWMCONT (General PWM Control Register)

Table 15.1.1 GPWMCONT (General PWM Control Register)

GPWMCONT Address = BAH Reset Value = 00000000B

General PWM Control Register

	GPWMTR	GPMS[1:0]		-----	-----	-----	GPCKS[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	X	X	X	R/W	R/W

GPWMTR	GPWM timer run control : 0 : Stop 1: Run
GPMS[1:0] (SYNC)	GPWM output mode select 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low
GPCKS[1:0] (SYNC)	GPWM clock select : 00 : 48MHz 01 : 48MHz/2 10 : 48MHz/4 11 : 48MHz/8

15.2 GPWMMAX (General PWM Max Register)

Table 15.2.1 GPWMMAX (General PWM Max Register)

GPWMMAXH (SYNC) Address = BCH Reset Value = 00000000B

General PWM Max Register High

	GPWMMAXH[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

GPWMMAXL (SYNC) Address = BBH Reset Value = 00000010B

General PWM Max Register Low

	GPWMMAXL[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.3 GPWMDY (General PWM Duty Register)

Table 15.3.1 GPWMDY (General PWM Duty Register)

GPWMDYH (SYNC)	Address = BEH				Reset Value = 11111111B			
General PWM Duty Register High								
	GPWMDYH[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

GPWMDYL (SYNC)	Address = BDH				Reset Value = 11111111B			
General PWM Duty Register Low								
	GPWMDYL[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16. Capture

Table 16.1 Capture

SFR	Description	address	Reset value
CAPCONT	Capture Control Register	D8H	03H
CAPH_H	Capture High-level Count High	CBH	00H
CAPH_L	Capture High-level Count Low	CCH	00H
CAPT_H	Capture Total Count High	C9H	00H
CAPT_L	Capture Total Count Low	CAH	00H

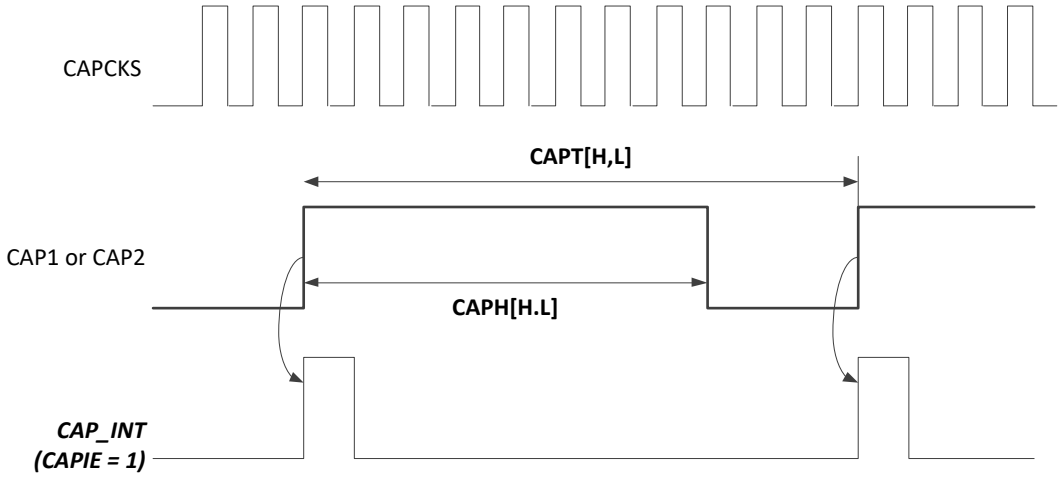


Figure 16.1 Capture

16.1 CAPCONT (Capture Control Register)

Table 16.1.1 CAPCONT (Capture Control Register)

CAPCONT Address = D8H Reset Value = 00000011B

Capture Control Register

	CAPIF	CAPIE	-----	CAPPINSEL	-----	CAPCKS[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	R	W	X	R/W	X	R/W	R/W	R/W

CAPIF	Capture Interrupt flag
CAPIE	Capture Interrupt enable
CAPPINSEL	Capture input pin select : 0: CAP2(PIN **CH7**) 1: CAP1(PIN**CH0**)
CAPCKS[2:0]	Capture clock select : 000 : 48MHz/4 100 : 48MHz/64 001 : 48MHz/8 101 : 48MHz/128 010 : 48MHz/16 110 : 48MHz/256 011 : 48MHz/32 111 : 48MHz/512

16.2 CAPT (Capture Total Count)

Table 16.2.1 CAPT (Capture Total Count)

CAPT_H	Address = C9H				Reset Value = 00000000B		
Capture Total Count High							
	CAPT[15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

CAPT_L	Address = CAH				Reset Value = 00000000B		
Capture Total Count Low							
	CAPT[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

16.3 CAPH (Capture High-level Count)

Table 16.3.1 CAPH (Capture High-level Count)

CAPH_H	Address = CBH				Reset Value = 00000000B		
Capture High-level Count High							
	CAPH[15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

CAPH_L	Address = CCH				Reset Value = 00000000B		
Capture High-level Count Low							
	CAPH[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

17. Addition and Subtraction Unit (ASU)

ASU provides 32-bit Addition and Subtraction calculation.

Table 17.1 Addition and Subtraction Unit (ASU)

SFR	Description	address	Reset value
AS_MD_CONT	ASU and MDU Control Register	E1H	10H
ASUD1_1	ASU Data 1 byte 1	E8H	00H
ASUD1_2	ASU Data 1 byte 2	E9H	00H
ASUD1_3	ASU Data 1 byte 3	EAH	00H
ASUD1_4	ASU Data 1 byte 4	EBH	00H
ASUD2_1	ASU Data 2 byte 1	ECH	00H
ASUD2_2	ASU Data 2 byte 2	EDH	00H
ASUD2_3	ASU Data 2 byte 3	EEH	00H
ASUD2_4	ASU Data 2 byte 4	EFH	00H
ASUR1	ASU Result Register 1	DCH	00H
ASUR2	ASU Result Register 2	DDH	00H
ASUR3	ASU Result Register 3	DEH	00H
ASUR4	ASU Result Register 4	DFH	00H

	MSB			LSB
ASUD1	ASUD1_4	ASUD1_3	ASUD1_2	ASUD1_1
ASUD2	ASUD2_4	ASUD2_3	ASUD2_2	ASUD2_1
ASUR	ASUR4	ASUR3	ASUR2	ASUR1

Addition Calculation (AS_MD_CONT.0 = 0)	ASUR = ASUD1 + ASUD2	ASUR4 limit at 0x7F
Subtraction Calculation (AS_MD_CONT.0 = 1)	ASUR = ASUD1 – ASUD2	ASUR4 limit at 0x81

17.1 AS_MD_CONT (ASU and MDU Control Register)

Table 17.1.1 AS_MD_CONT (ASU and MDU Control Register)

AS_MD_CONT Address = E1H Reset Value = 00010000B

ASU and MDU Control Register

	-----	-----	-----	MDUF	-----	-----	MDUS	ASUS
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R	X	X	R/W	R/W

MDUF	MDU finish flag : 0 : MDU busy. 1 : MDU calculation finished.
MDUS	MDU Signed select : 0 :Signed calculation. 1 :Unsigned calculation.
ASUS	ASU Subtraction select : 0 : Addition calculation. 1: Subtraction calculation.

17.2 ASUD1 (ASU Data 1)

Table 17.2.1 ASUD1 (ASU Data 1)

ASUD1_1 Address = E8H Reset Value = 00000000B

	ASUD1_1[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUD1_2 Address = E9H Reset Value = 00000000B

	ASUD1_2[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUD1_3 Address = EAH Reset Value = 00000000B

	ASUD1_3[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUD1_4 Address = EBH Reset Value = 00000000B

	ASUD1_4[7:0]

	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.3 ASUD2 (ASU Data 2)

Table 17.3.1 ASUD2 (ASU Data 2)

ASUD2_1	Address = ECH				Reset Value = 00000000B			
	ASUD2_1[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUD2_2	Address = EDH				Reset Value = 00000000B			
	ASUD2_2[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUD2_3	Address = EEH				Reset Value = 00000000B			
	ASUD2_3[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUD2_4	Address = EFH				Reset Value = 00000000B			
	ASUD2_4[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.4 ASUR (ASU Result Register)

Table 17.4.1 ASUR (ASU Result Register)

ASUR1	Address = ECH						Reset Value = 00000000B	
	ASUR1[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUR2	Address = EDH						Reset Value = 00000000B	
	ASUR2[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUR3	Address = EEH						Reset Value = 00000000B	
	ASUR3[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUR4	Address = EFH						Reset Value = 00000000B	
	ASUR4[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

18. Multiplication and Division Unit (MDU)

The **MDU** is an on-chip arithmetic co-processor which enables the **CGH001A** to perform additional extended arithmetic operations. All operations are singed/unsigned integer operations. Operands and results are stored in **MD0**–**MD5** registers. The module is controlled by the **AS_MD_CONT** and **MD_CONT** register. Any calculation of the **MDU** overwrites its operands. The **MDU** support five operations: Division 32-bit/16-bit, Division 16-bit/16-bit, Multiplication, Shift and Normalize.

Table 18.1 Multiplication and Division Unit (MDU)

SFR	Description	address	Reset value
AS_MD_CONT	ASU and MDU Control Register	E1H	10H
MD_CONT	MDU Control Register	DBH	00H
MD0	Multiplication Division Register 0	E2H	00H
MD1	Multiplication Division Register 1	E3H	00H
MD2	Multiplication Division Register 2	E4H	00H
MD3	Multiplication Division Register 3	E5H	00H
MD4	Multiplication Division Register 4	E6H	00H
MD5	Multiplication Division Register 5	E7H	00H

18.1 AS_MD_CONT (ASU and MDU Control Register)

Table 18.1.1 AS_MD_CONT (ASU and MDU Control Register)

AS_MD_CONT Address = E1H Reset Value = 00010000B

ASU and MDU Control Register

	-----	-----	-----	MDUF	-----	-----	MDUS	ASUS
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R	X	X	R/W	R/W

MDUF	MDU finish flag : 0 : MDU busy. 1 : MDU calculation finished.
MDUS	MDU Signed select : 0 :Signed calculation. 1 :Unsigned calculation.
ASUS	ASU Subtraction select : 0 : Addition calculation. 1: Subtraction calculation.

18.2 MD_CONT (MDU Control Register)

Table 18.2.1 MD_CONT (MDU Control Register)

MD_CONT			Address = DBH		Reset Value = 00010000B			
MDU Control Register								
	MDEF	MDOV	SLR	SC[4:0]				
Bit	7	6	5	4	3	2	1	0
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W

MDEF	MDU Error flag : Indicates an improperly performed operation (when one of the arithmetic operations has been restarted or interrupted by a new operation).
MDOV	MDU Overflow flag : Overflow occurrence in the MDU operation.
SLR	Shift direction : 0 : shift left operation 1 : shift right operation
SC[4:0]	Shift counter : When set to all ‘0‘s, normalize operation is selected. After normalization, the SC[4:0] contain the number of normalizing shifts performed. When at least one of these bit is set high shift operation is selected. The number of shifts performed is determined by the number written to SC[4:0], where SC.4 is the MSB.

18.2.1 MDEF

The **MDEF** error flag indicates an improperly performed operation (when one of the arithmetic operations has been restarted or interrupted by a new operation). The error flag mechanism is automatically enabled with the first write operation to **MD0**and disabled with the final read instruction from **MD3** (multiplication or shift/norm) or **MD5** (division) in phase three.

The error flag is set when:

There is a write access to MDx registers (any of **MD0**-**MD5** and **MD_CONT**) during phase two of **MDU** operation (restart or calculations interrupting) There is a read access to one of MDx registers during phase two of **MDU** operation when the error flag mechanism is enabled. In such condition error flag is set but the calculation is not interrupted. The error flag is reset only after read access to **MD_CONT** register. The error flag is read only.

18.2.2 MDOV

The **MDOV** overflow flag is set when one of the following conditions occurs: Division by zero multiplication with a result greater than FFFFH

Start of normalizing if the (‘**MD3**.7’ =‘1’) most significant bit of **MD3** is set any operation of the **MDU** that does not match the above conditions clears the overflow flag. Note that the overflow flag is exclusively controlled by hardware. It cannot be written.

18.3 MD0 – MD5 (Multiplication Division Register)

Table 18.3.1 MD0 – MD5 (Multiplication Division Register)

MD0 Address = E2H Reset Value = 00000000B

Multiplication Division Register 0

	MD0[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD1 Address = E3H Reset Value = 00000000B

Multiplication Division Register 1

	MD1[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD2 Address = E4H Reset Value = 00000000B

Multiplication Division Register 2

	MD2[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD3 Address = E5H Reset Value = 00000000B

Multiplication Division Register 3

	MD3[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD4 Address = E6H Reset Value = 00000000B

Multiplication Division Register 4

	MD4[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD5 Address = E7H Reset Value = 00000000B

Multiplication Division Register 5

	MD5[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

18.4 MDU Operation Description

The operation of the **MDU** consists of three phases:

18.4.1 Loading the MDx registers

The type of calculation the **MDU** has to perform is selected by the order in which the MDx registers are written to. A write to **MD0** is the first transfer to be done in any case. Next writes must be done as shown in the table below to determine the **MDU** operation. The last write will start the selected operation.

Table 18.4.1 Loading the MDx registers

Operation	**32-bit/16-bit**	**16-bit/-16bit**	**16-bit x 16-bit**	**Shift/ normalizing**
First write	MD0 Dividend Low	MD0 Dividend Low	MD0 Multiplicand Low	MD0 LSB
	MD1 Dividend	MD1 Dividend High	MD4 Multiplicator Low	MD1
	MD2 Dividend		MD1 Multiplicand High	MD2
	MD3 Dividend High			MD3 MSB
	MD4 Divisor Low	MD4 Divisor Low		
Last write	MD5 Divisor High	MD5 Divisor High	MD5 Multiplicator High	MD_CONT start conversion

18.4.2 Executing calculation

During the calculation period, the **MDU** works in parallel to the CPU. When the calculation is complete, the hardware will set the **MDUF** bit to one (**MDUF** = '1'). The flag will be cleared at the next calculation.

The following table provides the execution time for each mathematical operation.

Table 18.4.2 Executing calculation

Operation	**Number of clock cycles**	
Division 32-bit/16-bit	17 clock cycles	
Division 16-bit/16-bit	9 clock cycles	
Multiplication	11 clock cycles	
Shift	Min 3 clock cycles (SC = 01H)	Max 18 clock cycles (SC = 1FH)
Normalize	Min 4 clock cycles (SC <= 01H)	Max 19 clock cycles (SC = 1FH)

18.4.3 Reading the result from the MDx registers

The Read-out sequence of the first "MDx" registers is not critical but the last read determines the end of a whole calculation.

Table 18.4.3 Reading the result from the MDx registers

Operation	**32-bit/16-bit**	**16-bit/16-bit**	**16-bit x 16-bit**	**Shift/ normalizing**
First read	MD0 Quotient Low	MD0 Quotient Low	MD0 Product Low	MD0 LSB
	MD1 Quotient	MD1 Quotient High	MD1 Product	MD1
	MD2 Quotient		MD2 Product	MD2
	MD3 Quotient High			
	MD4 Remainder Low	MD4 Remainder Low		
Last read	MD5 Remainder High	MD5 Remainder High	MD3 Product High	MD3 MSB

18.4.4 Shifting

In shift operation, 32-bit integer variable stored in **MD0** to **MD3**registers (the latter contains the most significant byte) is shifted left or right by a specified number of bits. The **SLR** bit (**MD_CONT**.5) defines the shift direction, and bits **SC**[4:0] (**MD_CONT**.4 –**MD_CONT**.0) specifies the shift count (which must not be 0). During shift operation, zeroes come into the left end of **MD3** for shifting right or right end of the **MD0** for shifting left.

18.4.5 Normalizing

All leading zeroes of 32-bit integer variable stored in **MD0** to **MD3** registers, the latter contains the most significant byte are removed by shift left operations. The whole operation is completed when the MSB (most significant bit) of **MD3** register contains a '1'. After normalizing, bits **SC**[4:0] (**MD_CONT**.4 –**MD_CONT**.0) contain the number of shift left operations, which were done.

19. Motor Driving Engine (MDE)

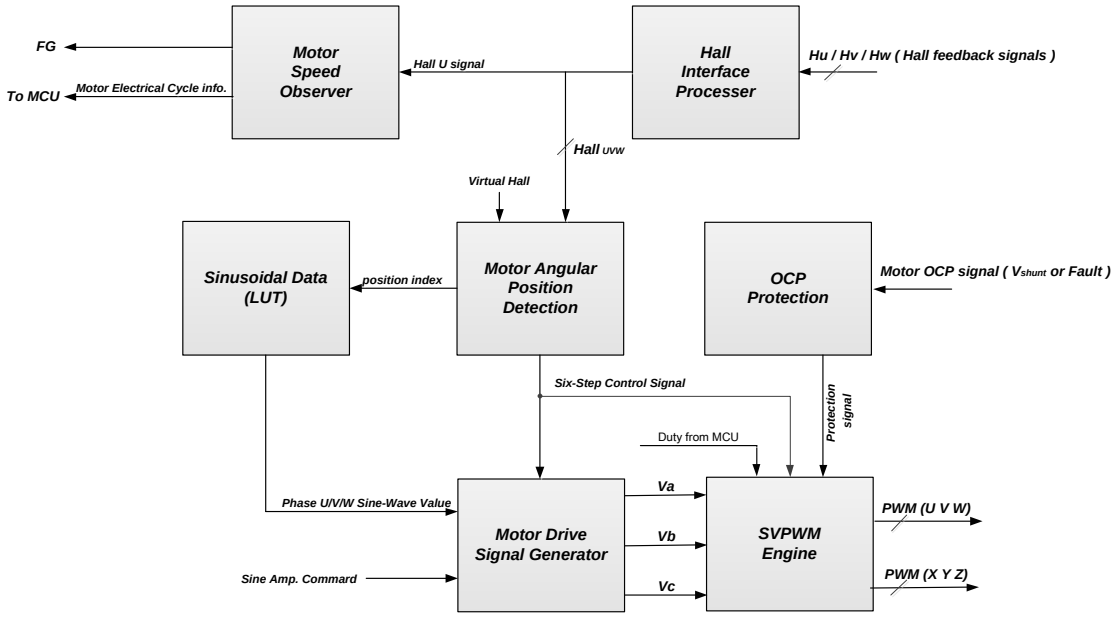


Figure 19.1 : MDE Architecture

CGH001A has built-in MDE (Motor Driving Engine), which provides motor sine-wave and square wave control drive architecture. The description is shown in Figure 19.1, which includes Hall Interface Processer, Motor Speed Observer, Motor Angular Position Detection, Sinusoidal Data (LUT), Motor Drive Signal Generator, SVPWM Engine and OCP Protection and other 7 control blocks.

First, the hall signals (Hu, Hv and Hw) fed back by the three-phase motor are processed by the de-bounce of the Hall Interface Processer Block and then output to the Motor Speed Oberver and Motor Angular Position Detection. The Motor Speed Oberver Block calculates the motor speed. , Motor Angular Position Detection estimates the position index of the three-phase sinusoidal wave and six-step control signal.

In sine-wave control drive, the position index of Motor Angular Position Detection Block of the three-phase sine wave is input to the Sinusoidal Data (LUT). After performing a table lookup of the three-phase sine wave, the three-phase sine wave value is output to the Motor Signal Generator Block to perform three-phase sine wave calculations (Va, Vb and Vc). In the square wave control drive, the Motor Angular Position Detection Block generates six-step control signal according to the hall status and outputs it to the Motor Signal Generator Block.
The last stage performs SVPWM modulation and outputs PWM_{UVW} and PWM_{XYZ} to the motor frequency conversion circuit.

OCP Protection Block, when an overcurrent occurs in the system, is protected by hardware and turns off six PWM signals. Detailed descriptions of the control functions of each block are detailed in the following chapters.

19.1 HALL Interface Processer

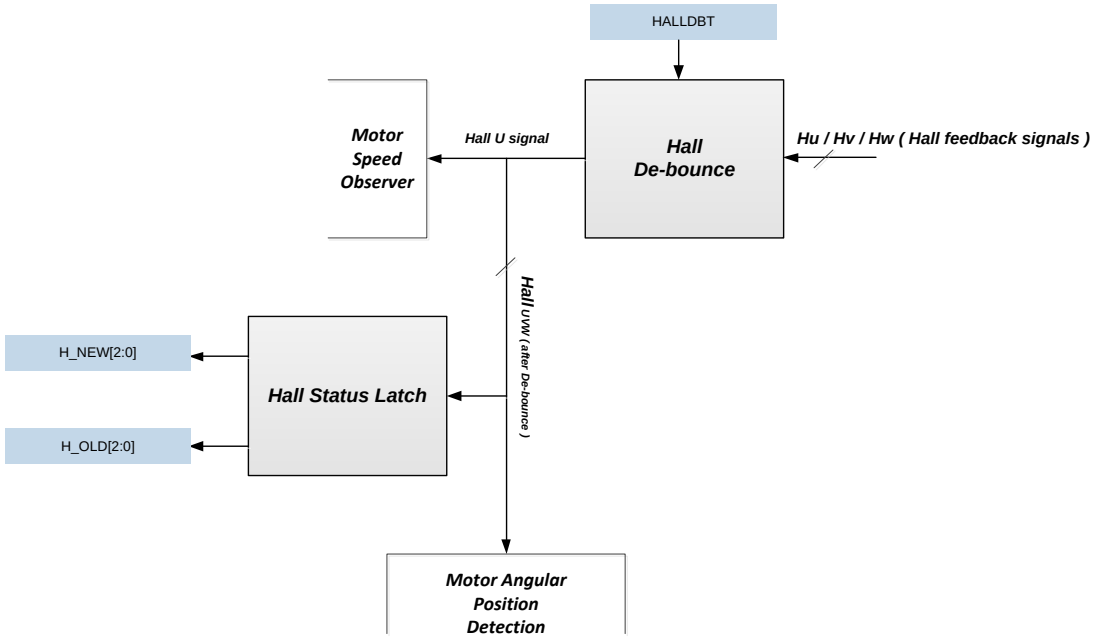


Figure 19.1.1 : Hall I/F Processer Architecture

The Hall sensor is installed in the motor. When the motor is running, it will generate a lot of noise, causing the hall feedback signals (Huvw) to have a lot of noise. If filtering is not performed, it will cause error commutation of the motor drive.

In the HALL Interface Processer Block, design a de-bounce circuit to filter the three Hall signals. Set the de-bounce time of Hu, Hv and Hw through HALLDBT (see Table 19.1.1), and set the Hall de-bounce settings. The set time is: 1/3MHz X HALLDBT [5:0].

HALLDBT Address = 9CH Reset Value = 00001110B

Hall De-bounce Time Register

	-----	-----	HALLDBT[5:0]					
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

HALLDBT is use to filter the HALL signal.

De-bounce time = 1/3MHz X HALLDBT [5:0]

Table 19.1.1 : HALLDBT SFR Description

Hu (after de-bounce) is connected to the Motor Speed Observer Block to calculate the motor speed, and Hu, Hv and Hw (after de-bounce) are connected to the Motor Angular Position Detection Block to estimate the motor rotor position and six-step control signal.

In the HALL Interface Processer Block, latch the current and previous Hall status and put them in HALLST (see Table 19.1.2) for the MCU to read and use.

HALLST Address = 94H Reset Value = 00000000B

Hall Status Register

	-----	H_OLD[2:0]			-----	H_NEW[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	R	R	R	X	R	R	R

H_OLD[2:0]	Hall old status : [2] : HALL U status. [1] : HALL V status. [0] : HALL W status.
H_NEW[2:0]	Hall new status : [2] : HALL U status. [1] : HALL V status. [0] : HALL W status.

Table 19.1.2 : HALLST SFR Description

19.2 Motor Speed Observer

The Motor Speed Observer provides motor electrical cycle (motor speed) information to the MCU for motor speed close-loop control. The Motor Speed Observer has a built-in counter whose input signal is HALLU. It counts the time from rise edge to rise edge of HALLU to obtain the motor electrical cycle (motor speed) information. See Figure 19.2.1.

First, after setting HCKS (see Table 19.2.1 MCONT1. HCKS SFR) according to the motor speed range, select the clock frequency of the Observer, the hardware starts counting the time of motor electrical cycle, and the MCU can start counting from the ROTORSPEED SFR (see Table 19.2. 2 ROTORSPEED SFR) reads the 16-bits counter value. In the next step, the MCU can perform speed close-loop control according to the ROTORSPEED SFR. Timing diagram, please see Figure 19.2.2.

According to the motor speed range, the value range read by ROTORSPEED SFR must be in the range of 0x0200~0xFFFF to avoid control abnormalities; if the value read by ROTORSPEED SFR is not between 0x0200~0xFFFF, HCKS needs to be changed. In addition, if the value of ROTORSPEED SFR is 0xFFFF, it means that the motor may be rotating very slowly or has stopped running. At this time, the value of MOTOSTOP (see Table 19.2.1 MCONT1. MOTOSTOP SFR) will be "1".

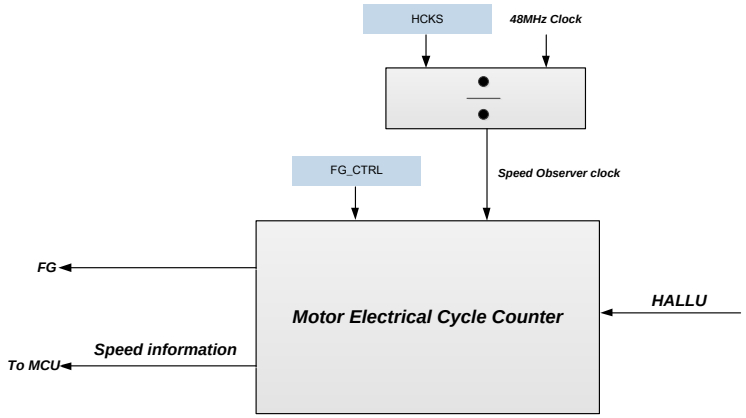


Figure 19.2.1 Motor Speed Observer Architecture

MCONT1 Address = 9DH Reset Value = X0110000B

Motor Control Register 1

	MOTOSTOP	HCKS[2:0]			HALLALS	DMS	MPWMA	AMDS
Bit	7	6	5	4				
Type	R	R/W	R/W	R/W				

MOTOSTOP	1 : Motor Stop	
HCKS[2:0]	Hall clock select :	
	000 : 48MHz/4	100 : 48MHz/64
	001 : 48MHz/8	101 : 48MHz/128

010 : 48MHz/16	110 : 48MHz/256
011 : 48MHz/32	111 : 48MHz/512

Table 19.2.1 MCONT1. HCKS and MOTOSTOP SFR

ROTORSPEEDH Address = 97H Reset Value = 11111111B

Rotor Speed Count Register High

	ROTORSPEED[15:8]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

ROTORSPEEDL Address = 96H Reset Value = 11111111B

Rotor Speed Count Register Low

	ROTORSPEED[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

Table 19.2.2 ROTORSPEED SFR (Rotor Speed Count Register)

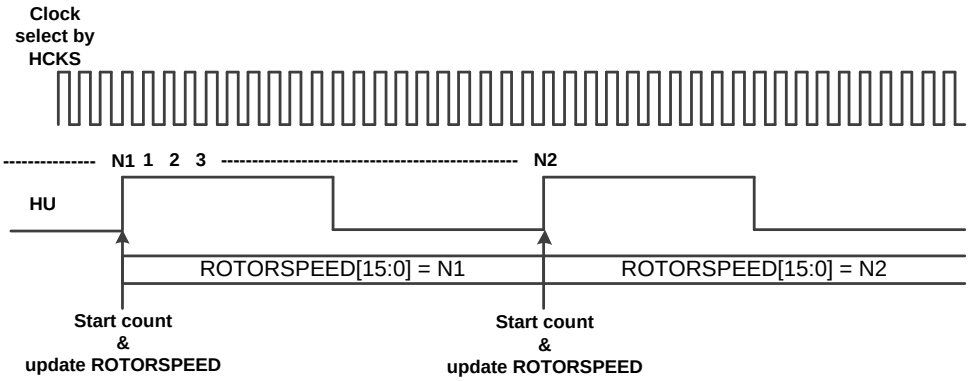


Figure 19.2.2 Rotor electrical cycle counter

In addition to providing motor electrical cycle (motor speed) information, Motor Speed Observer can also output a fixed pulse number in a hall cycle according to the setting of FG_CTRL SFR (see Table 19.2.3), that is, it can be used as a frequency generator (FG). Figure 19.2.3 shows an FG output waveform when the control bits in the FG_CTRL SFR are FG_EN=1, FG10PT8P=0, and FGPULSE_SEL=5.

FG_CTRL Address = C5H Reset Value = 0x00H

Frequency Generator Control Register

	FG_EN	FG10PT8P	-----	-----	FGOUT_SEL	FGPULSE_SEL		
Bit	7	6	5	4	3	2	1	0
Type	W	W	X	X	W	W		

FG_EN FG output enable:

	0 : Disable 1 : Enable		
FG10PT8P	10 poles FG Convert to 8 poles FG: 0 : Normal 1 : Enable		
FGOUT_SEL	FG output pin select: 0 : out to CH3 pin 1 : out to TX pin		
FGPULSE_SEL	FG pulse number selection:		
		FG10PT8P = 0	*FG10PT8P = 1*
	000 :	1 pulses/cycle	4 pulses/5-cycle
	001 :	2 pulses/cycle	8 pulses/5-cycle
	010 :	4 pulses/cycle	16 pulses/5-cycle
	011 :	5 pulses/cycle	20 pulses/5-cycle
	100 :	8 pulses/cycle	32 pulses/5-cycle
	101 :	12 pulses/cycle	48 pulses/5-cycle

Table 19.2.3 FG_CTRL SFR (Frequency Generator Register)

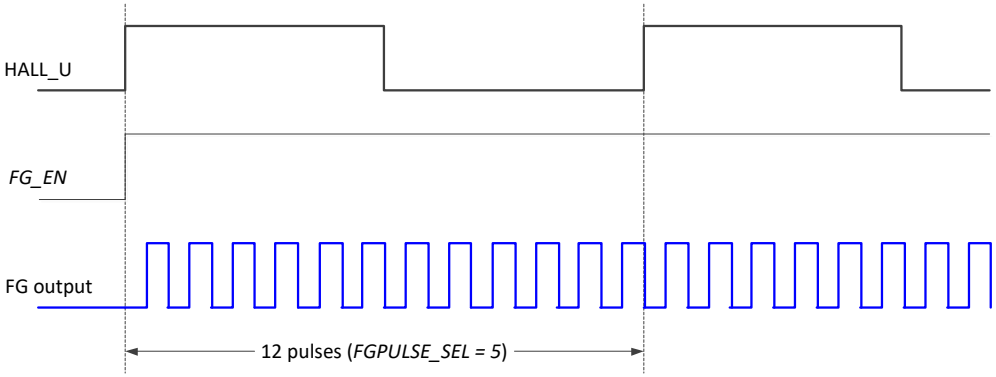


Figure 19.2.3 FG output when FG_EN=1, FG10PT8P=0, and FGPULSE_SEL=5

19.3 Motor Angular Position Detection

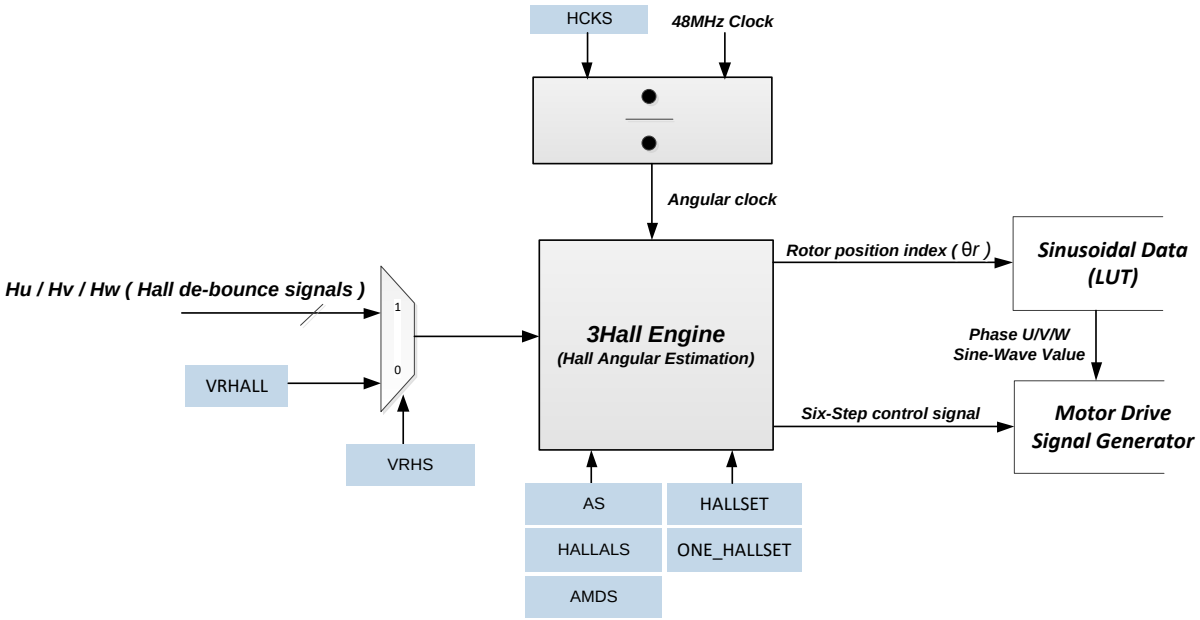


Figure 19.3.1 Motor Angular Position Architecture

Motor Angular Position Detection Block has a built-in 3Hall Engine, which estimates the rotor position index and six-step control signal based on the hall input signal. Its input signal can be selected through VRHS. When VRHS=0 (see Table 19.3.1), its 3Hall Engine The input signal is Real hall (i.e. external hall signals input). Otherwise, VRHS=1, the input signal is VRHALL SFR (see Table 19.3.2).

MCONT2 Address = A2H Reset Value = 00000000B

Motor Control Register 2

	-----	-----			-----	VRHS	AOCPS	-----
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	X

VRHS Virtual Hall select :

0 : Real Hall. (HALL U, HALL V, HALL W)

1 : Virtual Hall.

Table 19.3.1 VRHS SFR

VRHALL Address = D9H Reset Value = 00000101B

Virtual Hall Register

	-----	-----	-----	-----	-----	VRH[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

VRH[2:0] Virtual Hall value.

VRH.2 is Virtual HALL U. VRH.1 is Virtual HALL V. VRH.0 is Virtual HALL W.

Table 19.3.2 VRHALL SFR

First, after setting HCKS (Table 19.3.3 MCONT1. HCKS SFR) according to the motor speed range, select the clock frequency of angular estimate, the hardware starts counting the time of motor angle step, the 1 angle step is 0.9375º (384 step / 360º), according to the motor speed range, setting the appropriate HCKS can count each angle step to have the best resolution.

Hall sensor has two installation methods that hall signal is aligned with Line Voltage or Phase Voltage.
Hall alignment select HALLALS = 0 (see Table 19.3.3), Hall signal is aligned with Line Voltage, in addition, when HALLALS = 1, Hall signal is aligned with Phase Voltage.

MCONT1 Address = 9DH Reset Value = X0110000B

Motor Control Register 1

	MOTOSTOP	HCKS[2:0]			HALLALS	DMS	MPWMA	AMDS
Bit	7	6	5	4	3	2	1	0
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

HCKS[2:0]	Hall clock select :	
	000 : 48MHz/4	100 : 48MHz/64
	001 : 48MHz/8	101 : 48MHz/128
	010 : 48MHz/16	110 : 48MHz/256
	011 : 48MHz/32	111 : 48MHz/512
HALLALS	Hall alignment select :	
	0 : Line voltage (Line to Line)	
	1 : Phase voltage	
AMDS	Auto mode direction select :	
	0 : When MPWMA = ‘1’, driving direction is forward.	
	1 : When MPWMA = ‘1’, driving direction is reverse.	

Table 19.3.3 MCONT1.HCKS / HALLALS / AMDS SFR

CGH001A must set the forward direction HALL sequence to the HALLSET SFR so that CGH001A can automatically generate the signals required for its motor driving. When HALLALS = 0, Figure 19.3.2 and Figure 19.3.3 are HALLSET (see Table 19.3.4) settings determine the description.

Figure 19.3.3, when HALLALS = 1, the hall signals is aligned with Phase voltage, Phase to Phase voltage sequence is Vuv leads Vvw by 120 degrees and Vvw leads Vwu by 120 degrees. (Forward direction defines in CGH001A). As shown

in the figure, hall signals forward sequence is 5 4 6 2 3 1, filled in HALLSET1_1, HALLSET1_2, HALLSET2_1, HALLSET2_2, HALLSET3_1 and HALLSET3_2 in order.

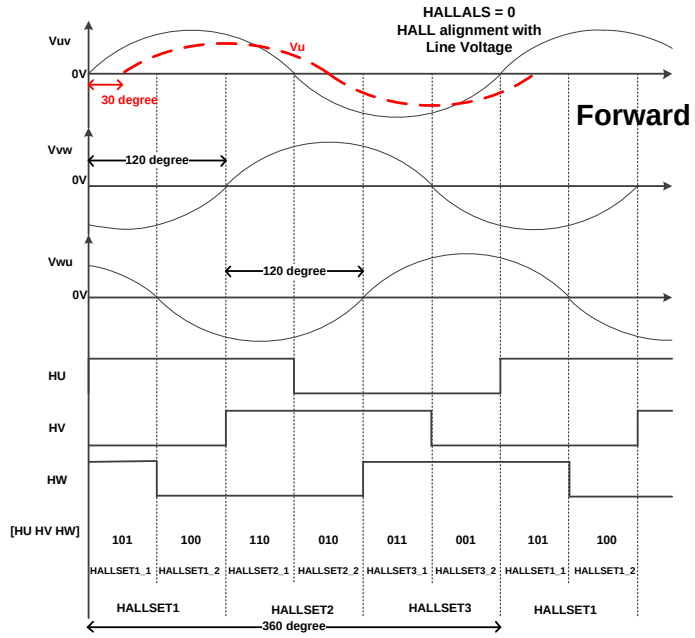


Figure 19.3.2 HALLSET (Hall Setting Register 1, 2, 3)

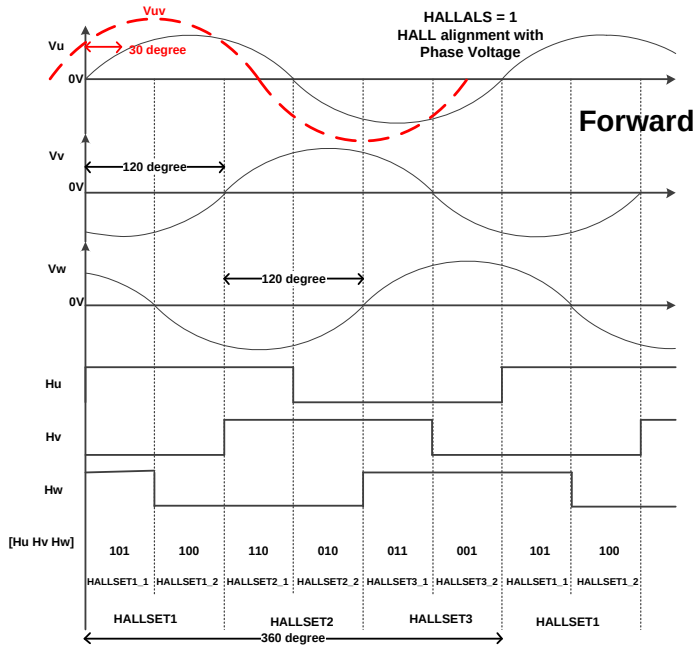


Figure 19.3.3 Hall signal is alignment with Phase Voltage.

AS (see Table 19.3.5) is setting for leading angle, AS resolution is 0.9375º/bit, AS setting range is -59.0625° ~ 59.0625.

When MWPMA = '1' (auto mode), AS is active.

MDE provides motor reverse setting and simply set AMDS (see Table 19.3.3) to reverse the motor.

HALLSET1 (SYNC) Address = 91H Reset Value = 01000101B

Hall Setting Register 1

	-----	HALLSET1_2[2:0]			-----	HALLSET1_1[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	X	R/W	R/W	R/W

[2] : HALL U status. [1] : HALL V status. [0] : HALL W status.

HALLSET2 (SYNC) Address = 92H Reset Value = 00100110B

Hall Setting Register 2

	-----	HALLSET2_2 [2:0]			-----	HALLSET2_1[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	X	R/W	R/W	R/W

[2] : HALL U status. [1] : HALL V status. [0] : HALL W status.

HALLSET3 (SYNC) Address = 93H Reset Value = 00010011B

Hall Setting Register 3

	-----	HALLSET3_2[2:0]			-----	HALLSET3_1[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	X	R/W	R/W	R/W

[2] : HALL U status. [1] : HALL V status. [0] : HALL W status.

Table 19.3.4 HALLSET123 SFR

AS (SYNC) Address = 8FH Reset Value = 00000000B

Angle Shift Control Register

	AS_LS	-----	AS_VALUE[5:0]					
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	R/W	R/W	R/W	R/W	R/W	R/W

AS_LS Angle Shift Lag select:

0 : 0° ~59.0625° = 0~ 63(AS_VALUE)

1 : 0° ~-59.0625° = 0~ -63(AS_VALUE)

Table 19.3.5 AS SFR

The main function of 3Hall Engine is to estimate the U, V, and W phase rotor position index (θr). The 3Hall Engine mainly generates the U, V, and W phase rotor position index (θr) based on the 3 Hall signal status and current speed, combined with the settings of AS, HALLALS, and AMDS, and then generates sine data by looking up the Sinusoidal Data (LUT) Block. In addition, in order to reduce external PCB costs, 3Hall Engine also supports observing the status and current speed of a single Hall signal (Hall_U). Through additional settings of ONE_HALLSET (see Table 19.3.6), it can also

generate U, V, and W phase rotor position indexes (θr).

ONE_HALLSET	Address = 95H				Reset Value = 0000_0000B			
One Hall Setting Register (when SFR IMPMISC_KEY = 0xa5)								
	STA_ZONE_EN	3TO1_RUN	-----	-----	1HALL_ONLY	ZONE[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	W	W	X	X	W	W	W	W

STA_ZONE_EN	Hall U rising edge start zone setting enable (for 3-Hall Start and 1-Hall Rotation or One Hall solution using) 0 : Hall U rising edge start zone setting by hardware when 1-hall run 1 : Hall U rising edge start zone setting by software when 1-hall run
3TO1_RUN	3-Hall Start and 1-Hall Rotation enable 0 : 3-Hall Rotation or 1-Hall Start up and Rotation 1 : 3-Hall Start and 1-Hall Rotation
1HALL_ONLY	One Hall Only enable (Only Hall U for One Hall Rotation) 0 : Disable One Hall Only 1 : Enable One Hall Only
ZONE	Hall U rising edge start ZONE **(when** STA_ZONE_EN **=1)** 000: Hall U rising edge start at ZONE0 (HALLSET1_1), start angle is 0 001: Hall U rising edge start at ZONE1 (HALLSET1_2), start angle is 64 010: Hall U rising edge start at ZONE2 (HALLSET2_1), start angle is 128 011: Hall U rising edge start at ZONE3 (HALLSET2_2), start angle is 192 100: Hall U rising edge start at ZONE4 (HALLSET3_1), start angle is 256 101: Hall U rising edge start at ZONE5 (HALLSET3_2), start angle is 320

Table 19.3.6 ONE_HALLSET SFR

The usage of a single hall operation can be set by the three bits STA_ZONE_EN, 3TO1_RUN, and 1HALL_ONLY in the ONE_HALLSET SFR and the area aligned with the rising edge of Hall_U (determined by HALL_SET). As shown in Figure 19.3.4, when the rising edge of Hall_U is aligned with ZONE1, if you want to use **3 halls to start up and then 1 hall to rotate**, the ONE_HALLSET SFR should be set to 0x41.

If the **1 hall solution** is adopted, that is, the software planning startup program is used with the hardware to automatically calculate the rotor position index; when the rotor is started and you want to switch to the 1 hall fully automatic auxiliary rotor rotation supported by the hardware, after executing the 1 hall start After the program, set the ONE_HALLSET SFR to 0x89 (HALL_U rising edge is aligned in ZONE1), which means MDE will take over the 1 hall automatic rotation program.

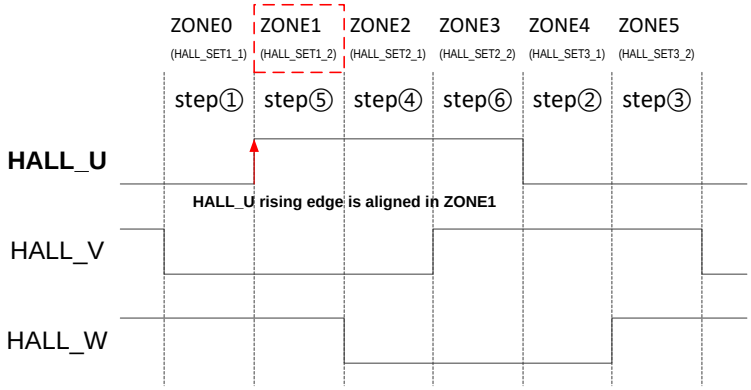


Figure 19.3.4 Hall_U rising edge is aligned in ZONE1.

19.4 Sinusoidal Data (LUT)

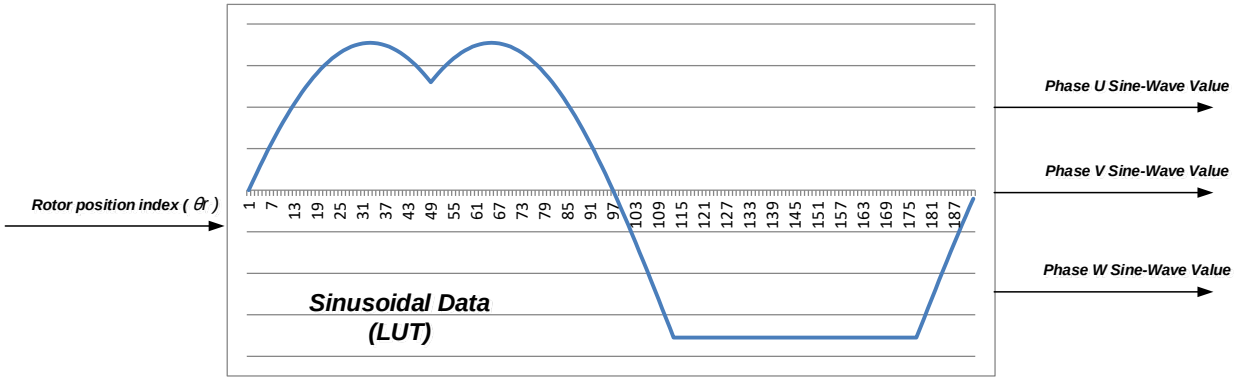


Figure 19.4.1 : Sinusoidal Data (LUT) Architecture

The Sinusoidal Data (LUT) Block has a built-in three-phase SVPWM look-up table. The input signal is the U, V and W phase Rotor position index (θr) estimated by the Motor Angular Position Detection Block. After looking up the table, the three-phase sine wave value is output to the Motor Signal Generator Block to perform three-phase sine wave calculations.

19.5 Motor Drive Signal Generator

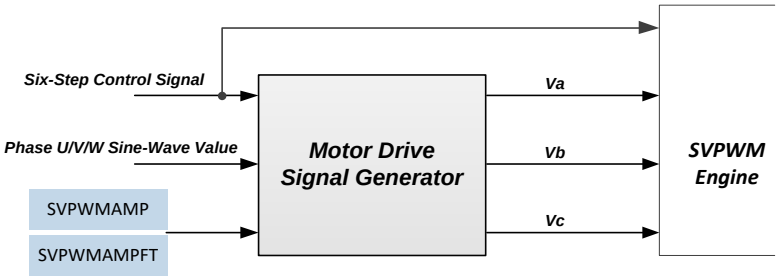


Figure 19.5.1 : Motor Drive Signal Generator Architecture

Motor Drive Signal Generator Block sets SVPWMAMP and SVPWMAMPFT SFR (see Table 19.5.1) to change the amplitude of the three-phase sine wave according to the required speed of the motor drive. The corresponding sine wave value is determined by the Sinusoidal Data (LUT) Block table lookup.

Through the operation of SVPWMAMP and SVPWMAMPFT and Phase U V W sine-wave vale, the output voltage values of Va, Vb and Vc are obtained and provided to the SVPWM Engine Block for SVPWM modulation.

The SVPWM of CGH001A has two modes: seven-segment and five-segment (see Section 19.6.2) SVPWM. The setting range of SVPWMAMP is 0 ~ MPWM_CYC/2. When the value is larger, the three-phase voltage output by it will be larger.

SVPWMAMPFT is the fine tune of SVPWMAMP. Its function is between the two levels of SVPWMAMP. It can have 8 levels of fine tune to achieve accurate speed control.

SVPWMAMPH(SYNC) Address = C4H Reset Value = 00000000B

SVPWM Amplitude Register High

	-----	-----	-----	-----	-----	SVPWMAMP[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

SVPWMAMPL(SYNC) Address = C3H Reset Value = 00000000B

SVPWM Amplitude Register Low

	SVPWMAMP[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SVPWMAMPFT Address = DAH Reset Value = 00000000B

SVPWM Amplitude Fine-Tune Register

	-----	-----	-----	-----	-----	SVPWMAMPFT[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

Table 19.5.1 SVPWMAMP and SVPWMAMPFT SFR

19.6 SVPWM Engine

19.6.1 SVPWM Engine Architecture

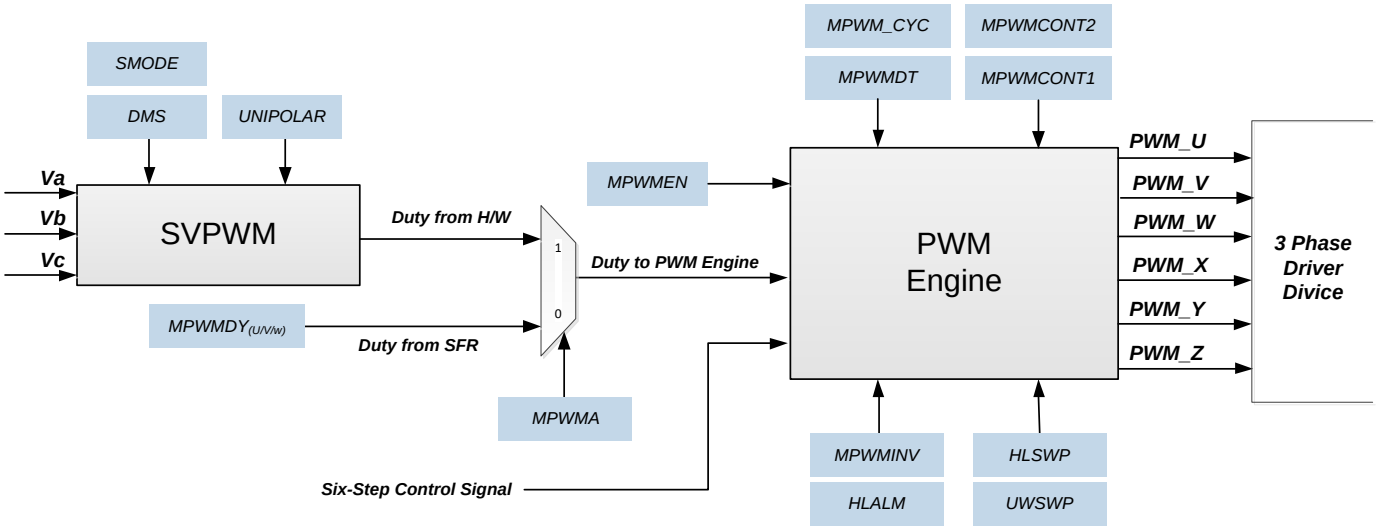


Figure 19.6.1 : SVPWM Engine Block Architecture

19.6.2 SVPWM Current Drive

Motor sinusoidal drive is based on providing sinusoidal current changes to each motor winding at the rotor position. These currents are phase-shifted by 120° from each other, relative to its corresponding Hall sensor. In BLDC motor control, the drive signals that are used require variable voltages that change with respect to the speed and position of the motor. This variable voltage is applied using the PWM technique. Provide PWM signals of sine wave to MOSFET inverter through PWM Engine. In this application, the sinusoidal current drive is applied using data extracted from the Space Vector Pulse-Width Modulation (SVPWM) technique.

The SVPWM method is a vector-based scheme used in three-phase systems, such as motor control applications. Rather than producing pure sinusoid waveform from the drive signals for each motor terminals with respect to ground, SVPWM generates three sinusoidal line-to-line voltage (differential voltage) between two terminals. A space vector representation is created, where the spaces between unit vectors are separated by 60.0° correspond to every state in an electrical cycle, as shown in Figure 19.6.2. Each desired voltage can be simulated by adding the components of two adjacent active vectors and null vectors represented by the 000 and 111 logic states (located at the origin). The resulting desired voltage is represented by the manipulated duty cycle of PWM peripheral.

Table 19.6.1 provides the equation for the PWM switching time for each sector. Once the approximate angular position is identified, the resultant vector magnitude is calculated, with respect to the adjacent voltage space vectors and null vector T0, T1 and T2 representing conduction time within a period.

Sector	Switching Time Equation
1	PWM1 = T1 + T2 + T0/2 PWM2 = T2 + T0/2 PWM3 = T0/2
2	PWM1 = T1 + T0/2 PWM2 = T1 + T2 + T0/2 PWM3 = T0/2
3	PWM1 = T0/2 PWM2 = T1 + T2 + T0/2 PWM3 = T2 + T0/2
4	PWM1 = T0/2 P PWM2 = T1 + T0/2 PWM3 = T1 + T2 + T0/2
5	PWM1 = T2 + T0/2 PWM2 = T0/2 PWM3 = T1 + T2 + T0/2
6	PWM1 = T1 + T2 + T0/2 PWM2 = T0/2 PWM3 = T1 + T0/2

Table 19.6.1 Equations for PWM Switching Time by each Sensor

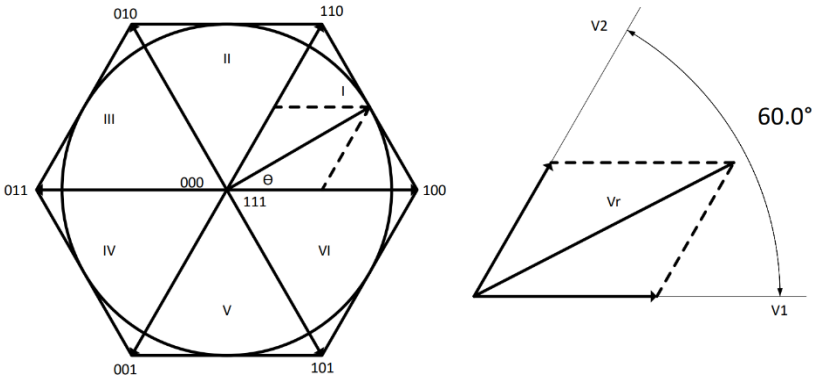


Figure 19.6.2 : SVPWM Representation in an Orthogonal Plane

The approximate PWM output from SVPWM, with respect to its angular position, is plotted in Figure 19.6.3. The waveform produced has a shape of a saddle due to the third harmonic injection by SVPWM. Each PWM output is shifted 120° from each other. The angular position is scaled from 360° to 384 for more convenient implementation in this application.

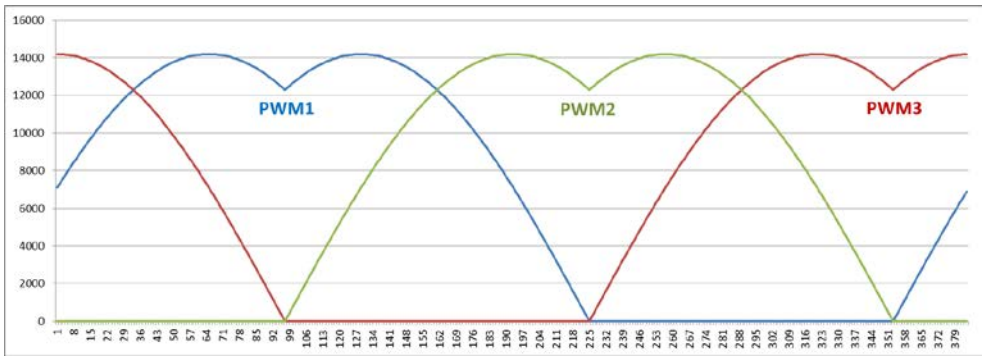


Figure 19.6.3 : SVPWM Voltage Waveform

CGH001A provides two types of SVPWM, namely seven-segment SVPWM (see Figure19.6.4) and five-segment

SVPWM (see Figure19.6.5). Seven-segment SVPWM current waveform is smoother, and its harmonic interference is smaller. Five-segment SVPWM reduces switching losses because each of its three phases does not switch for one-third of a cycle. In sine wave drive, you can use SMODE to set the SVPWM mode to seven-segment SVPWM or five-segment SVPWM (see Table19.6.2).

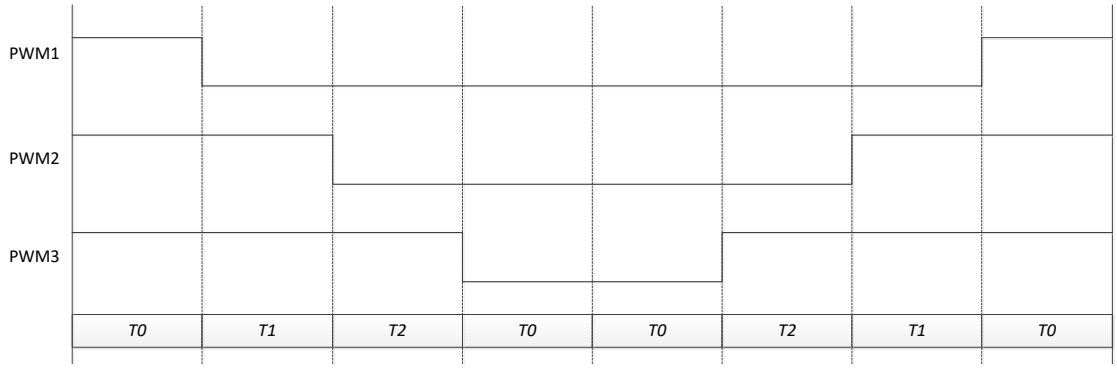


Figure 19.6.4 : Seven-Segment SVPWM Output Level

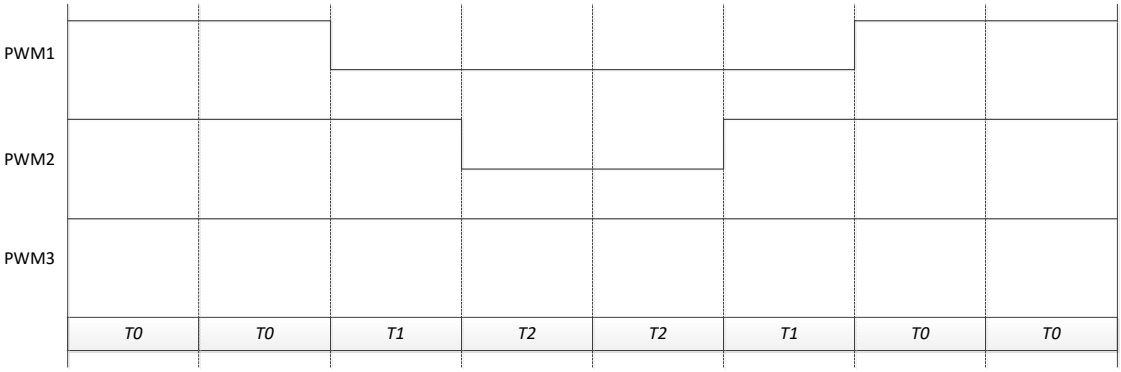


Figure 19.6.5 : Five-Segment SVPWM Output Level

IMPMISC_FUN Address = AFH Reset Value = 00010000B

Improve Miscellaneous Function Setting Register (when SFR IMPMISC_KEY = 0xa5)

	SMODE	CSHC	SIN_USER	MINDUTY_EN	UNIPOLAR	HLALM	HLSWP	UWSWP
Bit	7	6	5	4	3	2	1	0
Type	W	W	X	W	W	W	W	W

SMODE SVPWM Mode (when MCONT1.DMS = 1) :

0 : Seven-segment SVPWM

1 : Five-segment SVPWM

Table19.6.2 : IMPMISC_FUN SMODE SFR

19.6.3 Motor PWM Output Setting

Motor PWM Engine is based MPWMEN (see Table19.6.3) to active PWM counter, when MPWMEN = 1, Motor PWM output (U, V, W, X, Y, Z).

MPWMA (see Table19.6.4) can select the Duty input source of Motor PWM. When MPWMA = 0, Motor PWM determines PWM Duty by $MPWMDY_{(U/V/W)}$ (see Table19.6.5), and outputs PWM signal.

MPWMA = 1, the calculated PWM Duty value of Va, Vb and Vc is directly input to the SVPWM Engine for PWM modulation.

CGH001A supports sine wave and square wave drive modes. Simply set DMS (see Table19.6.4) to switch sine wave or square wave mode. When DMS = 0, it is square wave drive mode. On the contrary, DMS = 1 is sine wave drive model.

MCONT3 Address = ACH Reset Value = 00000011B

Motor Control Register 3

	MPWMEN	-----		ERS_MASK	-----	I_SHORT[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	X	W	X	R/W	R/W	R/W

MPWMEN	MPWM timer Enable : 0 : Stop 1 : Run

Table19.6.3 : MCONT3. MPWMEN SFR (NHOL=1)

MCONT1 Address = 9DH Reset Value = X0110000B

Motor Control Register 1

	MOTOSTOP	HCKS[2:0]			HALLALS	DMS	MPWMA	AMDS
Bit	7	6	5	4	3	2	1	0
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DMS	Driving mode select : 0 : 120° Square-Wave 1 : Sin-Wave
MPWMA	MPWM auto mode : 0 : Disable. (control by firmware) 1 : Enable. (control by MDE)

Table19.6.4 : MCONT1. DMS & MPWMA SFR

MPWMDYUH (SYNC) Address = A6H Reset Value = 00000111B

Motor PWM Duty Register U High (Phase U)

	-----	-----	-----	-----	-----	MPWMDYU[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

MPWMDYUL (SYNC) Address = A5H Reset Value = 11111111B

Motor PWM Duty Register U Low (Phase U)

	MPWMDYU[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MPWMDYVH (SYNC) Address = ABH Reset Value = 00000111B

Motor PWM Duty Register V High (Phase V)

	-----	-----	-----	-----	-----	MPWMDYV[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

MPWMDYVL (SYNC) Address = AAH Reset Value = 11111111B

Motor PWM Duty Register V Low (Phase V)

	MPWMDYV[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MPWMDYWH (SYNC) Address = AEH Reset Value = 00000111B

Motor PWM Duty Register W High (Phase W)

	-----	-----	-----	-----	-----	MPWMDYW[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

MPWMDYWL (SYNC) Address = ADH Reset Value = 11111111B

Motor PWM Duty Register W Low (Phase W)

	MPWMDYW[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table19.6.5 : MPWMDY$_{(U/V/W)}$ SFR

In square wave drive mode, CGH001A provides unipolar PWM switching technology to reduce static power losses when

using MOSFET switches. Unipolar PWM switching means that when the lower side switches PWM, the upper side switches the complementary PWM signal to the lower side. Therefore, during unipolar PWM switching, dead time insertion is introduced in the complementary upper and lower PWM signals (see Figure19.6.6). When in square wave drive mode and setting UNIPOLAR = 1, it enables unipolar PWM switching (see Table 19.6.6). It should be noted that before enabling unipolar PWM switching, the PWM output mode must also be set: High side PWM (U, V, W) to "Active High" and Low side PWM (X, Y, Z) to "Active Low" (see Table19.6.8).

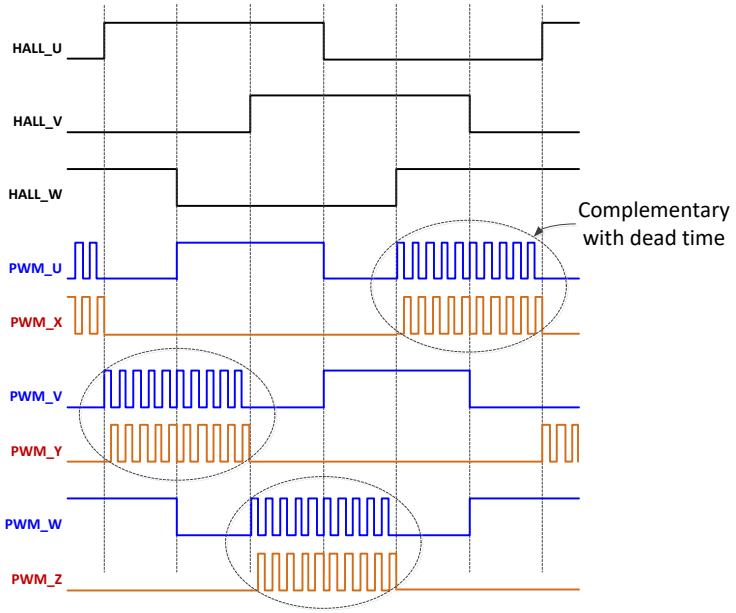


Figure 19.6.6 : Unipolar PWM Switching

IMPMISC_FUN Address = AFH Reset Value = 00010000B

Improve Miscellaneous Function Setting Register (When SFR IMPMISC_KEY = 0xa5)

	SMODE	CSHC	SIN_USER	MINDUTY_EN	UNIPOLAR	HLALM	HLSWP	UWSWP
Bit	7	6	5	4	3	2	1	0
Type	W	W	X	W	W	W	W	W

UNIPOLAR Enable unipolar PWM Switching (when MCONT1.DMS = 0) :

0 : Disable Unipolar PWM Switching

1 : Enable Unipolar PWM Switching

Table19.6.6 : IMPMISC_FUN UNIPOLAR SFR

Period of Motor PWM is based on MPWM_CYC (see Table19.6.7) setting value. The base frequency of Motor PWM counter is 48MHz. The counter counts up to MPWM_CYC and then counts down to 0 (see Figure19.6.7). Therefore, the value set by MPWM_CYC determines the frequency of Motor PWM. For example: MPWM_CYC = 1250, Period of Motor PWM = 1250 x 2 x 1/(48MHz) = 52.08us, Freq. of Motor PWM is 19.2KHz.

MPWM_CYC_H (SYNC) Address = A4H Reset Value = 00000000B

Motor PWM Max Register High

	-----	-----	-----	-----	-----	MPWM_CYC[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

MPWM_CYC_L (SYNC) Address = A3H Reset Value = 00000010B

Motor MPWM_CYC Register Low

	MPWM_CYC[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table19.6.7 : MPWM_CYC SFR Description

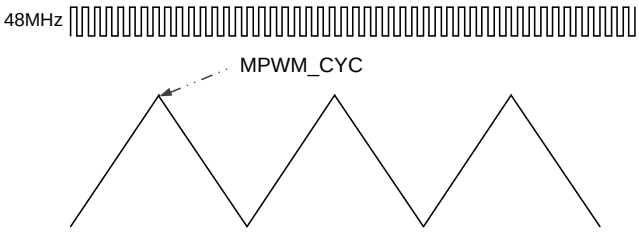


Figure 19.6.7 : Motor PWM is count up and down timer

Motor PWM output (U, V, W, X, Y, Z) has 4 type modes to be setting. High side PWM (U、V、W) can be setting mode by MPWMCONT1 (see Table19.6.8) , Low side PWM (X、Y、Z) can be setting mode by MPWMCONT2 (see Table19.6.8), the 4 type mode is “Force Low”, “Force High”, “Force Low”, “Active High” and “Active Low”.

MPWMCONT1 (SYNC) Address = B1H Reset Value = 00000000B

MPWM Control Register 1

	-----	-----	PWMW[1:0]		PWMV[1:0]		PWMU[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

PWMW	Phase W High-side (W) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low
PWMV	Phase V High-side (V) output mode select :

	00 : Force Low 01 : Force High 10 : Active High 11 : Active Low
PWMU	Phase U High-side (U) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low

MPWMCONT2 (SYNC) Address = B2H Reset Value = 00000000B

MPWM Control Register 2

	-----	-----	PWMZ[1:0]		PWMY[1:0]		PWMX[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

PWMZ	Phase W Low-side (Z) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low
PWMY	Phase V Low-side (Y) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low
PWMX	Phase U Low-side (X) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low

Table19.6.8 : MPWMCONT1/2 SFR Description

MPWMDT (see Table19.6.9) compensation PWM output with Dead-Time is use to prevent short-though between high-side and low-side power device. Dead-Time setting example: if MPWMDT = 100, Dead Time = 100 x (1 / 48MHz) = 2.08us.

MPWMDT (SYNC)			Address = A7H		Reset Value = 00000000B			
Motor PWM Dead-Time Register								
	MPWMDT[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table19.6.9 : MPWMDT SFR Description

Via MPWMINV (see Table18.6.10) setting , Motor U, V, W, X, Y, Z PWM output support Inverse function that is to inverse the PWM output signal at the last stage output.

MPWMINV(SYNC)			Address = B3H		Reset Value = 00000000B			
MPWM Inverse Selection Register								
	-----	-----	ZINV	WINV	YINV	VINV	XINV	UINV
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

ZINV	Low-side PWM Z output inverse select : 0 : Non-inverse 1 : Inverse
WINV	High-side PWM W output inverse select : 0 : Non-inverse 1 : Inverse
YINV	Low-side PWM Y output inverse select : 0 : Non-inverse 1 : Inverse
VINV	High-side PWM V output inverse select : 0 : Non-inverse 1 : Inverse
XINV	Low-side PWM X output inverse select : 0 : Non-inverse 1 : Inverse
UINV	High-side PWM U output inverse select : 0 : Non-inverse 1 : Inverse

Table19.6.10 : MPWMINV SFR Description

Figure19.6.8 illustrates the waveform output by Motor PWM when MPWMCONT1, MPWMCONT2, MPWMINV and MPWMDT are set at the same time.

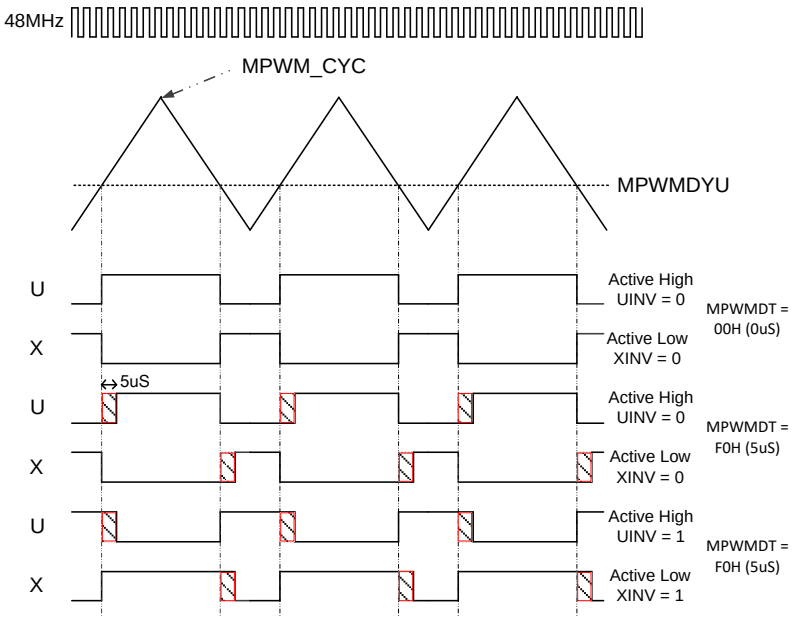


Figure 19.6.8 : PWM Output with Dead Time and PWM mode

In order to connect with the 3 phase Gate-driver and optimize PCB Layout considerations, the Motor PWM output (U, V, W, X, Y, Z) has a swap function, which can be performed via HLALM, HLSWP, UWSWP (see Table19.6.10). The combination of swap is shown in Figure 19.6.9.

IMPMISC_FUN Address = AFH Reset Value = 00010000B

Improve Miscellaneous Function Setting Register (When SFR IMPMISC_KEY = 0xa5)

	SMODE	CSHC	SIN_USER	MINDUTY_EN	UNIPOLAR	HLALM	HLSWP	UWSWP
Bit	7	6	5	4	3	2	1	0
Type	W	W	X	W	W	W	W	W

HLALM	PWM High/Low Side Alignment: 0 : PWM_U, PWM_X, PWM_V, PWM_Y, PWM_W, PWM_Z 1 : PWM_U, PWM_V, PWM_W, PWM_X, PWM_Y, PWM_Z
HLSWP	PWM High and Low Side Swap 0 : PWM_U, PWM_X, PWM_V, PWM_Y, PWM_W, PWM_Z 1 : PWM_X, PWM_U, PWM_Y, PWM_V, PWM_Z, PWM_W
UWSWP	PWM_U/PWM_X and PWM_W/PWM_Z Swap 0 : PWM_U, PWM_X, PWM_V, PWM_Y, PWM_W, PWM_Z 1 : PWM_W, PWM_Z, PWM_V, PWM_Y, PWM_U, PWM_X

Table19.6.10 : IMPMISC_FUN HLALM, HLSWP, and UWSWP SFR

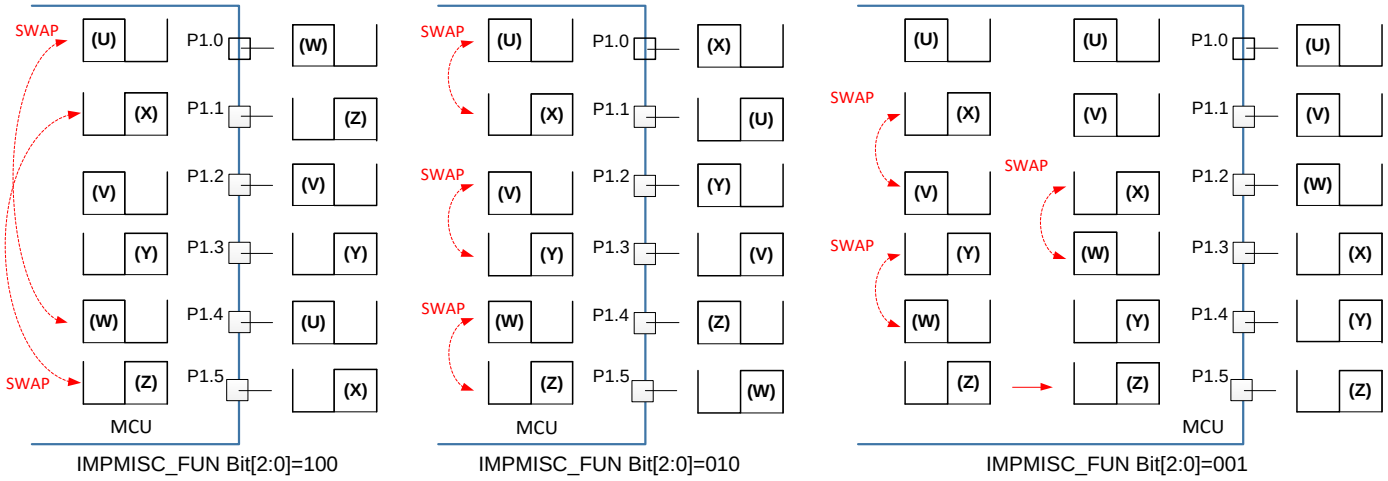


Figure 19.6.9 : PWM Pin Swap

19.7 OCP Protection (Over Current Protection)

19.7.1 OCP Block Architecture

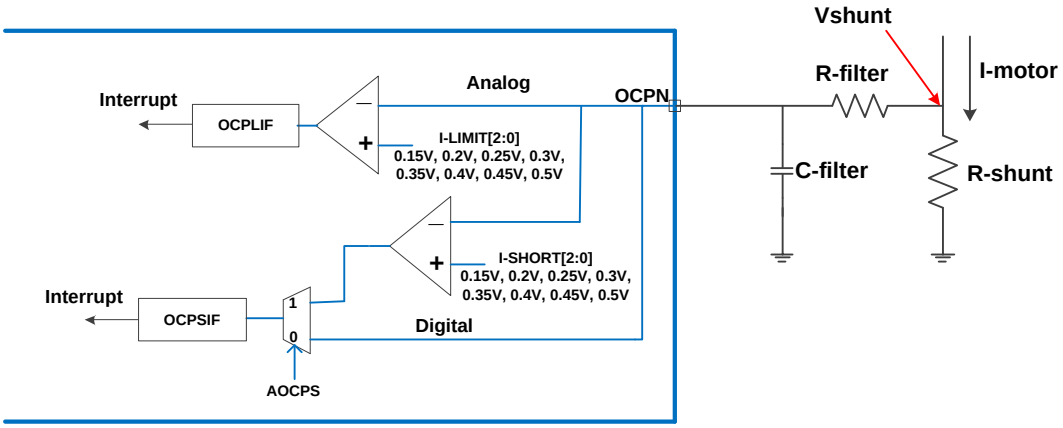


Figure 19.7.1 : OCP Unit Architecture

19.7.2 OCP Block description and setting

CGH001A is embedded H/W Over Current Protection Circuit, supports Analog and Digital OCP two modes, when AOCPS = 1 (see Table19.7.1), that is, set to Analog OCP, the built-in OCP comparator will be used to detect over current status, the voltage setting value of its comparator is I_ SHORT (see Table19.7.2), When the OCPN voltage value is greater than the I_ SHORT set voltage value, H/W will immediately force the PWM to 0 to protect the Power Device (MOS, IGBT..). In addition, CGH001A is embedded 2nd OCP protection, when the OCPN voltage value is greater than the I_ LIMIT (see Table19.7.3) set voltage value, OCP H/W will only send I_LIMIT interrupt signal and will not turn off the PWM signal. In case of overload, perform load reduction operation first.

AOCPS = 0 (see Table19.7.1), turn on Digital OCP mode, Digital OCP is generally used when connected to the IPM module. The Fault PIN of the IPM is directly connected to the OCPN pin for OCP protection.

MCONT2 Address = A2H Reset Value = 00000000B

Motor Control Register 2

	-----	-----			-----	VRHS	AOCPS	-----
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	X

AOCPS	Analog OCP select : 0 : Digital OCP 1 : Analog OCP

Table19.7.1 : AOCPS SFR Description

MCONT3 Address = ACH Reset Value = 00000011B

Motor Control Register 3

	MPWMEN	-----		ERS_MASK	-----	I_SHORT[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	X	W	X	R/W	R/W	R/W

I_SHORT[2:0]	OCP SHORT level select : (OCPSIF) 000 : 0.15V 001 : 0.2V 010 : 0.25V 011 : 0.3V (default) 100 : 0.35V 101 : 0.4V 110 : 0.45V 111 : 0.5V

Table19.7.2 : MCONT3. I_SHORT SFR (NHOL=1)

AOCPCONT Address = 9EH Reset Value = 00001111B

Analog OCP Control Register

	OCPLT	-----	-----	I_LIMIT[2:0]			-----	
Bit	7	6	5	4	3	2	1	0
Type	R	X	X	R/W	R/W	R/W	R/W	R/W

OCPLT	OCP Limit status 0 : No Over current Limit. 1 : Over current Limit occur.
I_LIMIT[2:0]	OCP LIMIT level select : (OCPLIF) 000 : 0.15V 001 : 0.2V 010 : 0.25V 011 : 0.3V (default) 100 : 0.35V 101 : 0.4V 110 : 0.45V 111 : 0.5V

Table19.7.3 : AOCPCONT SFR Description

The MCU may read the OCPST (see Table19.7.4) to observe the over current status of the system. When OCPST =1, the system is in the over current state. In addition, The MCU may read the OCPLT (see Table19.7.3) to observe the

OCP Limit current status of the system. When OCPLT =1, the system is in the OCP Limit current state.

Analog OCP can set digital de-bounce time to avoid OCP malfunction caused by noise. By setting OCPDBT (see Table19.7.4), Analog OCP 0~1.291uS de-bounce time can be set.

There are 2 modes to release OCP status, Auto Mode and User Mode. For its setting and action, please refer to Figure 19.7.2 and Figure 19.7.3.

OCPCONT Address = A1H Reset Value = 00000100B

OCP Control Register

	OCPST	OCPDBT[4:0]					OCPC	OCPMS
Bit	7	6	5	4	3	2	1	0
Type	R	R/W	R/W	R/W	R/W	R/W	W	R/W

OCPST	OCP Short status: 0 : No Over current Short 1 : Over current Short occur. Six PWM output is high-impedance.
OCPDBT[4:0]	PIN OCPN input de-bounce time (default 41.67nS) 0~31 = 0~1.291uS (48MHz/2 fixed)
OCPC	OCP status clear bit : In User mode, user can write '1' to clear OCP status, the PWM will output at next PWM cycle.
OCPMS	OCP mode select : 0 : Auto mode 1: User mode

Table19.7.4 : OCPCONT SFR Description

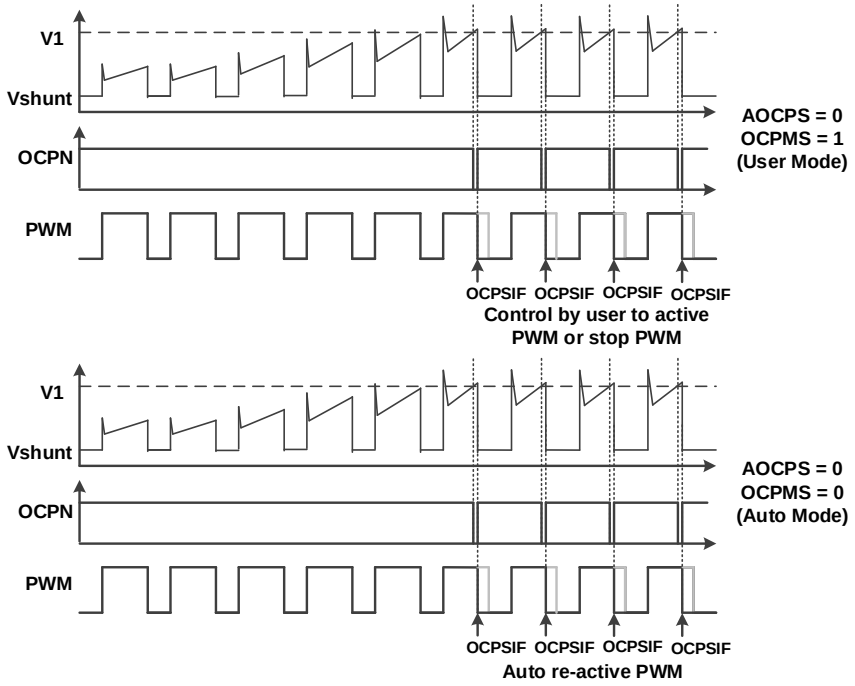


Figure 19.7.2 : Digital OCP Short occur and PWM out

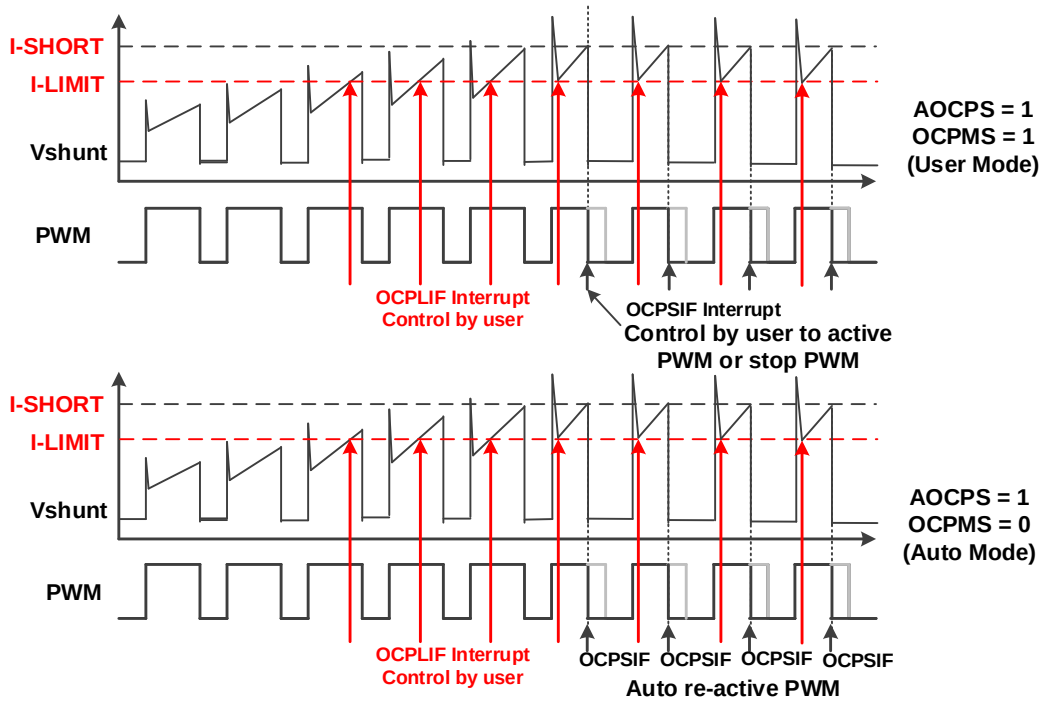


Figure 19.7.3 : Analog OCP Short occur and PWM out

19.8 MDE SFR List

19.8.1 MCONT1 SFR

MCONT1 Address = 9DH Reset Value = X0110000B

Motor Control Register 1

	MOTOSTOP	HCKS[2:0]			HALLALS	DMS	MPWMA	AMDS
Bit	7	6	5	4	3	2	1	0
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MOTOSTOP	1 : Motor Stop
HCKS[2:0]	Hall clock select : 000 : 48MHz/4 001 : 48MHz/8 010 : 48MHz/16 011 : 48MHz/32 100 : 48MHz/64 101 : 48MHz/128 110 : 48MHz/256 111 : 48MHz/512
HALLALS	Hall alignment select : 0 : Line voltage (Line to Line) 1 : Phase voltage
DMS	Driving mode select : 0 : 120° Square-Wave 1 : Sin-Wave
MPWMA	MPWM auto mode : 0 : Disable. (control by firmware) 1 : Enable. (control by MDE)
AMDS	Auto mode direction select : 0 : When MPWMA = '1', driving direction is forward. 1 : When MPWMA = '1', driving direction is reverse.

19.8.2 MCONT2 SFR

MCONT2 Address = A2H Reset Value = 00000000B

Motor Control Register 2

	-----	-----			-----	VRHS	AOCPS	-----
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	X

VRHS	Virtual Hall select : 0 : Real Hall. (HALL U, HALL V, HALL W) 1 : Virtual Hall.
AOCPS	Analog OCP select : 0 : Digital OCP 1 : Analog OCP

19.8.3 MCONT3 SFR

MCONT3 Address = ACH Reset Value = 00000011B

Motor Control Register 3

	MPWMEN	-----	-----	ERS_MASK	-----	I_SHORT[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	X	W	X	R/W	R/W	R/W

MPWMEN [7]	MPWM timer run control : 0 : Stop 1 : Run
ERS_MASK [4]	PWM Mask(1~2 PWM cycles) Enable when Error Step Occur (Enable when SFR IMPMISC_KEY=0xa5): 0 : No Mask (Driving by Previous Step) 1 : PWM Mask 1~2 PWM cycles in the end of Error Step
I_SHORT[2:0] [2:0]	OCP SHORT level select : (OCPSIF) 000 : 0.15V 001 : 0.2V 010 : 0.25V 011 : 0.3V (default) 100 : 0.35V 101 : 0.4V 110 : 0.45V 111 : 0.5V

19.8.3 HALLDBT (Hall De-bounce Time Register) SFR

HALLDBT Address = 9CH Reset Value = 00001110B

Hall De-bounce Time Register

	-----	-----	HALLDBT[5:0]					
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

HALLDBT is use to filter the HALL signal.

De-bounce time = 1/3MHz X HALLDBT [5:0]

19.8.4 HALLSET (Hall Setting Register 1, 2, 3) SFR

HALLSET1 (SYNC) Address = 91H Reset Value = 01000101B

Hall Setting Register 1

	-----	HALLSET1_2[2:0]			-----	HALLSET1_1[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	X	R/W	R/W	R/W

[2] : HALL U status. [1] : HALL V status. [0] : HALL W status.

HALLSET2 (SYNC) Address = 92H Reset Value = 00100110B

Hall Setting Register 2

	-----	HALLSET2_2 [2:0]			-----	HALLSET2_1[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	X	R/W	R/W	R/W

[2] : HALL U status. [1] : HALL V status. [0] : HALL W status.

HALLSET3 (SYNC) Address= 93H Reset Value = 00010011B

Hall Setting Register 3

	-----	HALLSET3_2[2:0]			-----	HALLSET3_1[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	X	R/W	R/W	R/W

[2] : HALL U status. [1] : HALL V status. [0] : HALL W status.

19.8.5 HALLST (Hall Status Register) SFR

HALLST Address = 94H Reset Value = xxxxxxxxB

Hall Status Register

	-----	H_OLD[2:0]			-----	H_NEW[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	R	R	R	X	R	R	R

H_OLD[2:0]	Hall old status : [2] : HALL U status. [1] : HALL V status. [0] : HALL W status.
H_NEW[2:0]	Hall new status : [2] : HALL U status. [1] : HALL V status. [0] : HALL W status.

19.8.6 ROTORSPEED (Rotor Speed Count Register) SFR

ROTORSPEEDH Address = 97H Reset Value = 11111111B

Rotor Speed Count Register High

	ROTORSPEED[15:8]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

ROTORSPEEDL Address = 96H Reset Value = 11111111B

Rotor Speed Count Register Low

	ROTORSPEED[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

19.8.7 VRHALL (Virtual Hall Register) SFR

VRHALL Address = D9H Reset Value = 00000101B

Virtual Hall Register

	-----	-----	-----	-----	-----	VRH[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

VRH[2:0] Virtual Hall value.

VRH.2 is Virtual HALL U.

VRH.1 is Virtual HALL V.

VRH.0 is Virtual HALL W.

19.8.8 MPWM_CYC (Motor PWM Cycle Register) SFR

MPWM_CYC_H (SYNC) Address = A4H Reset Value = 00000000B

Motor PWM Cycle Register High

	-----	-----	-----	-----	-----	MPWM_CYC [10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

MPWM_CYC_L (SYNC) Address = A3H Reset Value = 00000010B

Motor PWM Cycle Register Low

	MPWM_CYC [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

19.8.9 MPWMDY (Motor PWM Duty Register) SFR

MPWMDYUH (SYNC) Address = A6H Reset Value = 00000111B

Motor PWM Duty Register U High (Phase U)

	-----	-----	-----	-----	-----	MPWMDYU[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

MPWMDYUL (SYNC) Address = A5H Reset Value = 11111111B

Motor PWM Duty Register U Low (Phase U)

	MPWMDYU[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MPWMDYVH (SYNC) Address = ABH Reset Value = 00000111B

Motor PWM Duty Register V High (Phase V)

	-----	-----	-----	-----	-----	MPWMDYV[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

MPWMDYVL (SYNC) Address = AAH Reset Value = 11111111B

Motor PWM Duty Register V Low (Phase V)

	MPWMDYV[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MPWMDYWH (SYNC) Address = AEH Reset Value = 00000111B

Motor PWM Duty Register W High (Phase W)

	-----	-----	-----	-----	-----	MPWMDYW[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

MPWMDYWL (SYNC) Address = ADH Reset Value = 11111111B

Motor PWM Duty Register W Low (Phase W)

	MPWMDYW[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

19.8.10 MIN_DUTY (Minimum Duty Limit Register) SFR

MIN_DUTY Address = BFH Reset Value = 00000000B

Minimum Duty Limit Register

	MIN_DUTY[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

19.8.11 MPWMDT (Motor PWM Dead-Time Register) SFR

MPWMDT (SYNC) Address = A7H Reset Value = 00000000B

Motor PWM Dead-Time Register

	MPWMDB[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

19.8.12 MPWMCONT1 (MPWM Control Register 1) SFR

MPWMCONT1 (SYNC) Address = B1H Reset Value = 00000000B

MPWM Control Register 1

	-----	-----	PWMW[1:0]		PWMV[1:0]		PWMU[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

PWMW Phase W High-side (W) output mode select :

00 : Force Low

01 : Force High

10 : Active High

11 : Active Low

PWMV Phase V High-side (V) output mode select :

00 : Force Low

01 : Force High

10 : Active High

11 : Active Low

PWMU Phase U High-side (U) output mode select :

00 : Force Low

01 : Force High

10 : Active High

11 : Active Low

19.8.13 MPWMCONT2 (MPWM Control Register 2) SFR

MPWMCONT2 (SYNC) Address = B2H Reset Value = 00000000B

MPWM Control Register 2

	-----	-----	PWMZ[1:0]		PWMY[1:0]		PWMX[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

PWMZ	Phase W Low-side (Z) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low
PWMY	Phase V Low-side (Y) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low
PWMX	Phase U Low-side (X) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low

19.8.14 MPWMINV (MPWM Inverse Selection Register) SFR

MPWMINV(SYNC) Address = B3H Reset Value = 00000000B

MPWM Inverse Selection Register

	-----	-----	ZINV	WINV	YINV	VINV	XINV	UINV
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

ZINV	Low-side PWM Z output inverse select : 0 : Non-inverse 1 : Inverse
WINV	High-side PWM W output inverse select : 0 : Non-inverse 1 : Inverse
YINV	Low-side PWM Y output inverse select : 0 : Non-inverse 1 : Inverse
VINV	High-side PWM V output inverse select : 0 : Non-inverse 1 : Inverse
XINV	Low-side PWM X output inverse select : 0 : Non-inverse 1 : Inverse
UINV	High-side PWM U output inverse select : 0 : Non-inverse 1 : Inverse

19.8.15 SVPWMAMP (SVPWM Amplitude Register) SFR

SVPWMAMPH(SYNC) Address = C4H Reset Value = 00000000B

SVPWM Amplitude Register High

	-----	-----	-----	-----	-----	SVPWMAMP[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

SVPWMAMPL(SYNC) Address = C3H Reset Value = 00000000B

SVPWM Amplitude Register Low

	SVPWMAMP[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

19.8.16 SVPWMAMPFT (SVPWM Amplitude Fine-Tune Register) SFR

SVPWMAMPFT Address = DAH Reset Value = 00000000B

SVPWM Amplitude Fine-Tune Register

	-----	-----	-----	-----	-----	SVPWMAMPFT[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

19.8.17 SVPWMANG (SVPWM Angular Register) SFR

SVPWMANGH(SYNC) Address = C2H Reset Value = 00000000B

SVPWM Angular Register High

	-----	-----	-----	-----	-----	-----	-----	SVPWMANG[8]
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	X	X	R/W

SVPWMANGL(SYNC) Address = C1H Reset Value = 00000000B

SVPWM Angular Register Low

	SVPWMANG[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

19.8.18 AS (Angle Shift Control Register) SFR

AS (SYNC) Address = 8FH Reset Value = 00000000B

Angle Shift Control Register

	AS_LS	-----	AS_VALUE[5:0]					
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	R/W	R/W	R/W	R/W	R/W	R/W

AS_LS Angle Shift Lag select:

0 : 0° ~59.0625° = 0~ 63(AS_VALUE)

1 : 0° ~ -59.0625° = 0~ -63(AS_VALUE)

19.8.19 Over Current Protect (OCP) SFR

OCPCONT Address = A1H Reset Value = 00000100B

OCP Control Register

	OCPST	OCPDBT[4:0]					OCPC	OCPMS
Bit	7	6	5	4	3	2	1	0
Type	R	R/W	R/W	R/W	R/W	R/W	W	R/W

OCPST	OCP Short status: 0 : No Over current Short 1 : Over current Short occur. Six PWM output is high-impedance.
OCPDBT[4:0]	PIN OCP input de-bounce time (default 41.67nS) 0~31 = 0~1.291uS (48MHz/2 fixed)
OCPC	OCP status clear bit : In User mode, user can write '1' to clear OCP status, the PWM will output at next PWM cycle.
OCPMS	OCP mode select : 0 : Auto mode 1: User mode

19.8.20 Analog Over Current Protect (AOCP) SFR

AOCPCONT Address = 9EH Reset Value = 00001111B

Analog OCP Control Register

Bit	7	6	5	4	3	2	1	0
	OCPLT	-----	-----	I_LIMIT[2:0]			-----	
Type	R	X	X	R/W	R/W	R/W	X	X

OCPLT	OCP Limit status 0 : No Over current Limit. 1 : Over current Limit occur.
I_LIMIT[2:0]	OCP LIMIT level select : (OCPLIF) 000 : 0.15V 001 : 0.2V 010 : 0.25V 011 : 0.3V (default) 100 : 0.35V 101 : 0.4V 110 : 0.45V 111 : 0.5V

19.8.21 IMPMISC_KEY (IMPROVE Miscellaneous Function Turn On Key) SFR

IMPMISC_KEY Address = 9FH Reset Value = 00000000B

Improve Miscellaneous Function Turn On Key Register

Bit	7	6	5	4	3	2	1	0
	IMPMISC_KEY[7:0]							
Type	W	W	W	W	W	W	W	W

Write down the **0xa5**, turn on the switch of miscellaneous function in SFR IMPMISC_FUN

19.8.22 IMPMISC_FUN (IMPROVE Miscellaneous Function Setting) SFR

IMPMISC_FUN Address = AFH Reset Value = 00010000B

Improve Miscellaneous Function Setting Register (when SFR IMPMISC_KEY = 0xa5)

	SMODE	CSHC	SIN_USER	MINDUTY_EN	UNIPOLAR	HLALM	HLSWP	UWSWP
Bit	7	6	5	4	3	2	1	0
Type	W	W	X	W	W	W	W	W

SMODE [7]	SVPWM Mode (when MCONT1[2] = 1) 0: Seven-segment SVPWM 1: Five-segment SVPWM
CSHC [6]	Change Step in Hall Change (6-Step) 0: Change Step in PWM Minimum 1: Change Step in PWM Minimum or Hall Change
SIN_USER [5]	Sine wave user mode 0: Sine Wave angle write by Auto 1: Sine Wave angle write by User (duty auto generate by MDE)
MINDUTY_EN [4]	Minimum Duty Limit enable (SFR 0xBF) 1: Enable Minimum Duty Limit
UNIPOLAR [3]	6-Step Control with Unipolar PWM Switching (PWM output mode select SFR must set active “High” or active “Low”) 1: Enable Unipolar PWM Switching in 6-Step Control
HLALM [2]	PWM High/Low Side Alignment: 0 : PWM_U, PWM_X, PWM_V, PWM_Y, PWM_W, PWM_Z 1 : PWM_U, PWM_V, PWM_W, PWM_X, PWM_Y, PWM_Z
HLSWP [1]	PWM High and Low Side Swap 0 : PWM_U, PWM_X, PWM_V, PWM_Y, PWM_W, PWM_Z 1 : PWM_X, PWM_U, PWM_Y, PWM_V, PWM_Z, PWM_W
UWSWP [0]	PWM_U/PWM_X and PWM_W/PWM_Z Swap 0 : PWM_U, PWM_X, PWM_V, PWM_Y, PWM_W, PWM_Z 1 : PWM_W, PWM_Z, PWM_V, PWM_Y, PWM_U, PWM_X

19.8.23 ONE_HALLSET (One Hall Setting) SFR

ONE_HALLSET Address = 95H Reset Value = 0000_0000B

One Hall Setting Register (when SFR IMPMISC_KEY = 0xa5)

	STA_ZONE_EN	3TO1_RUN	-----	-----	1HALL_ONLY	ZONE[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	W	W	X	X	W	W	W	W

STA_ZONE_EN	Hall U rising edge start zone setting enable (for 3-Hall Start and 1-Hall Rotation or One Hall solution using) 0 : Hall U rising edge start zone setting by hardware when 1-hall run 1 : Hall U rising edge start zone setting by software when 1-hall run
3TO1_RUN	3-Hall Start and 1-Hall Rotation enable 0 : 3-Hall Rotation or 1-Hall Start up and Rotation 1 : 3-Hall Start and 1-Hall Rotation
1HALL_ONLY	One Hall Startup and One Hall Rotation enable 0 : Disable One Hall Only 1 : Enable One Hall Only
ZONE	Hall U rising edge start ZONE **(when** STA_ZONE_EN **=1)** 000: Hall U rising edge start at ZONE0 (HALLSET1_1), start angle is 0 001: Hall U rising edge start at ZONE1 (HALLSET1_2), start angle is 64 010: Hall U rising edge start at ZONE2 (HALLSET2_1), start angle is 128 011: Hall U rising edge start at ZONE3 (HALLSET2_2), start angle is 192 100: Hall U rising edge start at ZONE4 (HALLSET3_1), start angle is 256 101: Hall U rising edge start at ZONE5 (HALLSET3_2), start angle is 320

19.8.24 FG_CTRL (Frequency Generator Control) SFR

FG_CTRL Address = C5H Reset Value = 0x00H

Frequency Generator Control Register

	FG_EN	FG10PT8P	-----	-----	FGOUT_SEL	FGPULSE_SEL		
Bit	7	6	5	4	3	2	1	0
Type	W	W	X	X	W	W		

FG_EN	FG output enable: 0 : Disable 1 : Enable		
FG10PT8P	10 poles FG Convert to 8 poles FG: 0 : Normal 1 : Enable		
FGOUT_SEL	FG output pin select: 0 : out to CH3 pin 1 : out to TX pin		
FGPULSE_SEL	FG pulse number selection:		
		FG10PT8P = 0	*FG10PT8P = 1*
	000 :	1 pulses/cycle	4 pulses/5-cycle
	001 :	2 pulses/cycle	8 pulses/5-cycle
	010 :	4 pulses/cycle	16 pulses/5-cycle
	011 :	5 pulses/cycle	20 pulses/5-cycle
	100 :	8 pulses/cycle	32 pulses/5-cycle
	101 :	12 pulses/cycle	48 pulses/5-cycle

19.9 SYNC

MDE behavior is synchronized with **MPWM**, many **MDE** SFRs have **shadow register** that is used to update these SFRs at the same time with **SYNC** register. Write **SYNC** any value will synchronization update these SFRs at the same time.

Table 19.9.1 SYNC

SYNC				Address = D7H		Reset Value = 00000000B	
MDE Sync Register							
	SYNC[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

Write only.

Shadow register: (need SYNC)

HALLSET1

HALLSET2

HALLSET3

AS

MPWM_CYC_H, MPWM_CYC_L

MPWMDYUH, MPWMDYUL

MPWMDYVH, MPWMDYVL

MPWMDYWH, MPWMDYWL

MPWMDT

MPWMINV

MPWMCONT1

MPWMCONT2

GPWMMAX

GPWMDY

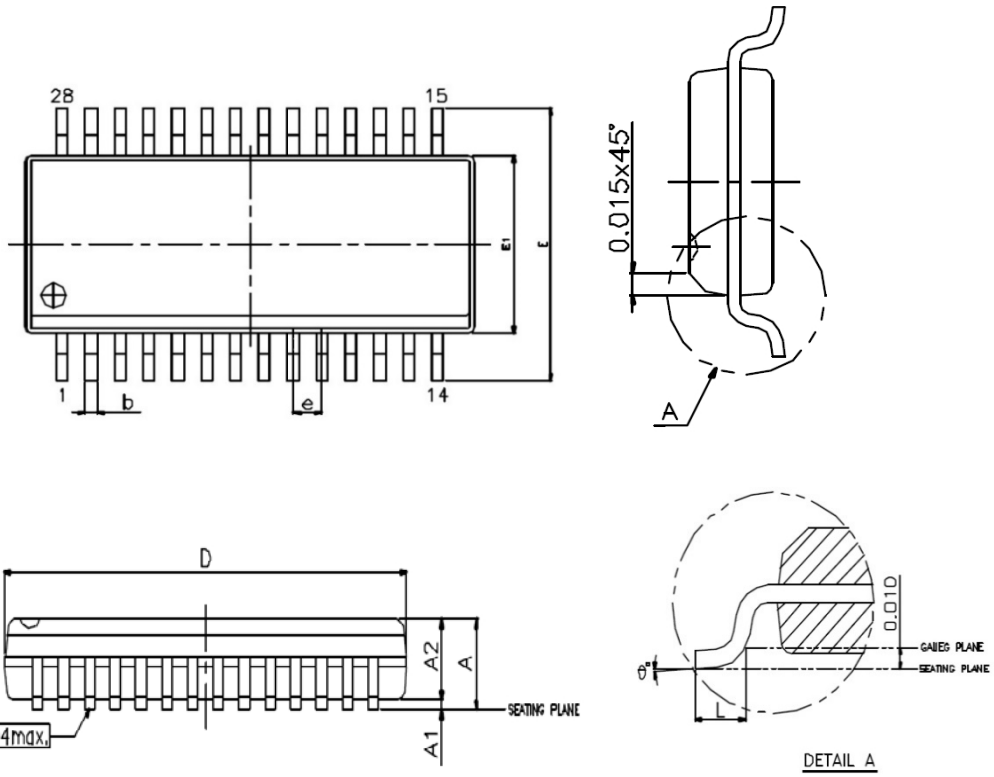
GPWMOCNT.GPMS, GPWMOCNT.GPCT, GPWMOCNT.GPCKS

SVPWMAMP

SVPWANG

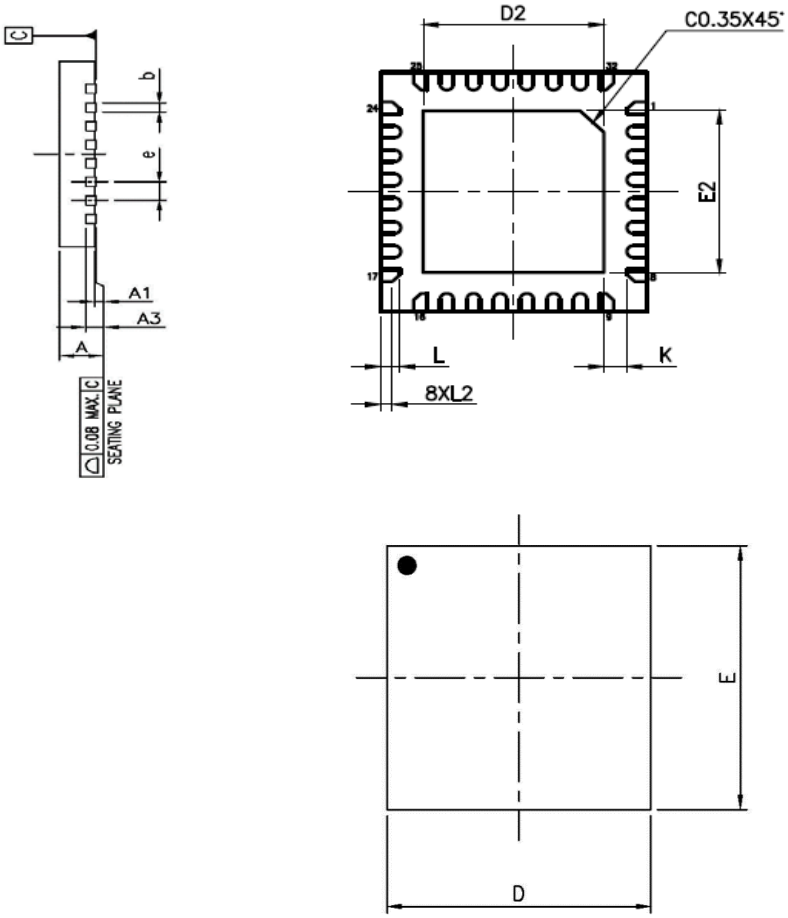
20. Package Information

20.1 SSOP-28 150 mil (AL28) Outline Dimensions



Unit	mm		inch	
Symbols	Min.	Max.	Min.	Max.
A	1.346	1.752	0.053	0.069
A1	0.101	0.254	0.004	0.010
A2	----	1.498	----	0.059
b	0.203	0.304	0.008	0.012
D	9.804	10.007	0.386	0.394
E1	3.810	3.987	0.150	0.157
e	0.635 BASIC		0.025 BASIC	
E	5.791	6.198	0.228	0.244
L	0.406	1.270	0.016	0.050
θ ◦	0	8	0˚	8˚

20.2 QFN-32 4x4x0.55 (AZ32) Outline Dimensions



Unit	mm			inch		
JEDEC	N/A			N/A		
PKG CODE	UQFN(W432)			UQFN(W432)		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.150 REF.			0.006 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	4.00 BSC			0.157 BSC		
E	4.00 BSC			0.157 BSC		
e	0.40 BSC			0.016 BSC		
L	0.25	0.30	0.35	0.010	0.012	0.014
L2	0.13	0.18	0.23	0.005	0.007	0.009

K	0.20	----	----	0.008	----	----
D2	----	----	2.75	----	----	0.108
E2	----	----	2.75	----	----	0.108

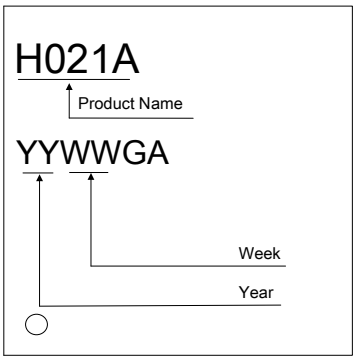
	LEAD FINISH		JEDEC CODE
PAD SIZE	Pure Tin	PPF	
122x12*MIL	V	X	N/A

21. Marking Distinguish

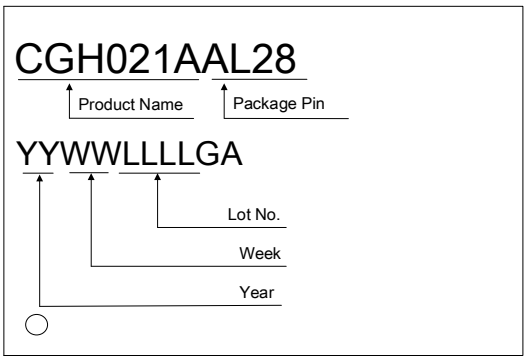
21.1 Standard Ink (w/o code)

Figure 21.1 Standard Ink (w/o code)

QFN4x4



SSOP28 150mil

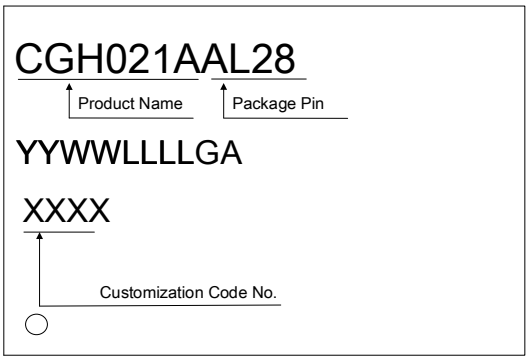


21.2 Customization Ink (with customization code)

Figure 21.2 Customization Ink (with customization code)

QFN4x4 (no customization code)

SSOP28 150mil



22. Ordering Information

22.1 Standard Product Name

Figure 22.1 Standard Product Name

CG H001A AL28

CG	H001A	AL28
CheerGoal	*Product Name*	*Package* *AL28 : SSOP-28* *AZ32 : QFN32-4x4*

22.2 Customization Product Name

- With customization code, produce by order.

Figure 22.2 Customization Product Name

CG H001A AL28 - XXXX

CG	H001A	AL28	XXXX
CheerGoal	*Product Name*	*Package* *AL28 : SSOP-28* *AZ32 : QFN32-4x4*	*Customization Code NO.*

23. Revision History

Table 21 Revision History

Update Date	Version	Modify content
2024/03/04	V0.0	1. Preliminary edition
2024/08/16	V0.1	2. The links of contents updated