



MG65P701A

Datasheet

8-Bit Micro-Controller with
Lithium battery charge function

Version 2.00

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1 Features

- Single Chip 8-bit CPU
- Memory
 - Program OTP ROM : 8K Bytes
 - Data RAM : 128 Bytes
- Operating voltage: 2.0V to 5.5V
- 16-bit Programmable GPIO
 - Input/output pins P0[7:0]
 - Input/output pins P1[7:0]
 - Two PWM output pins (PWM1, PWM0 Share P1.7, P1.6)
- Build-in a watchdog timer
- Build-in an 8-channel 12-bit ADC
- Build-in a over current protection circuit
- Build-in a over voltage protection circuit
- Build-in RTC (Real time clock)
- One re-loadable 8-bit timer
- One re-loadable 10-bit timer
- One re-loadable 16-bit timer
- One 10-bit PWM
- One 16-bit PWM
- HALT mode and STOP mode for power saving
- Build-in three oscillation circuits:
 - 32MHz ($\pm 2\%$) internal oscillator
 - 32KHz internal oscillator
 - 32KHz crystal oscillator
 - Dual clock operation
 - Oscillator pad shares with P1.2~ P1.3 select by option register
- Build-in low voltage detectors (typical voltage: below 2.4V or 2.7V select by SFR) and low voltage reset (typical voltage: below 2.0V)

1.1 Application Field

Power management
Power Bank
Transducer / sensor

2 General Description

MG65P701A integrates an 8-bit CPU core, SRAM and system control circuits by a CMOS silicon gate technology. The ROM can store data table and program.

16 I/O, 8-channel ADC and voltage comparator very suitable for Lithium battery power bank.

3 Pin Configurations

3.1 SOP16

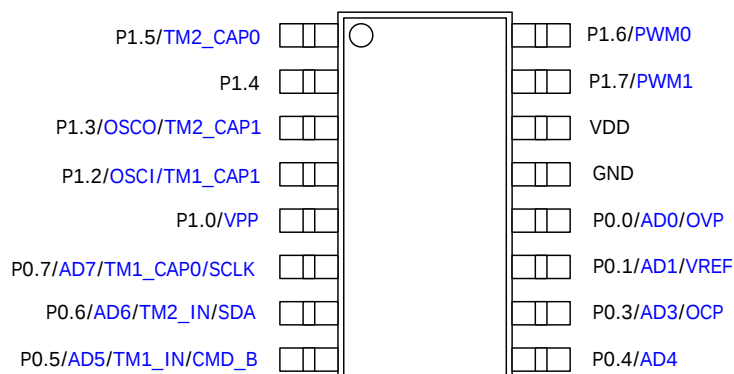


Figure 3-1 package SOP16

Pin	Name	Type	Description
1	P1.5	B	Programmable I/O port, CMOS output, input with pull high and interrupt function.
2	P1.4	B	Programmable I/O port, CMOS output, input with pull high and interrupt function.
3	P1.3 / OSCO	B	Programmable I/O port, CMOS output, input with pull high and interrupt function and shares with 32K OSC pad.
4	P1.2 / OSCI	B	Programmable I/O port, CMOS output, input with pull high and interrupt function and shares with 32K OSC pad.
5	P1.0 / VPP	B	Programmable I/O port, CMOS output, input with pull high and interrupt function. The P1.0 shares OTP interface VPP pin.
6	P0.7 / AD7 / SCLK	B	Programmable I/O port, CMOS output, input with pull high and interrupt function. The P0.7 shares A/D channel 7 input and OTP interface SCLK pin.
7	P0.6 / AD6 / SDA	B	Programmable I/O port, CMOS output, input with pull high and interrupt function. The P0.6 shares A/D channel 6 input and OTP interface SDA pin.
8	P0.5 / AD5 / CMD_B	B	Programmable I/O port, CMOS output, input with pull high and interrupt function. The P0.5 shares A/D channel 5 input and OTP interface CMD_B pin.
9	P0.4 / AD4	B	Programmable I/O port, CMOS output, input with pull high and interrupt function. The P0.4 shares A/D channel 4 input pin.
10	P0.3 / AD3 / OCF	B	Programmable I/O port, CMOS output, input with pull high and interrupt function. The P0.3 shares A/D channel 3 input and OCF pin.
11	P0.1 / AD1 / VREF	B	Programmable I/O port, CMOS output, input with pull high and interrupt function. The P0.1 shares A/D channel 1 input and ADC external reference voltage input pin.
12	P0.0 / AD0 / OVP	B	Programmable I/O port, CMOS output, input with pull high and interrupt function. The P0.0 shares A/D channel 0 input and OVP pin.
13	GND	G	Ground pin
14	VDD	P	Positive power pins
15	P1.7 / PWM1	B	Programmable I/O port, CMOS output, input with pull high and interrupt function and shares with PWM1 output.
15	P1.6 / PWM0	B	Programmable I/O port, CMOS output, input with pull high and interrupt function and shares with PWM0 output.

Note: In the "Type" field,
 "I" means input only.
 "O" means output only.
 "B" means bi-direction.
 "P" means Power, "G" means Ground.

4 Block Diagram

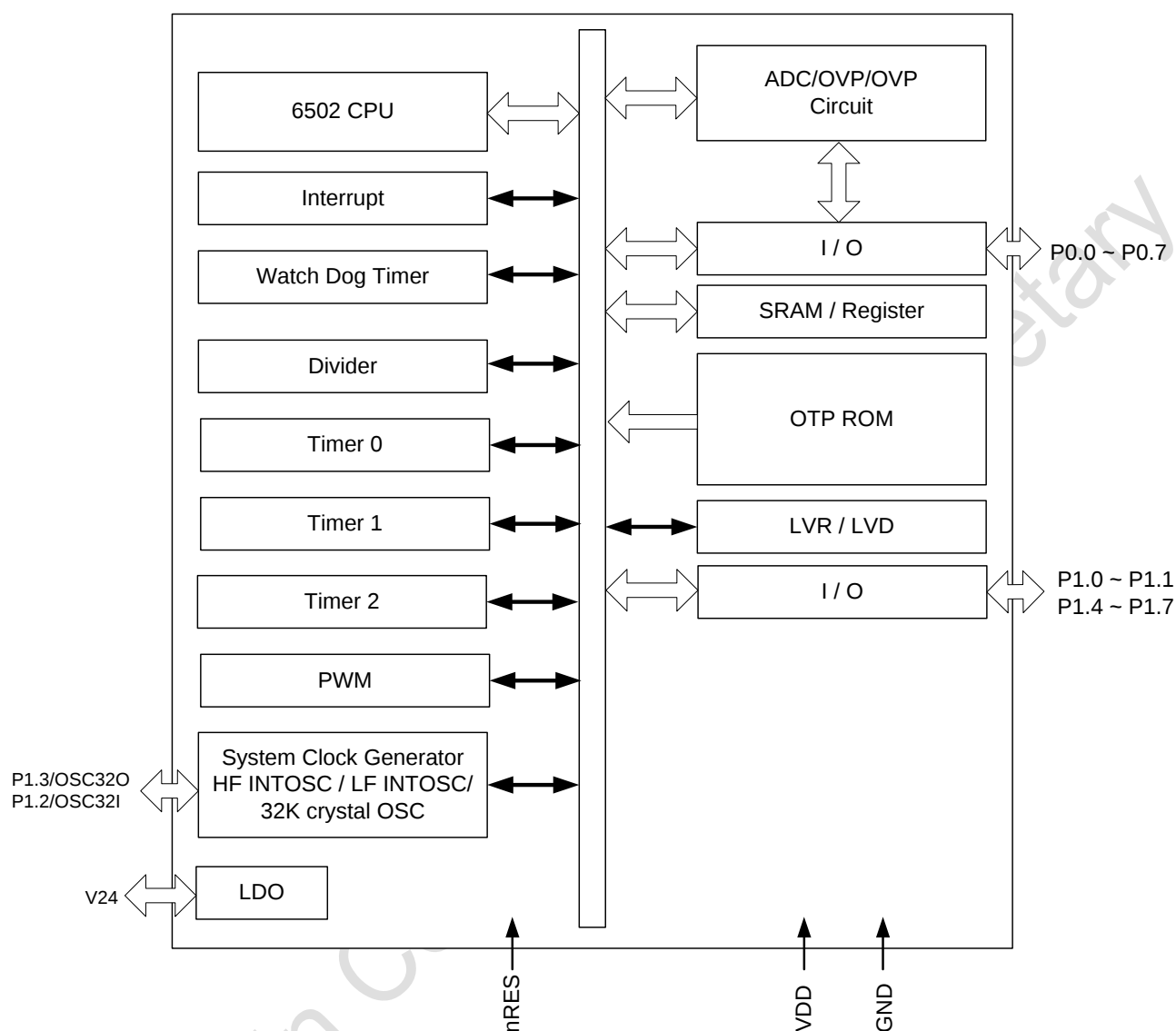


Figure 4-1 Block Diagram

5 Function Description

5.1 Registers

PCH	1	A
		Y
		X
		P
		PCL
		S

5.2 Accumulator

The accumulator is a general-purpose 8-bit register, which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of two data words used in these operations.

5.3 Index Register(X,Y)

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction, which specifies indexed addressing, the CPU fetches the OP Code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-index of index address is possible.

5.4 Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both the program and the CPU.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N	V	1	B	D	I	Z	C

N: Signed flag, 1 = negative, 0 = positive

V: Overflow flag, 1 = true, 0 = false

B: BRK interrupt command, 1 = BRK, 0 = IRQB

D: Decimal mode, 1 = true, 0 = false

I: IRQB disable flag, 1 = disable, 0 = enable

Z: Zero flag, 1 = true, 0 = false

C: Carry flag, 1 = true, 0 = false

5.5 Program Counter(PC)

The 16-bit program counter register provides the addresses, which step the micro-controller through sequential program instructions. Each time the micro-controller fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

5.6 Stack Point(S)

The stack pointer is an 8-bit register, which is used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the micro-controller to perform stack manipulations under direction of either the program or interrupts (/NMI or /IRQ). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer is initialized by the user's firmware.

6 Memory Organization

There are 128 bytes SRAM, located in address 0000H to 007FH, in the MG65P701A. They could be used as either working RAM or stacks according to application programs. For the purpose above, the location 0000H to 007FH and 0100H to 017FH are overlaps. In other words, accessing any locations inside the range 0000H to 007FH is equivalent to access the corresponding ones in the range 0100 to 017FH. All special function registers, SFRs, are located at the region 00B0H to 00FFH. Such an arrangement could benefit from the faster access time of zero-page.

There are 8K bytes program / data ROM in MG65P701A. The ROM address from E000H to FFFFH can store program and data. The address mapping of MG65P701A is shown as below

MG65P701A Memory Map

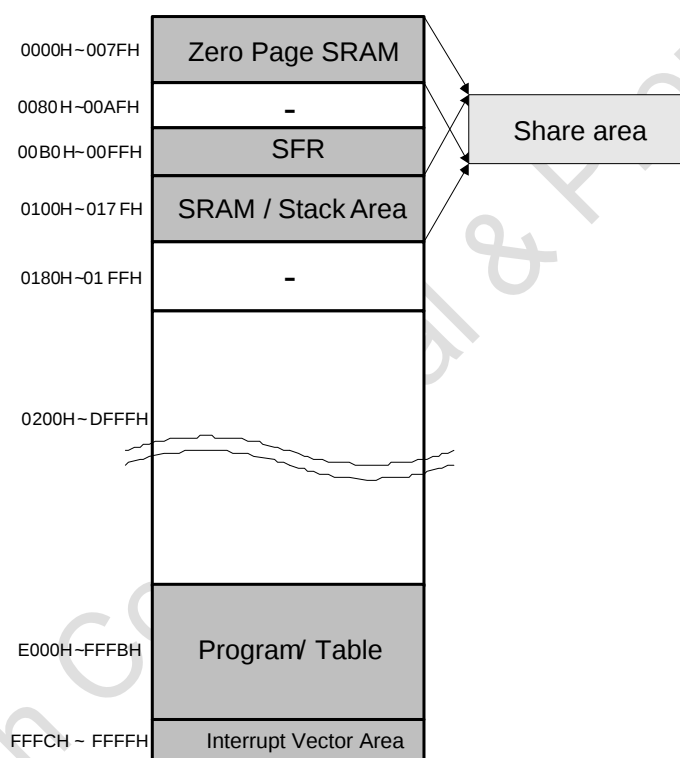


Figure 6-1 Memory Map

6.1 SFR Mapping

The address 00B0H to 00FFH is reserved for special function registers (SFR). The SFR is used to control or store the status of I/O, timers, system clock and other peripheral.

※ All SFRs are not supported by bit-manipulation instructions.

Table 6-1 SFR Table

SFR (special function register): 00B0H~00FFH

Address	Content	Default
00B0	RESOK	XXXX----
00B1		-----
00B2	IRQ_EN0	00000000
00B3	IRQ_EN1	-----000
00B4	IRQ_ST0/IRQ_CLR0	00000000
00B5	IRQ_ST1/IRQ_CLR1	-----000
00B6		-----
00B7	SYS_ST	0-----X
00B8		-----
00B9	DIV_SEL/DIV_ST	-----00
00BA	SCK_SEL	0-000-0
00BB		-----
00BC	PWR_CR	-0-0-000
00BD		-----
00BE	RTC	--000000
00BF		-----

Address	Content	Default	Address	Content	Default
00C0		-----	00D0		-----
00C1		-----	00D1	TM0	11111111
00C2		-----	00D2	TM0_CTL	00---000
00C3	CPCR0	00000000	00D3		-----
00C4	CPCR1	0000-000	00D4	TM1L	11111111
00C5		-----	00D5	TM1H	-----11
00C6	OVPLV	00000000	00D6	TM1_CAPL	-----11
00C7	OCPLV	00000000	00D7	TM1_CAPH	11111111
00C8		-----	00D8	TM1_CTL	00000000
00C9	DT_SEL	-0000000	00D9		-----
00CA	PB_SEL	----0000	00DA	TM2L	11111111
00CB		-----	00DB	TM2H	11111111
00CC		-----	00DC	TM2_CAPL / PWMR_L	11111111
00CD		-----	00DD	TM2_CAPH / PWMR_H	11111111
00CE		-----	00DE	TM2_CTL	00000000
00CF		-----	00DF		-----

Address	Content	Default	Address	Content	Default
00E0	PWMR0	00000000	00F0		-----
00E1	PWMR1	-----10	00F1		-----
00E2	PWM_CTL / PWM_ST	00001111	00F2		-----
00E3		-----	00F3		-----
00E4	P0port / P0obuf	00000000/ XXXXXXXX	00F4		-----
00E5	P0dir	00000000	00F5	ADC_CTL0/ADC_STS	00000000
00E6	P0plh	11111111	00F6	ADC_CTL1	----0000
00E7	P0an	00000000	00F7	ADB_L	0000----
00E8	P0es	00000000	00F8	ADB_H	00000000
00E9		-----	00F9		-----
00EA	P1port / p1obuf	00000000/ XXXXXXXX	00FA	CWPR	XXXXXXXX

00EB	P1dir	00000000	00FB	IAP_PR	XXXXXXXX
00EC	P1plh	00111111	00FC		-----
00ED		-----	00FD		-----
00EE	POsel	--000000	00FE		-----
00EF		-----	00FF		-----

6.2 Condition Write Protect Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FAH	CWPR	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	-	√

Condition Write Protect flag register (CWPR) is used to protect [SYS_ST.7 \(WDT\)](#), [PWR_CR.1 \(CKC0\)](#), [PWR_CR.2 \(CKC1\)](#), [PWR_CR.0 \(HALT\)](#) and [SCK_SEL](#). If want to change these SFR, it must write "78H" to CWPR first.

PT7~PT0: Write Protect Pattern. In MG65P701A write protect pattern is "78H"

Note:

1. When CWPR is written by firmware, it would be automatically cleared by hardware after the "next write action" of firmware.

※Bit-manipulation instructions are not available on this register.

7 Interrupt

There are thirteen kinds interrupt source is provided in MG65P701A. The flag IRQ_EN and IRQ_ST are used to control the interrupts. When flag IRQ_ST is set to '1' by hardware and the corresponding bits of flag IRQ_EN has been set by software, an interrupt is generated. When an interrupt occurs, all of the interrupts are inhibited until the CLI or STA IRQ_EN, # I instruction is invoked. Executing the SEI instruction can also disable the interrupts.

Table 7-1 Interrupt Vector Table

Vector Address	Item	Flag	Properties	Memo
FFFEH, FFFFH	P0 IRQ	P0evt	Ext.	P0.0 ~ P0.7 interrupt
	P1 IRQ	P1evt	Ext.	P1.0 ~ P1.7 interrupt
	TM0 IRQ	TM0evt	Int.	TM0 underflow interrupt
	TM1 IRQ	TM1evt	Int.	TM1 underflow interrupt
	TM2 IRQ	TM2evt	Int.	TM2 underflow interrupt
	DIV	DIVevt	Int.	Divider carry out interrupt
	RTC	RTCEvt	Int.	Real time clock interrupt
	OCPH	OCHPEvt	Ext.	Lithium battery over current event (Rising edge)
	OVPH	OVPHEvt	Ext.	Lithium battery over voltage event (Rising edge)
	OCPL	OCLPEvt	Ext.	Lithium battery over current event (Falling edge)
	OVPL	OVPLEvt	Ext.	Lithium battery over voltage event (Falling edge)
	Ext. protect signal	EXT_PREvt	Ext.	External Lithium battery protect signal
	ADC	ADCEvt	Int.	ADC conversion is complete
FFFCH, FFFDH	RESB	None	Ext.	External reset signal
	WDT	SYS_ST.7	Int.	Watch dog timer reset
	LVR	None	Int.	Low voltage reset

7.1 Interrupt Register

7.1.1 IRQ enable register 0 & IRQ enable register 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00B2H	IRQ_EN0	RTC	ADC	DIV	TM2	TM1	TM0	P1	P0	-	√
00B3H	IRQ_EN1	-	-	-	EXT_PR	OCPH	OCPL	OVPH	OVPL	-	√

Program can enable or disable the ability of triggering IRQ through this register.

0: Disable (default "0" at initialization)

1: Enable

P0: Rising or falling edge occurs at P0 interrupt mode (Setup by P0ES)

P1: Falling edge occurs at P1 input mode

TM0: Timer0 underflow

TM1: Timer1 underflow

TM2: Timer2 underflow

DIV: Divider selected interrupt frequency occurred

ADC: The ADC conversion data is complete

RTC: RTC 0.5S interrupt

OVPL: Lithium battery over voltage interrupt (Falling edge)

OVPH: Lithium battery over voltage interrupt (Rising edge)

OCPL: Lithium battery over current interrupt (Falling edge)

OCPH: Lithium battery over current interrupt (Rising edge)

EXT_PR: External Lithium battery protect signal

7.1.2 IRQ status flag 0 & IRQ status flag 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00B4H	IRQ_ST0	RTCEvt	ADCEvt	DIVevt	TM2evt	TM1evt	TM0evt	P1evt	P0evt	√	-
00B5H	IRQ_ST1	-	-	-	EXT_PRev	OCPhEv	OCPLev	OVPhEv	OVPLev	√	-

When IRQ occurs, program can read this register to know which source triggering IRQ. If the interrupt triggering is enabled and the interrupt event is accepted, the correspond IRQ status flag should be cleared by program after the interrupt vector is loaded into program counter.

7.1.3 IRQ clear flag 0 & IRQ clear flag 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00B4H	IRQ_CLR0	RTC	ADC	DIV	TM2	TM1	TM0	P1	P0	-	√
00B5H	IRQ_CLR1	-	-	-	EXT_PR	OCPL	OCPL	OVPL	OVPL	-	√

Program can clear the interrupt event by writing '1' into the corresponding bit.

7.1.4 System status flag

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00B7H	SYS_ST	WDT	-	-	-	-	-	-	LVD	√	√

WDT: WDT reset flag. (Clear by POR, LVR and external reset)

1: WDT reset occurs.

0: This bit is set by hardware and clears by writing '1'. (This register is protected by CWPR)

LVD: Low voltage detected. (Clear by WDT, POR, LVR and external reset)

1: VDD is under 2.4V or 2.7V.

0: This bit is set by hardware and clears by writing '1'.

7.2 Interrupt System

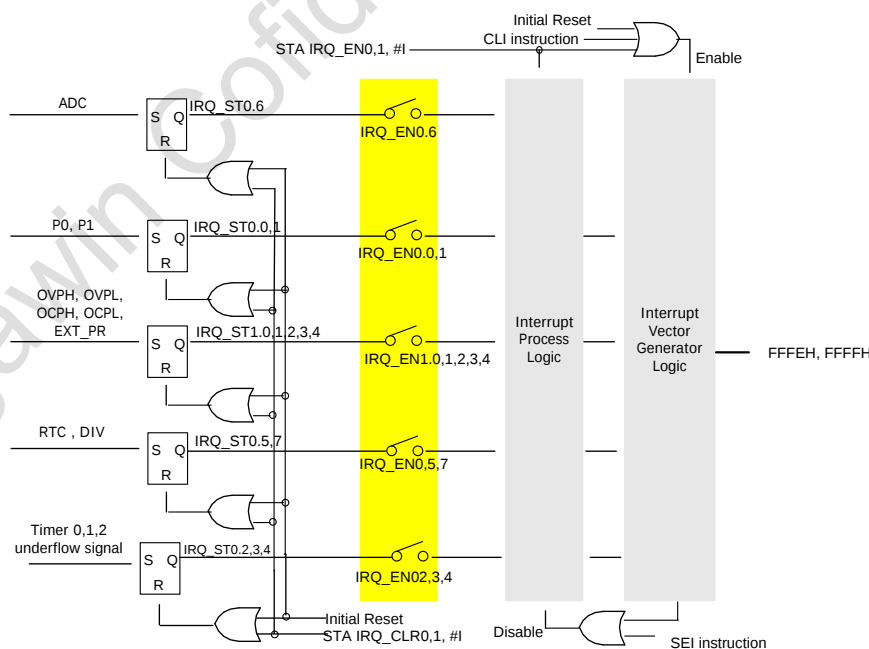


Figure 7-1 Interrupt System Diagram

8 Reset

MG65P701A provides 5 kind reset source (External reset, LVR, POR, WDT and RESET OK). The Chip reset Circuit shown below:

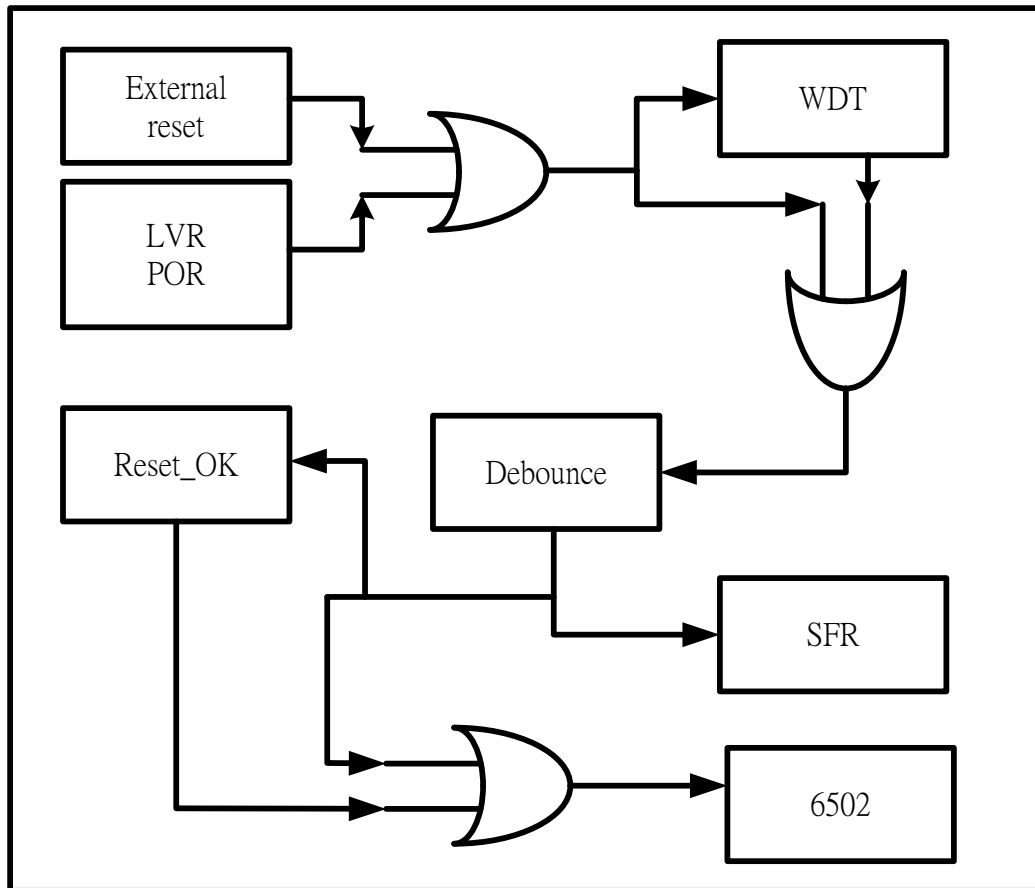


Figure 8-1 System Reset Diagram

8.1 Low Voltage Reset(LVR)

The MG65P701A provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V ~ VLVR, such as changing a battery, the LVR will automatically reset the device internally.

The LVR includes the following specifications

1. The low voltage (0.9V~VLVR) has to remain in their original state to exceed 1ms. If the low voltage state does not exceed 1ms, the LVR will ignore it and do not perform a reset function.
2. In the LVR mode, the SRAM is held. The port1 and port2 become tri-status. The LCD driver loads default value.

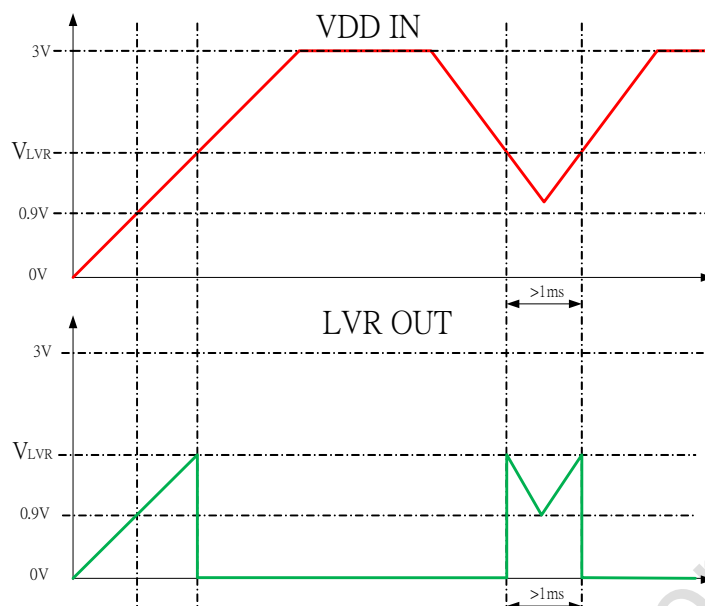


Figure 8-2 Low voltage reset hold time

8.2 Watchdog Timer(WDT)

(The example is base on 32.768 KHz, The SCK_SEL.Bit4 = 0)

Name		Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
WDT	-	1Hz	2Hz	4Hz	8Hz	16Hz	32Hz	64Hz	-	-

The watchdog timer time-out period is obtained by the equation: $(F_{MOSC} / 256) / 128$ or $(F_{MOSC} / 256) / 128$ select by SCK_SEL.Bit4 (CKS4).

Before watchdog timer time-out occurs, the program must clear the 7-bit WDT timer by writing 1 to STS_ST.7. WDT overflow will cause system reset and set SYS_ST.7 to high.

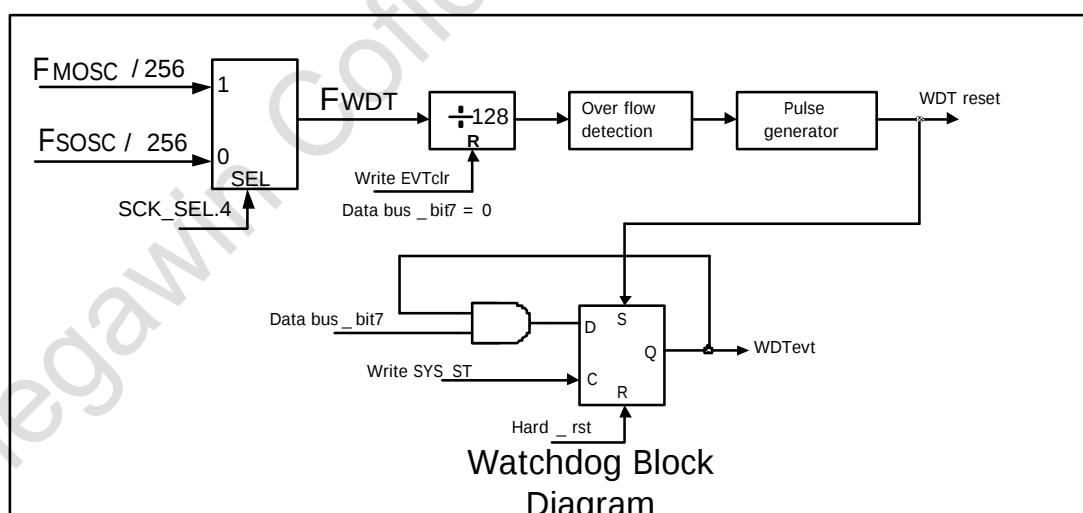


Figure 8-2 Watch Dog Diagram

8.3 Reset OK

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00B0H	RESOK	RK7	RK6	RK5	RK4	-	-	-	-	-	√

RESOK (Reset OK): If the device reset OK and work well, **must** write #90 into this register.

For example:

```

Program_start:      LDA    #10010000b
                   STA    $B0

```

8.4 Programming Notice

The status after different reset condition is listed below:

	Power on reset	CPU /RES pin reset
SRAM Data	Unknown	Unchanged
CPU Register	Unknown	Unknown
Special Function Register	Default value	Default value

9 Power Control Register

9.1 Power Saving Control

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00BCH	PWR_CR	-	IO_RES	-	LVD_SEL	-	CKC1	CKC0	HALT	-	√

IO_RES: IO reset selector.

0: IO status is reset by WDT, LVR and POR, EXT_RESET (Default).

1: IO status is reset by LVR, EXT_RESET and POR.

LVD_SEL: LVD voltage select

0: The LVD voltage is 2.4V

1: The LVD voltage is 2.7V

※ CKC1, CKC0 and HALT are protected by CWPR

CKC1	CKC0	System clock control
0	0	F _{MOSC} enable, F _{SOSC} enable (Dual mode)
0	1	F _{MOSC} enable, F _{SOSC} disable (Single mode)
1	0	F _{MOSC} disable, F _{SOSC} enable (Slow mode)
1	1	F _{MOSC} disable, F _{SOSC} disable (Stop mode)

HALT: F_{CPU} off-line control bit. 1: F_{CPU} off-line, 0: F_{CPU} on-line

Program can switch the normal operation mode to the power-saving mode for saving power consumption through this register. There are three power saving modes in this system.

Slow mode: (PWR_CR.CKC1 = 1, PWR_CR.CKC0 = 0)

The main uC clock (F_{MOSC}) stops oscillating. Only very low power is needed for uC to keep running.

Stop mode: (PWR_CR.CKC1 = 1, PWR_CR.CKC0 = 1)

Both system clocks stop oscillating. The uC can be awakened from stop mode by 4-ways: port 0 falling edge, port0 rising edge, port 1 falling, hardware reset, or power-on reset. When the stop mode is released, **oscillator will be enabled again**.

If uC clock source is F_{SOSC} and system into STOP mode (set PWR_CR[2:1] = 11). The F_{SOSC} will be enabled and F_{MOSC} still keep same status, when uC waken up by port0 or port1.

Halt mode: (PWR_CR.HALT = 1)

The F_{CPU} clock in off-line status. The oscillator(s) still keep same status. The uC can be awakened from halt mode by 3-ways: the interrupt events, hardware reset, or power-on reset.

10 System Clock Register

10.1 Clock Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00BAH	SCK_SEL	CKS7	-	-	CKS4	CKS3	CKS2	-	CKS0	-	√

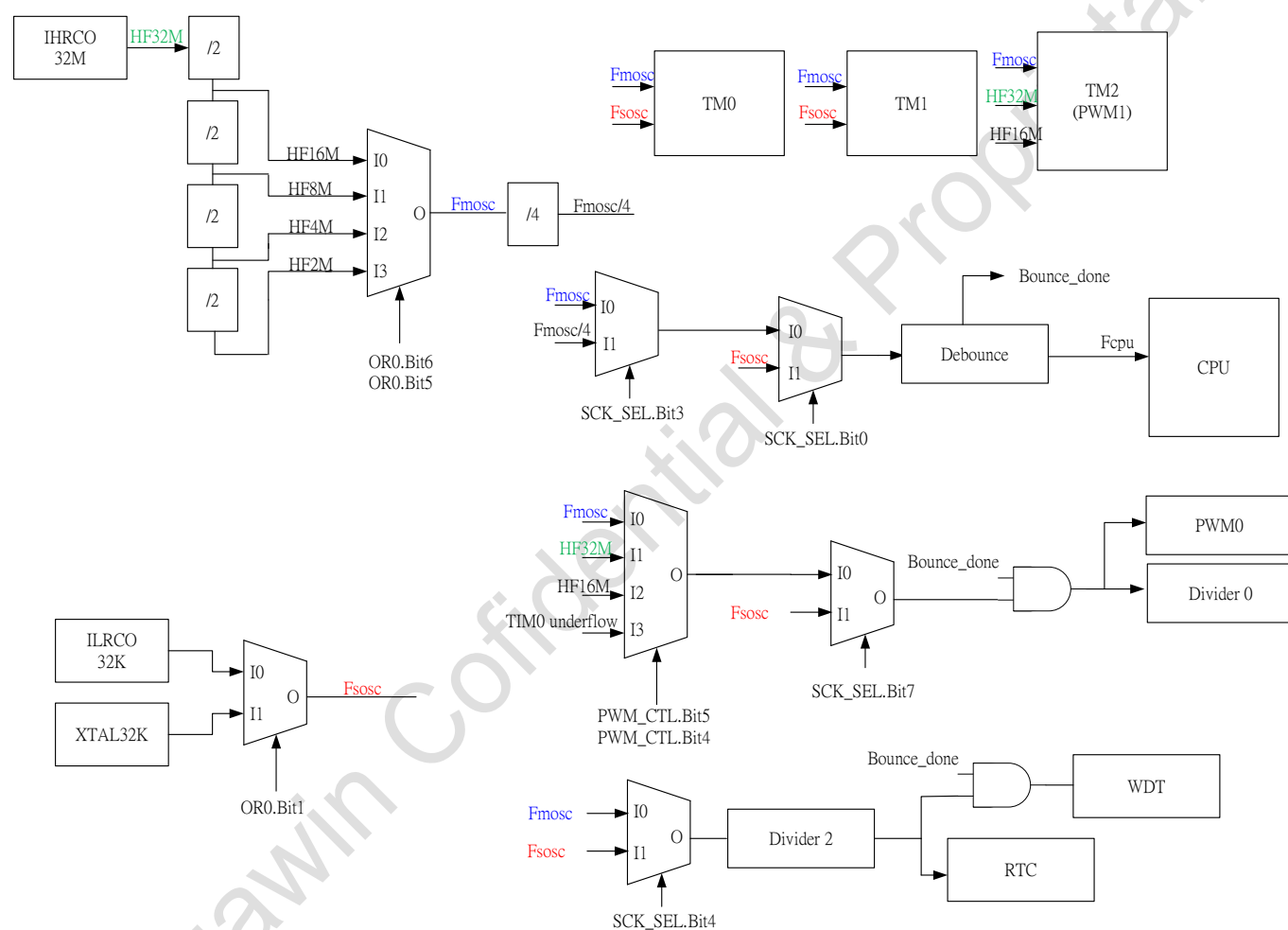
CKS0: F_{CPU} clock source select. 0: F_{MOSC} , 1: F_{SOSC}

CKS2: De-bounce (awakened from stop mode) time selector. 0: $F_{CPU}/16384$, 1: $F_{CPU}/256$

CKS3: F_{CPU} clock source select. 0: $F_{MOSC}/4$, 1: F_{MOSC}

CKS4: Select the input clock source of divider2 (F_{RTC} and F_{WDT} clock). 0: F_{SOSC} 1: F_{MOSC}

CKS7: Select the input clock source of divider0 (PWM clock). 0: F_{MOSC} , HF32M, HF16M or Tim0 underflow 1: F_{SOSC}



11 RTC Divider

The MG65P701A have an 8 bit divider and 4 kinds interrupt select to use. The divider clock source is F_{MOSC} or F_{SOSC} Divider can be reset to 00h by POR and LVR.

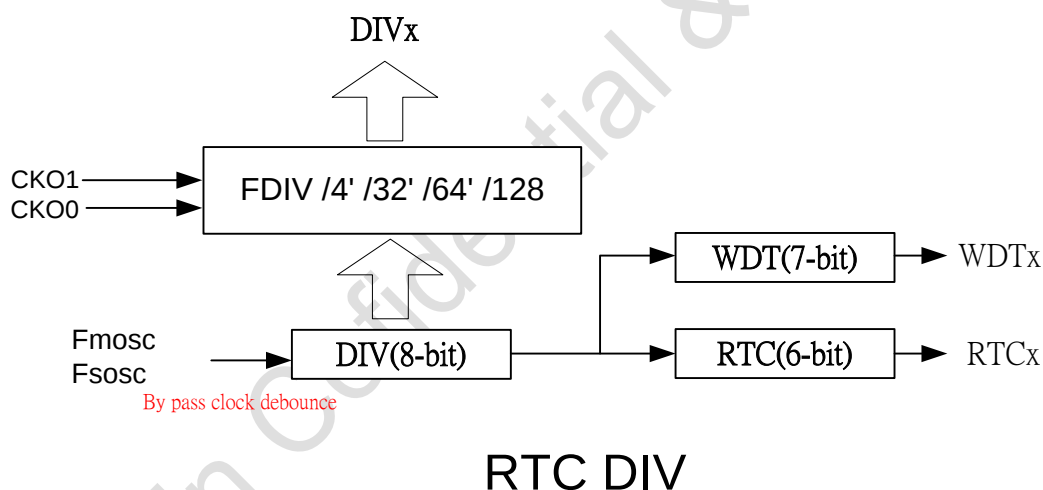
11.1 RTC Divider Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00B9H	DIV_ST	FDIV/ 256	FDIV/ 128	FDIV/ 64	FDIV/ 32	FDIV/ 16	FDIV/ 8	FDIV/ 4	FDIV/ 2	√	-
00B9H	DIV_SEL			-	-	-		CKO1	CKO0	-	√

CKO1, CKO0: Select DIV interrupt frequency

For example: (Fdiv is 32768Hz)

CKO1	CKO0	Selected DIV frequency (FDIV= F_{sosc})	
0	0	FDIV / 4	(8192 Hz)
0	1	FDIV / 32	(1024 Hz)
1	0	FDIV / 64	(512 Hz)
1	1	FDIV / 128	(256 Hz)



12 Real Time Clock

12.1 RTC Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00BEH	RTC	-	-	S5	S4	S3	S2	S1	S0	√	√

The RTC part contains 6 bit registers with an auto-incrementing register, an on-chip 32.768 kHz oscillator with an integrated capacitor, a frequency divider which provides the source clock for the Real-Time Clock (RTC).

Program can enable or disable the ability of triggering RTC interrupt through IRQ_EN.7 register, and read the IRQ_ST0.7 to know the RTC triggering interrupt. The RTC register and IRQ_ST0.7 can be reset by POR, LVR. Program can clear the RTC interrupt event by writing '1' into the IRQ_CLR0.7.

(The example frequency is $F_s = 32.768$ KHz)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00BEH	RTC	-	-	2Hz	4Hz	8Hz	16Hz	32Hz	64Hz	√	√

13 Timer

13.1 Timer0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D1H	TM0	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00D2H	TM0_CTL	STC	RL/S	-	-	-	TCS0	TKI1	TKI0		√

Timer 0 is an 8-bit down-count counter.

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock

RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TCS0: select the input clock source of timer0. 0: F_{MOSC} , 1: F_{SOSC}

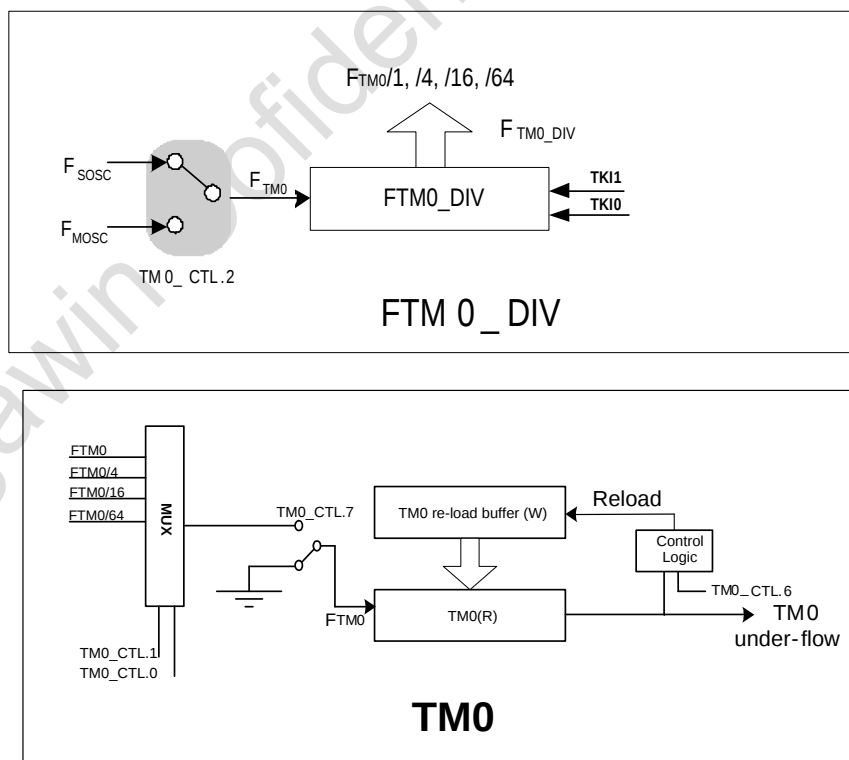
TKI1	TKI0	Selected TM0 input frequency (F_{TM0_DIV})
0	0	$F_{TM0} / 1$
0	1	$F_{TM0} / 4$
1	0	$F_{TM0} / 16$
1	1	$F_{TM0} / 64$

F_{TM0_UV} , can be calculated with the equation:

$F_{TM0_UV} = F_{TM0} / (TM0+1)$, where the F_{TM0} is the timer input frequency set by TKI1 and TKI0.

For example: (if $F_{TM0} = 2.000\text{MHz}$, TKI1=TKI0=0)

TM0	Frequency
00H	Reserved
01H	1.000MHz
02H	667kHz
...	...
FFH	7.84kHz



13.2 Timer1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00D5H	TM1H	-	-	-	-	-	-	T9	T8	√	√
00D4H	TM1L	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00D7H	TM1_CAPH							C9	C8	√	-
00D6H	TM1_CAPL	C7	C6	C5	C4	C3	C2	C1	T0	√	-
00D8H	TM1_CTL	STC	RL/S	TKES	CPS	CTKS	TCS1	TKI1	TKI0	-	√

Timer 1 is a 10-bit down-count counter.

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock

RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TKES: Event or series input clock-in trigger edge selector. 0: rising edge, 1: falling edge

CPS: Capture TM1 Counting Value trigger source select. 0: P0.7, 1: P1.2.

CTKS: Capture source trigger edge selector; 0: rising edge, 1: falling edge

TCS1: select the input clock source of timer1. 0: F_{MOSC} , 1: F_{SOSC}

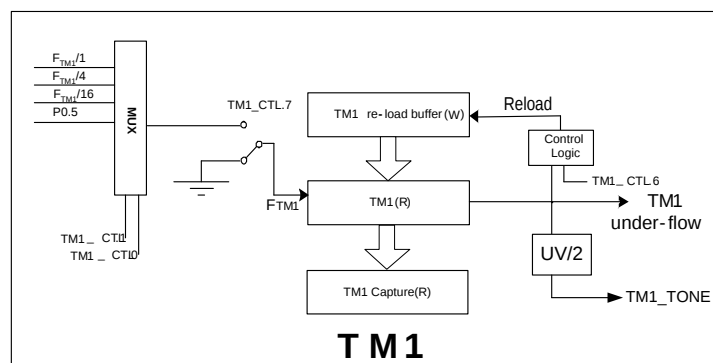
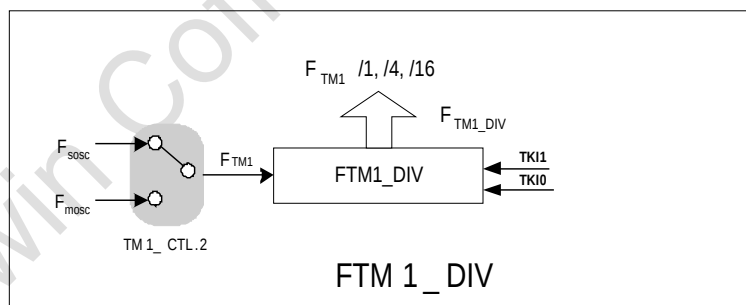
TKI1	TKI0	Selected TM1 input frequency (F_{TM1_DIV})
0	0	$F_{TM1} / 1$
0	1	$F_{TM1} / 4$
1	0	$F_{TM1} / 16$
1	1	P0.5

F_{TM1_UV} , can be calculated with the equation:

$F_{TM1_UV} = F_{TM1} / (TM1+1)$, where the F_{TM1} is the timer input frequency set by TKI1 and TKI0.

For example: (if $F_{TM1} = 2.000\text{MHz}$, $TKI1=TKI0=0$)

TM1	Frequency
000H	Reserved
001H	1.000MHz
002H	667kHz
...	...
0FFH	7.84kHz



13.3 Timer2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00DBH	TM2H	T15	T14	T13	T12	T11	T10	T9	T8	√	√
00DAH	TM2L	T7	T6	T5	T4	T3	T2	T1	T0	√	√
00DDH	TM2_CAP_H PWMR_H	C15	C14	C13	C12	C11	C10	C9	T8	√	√
00DCH	TM2_CAPL PWMR_L	C7	C6	C5	C4	C3	C2	C1	T0	√	√
00DEH	TM2_CTL	STC	RL/S	TKES	CPS	CTKS	ENCP	TKI1	TKI0		√

※ Bit-manipulation instructions are not available on this register.

Timer 2 is a 16-bit down-count counter.

STC: Start/Stop counting. 1: start and pre-load the value to counter, 0: stop timer clock

RL/S: Auto-reload disable/enable. 1: disable auto-reload, 0: enable auto-reload

TKES: Event or series input clock-in trigger edge selector. 0: rising edge, 1: falling edge

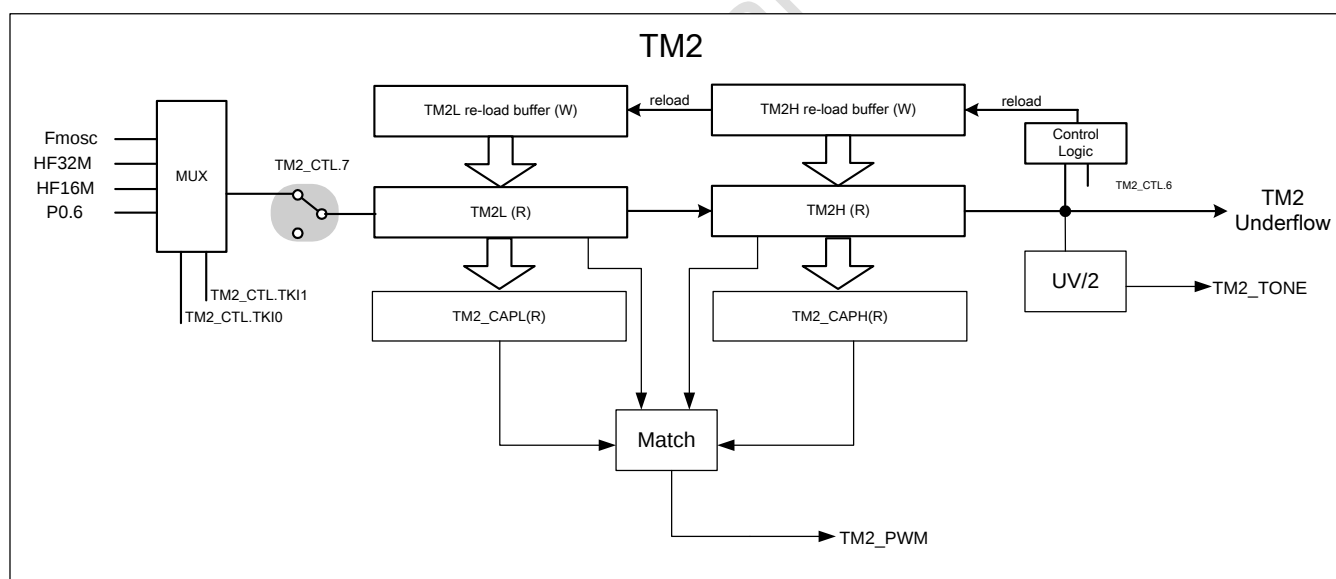
CPS: Capture TM2 Counting Value trigger source select. 0: P1.5, 1: P1.3.

CTKS: Capture source trigger edge selector; 0: rising edge, 1: falling edge

ENCP: TM2 capture function control. 0: Disable (PWM buffer enable), 1: Enable (Capture buffer)

※ The TM2 PWM output would disable, when TM2_CAP/PWMR is configured capture buffer.

TKI1	TKI0	Selected TM2 input clock source
0	0	Fmosc
0	1	HF32M
1	0	HF16M
1	1	P0.6



14 PWM

14.1 PWM Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E2H	PWM_CTL	DT_SCR	PWM_MOD	PWKS1	PWKS0	PWC03	PWC02	PWC01	PWC00	-	√
00E2H	PWM_ST	-	-	-	-	-	-	PWM1	PWM0	√	-

DTSCR: PWM source of dead time control circuit select:

0: 10-bit PWM output

1: 16-bit PWM output (share with TM2 function)

PWM_MOD: PWM output mode select:

PWM_MOD	PWM1 (P1.7)	PWM0 (P1.6)
0	TM2 PWM output	10-bit PWM output
1	PWMH	PWML

PWKS1, PWKS0: PWM clock source selection.

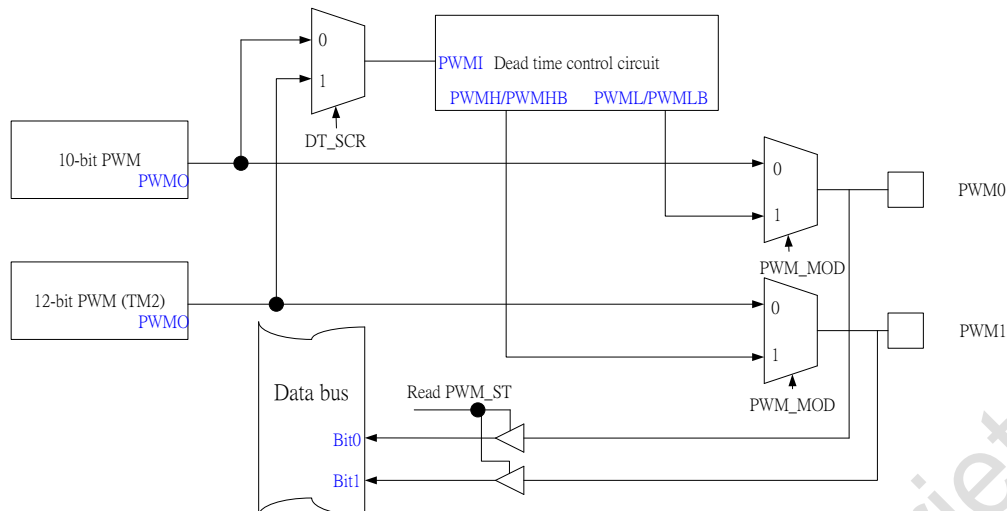
PWKS1	PWKS0	PWM clock source
0	0	Fmosc
0	1	HF32M
1	0	HF16M
1	1	TM0 underflow

PWC03, PWC02, PWC01, PWC00: PWM compare bits selection.

PWC03, PWC02, PWC01, PWC00: PWM compare bits selection.													
PWC03	PWC02	PWC01	PWC00	PWM counter compare bits									
				Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0			-	-	-	-	-	-	-	PW00
0	0	0	1			-	-	-	-	-	-		PW01
0	0	1	0			-	-	-	-	-		PW02	PW01
0	0	1	1			-	-	-	-		PW03	PW02	PW01
0	1	0	0			-	-	-		PW04	PW03	PW02	PW01
0	1	0	1			-	-		PW05	PW04	PW03	PW02	PW01
0	1	1	0			-		PW06	PW05	PW04	PW03	PW02	PW01
0	1	1	1				PW07	PW06	PW05	PW04	PW03	PW02	PW01
1	0	0	0				PW08	PW07	PW06	PW05	PW04	PW03	PW02
1	0	0	1			PW09	PW08	PW07	PW06	PW05	PW04	PW03	PW02
1	0	1	0			PW09	PW08	PW07	PW06	PW05	PW04	PW03	PW02
1	0	1	1			PW09	PW08	PW07	PW06	PW05	PW04	PW03	PW02
1	1	0	0			PW09	PW08	PW07	PW06	PW05	PW04	PW03	PW02
1	1	0	1			PW09	PW08	PW07	PW06	PW05	PW04	PW03	PW02
1	1	1	0			PW09	PW08	PW07	PW06	PW05	PW04	PW03	PW02
1	1	1	1			PW09	PW08	PW07	PW06	PW05	PW04	PW03	PW02
1	1	1	1			PW09	PW08	PW07	PW06	PW05	PW04	PW03	PW02

PWM1: PWM1 output status.

PWM0: PWM0 output status.



14.2 PWM Buffer Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E1H	PWMR1	-	-	-	-	-	-	PW9	PW8	√	√
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E0H	PWMR0	PW07	PW06	PW05	PW04	PW03	PW02	PW01	PW00	√	√

The PWM clock source is controlled by PWKS1 and PWKS0.

The P1.6 pin will provides PWM waveform and output duty is proportional to the code value of PWM buffer.

14.3 PWM Dead Time Select Register

The MG65P701A would be select PWMH and PWML dead time by DT_SEL.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C9H	DT_SEL	-	PWMH_SL	PWML_SL	DTSC1	DTSC0	SEL2	SEL1	SEL0	-	√

PWMH_SL: PWMH output inverting select: 0 PWMH 1: inverted

PWML_SL: PWML output inverting select: 0 PWML 1: inverted

DTSC1, DTSC0: Dead time clock source select

00: $T_d = 1/HF32M$

01: $T_d = 1/HF16M$

10: $T_d = 1/HF8M$

11: $T_d = 1/HF4M$

SEL2, SEL1, SEL0: Dead time select

000: dead time is $[T_d - (1/HF32M)] \sim (T_d)$

001: dead time is $[T_d - (1/HF32M)] \sim (2T_d)$

010: dead time is $[T_d - (1/HF32M)] \sim (3T_d)$

011: dead time is $[T_d - (1/HF32M)] \sim (4T_d)$

100: dead time is $[T_d - (1/HF32M)] \sim (5T_d)$

101: dead time is $[T_d - (1/HF32M)] \sim (6T_d)$

110: dead time is $[T_d - (1/HF32M)] \sim (7T_d)$

111: dead time is $[T_d - (1/HF32M)] \sim (8T_d)$

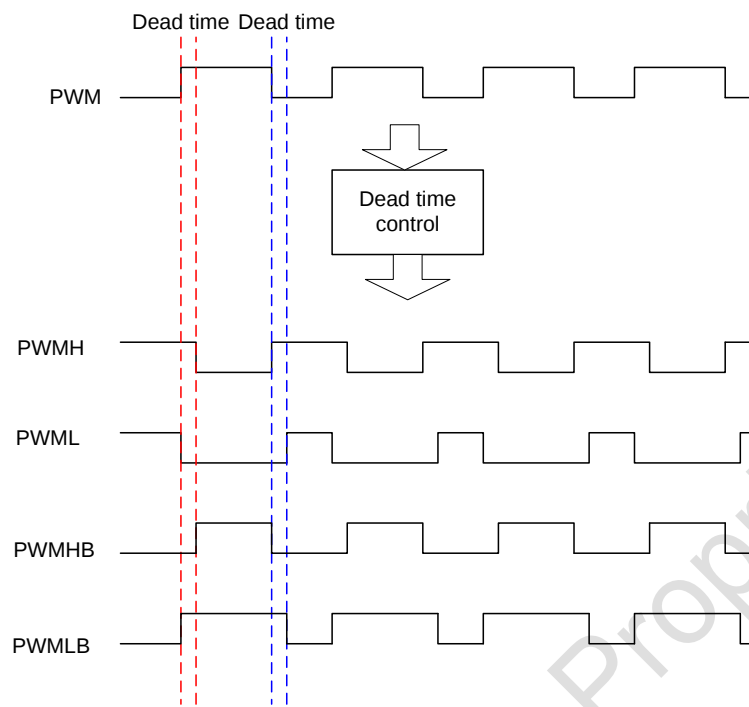


Figure 12-3 PWM output waveform

15 Configurable I/O Ports

15.1 Port 0

15.1.1 Port 0 Port

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E4H	P0port	P07	P06	P05	P04	P03	P02	P01	P00	√	-

Port 0 is combined with 8-bit I/O port. P0.7~P0.0 can be programmed as input or output individually. When P0.n is configured as an output pin, the P0.n pin would output the logic content of internal P0obuf.n (P0 output buffer). The default value of P0obuf is 00000000b.

When the P0.n is configured as output mode, reading P0.n would always read logic '0'.

When the P0.n is configured as input mode, reading P0.n would always read the logic value from pad.

15.1.2 Port 0 Output Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E4H	P0obuf	P07	P06	P05	P04	P03	P02	P01	P00	-	√

This register is used to buffer the output value of P0.7 ~ P0.0 in output mode and it is write-only.

※ Bit-manipulation instructions are not available on this register.

15.1.3 Port 0 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E5H	P0dir	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	-	√

P0_DR (Port 0 Direction)

P0_DR.n = 0: P0.n is configured as an input pin. (Default)

1: P0.n is configured as an output pin.

※ Bit-manipulation instructions are not available on this register.

15.1.4 Port 0 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E6H	P0plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

1: Enable internal pull-high (default); 0: Disable internal pull-high

PHn: Control bit is used to enable the pull-high of P0.n pin.

※ Bit-manipulation instructions are not available on this register.

15.1.5 Port 0 Analog Function Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E7H	P0an	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	-	√

0: Normal I/O function; 1: Analog function

MFn: Control bit is used to P0.n function selection.

※ Bit-manipulation instructions not available on this register.

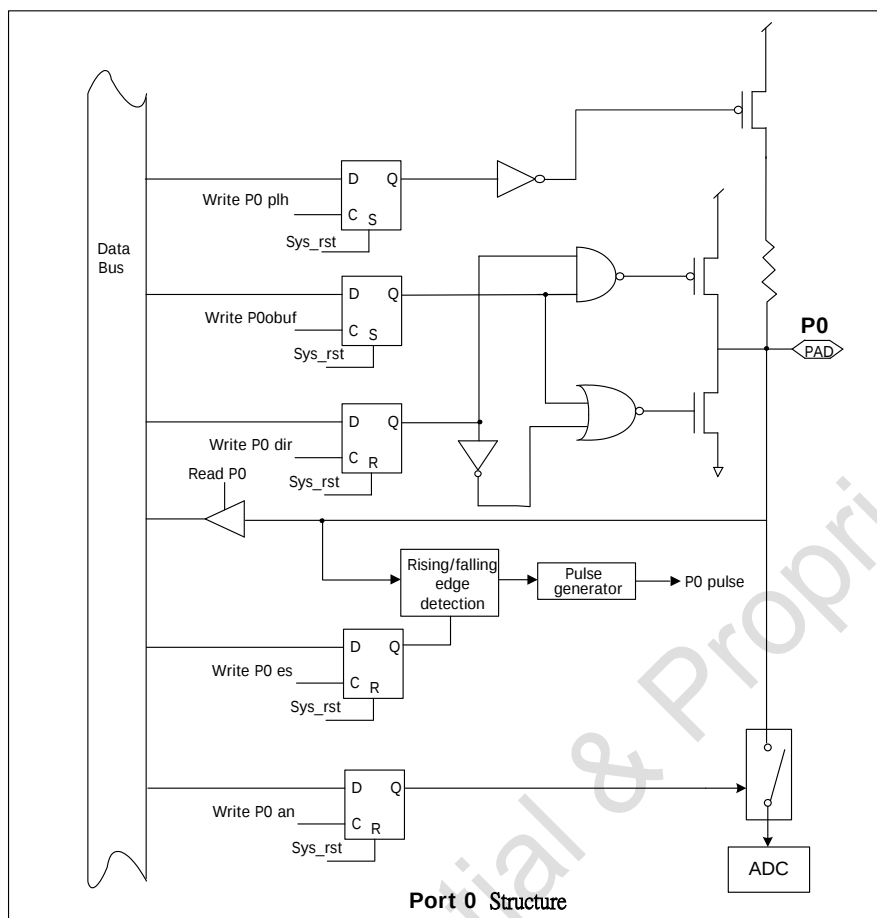
15.1.6 Port 0 Interrupt Edge Select Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00E8H	P0es	ES7	ES6	ES5	ES4	ES3	ES2	ES1	ES0	-	√

0: Falling edge; 1: Rising edge

MFn: Control bit is used to P0.n interrupt edge selection.

※ Bit-manipulation instructions not available on this register.



15.2 Port 1

15.2.1 Port 1 Port

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EAH	P1port	P17	P16	P15	P14	P13	P12	P11	P10	√	-

Port 1 is combined with 8-bit I/O port. P1.7~P1.0 can be programmed as input or output individually. When P1.n is configured as an output pin, the P1.n pin would output the logic content of internal P1obuf.n (P1 output buffer). The default value of P1obuf is 00000000b.

When the P1.n is configured as output mode, reading P1.n would always read logic '0'.

When the P1.n is configured as input mode, reading P1.n would always read the logic value from pad.

15.2.2 Port 1 Output Buffer

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EAH	P1obuf	P17	P16	P15	P14	P13	P12	P11	P10	-	√

This register is used to buffer the output value of P1.7 ~ P1.0 in output mode and it is write-only.

※ Bit-manipulation instructions are not available on this register.

15.2.3 Port 1 Direction Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EBH	P1dir	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	-	√

P0_DR (Port 0 Direction)

P1_DR.n = 0: P1.n is configured as an input pin. (Default)

1: P1.n is configured as an output pin.

※ Bit-manipulation instructions are not available on this register.

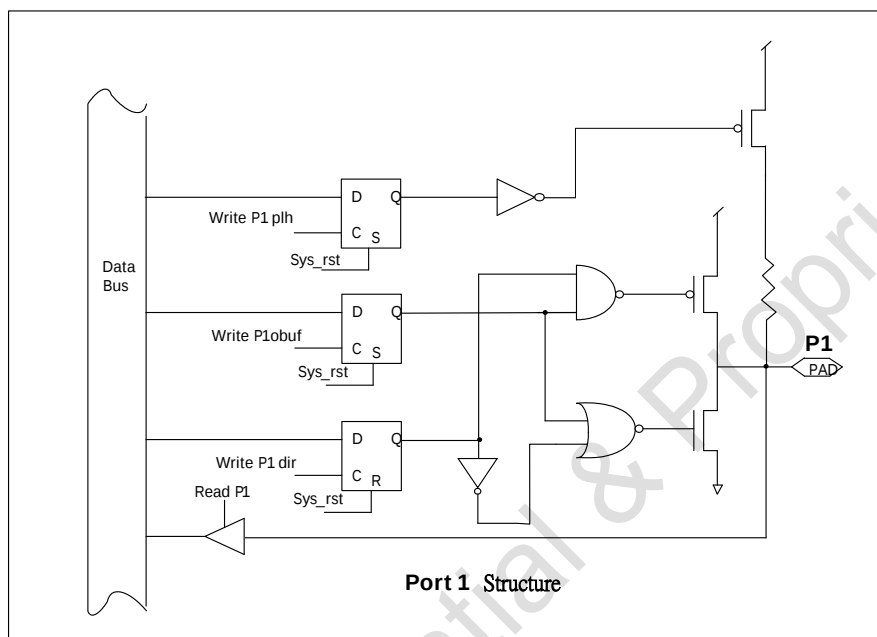
15.2.4 Port 1 Pull-high Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00ECH	P1plh	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	-	√

1: Enable internal pull-high (default); 0: Disable internal pull-high

PHn: Control bit is used to enable the pull-high of P1.n pin.

※ Bit-manipulation instructions are not available on this register.



15.3 Port 0 & Port 1 Function Control Register

15.3.1 Port 0 & Port 1 Output Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00EEH	POsel	-	-	PO5	PO4	PO3	PO2	PO1	PO0	-	√

POn: Control bit is used to P0 or P1 output selection.

PO0: P0.7 output selection. 0: P0.7obuf output, 1: TM1_tone output

PO1: P1.2 output selection. 0: P1.2obuf output, 1: TM1_tone output

PO2: P1.5 output selection. 0: P1.5obuf output, 1: TM2_tone output

PO3: P1.3 output selection. 0: P1.3obuf output, 1: TM2_tone output

PO4: P1.6 output selection. 0: P1.6obuf output, 1: PWM0 output

PO5: P1.7 output selection. 0: P1.7obuf output, 1: PWM1 output

※ Bit-manipulation instructions not available on this register.

16 ADC

The MG65P701A provides an 8-channel 12-bit ADC. The ADC input shares P0.0 ~P0.7.

16.1 ADC Control Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F5H	ADC_CTL0	ADEN	MOD_SEL	VREF_SEL	CS3	CS2	CS1	CS0	SOC	-	√
00F6H	ADC_CTL1	-	-	-	CH4_SEL	EN_BUF	EN_AZ	CK1	CK0	-	√
00F5H	ADC_STS	-	-	-	-	-	-	-	RDY	√	-

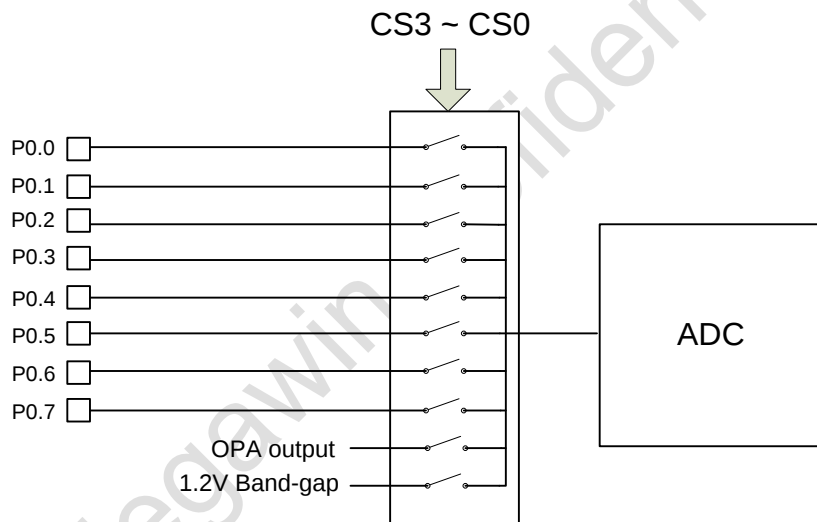
ADEN: "0": Disable ADC function (default), "1": Enable ADC function

MOD_SEL: ADC conversion mode select 0: single-ended mode 1: differential mode

VREF_SEL: ADC reference voltage selection. 0: VDD 1: external reference voltage

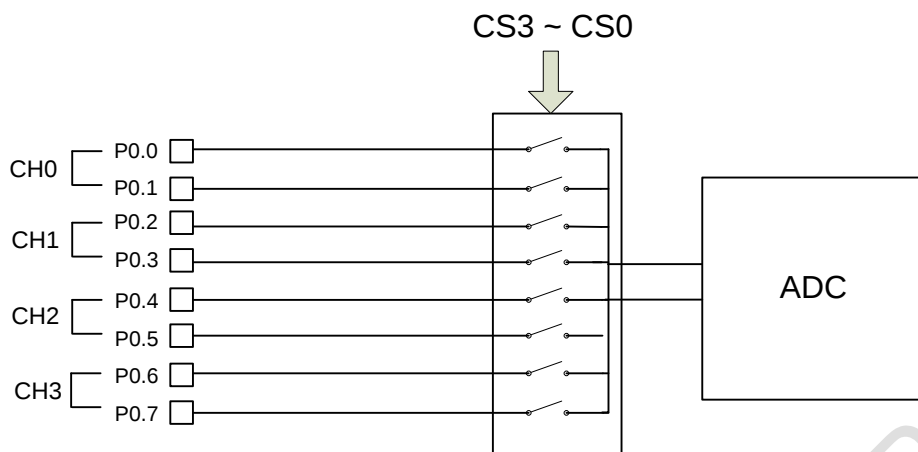
CS3 ~ CS0 analog channel select. (Signal-ended mode)

CS3	CS2	CS1	CS0	ADC input channel
0	0	0	0	VIPA=Channel 0 (P0.0), VINA=GND
0	0	0	1	VIPA=Channel 1 (P0.1), VINA=GND
0	0	1	0	VIPA=Channel 2 (P0.2), VINA=GND
0	0	1	1	VIPA=Channel 3 (P0.3), VINA=GND
0	1	0	0	VIPA=Channel 4 (P0.4), VINA=GND
0	1	0	1	VIPA=Channel 5 (P0.5), VINA=GND
0	1	1	0	VIPA=Channel 6 (P0.6), VINA=GND
0	1	1	1	VIPA=Channel 7 (P0.7), VINA=GND
1	0	0	0	VIPA=OCP circuit output, VINA=GND
1	0	0	1	VIPA= 1.2V Band-gap output, VINA=GND



CS3 ~ CS0 analog channel select. (Differential mode)

CS3	CS2	CS1	CS0	ADC input channel
0	0	0	X	VIPA=P0.0, VINA=P0.1
0	0	1	X	VIPA=P0.2, VINA=P0.3
0	1	0	X	VIPA=P0.4, VINA=P0.5
0	1	1	X	VIPA=P0.6, VINA=P0.7



SOC: Start the A/D conversion. (0→ 1 = start)

CK1 ~ CK0: ADC clock select

CK1	CK0	ADC clock input
0	0	2MHz
0	1	1MHz
1	0	0.5MHz
1	1	32KHz

EN_AZ: ADC offset control signal. 0: Disable offset output 1: Enable offset output

EN_BUF: ADC input buffer control signal. 0: Disable 1: Enable

CH4_SEL: The ADC channel 4 internal resistor control. 0: 1:1 input 1: 1/2 Bias input

RDY: Set by hardware and clear by ADC_CTL.0 start signal. The ADC_STS.0 set to "1" means that A/D convert is completed.

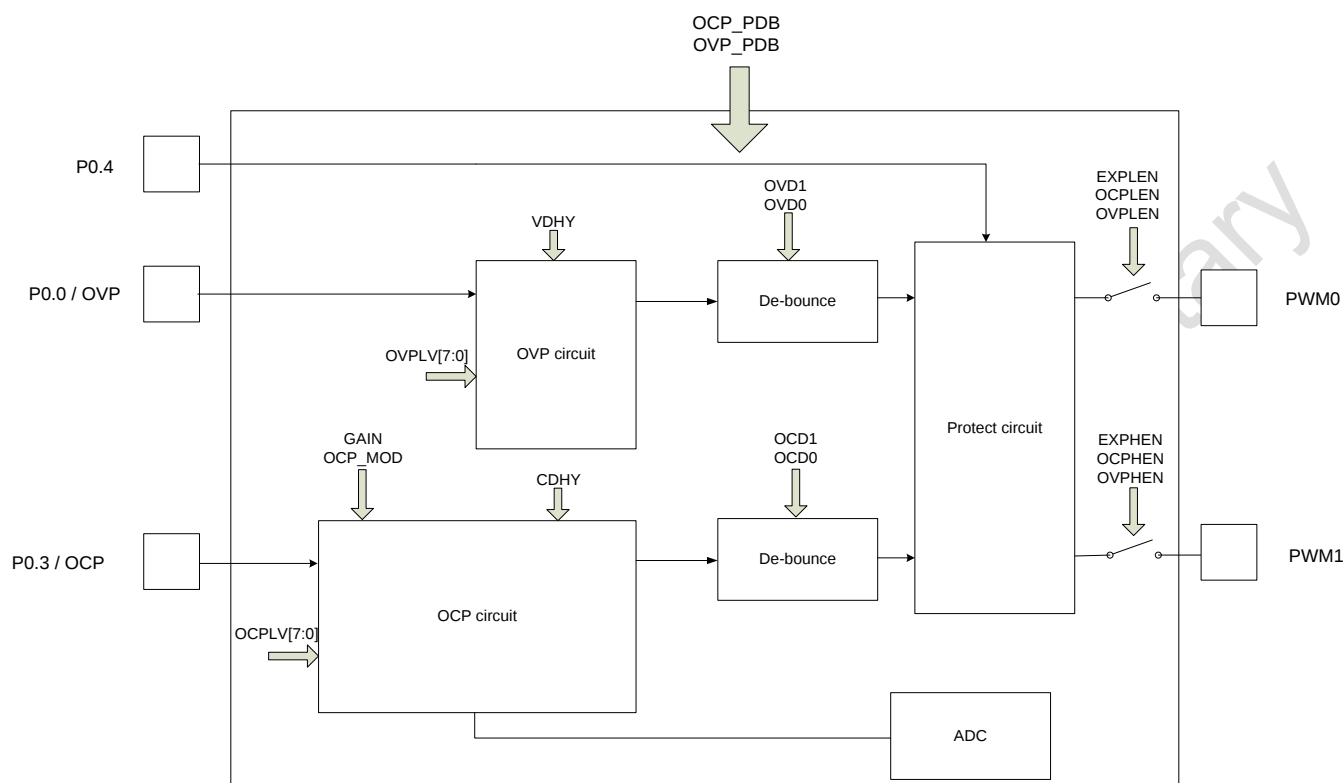
16.2 ADC Data Bus

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00F7H	ADB_L	ADB3	ADB2	ADB1	ADB0					√	-
00F8H	ADB_H	ADB11	ADB10	ADB9	ADB8	ADB7	ADB6	ADB5	ADB4	√	-

After the conversion is completed, the ADB_H and ADB_L could be read to get the conversion result data.

17 Over Current/Voltage Protection

The OCP/OVP circuit includes OCP circuit, OVP circuit and ADC. These blocks are controlled by below SFR.



17.1 Charge Protection Control Register 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C3H	CPCR0	OCP_PDB	OVP_PDB	OCPHEN	OCPLEN	OVPHEN	OVPLEN	CDHY	VDHY	-	√

OCP_PDB: Over current protect circuit power down signal: 0: power down OCP circuit. 1: enable

OVP_PDB: Over voltage protect circuit power down signal: 0: power down OVP circuit. 1: enable

OCPHEN: PWMH over current protect control: 0: disable 1: enable

OCPLEN: PWML over current protect control: 0: disable 1: enable

OVPHEN: PWMH over voltage protect control: 0: disable 1: enable

OVPLEN: PWML over voltage protect control: 0: disable 1: enable

CDHY: Current detector hysteresis windows control signal. 0: disable 1: enable

VDHY: Voltage detector hysteresis windows control signal. 0: disable 1: enable

17.2 Charge Protection Control Register 1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C4H	CPCR1	EXPHEN	EXPLEN	CMOD1	CMOD0	-	GAIN1	GAIN0	OCP_MOD	-	√

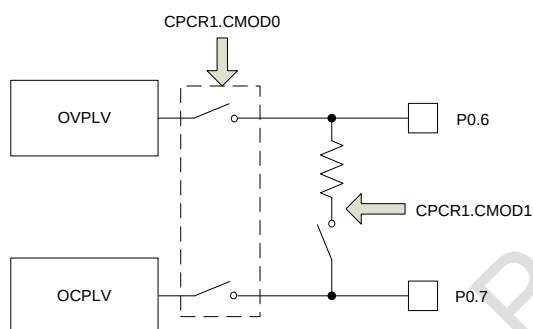
EXPHEN: PWMH external protect control (P0.4). 0: disable 1: enable

EXPLEN: PWML external protect control (P0.4). 0: disable 1: enable

CMOD1: Charge mode selection 1. 0: disable short P0.6 & P0.7 function 1: enable short P0.6 & P0.7 function

CMOD0: Charge mode selection 0. 0: disable OVP & OCP reference voltage output function

1: enable OVP & OCP reference voltage output function



GAIN1~ GAIN0: OCP gain select

GAIN1	GAIN0	Gain
0	0	8
0	1	16
1	0	32
1	1	64

OCP_MOD: OCP charge / discharge mode select: 0: Charge mode 1: Discharge mode

17.3 OCP & OVP De-bounce Selection Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00CAH	PB_SEL	-	-	-	-	OCD1	OCD0	OVD1	OVD0	-	√

OCD: OCP de-bounce timing selection.

00: No de-bounce

01: De-bounce 500ns

10: De-bounce 1000ns

11: De-bounce 2000ns

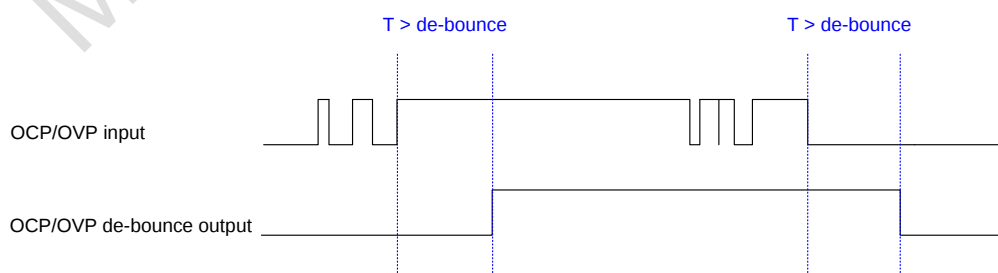
OVD: OVP de-bounce timing selection.

00: No de-bounce

01: De-bounce 500ns

10: De-bounce 1000ns

11: De-bounce 2000ns



17.4 OVP Level Selection Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C6H	OVPLV	OVPLV7	OVPLV6	OVPLV5	OVPLV4	OVPLV3	OVPLV2	OVPLV1	OVPLV0	-	√

The OVPLV provides the over voltage protection reference level.

OVPLV output voltage

OVPLV content	OVPLV output
00H	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 0$
01H	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 1$
02H	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 2$
03H	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 3$
.....	
FDH	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 253$
FEH	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 254$
FFH	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 255$

Example:

$\text{ADC}_{\text{VREF}} = 5\text{V}$, OVPLV content = 80H

OVPLV out = $0.00392 \cdot 5 \cdot 128 = 2.5088\text{v}$

17.5 OCP Level Selection Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00C7H	OCPLV	OCPLV7	OCPLV6	OCPLV5	OCPLV4	OCPLV3	OCPLV2	OCPLV1	OCPLV0	-	√

The OCPLV provides the over current protection reference level.

OCPLV output voltage

OCPLV content	OCPLV output
00H	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 0$
01H	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 1$
02H	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 2$
03H	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 3$
.....	
FDH	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 253$
FEH	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 254$
FFH	$0.00392 \cdot \text{ADC}_{\text{VREF}} \cdot 255$

Example:

$\text{ADC}_{\text{VREF}} = 2.5\text{V}$, OCPLV content = 80H

OCPLV out = $0.00392 \cdot 2.5 \cdot 128 = 1.2224\text{v}$

18 In Application Programming(IAP)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R	W
00FBH	IAP_PR	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	-	√

PR7 ~ PR0: Write Protect Pattern.

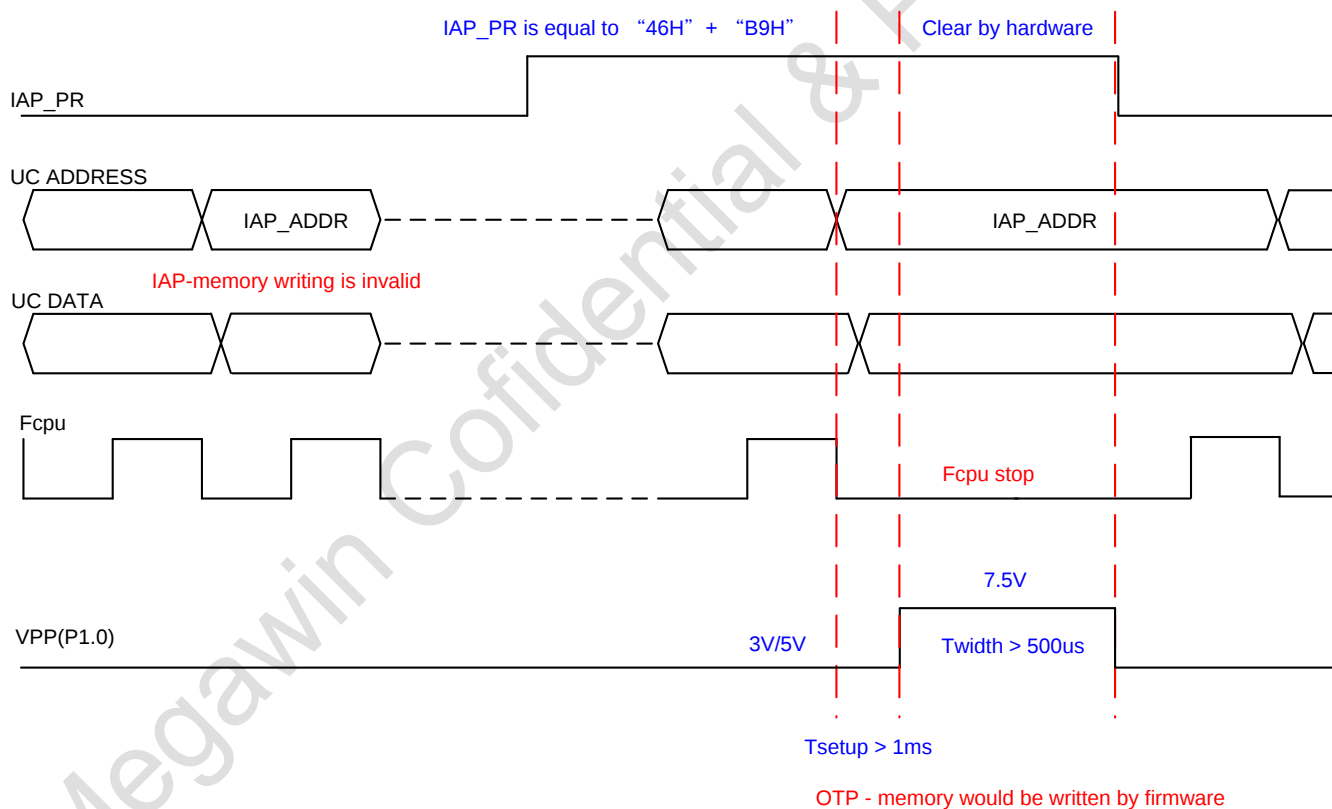
IAP-memory block would be written by firmware, when IAP_WP is written "46H" then "B9H".

The IAP_WP will be automatically cleared by **next uC write action or OTP VPP falling edge**.

Example:

```

Sei
  lda    #78H
  sda    cwpr
  lda    #80H
  sta    SYS_ST    ;;(B7H)
  lda    #46H
  sta    IAP_PR    ;;(F1h)
  lda    #B9H
  sta    IAP_PR    ;;(F1h)
  lda    #$40      ;;The data will be written into OTP.
  sta    $E000     ;;IAP_AREA (E000h ~ FFFFh)
cli
  
```



19 Option Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	FMOSC1	FMOSC0	LOCK	-	WDT	FSOSC	ENSCK

Bit6 ~ Bit5: Fmosc clock source selection

FMOSC1, FMOSC0

00 (HF16M/1): Fmosc use 16MHz clock

01 (HF16M /8): Fmosc use 2MHz clock

10 (HF16M /2): Fmosc use 8MHz clock

11 (HF16M /4): Fmosc use 4MHz clock

Bit 4: LOCK: ICP interface lock bit

0: dump code is locked. (Default)

1: dump code is not locked.

Bit2: WDT: WDT control bit

0 (Disable): Disable watchdog timer function

1 (Enable): Enable watchdog function

Bit1: FSOSC: P1.2 and P1.3 function selection

0(External): External 32K crystal oscillator

1(Internal): Internal 32K oscillator

Bit0: ENSCK: RTC function selection

0(Enable): Enable RTC function (32K crystal OSC always enable)

1(Disable): Disable RTC function

20 Application Circuit

20.1 Reference Schematics

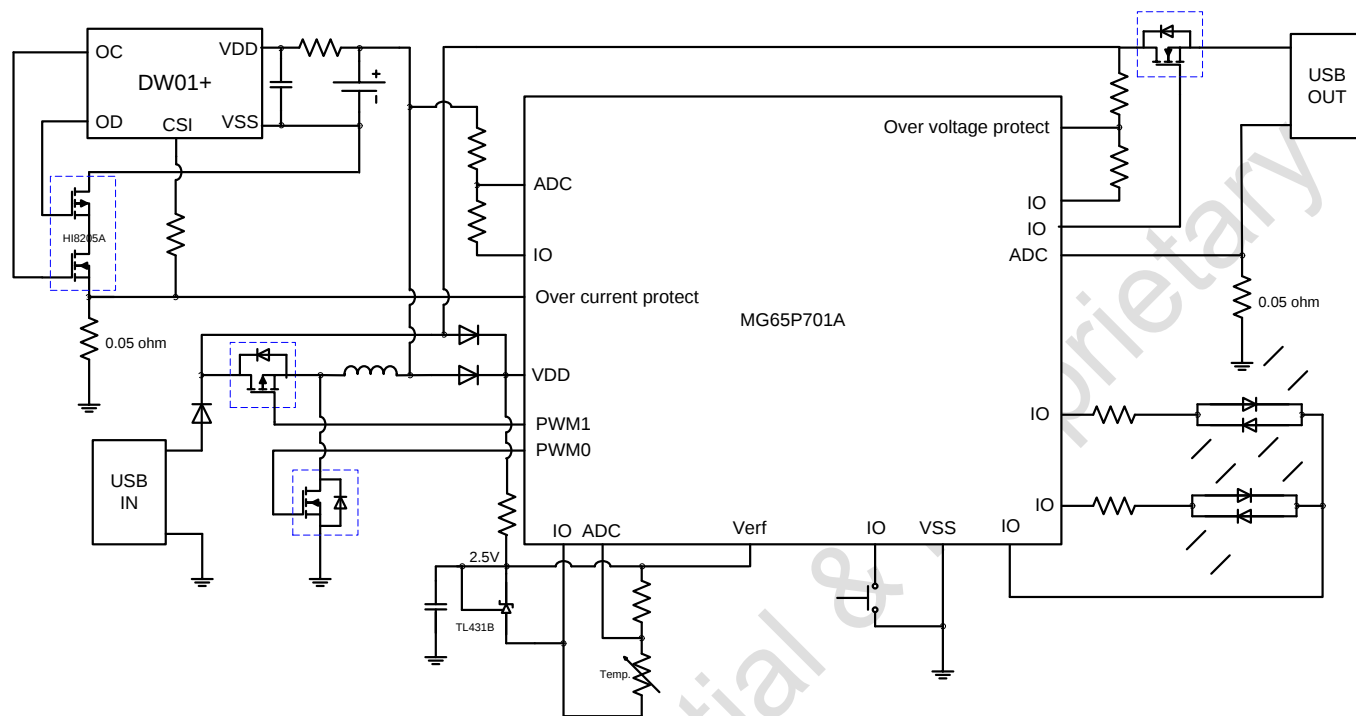


Figure 20-1 Application Circuit – Power bank with DW01+

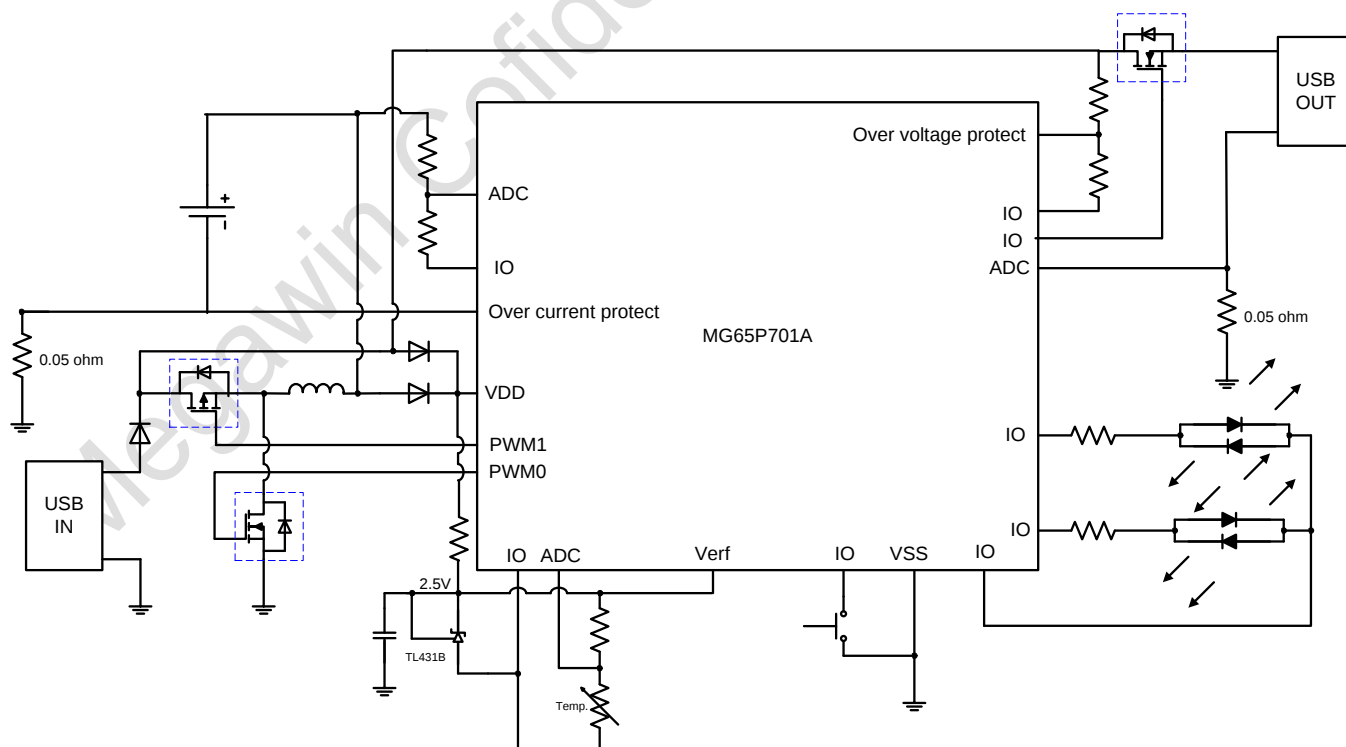
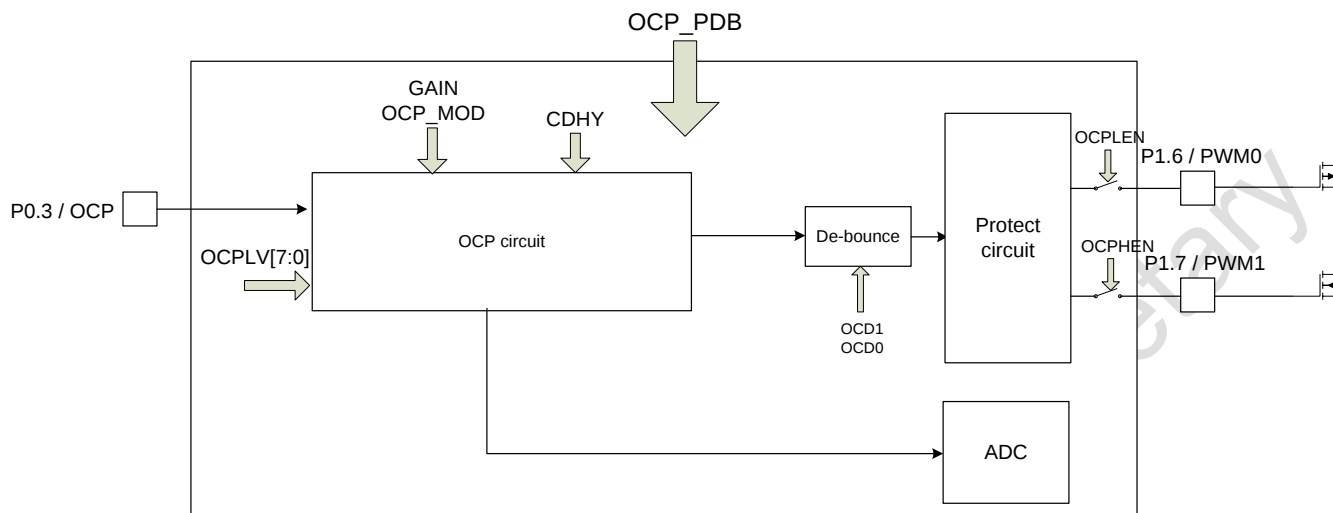


Figure 20-2 Application Circuit – Power bank with LED display

21 Application Note

21.1 Setup Over Current Protection Circuit



OCP function setup

1. Enable over current protection circuit. (OCP_PDB = 1)
2. Setup reference level of over current protection. (Setup the OCPLV contents)
3. Calibration OCP circuit offset.

EXAMPLE CODE:

```

OFFSET1:
    LDA    #$E0
    STA    $CD
    TAX
    BBR    1,$CF,ADJ_UP1

ADJ_DOWN1:
    DEX
    TXA
    AND    #$3F
    CMP    #$3F
    BEQ    FAIL
    STX    $CD
    BBS    1,$CF,ADJ_DOWN1
    JMP    PASS1

ADJ_UP1:
    INX
    TXA
    AND    #$3F
    BEQ    FAIL
    STX    $CD
    BBR    1,$CF,ADJ_UP1
    ; when offset adjustment pass

PASS1:
    PHX
    PLA
    AND    #$7F
    STA    $CD
    JMP    OFFSET2

FAIL:
    ..... ; when offset adjustment fail

OFFSET2:
    LDA    #$E0
    STA    $CE
    TAX
    BBR    2,$CF,ADJ_UP2

ADJ_DOWN2:
    DEX
    TXA
    AND    #$3F
    CMP    #$3F
    BEQ    FAIL
  
```

```

                STX    $CE
                BBS    2,$CF,ADJ_DOWN2
                JMP    PASS2

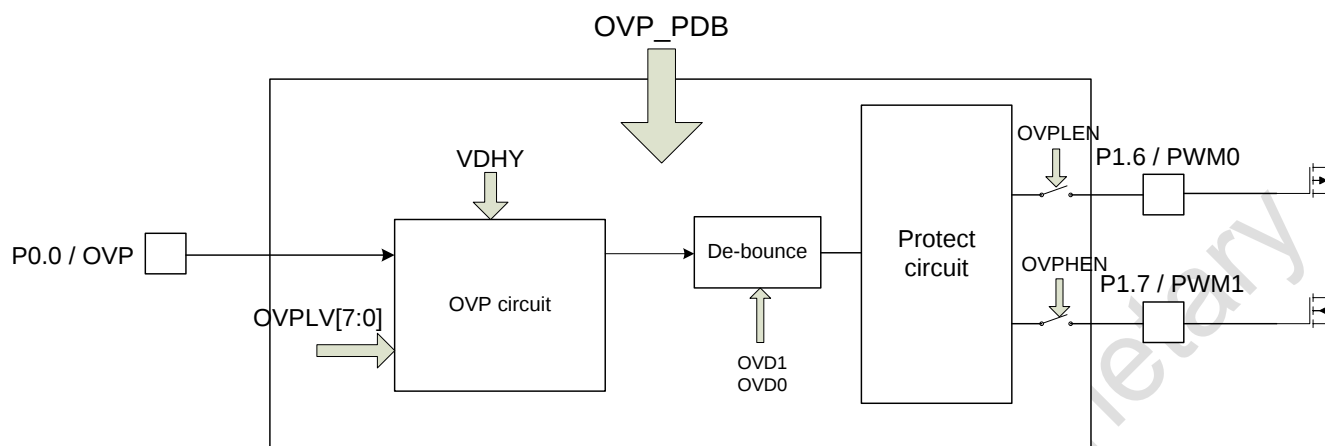
ADJ_UP2:
                INX
                TXA
                AND    #$3F
                BEQ    FAIL
                STX    $CE
                BBR    2,$CF,ADJ_UP2
                ; when offset adjustment pass

PASS2:
                PHX
                PLA
                AND    #$7F
                STA    $CE
                .....

```

4. Enable OCP circuit hysteresis function. (CDHY = 1)
5. Select over current protection de-bounce timing of output. (Setup the OCD1 and OCD0)
6. Select the protection pin by over current protection output. (Setup the OCPHEN and OCPLN)
7. When OCP event occurs, the PWM0 or PWM1 output would be stop.

21.2 Setup Over Voltage Protection Circuit



OVP function setup

1. Enable over voltage protection circuit. (OVP_PDB = 1)
2. Setup reference level of over voltage protection. (Setup the OVPLV contents)
3. Calibration OVP circuit offset.

EXAMPLE CODE:

OFFSET:

```
LDA    #$E0
STA    $CC
TAX
BBR    0,$CF,ADJ_UP
```

ADJ_DOWN:

```
DEX
TXA
AND    #$3F
CMP    #$3F
BEQ    FAIL
STX    $CC
BBS    0,$CF,ADJ_DOWN
JMP    PASS
```

ADJ_UP:

```
INX
TXA
AND    #$3F
BEQ    FAIL
STX    $CC
BBR    0,$CF,ADJ_UP
```

PASS: ; when offset adjustment pass

```
PHX
PLA
AND    #$7F
STA    $CC
```

FAIL: ; when offset adjustment fail

4. Enable OVP circuit hysteresis function. (VDHY = 1)
5. Select over voltage protection de-bounce timing of output. (Setup the OVD1 and OVD0)
6. Select the protection pin by over voltage protection output. (Setup the OVPHEN and OVPLEN)
7. When OVP event occurs, the PWM0 or PWM1 output would be stop.

22 Electrical Characteristics

22.1 Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	VSS-0.3 to VSS+4.0	V
Applied Input / Output Voltage	VSS-0.3 to VDD+0.3	V
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-50 to +125	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

22.2 DC Characteristics

(VDD-VSS = 3.0 V, FOSC = 4MHz, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input High Voltage	VIH	-	0.7 VDD	-	VDD	V
Input Low Voltage	VIL	-	0	-	0.3 VDD	V
Op. Current	IOP	Dual mode, No load, LCD on Fcpu=4Mhz		1.8	5.6	mA
Halt Current	ISTB1	Slow mode, HALT, Fcpu=32768Hz, DIVx INT off		10		uA
Stop Current	ISTB2	STOP mode,	-	1		uA
P0 ~ P1 Internal Pull-high Resistor	RPH1	VIL = 0V	30K	50K	70K	Ω
/RES Pull-high Resistor	RRES	VIL = 0V	-	30K	-	Ω
Port 0 drive current	IOH1	VOH = 2.4V, VDD = 3.0V	5	-	-	mA
Port 0 sink current	IOL1	VOL = 0.4V, VDD = 3.0V	10	-	-	mA
Port1.0 ~Port 1.5 drive current	IOH2	VOH = 2.4V, VDD = 3.0V	5	-	-	mA
Port1.0 ~Port 1.5 sink current	IOL2	VOL = 0.4V, VDD = 3.0V	10	-	-	mA
Port1.6 ~Port 1.7 drive current	IOH3	VOH = 2.6V, VDD = 3.0V	50	-	-	mA
		VOH = 4.6V, VDD = 5.0V	100			
Port1.6 ~Port 1.7 sink current	IOL3	VOL = 0.4V, VDD = 3.0V	50	-	-	mA
		VOL = 0.4V, VDD = 5.0V	100			
Low Voltage Detector 0	VLVD0	VDD > 2.4V	-	2.4	-	V
Low Voltage Detector 1	VLVD1	VDD > 2.7V	-	2.7	-	V
Low Voltage Reset	VLVR	-	-	2.0	-	V

22.3 AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Built-in CPU Op. Frequency	FCPU	Internal OSC, VDD = 3.0V	0.008	4	8	MHz
POR duration	TPOR	FOSC = 4 MHz	-	4	1	mS
System Start-Up Time	Tsst	Power-up, reset		16384		1/FCPU
System Wake-Up Time	Tswt	wake-up from STOP mode	256		16384	1/FCPU

23 Revision History

Revision	Page	Descriptions	Date
V1.00		1. Initial release	2013/05/15
V1.01		1. Correct errors in function description	2013/09/26
V1.02		1. Modify DC characteristics	2013/09/27
V1.03		1. Modify PWM register contents	2013/10/23
V1.04		1. Modify features description	2013/11/25
		2. Add ADC input channel diagram	
		3. Modify OCP / OVP block diagram	
V1.05		1. Modify feature description & LVR voltage	2013/11/27
V1.06		1. Add DAC output function	2013/12/23
V1.07		1. Correct errors in OCP / OVP function	2014/02/14
V1.08		1. Modify ADC clock source	2014/02/21
V1.09		1. Modify ADC input channel SPEC.	2014/03/28
V1.10		1. Modify feature description	2014/04/21
V2.00		1. Modify feature description	2014/05/20
		2. Add application note	