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USB Bridge

MA111
Data Sheet

Version: 0.89

Features

- HID USB to Serial Bridge
  - USB bridge to GPIO control, UART TX/RX, SPI Master and I2C Master
  - Standard USB class device requires no custom driver
  - USB Full speed (12Mbps) operation and USB specification 2.0 compliant
  - Built-in USB transceiver and 3.3V regulator
  - Integrated clock recovery, no external crystal required
  - USB suspend states reported via UPD pins
  - Windows HID Libraries
    - Support Windows 7, Windows 8.1, Windows 10
- 11 GPIO pins with configurable options
  - Usable as disable, digital input, open-drain, open-drain with pull-up and push-pull output
  - Interrupt report on GPIO0~GPIO7 input changed
  - Remote wakeup capability on WKP0 and WKP1
  - Configurable 12MHz or 6MHz clock output
  - Up to 3-channel 8-bit PWM output
- UART Interface
  - 8-bit data format
  - Parity: odd, even, mark, space and no parity
  - Stop bits: 1 and 2
  - Baud Rate: 600, 1200, 2400, 4800, 9600, 19200, 38400, 51200, 57600, 102400, 115200 and 230400
  - Line Break detection and transmission
  - CTS/RTS flow control option
  - Selectable MSB first or LSB first on data transmission
  - DE output for RS-485 bus transceiver control
  - Configurable polarity for DE/CTS/RTS output
  - Master/slave mode in multi-processor communication
    - Provide 2 slave address recognition
- SPI Master Interface
  - 3 or 4-wire master mode operation
  - Supports all four SPI operation modes (mode 0, 1, 2, and 3)
  - 8-bit data format
  - Selectable MSB first or LSB first on data transmission
  - Support SPI clock rate on 2MHz or 6MHz
- I2C Master Interface
  - 8-bit data format
  - Support clock rate on 25K/50K/75K/100KHz
  - Read/Write timeout control
  - Not support multiple masters application on I2C bus
- Operating voltage range
  - USB bus powered: 4.0V – 5.5V
  - Self-powered: 3.0V – 3.6V
- Operating Temperature: (-40°C to +85°C)*
- Package Types:
  - SOP16 (150mil): MA111AS16
  - QFN16 (4x4mm): MA111AY16

*: Tested by sampling.

List of Contents

1. General Description

The MA111 is a highly-integrated USB bridge to support UART protocol, SPI master, Two Wire serial Interface I2C master and GPIO read/write/interrupt/wakeup functions. It includes a USB 2.0 full-speed function controller, USB transceiver, oscillator and on-chip 3.3V regulator for USB transceiver power (that is applied on VDD range from 4.0V to 5.5V).

The MA111 is a driver free USB Data Bridge solution. Megawin provides a DLL in Window environment that makes user to handle MA111 easily. The available supported OS includes Windows 7, Windows 8.1 and Windows 10.

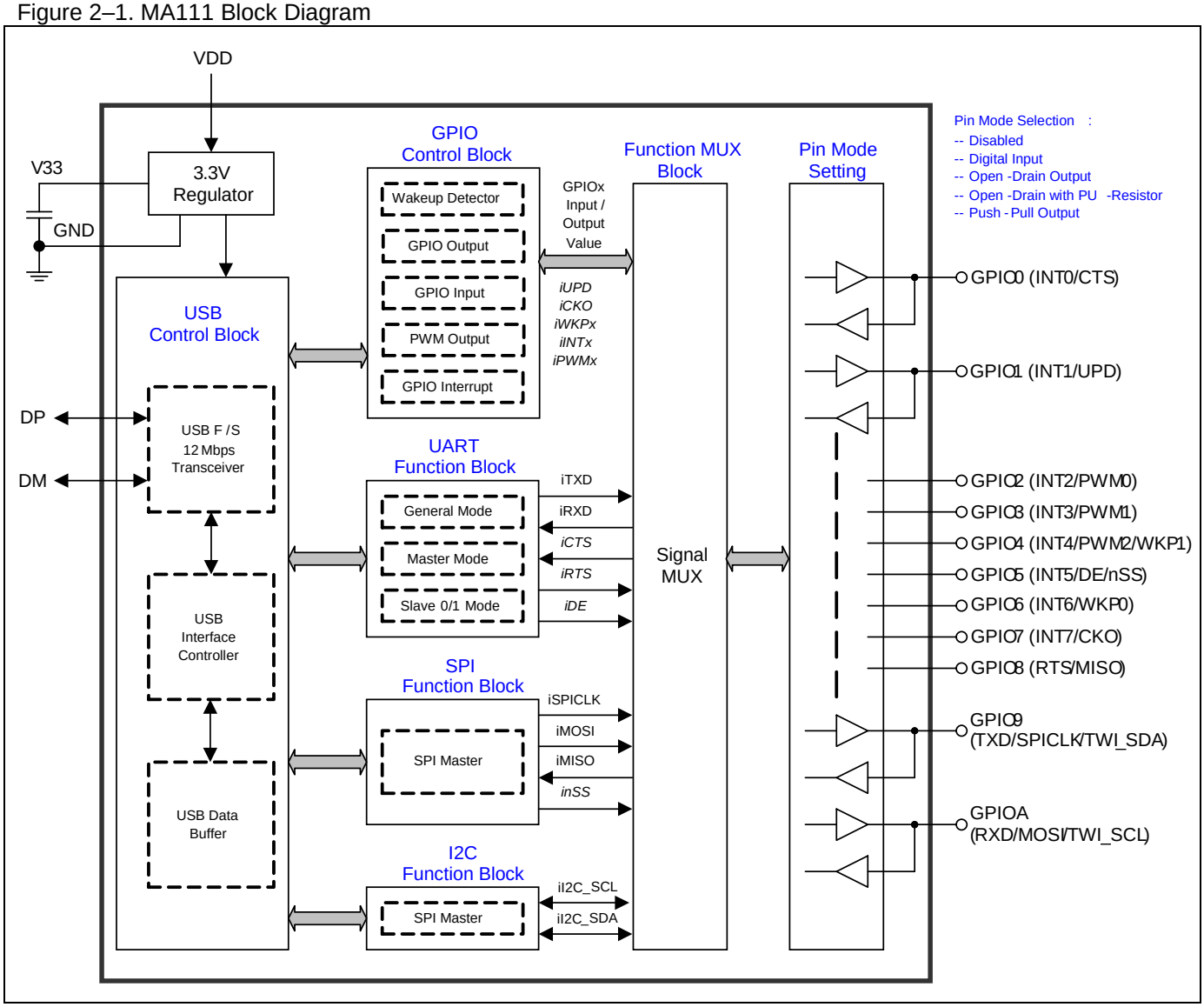
In the MA111, there are 7 function modules, including USB control block, GPIO control block, UART function block, SPI function block, I2C function block, Function MUX block and Pin Mode setting block. After power-on, all pins serves the GPIO control function with default setting in Function MUX block. Except USB interface pins and VDD/VSS pins, MA111 has 11 GPIO pins, GPIO0 ~ GPIOA. GPIO control block accept the user's request to perform the pin In/Out function through USB command. For properly In/Out function, user would configure the "Pin Mode" on each GPIO pin, such as push-pull output or digital input, to apply the system required.

There are 3 serial interface function block in the MA111, including UART, SPI master and I2C master. User software only can choose one of these three serial interfaces to perform the data transfer. So, the MA111 cannot support UART and SPI or I2C concurrently. But, user can switch the UART/SPI/I2C function by software configured through USB command.

If the MA111 is configured to UART mode, the TXD and RXD are the necessary functions and appears on dedicated GPIO pins (GPIO9 and GPIOA) through function MUX. User still needs to configure the suitable pin mode on GPIO9 and GPIOA to fit the TXD and RXD application, such as push-pull mode on TXD(GPIO9) and digital input on RXD(GPIOA). Other signals on UART, RTS, CTS or DE, are optional by user selection through USB command to enable the function on dedicated GPIO pins and decide the Pin Mode setting. If the MA111 is configured to SPI master or I2C mode, the same structure is applied on GPIO assignment.

2. Block Diagram

Figure 2–1. MA111 Block Diagram



3. Pin Configurations

3.1. Package Instruction

Figure 3–1. MA111 SOP16 Top View

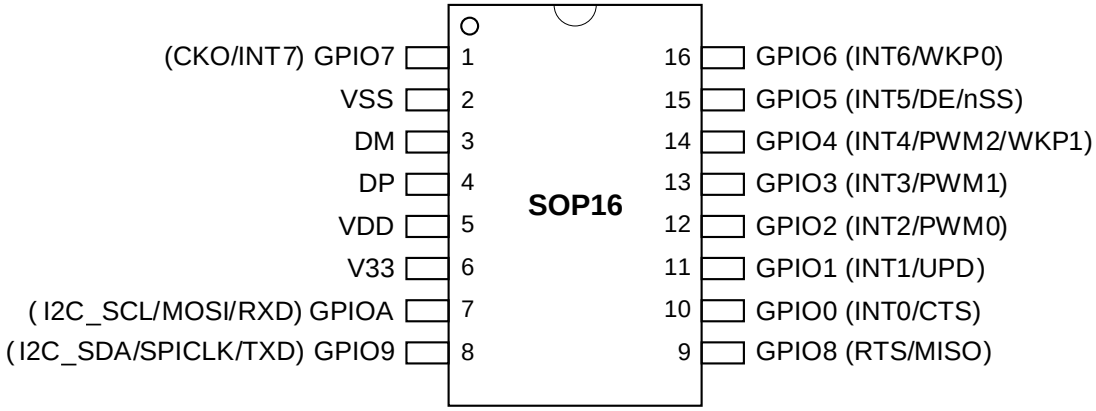
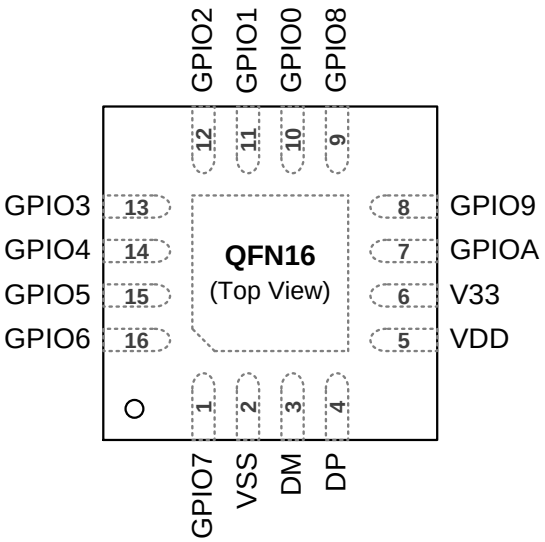


Figure 3–2. MA111 QFN16 Top View



3.2. Pin Description

Table 3–1. Pin Description

MNEMONIC	PIN NUMBER			I/O TYPE	DESCRIPTION
	16-Pin SOP	16-Pin QFN	--		
GPIO0 (INT0) (CTS)	10	10	--	I/O	* GPIO0. Default pin configuration is disabled. * INT0: Interrupt 0 input. * CTS: CTS input in UART mode.
GPIO1 (INT1) (UPD)	11	11	--	I/O	* GPIO1. Default pin configuration is disabled. * INT1: Interrupt 1 input. * UPD: USB bus Power Down indicator output.
GPIO2 (INT2) (PWM0)	12	12	--	I/O	* GPIO2. Default pin configuration is disabled. * INT2: Interrupt 2 input. * PWM0: PWM channel 0 output.
GPIO3 (INT3) (PWM1)	13	13	--	I/O	* GPIO3. Default pin configuration is disabled. * INT3: Interrupt 3 input. * PWM1: PWM channel 1 output.
GPIO4 (INT4) (PWM2) (WKP1)	14	14	--	I/O	* GPIO4. Default pin configuration is disabled. * INT4: Interrupt 4 input. * PWM2: PWM channel 2 output. * WKP1: MA111 wakeup input 1.
GPIO5 (INT5) (DE) (nSS)	15	15	--	I/O	* GPIO5. Default pin configuration is disabled. * INT5: Interrupt 5 input. * DE: Driver Enable for RS-485 transceiver control in UART mode. * nSS: Chip Select output in SPI Master mode.
GPIO6 (INT6) (WKP0)	16	16	--	I/O	* GPIO6. Default pin configuration is disabled. * INT6: Interrupt 6 input. * WKP0: MA111 wakeup input 0.
GPIO7 (INT7) (CKO)	1	1	--	I/O	* GPIO7. Default pin configuration is disabled. * INT7: Interrupt 7 input. * CKO: 12MHz or 6MHz clock output.
GPIO8 (RTS) (MISO)	9	9	--	I/O	* GPIO8. Default pin configuration is open-drain with pull-up resistor. * RTS: RTS output in UART mode. * MISO: Master In & Slave Out in SPI master mode.
GPIO9 (TXD) (SPICLK) (I2C_SDA)	8	8	--	I/O	* GPIO9. Default pin configuration is open-drain with pull-up resistor. * TXD: Transmit Data output in UART mode. * SPICLK: SPI Clock output in SPI master mode. * I2C_SDA: I2C Serial Data pin in I2C master mode.
GPIOA (RXD) (MOSI) (I2C_SCL)	7	7	--	I/O	* GPIOA. Default pin configuration is open-drain with pull-up resistor. * RXD: Receive Data input in UART mode. * MOSI: Master Out & Slave In in SPI master mode. * I2C_SCL: I2C Serial Clock pin in I2C master mode.
DP	4	4	--	I/O	* DP: USB DP(D+) pin.
DM	3	3	--	I/O	* DM: USB DM(D-) pin.
VDD	5	5	--	P	Power supply input.
VSS	2	2	--	G	Ground, 0 V reference.
V33	6	6	--	P	3.3V input/output

4. MA111 Operating Mode

There are 4 operation modes in MA1111, GPIO mode, UART mode, SPI master mode and I2C master mode. After power-on, all pins of MA111 are operating in GPIO mode. User can select the functional block to switch the GPIO function to serve the alternated communication, such as UART TXD/RXD, CTS, RTS, DE etc. The other pin without UART function will be kept the GPIO function. User only can select one of 3 serial interface, UART, SPI master and I2C master, in the MA111 operation.

Each function block don't control the pin configuration. So, user must program the pin configuration on each GPIO pin to match the application requirement.

5. GPIO Configuration

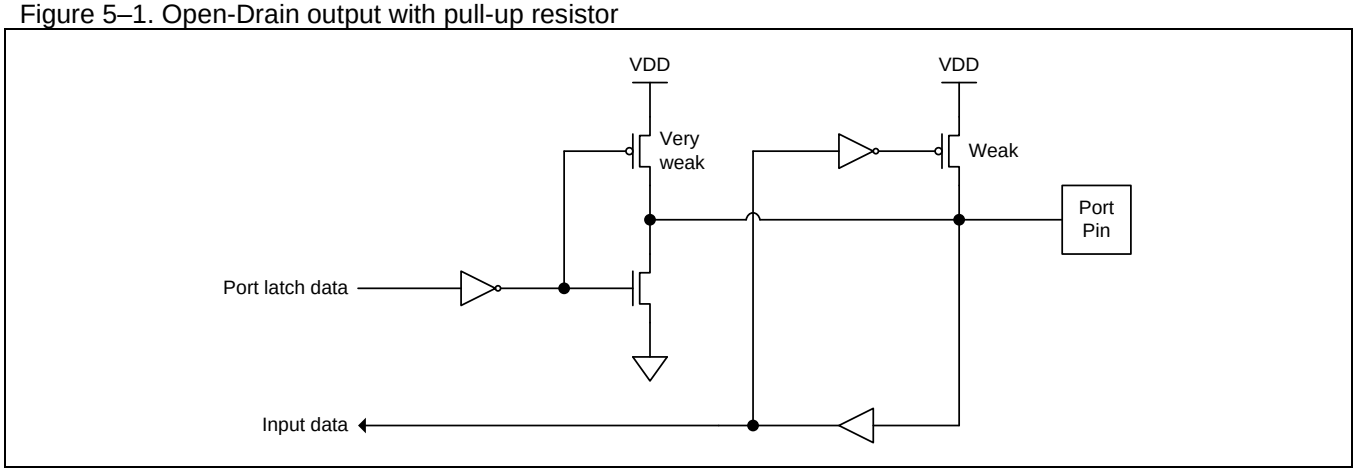
Table 5–1 lists the default configuration and options of all pins. All pins have the same setting options except the GPIO8/9/A which are the quasi bi-direction as the default configuration right after power-up reset. The default output value of all GPIO in the MA111 is "1".

Table 5–1. Pin Description

Pin Name	Default Configuration	Configuration Options
GPIO0	Disabled	Disabled Digital Input Push-Pull Output Open-Drain Output Open-Drain Output with pull-up
GPIO1	Disabled	
GPIO2	Disabled	
GPIO3	Disabled	
GPIO4	Disabled	
GPIO5	Disabled	
GPIO6	Disabled	
GPIO7	Disabled	
GPIO8	Open-Drain output with Pull-up (Quasi bi-direction)	
GPIO9	Open-Drain output with Pull-up (Quasi bi-direction)	
GPIOA	Open-Drain output with Pull-up (Quasi bi-direction)	

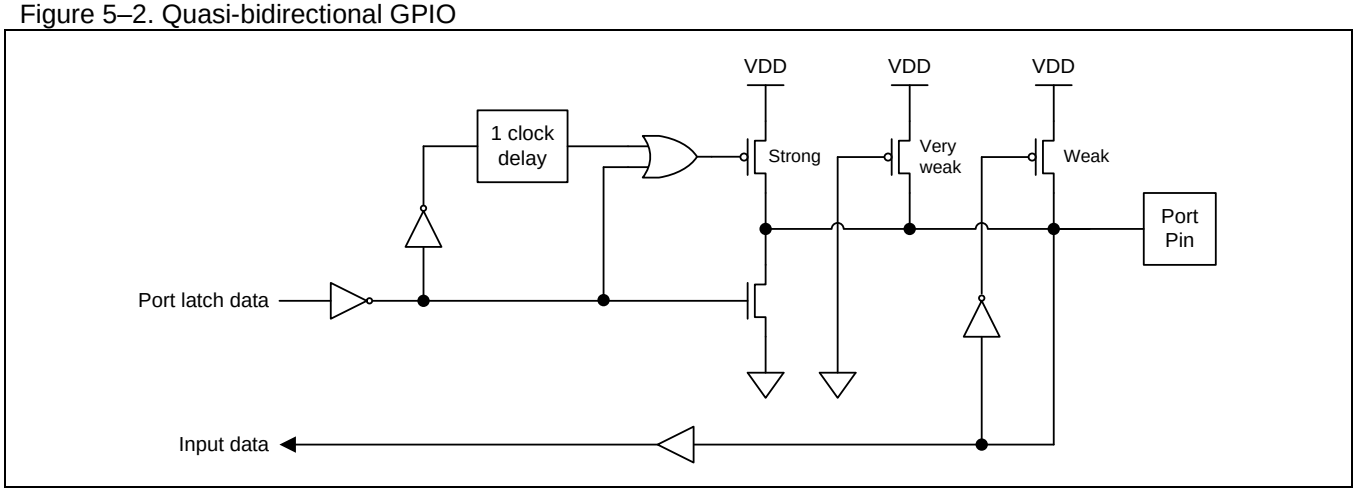
To configure the GPIO to digital input, software must set the port pin to open-drain output mode and set output data to "1". Then the GPIO configuration is equivalent to digital input pin. The on-chip pull-up resistance is embedded two resistors on each GPIO pin. One is weak pull-up resistor and another one is very weak pull-up resistor. Figure 5–1 shows the on-chip pull-up resistors on open-drain output mode.

Figure 5–1. Open-Drain output with pull-up resistor



Especially for the quasi-bidirectional port pin, its configuration is illustrated in Figure 5–2. The output high will has one clock driving by push-pull mode output to enhance rising time, then keep the port pin state by pull-up resistors, weak & very weak. This configuration exists on GPIO8/9/A.

Figure 5–2. Quasi-bidirectional GPIO



6. GPIO Operating Mode

All GPIO pins of MA111 can serve the general behavior to set port pin output and to read port pin input. In GPIO mode, MA111 GPIO also provide the alternated function. The following sections describe the alternated function in GPIO mode:

Note:
If the port pin is selected to alternated function, software must avoid to set the port output value that will override the alternated function behavior.

6.1. GPIO Output and Input

For GPIO output, user software needs to control the target GPIO pin as following flow:
- *Set the output value to initialize the target GPIO state. In default, each GPIO output value is "1".*
- *Set the output mode on target GPIO. It will be push-pull output, open-drain output or open-drain output with pull-up.*
- *If the output pin is set to open-drain output, the external pull-up resistor on the pin is necessary.*
- *Software writes the output value on the GPIO pin by application requirement.*

For GPIO input, user software needs to control the target GPIO pin as following flow:
- *Keep the output value on the target GPIO as default state "1".*
- *Set the input mode on target GPIO. It will be open-drain (digital input) or open-drain output with pull-up.*
- *Software reads the pin state on the GPIO pin by application requirement.*

To reduce power consumption, software must keep the un-used GPIO in power-on reset state. That means the software does not need any setting on un-used GPIO pin after MA111 power-on.

6.2. CKO on GPIO7

MA111 can output internal clock onto PGIO7. There are two frequencies to select: 6MHz and 12MHz. When GPIO7 serves CKO function, the output type is defined in port pin configuration. If user selects the GPIO7 configuration to disabled state, the CKO will not behave on GPIO7. In general, setting push-pull mode on GPIO7 for CKO function is necessary.

Note:
- *For VDD= 4.5V~5.5V application, CKO can support 12MHz and 6MHz output frequency.*
- *For VDD= 3.0V~4.5V application, CKO only can support 6MHz output frequency.*

6.3. UPD on GPIO1

GPIO1 can be configured to be UPD output which is USB bus power down indicator (USB Suspend). If UPD output is configured, The MA111 will act UPD output to indicate the USB suspend state. The active polarity of UPD is configured by software.

6.4. WKP0~1 on GPIO6/4

The MA111 provides the USB remote wakeup capability. That is, when USB bus enters suspend state, user system can wake up the USB system through WKP0 and WKP1 of the MA111. The WKP0 and WKP1 can be enabled and program the active polarity individually.

6.5. INT0~INT7 on GPIO0~GPIO7

The MA111 can report INT0~INT7 input state changed individually. In real application, host software receives the INT0~INT7 event, then start to read the Pin status. That will reduce the host software effort to poll the GPIO pin input state. MA111 report capability on INT0~INT7 could be enabled individually by software configured.

6.6. Single Pulse output on GPIOs

The MA111 has embedded a special command to implement the pulse output on an output GPIO pin. User can select a GPIO as an output pin and set an output value as pin initial state. Then software invokes the SetGPIOPulse() command to trigger the MA111 output a pulse on the GPIO pin. For example, software sets GPIO1 as output pin and output logic high. If the MA111 receives the SetGPIOPulse() command on GPIO1, it will output a logic low pulse on GPIO1. The minimal low pulse width is 200ns, 250ns typically. Otherwise, if software sets the GPIO1 to output logic low, the MA111 will output a high pulse on GPIO1 after SetGPIOPulse() received. The high pulse timing is same as low pulse specification.

6.7. PWM output on GPIO2/3/4

The MA111 provides 3 channels PWM output on GPIO. PWN0/1/2 are located at GPIO2/3/4. This function implements the 8-bit resolution PWM. If UART function is enabled, PWM2 function will be disabled.

For PWM output, the duty cycle is decided by SetPWMDutyValue command. The PWM dutyp cycle equation is list as following:

PWM Duty Cycle = 1 – { SetPWMDutyValue } / 256.

For examples,
a. If SetPWMDutyValue = 0x00, the duty cycle is 100%.
b. If SetPWMDutyValue = 0x40, the duty cycle is 75%.
c. If SetPWMDutyValue = 0xC0, the duty cycle is 25%.
d. If SetPWMDutyValue = 0xFF, the duty cycle is 1/256.

7. UART Operating Mode

When UART mode is enabled in the MA111, the GPIO9 and GPIOA are forced to serve the UART TXD output and the UART RXD input. But the port pin configuration is programmed by software. Such as, user can configure TXD to push-pull output or open-drain output with on-chip pull-up resistor.

The UART engine in MA111 only provides 8-bit data format with parity options and 1 or 2 stop bit selections. It provide the parity options on: none, even, odd, mark and space. It provides the baud rate selections as 600, 1200, 2400, 4800, 9600, 19200, 38400, 51200, 57600, 102400, 115200 and 230400. It also provide the break output and break detection.

Table 7–1 lists the UART data format and baud rate available in MA111.

Table 7–1. UART Data Formats and Baud Rates

Item	Function Selection
Data Bits	8
Stop Bits	1 and 2
Parity Type	None, Even, Odd, Mark and Space
Baud Rates	600 bps to 230400 bps

Except UART data transmission, the MA111 supports the other advanced fuction as following section:

7.1. CTS/RTS Flow Control

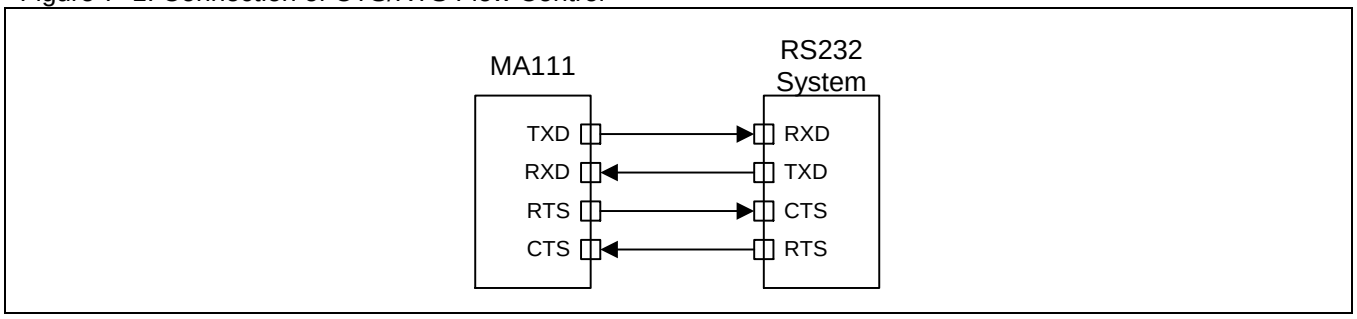
The MA111 provide the UART CTS/RTS flow control function on GPIO0 and GPIO8. If user requires the flow control function, software must enable the CTS/RTS behavior on GPIO pins.

RTS, Request To Send, is an output from the MA111 to the external UART device to indicate accepting more data or not. When the MA111's UART RX FIFO has free space, RTS output is active. If the FIFO is full, RTS output will go to inactive state.

CTS, Clear To Send, is an input to the MA111 and is an output from external UART device. When the external UART device's RX FIFO is getting full, external UART device uses this signal to indicate to the MA111. Then the MA111 will stop the TXD sending once CTS input is inactive.

Both of RTS and CTS, the signal polarity is configured by software individually. And the function is also enabled individually.

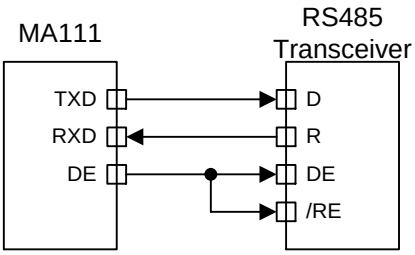
Figure 7–1. Connection of CTS/RTS Flow Control



7.2. RS-485 Transceiver DE Control

Software can configure DE output on GPIO5 to be a control input for RS-485 bus transceiver's DE and /RE. When MA111 DE output is enabled, the pin is asserted during UART TXD transmission. The DE signal polarity can be configurable by software.

Figure 7–2. Connection of RS-485 Transceiver

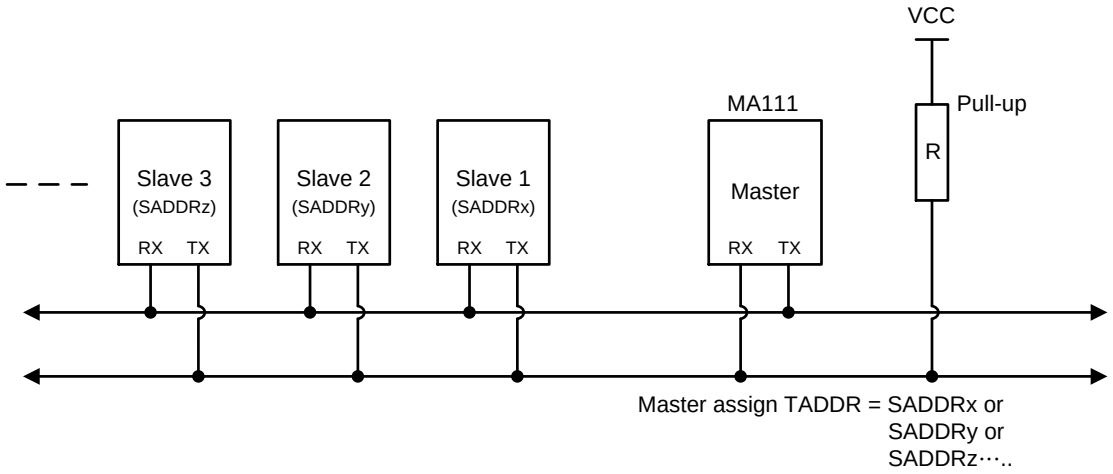


7.3. Master Mode in Multi-Processor Communication

MA111 support the UART operation in Multi-Processor communication both on master mode and slave mode. When UART master mode is enabled in MA111, software must define a Target Address (TADDR) to call a slave device to go to the communication. The TADDR can be changed by software before starting a new transaction to another slave device.

Note:
If the MA111 is applied to this operating mode, the maximum baud-rate cannot be higher than 57600.

Figure 7–3. Multi-Processor Communication of MA111 in Master Role



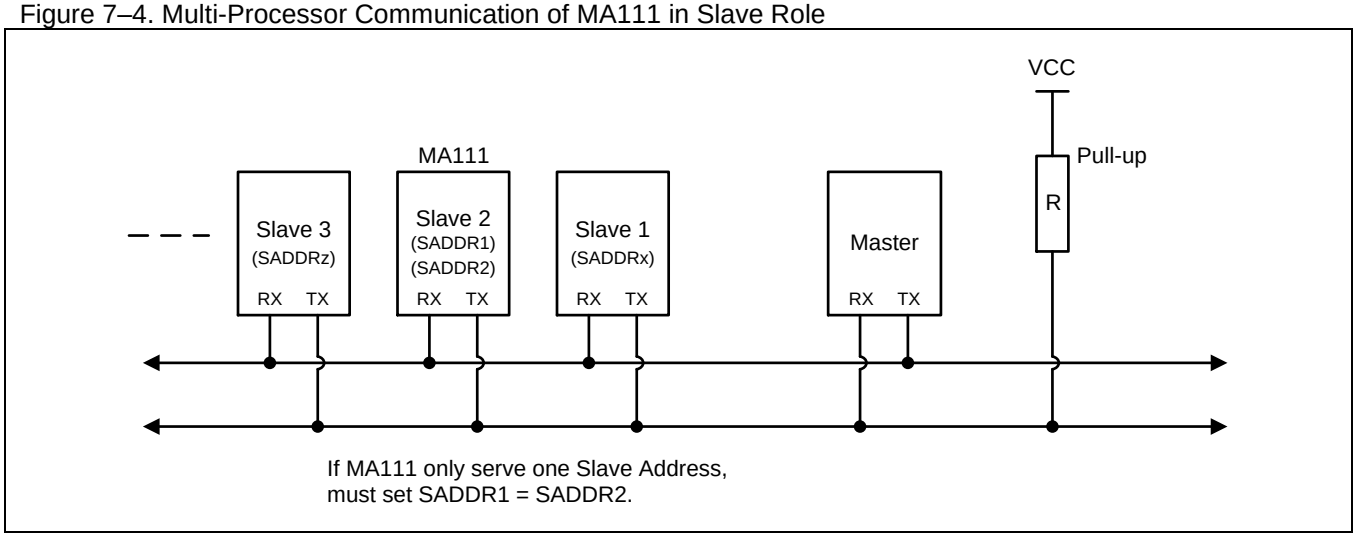
7.4. Slave Mode in Multi-Processor Communication

When the MA111 is configured to serve a slave device in Multi-Processor mode, it can recognize the UART slave address in multi-processor communication. It can recognize two different device addresses in maximum. That is, MA111 can emulate two slave devices to communicate with master device in the same time. The two slave device addresses, SADDR1 and SADDR2, are defined and changed by user software.

If there is only one slave address that the MA111 needs to service, software must set the SADDR2 to the same value with SADDR1.

Note:
If the MA111 is applied to this operating mode, the maximum baud-rate cannot be higher than 57600.

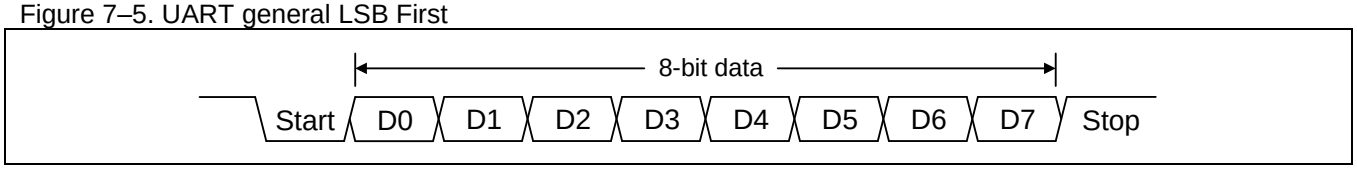
Figure 7–4. Multi-Processor Communication of MA111 in Slave Role



7.5. Bit-Order-Reversed Data Format

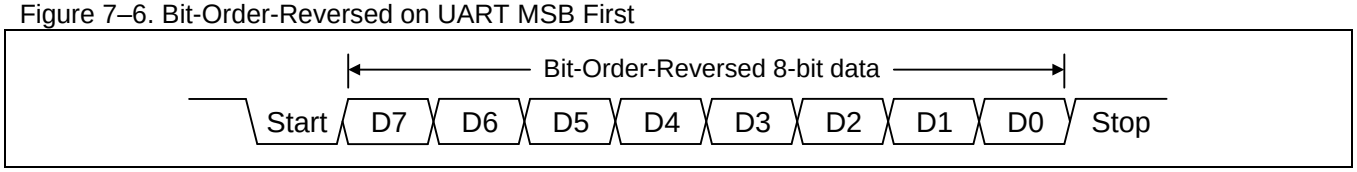
In the general UART application, the format on the UART transmission is LSB first. Figure 7–5 shows the waveform for the general LSB first.

Figure 7–5. UART general LSB First



The MA111 provides a selection for UART transmission with Bit-Order-Reversed option on MSB first format. Figure 7–6 shows the UART MSB first waveform.

Figure 7–6. Bit-Order-Reversed on UART MSB First



7.6. GPIO Setting on UART Mode

For proper operation in the MA111 UART mode, the following suggestions are the reference for user software programming.

- *Keep the default output value on the GPIO9(TXD) and as default state "1".*
- *Keep the default output value on the GPIOA(RXD) and as default state "1".*
- *Do not change the default output value("1") on the GPIO0(CTS), if CTS is enabled.*
- *Set the output value for RTS/DE inactive state on the GPIO8/5(RTS/DE), if RTS/DE is enabled.*
- *Configure the GPIO9 to push-pull output, open-drain output or open-drain output with pull-up to be TXD output pin.*
- *Configure the GPIOA to open-drain output or open-drain with pull-up to be the RXD input pin.*
- *Configure the GPIO0(CTS) to open-drain output or open-drain with pull-up to be the input pin, if necessary.*
- *Configure the GPIO8(RTS) to push-pull output, open-drain output or open-drain output with pull-up to be RTS output pin, if necessary.*
- *Configure the GPIO5(DE) to push-pull output, open-drain output or open-drain output with pull-up to be DE output pin, if necessary.*
- *If the output pin is set to open-drain output, the external pull-up resistor on the pin is necessary.*
- *Start the UART mode configuration flow and then perform the UART transfer…….*

8. SPI Master Operating Mode

When SPI Master mode is enabled in the MA111, the GPIO8, GPIO9 and GPIOA are forced to serve the SPI master MISO input, SPICLK output and MOSI output. But the port pin configuration is programmed by software. Such as, user can configure MOSI to push-pull output or open-drain output with on-chip pull-up resistor.

The MA111 SPI master engine provides a high-speed serial interface as a full-duplex and synchronous communication bus. It can operate as a master device in both 3-wire or 4-wire modes. The 4-wire mode has a output signal nSS on GPIO5 for chip select funciton on slave device. If user needs to access multiple slaves, software can configure the MA111 SPI to be 3-wire mode and control the other GPIO pins to select multiple SPI slave devices.

Table 8–1 lists the SPI function selection in MA111.

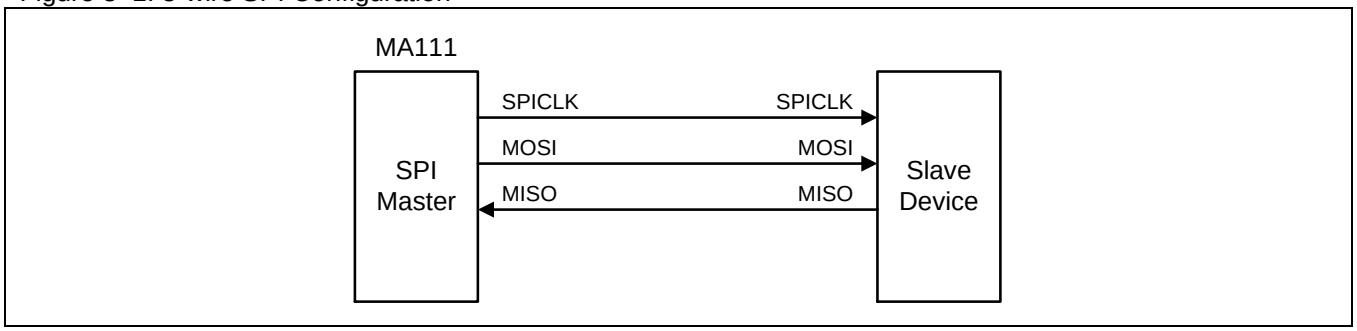
Table 8–1. SPI Data Formats and Function Selection

Item	Function Selection
Data Unit	8-bit
SPICLK	2MHz or 6MHz
Data Order	MSB first or LSB first
Operating Mode	Mode 0, 1, 2 and 3

8.1. 3-Wire SPI Configuration

The MA111 supports SPI communication on 3-wire configuration. Figure 8–1 shows the configuration on 3-wire SPI.

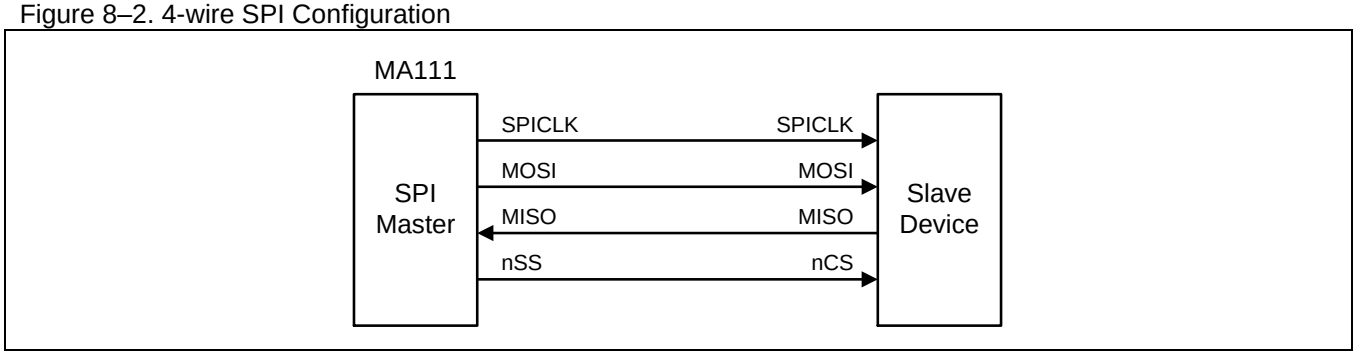
Figure 8–1. 3-wire SPI Configuration



8.2. 4-Wire SPI Configuration

The MA111 supports SPI communication on 4-wire configuration. Figure 8–2 shows the configuration on 4-wire SPI.

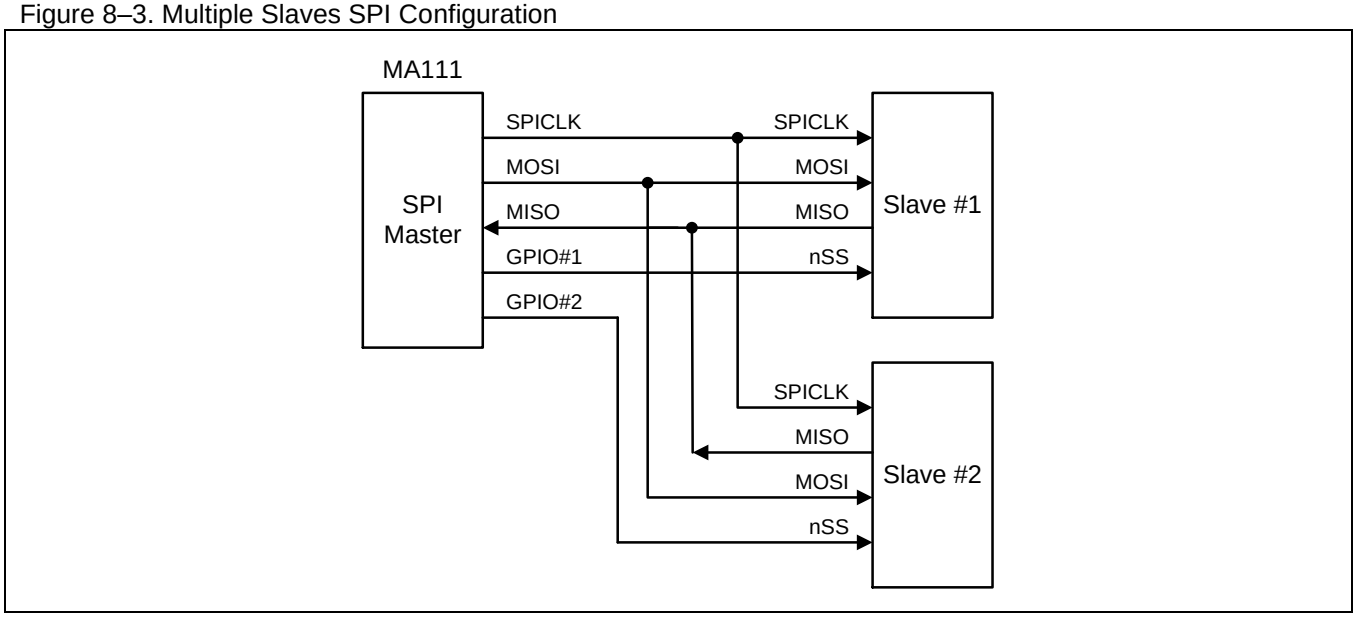
Figure 8–2. 4-wire SPI Configuration



8.3. Multiple Slaves SPI Configuration

The MA111 support the SPI communication to multiple slave devices. Software sets the MA111 to 3-wire mode and controls the different GPIO to the target slave device. Figure 8–3 shows the multiple slaves SPI configuration with the MA111.

Figure 8–3. Multiple Slaves SPI Configuration



8.4. SPI Data Mode (0/1/2/3)

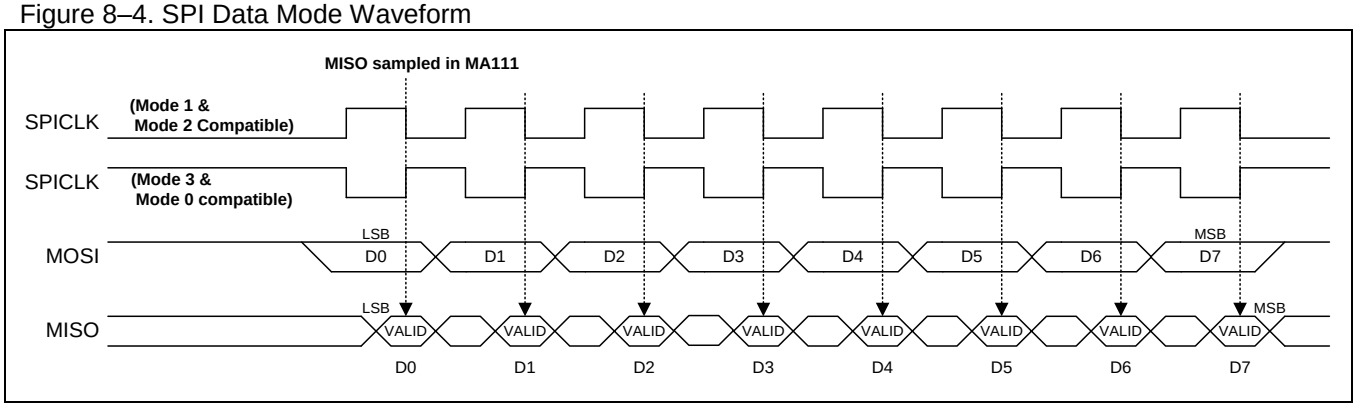
The MA111 SPI master supports SPI operating mode 0, 1, 2 and 3 for the combination of Clock Phase (CPHA) and Clock Polarity (CPOL). Table 8–2 lists the mode definition of CPHA and CPOL.

Table 8–2. SPI Mode Definition

SPI Mode	CPOL	CPHA	Leading Edge	Trailing Edge	MISO sampled in MA111
0	0	0	Sample (Rising)	Setup (Falling)	SPICLK Rising
1	0	1	Setup (Rising)	Sample (Falling)	SPICLK Falling
2	1	0	Sample (Falling)	Setup (Rising)	SPICLK Falling
3	1	1	Setup (Falling)	Sample (Rising)	SPICLK Rising

Figure 8–4 shows the MA111 SPI waveform for SPI 4 operating modes. It is a LSB first waveform and it can be applied to MSB first with the same clock state and the same sampled edge.

Figure 8–4. SPI Data Mode Waveform



8.5. GPIO Setting on SPI Mode

For proper operation in the MA111 SPI mode, the following suggestions are the reference for user software programming.

- *Keep the default output value on the GPIO8(MISO) and as default state "1".*
- *Keep the default output value on the GPIO9(SPICLK) and as default state "1".*
- *Keep the default output value on the GPIOA(MOSI) and as default state "1".*
- *Keep the default output value on the GPIO5(nSS) and as default state "1".*
- *Configure the GPIO8(MISO) to open-drain output or open-drain with pull-up to be the MISO input pin.*
- *Configure the GPIO9 to push-pull output, open-drain output or open-drain output with pull-up to be SPICLK output pin.*
- *Configure the GPIOA to push-pull output, open-drain output or open-drain output with pull-up to be MOSI output pin.*
- *Configure the GPIO5 to push-pull output, open-drain output or open-drain output with pull-up to be nSS output pin, if necessary.*
- *If the output pin is set to open-drain output, the external pull-up resistor on the pin is necessary.*
- *Start the SPI mode configuration flow and then perform the SPI transfer…….*

9. I2C Master Operating Mode

The Two-Wire serial Interface is a two-wire, bi-directional serial bus lines, one for clock (I2C_SCK) and one for data (I2C_SDA). The I2C mode in the MA111 is fully compatible to I2C bus and ***only support the one master, the MA111. The MA111 cannot support multiple masters communication on I2C bus.***

There are 4 selections for I2C clock rate in the MA111. Table 9–1 lists the I2C_SCL speed selection.

Table 9–1. I2C Clock Rate Selection

I2C_SCL Speed Selection	Typical I2C_SCL Rate
25KHz	~ 30KHz
50KHz	~ 55KHz
75KHz	~ 81KHz
100KHz	~ 111KHz

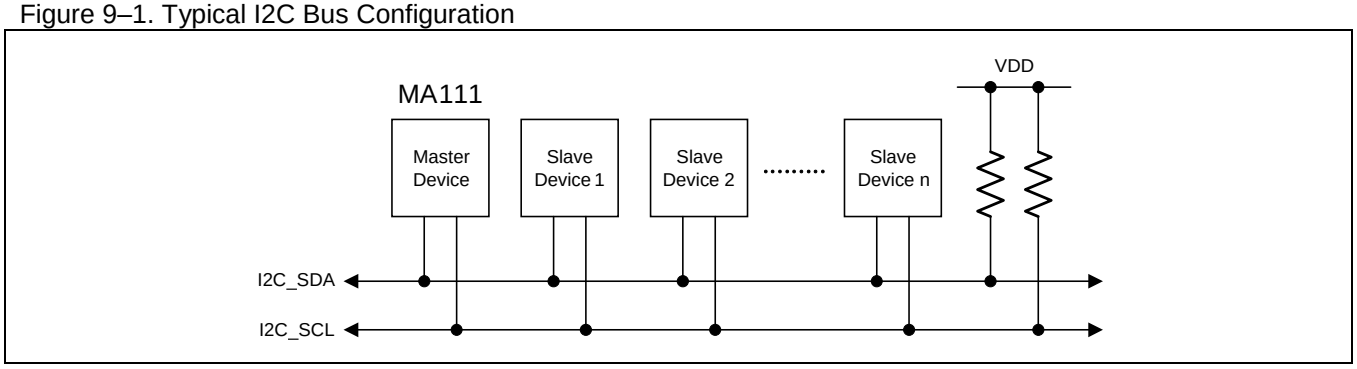
By the way, there are 8 selection for I2C_SCL timeout detection in the MA111: 20ms, 40ms, 80ms, 160ms, 320ms, 640ms, 960ms and 1280ms. The timeout selection is configured by user software. The MA111 provides 3 communication units for I2C bus transfer: sequential write, sequential read and random read.

9.1. I2C Bus Configuration

The I2C protocol allows the systems designer to interconnect up to 128 different devices using only I2C_SCL and I2C_SDA. The I2C bus provides control of I2C_SDA (serial data), I2C_SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation. The only external hardware needed to implement this bus is a single pull-up resistor for each of the I2C bus lines.

Figure 9–1 shows the typical I2C bus configuration for device connection.

Figure 9–1. Typical I2C Bus Configuration



9.2. GPIO Setting on I2C Mode

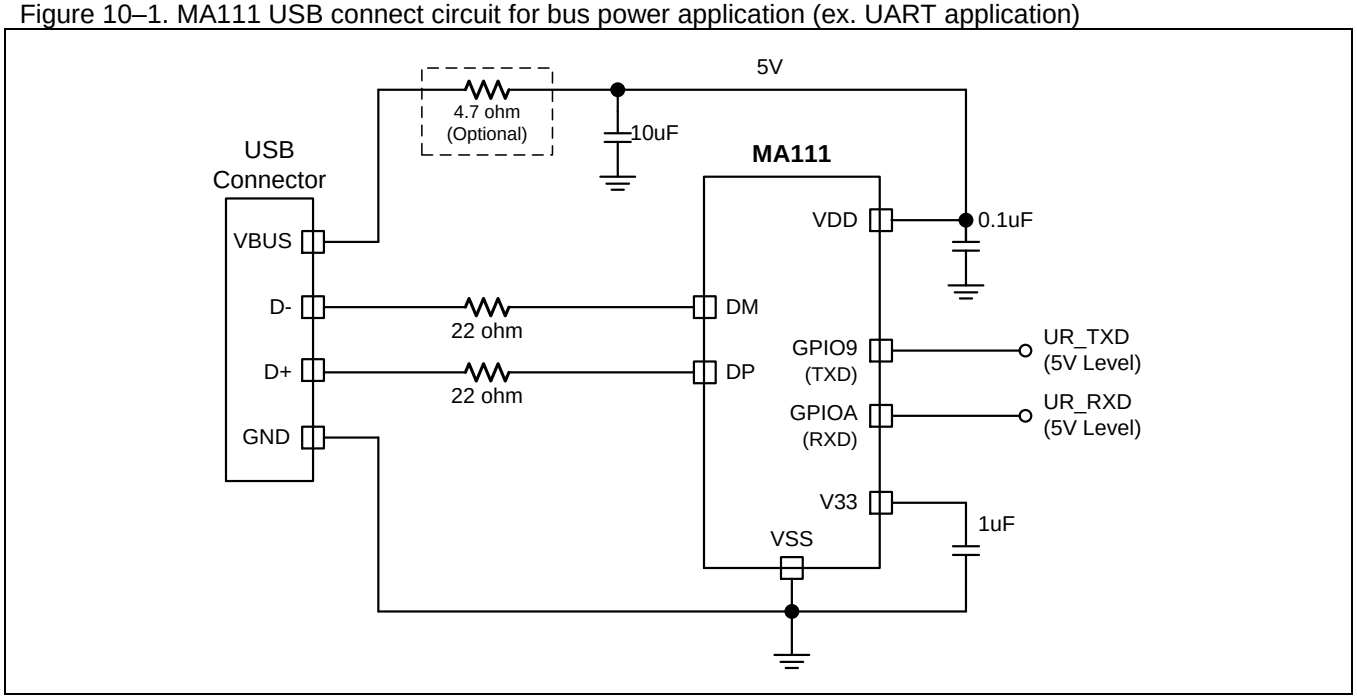
For proper operation in the MA111 I2C mode, the following suggestions are the reference for user software programming.

- *Keep the default output value on the GPIO9(I2C_SDA) and as default state "1".*
- *Keep the default output value on the GPIOA(I2C_SCL) and as default state "1".*
- *Configure the GPIO9(I2C_SDA) to open-drain output or open-drain with pull-up to be the in-out pin.*
- *Configure the GPIOA(I2C_SCL) to open-drain output or open-drain with pull-up to be the in-out pin.*
- *If the output pin is set to open-drain output, the external pull-up resistor on the pin is necessary.*
- *Start the I2C mode configuration flow and then perform the I2C transfer…….*

10. Application Notes

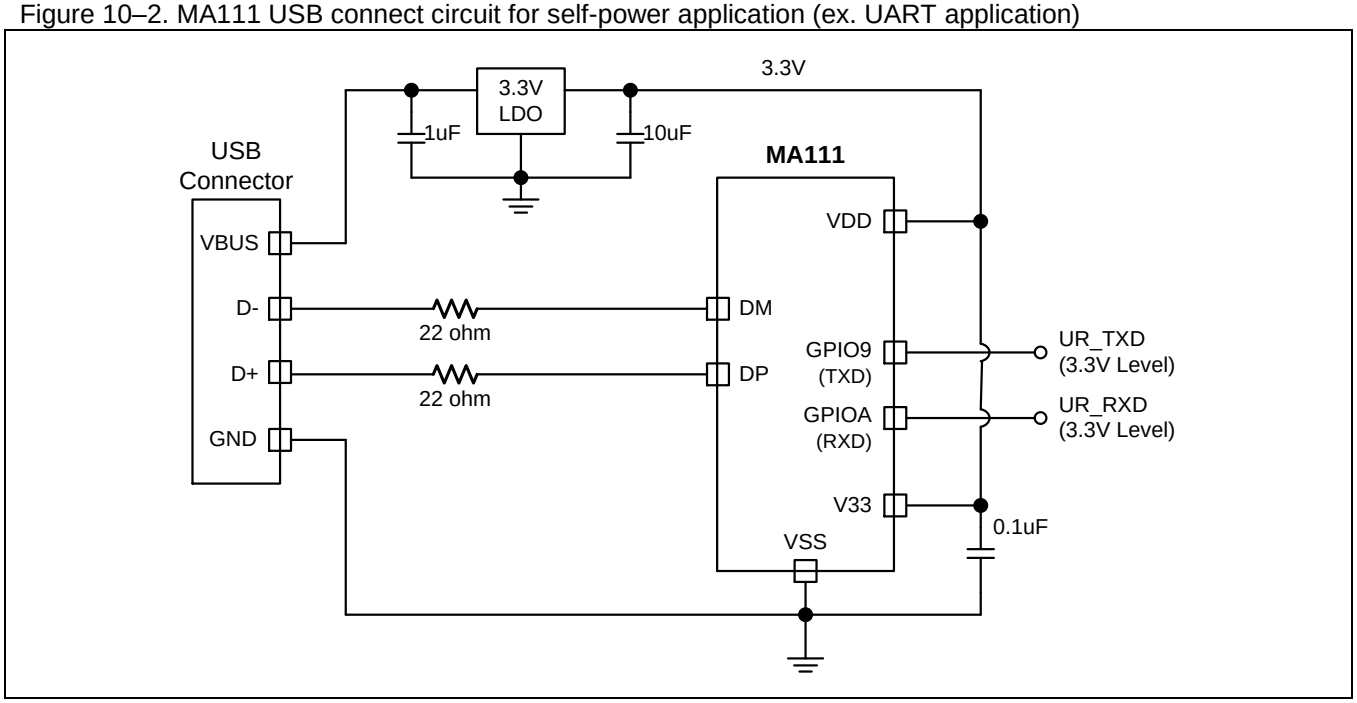
10.1. MA111 Connect for Bus Power Application

Figure 10–1. MA111 USB connect circuit for bus power application (ex. UART application)



10.2. MA111 Connect for Self-power Application

Figure 10–2. MA111 USB connect circuit for self-power application (ex. UART application)



11. Electrical Characteristics

11.1. Absolute Maximum Rating

Parameter	Rating	Unit
Ambient temperature under bias	-40 ~ +85	°C
Storage temperature	-65 ~ + 150	°C
Voltage on any Port I/O Pin with respect to VSS	-0.5 ~ VDD + 0.5	V
Voltage on VDD with respect to VSS	-0.5 ~ +6.0	V
Maximum total current through VDD and VSS	200	mA
Maximum output current sunk by any Port pin	40	mA

*Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

11.2. DC Characteristics

VDD = 5.0V±10%, VSS = 0V, T_A = 25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
Input/Output Characteristics						
V_{IH}	Input High voltage (All GPIO)		0.75			VDD
V_{IL}	Input Low voltage (All GPIO)				0.15	VDD
I_{IH}	Logic 1 input current	V_{PIN} = VDD		0	10	uA
I_{IL}	Input Low leakage current (All GPIO in digital input)	V_{PIN} = VSS		0	10	uA
I_{H2L}	Logic 1 to 0 transition current (All inputs with on-chip pull-up resistor)	V_{PIN} = V_{H2L}		330	500	uA
I_{OH}	Output High current (All push-pull output ports)	V_{PIN} =2.4V	12			mA
I_{OL}	Output Low current (All I/O Ports)	V_{PIN} =0.4V	12			mA
R_{ph1}	Weak pull-high resistor (All I/O Ports)	V_{PIN}=2V		10		Kohm
R_{ph2}	Very weak pull-high resistor (All I/O Ports)	V_{PIN}=0V		260		Kohm
Power Consumption						
I_{OP1}	Normal mode operating current	USB Connected No load on GPIO		5.6		mA
I_{PD1}	Power down mode current	USB Connected		256	500	uA
Operating Condition						
V_{PSR}	Power-on Slop Rate	T_A = -40°C to +85°C	0.05			V/ms
V_{POR}	Power-on Reset Valid Voltage	T_A = -40°C to +85°C			0.1	V

(1) Data based on characterization results, not tested in production.

11.3. USB Transceiver Electrical Characteristics

VDD = 4.0V ~ 5.5V, VSS = 0V, T_A = 25°C, unless otherwise specified

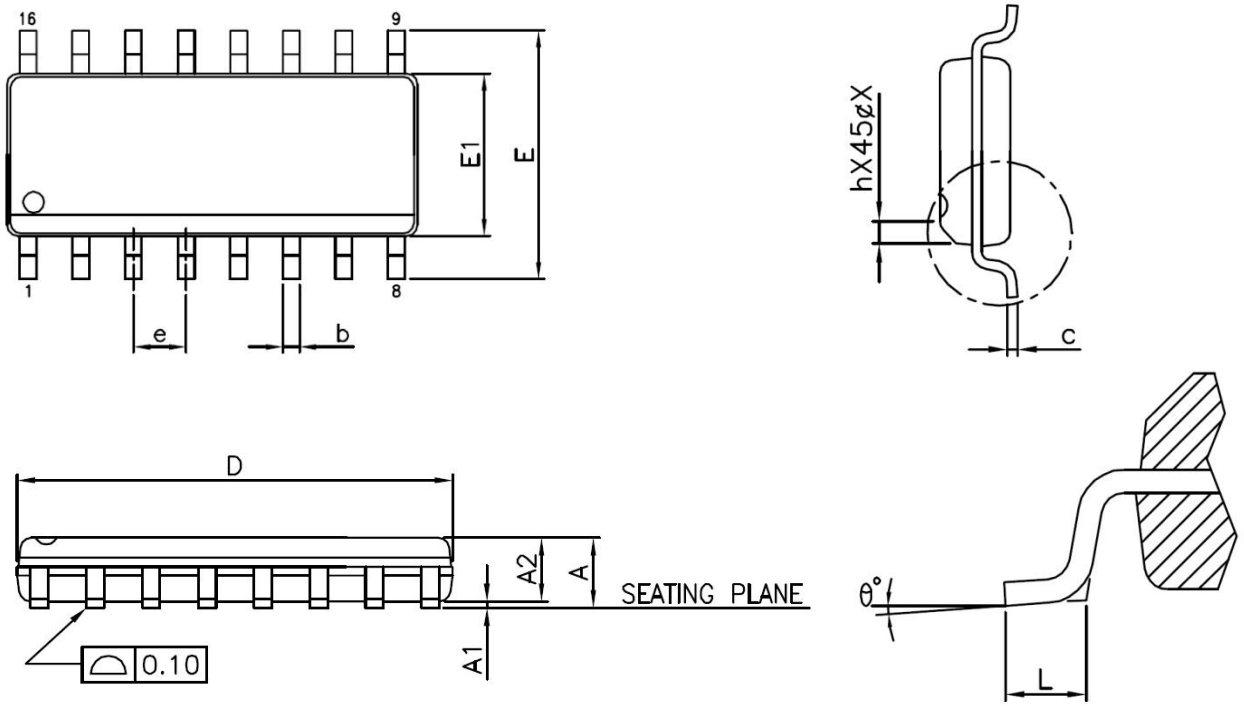
Symbol	Parameter	Test Condition	Limits			Unit
			min	typ	max	
V_{V33}	3.3V regulator output voltage	T_A = 25°C	3.0	3.3	3.6	V
I_{V33}	Regulator Output drive current	T_A = 25°C			35	mA
R_{PU}	Pull-Up Resistance	On DP	0.95	1.1	1.3	Kohm
Transmitter						
V_{OH}	Output High Voltage		2.8			V
V_{OL}	Output Low Voltage				0.8	V
V_{CRS}	Output Cross Over point		1.3		2.0	V
Z_{DRVH}	Output Impedance on Driving High		28		44	Ohm
Z_{DRVL}	Output Impedance on Driving Low		28		44	Ohm
T_R	Output Rise Time		4		20	ns
T_F	Output Fall Time		4		20	ns
Receiver						
V_{DI}	Differential Input Sensitivity	| DP – DM |	0.2			V
V_{CM}	Differential Input Common Mode Range		0.8		2.5	V
I_L	Input Leakage current	Pull-up Disabled		<1.0		uA

(1) Data based on characterization results, not tested in production.

12. Package Dimension

12.1. SOP-16 (150mil)

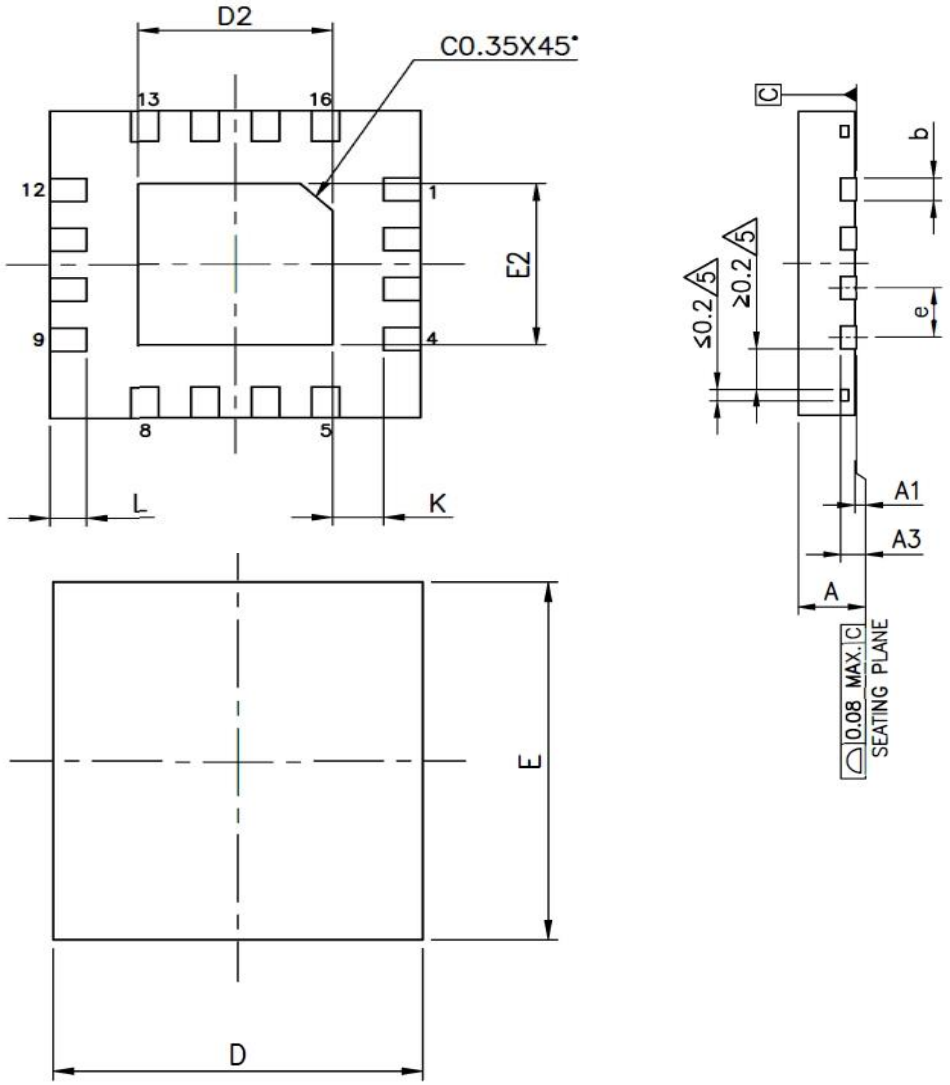
Figure 12–1. SOP-16(150mil)



Unit	mm		Inch	
Symbols mm	Min.	Max.	Min.	Max.
A	----	1.75	----	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	----	0.049	----
b	0.31	0.51	0.012	0.020
c	0.10	0.25	0.004	0.010
D	9.90 BSC		0.390 BSC	
E	6.00 BSC		0.236BSC	
E1	3.90 BSC		0.154BSC	
e	1.27 BSC		0.050BSC	
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.010	0.020
θ°	0°	8°	0°	8°

12.2. QFN-16 (4x4mm)

Figure 12–2. QFN-16 (4x4mm)



Unit	mm			inch		
JEDEC	MO-220					
PKG	WQFN(X416)					
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF.			0.008 REF.		
b	0.25	0.30	0.35	0.01	0.012	0.014
D	4.00 BSC			0.157 BSC		
D2	2.00	2.10	2.15	0.079	0.083	0.085
E	4.00 BSC			0.157BSC		
E2	2.00	2.10	2.15	0.079	0.083	0.085
E	0.65 BSC			0.026 BSC		
L	0.50	0.55	0.60	0.020	0.022	0.024
K	0.20	---	----	0.008	----	---

13. Revision History

Table 13–1. Revision History

Rev	Descriptions	Date
v0.86	Preliminary version release.	2017/11/15
v0.87	1. Update USB connect circuit in Section 10.	2018/11/26
	2. Update Package diagrams in Section 3.1.	2018/11/27
	3. Update power down mode current in Section 11.2	2018/11/27
	4. Add Block Diagram including SPI & TWI module.	2018/11/27
	5. Add function description for SPI & TWI.	2018/11/27
	6. Add GPIO setting reference on UART/SPI/TWI mode.	2018/11/27
	7. Add the diagrams for open-drain with pull-up and quasi-bidirectional GPIO.	2018/11/27
V0.88	1. Modify GPIO general description from 10 to 11	2019/08/09
	2. Fixed GPIO for UART software programming description – Configure the GPIO0(RTS) to GPIO8(RTS) and TXD to RTS.	2019/08/09
	3. Fixed GPIO for UART software programming description – Configure the GPIO0(DE) to GPIO5(RTS) and TXD to DE.	2019/08/09
V0.89	1. Modify “TWI” string to “I2C”	2022/10/18

14. Disclaimers

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