MA853

One Hall for 3 phase brushless DC motor controller

Data Sheet

Version: 0.3

Features

MA853 is SIP chip, which has dual core (Arm® Cortex®-M0/ MCU and hardware motor controller/MCD) for 3 phase brushless DC motor controller with one hall sensor. Available in QFN32 (4x4x0.85mm) package.

MCU

- Cortex®-M0, frequency up to 48MHz.
- Memory (16KB embedded Flash storage and 2KB SRAM.)
- Built-in 48MHz HSI high-speed oscillator.
- Multiple low power modes include Sleep mode, Stop mode and Deep Stop mode.
- 5 timers:
  - One 16-bit 4-channel advanced timer (TIM1), capable of generating four PWM outputs or three complementary PWM pairs, support center- or edge-aligned PWM mode, support hardware dead time insertion and fault brake, support PWM phase-shift output mode.
  - One 16-bit 4-channel general purpose timer (TIM3), capable of generating four PWM outputs or capture four channel input signals, support decode of hall sensor and quadrature encoder, support infrared decode.
  - One 16-bit basic timer (TIM14), capable of generating one PWM output or capture one channel input signal.
  - One watchdog timer equipped with independent clock source (IWDG).
  - One 24-bit Systick timer.
- Up to **10** fast I/O ports:
  - All I/O ports can be mapped to 10 external interrupts.
  - All I/O ports can accept input or generate output signal voltage level is not higher than V_{DD}.
- One USART1.
- One 12-bit ADC (Analog-to-Digital converter) supports 1M SPS conversion rate, with 8 external inputs and 1 internal input that can sample on-chip voltage sensor.
- Embedded CRC engine
- Serial Wire Debug (SWD) for debug function.
- Operating temperature range includes -40°C ~ 105°C industrial tier.

MCD

- 1-Hall sine wave PWM drive
- Pre-driver for external N-ch MOSFET
- Closed loop speed control, configurable speed curve
- Adjustable driving current for the gate of external MOSFET
- Operating voltage range: 5 to 16 V
- Serial interface
- Standby mode
- Soft start
- Output RPM information
- Built-in protection features:
  Under Voltage Lock Out (UVLO), Under voltage protection for the charge pump,
  Over Voltage Protection (OVP), Lock detection, Thermal Shutdown (TSD),

Over Current limitation (OCL), Over current protection (ISD)

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1 Introduction

1.1 Overview

The MA853 has dual core (Arm® Cortex®-M0/MCU and hardware motor controller/MCD) for 3 phase brushless DC motor controller. The MCD can be operated by 1-Hall sine-wave commutation and 1-Hall 150° commutation. Also, a closed loop speed control function is implemented without using an external microcontroller. Motor rotation speed can be controlled by inputting PWM signal or applying analog voltage to the SPD pin. The operation moves to the standby mode when a zero cross of the Hall signal is not detected for a lock detection period after the voltage of VSTBY(L) or less is applied to the SPD pin. In the standby mode, the IC power consumption is reduced by powering off its internal 5-V regulator. In case that the Hall element is power supplied by the IC's 5-V regulator, the power consumption of the whole motor system can be reduced. In case that motor is configured as not stop when the voltage of SPD pin is VSTBY(L) or less, standby mode is disabled.

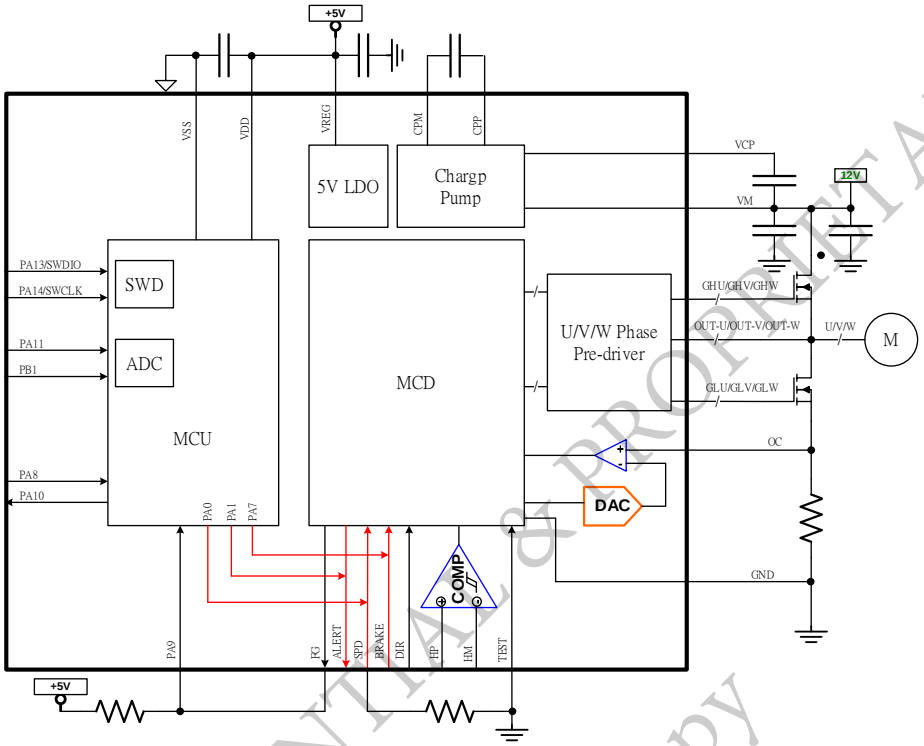
The MCU has a maximum clocked frequency of 48MHz, built-in 16KB Flash storage, and contains an extensive range of peripherals and I/O ports. It contains one 12-bit ADC, one 16-bit advanced timer, one 16-bit general purpose timer and one 16-bit basic timer, as well as communication interface including one USART. The operating voltage of MCU is 2.0V to 5.5V, and the operating temperature range (ambient temperature) is -40°C to 105°C extended industrial tier.

MA853 has dual cores, MCD and MCU. The MCD core can run motor control well. And the MCU has more I/O for the flex control behaviors and can assist MCD in more themes. This device is available in QFN32 (4x4x0.85 mm).

2 Function Introduction

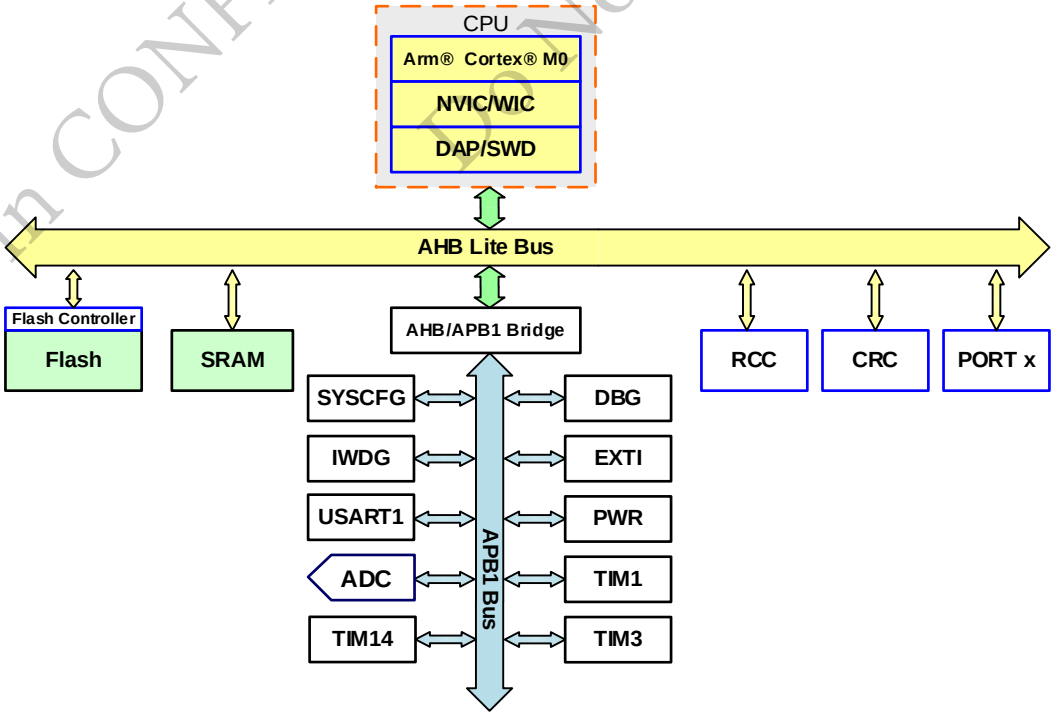
2.1 Function Block diagram

Figure 2-1 Function Block Diagram



2.2 MCU Block diagram

Figure 2-2 MCU Block Diagram



2.3 MCU Core introduction

The Arm® Cortex®-M0 processor provides real-time processing and advanced interrupt handling system, which is perfect for cost-effective and low-pin-count microcontrollers targeting real-time control and low power applications.

The Arm® Cortex®-M0 is a 32-bit RISC processor, provides state-of-the-art code efficiency, which is extremely suitable for small memory size microcontrollers and small code size applications.

2.4 Flash

This product provides up to 16KB embedded Flash memory available for storing code and data.

2.5 SRAM

This product provides up to 2KB embedded SRAM.

2.6 Voltage regulator

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that used by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

2.7 Power supply supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enabled.

2.8 Timers and watchdogs

This product has one advanced timer, one general purpose timer, one basic timer, one watchdog timer and one Systick timer. The table below compares the features of advanced, general purpose and basic timers.

Table 2-1 Feature summary of advanced, general purpose and basic timers

Type	Instance	Resolution	Counter direction	pre-divider	DMA request	Capture/compare channels	Complementary output
Advanced	TIM1	16-bit	up, down, up/down	1 to 65536	No	4 (no capture)	3
General purpose	TIM3	16-bit	up, down, up/down	1 to 65536	No	4	No
Basic	TIM14	16-bit	up	1 to 65536	No	1	No

Advanced timer (TIM1)

The advanced timer includes a 16-bit counter, four capture/compare channels and three phases complementary PWM generator. This timer supports hardware dead-time insertion when using as complementary PWM generator. This timer can also be used as a full-function general purpose timer. This timer has four independent channels, each channel can be used for:

- Output compare
- PWM generator (center- or edge-aligned)

- Single pulse output

When this timer is used as a general-purpose timer, it has the same function as the TIM2. When this timer is used as a 16-bit PWM generator, it can be configured to a broad duty cycle range from 0% to 100%.

In debug mode, the counter can be frozen.

The advanced timer has lots of identical features and internal structures as the general-purpose timer, in this way the advanced timer can work together with the general-purpose timer through the link function, to provide synchronization and event trigger function.

General-purpose timer (TIM3)

This product has one general-purpose timer (TIM3). The timer has a 16-bit counter, support both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output. These general-purpose timers can also work together through the timer link function, to provide synchronization between timers and event trigger function.

These timers can also be used to decode incremental encoder signals and can also be used to decode one to four Hall sensors' digital output. Any general-purpose timer can be used to generate PWM output or work as basic timer.

In debug mode, the counter can be frozen.

Basic timer (TIM14)

This product has one 16-bit basic timer (TIM14). Each timer has one 16-bit counter, supporting only up counting, with automatically reload. The timer also has one 16-bit frequency pre-divider and one independent channel. Each channel can be used as input capture, output compare, PWM or one pulse mode output.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 40KHz oscillator. As it is independent of the main clock, it can run in shutdown and standby modes. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter can be frozen.

System tick timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a general down counter. It has the following features:

- 24-bit down counter
- Auto-reload capability
- A makeable interrupt can be generated when counter value is 0
- Programmable clock source

2.9 GPIO

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripherals function port. Most GPIO pins are shared with digital or analog functions.

If necessary, the peripheral functions of the I/O pins can be locked by specific operation to avoid accidental writing to the I/O register.

2.10 USART

This product has one Universal Synchronous/Asynchronous Receiver/Transmitter (USART) interfaces. The USART provides flexibility for full-duplex data exchange with peripherals using the industry standard NRZ asynchronous serial data format. This module can support a wide range of baud rates through the integrated baud rate generator (including integer and fraction settings). Support LSB or MSB receive/transmit mode. Support 8- or 9-bit programmable data length. Support 0.5-/1-/1.5-/2-bit stop bit configuration. The USART can support synchronous or asynchronous one-way communication and half-duplex single-wire communication. Support maximum 6Mbps baud rate.

2.11 ADC

This product has one 12-bit analog/digital converter (ADC), support up to 1Msps conversion rate, with up to two external channels and one internal channel available. Support single-shot single-cycle and continuous scan conversion. Support any sequence sampling mode, the sampling channels can be sequenced in any order. One internal channel is used to sample the built-in voltage reference, and in application the voltage level of the chip power supply can be derived from the sampled conversion value.

The analog watchdog function allows the application to monitor one or all selected channels. When the monitored signal exceeds a preset threshold, an interrupt will be generated.

The triggers generated by the general-purpose timers and the advanced timers can be selected to trigger the ADC sampling, in this way the ADC sampling can be synchronized with the timer.

2.12 CRC

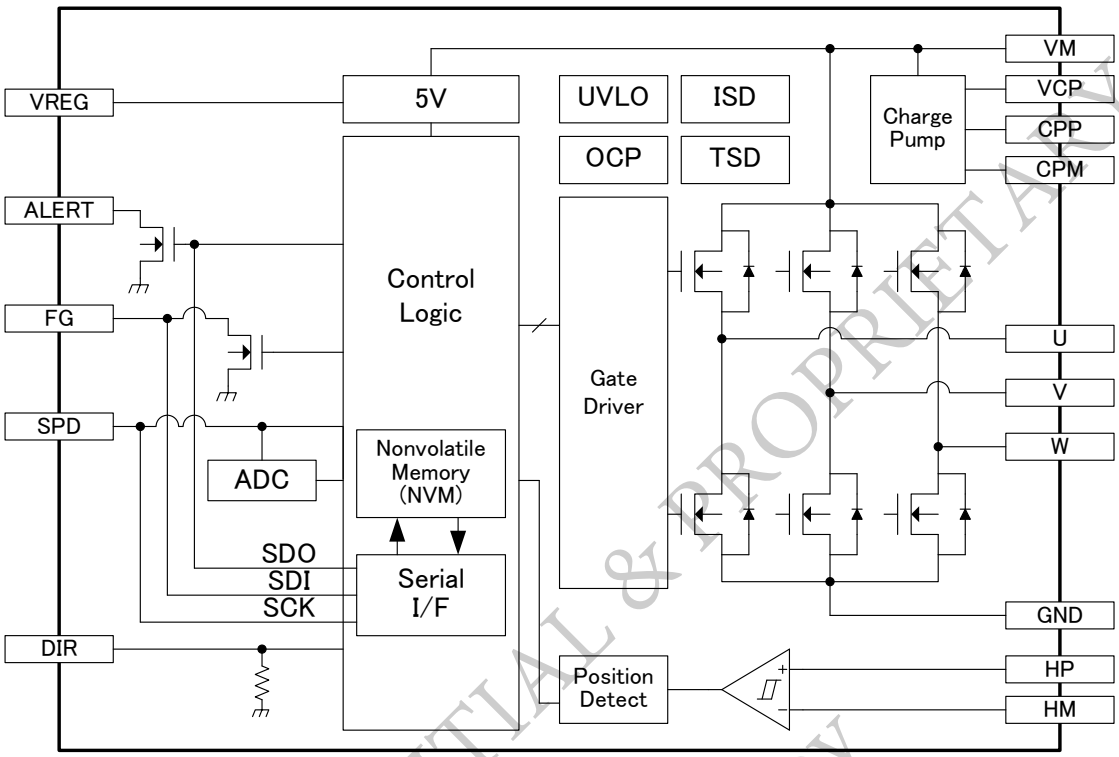
The cyclic redundancy check (CRC) module uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. Among many applications, CRC is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a method to detect flash memory errors. The CRC module can be used to calculate the signature of the software package in real time and compare it with the signature generated when the software is linked and generated.

2.13 SWD

This product equips ARM standard Serial Wire Debug (SWD).

2.14 MCD Block diagram

Figure 2-3 MCD Block Diagram

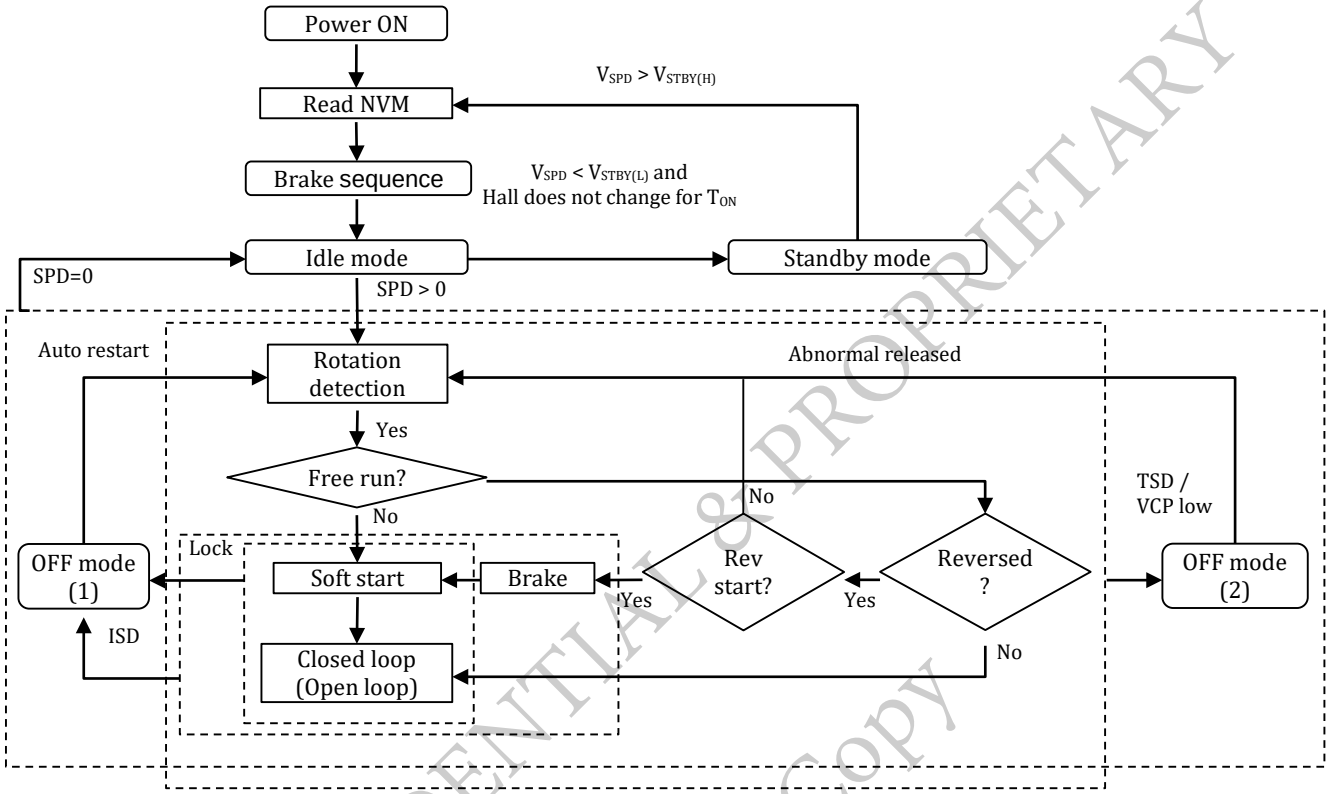


2.15 MCD introduction

MCD can be operated by 1-Hall sine-wave commutation and 1-Hall 150° commutation. Also, a closed loop speed control function is implemented without using an external microcontroller. Motor rotation speed can be controlled by inputting PWM signal or applying analog voltage to the SPD pin.

The operation moves to the standby mode when a zero cross of the Hall signal is not detected for a lock detection period after the voltage of $V_{STBY(L)}$ or less is applied to the SPD pin. In the standby mode, the IC power consumption is reduced by powering off its internal 5 V regulator. In case that the Hall element is power supplied by the IC's 5 V regulator, the power consumption of the whole motor system can be reduced. In case that motor is configured as not stop when the voltage of SPD pin is $V_{STBY(L)}$ or less, standby mode is disabled.

Figure 2-4 Basic operation flow chart



2.15.1 MCD status

Table 2-2 MCD status in each mode

		Read NVM	Stop mode	OFF mode (1)	OFF mode (2)	Standby mode	Normal mode
VREG		5V	5V	5V	5V	OFF	5V
Charge pump		Active	Active	Active	Active	Inactive	Active
FG function	FG	During reading: L After reading: Hi-Z	Hall output (Hi-Z under 1Hz)	Hi-Z	Hall output (Hi-Z under 1Hz)	Hi-Z	Hall output (Hi-Z under 1Hz)
	RDO		State sustaining	State sustaining	State sustaining	Hi-Z	Lock is detected: L Lock is released: Hi-Z
ALERT		Hi-Z	State sustaining (Note 1)	L (Note 3)	L (Note 3)	Hi-Z	Fault (Note 2) is detected: L (Note 3) Fault is released: Hi-Z
GLx (x: U, V, W) GHx (x: U, V, W)		L	L	L	L	Hi-Z	Active

Note 1: ALERT = L when TSD / VCP is dropped. ALERT is released when the cause of fault is released.
Note 2: Fault means ISD / TSD / VCP dropping and lock.
Note 3: When ALERTINV = 0. ALERT outputs H level when ALERTINV = 1.

2.15.2 1-Hall commutation

MCD can be operated by 1-Hall sine-wave commutation and 1-Hall 150° commutation.
The type of commutation can be switched by register.
Rotation direction is defined by DIR and register setting.

Figure 2-5 Timing chart of Hall input signal and sine-wave commutation signal

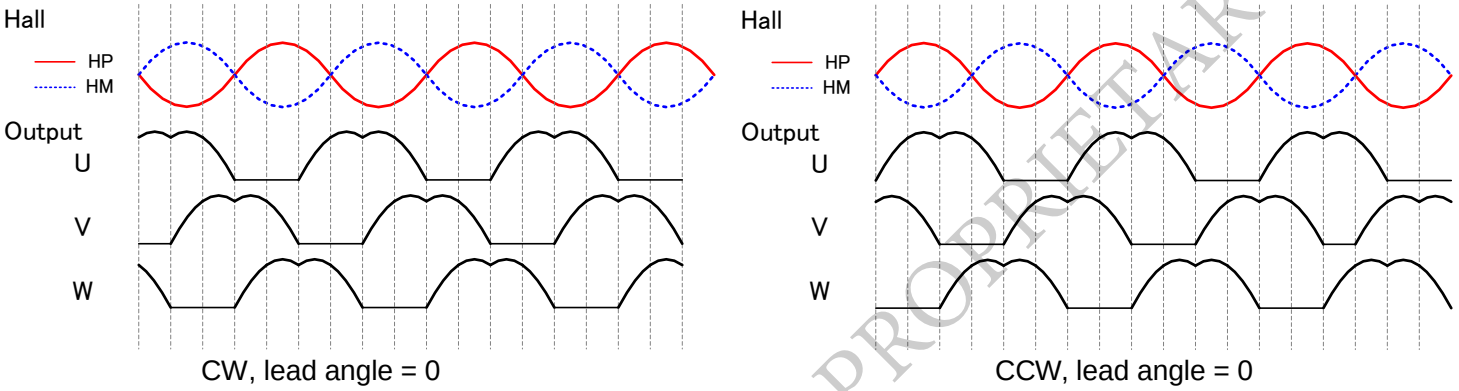
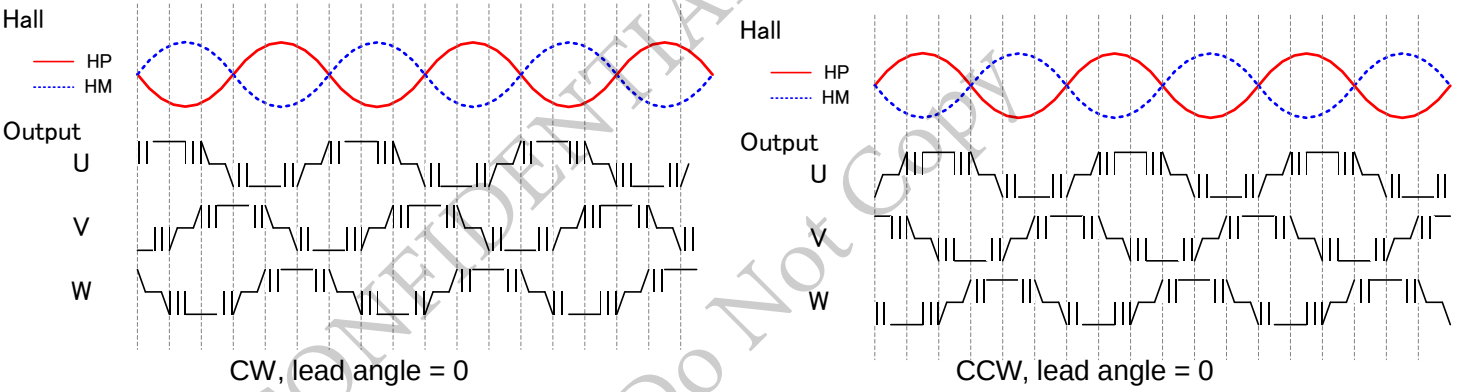


Figure 2-6 Timing chart of Hall input and 150° commutation signal



2.15.3 PWM frequency

PWM is generated from internal oscillator.

Table 2-3 Division ratio vs PWM frequency

Division ratio	PWM frequency
512	23.4kHz
256	46.9kHz
128	93.7kHz
64	187.5kHz

Table 2-4 The setting of PWM frequency

PWMSEL [2:0]			f_{hall}					
			0 to 250 150 to 0	250 to 500 400 to 150	500 to 1000 900 to 400	1000 to 1500 1400 to 900	1500 to 2000 1900 to 1400	Over 2000 Under 1900
0	0	0	23.4kHz					
0	0	1	46.9kHz					
0	1	0	93.7kHz					
0	1	1	187.5kHz					
1	0	0	23.4kHz	23.4kHz	46.9kHz	46.9kHz	93.7kHz	93.7kHz
1	0	1	23.4kHz	46.9kHz	46.9kHz	93.7kHz	93.7kHz	187.5kHz
1	1	0	23.4kHz	46.9kHz	93.7kHz	93.7kHz	187.5kHz	187.5kHz
1	1	1	46.9kHz	93.7kHz	93.7kHz	187.5kHz	187.5kHz	187.5kHz

Note: There is a 100Hz hysteresis when the motor decreases its speed.

2.15.4 Lead angle control

MCD contains the function of lead angle control.

This function requires a Hall signal to compensate the lead angle with the setting of LATABLE.

Table 2-5 Table of LATABLE

LATABLE [4:0]					The value of lead angle
0	0	0	0	0	LATABLE = 0 to 27 Lead angle (deg) = 1.875 (deg) x Speed (RPM) / 4096 x LATABLE Maximum lead angle is 58.125°
……					
1	1	0	1	1	
1	1	1	0	0	7.5° fixed
1	1	1	0	1	15° fixed
1	1	1	1	0	22.5° fixed
1	1	1	1	1	30° fixed

Figure 2-7 Example of the setting of lead angle LATABLE = 14 (1b01110)

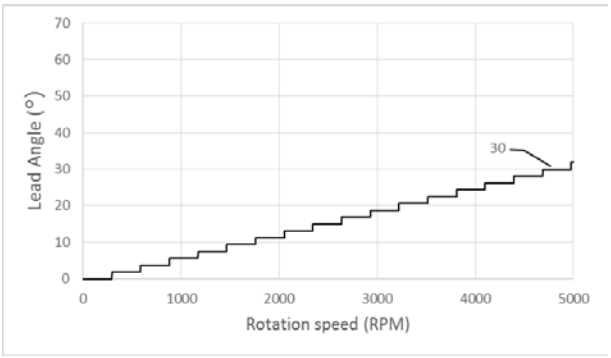
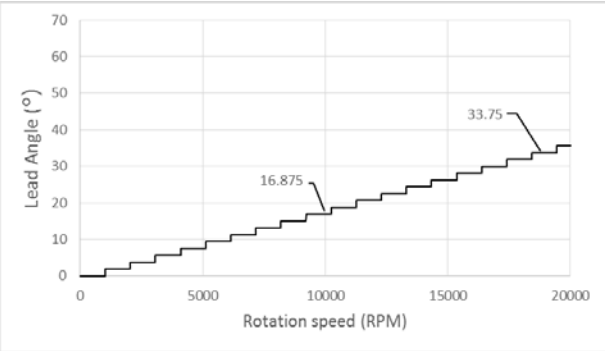


Figure 2-8 Example of the setting of lead angle LATABLE = 4 (1b00100)



This IC features Intelligent Phase control (InPAC), which can automatically optimize lead angle by comparing the zero-cross timing of the hall signal with the zero-cross timing of the motor current.

Table 2-6 The setting of controlling lead angle

LASEL	Auto
0	InPAC enable
1	InPAC disable

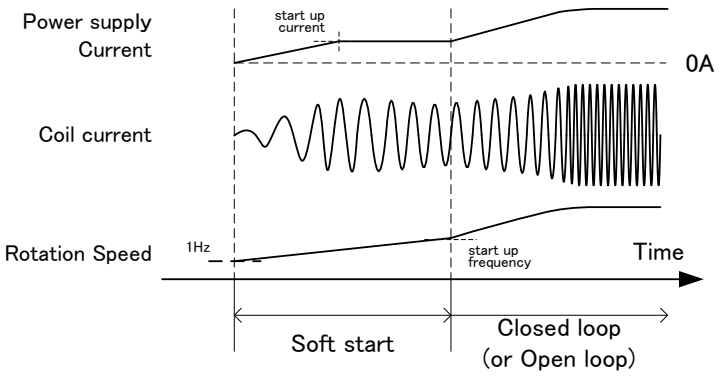
InPAC is enabled when LASEL=0.
Lead angle=Optimized lead angle by InPAC + lead angle set in LATABLE
Since a low motor current in low speed makes a difficulty of detecting zero cross, InPAC regards an optimized lead angle is zero when the motor speed becomes under startup frequency.

When LASEL=1, InPAC is disabled, and an optimized lead angle is zero.

2.15.5 Soft Start

Soft start operates when the motor starts from the stop state to prevent rush current.

Figure 2-9 Timing chart of soft start



Soft start increases the output duty gradually from 0 % until the output current reaches the startup current.
The rotation frequency increases from 1 Hz.
Soft start is finished and switches to the closed loop speed control or the open loop speed control when the rotation frequency reaches the switching frequency (startup frequency).
The way of commutation is defined by register setting.

The time for lock detecting in soft start can be selected by register setting so that slow start motor can be used.

Table 2-7 The setting of the time for lock detecting in soft start

SS_LOCK	The time for lock detecting (s)
0	TON x 1
1	TON x 5

2.15.6 Acceleration and deceleration control

Acceleration and deceleration rate of motor can be controlled by limiting of PWM duty.

Table 2-8 Acceleration and deceleration rate

Duty change limit (DUTYCHGLIMIT)	Variation amount of duty every 2.7ms (Δ/512)	Time (sec) from 0% to 100%
0	N/A (64/8)	0.17
1	2/8	5.53
2	3/8	3.69
3	4/8	2.76
4	6/8	1.84
5	10/8	1.11
6	20/8	0.55
7	56/8	0.20

Figure 2-10 Example of DUTYCHGLIMIT = 2

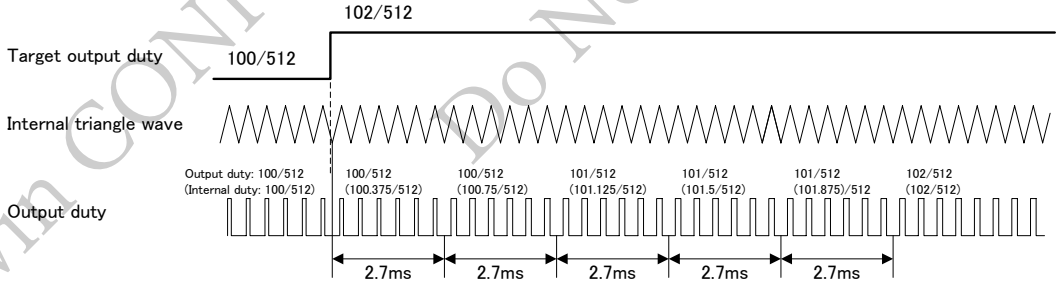


Table 2-9 Acceleration and deceleration control

Item	Soft start	Closed loop			Open loop	Mild brake	Reverse brake
		Acceleration	Steady	Deceleration			
Period of changing duty	2.7 ms	10.8 or 2.7 ms	2.7 ms		10.8 or 2.7 ms	10.8 or 2.7 ms	10.8 or 2.7 ms
Variation amount of duty	Duty chg limit for soft start	Duty chg limit	Determined by PI (Maximum variation amount is Duty chg limit)		Duty chg limit	Duty chg limit	Duty chg limit

2.15.7 Output current for the gate of external MOSFET

MCD drives external MOSFETs. This IC contains six half bridge pre-drivers and drives high-side and low-side Nch-MOSFETs. The voltage for high-side gate of MOSFET is V_M + 8V(typ.). The voltage for low-side gate of MOSFET is 8 V(typ.). The register, ISOURCE_SEL、ISINK_SEL set a driving current to the gate.

Table 2-10 Setting of source current for MOSFET

ISOURCE_SEL [2:0]	Source current (mA)
000	10.0
001	13.9
010	19.3
011	26.8
100	37.3
101	51.8
110	72.0
111	100.0

Table 2-11 Setting of sink current for MOSFET

ISINK_SEL [2:0]	Sink current (mA)
000	20.0
001	27.8
010	38.6
011	53.7
100	74.6
101	103.6
110	143.9
111	200.0

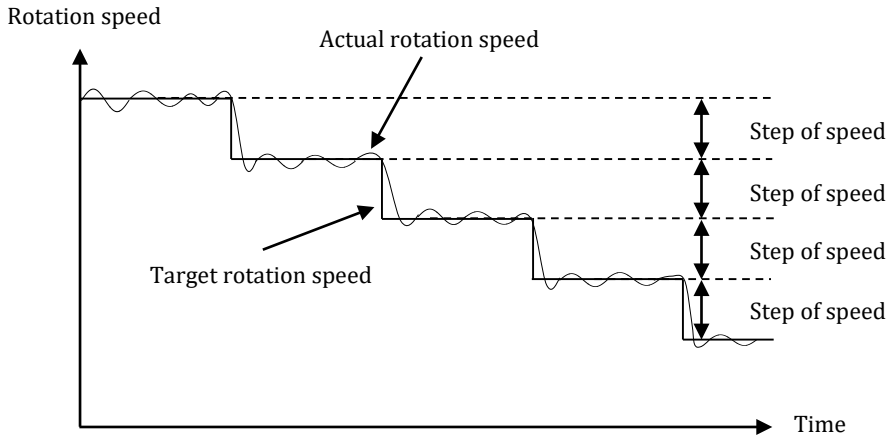
2.15.8 Limitation of step of reducing rotation speed

Limiting the step of reducing rotation speed, motor locking can be avoided.

Table 2-12 The setting of step of speed

RPMLIMIT[2:0]	Step of speed(rpm)
000	No limit
001	512
010	2200
011	3800
100	5400
101	7000
110	8600
111	10240

Figure 2-11 Diagram of reaching a target speed



2.16 MCD Input / Output Signals

2.16.1 SPD

SPD pin controls the motor start, the motor stop, and the rotation speed.
PWM duty signal input or analog voltage signal input can be configured by the register. Also, the polarity of the signal can be configured by the register.

Table 2-13 Polarity of SPD

	Positive logic (Default)	Negative logic
Analog voltage input	$V_{VSP(L)}$: SPD command = 0 (0%) $V_{VSP(H)}$: SPD command = 512(100%)	$V_{VSP(L)}$: SPD command = 512 (100%) $V_{VSP(H)}$: SPD command = 0 (0%)
PWM duty input	H active	L active (Note 1)

Note 1: The polarity of the input signal is inverted inside the IC, and the inverted signal is used as the positive logic SPD.

In case of analog voltage input, the resolution is 9-bit in the voltage range of $V_{VSP(L)}$ to $V_{VSP(H)}$.
In case of PWM duty input, its frequency range is from 1 kHz to 100 kHz. When the frequency range is from 1 kHz to 20 kHz, the resolution is 9-bit. And when it is 20 kHz or more, the resolution decreases. For example, in case of 40 kHz, the resolution is 8-bit, and in case of 100 kHz, it becomes 7-bit.
In addition, the SPD pin can be also used as the clock input pin for the serial interface (for SCK signal).

2.16.2 DIR

DIR pin controls the motor rotation direction; forward rotation (CW) and reverse rotation (CCW).
Relation of DIR pin polarity and the rotation direction is configured by the register.

Table 2-14 The relation of register and DIR

Register (DIR)	DIR pin	Rotation direction
0	L	CW
	H	CCW
1	L	CCW
	H	CW

2.16.3 ALERT

ALERT pin is an open drain type output pin. When an abnormal state (over current, over temperature, motor lock, or under voltage for charge pump) is detected, this pin outputs low signal.
In addition, this pin can be also used as the data output pin for serial interface (for SDO signal) when the serial interface is 3 lines type. If a serial interface has 2 lines, ALERT pin outs only ALERT signal.
The fault alarm which means low speed activates when the starting rotation speed which is set by STARTRPM is the number which is described in table below over ten seconds. Fault alarm is released when the rotation speed reaches over 70% of the STARTRPM.

Table 2-15 The condition of low speed (Fault alarm) detection

Starting rotation speed setting	Threshold of detection
STARTRPM ≥ 1000rpm	STARTRPM x 50%
700rpm ≥ STARTRPM > 1000rpm	STARTRPM – 500rpm
288rpm ≥ STARTRPM > 700rpm	200rpm
STARTRPM < 288 rpm	Do not detect

ALERT pin signal is defined as table below.

Table 2-16 Register setting vs FG and ALERT

Register			FG output signal (Note1)		ALERT output signal (Note 2)	
RDSEL	ALRMSEL	ALERTINV	Signal	Polarity	Signal	Polarity
0	0	0	FG	—	Lock / Low voltage of charge pump / ISD / TSD	L
0	0	1	FG	—	Lock / Low voltage of charge pump / ISD / TSD	H
0	1	0	FG	—	Low speed (Fault alarm) / Low voltage of charge pump / ISD / TSD(Note3)	L
0	1	1	FG	—	Low speed (Fault alarm) / Low voltage of charge pump / ISD / TSD(Note3)	H
1	0	0	Lock	L	Lock / Low voltage of charge pump / ISD / TSD	L
1	0	1	Lock	L	Lock / Low voltage of charge pump / ISD / TSD	H
1	1	0	Low speed (Fault alarm)	L	Low speed (Fault alarm) / Low voltage of charge pump / ISD / TSD(Note3)	L
1	1	1	Low speed (Fault alarm)	L	Low speed (Fault alarm) / Low voltage of charge pump / ISD / TSD(Note3)	H

Note 1: When FG pin signal is lock or Low speed (Fault alarm), its polarity is always “L”, and the level of signal is “L”. FG pin outs “L” in 3ms when the power on or reboot from STBY mode.
Note 2: When REVALERT is set to “1”, ALERT signal is out in the reverse rotation detection.
Note 3: Low speed (Fault alarm) / Low voltage of charge pump / ISD / TSD(Note3) appear immediately after failure occurring.

2.16.4 HP, HM

Pins of HP and HM are input pins for Hall signals.
In case of using Hall element, please input signals whose characteristics are shown below.

Figure 2-12 Hall signal waveform

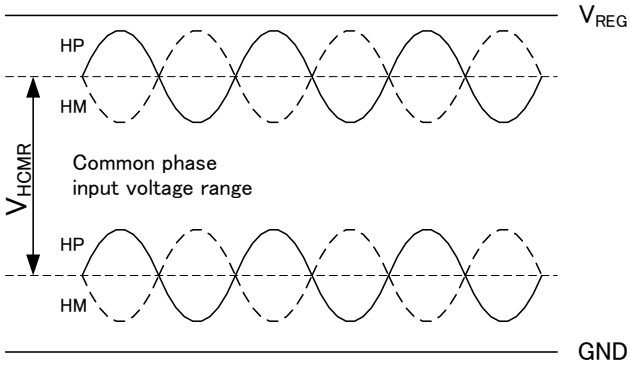
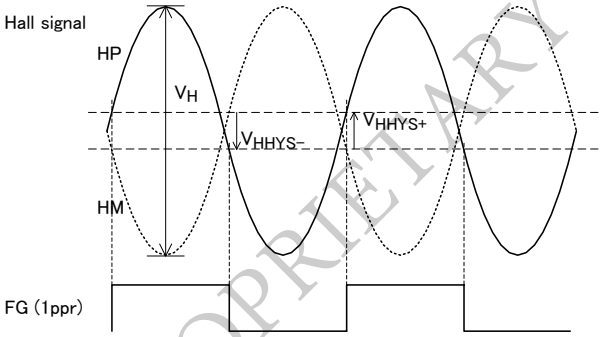


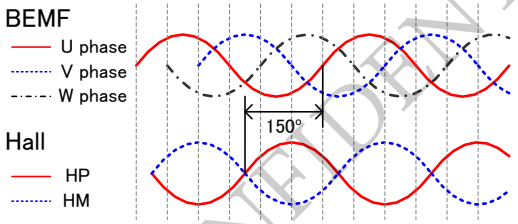
Figure 2-13 Hall and FG signal waveform



In case of using Hall IC, the Hall signal must be input to HP pin. Voltage of HM pin should be fixed.

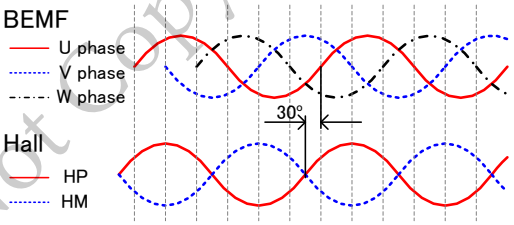
As default, please align the Hall sensor so that the relationship between Hall signals and induced voltage is as charts below.

Figure 2-14 Waveform of Hall signal and induced voltage in CW



Forward rotation (CW)

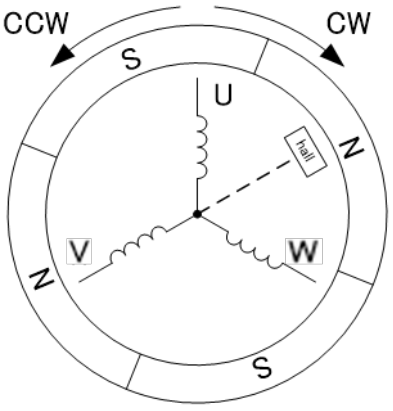
Figure 2-15 The waveform of Hall signal and induced voltage in CCW



Reverse rotation (CCW)

Figure below is the example of the default Hall position.

Figure 2-16 Example of the default position of Hall element



2.16.5 FG

FG pin is an open drain type output pin. It outputs the rotation speed signal that is obtained from the Hall signal. According to the register setting, FG pin can also output RDO signal when motor lock is detected. RDO signal is low level in motor lock detection.
In addition, FG pin can be also used as the data input or input/output pin for serial interface (for SDI or SIO signal).

1 ppr (pulse per revolution), 3ppr, 2.4ppr, 0.5ppr can be selected as FG signal.
Below table show the number of FG pulse per 1 rotation of motor.

Table 2-17 Relation of FG signal setting and the number of output pulses per one motor cycle

FGSEL [2:0]	FG signal setting	Number of motor poles				
		2 poles	4 poles	6 poles	8 poles	10 poles
000	1 ppr	1	2	3	4	5
001	2/3 ppr	2/3	4/3	2	8/3	10/3
010	1/2 ppr	0.5	1	1.5	2	2.5
011	2 ppr	2	4	6	8	10
100	3 ppr	3	6	9	12	15
101	2.4 ppr	2.4	4.8	7.2	9.6	12
110	1/3 ppr	1/3	2/3	1	4/3	5/3
111	Don't use					

Note: FG pin outputs the signal when the frequency of the Hall signal is 1Hz or more.
When the frequency of the Hall signal is less than 1Hz, FG signal is fixed to Hi-Z.
Note: When FG signal is set to 1 ppr, a signal synchronized with the Hall signal is output.
When FG signal is set to the others, internal processed result is output.

FG pin can be also used as the data input pin for serial interface (for SDI signal) when the serial interface is 3 lines type. If a serial interface has 2 lines, FG pin can be also used as the data input/output pin for serial interface (for SIO).

2.16.6 BRAKE

BRAKE pin is for controlling the motor braking function. MCD has several braking functions, motor off, short brake, reverse brake, mild brake.

Table 2-18 Brake function setting

BRAKE pin	Register		Motor status
	BRK_INV	BRK_MODE [1:0]	
L	0: Positive polarity	Don't care	No brake
L	1: Negative polarity	00	No brake
L	1: Negative polarity	01	Short brake
L	1: Negative polarity	10	Reverse brake
L	1: Negative polarity	11	Mild brake
H	0: Positive polarity	00	No brake
H	0: Positive polarity	01	Short brake
H	0: Positive polarity	10	Reverse brake
H	0: Positive polarity	11	Mild brake
H	1: Negative polarity	Don't care	No brake

Table 2-19 Lock detection setting during reverse brake

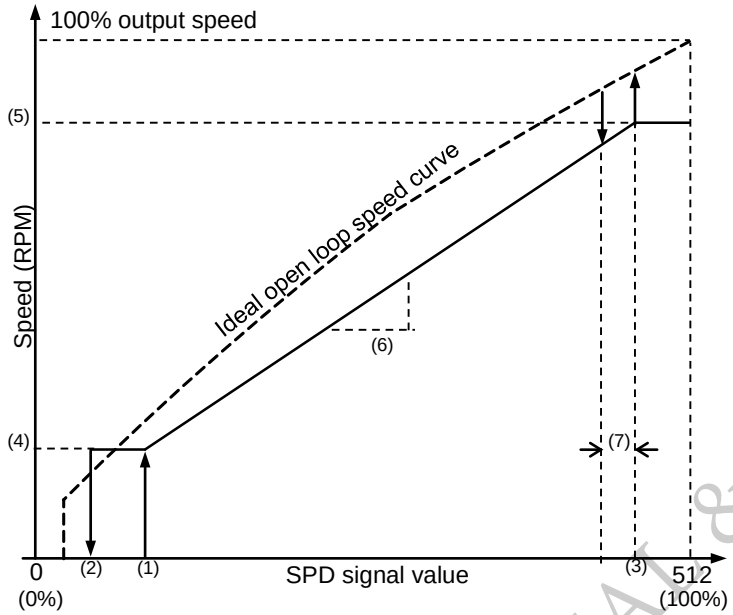
Driving status right after power on	BRAKEALT	ALRMSEL	Flag output on ALERT pin
Short brake	Don't care	Don't care	Low voltage of charge pump / ISD / TSD
Reverse brake	0	0	Low voltage of charge pump / ISD / TSD
Reverse brake	1	0	Lock / Low voltage of charge pump / ISD / TSD
Reverse brake	Don't care	1	Low voltage of charge pump / ISD / TSD
Mild brake	Don't care	Don't care	Low voltage of charge pump / ISD / TSD

2.17 MCD Speed Control

2.17.1 Closed loop

The basic speed curve (relation between SPD signal value and rotation speed) of closed loop speed control is as follows.

Figure 2-17 Speed slope example in closed loop control



(1) Startup point
(2) Stop point
(3) Output clamping point
(4) Startup speed
(5) Maximum speed (depending on speed slope)
(6) Speed slope
(7) MAXOPEN hysteresis

Please set as follows.
(3) > (1) ≥ (2)

(1) Startup point:

Output is enabled when SPD signal value exceeds the startup threshold. The threshold range is from 0 (0 %) to 255 (49.8 %) with a 0.2 % resolution. It is set by the 8-bit register STARTDUTY.

SPD duty to enable output (%) = 100 x STARTDUTY / 512

(2) Stop point:

Output is disabled when SPD signal value decreases to the stop threshold. The threshold range is from 0 (0 %) to 254 (49.6 %) with a 0.4 % resolution. It is set by the 7-bit register STOPDUTY.

SPD duty to disable output (%) = 200 x STOPDUTY / 512

(3) Output clamping point and (7) MAXOPEN hysteresis:

In case MAXDUTY = 0: When SPD signal value exceeds the output clamping threshold, the rotation speed is fixed. The threshold range is from 257 (50.2 %) to 512 (100 %) with a 0.2 % resolution. It is set by the 8-bit register MAXDUTY.

SPD duty to clamp output (%) = 100 x (257 + MAXDUTY) / 512

In case MAXOPEN = 1: When SPD signal value exceeds the output clamping threshold, the control switches to open loop speed control. The output duty during open loop speed control corresponds to SPD signal value. The hysteresis of SPD signal value to let the control switch back to closed loop speed control range is from 2 (0.4 %) to 32 (6.25 %) with a 0.4 % resolution. It is set by the 4-bit register MAXDUTYHYS.

SPD duty hys (%) = 200 x (MAXDUTYHYS + 1) / 512

(4) Startup speed:

The minimum rotation speed in startup is set by the 12-bit register STARTRPM. Setting range is from 0 to 4095 RPM with 1 RPM resolution.

Startup speed (RPM) = STARTRPM

(5) Maximum speed and (6) Speed slope:

Maximum speed depends on the speed slope, which is set by the register SPEEDSLOP. It is a 14-bit register.

SPEEDSLOP = 64 x (Maximum speed – Startup speed) / (MAXDUTY + 257 – STARTDUTY)

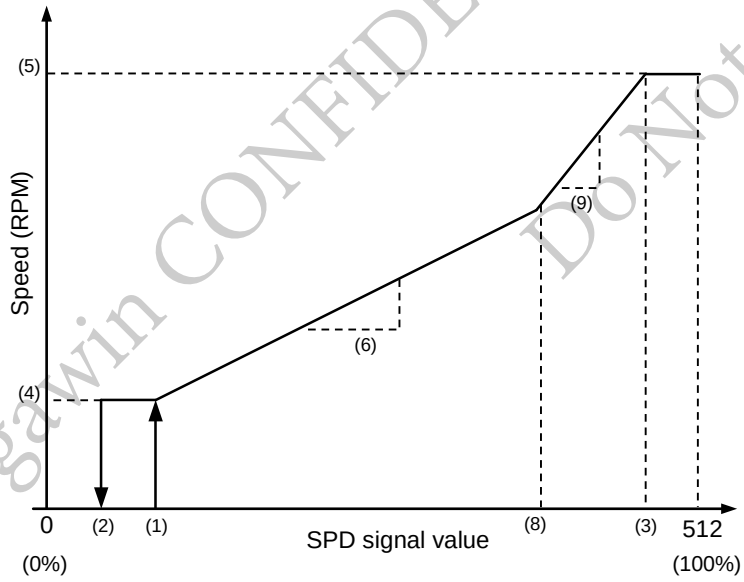
Configurations of MAXOPEN, NOSTOP, and MAXOFF registers determine the behavior when SPD signal value is equivalent to the startup (output enabling) point or less.

Table 2-20 Rotation Behavior (SPD signal value ≤ Startup point)

MAXOPEN	NOSTOP	MAXOFF	Target speed		
			SPD =0 %	0 % < SPD ≤ Startup point	Stop point < SPD ≤ Startup point
0	0	0	0	0	Duty up: 0 Duty down: Startup speed
	0	1	Maximum Speed	0	Duty up: 0 Duty down: Startup speed
	1	0	Startup speed	Startup speed	Startup speed
	1	1	Maximum Speed	Maximum Speed	Startup speed
1	0	0	0	0	Duty up: 0 Duty down: Startup speed
	0	1	100 % Output	0	Duty up: 0 Duty down: Startup speed
	1	0	Startup speed	Startup speed	Startup speed
	1	1	100 % Output	100 % Output	Startup speed

Adding a speed change point to the speed curve is possible.

Figure 2-18 Speed Slope Example in Closed loop speed control



(1) Startup point
(2) Stop point
(3) Output clamping point
(4) Startup speed
(5) Maximum speed (depending on speed slope)
(6) First speed slope
(8) Speed change point
(9) Second speed slope

Please set as follows.
(3) > (8) > (1) ≥ (2)

(in case of adding speed change point)

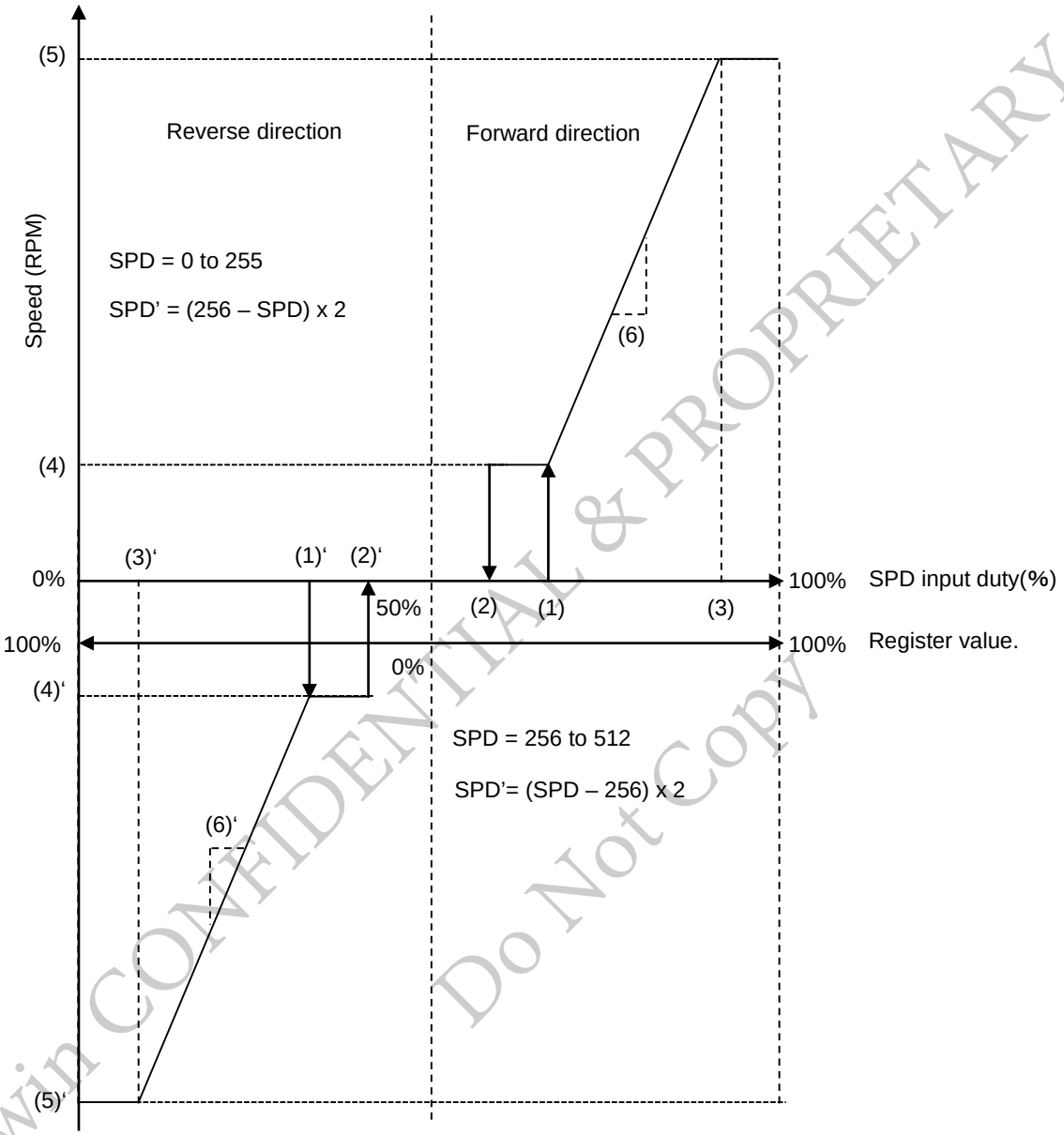
(8) Speed change point:
The SPD signal value range of the speed change point is from 0 (0.4 %) to 510 (99.6 %) with a 0.4 % resolution. It is set by the 8-bit register CHANGEDUTY.
SPD duty of change point (%) = 200 x CHANGEDUTY / 512

In case of not using the speed change point, set CHANGEDUTY to 0.

(9) Second speed slope:
After passing the speed change point, the register SPEEDSLOP2 sets the speed slope.

In case of DIR50=1, rotation direction of motor is controlled by the duty of SPD signal.
Motor rotates forward direction when SPD duty is 50% or more. Motor rotates reverse direction when SPD duty is under 50%.

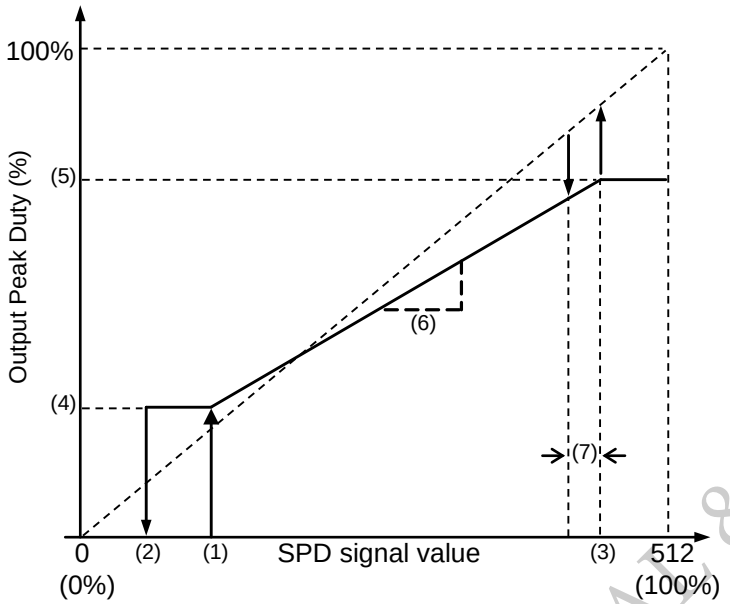
Figure 2-19 Speed Slope Example in Closed loop speed control (in case of DIR50=1)



2.17.2 Open loop

The basic speed curve (relation between SPD signal value and output duty) of open loop speed control is as follows.

Figure 2-20 Speed slope example in Open loop speed control



(1) Startup point
(2) Stop point
(3) Output clamping point
(4) Startup output duty
(5) Maximum output duty (depending on speed slope)
(6) Speed slope
(7) MAXOPEN hysteresis

Please set as follows.
(3) > (1) ≥ (2)

(1) Startup point:
Output is enabled when SPD signal value exceeds the startup threshold. The threshold range is from 0 (0 %) to 255 (49.8 %) with a 0.2 % resolution. It is set by the 8-bit register STARTDUTY.
SPD duty to enable output (%) = 100 x STARTDUTY / 512

(2) Stop point:
Output is disabled when SPD signal value decreases to the stop threshold. The threshold range is from 0 (0 %) to 254 (49.6 %) with a 0.4 % resolution. It is set by the 7-bit register STOPDUTY.
SPD duty to disable output (%) = 200 x STOPDUTY / 512

(3) Output clamping point and (7) MAXOPEN hysteresis:
In case MAXDUTY = 0: When SPD signal value exceeds the output clamping threshold, the output duty is fixed. The threshold range is from 257 (50.2 %) to 512 (100 %) with a 0.2 % resolution. It is set by the 8-bit register MAXDUTY.
SPD duty clamp output (%) = 100 x (257 + MAXDUTY) / 512

In case MAXOPEN = 1: When SPD signal value exceeds the output clamping threshold, the output duty becomes corresponding to SPD signal value. The hysteresis range of SPD signal value to let the output return to original speed curve is from 2 (0.4 %) to 32 (6.25 %) with a 0.4 % resolution. It is set by the 4-bit register MAXDUTYHYS.
SPD duty hys (%) = 200 x (MAXDUTYHYS + 1) / 512

(4) Startup output duty:
The minimum output duty in startup is set by an upper 8-bit of the 12-bit register STARTRPM. Setting range is from 0 (0 %) to 255 (49.8 %) with a 0.2 % resolution.
Startup output duty (%) = 100 x STARTRPM [11:4] / 512

(5) Maximum output duty and (6) Speed slope:
Maximum output duty depends on the speed slope, which is set by the register SPEEDSLOP. It is a 14-bit register.
SPEEDSLOP = 2^{19} x (Maximum output duty (%) – Startup output duty (%)) / (MAXDUTY + 257 – STARTDUTY) / 100.

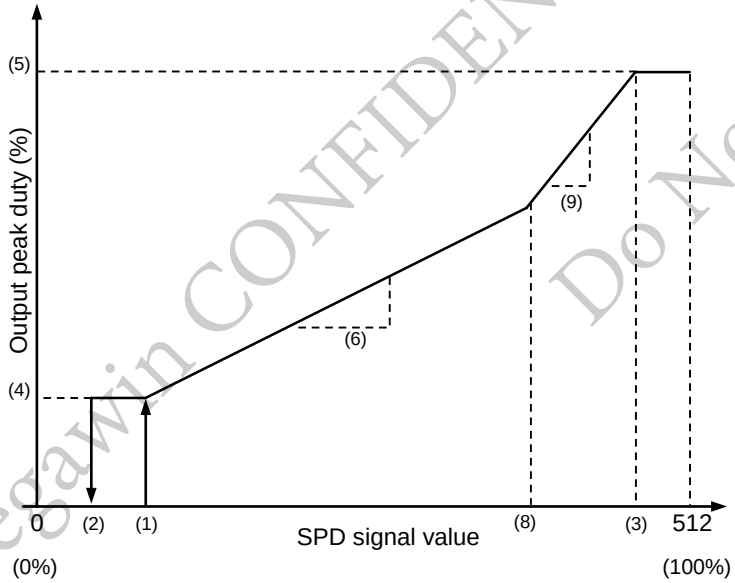
Configurations of MAXOPEN, NOSTOP, and MAXOFF registers determine the behavior when SPD signal value is equivalent to the startup (output enabling) point or less.

Table 2-21 Rotation Behavior (SPD signal value ≤ Startup point)

MAXOPEN	NOSTOP	MAXOFF	Output Duty		
			SPD =0 %	0 % < SPD ≤ Startup point	Stop point < SPD ≤ Startup point
0	0	0	0	0	Duty up: 0 Duty down: Startup Output
	0	1	Maximum Output	0	Duty up: 0 Duty down: Startup Output
	1	0	Startup Output	Startup Output	Startup Output
	1	1	Maximum Output	Maximum Output	Startup Output
1	0	0	0	0	Duty up: 0 Duty down: Startup Output
	0	1	100 % Output	0	Duty up: 0 Duty down: Startup Output
	1	0	Startup Output	Startup Output	Startup Output
	1	1	100 % Output	100 % Output	Startup Output

Adding a speed change point to the speed curve is possible.

Figure 2-21 Speed Slope Example in Open loop speed control



(1) Startup point
(2) Stop point
(3) Output clamping point
(4) Startup output duty
(5) Maximum output duty (depending on speed slope)
(6) First speed slope
(8) Speed change point
(9) Second speed slope

Please set as follows.
(3) > (8) > (1) ≥ (2)

(in case of adding speed change point)

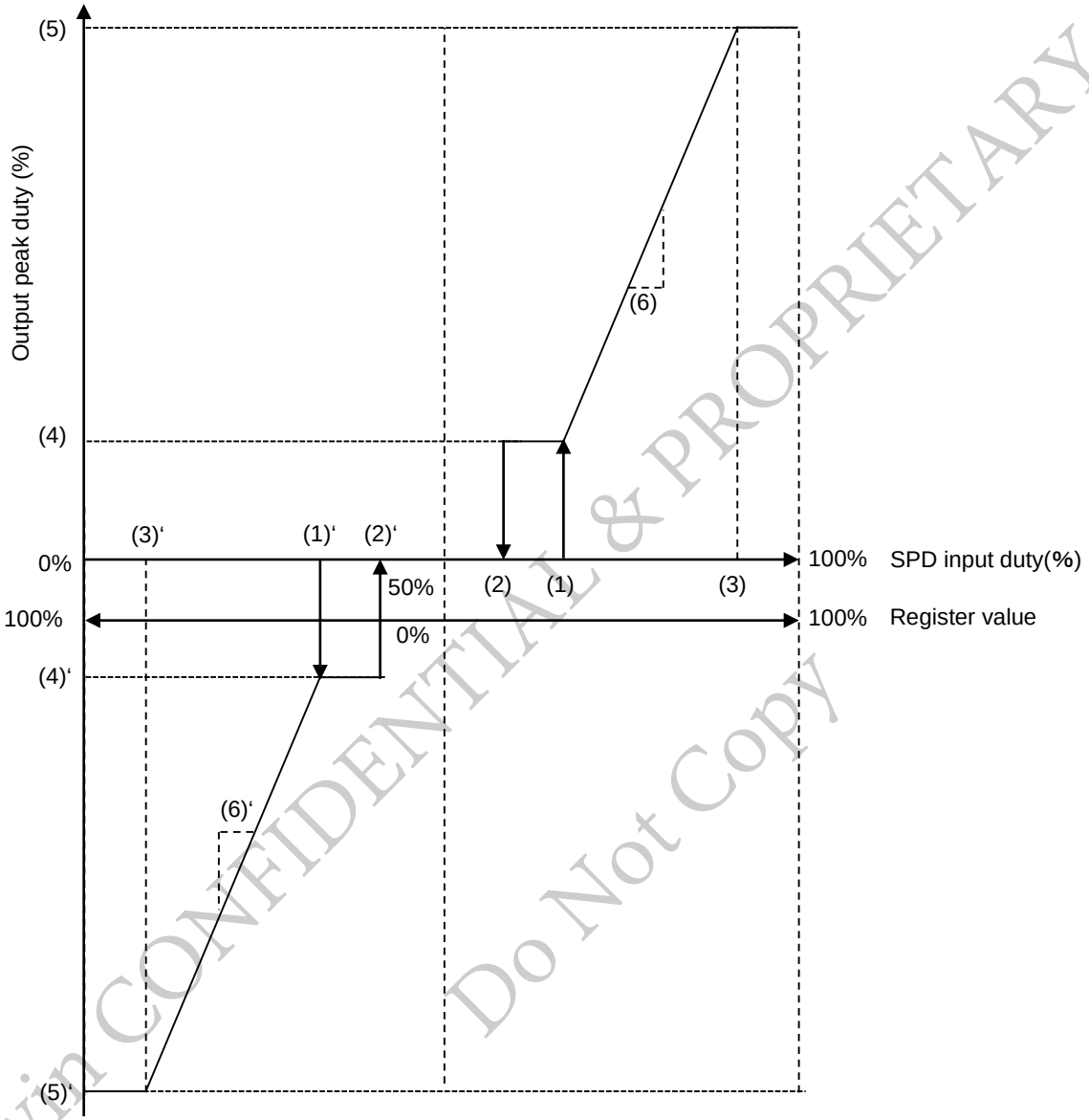
(8) Speed change point:
The SPD signal value range of the speed change point is from 0 (0.4 %) to 510 (99.6 %) with a 0.4 % resolution. It is set by the 8-bit register CHANGEDUTY.
SPD duty of change point (%) = 200 x CHANGEDUTY / 512

In case of not using the speed change point, set CHANGEDUTY to 0.

(9) Second speed slope:
After passing the speed change point, the register SPEEDSLOP2 sets the speed slope.

In case of DIR50=1, rotation direction of motor is controlled by the duty of SPD signal.
Motor rotates forward direction when SPD duty is 50% or more. Motor rotates reverse direction when SPD duty is under 50%,

Figure 2-22 Speed Slope Example in Open loop speed control (in case of DIR50=1)



2.17.3 Open/Close loop control with MCU

Based on MCD open loop control, MCU can support more speed changing points by MA853 motor Studio as shown as **Figure 2-23**.

MCU detects SPD signal and converts the input duty to output duty by curve table. The curve table can set to MCU by MA853 Motor Studio. And MCU has ADC to measure supply voltage for OVP(Over-voltage protect) and UVP(Under-voltage protect).

Based on MCD close loop control, MCU only set OVP/UVP and RBlock function as shown as **Figure 2-24**.

Figure 2-23 Open loop speed control with multi speed changing points by MCU

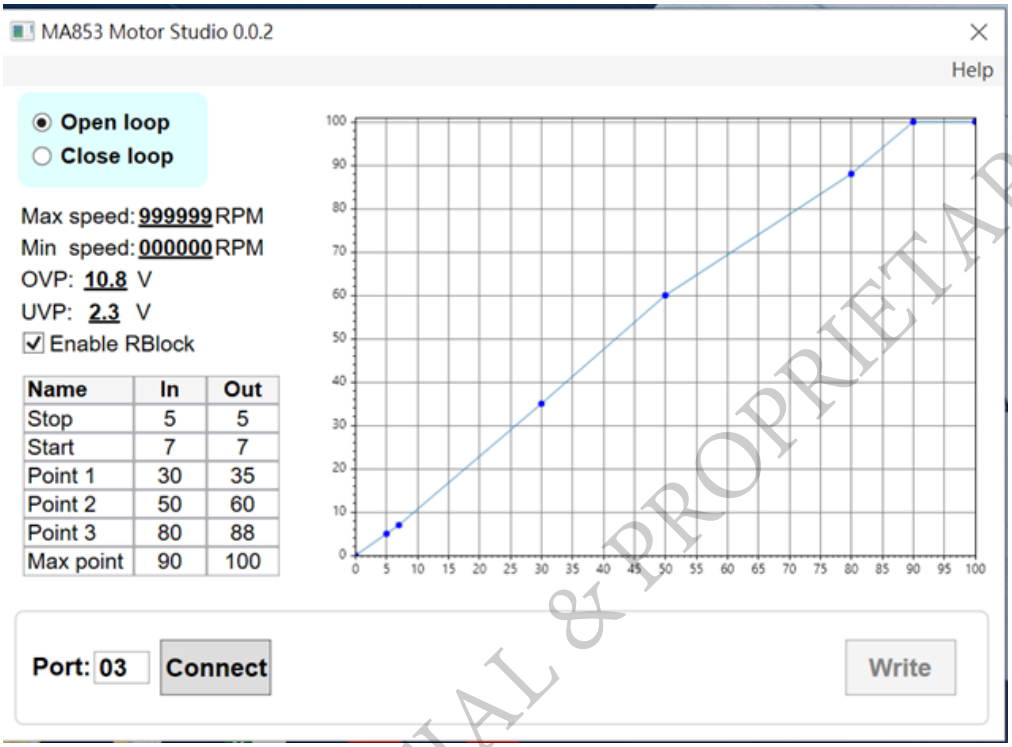
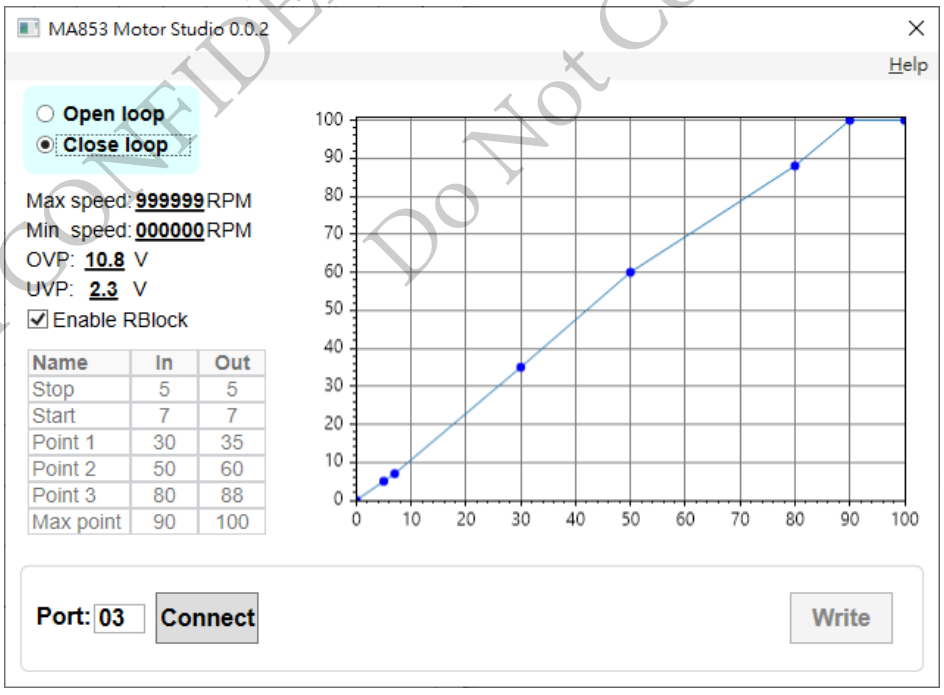


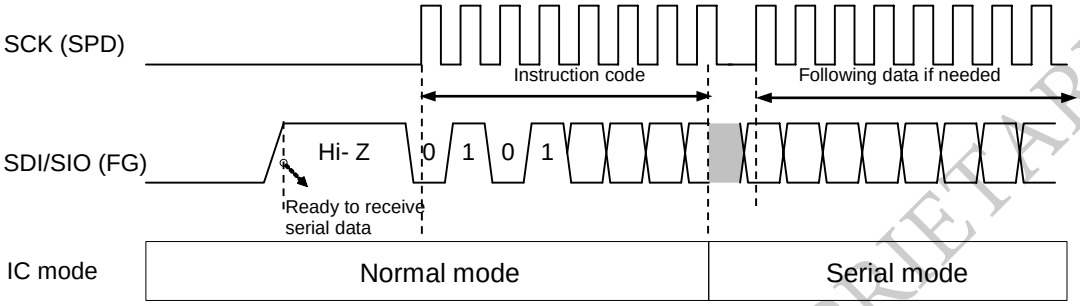
Figure 2-24 Close loop speed control



2.18 MCD Serial I/F and NVM

Data of internal registers and non-volatile memory (NVM) can be configured via serial interface.
When FG pin is Hi-Z, receiving serial commands is possible. IC enters serial mode after receiving the instruction code. In this mode, motor output stops, and FG pin is fixed to Hi-Z.

Figure 2-25 Timing chart



After inputting instruction code and following data (if needed),
If ENB of Status Register is “0”, IC returns to normal mode.
If ENB of Status Register is “1”, IC stays in serial mode.

2.18.1 Serial commands

Table 2-22 Serial commands (Instruction Code)

Command	Code	Description	Following Data
SR_READ	010 01 001	Read status register	8-bit data out
SR_WRITE	010 01 010	Write status register	8-bit data in
REG_READ	010 10 001	Read normal register	8-bit addr in + 16-bit data out
REG_WRITE	010 10 010	Write normal register	8-bit addr in + 16-bit data in
NVM_LOAD	010 11 001	Load NVM data to normal register	None
NVM_SAVE	010 11 010	Store data of normal register to NVM	None
NVM_ABORT	010 11 100	Terminate NVM writing process forcedly	None

2.18.2 Status register

Table 2-23 Status Register (SR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	—	—	CAL_ERR	NVM_WR	WIRE	ENB	BUSY

Name	Description	Detail
BUSY	State of register processing	BUSY=0: Standby, BUSY=1: Under processing (REG_READ, REG_WRITE, NVM_LOAD, NVM_SAVE, NVM_COPY)
ENB	Serial command enable setting	ENB=0: Normal mode (Only SR_READ SR_WRITE is acceptable.) ENB=1: Serial mode (All commands are acceptable.)
WIRE	Serial communication mode setting	WIRE=0: 3-wire mode (SCK=SPD, SDI=FG, and SDO=ALERT) WIRE=1: 2-wire mode (SCK=SPD and SDIO=FG)
NVM_WR	NVM mode setting	NVM_WR=0: READ enable, WRITE disable NVM_WR=1: READ disable, WRITE enable
CAL_ERR	Result of Hall position detection	CAL_ERR=0: Success CAL_ERR=1: Failure

2.18.3 Register map

Table 2-24 Register map

ADDR	Bit	Name	Description	Default
0	15:0	USERID [15:0]	-	0
1	15	NOSTOP	Non-stop mode (0: disable, 1: enable)	0
	14:8	STOPDUTY [6:0]	Stop duty	0
	7:0	STARTDUTY [7:0]	Startup duty	0
2	15:8	CHANGEDUTY [7:0]	Speed change point duty	0
	7:0	MAXDUTY [7:0]	Maximum duty	0
3	15:4	STARTRPM [11:0]	Rotation speed in startup	0
	3:0	MAXDUTYHYS [3:0]	Recovery hysteresis from open loop to closed loop speed control	0
4	15:2	SPEEDSLOPE [13:0]	Speed slope	0
	1	MAXOPEN	Switching to open loop speed control when SPD signal value exceeds the threshold (0: disable, 1: enable)	0
	0	MAXOFF	Rotating with full speed when SPD signal value corresponds to the startup point or less. (0: disable, 1: enable)	0
5	15:2	SPEEDSLOPE2[13:0]	Speed slope after passing speed change point	0
	1	REVALERT	ALERT output in reverse detection	0
	0	OPENLOOP	OPEN LOOP/CLOSEDLOOP (0: closed loop, 1: open loop)	0
6	15	KiX	To eight times the KI (0: x1, 1: x8)	0
	14:8	Ki [6:0]	KP (0 to 127)	0
	7	KpX	To eight times the KI (0: x1, 1: x8)	0
	6:0	Kp [6:0]	KI (0 to 127)	0
7	15	STBY	Standby mode (0: disable, 1: enable)	0
	14	DIR	Relation of DIR pin polarity and rotation direction (0: positive, 1: negative)	0
	13:11	POLEPAIR [2:0]	Pair of motor poles	0
	10:9	MAXSPEED [1:0]	Maximum rotation speed	0
	8	HALLINV	Hall signal polarity conversion (0: positive, 1: negative)	0
	7:6	HALLPOS [1:0]	Hall alignment sector	0
	5:0	HALLOFFSET [5:0]	Hall position offset	0
8	15	RDSEL	The signal selection to output FG pin (0: FG signal, 1: RDO signal or ALARM signal)	0
	14:12	FGSEL [2:0]	FG signal type setting	0
	11	SPDSEL	SPD command type setting (0: Analog voltage input, 1: PWM duty input)	0
	10	SPDINV	SPD signal polarity conversion (0: positive, 1: negative)	0
	9	REVBRAKE	Reverse startup (0: disable, 1: enable)	0
	8	150DRV	150° commutation (0: sine-wave drive, 1:150° commutation)	0
	7	ISDLATCH	ISD latch (0: disable, 1: enable)	0
	6:5	OCPMASK [1:0]	Masking period for current limit	0
	4:3	OCPHYS [1:0]	Current limit setting	0
	2:0	PWMSEL [2:0]	Output PWM frequency setting	0

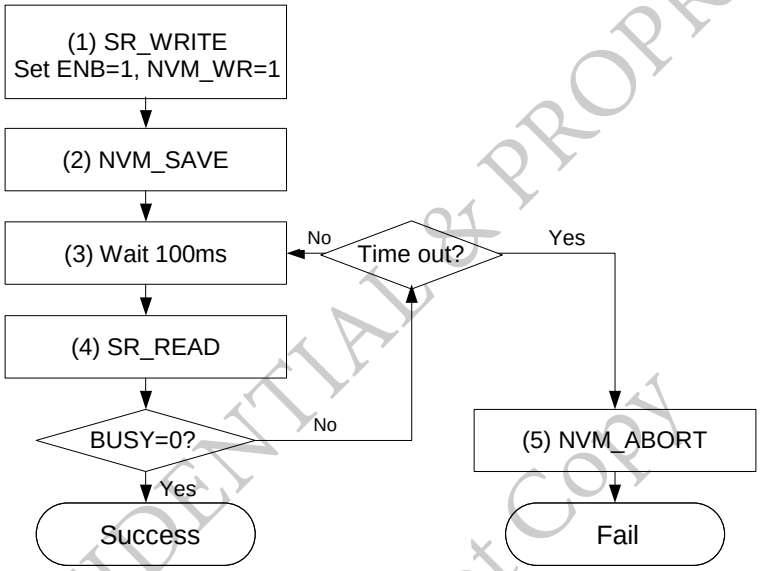
ADDR	Bit	Name	Description	Default
9	15	TON	Lock detection ON period	0
	14	TOFF	Lock detection OFF period	0
	13	LOCKDIS	Disable lock detection	0
	12:10	DUTYCHGLIMIT [2:0]	Duty changing limit	0
	9:8	STARTFREQ [1:0]	Startup switching frequency	0
	7:5	STARTCURRENT [2:0]	Startup current limit	0
	4:0	LATABLE [4:0]	Lead angle table	0
10	15	LASEL	Lead angle selection	0
	14	BRK_360_SEL	0: 180° reset during mild brake, 1: 360° reset during mild brake	0
	13	OCPDIS	Disable current limit (0: OCP enable, 1: OCP disable)	0
	12:11	SS_ADD_SEL [1:0]	Soft start current (OCP × 0%, 30%, 40%, 50%)	0
	10:9	SS_UP_SEL [1:0]	Increasing amount of the current in soft start (OCP * +1%, +2%, +5%, +10%)	0
	8:6	SS_DUTYCHGLIMIT [2:0]	Duty change limit in soft start phase (equivalent to DUTYCHGLIMIT)	0
	5	OC_LEVEL	Reference voltage for OCP (0: 0.25V, 1: 0.125V)	0
	4	DUTY_UP_TIME	Changing period of PWM duty (0: each 2.7ms, 1: each 10.9ms)	0
	3	ISD_LEVEL	Reference voltage for ISD (0: 1.0V, 1: 0.5V)	0
	2:0	RPMLIMIT [2:0]	Limit of step of changing rotation speed (No limit, 512rpm, 2200rpm, 3800rpm, 5400rpm, 7000rpm, 8600rpm, 10240rpm)	0
11	15:14	BRK_MODE [1:0]	The setting of brake (No brake, Short brake, Reverse brake, Mild brake)	0
	13	BRK_INV	Polarity of BRAKE pin (0: positive, 1: negative)	0
	12:10	WAIT_TIME [2:0]	Wait time after power on (0s, 1s, 2s, 3s, 4s, 5s, 6s, 7s)	0
	9:8	WAIT_MODE [1:0]	Output status at power on (No brake, Short brake, Reverse brake, Mild brake)	0
	7	WAIT_CON	Output status after a certain time from power on (0: Brake off after WAIT_TIME from power on, 1: Sustain the brake status which is set by WAIT_MODE after WAIT_TIME from power on)	0
	6	LOCK_BRK	Short brake setting when locking protection (0: OFF, 1: Short brake)	0
	5	ALRMSEL	The output setting for ALERT (FG/Lock/Low speed (Fault alarm))	0
	4	ALERTINV	Polarity of ALERT pin (0: Fault when L, 1: Fault when H)	0
	3	IND_SEL	DC excitation ON/OFF (0: disable, 1: enable)	0
	2	SS_LOCK	Lock detection when soft start	0
	1	ALARM_LAT_SEL	0: Release ALARM when no torque command / brake setting, 1: Sustain ALARM however no torque command / brake setting	0
	0	ISD_MASK	ISD mask setting (0: enable, 1: disable)	0
12	15:13	ISOURCE_SEL [2:0]	High side / Low side Source current	0
	12:10	ISINK_SEL [2:0]	High side / Low side Sink current	0
	9:8	DEADTIME [1:0]	Dead time (200ns 500ns 1μs 1.5μs)	0
	7	DIR50	DIR50 signal (0: disable, 1: enable)	0
	6:5	RS_SEL [1:0]	Input filter of OC pin (None, 200kHz, 100kHz, 50kHz)	0
	4	ANTITHROUGH	Dead time auto tuning (0: Auto, 1: Manual)	0
	3:2	INPACEDGE	—	0
	1	INPACAPPLY	—	0
	0	BRAKEALT	The setting of lock detection when in reverse brake	0

ADDR	Bit	Name	Description	Default
13	15:6	Trq_duty [9:0]	SPD command	0
	5	UNUSED	Don't care	0
	4:3	Hall_off_Freq [1:0]	Hall position detection, frequency of forced rotation	0
	2:1	Hall_cal_Freq [1:0]	Hall position detection, Frequency of detection when starting	0
	0	Hall_cal	Hall position detection enable	0

2.18.4 Flowchart of writing Non-Volatile Memory (NVM)

Flow chart of NVM write is as follows.

Figure 2-26 NVM writing flowchart



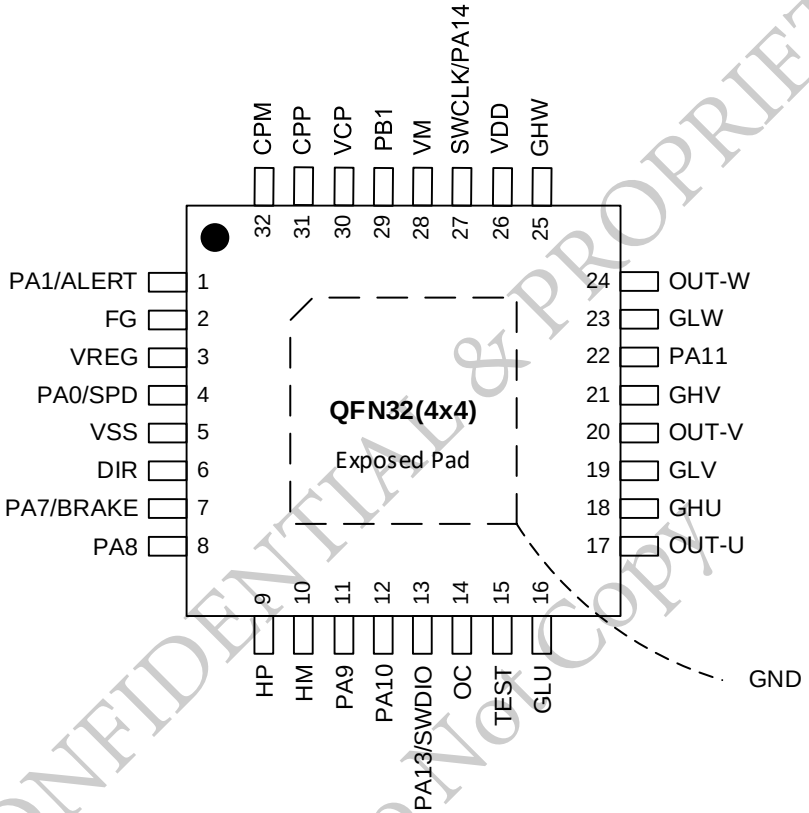
The writing period may be longer depending on the operating conditions. However, if the BUSY bit of the status register does not return to 0 within 1.3 seconds, it is considered a writing error. Please forcibly terminate the writing process using the NVM_ABORT command.

After NVM writing process has completed, always return NVM_WR setting to 0.

3 Pinout and assignment

3.1 QFN32 pinout

Figure 3-1 QFN32 pinout diagram



3.2 Pin assignment

Table 3-1 Pin assignment table

QFN32	MCU/MCD	Name	Type (1)	I/O level (2)	Additional function	Description
1	MCU	PA1	I/O	TC	-	Needs to be changed to Output function
	MCD	ALERT	OD	-	-	Output pin for alert signal, Serial I/F data output pin
2	MCD	FG	OD	-	-	Output pin for rotation number signal, Serial I/F data I/O pin
3	MCD	VREG	S	-	-	5V reference voltage output pin
4	MCU	PA0	I/O	-	-	Needs to be changed to AF2 PWM function
	MCD	SPD(4)	I	-	-	Input pin for speed command, Serial I/F clock input pin
5	MCU	VSS	S	-	-	MCU Ground pin
6	MCD	DIR	I	-	-	Input pin for rotation direction signal (50 kΩ pull-down)
7	MCU	PA7	I/O	TC		Needs to be changed to Output function
	MCD	BRAKE	I	-	-	Input pin for brake command (50kΩ pull-down)
8	MCU	PA8	I/O	TC	-	Needs to be changed to AF4 Capture function
9	MCD	HP	I	-	-	Hall signal input (+) pin
10	MCD	HM	I	-	-	Hall signal input (-) pin
11	MCU	PA9	I/O	TC	-	Needs to be changed to AF3 Capture function
12	MCU	PA10	I/O	TC	-	Needs to be changed to Output function
13	MCU	PA13/SWDIO	I/O	TC	-	Programming Pins and USART1 RX Functions
14	MCD	OC	I	-	-	Input pin for the current sense resistor
15	MCD	TEST(5)	I	-	-	TEST pin
16	MCD	GLU	O	-	-	U-phase low-side MOSFET gate driver output
17	MCD	OUT-U	I	-	-	Input pin for U-phase signal of the motor
18	MCD	GHU	O	-	-	U-phase high-side MOSFET gate driver output
19	MCD	GLV	O	-	-	V-phase low-side MOSFET gate driver output
20	MCD	OUT-V	I	-	-	Input pin for V-phase signal of the motor
21	MCD	GHV	O	-	-	V-phase high-side MOSFET gate driver output
22	MCU	PA11	I/O	TC	ADC1_VIN[4]	Need to change to ADC channel 4 function
23	MCD	GLW	O	-	-	W-phase low-side MOSFET gate driver output
24	MCD	OUT-W	I	-	-	Input pin for W-phase signal of the motor
25	MCD	GHW	O	-	-	W-phase high-side MOSFET gate driver output

QFN32	MCU/MCD	Name	Type (1)	I/O level (2)	Additional function	Description
26	MCU	VDD	S	-	-	MCU VDD pin
27	MCU	PA14/SWCLK (NRST) (3)	I/O	TC	-	Programming Pins and USART1 TX Functions
28	MCD	VM	S	-	-	Power supply pin
29	MCU	PB1	I/O	TC	ADC1_VIN[0]	Need to change to ADC channel 0 function
30	MCD	VCP	S	-	-	Connect pin for accumulation capacitor of charge pump
31	MCD	CPP	S	-	-	Connect pin for pumping capacitor of charge pump
32	MCD	CPM	S	-	-	Connect pin for pumping capacitor of charge pump
Paddle	MCD	GND	S			MCD Ground pin

Note 1. I = input, O = output, OD = output drain, S = power pins, HiZ = high resistance state.

Note 2. TC: standard IO. Input signal level should not exceed VDD.

Note 3. When SFT_NRST_RMP bit of RCC_SYSCFG is set to 1, PA14 is mapped as an NRST external reset and should be held low for at least 4us for reliable reset.

Note 4: SPD pin should not be left to open state.

Note 5: TEST pin must be connected to GND

3.3 Pin multiplexing

Table 3-2 PA port multiplexing AF0-AF4

Pin	AF0	AF1	AF2	AF3	AF4
PA0	-	-	TIM1_CH3N	-	-
PA8	-	-	-	-	TIM3_CH1
PA9	-	-	-	TIM14_CH1	-
PA13	SWDIO	USART1_RX	-	-	-
PA14	SWCLK	USART1_TX	-	-	-

4 Electrical Characteristics

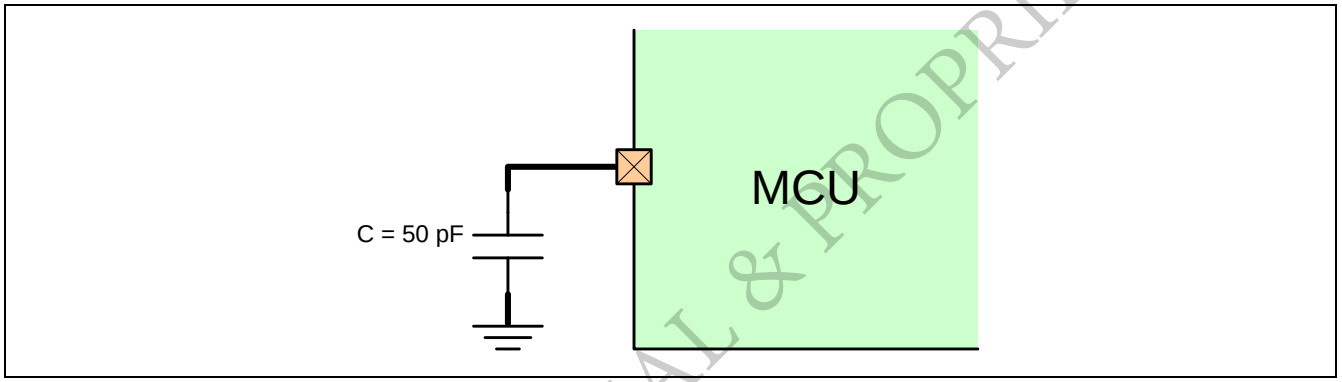
4.1 Test condition

All voltages are referenced to V_{SS} unless otherwise stated.

4.1.1 Load capacitance

The load conditions for pin parameters measurement are shown in the **Figure 4-1**.

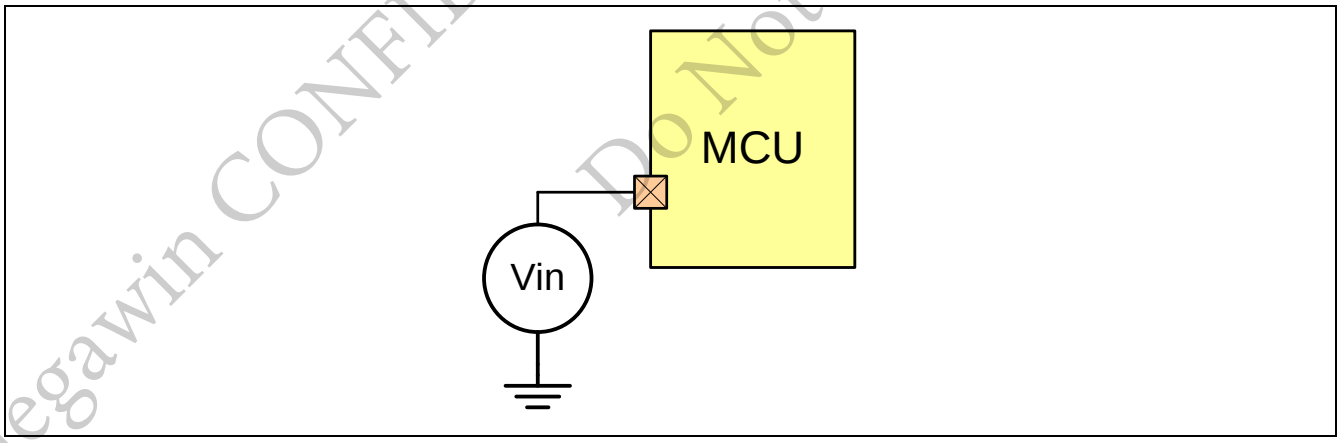
Figure 4-1 Load condition of the pin



4.1.2 I/O input voltage

The measurement of the input voltage on the pin is shown in **Figure 4-2**.

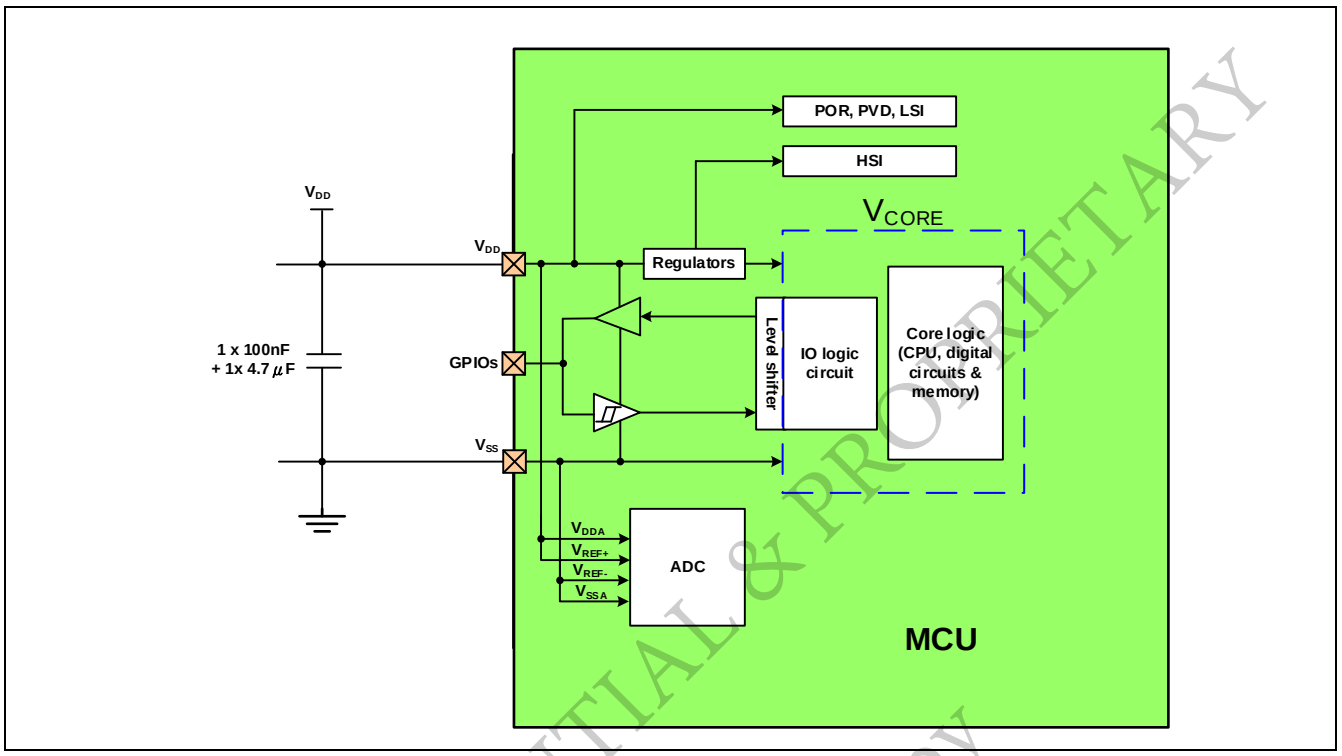
Figure 4-2 Pin input voltage



4.1.3 Power scheme

The power supply design scheme is shown in **Figure 4-3**.

Figure 4-3 Power scheme (1)



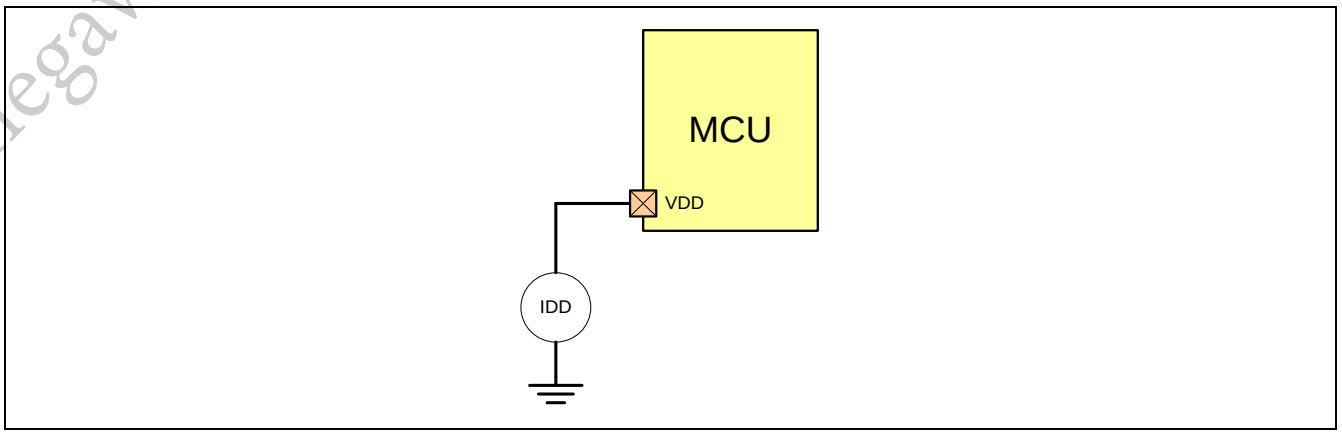
Notes:

1. For optimal chip performance, it is recommended to use the filtering ceramic capacitors shown in the figure above for decoupling between power pair (VDD, VSS)
2. For this product, the V_{DD}, V_{DDA}, and V_{REF+} are all connected to the VDD pin inside the chip, and V_{SS}, V_{SSA}, and V_{REF-} are all connected to the VSS pin inside the chip.

4.1.4 Current consumption measurement

The measurement of the current consumption on the pin is shown in **Figure** 4-4.

Figure 4-4 Current consumption measurement scheme



4.2 Absolute maximum rating

Stresses above the absolute maximum ratings given in "Absolute Group Maximum Ratings" list (Table 4-1, Table 4-2) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Voltage characteristics for MCU

Symbol	Description	Minimum	Maximum	Unit
V_{DDx}-V_{SSx}	External main supply voltage (including V_{DDA} and V_{SSA}) (1)	-0.3	5.8	V
V_{IN} (2)	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	

1. All power (VDD) and ground (VSS) pins must always be connected to the external power supply system within the permitted range.
2. The maximum value of V_{IN} must be respected. Refer to the table below for the maximum allowed injected current values.

Table 4-2 Current characteristics for MCU

Symbol	Description	Maximum	Unit
$I_{VDD/VDDA}$ (1)	Total current through V_{DD}/V_{DDA} power pins (supply current) (1)	+60	mA
$I_{VSS/VSSA}$ (1)	Total current through V_{SS}/V_{SSA} ground pins (outflow current) (1)	-60	
I_{IO}	Output sink current on any I/O and control pins, V_{DD} = 5.0V	+20	
	Output source current on any I/O and control pins, V_{DD} = 5.0V	-20	
	Output sink current on any I/O and control pins, V_{DD} = 3.3V	+15	
	Output source current on any I/O and control pins, V_{DD} = 3.3V	-15	
	Output sink current on any I/O and control pins, V_{DD} = 2.0V	+6	
	Output source current on any I/O and control pins, V_{DD} = 2.0V	-6	
$I_{INJ(PIN)}$ (2)(3)	NRST pin injection current	±5	
	HSE OSC_IN pin injection current	±5	
$\sum I_{INJ(PIN)}$ (5)	Other pins injection current (4)	±25	

1. All main power (V_{DD}) and ground (V_{SS}) pins must always be connected to an external power supply in the permitted range.
2. This current consumption must be correctly distributed to all I/O and control pins.
3. The reverse injection current can interfere with the analog performance of the device.
4. When $V_{IN} > V_{DDA}$, a positive injected current is generated; when $V_{IN} < V_{SS}$, a reverse injected current is generated. Do not exceed $I_{INJ(PIN)}$.
5. When there is simultaneous injection current for multiple inputs, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse injection current (instantaneous value).

Table 4-3 Absolute Maximum Ratings for MCD

Characteristics		Symbol	Rating	Unit
Power supply voltage of the motor		V_M	18	V
5V reference voltage		V_{REG}	6 (Note 1)	V
Charge pump voltage		V_{CP}	V_M+10 (Note 1)	V
Input voltage	HP, HM, DIR, BRAKE, OC	V_{IN}	-0.3 to 6	V
	SPD		-0.3 to 6 (18) (Note2)	V
Output voltage	ALERT, FG, GLU, OUT-U, GLV, OUT-V, GLW, OUT-W,	V_{OUT}	18	V
	GHU, GHV, GHW		V_M+10	V
Source current	VREG	I_{OUT}	10	mA
	GLU, GHU, GLV, GHV, GLW, GHW		100	mA
Sink current	ALERT, FG,	I_{IN}	10	mA
	GLU, GHU, GLV, GHV, GLW, GHW		200	mA
Operating temperature		T_{opr}	-40 to 105	°C
Storage temperature		T_{stg}	-55 to 150	°C
Junction temperature		$T_{j\,(MAX)}$	150	°C

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the ratings may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. Please use the IC within the specified operating ranges.

Note: Output current is limited depend on the ambient temperature and the device implementation. The maximum junction temperature ($T_{j\,(MAX)}$) should not exceed 150°C.

Note 1: VREG and VCP pin voltage are generated in the IC. Do not apply voltage externally.

Note 2: This terminal should be used within operating range. However up to 18V can be applied, it DOES NOT mention that IC will not deteriorate in such case.

4.3 Operating conditions

4.3.1 General operating conditions for MCU

Table 4-4 General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	-	48	
V_{DD}	Digital circuit operating voltage	All power modes except Standby mode	1.8	3.3	5.5	V
V_{DD}	Digital circuit operating voltage	Standby mode	2.0	3.3	5.5	
V_{DDA}	Analog circuit operating voltage (Performance is guaranteed)	Must be the same as V_{DD} (1)	2.5	3.3	5.5	
	Analog circuit operating voltage (Performance is not guaranteed)		1.8	-	2.5	
P_D	Power dissipation (2)	QFN20	-	-	196	mW
T_A	Ambient temperature (Extended industrial level)	-	-40	-	105	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_J	Junction temperature (3) (Extended industrial level)	-	-40	-	125	

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}, the maximum permissible difference between V_{DD} and V_{DDA} is 300mV during power up and normal operation.
2. If T_A is low, higher P_D values are allowed if T_J does not exceed T_{Jmax}.
3. In low power dissipation state, T_A can be extended to this range if T_J does not exceed T_{Jmax}.

4.3.2 Operating conditions at power-up/power-down for MCU

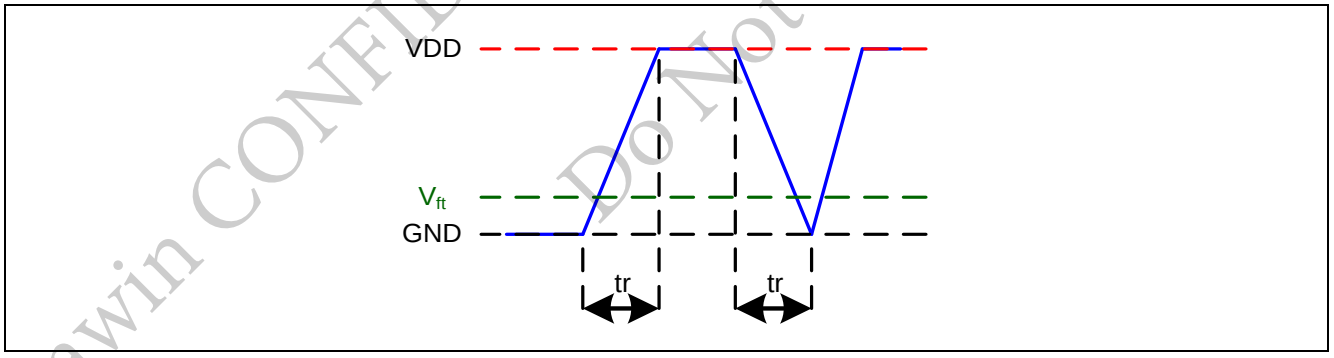
The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 4-4.

Table 4-5 Operating conditions at power-up/power-down

Symbol	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time t_r	0.2	-	∞	us/V
	V_{DD} fall time t_f	60	-	∞	
V_{ft} (3)	Power-down threshold voltage	-	0	-	mV

1. Data based on characterization results, not tested in production.
2. The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phased in the following waveform diagram, and no power-down is allowed during power-on process.
3. Note: To ensure the reliability of chip power-on, all power-on should start from 0V.

Figure 4-5 Power-on and power-down waveforms



4.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 4-4.

Table 4-6 Embedded reset and power control block characteristics

Symbol	Parameter	Condition	Min. (3)	Typ.	Max. (3)	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3:0]=0000 (Rising edge)	-	1.8	-	V
		PLS[3:0]=0000 (Falling edge)	-	1.7	-	
		PLS[3:0]=0001 (Rising edge)	-	2.1	-	
		PLS[3:0]=0001 (Falling edge)	-	2.0	-	

Symbol	Parameter	Condition	Min. (3)	Typ.	Max. (3)	Unit
		PLS[3:0]=0010 (Rising edge)	-	2.4	-	
		PLS[3:0]=0010 (Falling edge)	-	2.3	-	
		PLS[3:0]=0011 (Rising edge)	-	2.7	-	
		PLS[3:0]=0011 (Falling edge)	-	2.6	-	
		PLS[3:0]=0100 (Rising edge)	-	3.0	-	
		PLS[3:0]=0100 (Falling edge)	-	2.9	-	
		PLS[3:0]=0101 (Rising edge)	-	3.3	-	
		PLS[3:0]=0101 (Falling edge)	-	3.2	-	
		PLS[3:0]=0110 (Rising edge)	-	3.6	-	
		PLS[3:0]=0110 (Falling edge)	-	3.5	-	
		PLS[3:0]=0111 (Rising edge)	-	3.9	-	
		PLS[3:0]=0111 (Falling edge)	-	3.8	-	
		PLS[3:0]=1000 (Rising edge)	-	4.2	-	
		PLS[3:0]=1000 (Falling edge)	-	4.1	-	
		PLS[3:0]=1001 (Rising edge)	-	4.5	-	
		PLS[3:0]=1001 (Falling edge)	-	4.4	-	
		PLS[3:0]=1010 (Rising edge)	-	4.8	-	
		PLS[3:0]=1010 (Falling edge)	-	4.7	-	
$V_{POR/PDR}$ (1)	Power-on reset threshold	-	-	1.65	-	V
V_{hyst_PDR}	PDR hysteresis	-	-	50	-	mV
$T_{RSTTEMPO}$ (2)	Reset duration	-	-	4.7	-	ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.
3. Drawn from comprehensive evaluation.

Note: The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction

4.3.4 Built-in voltage reference

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 4-4.

Table 4-7 Build-in voltage reference

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Built-in voltage reference	-40°C < T_A < 105°C	-	1.2	-	V
$T_{s\_vrefint}$ (1)	ADC sampling time when readout build-in voltage reference	-	-	11.8	-	us

1. The sampling time is obtained through multiple tests

4.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and connected to a static level - V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting cycle, 24 ~ 48 MHz is 1 waiting cycle).
- The instruction prefetching function is on. When the peripherals are enabled: f_{PCLK1} = f_{HCLK}.

Note: The instruction prefetching function must be set before setting the clock and bus divider.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 4-4.

Table 4-8 Typical current consumption in Run mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled						Typical All peripherals disabled						Unit
				-40°C	0°C	25°C	55°C	85°C	105°C	-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DD}	Supply current in Run mode	HSI is clock source	48M	4.22	4.36	4.43	4.54	4.63	4.70	3.06	3.19	3.25	3.35	3.44	3.51	mA
			24M	3.05	3.16	3.23	3.31	3.39	3.44	2.34	2.45	2.50	2.58	2.66	-	
			12M	2.15	2.27	2.32	2.40	2.46	2.49	1.81	1.91	1.96	2.04	2.09	-	
			6M	1.70	1.79	1.85	1.92	2.00	2.04	1.53	1.62	1.67	1.74	1.82	1.87	
			3M	1.22	1.30	1.35	1.42	1.48	1.52	1.13	1.21	1.26	1.33	1.39	1.43	
			750K	0.87	0.94	0.98	1.04	1.10	1.13	0.84	0.91	0.95	1.01	1.07	1.10	
			375K	0.80	0.87	0.91	0.97	1.03	1.06	0.79	0.86	0.90	0.96	1.02	1.05	
			187.5K	0.77	0.84	0.88	0.94	1.00	1.03	0.77	0.84	0.88	0.93	0.99	1.02	

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled						Typical All peripherals disabled						Unit
				-40°C	0°C	25°C	55°C	85°C	105°C	-40°C	0°C	25°C	55°C	85°C	105°C	
			93.75K	0.76	0.83	0.87	0.92	0.98	1.01	0.75	0.83	0.86	0.92	0.98	1.01	
		HSIDIV is clock source	8M	1.83	1.92	1.70	1.78	1.84	1.88	1.63	1.73	1.50	1.57	1.64	1.68	
			4M	1.68	1.76	1.79	1.51	1.57	1.61	1.56	1.65	1.65	1.39	1.45	1.49	
			2M	1.19	1.28	1.32	1.39	1.46	1.50	1.13	1.22	1.27	1.33	1.40	1.44	
			1M	0.95	1.03	1.07	1.13	1.19	1.23	0.92	1.00	1.04	1.10	1.16	1.20	
			500K	0.83	0.90	0.94	1.00	1.06	1.09	0.81	0.89	0.93	0.99	1.04	1.08	
			125K	0.74	0.81	0.85	0.91	0.96	0.99	0.73	0.80	0.84	0.90	0.96	0.99	
			62.5K	0.72	0.79	0.83	0.89	0.94	0.97	0.72	0.79	0.83	0.89	0.94	0.97	
			31.25K	0.71	0.78	0.82	0.88	0.93	0.97	0.71	0.78	0.82	0.88	0.93	0.96	
		LSI is clock source	40K	0.19	0.21	0.21	0.22	0.23	0.24	0.19	0.20	0.21	0.22	0.23	0.23	

Table 4-9 Typical current consumption in Sleep mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled						Typical All peripherals disabled						Unit
				-40°C	0°C	25°C	55°C	85°C	105°C	-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DD}	Supply current in Sleep mode	HSI is clock source	48M	3.24	3.35	3.41	3.50	3.58	3.61	2.09	2.18	2.24	2.32	2.40	2.43	mA
			24M	2.18	2.27	2.33	2.40	2.48	2.52	1.49	1.57	1.62	1.69	1.76	1.80	
			12M	1.51	1.59	1.64	1.71	1.78	1.81	1.16	1.24	1.29	1.35	1.42	1.46	
			6M	1.67	1.76	1.81	1.89	1.97	2.01	1.50	1.58	1.64	1.71	1.78	1.82	
			3M	1.20	1.29	1.33	1.39	1.46	1.50	1.12	1.20	1.24	1.31	1.37	1.41	
			750K	0.86	0.94	0.98	1.04	1.10	1.13	0.84	0.91	0.95	1.01	1.07	1.10	
			375K	0.80	0.87	0.91	0.97	1.03	1.06	0.79	0.86	0.90	0.96	1.02	1.05	
			187.5K	0.77	0.84	0.88	0.94	0.99	1.03	0.76	0.84	0.88	0.93	0.99	1.02	
			93.75K	0.76	0.83	0.87	0.92	0.98	1.01	0.75	0.82	0.86	0.92	0.98	1.01	
		HSIDIV is clock source	8M	1.30	1.39	1.44	1.51	1.58	1.61	1.11	1.20	1.24	1.31	1.38	1.42	
			4M	1.75	1.81	1.26	1.26	1.33	1.36	1.63	1.69	1.11	1.15	1.21	1.24	
			2M	1.23	1.32	1.37	1.44	1.50	1.54	1.18	1.26	1.31	1.39	1.44	1.48	
			1M	0.97	1.05	1.09	1.15	1.21	1.25	0.94	1.02	1.06	1.12	1.19	1.23	
			500K	0.84	0.91	0.95	1.01	1.07	1.11	0.82	0.89	0.94	1.00	1.06	1.09	
			125K	0.74	0.81	0.85	0.91	0.96	0.99	0.73	0.80	0.84	0.90	0.96	0.99	
			62.5K	0.72	0.79	0.83	0.89	0.94	0.98	0.72	0.79	0.83	0.89	0.94	0.97	
			31.25K	0.71	0.78	0.82	0.88	0.93	0.97	0.71	0.78	0.82	0.88	0.93	0.97	
		LSI is clock source	40K	0.19	0.21	0.21	0.22	0.23	0.24	0.19	0.20	0.21	0.22	0.23	0.24	

Table 4-10 Typical current consumption in stop mode (1)

Symbol	Parameter	Conditions	Typical						Unit
			-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DD}	Supply current in Stop mode	Enter Stop mode after reset, V_{DD}=3.3V	110.19	117.98	121.73	125.54	113.52	118.95	μA

Symbol	Parameter	Conditions	Typical						Unit
			-40°C	0°C	25°C	55°C	85°C	105°C	
	Supply current in Deep Stop mode	Enter Deep Stop mode after reset, V_{DD}=3.3V	5.75	6.20	6.44	6.79	7.76	9.31	

Note 1. The I/O state is an analog input.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode and connected to a static level - V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise specified.
- The given value is calculated by measuring the current consumption.
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient operating temperature and V_{DD} supply voltage conditions are listed in Table 4-4.

Table 4-11 On-chip peripheral current consumption (1)

Symbol	Parameter	Bus	Typical	Unit
I_{DD}	CRC	AHB	0.67	uA/MHz
	GPIOA		0.32	
	GPIOB		0.27	
	TIM1	APB1	5.11	
	TIM3		3.13	
	USART1		1.96	
	TIM14		1.50	
	ADC1		0.73	
	PWR		0.10	
	EXTI		0.09	
	SYSCFG		0.09	
	DBG		0.04	
	WWDG		0.03	

Note1. f_{HCLK} = 48MHz，f_{APB1} = f_{HCLK}, the prescale coefficient of each peripheral is the default value.

Wake up time from low power mode

The wake-up time listed in the table below is measured during the wake-up process of the internal clock HSI. The clock source used to wake up the chip depends on the current operating mode:

Stop or Standby mode: the clock source is the oscillator

Sleep mode: the clock source is the clock used when entering the Sleep mode.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 4-4.

Table 4-12 Wake up time from low power mode

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wake up from Sleep mode	System clock is HSIDIV	3.22	μs
t_{WUSTOP}	Wake up from Stop mode	System clock is HSIDIV	26.65	μs
$t_{WUDEEPSTOP}$	Wake up from Deep Stop mode	System clock is HSIDIV	28.88	μs

4.3.6 External clock source characteristics

High-speed external user clock generated from an external source

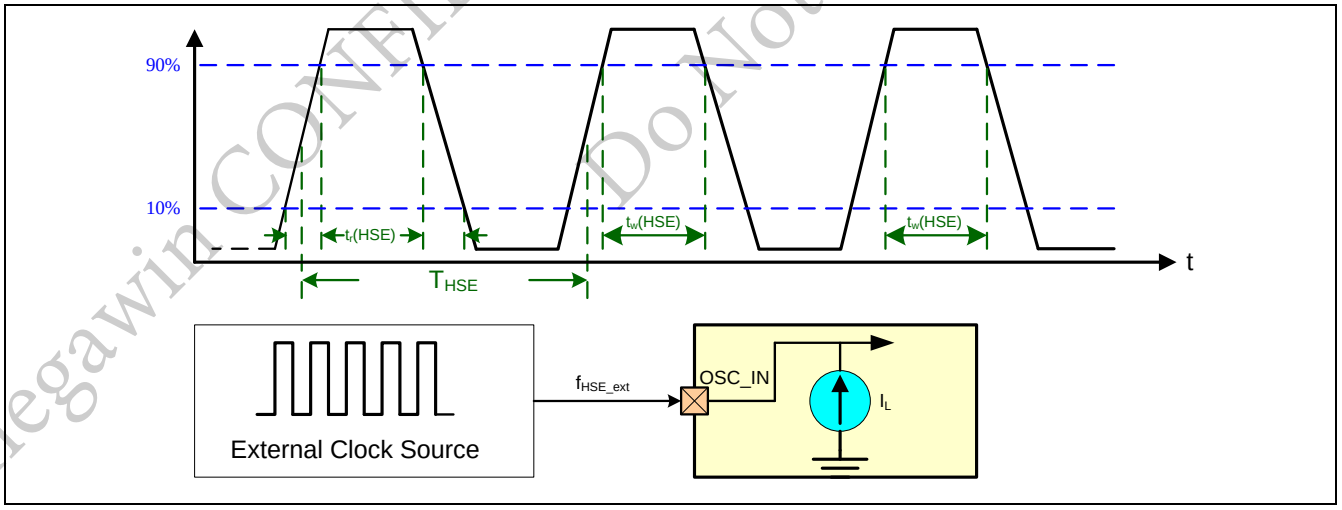
The characteristic parameters given in the following table are measured by a high-speed external clock source, and the ambient temperature and power supply voltage meet General operating conditions.

Table 4-13 High-speed external user clock characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock source frequency (1)	-	-	8	48	MHz
V_{HSEH}	OSC_IN input high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time (1)	-	20	-	-	ns

Note 1: Guaranteed by design, not tested in production

Figure 4-6 High-speed external clock source AC timing diagram



4.3.7 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 4-14 HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
ACC_{HSI} (3)	HSI oscillator deviation	T_A = 0°C ~ 55°C	-1	-	1	%
		T_A = -40°C ~ 105°C	-2	-	2	%
$T_{stab(HSI)}$ (2)	HSI oscillator startup time	-	-	-	20	μs
$I_{DD(HSI)}$ (2)	HSI oscillator power consumption	-	-	480	-	μA

Note1. V_{DD} = 3.3V, TA = - 40°C ~ 105°C, unless otherwise specified.

Note2. Guaranteed by design, not tested in production.

Note3. Drawn from comprehensive evaluation.

Low-speed internal (LSI) oscillator

Table 4-15 LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	-	-	40	-	KHz
ACC_{LSI} (3)	LSI oscillator deviation	T_A = 0°C ~ 55°C	-15	-	15	%
		T_A = -40°C ~ 105°C	-20	-	20	%
$T_{stab(LSI)}$ (2)	LSI oscillator startup time	-	-	-	100	μs
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	-	-	1	-	μA

Note1. V_{DD} = 3.3V, T_A = -40°C ~ 105°C, unless otherwise stated.

Note2. Guaranteed by design, not tested in production.

Note3. Drawn from comprehensive evaluation.

4.3.8 Memory characteristics

Table 4-16 Flash memory characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	16-bit programming time	-	-	37.24	-	μs
t_{ERASE}	Page (1024 bytes) erase time	-	4	-	6	ms
t_{ME}	Mass erase time	-	30	-	40	ms
I_{DD}	Supply current	Read mode	-	-	1.5	mA
		Write mode	-	-	2	mA
		Erase mode	-	-	1	mA

Table 4-17 Flash memory endurance and data retention (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{END}	Endurance	T_A = 105°C	100000	-	-	Cycles
T_{DR}	Data retention	T_A = 25°C	25	-	-	Years

4.3.9 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 4-4 are used for tests. All I/O ports are CMOS compatible.

Table 4-18 I/O static characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low level input voltage	-	-	-	0.3 * V_{DD}	V
V_{IH}	High level input voltage	-	0.7 * V_{DD}	-	-	V
V_{hy}	Schmitt trigger hysteresis (1)	-	0.1 * V_{DD}	-	-	V
I_{lkg}	Input leakage current (2)	-	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor (3)	V_{IN} = V_{SS}	-	60	-	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)	V_{IN} = V_{DD}	-	60	-	kΩ
C_{IO}	I/O pin capacitance	-	-	-	10	pF

Note1. Drawn from comprehensive evaluation, not tested in production.

Note2. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.

Note3. The pull-up and pull-down resistors are poly resistors.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

In the user application, the number of I/O pins must ensure that the drive current must be limited to respect the absolute maximum rating specified in Table 4-1:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum operating current that the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are provided under the ambient temperature and VDD supply voltage in accordance with the conditions summarized in Table 4-4. All I/O ports are CMOS compatible.

Table 4-19 Output voltage static characteristics

Symbol	Parameter	Conditions	Typical	Unit
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA，V_{DD}=2.0V	0.36	V
V_{OH} (2)	Output high voltage		1.56	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA，V_{DD}=3.3V	0.2	
V_{OH} (2)	Output high voltage		3.01	

Symbol	Parameter	Conditions	Typical	Unit
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 8mA，V_{DD} =3.3V	0.27	
V_{OH} (2)	Output high voltage		2.91	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA，V_{DD}=5.0V	0.15	
V_{OH} (2)	Output high voltage		4.75	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 8mA，V_{DD} =5.0V	0.2	
V_{OH} (2)	Output high voltage		4.67	
V_{OL} (2)	Output low voltage	$\|I_{IO}\|$=20mA，V_{DD} =5.0V	0.54	
V_{OH} (2)	Output high voltage		4.18	

Note1. The current I_{IO} drawn by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VSS}.

Note2. The current I_{IO} output by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VDD}.

Note3. Resulted from comprehensive evaluation.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in the following figure and table, respectively.

Unless otherwise stated, the parameters listed in the following table are provided under the ambient temperature and supply voltage in accordance with the condition Table 4-4.

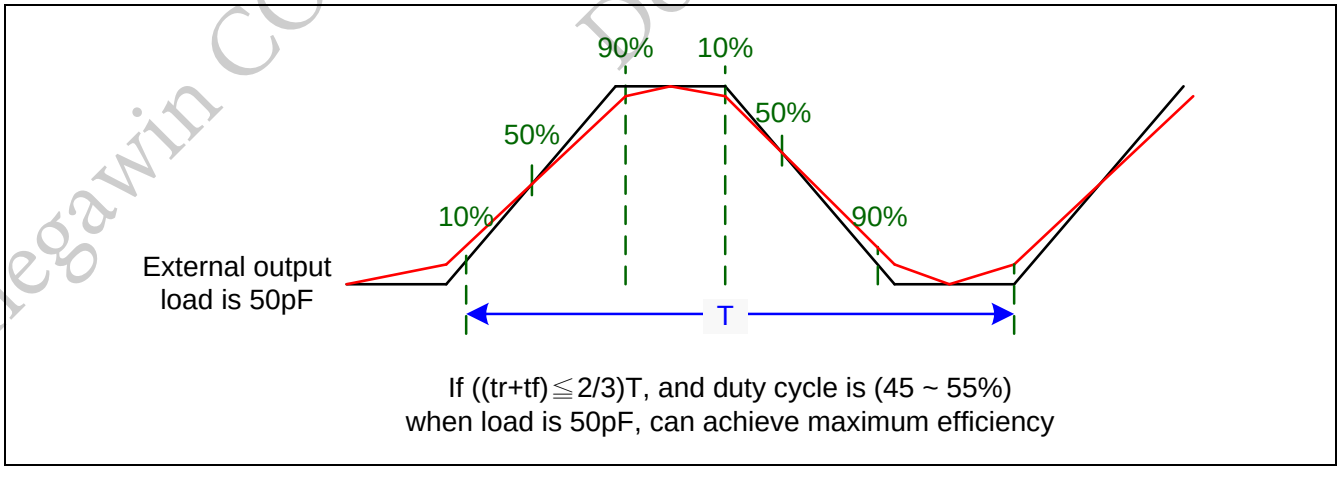
Table 4-20 I/O AC characteristics (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
$t_{f(IO)out}$	Output fall time	C_L = 50pF V_{DD}=3.3V	5.8	ns
$t_{r(IO)out}$	Output rise time		5.6	ns

Note1. The maximum frequency is defined in Figure 4-7.

Note2. Guaranteed by design, not tested in production.

Figure 4-7 I/O AC characteristics



4.3.10 Timer characteristics

The parameters listed in the following table are guaranteed by design.

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see section 4.3.9 I/O port characteristics.

Table 4-21 TIMx (1) characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	20.8	-	ns
f_{EXT}	External clock frequency of channel 1 to 4	-	0	-	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0208	1365.3	us
t_{MAX_COUNT}	Maximum possible counter value (TIM_PSC adjustable)	-	-	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	-	1365.3	us
t_{MAX_IN}	TIM maximum input frequency	-	-	48	MHz

Note1. Guaranteed by design, not tested in production.

4.3.11 ADC characteristics

Unless otherwise specified, the parameters in the table below are measured under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions summarized in Table 4-4.

Table 4-22 ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S (1)	Sampling frequency	VDD > 2.8V			1	MHz
		VDD <=2.8V	-	-	400	KHz
f_{TRIG} (1)	External trigger frequency (3)	f_{ADC} = 16MHz	-	-	1	MHz
		-	-	-	16	$1/f_{ADC}$
V_{AIN} (2)	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN} (1)	External input impedance	-	See equation 2			kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	1.5	kΩ
C_{ADC} (1)	Internal sample and hold capacitance	-	-	-	10	pF
t_{STAB} (1)	Stabilization time	-	-	-	10	μs
t_{latr} (1)	Delay between trigger and conversion start	-	-	-	-	$1/f_{ADC}$
t_S (1)	Sampling time	f_{ADC} = 16MHz	0.156	-	15.031	μs
		-	2.5	-	240.5	$1/f_{ADC}$
t_{CONV} (1)	Total conversion time (including sampling time)	f_{ADC} = 16MHz	0.9375	-	15.8125	μs
		-	15 ~ 253 (sampling t_S + successive approximation 12.5)			$1/f_{ADC}$
ENOB	Effective number of bits	-	-	10.5	-	bit

Note1. Guaranteed based on test during characterization. Not tested in production.

Note2. Guaranteed by design, not tested in production.

Note3. In this product, VREF+ is internally connected to VDDA， VREF− is internally connected to VSSA.

Note4. Guaranteed by design, not tested in production.

Note5. For external trigger, a delay of $1/f_{ADC}$ must be added.

AIN Input impedance

Equation 2

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The formula above is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (12-bit resolution), is derived from tests under f_{ADC} = 15MHz.

Table 4-23 Maximum RAIN at fADC = 15MHz (1)

T_S (cycles)	t_S (μs)	Maximum R_{AIN} (kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

Note1. Guaranteed by design. Not tested in production.

Table 4-24 ADC static parameters (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
ET	Comprehensive error	f_{PCLK1} = 48MHz, f_{ADC} = 16MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C	-2.1 ~ 3.8	LSB
EO	Offset error		-2.4 ~ 1.1	
EG	Gain error		-0.6 ~ 1.0	
ED	Differential linearity error		-0.8 ~ 1.0	
EL	Integral linearity error		-2.8 ~ 1.5	

Note1. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in section 0

Absolute maximum rating does not affect the ADC accuracy.

Note2. Guaranteed based on characterization. Not tested in production.

The implications of the ADC static parameters are seen below, and the corresponding schematic diagram is shown in Figure 4-8.

- ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.
- EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.
- EG = Gain error: The deviation between the last ideal transition and the last actual transition.
- ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.
- EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

Figure 4-8 Schematic diagram of ADC static parameters

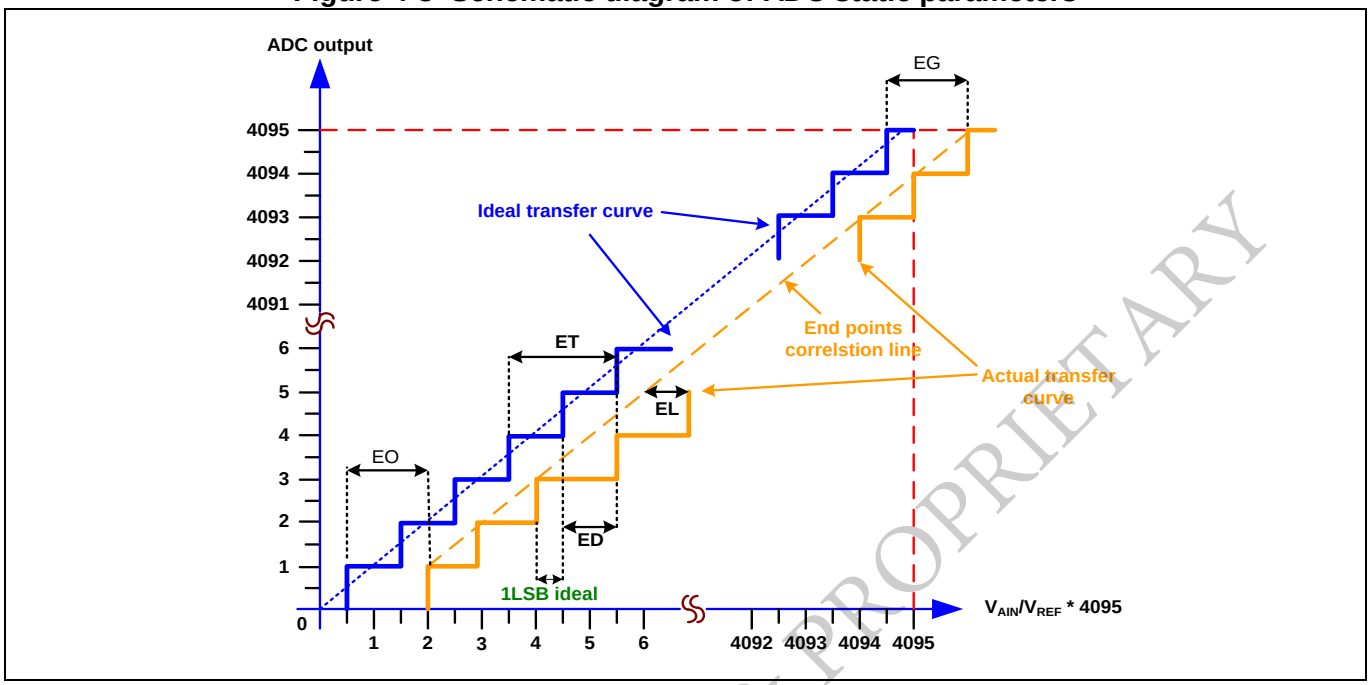
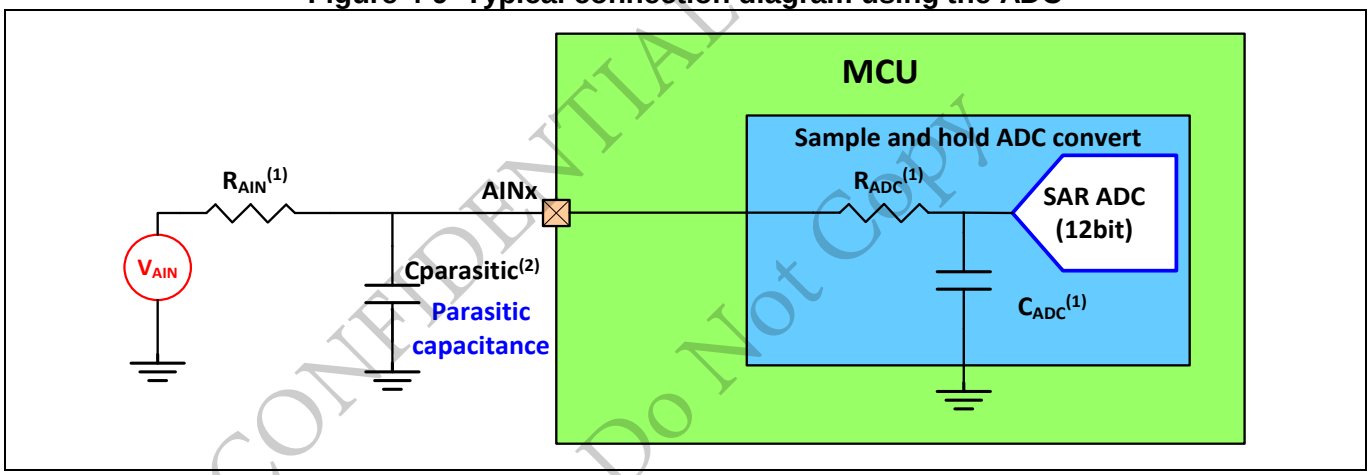


Figure 4-9 Typical connection diagram using the ADC



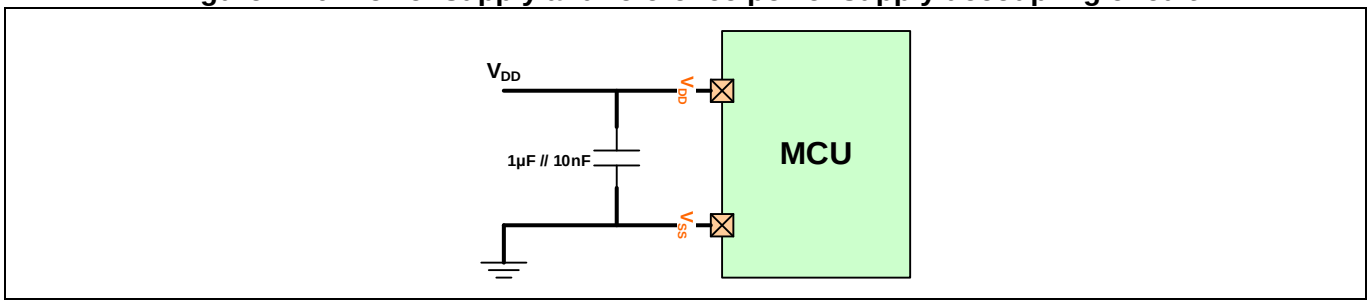
Note1. See Table 4-22 for the values of R_{AIN}, R_{ADC} and C_{ADC}.

Note2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply must be connected as shown below. The 10nF capacitor in the figure must be a ceramic capacitor (good quality) , and they should be as close as possible to the MCU chip.

Figure 4-10 Power supply and reference power supply decoupling circuit



4.4 Operation Range for MCD

Table 4-25 Operating Ranges for MCD
(Ta = -40 to 105 °C Unless otherwise specified)

Characteristics		Symbol	Min.	Typ.	Max.	Unit
VM pin power supply voltage1		$V_{M\ (opr1)}$	9	12	16	V
VM pin power supply voltage2 (Note1)		$V_{M\ (opr2)}$	5	—	9	V
VM pin power supply voltage3 (Note2)		$V_{M\ (opr3)}$	10.8	12	16	V
Input PWM frequency		f_{TSP}	1	—	100	kHz
Input SPI CLK frequency		f_{SCK}	15	—	500	kHz
Input voltage	HP, HM	V_{IN}	0.1	—	V_{REG} - 2.0	V
	DIR, SPD, BRAKE, OC		-0.3	—	5.5	V

Note 1: Electrical characteristics are only for reference because the variation of electrical characteristics becomes large.
Note 2: For NVM writing.

Table 4-26 NVM Characteristics for MCD

Characteristics	Conditions	Min.	Max.	Unit
Program / Erase cycle	Tj = 0 to 90 °C	10	—	Cycle

4.4.1 Electrical Characteristics for MCD

Table 4-27 Electrical Characteristics for MCD
(VM = 12 V, Ta = 25°C unless otherwise specified)

Characteristics		Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply current		I_{VM}	V_M =12 V, VREG = OPEN Hall signal input =100 Hz, Output = OPEN	—	10	12.5	mA
		I_{STBY}	VM = 12 V, Standby mode	—	0.33	0.5	mA
VREG pin voltage		V_{REG}	VM = 12 V, IVREG = 0 to 10 mA	4.5	5.0	5.5	V
Charge pump voltage		V_{CP}	VM – VCP: 0.1 µF, CPP – CPM: 0.01 µF VM = 9 V	V_M + 7.6	V_M + 8.1	V_M + 8.6	V
MOSFET gate signal voltage		$V_{O(H)-(H)}$	I_{OUT} of GHU, GHV, GHW = -1 mA	V_{CP} – 0.5	—	V_{CP}	V
		$V_{O(H)-(L)}$	I_{OUT} of GHU, GHV, GHW = 1 mA	—	—	0.6	V
		$V_{O(L)-(H)}$	I_{OUT} of GLU, GLV, GLW = -1 mA	6.9	7.7	8.5	V
		$V_{O(L)-(L)}$	I_{OUT} of GLU, GLV, GLW = 1 mA	—	—	0.6	V
Internal OSC frequency(1)		f_{OSC}	—	11.676	12.00	12.12	MHz
Output PWM frequency		$f_{PWM\ (1)}$	f_{OSC} = 12 MHz, PWMSEL [2:0] = 000	—	23.4	—	kHz
		$f_{PWM\ (2)}$	f_{OSC} = 12 MHz, PWMSEL [2:0] = 011	—	187.5	—	kHz
Hall input signal	Common phase input voltage range	V_{HCMR}	—	0.1	—	V_{REG} – 2.0	V
	Input amplitude range	V_H	—	40	—	—	mV
	Input current	I_{HIN}	—	—	—	1	µA
	Hysteresis (+) voltage	V_{HHYS+}	—	—	+8	—	mV
	Hysteresis (-) voltage	V_{HHYS-}	—	—	-8	—	mV
SPD pin	Standby mode	$V_{STBY(L)}$	Standby mode switching voltage	1.00	1.15	—	V

Characteristics		Symbol	Conditions	Min.	Typ.	Max.	Unit
	control voltage	$V_{STBY(H)}$	Standby mode releasing voltage	—	1.25	1.40	V
		$V_{STBY\ (hys)}$	Hysteresis voltage	—	100	—	mV
	Input current	I_{SPD}	V_{SPD} = 0 V to VREG	—	—	1	μA
SPD pin During PWM duty input	Input voltage	$V_{TSP(H)}$	High voltage	2.0	—	5.5	V
		$V_{TSP(L)}$	Low voltage	-0.3	—	1.0	V
		$V_{TSP\ (hys)}$	Hysteresis voltage	—	200	—	mV
	Input frequency	f_{TSP}	—	1	—	100	kHz
	100 % duty detection time	$T_{duty\ (100)}$	—	—	1.5	—	ms
	0 % duty detection time	$T_{duty\ (0)}$	—	—	100	—	ms
SPD pin During analog voltage input	Input voltage	$V_{VSP(H)}$	ADC = 512 (100%)	3.9	4.0	4.1	V
		$V_{VSP(L)}$	ADC = 0 (0%)	1.4	1.5	1.6	V
	ADC response time	t_{ADC}	—	—	—	10	ms

Note 1: The internal OSC frequency is not determined for the first version and will be frozen in mass production.

Table 4-27 Electrical Characteristics for MCD(Continue)

Characteristics		Symbol	Conditions	Min.	Typ.	Max.	Unit
DIR pin	Input voltage	$V_{DIR(H)}$	High voltage	2.0	—	5.5	V
		$V_{DIR(L)}$	Low voltage	-0.3	—	1.0	V
		$V_{DIR\ (hys)}$	Hysteresis voltage	—	200	—	mV
	Input current	$I_{DIR(H)}$	V_{DIR} = 5 V	80	100	120	μA
		$I_{DIR(L)}$	V_{DIR} = 0 V	—	—	1	μA
BRAKE pin	Input voltage	$V_{BRK(H)}$	High voltage	2.0	—	5.5	V
		$V_{BRK(L)}$	Low voltage	-0.3	—	1.0	V
		$V_{BRK\ (hys)}$	Hysteresis voltage	—	200	—	mV
	Input current	$I_{BRK(H)}$	V_{BRAKE} = 5 V	80	100	120	μA
		$I_{BRK(L)}$	V_{BRAKE} = 0 V	—	—	1	μA
FG pin	Output low voltage	$V_{OFG(L)}$	I_{FG} = 5 mA	—	0.15	0.30	V
	Output leakage current	I_{OFGR}	V_{FG} = 18 V	—	1.5	5.0	μA
ALERT pin	Output low voltage	$V_{OAL(L)}$	I_{ALERT} = 5 mA	—	0.15	0.30	V
	Output leakage current	I_{OALR}	V_{ALERT} = 18 V	—	—	1.0	μA
Voltage limit for the current sense resistor		V_{OC}	Voc = 0.250 V	0.2	0.25	0.3	V
			Voc = 0.125 V	0.1	0.125	0.15	V
Voltage limit for the over current protection		V_{ISD}	V_{ISD} = 0.5 V	0.4	0.5	0.6	V
			V_{ISD} = 1.0 V	0.8	1.0	1.2	V
Current for the detection of OC pin opening		$I_{OC(D)}$	$V_{OC(D)}$ = 0 V	—	0.1	1	μA
Thermal shutdown	Shutdown temperature	$T_{TSD(D)}$	In rising temperature (Design value)	—	170	—	°C
	Release hysteresis temperature	ΔT_{TSD}	In falling temperature (Design value)	—	40	—	°C
	Release temperature	$T_{TSD(R)}$	In falling temperature (Design value)	—	130	—	°C
Over voltage protection	Switching voltage (from sine-wave drive to 150° commutation)	$V_{OV(D)}$	In V_M rising	16.5	17.2	17.9	V
	Recovery hysteresis voltage (from 150° commutation to sine-wave drive)	ΔV_{OV}	In V_M falling	—	400	—	mV

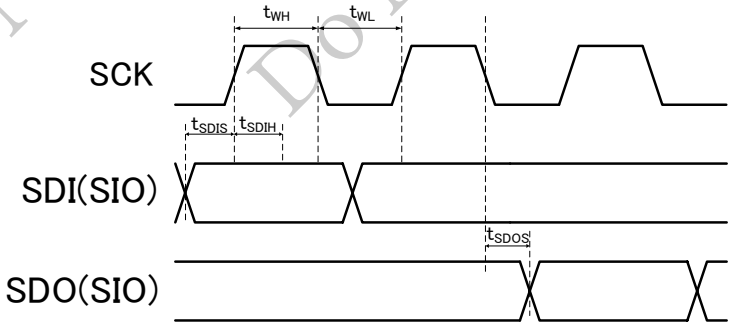
	Recovery voltage (from 150° commutation to sine-wave drive)	$V_{OV(R)}$	In V_M falling	16.1	16.8	17.5	V
Under voltage protection for VM	UVLO operating voltage	$V_{MUV(D)}$	In V_M falling	3.7	3.9	4.1	V
	UVLO hysteresis voltage	ΔV_{MUV}	In V_M rising	—	300	—	mV
	UVLO release voltage	$V_{MUV(R)}$	In V_M rising	4.0	4.2	4.4	V
Under voltage protection for V_{REG}	UVLO operating voltage	$V_{RUV(D)}$	In V_{REG} falling	—	3.7	—	V
	UVLO hysteresis voltage	ΔV_{RUV}	In V_{REG} rising	—	300	—	mV
	UVLO release voltage	$V_{RUV(R)}$	In V_{REG} rising	—	4.0	—	V
Under voltage protection for charge pump	Under voltage protection operating voltage	$V_{CUV(D)}$	In the voltage between VCP pin and VM pin falling, VM ≥ 5.5 V	—	3.7	—	V
	Under voltage protection hysteresis voltage	ΔV_{CUV}	In the voltage between VCP pin and VM pin rising, VM ≥ 5.5 V	—	300	—	mV
	Under voltage protection release voltage	$V_{CUV(R)}$	In the voltage between VCP pin and VM pin rising, VM ≥ 5.5 V	—	4.0	—	V

Table 4-28 Serial I/F for MCD

(VM = 12 V, Ta = 25 °C unless otherwise specified)

Characteristics		Symbol	Conditions	Min.	Typ.	Max.	Unit
SCK	Input voltage	$V_{SCK(H)}$	High voltage	2.0	—	5.5	V
		$V_{SCK(L)}$	Low voltage	-0.3	—	1.0	V
		$V_{SCK\ (hys)}$	Hysteresis voltage	—	100	—	mV
	Input frequency	f_{SCK}	—	15	—	500	kHz
	High period	t_{WH}	—	1	—	—	µs
	Low period	t_{WL}	—	1	—	—	µs
SDI(SIO)	Setup period	t_{SDIS}	—	1	—	—	µs
	Hold period	t_{SDIH}	—	500	—	—	ns
SDO(SIO)	Setup period	t_{SDOS}	—	—	—	500	ns

Figure 4-11 Serial I/F timing chart



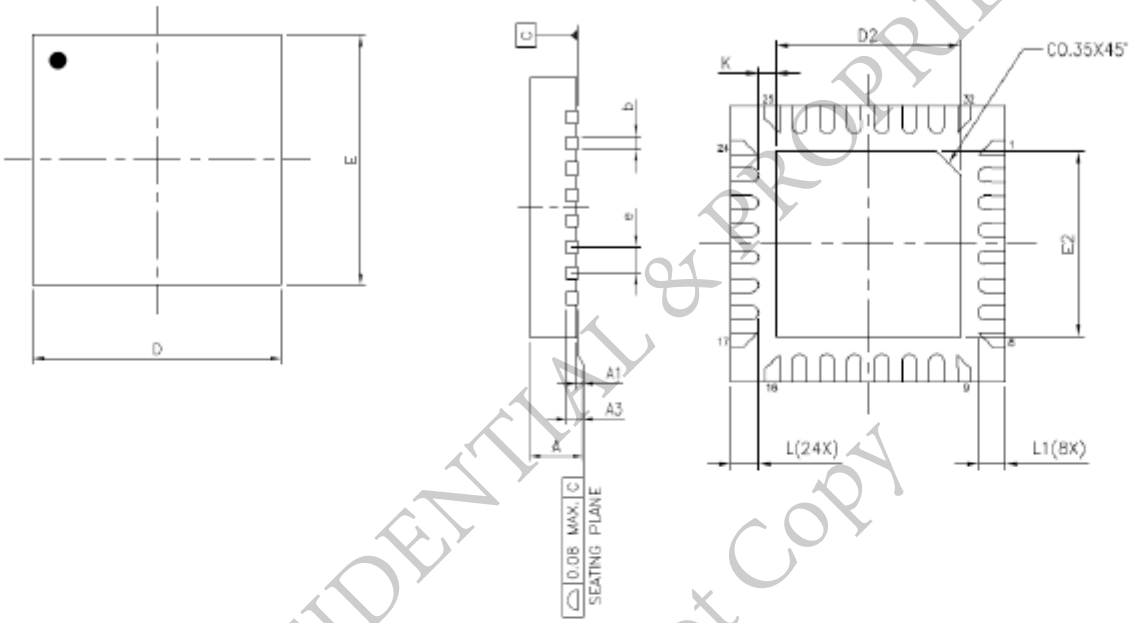
5 Package dimensions

5.1 QFN32 (4x4x0.85mm)

Figure 5-1 QFN32 package dimension

Package Dimension

QFN32 (4x4x0.85 mm) (with heat sink)



Unit	mm			Inch		
JEDEC	N/A			N/A		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	----	0.001	0.002
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	4.00 BSC			0.157 BSC		
E	4.00 BSC			0.157 BSC		
e	0.40 BSC			0.016 BSC		
L	0.25	0.30	0.35	0.010	0.012	0.014
L1	0.23	0.28	0.33	0.009	0.011	0.013
K	0.20	----	----	0.008	----	----
D2	2.65	2.70	2.75	0.104	0.106	0.108
E2	2.65	2.70	2.75	0.104	0.106	0.108

6 Revision history

Table 6-1 Revision history

Rev	Descriptions	Date
V0.1	1. Preliminary.	2025/07/01
V0.2	2. Update table and figure link in the catalog.	2025/07/11
V0.3	3. Update Figure 4-3	2025/07/18

7 Disclaimers

Herein, Megawin stands for "***Megawin Technology Co., Ltd.***"

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