

MG32F10x Layout Suggestion

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1 Printed circuit board

For technical reasons, it is preferable to use a multilayer PCB with a dedicated independent grounding layer (VSS) and dedicated independent power supply layer (VDD) to provide better coupling and shielding effect. In many applications, limited by economic conditions that cannot use such printed circuit boards, so it is necessary to ensure a good grounding and power supply structure.

2 Component location

In order to reduce cross-coupling on the PCB, different circuits need to be separated according to their impact on EMI when designing the layout. For example, high current circuits, low voltage circuits and digital devices.

3 Grounding and power supply(VSS/VDD)

Each module (noisy circuits, low sensitivity circuits, digital circuits) should be grounded individually, and all the ground should eventually be connected at one point. Avoid or minimize loop areas. To reduce the area of the power supply loop, the power supply should be as close to the ground as possible. This is because the power supply loop acts as an antenna, acting as a transmitter and receiver of EMI. Areas of the PCB without components need to be filled to provide good shielding (especially for single-layer PCB).

4 Decoupling

All pins need to be properly connected to the power supply. These connections, including pads, wires and Vias, shall have as little impedance as possible. A common approach is to increase the width of the line, including the use of a separate supply layer in a multi-layer PCB. At the same time, each power pin on the MG32F10x should be paralleled with a decoupled filter ceramic capacitor C(100nF) and chemical capacitor C(10 μ F). These capacitors should be as close to the power/ground pins as possible; Or on another layer of the PCB, under the power/ground pin. Typical values range from 10nF to 100nF, depending on the needs of practical applications. Figure 1 shows a typical layout of such power/ground pins.

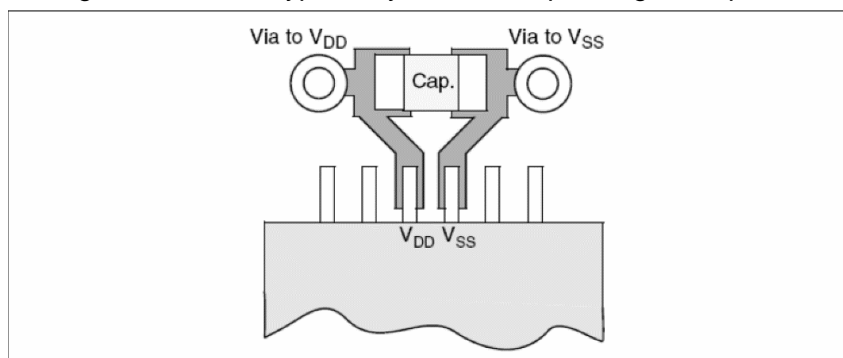


Figure 1 typical layout of VDD /VSS pins

5 Power supply scheme

The circuit is powered by a stable power supply VDD.

- Notify:

- If ADC is used, the VDD range must be between 2.4V and 3.6V
- If ADC is not used, the VDD ranges from 2V to 3.6V

- The VDD pins must be connected to a VDD power supply with external stabilized capacitors (11 100nF ceramic capacitors and one tantalum capacitor (4.7μF minimum, 10μF typical)).

- The VBAT pin must be connected to an external battery (1.8V < VBAT < 3.6V). If no external battery is available, this pin must be connected to the VDD power supply along with a 100nF ceramic capacitor

- VDDA pins must be connected to two external stabilized capacitors (10nF ceramic capacitor +1μF tantalum capacitor).

- VREF+ pins can be connected to VDDA external power supplies. If a separate external reference voltage is used on VREF+, a 10nF and a 1μF capacitor must be connected to the pins. In all cases, VREF+ must be between 2.4V and VDDA.

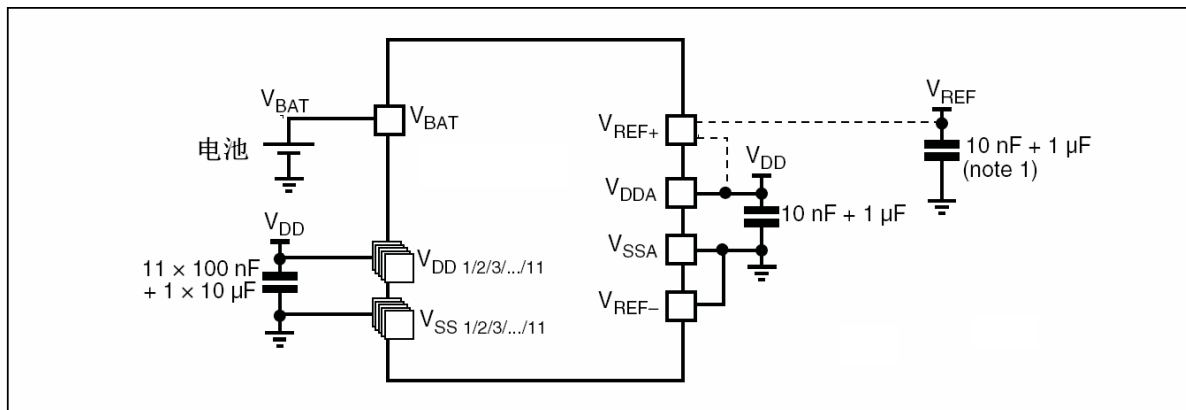


Figure 2 power supply scheme

Note 1. Optional. If a separate external reference voltage is used on VREF+, two capacitors (10nF and 1μF) must be connected.

Note 2. VREF+ connect to VDDA or VREF .

6 Other signals

In practical applications, EMC performance can be improved by paying attention to the following points:

- Signals that are affected by temporary disturbances (such as interrupt or shaking signals, rather than LED commands)

For these signals, laying the ground around the signal line, shortening the line distance, eliminating adjacent noise and sensitive wiring can improve EMC performance.

For digital signals, the best possible signal-property margin must be achieved to effectively distinguish between the two logical states (Raise logic '1' as high as possible and lower logic '0' as low as possible). A slow Schmidt trigger is recommended to eliminate the parasitic state.

- When wiring, the 3W principle should be met as far as possible, and the wiring should be kept away from adjacent lines as far as possible to reduce coupling and interference. If ADC and CMP require high precision, the wire of ADC and CMP should be around with ground.

- Noise signal (clock, etc.)
- Sensitive signal (high resistance, etc.)

7 Unused IO and its properties

All microcontrollers are designed for a variety of applications, and common applications do not use all microcontroller resources.

To improve EMC performance, unused clocks, timers, or I/O pins need to be handled accordingly. For example, I/O ports should be set to '0' or '1' (pull-up or pull-down for unused I/O pins). Modules that are not used should be disabled.

8 Clock

To minimize parallel wiring between LSE and HSE. In figure 3, LSE and HSE are directly separated when they are led out from the pad.

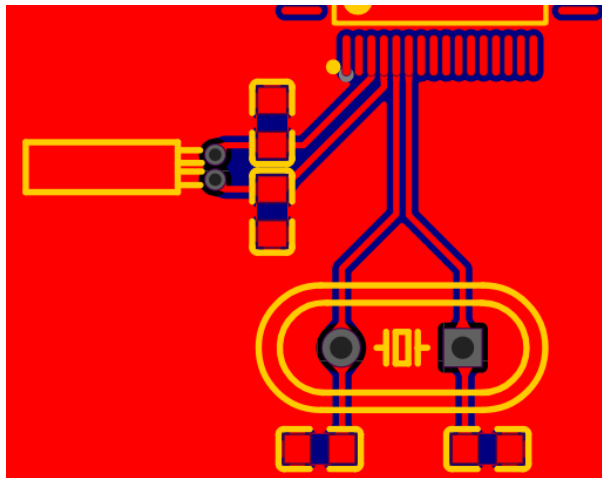


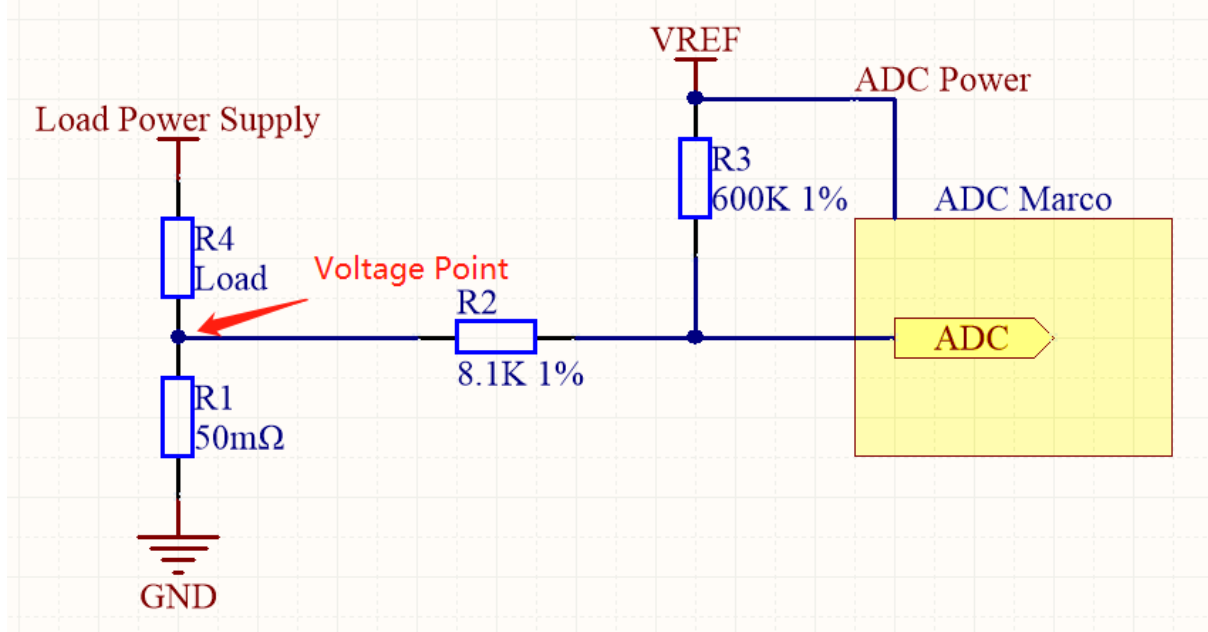
Figure 3 LSE and HSE layout

9 Analog signal

The analog signal is separated from the digital signal, and the analog signal needs to be shielded by the ground line, so that the sampling accuracy can be guaranteed as much as possible.

When the ADC analog voltage input is $<50\text{mV}$ while using MG32F103 and MG32F104 series, the sample circuit needs to be modified. The picture below is the reference design.

The sample circuit needs add R2 and R3 as below. The resistance of R1 can be modified, but the voltage of the voltage point in the picture must be $>3.2\text{mV}$.



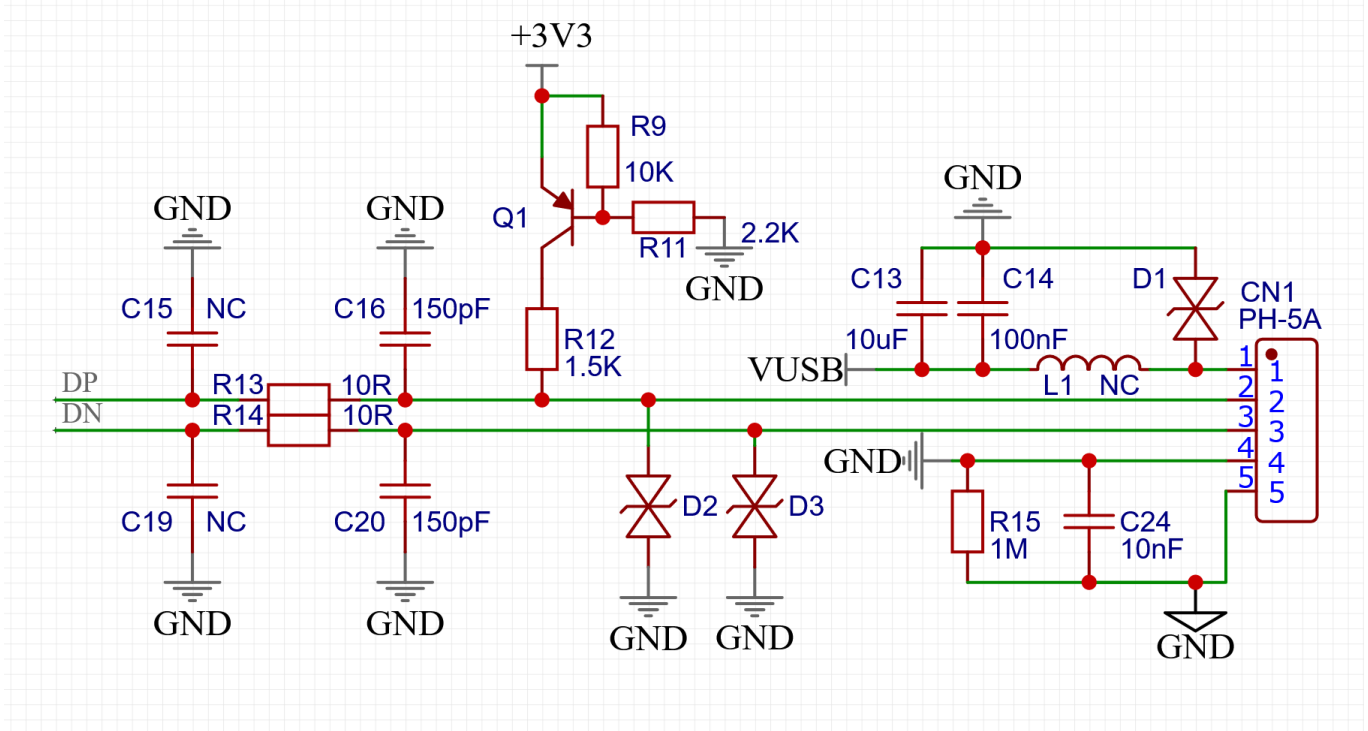
10 EMI

1. Make sure the power rating is suitable for the application and is optimized using a decoupling capacitor.
2. Provide sufficient filter capacitors on the power supply. High capacity/bypass and decoupling capacitors shall have low equivalent series inductance (ESL).
3. Create a ground plane if space is available on the wiring layer. These ground areas are connected to the ground plane through Vias.
4. Keep the current loop as small as possible. Add as many decoupling capacitors as possible.
5. The differential line pair must match the line length, otherwise it will result in timing offset, reduced signal quality, and increased EMI.
6. Differential routing is required to be on the same plate layer, because the impedance and hole difference between different layers will reduce the effect of differential mode transmission and introduce common mode noise.
7. Do not have Vias for high-speed signal routing. Ensure that the ground plane at the rear is complete, and shorten the wires routing distance away from adjacent wires. If the USB interface chip needs a series end resistor or D line is connected to a pull resistor. Be sure to place these resistors as close to the chip as possible.
8. The power pin of each VDD in MCU should leave 2 capacitor: 1uF and 0.1uF as far as possible
9. SPI or IIC communication line, each signal line string a resistance of about 10R, reserved a 120PF

capacitor. The signal line should be as short as possible.

10. Crystal wiring should be short enough, do not route the signal line on the back of the crystal, to ensure that the crystal ground plane is complete. If the layout allows, more ground Vias should be drilled around the crystal oscillator.

Schematic diagram design reference.



1. The pull up of DP wire needs to be controlled by triode. Make sure the circuit to the DP line is short enough.
2. The D1, D2 and D3 TVS need to be placed close to the USB port.
3. PIN1 is the power supply, a 10uF and 10nF should be placed near to PIN1 for filtering.
4. The distance between DP DN and USB port should be as short as possible.