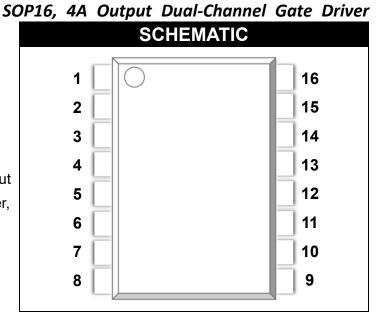


#### Description

The MPCS-3922 is isolated dual-channel gate drivers with 4A peak output current. It is designed to drive power MOSFETs, IGBTs, and SiC MOSFETs up to 5-MHz with well performanced propagation delay and pulse-width distortion. The input is electrically isolated from the two output drivers by a 5.7-kVRMS reinforced isolation barrier, offering at least 50KV/us common-mode transient immunity (CMTI). The internal isolation between the two secondary-side drivers supports a maximum working voltage of 1500 VDC. Each driver can be configured as either two low-side drivers, two high-side drivers, or a half-bridge driver with adjustable dead time (DT). A disable pin will deactivate both outputs when set to high, while leaving it open or grounding it allows normal operation. As a safety feature, primary-side logic failures will force both outputs to a low state.

### Applications

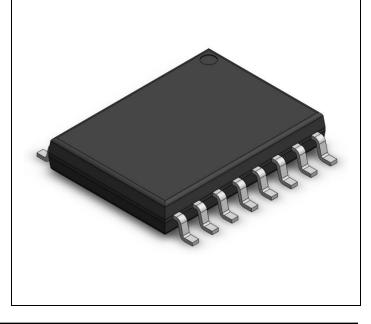
- Isolated converters in DC-DC and AC-DC power supplies
- AC and brushless DC motor drives
- Industrial inverters and Uninterruptible Power Supply (UPS)



### PIN DEFINITION

1.INA	16.Vdda
<b>2.IN</b> в	15.OUT <sub>A</sub>
3.Vcci	14.Vssa
4.GND	13.NC
5.DISABLE	12.NC
6.DT	11.V <sub>DDB</sub>
7.NC	10.OUT <sub>B</sub>
8.Vcci	9. V <sub>SSB</sub>

### PACKAGE OUTLINE



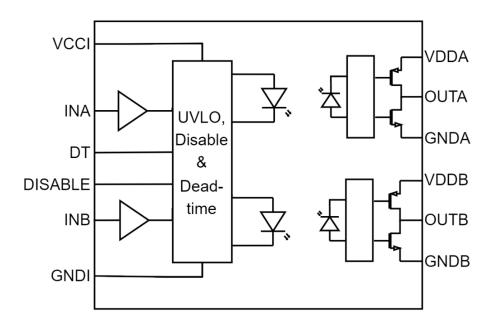


#### SOP16, 4A Output Dual-Channel Gate Driver

#### Features

- dual low-side, dual high-side or half-bridge driver
- Operating temperature range -40 to +110°C
- Switching parameters:
  - 19ns typical propagation delay
  - 10ns minimum pulse width
  - 5ns maximum delay matching
  - 6ns maximum pulse-width distortion
- Common-mode transient immunity (CMTI) greater than 50KV/us
- 4A peak source, 4A peak sink output
- Available in SOP16 package
- 3V to 18V input VCCI range
- Up to 30V VDD output drive supply
- Programmable overlap and dead time
- Rejects input pulses and noise transients shorter than 5 ns
- Fast disable for power sequencing

#### **Internal Circuit**





# SOP16, 4A Output Dual-Channel Gate Driver

SOP16, 4A Output Dudi-Channel Gate Div								
A	<b>BSOLUTE MA</b>		ATINGS					
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE			
Storage Temperature	T <sub>stg</sub>	-55	125	°C				
Operating Temperature	T <sub>A</sub>	-40	110	°C				
Output IC Junction Temperature	TJ	-	125	°C				
Input Bias Pin Supply Voltage	VCCI to GND	-0.3	20	V				
Output Supply Voltage	(VDDA - VSSA)	-0.3	30	V				
	(VDDB - VSSB)	0.0	50	v				
	OUTA to VSSA	-0.3	V <sub>DDA</sub> +0.3	V				
	OUTB to VSSB	-0.5	V <sub>DDB</sub> +0.3	v				
Output Voltage	OUTA to VSSA		V <sub>DDA</sub> +0.3					
	OUTB to VSSB	-2	V <sub>DDA</sub> +0.3 V <sub>DDB</sub> +0.3	V				
	Transient for 200 ns		V DDB +0.3					
	INA, INB, DIS, DT	-0.3	Vcci +0.3	V				
Input Signal Voltage	To GND	-0.5	VCCI +0.3	v				
input Signal Voltage	INA, INB	-5	Vcci +0.3	V				
	Transient for 50 ns	-0	VCCI <b>+0.3</b>	v				
Channel to Channel Voltage	VSSA - VSSB		1500	V				
Channel to Channel Voltage	VSSB - VSSA	-	1500	v				

<b>RECOMMENDED OPERATION CONDITIONS</b>								
PARAMETER	SYMBOL	MIN.	MAX.	UNIT				
Input Supply Voltage	VCCI	3	18	V				
Output Bias Supply Voltage	VDDA, VDDB	15	30	V				
Input Voltage	INA, INB, DIS, DT	0	V <sub>VCCI</sub>	V				
Operating Temperature	TA	-40	110	°C				



$\square$ –			SOP16	5, 4A	Outpu	t Dual-Channel Gate	Driver		
ELEC	TRICAL	OPTI	CAL C	HAR	ACTER	RISTICS			
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	NOTE		
		SUPPL	Y CURR	ENTS					
VCCI quiescent current	Ivcci	-	2.5	3	mA	$V_{\text{INA}}=0~V,~V_{\text{INB}}=0~V$			
VDDA and VDDB quiescent	IVDDA		2	3	mA	$V_{INA} = 0 V, V_{INB} = 0 V$			
current	IVDDB	-	2	5		V INA = 0 V, V INB = 0 V			
VCCI operating current	Ivcci	-	2.5	3	mA	(f = 500 kHz)			
VDDA and VDDB operating	I <sub>VDDA</sub>	_	4	4.5	mA	current per channel,			
current	I <sub>VDDB</sub>			ч.0		Соит = 100 рF			
	VCCI UVLO THRESHOLDS								
Rising threshold	V <sub>VCCI_ON</sub>	2.5	2.8	2.9	V	-			
Falling threshold VCCI_OFF	Vvcci_off	2.35	2.55	2.7	V	-			
Threshold hysteresis	Vvcci_hys	-	0.25	-	V	-			
	VI		O THRE	SHOLD	S				
Rising threshold	Vdda_on	11.3	12.6	13.3	V	VO > 5V			
VDDA_ON, VDDB_ON	VDDB_ON	11.0	12.0	10.0	.5 V	10 2 01			
Falling threshold	Vdda_off	9.8	11.1	11.8	V	7 VO < 5V			
VDDA_OFF, VDDB_OFF	VDDB_OFF	0.0		11.0	, in the second				
Threshold hysteresis	V <sub>DDA_HYS</sub>	-	1.5	_	V	_			
	VDDB_HYS		1.0		v				
INPUT CHANNEL CHARACTERISTICS									
Input high voltage	Vinah,	_	1.3	2	V	-			
	Vinbh, Vdish	- 1.5	2	,					
Input low voltage	$V_{\text{INAL}}, V_{\text{INBL}},$	0.8	1.2	-	V	-			
	V <sub>DISL</sub>								
Input hysteresis	VINA_HYS,	-	0.1	-	V	-			
	VINB_HYS				-				



			SOP1	5, 4A	Outpu	it Dual-Channel Gate	Driver		
ELECTRICAL OPTICAL CHARACTERISTICS									
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	NOTE		
OUTPUT CHARACTERISTICS									
	Iouta+	3			^				
Peak output source current	IOUTB+	3	-	-	A	VDD=30V, C <sub>VDD</sub> =10uF			
Dook output sink ourroat	Iouta-	3			^	VOUT=VDD-15V			
Peak output sink current	IOUTB-	3	-	-	A				
	Devery vi					$I_{OUT} = -10 \text{ mA}, T_A = 25^{\circ}\text{C},$			
Output resistance at high state	Routa_h,		2		Ω	Roha, Rohb do not represent			
	Routb_h					drive pull-up performance			
	R <sub>OUTA_L</sub>		1.6	-	Ω	10 m A T 25%			
Output resistance at low state	R <sub>OUTB_L</sub>	-			11	$I_{OUT} = -10 \text{ mA}, T_A = 25^{\circ}\text{C}$			
Output voltage at high state	Vouta_h	29.8	-	-	V	$V_{VDDA}, V_{VDDB} = 12 V,$			
Output voltage at high state	Voutb_h				v	$I_{OUT} = -10 \text{ mA}, T_A = 25^{\circ}C$			
Output voltage at low state	V <sub>OUTA_L</sub>	_	_	25	mV	$V_{VDDA}, V_{VDDB} = 12 V,$			
Oulput voltage at low state	V <sub>OUTB_L</sub>	- DUTB_L	-	25	mv	$I_{OUT} = 10 \text{ mA}, T_A = 25^{\circ}C$			
	DEADTIME	AND O	VERLAF	PROGI	RAMMIN	IG			
	0	verlap d	etermine	ed					
			by IN	IA INB		Pull DT pin to VCCI			
Dead time					DT pin is left open, min				
Dead time		-	9.5	15	ns	spec characterized only,			
						tested for outliers			
		100	165	300	ns	R <sub>DT</sub> = 20 kΩ			

COD1C

.

Unless otherwise noted,  $V_{VCCI} = 3.3 \text{ V or } 5 \text{ V}$ , 0.1- $\mu$ F capacitor from  $V_{CCI}$  to GND,  $V_{VDDA} = V_{VDDB} = 30 \text{ V}$ , 1- $\mu$ F capacitor from  $V_{DDA}$  and  $V_{DDB}$  to  $V_{SSA}$  and  $V_{SSB}$ ,  $T_A = -40^{\circ}$ C to +125°C.



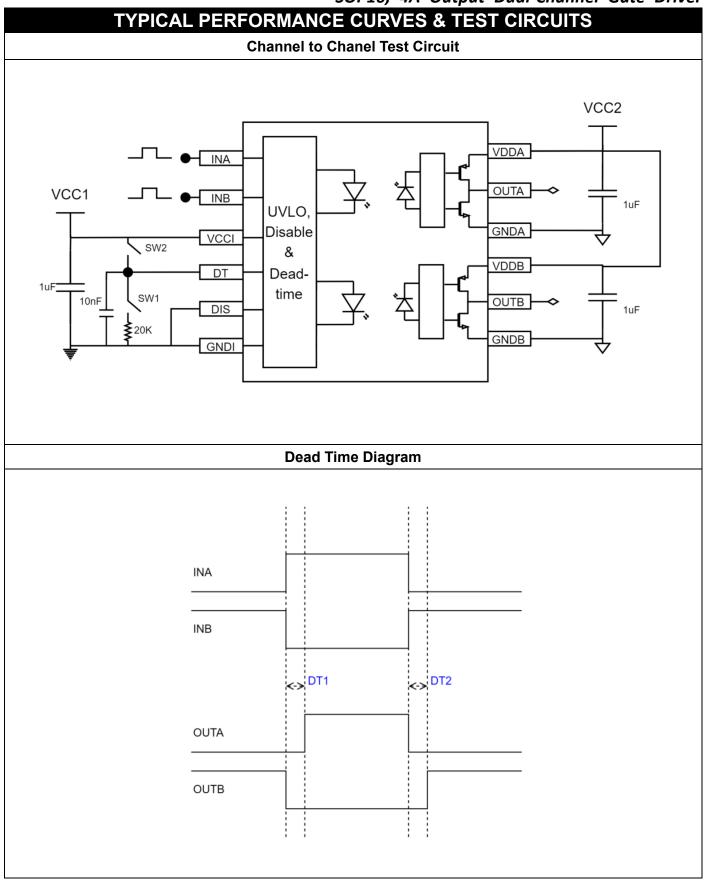
			SOF	P16, 4	4A O	utput Dual-Channel Gate I	Driver
	SWITC	HIN(	g Sp	ECIF	ICAT	ION	
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	NOTE
Output rise time, 20% to 80% measured points	trise	-	4.5	-	ns		
Output fall time, 90% to 10% measured points	t <sub>FALL</sub>	-	3.6	-	ns	C <sub>OUT</sub> = 1.8nF	
Propagation delay from INx to OUTx falling edges	<b>t</b> PDHL	35	60	150	ns	-	
Propagation delay from INx to OUTx rising edges	tpdlh	35	70	150	ns	-	
Pulse width distortion  t <sub>PDLH</sub> – t <sub>PDHL</sub>	t <sub>PWD</sub>	-	10	-	ns	-	
Propagation delays matching between Vouta, Voutв	tом	-	-	8	ns	f = 100 kHz	
$V_{DDA}$ , $V_{DDB}$ Power-up Delay Time: $U_{VLO}$ Rise to OUT <sub>A</sub> , OUT <sub>B</sub> .	$t_{VDD+ to OUT}$	-	10	-	us	$IN_{\text{A}}$ or $IN_{\text{B}}$ tied to $V_{\text{CCI}}$	
Output High Level Common Mode Transient Immunity	CMH	-	75	-	kV/us	INA and INB both are tied to Vcci; Vcm=1500V	
Output Low Level Common Mode Transient Immunity	CML	-	75	-	kV/us	$IN_{\mathbb{A}}$ and $IN_{\mathbb{B}}$ both are tied to GND; $V_{\text{CM}}{=}1500V$	

Unless otherwise noted,  $V_{VCCI} = 3.3 \text{ V or } 5 \text{ V}$ ,  $0.1 - \mu \text{F}$  capacitor from  $V_{CCI}$  to GND,  $V_{VDDA} = V_{VDDB} = 12 \text{ V}$ ,  $1 - \mu \text{F}$  capacitor from  $V_{DDA}$  and  $V_{DDB}$  to  $V_{SSA}$  and  $V_{SSB}$ ,  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

ISOLATION CHARACTERISTIC												
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	NOTE					
Withstand Insulation	Mar	5000	5000							V	RH ≤ 40%-60%,	
Test Voltage	Viso	5000		-	v	t = 1min, T <sub>A</sub> = 25 °C						
Input-Output	D		10 <sup>12</sup>		0							
Resistance	RI-0	-	1012	-	Ω	V <sub>I-O</sub> = 500V DC						



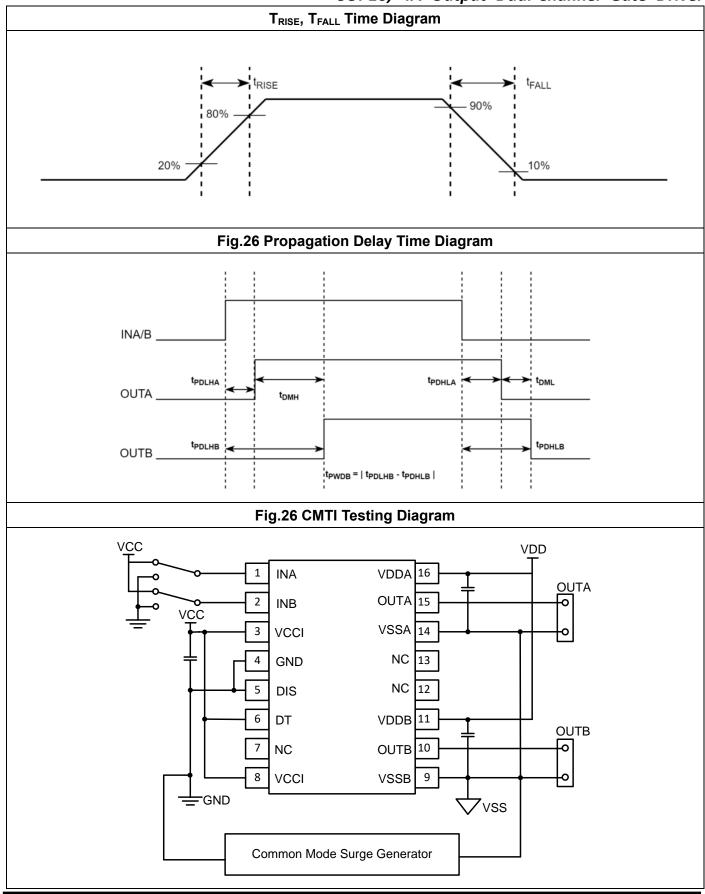
SOP16, 4A Output Dual-Channel Gate Driver



Rev: v.0.1(Preliminary)



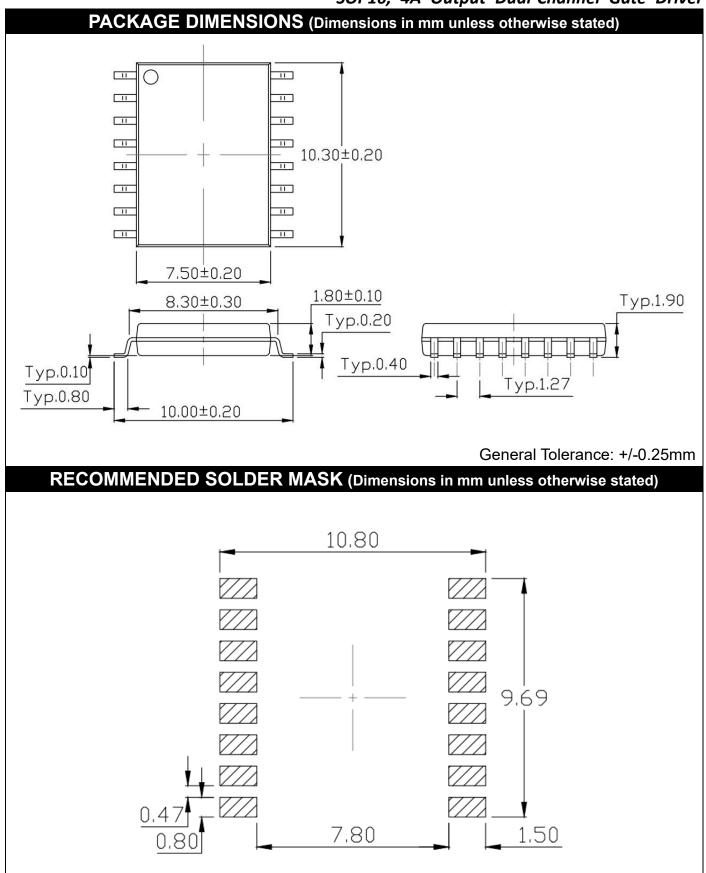
SOP16, 4A Output Dual-Channel Gate Driver



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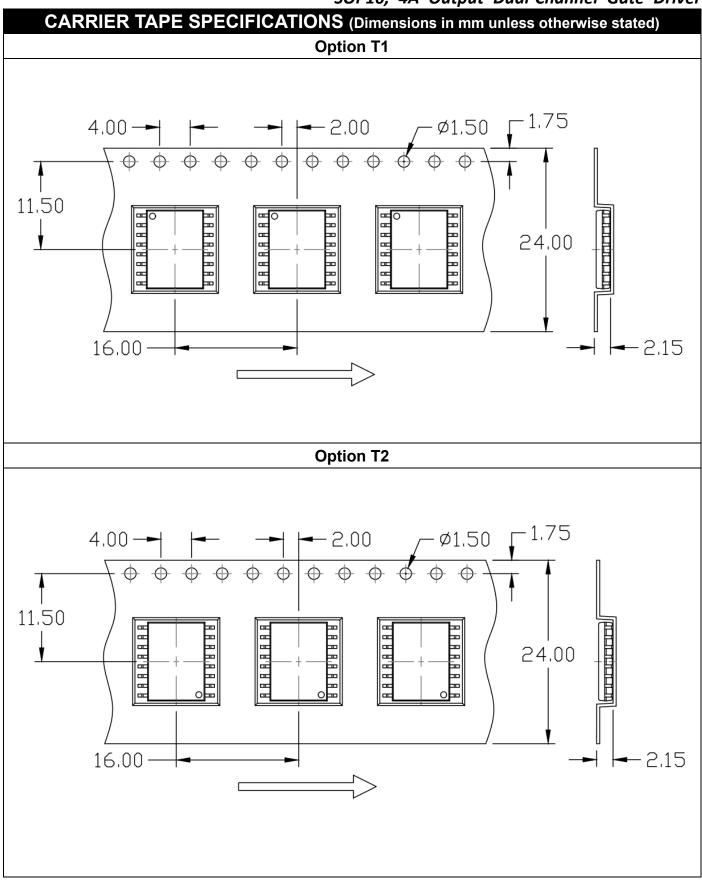
SOP16, 4A Output Dual-Channel Gate Driver



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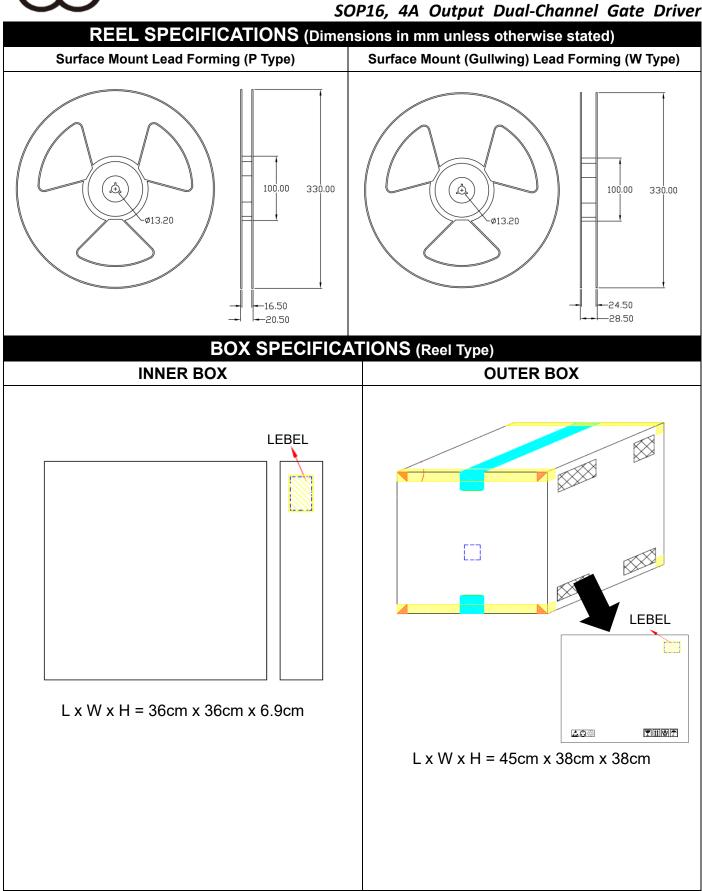


SOP16, 4A Output Dual-Channel Gate Driver



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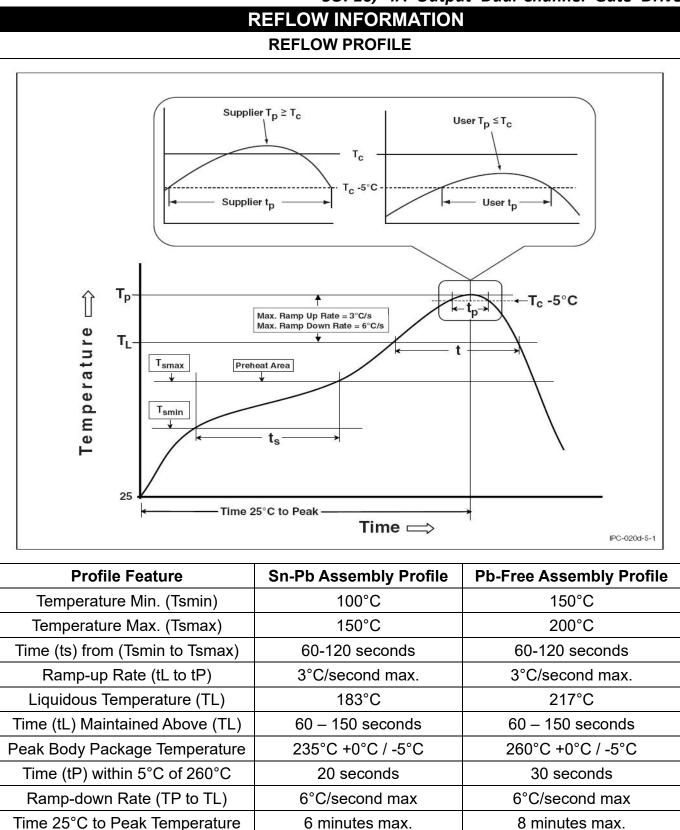
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		SOP10	6, 4A	<b>Output Dual-Channel Gate Driver</b>				
ORDERING AND MARKING INFORMATION								
	Ν	ARKING INFO	RMATI	ON				
	MYYWW 3922 TV			: Company Abbr. : Year date code : 2-digit work week : Part Number I : Factory identification mark : VDE Identification(Option)				
ORD	ERING INFORMAT	ION	LABEL INFORMATION					
М	PCS-3922-Z	<b>V</b>		b 喆光照明光電股份有限公司 WISELITE Optronics Co., Ltd				
S – Stack 3922 – Part N Z – Tape and	MPC – Company Abbr. S – Stack 3922 – Part Number Z – Tape and Reel Option (T1/T2) / –VDE Option (V or None)		Lot I Date Q'ty	No : XXXXXXXXXXX Bin Code : X No : XXXXXXXXXXX e Code : XXXX : XXXX pcs				
		PACKING QUA		(				
Option	Quantity	Quantity – Inner	r box	Quantity – Outer box				
T1/T2	1000 Units/Reel	2 Reels/Inner b	хох	5 Inner box/Outer box = 10k Units				

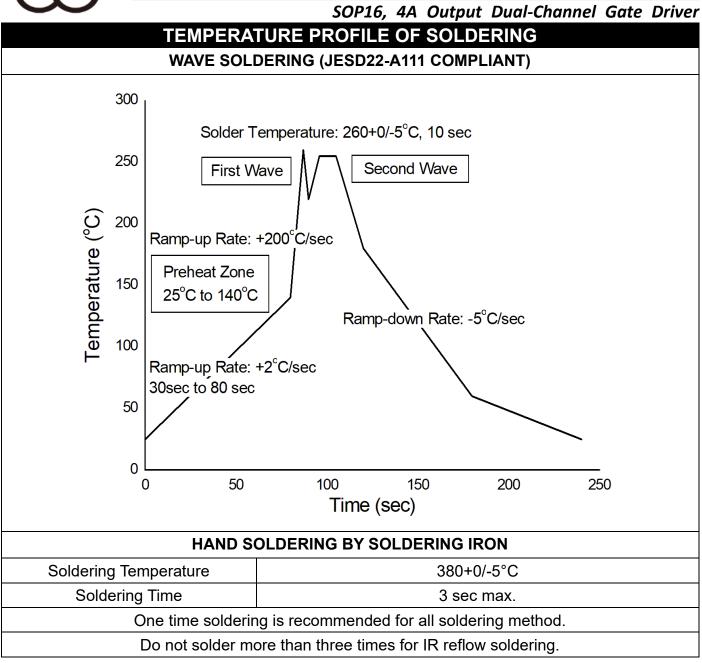






Rev: v.0.1(Preliminary)







#### SOP16, 4A Output Dual-Channel Gate Driver DISCLAIMER

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