MAD2418

Data Sheet

Version: 0.17

Features

Delta Sigma ADC

- **ADC Resolution 24 Bits**
- **24 Bits, No Missing Codes**
- **Up to 22 Bits Noise-Free Resolution**
- **±0.0020% Nonlinearity**
- **Data Output Rates up to 30kSPS**
  - Programmable output rates from 2.5SPS to 30kSPS by register setting
- **Fast Channel Cycling**
- **One-Shot Conversions with Single-Cycle Settling**
- **Flexible Input Multiplexer with Sensor Detect**
  - Four Differential Inputs
  - Eight Single-Ended Inputs
- **Chopper-Stabilized Input Buffer**
- **Low-Noise PGA with programmable gain up to 64**
  - Programmable gain of 1, 2, 4, 8, 16, 32, 64 by register setting
- **Self and System Calibration for All PGA Settings**

Power

- **Support Normal, Standby Mode and Power-down modes**
- **Built-in a power management controller with Power-down and wakeup control**

Clock

- **Built-in embedded crystal oscillator**
- **Support external clock input CLKIN from XTAL1 pin**
- **Support internal clock output CLKOUT to D0 pin**

Communication

- **SP-Compatible Serial Interface**
- **Support ADC command mode for register setting**
- **Support Read Data(RDATA) or Read Data Continuous(RDATAC) command to get ADC data**

Operating

- **Analog Supply range: 4.75V to 5.25V**
- **Digital Supply range: 1.8V to 3.6V**
- **Operating temperature range -40℃ ~ 85℃ (**1)**

Package Types

- **SSOP28**
- **SSOP20**

(**1): Tested by sampling.

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1. General Description

The chip is embedded a precision 24-bit analog-to-digital converter and designed to provide high-resolution measurement solutions for the most applications. The converter is implemented a low-noise input buffer, a low-noise programmable gain amplifier (PGA), a 4th-order delta-sigma (ΔΣ) modulator and a digital filter. It's designed to easy use for industrial process control, measurement instrumentation, weigh scales and other applications. The chip is packaged in an SSOP-28.

A flexible input multiplexer handles differential or single-end signals input with sensor detect. It can support maximum four differential inputs or eight single-ended inputs. The selectable input buffer can enable to increases the input impedance. The low-noise programmable gain amplifier (PGA) provides gains from 1 to 64 in binary steps. The digital filter can optimize a resolution of up to 24 bits and a data rate of up to 30K samples per second (SPS).

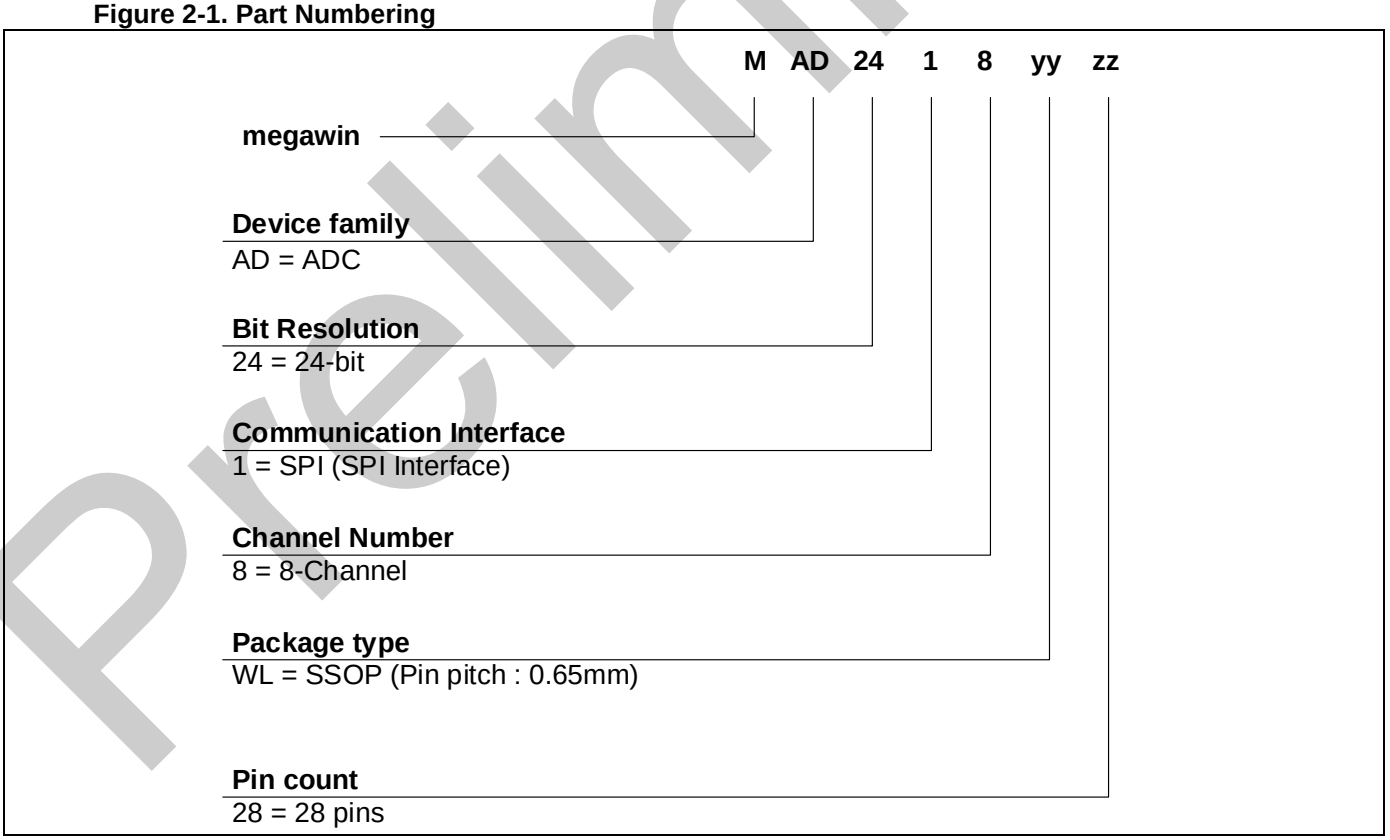
The chip is built-in embedded Power-On Reset (POR) circuit to generate internal hardware reset signal or input external active low reset signal from the RESET pin to reset the chip. For power management and reset control, the chip is built-in a power supervisor for power down control and wakeup control. Also the chip is supported to control chip power down or wakeup by external signal from the PDWN pin. The chip is embedded an on-chip oscillator circuit for 7.68MHz crystal. Four bidirectional digital I/O pins with a programmable clock output driver are provided for general use.

The converters offer fast channel cycling for measuring multiplexed inputs and can also perform one-shot conversions that settle in just a single cycle. The communication is handled by an SPI-compatible serial interface to get ADC code and control the ADC settings from external MCU device. Onboard calibration supports both self and system correction of offset and gain errors for all the PGA settings.

2. Order Information

Please contact the megawin sales for available options (package, …) and more information about this device.

Figure 2-1. Part Numbering



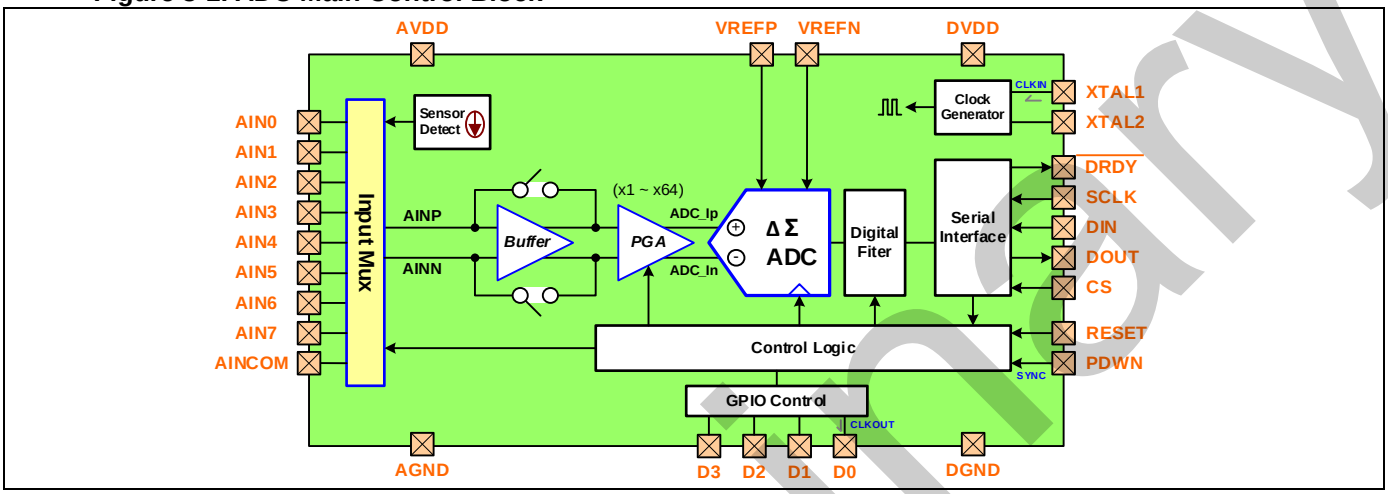
- **Part Number List**
  - **MAD2418WL28 : SSOP-28 (209 mil)**

3. Block Diagram

3.1. ADC Main Block

The following figure is showing the ADC control block diagram. It is embedded a precision 24-bit analog-to-digital converter with a 4th-order delta-sigma (ΔΣ) modulator and a digital filter, analog input multiplexer with sensor detect, a low-noise input buffer, a low-noise programmable gain amplifier (PGA) and a serial interface control block.

Figure 3-1. ADC Main Control Block

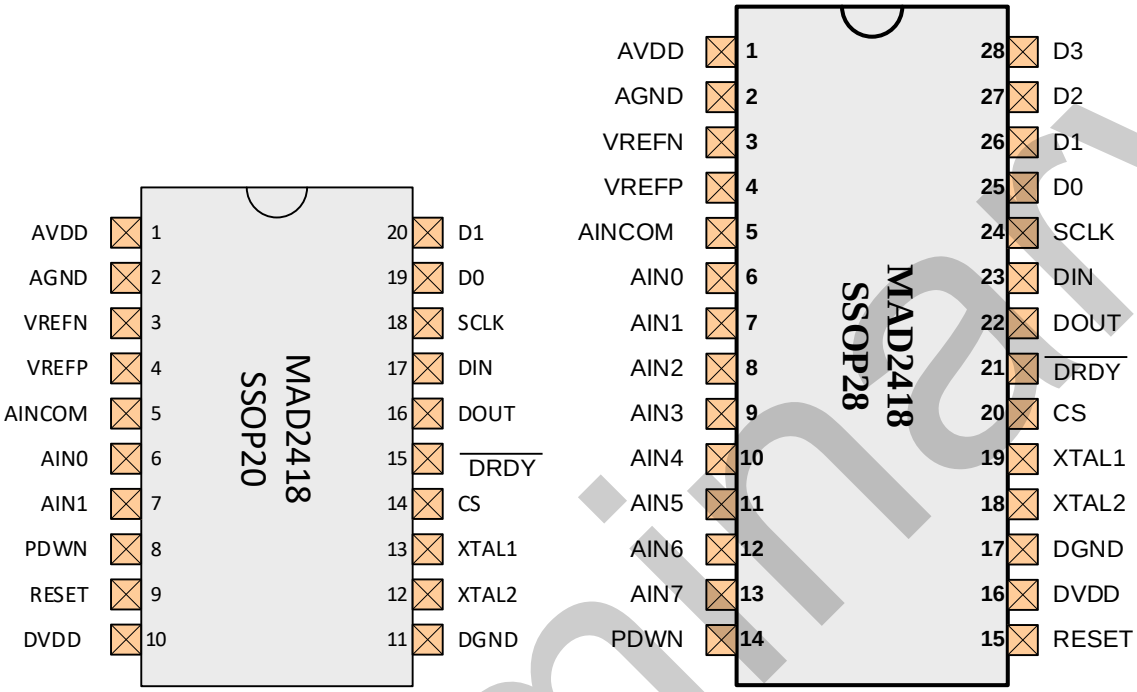


4. Pin Description

4.1. Pin Outline

4.1.1. SSOP20 & SSOP28 Package Pinout

Figure 4-1. SSOP20 & SSOP28 Package Pinout



4.2. Pin Definition

Table 4-1. Abbreviations for pin definition

IO Type		IO Structure	
P	Power/Ground pin	I	Digital Input
B	Bidirectional	P	Output Push-pull capability
I	Input	A	Analog I/O (Digital I/O disable)
O	Output	F	5V tolerant
A	Analog I/O	S	Schmitt trigger

Table 4-2. Pin Descriptions

Pin Name	Pin Number SSOP28	IO Type	Default Type	Default Value	IO Structure	Alternate Functions	Description
AVDD	1	P					ADC analog power supply
AGND	2	P					ADC analog ground
VREFN	3	A			A		ADC negative reference input
VREFP	4	A			A		ADC positive reference input
AINCOM	5	A			A		ADC analog input common
AIN0	6	A			A		ADC analog input 0
AIN1	7	A			A		ADC analog input 1
AIN2	8	A			A		ADC analog input 2
AIN3	9	A			A		ADC analog input 3
AIN4	10	A			A		ADC analog input 4
AIN5	11	A			A		ADC analog input 5
AIN6	12	A			A		ADC analog input 6
AIN7	13	A			A		ADC analog input 7
PDWN	14	I			I,F,S	PDWN	Power down input (active low)
						SYNC	Synchronization input
RESET	15	I			I,F,S		Chip reset input (active low)
DVDD	16	P					ADC digital power supply
DGND	17	P					ADC digital ground
XTAL2	18	A			A		Crystal oscillator output
XTAL1	19	A			A,F	XTAL1	Crystal oscillator input
						CLKIN	External clock input
CS	20	I			I,F,S		Chip select (active low)
$\overline{\text{DRDY}}$	21	O			P		Data ready output (active low)
DOUT	22	O			P		Serial data output
DIN	23	I			I,F,S		Serial data input
SCLK	24	I			I,F,S		Serial clock input
D0	25	B	O		I,P,S	D0	Digital I/O 0
						CLKOUT	Internal clock output
D1	26	B	I		I,P,S		Digital I/O 1
D2	27	B	I		I,P,S		Digital I/O 2
D3	28	B	I		I,P,S		Digital I/O 3

5. Functional Description

5.1. Serial Interface

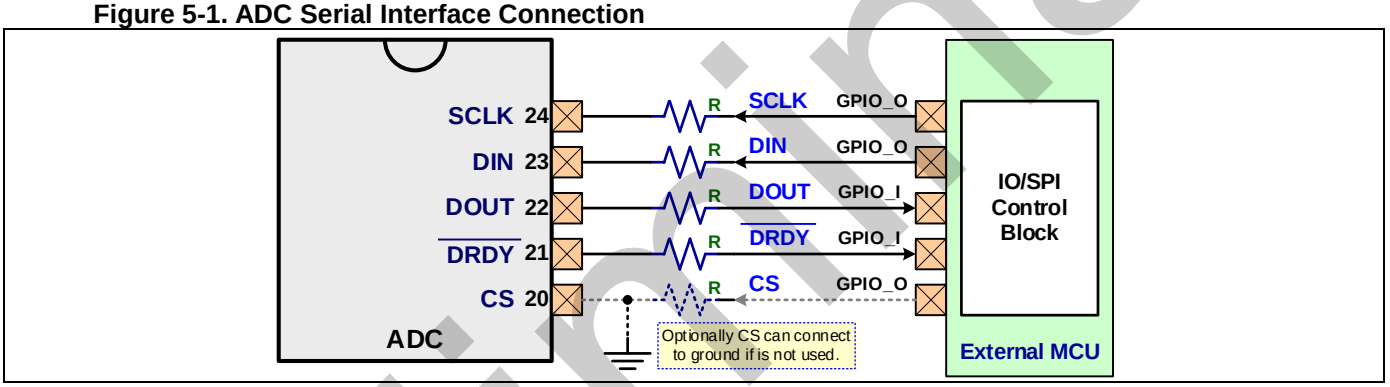
The ADC communication is handled by a SPI compatible serial interface to get ADC code and control the ADC settings from external MCU device. There are total five pins of **SCLK**, **DIN**, **DOUT**, **CS** and $\overline{\text{DRDY}}$ those are used for the communication. These pins are used for the controls of data retrieval, input selection, output data rate selection, PGA gain selection, power down, etc.

The **SCLK**, **DIN**, **DOUT** and **CS** pins are using as SPI compatible serial interface. When the ADC communication is a simple one MCU (master) with one ADC (slave) on user application, the **CS** pin can be not used optionally. It can directly connect to digital ground. The $\overline{\text{DRDY}}$ pin is an output signal to indicate the ADC data is ready. ADC output the signal to notify MCU ADC has converted one ADC sample and MCU can get the ADC code.

The ADC serial 24-bit data output is generated from **DOUT** pin when each time the ADC is converted completely and the first data bit is most significant bit. For actual application request, user can set the output first data bit is most significant bit or least significant bit by setting **SADC_ORDER** register through ADC command mode. Default the first data bit is most significant bit.

The following figure is showing the ADC serial interface connection diagram.

Figure 5-1. ADC Serial Interface Connection



5.2. Power and Reset

5.2.1. Chip Power

The chip power is implemented by separated analog power supply **AVDD** and digital power supply **DVDD**. The chip supports one power controller to manage power-on reset (POR) circuit, power down control and wakeup control.

The **AVDD** power can be connect to the same power voltage source of external sensor, like as load-cell. The **DVDD** power can be connect to the same power voltage source of external MCU device.

5.2.2. Chip Reset

The chip support multiple reset source those include power-on reset, SCLK Reset pattern, **RESET** pin trigger and software reset command. During chip reset, all internal registers are set to their initial values. The chip is embedded a Power-On Reset (POR) circuits which is always active. The POR circuit will generate the reset signal to reset the chip during chip power up period.

For SCLK Reset pattern, MCU firmware can send the reset timing as following figure through **SCLK** pin input. For software reset command, MCU firmware can trigger the reset event by **RESET** command through ADC command mode. For **RESET** pin trigger, MCU firmware can send an active low pulse as following figure through **RESET** pin input .

The following figures are showing the ADC SCLK Reset timing and RESET and SYNC/PDWN timing diagrams. Refer the table of "AC Timing Characteristics" about the AC timing parameters.

Figure 5-2. ADC SCLK Reset Timing

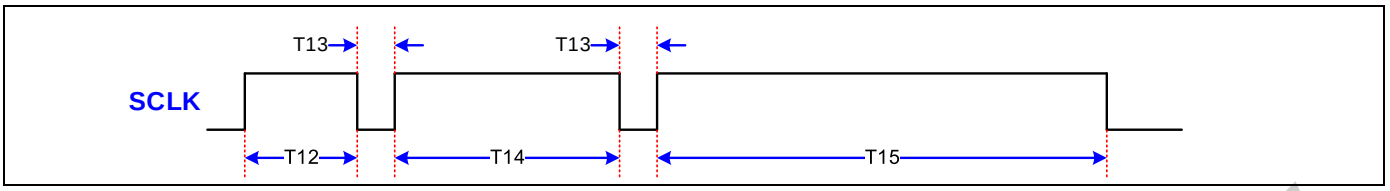
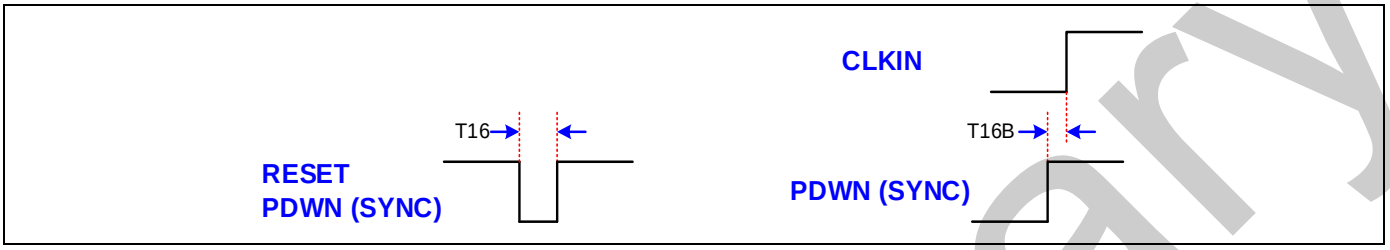


Figure 5-3. ADC RESET and SYNC/PDWN Timing



5.2.3. Power-Down and Wakeup Timing

The chip is supported the ***Standby*** mode and ***Power Down*** mode to save current consumption. For power management and reset control, the chip is built-in a power supervisor for power down control and wakeup control. User can set ADC to enter ***Standby*** mode by **STANDBY** command through ADC command mode. User can set ADC to enter ***Power Down*** mode by **PDWN** pin trigger.

When chip is entering ***Standby*** mode and ***Power Down*** mode, the ADC can wake up by **WAKE** command through ADC command mode.

5.3. Clock

5.3.1. Chip Clock

The master clock source can be provided using external clock source, an external crystal or internal embedded RC oscillator. When using an external clock source, supply the clock signal to **XTAL1** (CLKIN) pin and leave **XTAL2** pin floating. It is important that the external clock source must supplied a clean clock signal. When using a crystal, the chip is support **XTAL1** and **XTAL2** pins to connect external crystal. If other devices need a clock source, the **D0** pin is available to do as internal RC oscillator clock output (CLKOUT).

This clock is used to support ADC with a maximum conversion rate of 30000 SPS. User can set the ADC conversion rate by setting **SADC_DR** register.

5.4. ADC

5.4.1. Delta-Sigma ADC

The chip is embedded a precision 24-bit analog-to-digital converter and designed to provide high-resolution measurement solutions for the most applications. The converter is implemented a low-noise input buffer, a low-noise programmable gain amplifier (PGA), a 4th-order delta-sigma (ΔΣ) modulator and a digital filter. It's designed to easy use for weight scales and other applications by connecting directly with the external bridge sensor.

A flexible input multiplexer handles differential signals input. The selectable input buffer can enable to increases the input impedance. User can enable the low-noise input buffer for weak ADC input voltage by setting **SADC_BUFEN** register through ADC command mode. The PGA provides gains from 1 to 64. Also user can set the PGA gain ratio by setting **SADC_ PGA** register through ADC command mode. The digital filter can optimize a resolution of up to 24 bits and a data rate of up to 30000 samples per second (SPS).

5.4.2. Analog Mux

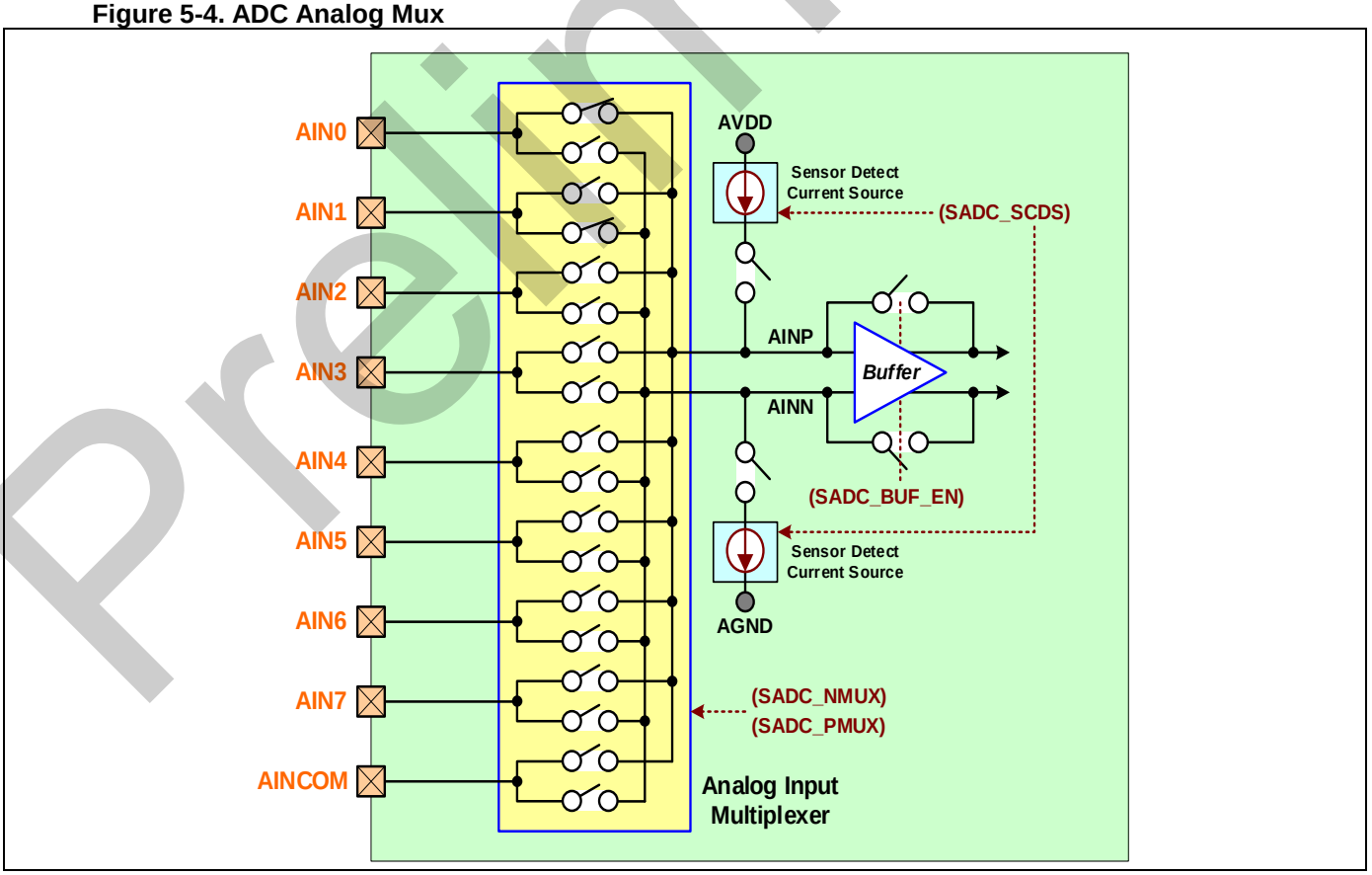
The chip is built-in the analog input multiplexers to support nine analog inputs with open and short sensor detection. These analog inputs can support four external differential inputs or eight external single-ended inputs.

The analog multiplexer selects the inputs to the ADC to be measured in differential mode or single-ended mode. When user configures to differential mode, the ADC inputs are coming from each two pins of **AIN0** to **AIN7** those are able to do as a couple of differential input pair. For the differential mode, the **AINCOM** pin is not used. When ADC inputs as analog single-end voltage input on application, each one pin of **AIN0** to **AIN7** and **AINCOM** pins are able to do analog input with single-end mode. For the single-end mode, the **AINCOM** pin is used the common input. Usually, It is can be tied to ground for most application.

User can set separated the ADC AINN and AINP inputs from **AIN0** to **AIN7** and **AINCOM** pins by setting **SADC_NSEL** and **SADC_PSEL** registers.

The following figure is showing the ADC analog multiplexer block diagram.

Figure 5-4. ADC Analog Mux



5.4.3. Sensor Detection

The sensor detect current sources (SDCS) provide a means to verify the integrity of the external sensor connected to the ADC. When enabled, the SDCS supply a current (I_{SDC}) of approximately 0.5uA, 2uA, or 10uA to the sensor through the input multiplexer. The SDCS bits in the ADCON register enable the SDCS and set the value of I_{SDC}.

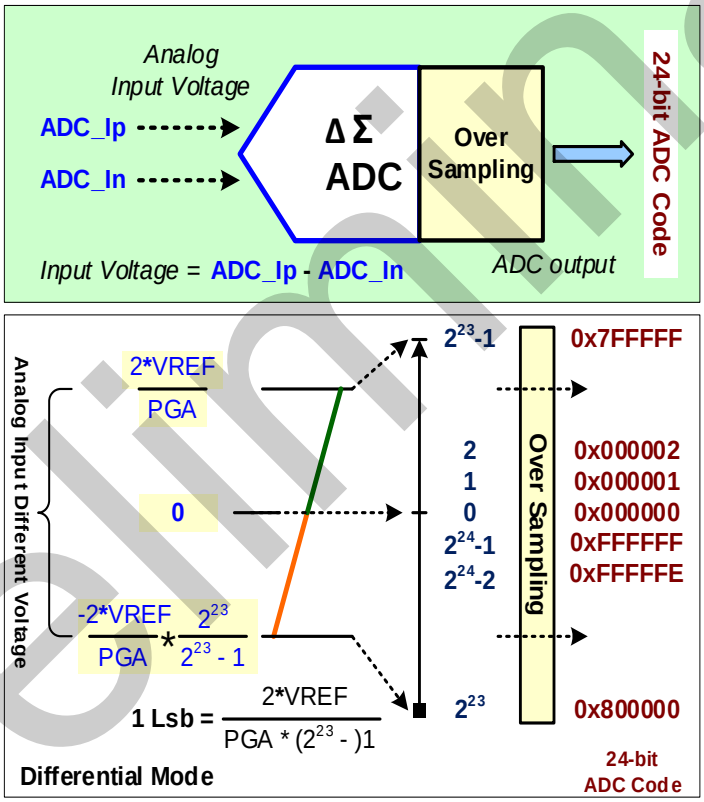
When the SDCS are enabled, the ADC automatically turns on the analog input buffer regardless of the BUFEN bit setting. This is done to prevent the input circuitry from loading the SDCS. When the SDCS are enabled, they source I_{SDC} to the input pin connected to AIN_P and sink I_{SDC} from the input pin connected to AIN_N.

5.4.4. ADC Input Voltage Range

The ADC analog differential input voltage is the delta voltage of input (**AINP** - **AINN**). The ADC output code is 24 bits in binary 2s' complement format. When the input delta voltage is 0 volt, it gets an ADC output code of 0x000000. A positive full-scale input voltage gets an ADC output code of 0x7FFFFF and the negative full-scale input voltage gets an ADC output code of 0x800000.

The following figure is showing the ADC analog differential input voltage range diagram.

Figure 5-5. ADC Input Voltage Range



The following formulas are listed the ADC full scale range (FSR) and analog input voltage range.

Full Scale Range

$$FSR = \frac{VREF * K}{PGA}$$

Input Range

$$\frac{0.5*K*VREF}{PGA} \sim \frac{-0.5*K*VREF}{PGA} * \frac{2^{23}}{2^{23}-1}$$

VREF: ADC reference voltage from **VREF** pin

PGA: PGA gain ratio

K: =4

5.4.5. ADC Output Code

The ADC can convert the analog differential input voltage from **AINP** and **AINN** inputs and output ADC 24-bit binary code to **DOUT** pin. User can calculate ADC conversion output code by following formulas.

ADC Output Code

$$BCD = \frac{VIN * PGA * (2^{23}-1)}{VREF * 0.5 * K}$$

VIN: analog input differential (**AIN1** - **AIN0**) voltage
VREF: ADC reference voltage from **VREF** pin
PGA: PGA gain ratio
K: =4

5.4.6. ADC ENOB and Noise Free Bits

The following formulas are used to calculate the ADC Effective-Number-of-Bits (ENOB) and Noise-Free Bits (NFB).

ENOB

$$ENOB = \frac{\ln(FSR / RMS\ Noise)}{\ln(2)}$$

Noise Free Bits

$$Bits = \frac{\ln(FSR / P\text{-}P\ Noise)}{\ln(2)}$$

FSR: ADC full scale range
P-P Noise: Peak-to-Peak noise

The RMS noise and Peak-to-Peak noise can be calculated in following formulas.

Noise (Voltage)

$$RMS\ Noise = \frac{P\text{-}P\ Noise}{6.6}$$

P-P (Peak-to-Peak) Noise $= (V_{Max} - V_{Min}) / PGA$

Table 5-1. ENOB, Free Noise Resolution table

Data Rate (SPS)	Effective Number of Bits (ENOB, rms), Buffer OFF						
	MAD2418						
	PGA						
	1	2	4	8	16	32	64
2.5	23.14	23.14	23.14	22.72	22.55	21.77	20.92
5	22.47	22.64	22.55	22.33	21.82	20.68	20.26
10	21.82	22.08	22.14	21.92	21.68	20.66	20.17
15	21.72	21.86	21.82	21.55	21.72	21.14	20.08
25	21.33	21.47	21.47	21.20	21.14	19.97	19.84
30	21.23	21.17	21.23	21.20	21.14	20.28	20.09
50	20.89	20.59	20.77	20.77	20.77	20.64	19.76
60	20.68	20.68	20.44	20.84	20.55	20.28	19.77
100	20.26	20.44	20.35	20.18	20.30	19.66	19.31
500	19.38	19.13	19.10	19.20	19.31	18.77	18.36
1000	18.61	18.53	18.58	18.52	18.68	18.71	17.57
2000	18.10	18.12	18.09	18.10	18.10	18.01	17.34
3750	17.47	17.77	17.69	17.82	17.57	16.88	16.61
7500	17.38	17.37	17.47	17.43	17.22	17.42	16.67
15000	17.08	17.18	17.13	17.20	16.86	17.03	16.08
30000	16.91	17.08	17.05	17.04	16.80	16.80	16.14

AVDD=5.0V, DVDD=1.8V, VREF=2.5V

Data Rate (SPS)	Free Nois Resolution (bits), Buffer OFF						
	MAD2418						
	PGA						
	1	2	4	8	16	32	64
2.5	20.42	20.42	20.42	20.00	19.83	19.05	18.19
5	19.75	19.91	19.83	19.61	19.09	17.96	17.54
10	19.09	19.36	19.42	19.19	18.96	17.93	17.45
15	19.00	19.14	19.09	18.83	19.00	18.42	17.36
25	18.61	18.75	18.75	18.48	18.42	17.25	17.12
30	18.51	18.45	18.51	18.48	18.42	17.56	17.37
50	18.17	17.87	18.05	18.05	18.05	17.91	17.03
60	17.96	17.96	17.71	18.12	17.83	17.56	17.05
100	17.54	17.71	17.62	17.46	17.57	16.93	16.59
500	16.66	16.41	16.38	16.48	16.59	16.05	15.64
1000	15.89	15.81	15.86	15.80	15.96	15.98	14.85
2000	15.37	15.39	15.37	15.37	15.38	15.29	14.61
3750	14.74	15.05	14.97	15.10	14.85	14.16	13.89
7500	14.66	14.65	14.75	14.47	12.86	11.24	10.50
15000	14.03	14.46	14.40	13.53	11.71	9.86	9.28
30000	14.19	14.36	14.32	14.27	12.35	10.48	11.52

AVDD=5.0V, DVDD=1.8V, VREF=2.5V

Data Rate (SPS)	Effective Number of Bits (ENOB, rms), Buffer ON						
	MAD2418						
	PGA						
	1	2	4	8	16	32	64
2.5	23.40	23.40	23.14	22.82	22.64	21.77	20.84
5	22.92	22.72	22.82	22.55	22.47	21.59	20.68
10	22.08	22.33	22.14	22.33	21.82	21.64	20.53
15	22.02	21.82	21.86	21.92	21.77	21.47	20.57
25	21.44	21.64	21.59	21.44	21.55	21.05	20.20
30	21.44	21.44	21.47	21.44	21.33	20.97	20.23
50	20.84	21.08	21.11	21.11	20.84	20.84	20.15
60	20.94	20.86	20.97	20.79	20.72	20.79	19.75
100	20.59	20.51	20.40	20.68	20.17	19.85	19.25
500	19.31	19.31	19.38	19.39	19.29	19.11	18.24
1000	18.80	18.81	18.98	19.02	18.86	18.72	17.94
2000	18.22	18.44	18.29	18.44	18.34	18.11	17.44
3750	17.50	17.86	17.93	17.79	17.92	17.53	16.67
7500	17.50	17.52	17.53	17.48	17.60	17.27	16.53
15000	17.22	17.29	17.40	17.36	17.26	16.89	16.15
30000	17.22	17.20	17.07	17.13	16.82	16.68	16.05

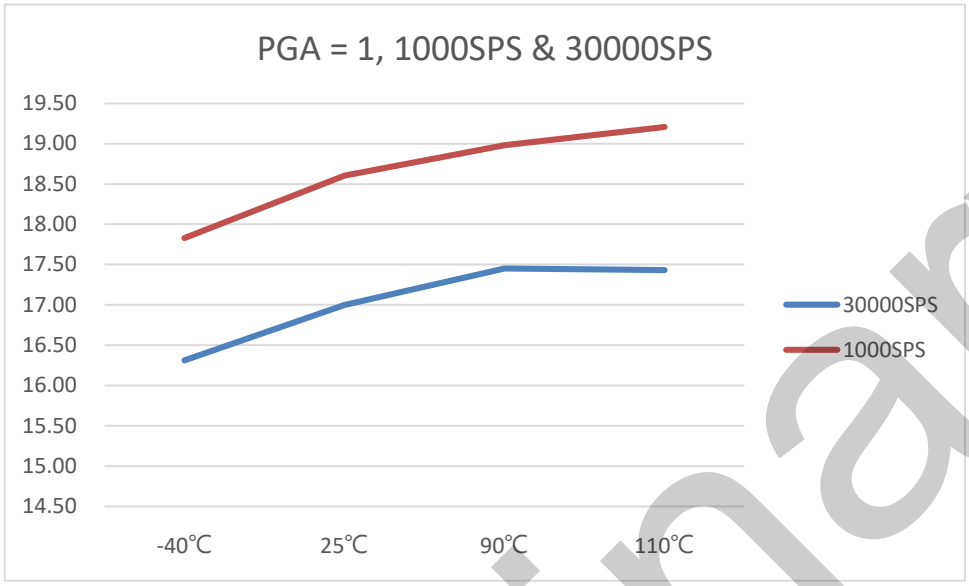
AVDD=5.0V, DVDD=1.8V, VREF=2.5V

Data Rate (SPS)	Free Nois Resolution (bits), Buffer ON						
	MAD2418						
	PGA						
	1	2	4	8	16	32	64
2.5	20.68	20.68	20.42	20.09	19.91	19.05	18.12
5	20.19	20.00	20.09	19.83	19.75	18.87	17.96
10	19.36	19.61	19.42	19.61	19.09	18.91	17.81
15	19.30	19.09	19.14	19.19	19.05	18.75	17.85
25	18.71	18.91	18.87	18.71	18.83	18.33	17.48
30	18.71	18.71	18.75	18.71	18.61	18.25	17.51
50	18.12	18.36	18.39	18.39	18.12	18.12	17.43
60	18.22	18.14	18.25	18.07	18.00	18.07	17.02
100	17.87	17.79	17.68	17.96	17.45	17.13	16.53
500	16.59	16.59	16.66	16.67	16.57	16.39	15.52
1000	16.08	16.09	16.26	16.30	16.14	16.00	15.22
2000	15.50	15.71	15.57	15.71	15.62	15.39	14.71
3750	14.78	15.14	15.21	15.07	15.20	14.81	13.95
7500	14.78	14.80	14.81	14.76	14.88	14.55	13.81
15000	14.50	14.57	14.67	14.64	14.53	14.16	13.43
30000	14.49	14.48	14.34	14.41	14.10	13.96	13.32

AVDD=5.0V, DVDD=1.8V, VREF=2.5V

Figure 5-6. EFFECTIVE NUMBER OF BITS vs TEMPERATURE

AVDD = 5V, DVDD = 1.8V, Vref = 2.5V, Input buffer off(Line Graph Based on Sample Test Results)



5.4.7. Voltage Reference Inputs

The voltage reference for the ADC is the differential voltage between **VREFP** and **VREFN**. **VREF** voltage is the different voltage and equals VREFP −VREFN.

During self gain calibration, all the switches in the input multiplexer are opened, **VREFN** is internally connected to **AINN**, and **VREFP** is connected to **AINP**. The input buffer may be disabled or enabled during calibration.

A high-quality reference voltage capable of driving the switched capacitor load presented by the ADC is essential for achieving the best performance. Noise and drift on the reference degrade overall system performance. It is especially critical that special care be given to the circuitry generating the reference voltages and their layout when operating in the low data rates setting to get low-noise performance and prevent the voltage reference from limiting performance.

5.5. Calibration

Offset and gain errors can be minimized using the ADC onboard calibration circuitry. Offset errors are corrected with the Offset Calibration (**SADC_OFC**) register and full-scale errors are corrected with the Full-Scale Calibration (**SADC_FSC**) register. Each of these registers is 24-bits and can be read from or written to. **SADC_OFC** is a Binary Two's Complement number that can range from −8,388,608 to 8,388,607, while **SADC_FSC** is unipolar ranging from 0 to 16,777,215.

The ADC supports both self-calibration and system calibration for any PGA setting using a set of five commands: **SELFOCAL**, **SELFGCAL**, **SELFCAL**, **SYSOCAL**, and **SYSGCAL**. Calibration can be done at any time, though in many applications the ADC drift performance is low enough that a single calibration is all that is needed. $\overline{\text{DRDY}}$ goes high when calibration begins and remains so until settled data is ready afterwards.

There is no need to discard data after a calibration. It is strongly recommended to issue a self-calibration command after power-up when the reference has stabilized. After a reset, the ADC performs self-calibration. Calibration must be performed whenever the data rate changes and should be performed when the buffer configuration or PGA changes.

5.5.1. Self-Calibration

Self-calibration corrects internal offset and gain errors. During self-calibration, the appropriate calibration signals are applied internally to the analog inputs.

SELFOCAL performs a self-offset calibration. The analog inputs AIN_P and AIN_N are disconnected from the signal source and connected to AVDD/2. Self-offset calibration updates the **SADC_OFC** register.

SELFGCAL performs a self-gain calibration. The analog inputs **AINP** and **AINN** are disconnected from the signal source and AINP is connected internally to VREFP while AINN is connected to VREFN. Self-gain calibration can be used with any PGA setting. Using the buffer will limit the common-mode range of the reference inputs during self - gain calibration since they will be connected to the buffer inputs and must be within the specified analog input range. When the voltage on **VREFP** or **VREFN** exceeds the buffer analog input range (AVDD – 2.0V), the buffer must be turned off during self-gain calibration. Otherwise, use system gain calibration or write the gain coefficients directly to the **SADC_FSC** register.

SELFCAL performs first a self-offset and then a self-gain calibration. The analog inputs are disconnected from the from the signal source during self-calibration. When using the input buffer with self-calibration, make sure to observe the common-mode range of the reference inputs as described above. Self-calibration updates both the **SADC_OFC** and **SADC_FSC** registers.

5.5.2. System Calibration

System calibration corrects both internal and external offset and gain errors using the **SYSOCAL** and **SYSGCAL** commands. During system calibration, the appropriate calibration signals must be applied by the user to the inputs.

SYSOCAL performs a system offset calibration. The user must supply a zero input differential signal. The ADC then computes a value that will nullify the offset in the system. System offset calibration updates the **SADC_OFC** register.

SYSGCAL performs a system gain calibration. The user must supply a full-scale input signal to the ADC. The ADC then computes a value to nullify the gain error in the system. System gain calibration can correct inputs that are 80% of the full-scale input voltage and larger. Make sure not to exceed the full-scale input voltage when using system gain calibration. System gain calibration updates the **SADC_FSC** register.

5.5.3. Auto-Calibration

Auto-calibration can be enabled by setting the **SADC_ACAL** register to have the ADC automatically initiate a self-calibration at the completion of a write command (**WREG**) that changes the data rate, PGA setting, or Buffer status.

5.6. ADC Conversion

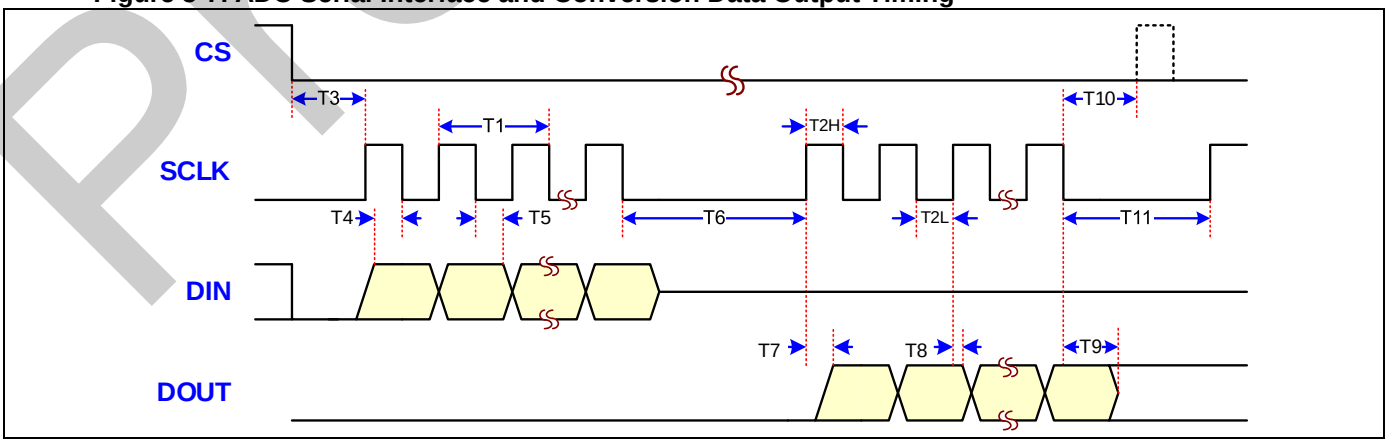
5.6.1. ADC Conversion Timing

The chip is automatically to convert the ADC analog input voltage from **AINP** and **AINN** inputs. After the ADC conversion is complete, the ADC will output the serial bits of ADC code to **DOUT** pin when the ADC data shift clock is receiving from **SCLK** pin.

The ADC serial 24-bit data output is generated from on **DOUT** pin when each time the ADC is converted completely. For actual application request, user can set the output first data bit is most significant bit or least significant bit by setting **SADC_ORDER** register.

The following figure is showing the ADC conversion data output timing diagram. Refer the table of "AC Timing Characteristics" about the AC timing parameters.

Figure 5-7. ADC Serial Interface and Conversion Data Output Timing

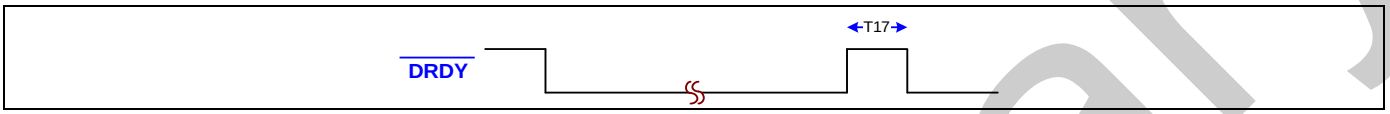


5.6.2. ADC $\overline{\text{DRDY}}$ Update Timing

The **$\overline{\text{DRDY}}$** signal is used to indicate ADC conversion data is ready and the ADC output code is available receiving on **DOUT** pin by shift clock from **SCLK** pin. When the **$\overline{\text{DRDY}}$** output goes high and remains high, it indicates the ADC is still during the conversion. After the ADC conversion is finished, $\overline{\text{DRDY}}$ goes low, indicating that data is available.

The following figure is showing the ADC $\overline{\text{DRDY}}$ update timing diagram. Refer the table of "AC Timing Characteristics" about the AC timing parameters.

Figure 5-8. ADC $\overline{\text{DRDY}}$ Update Timing



5.7. ADC Command Mode

The chip supports ADC command mode for register access. All of the commands are stand-alone except for the register reads and writes (RREG, WREG) which require a second command byte plus data. Additional command and data bytes may be shifted in without delay after the first command byte. The **SADC_ORDER** bit sets the order of the bits within the output data. CS must stay low during the entire command sequence.

The following table is the command definitions of ADC command mode.

Table 5-2. Command Definitions

COMMAND	DESCRIPTION	1ST COMMAND BYTE	2ND COMMAND BYTE
WAKEUP	Completes SYNC and Exits Standby Mode	0000 0000 (00h)	
RDATA	Read Data	0000 0001 (01h)	
RDATAC	Read Data Continuously	0000 0011 (03h)	
SDATAC	Stop Read Data Continuously	0000 1111 (0Fh)	
RREG	Read from REG rrr	0001 rrrr (1xh)	0000 nnnn
WREG	Write to REG rrr	0101 rrrr (5xh)	0000 nnnn
SELFCAL	Offset and Gain Self-Calibration	1111 0000 (F0h)	
SELFOCAL	Offset Self-Calibration	1111 0001 (F1h)	
SELFGCAL	Gain Self-Calibration	1111 0010 (F2h)	
SYSOCAL	System Offset Calibration	1111 0011 (F3h)	
SYSGCAL	System Gain Calibration	1111 0100 (F4h)	
SYNC	Synchronize the A/D Conversion	1111 1100 (FCh)	
STANDBY	Begin Standby Mode	1111 1101 (FDh)	
RESET	Reset to Power-Up Values	1111 1110 (FEh)	
WAKEUP	Completes SYNC and Exits Standby Mode	1111 1111 (FFh)	

<Note> n = number of registers to be read/written − 1.
r = starting register address for read/write commands.

5.7.1. ADC Command Mode Timing

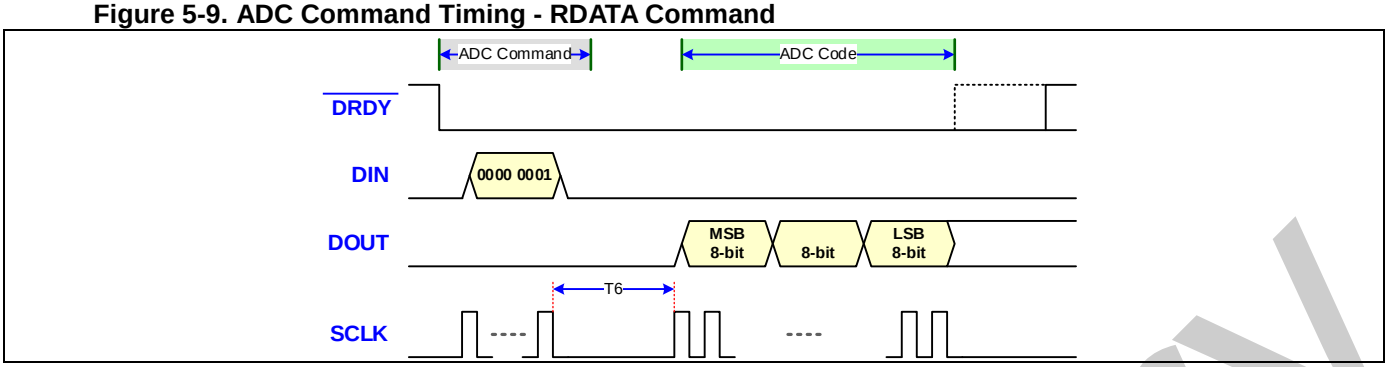
The chip supports simple ADC conversion mode by setting **SCLK** clock number which is maximum 32 clocks. When the clock number is over 32, the chip will escape the simple ADC conversion mode. When the chip detects the clock number 35th, the chip is entering ADC command mode.

At first, the period of clock number 38th to 41th is used to set the register address. The clock number 42th is used to set read or write for register access. Following, the period of clock number 44th to 51th is used as access 8-bit register data.

- **RDATA: Read Data**

Issue this command after $\overline{\text{DRDY}}$ goes low to read a single conversion result. After all 24 bits have been shifted out on DOUT, $\overline{\text{DRDY}}$ goes high. It is not necessary to read back all 24 bits, but $\overline{\text{DRDY}}$ will then not return high until new data is being updated. See the Timing Characteristics for the required delay between the end of the RDATA command and the beginning of shifting data on DOUT: T6.

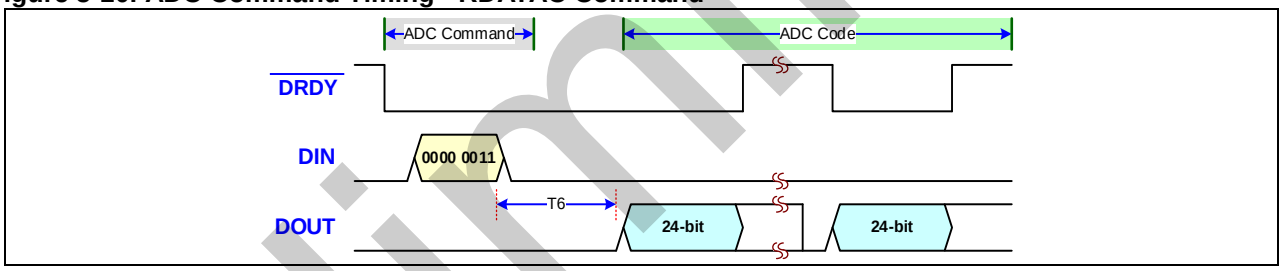
Figure 5-9. ADC Command Timing - RDATA Command



- **RDATAC: Read Data Continuous**

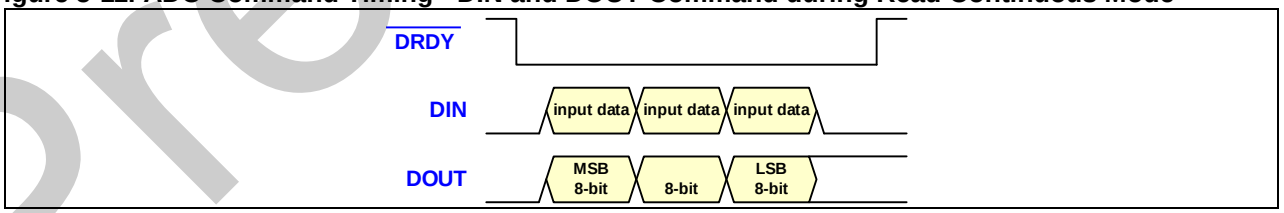
Issue command after $\overline{\text{DRDY}}$ goes low to enter the Read Data Continuous mode. This mode enables the continuous output of new data on each $\overline{\text{DRDY}}$ without the need to issue subsequent read commands. After all 24 bits have been read, $\overline{\text{DRDY}}$ goes high. It is not necessary to read back all 24 bits, but $\overline{\text{DRDY}}$ will then not return high until new data is being updated. This mode may be terminated by the Stop Read Data Continuous command (SDATAC). Because DIN is constantly being monitored during the Read Data Continuous mode for the SDATAC or RESET command, do not use this mode if DIN and DOUT are connected together. See the Timing Characteristics for the required delay between the end of the RDATAC command and the beginning of shifting data on DOUT: T6.

Figure 5-10. ADC Command Timing - RDATAC Command



On the following $\overline{\text{DRDY}}$, shift out data by applying SCLKs. The Read Data Continuous mode terminates if input data equals the SDATAC or RESET command in any of the three bytes on DIN.

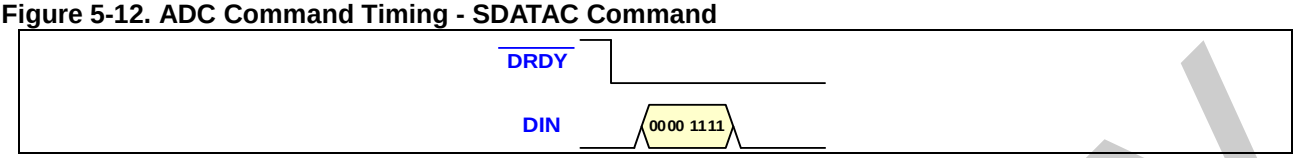
Figure 5-11. ADC Command Timing - DIN and DOUT Command during Read Continuous Mode



- **SDATAC: Stop Read Data Continuous**

Ends the continuous data output mode. (see RDATAC). The command must be issued after $\overline{\text{DRDY}}$ goes low and completed before $\overline{\text{DRDY}}$ goes high.

Figure 5-12. ADC Command Timing - SDATAC Command



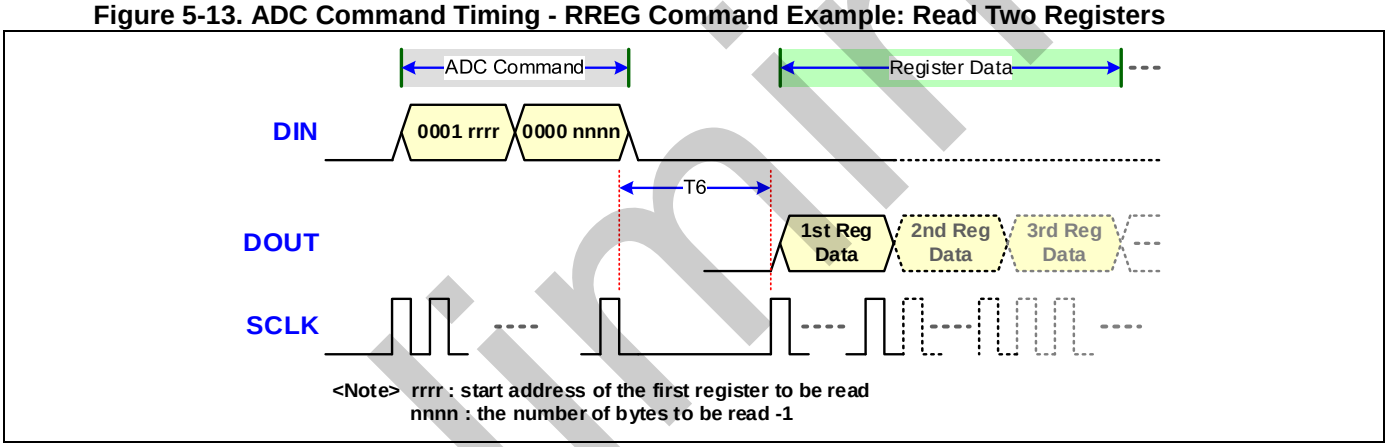
- **RREG: Read from Registers**

Output the data from up to 11 registers starting with the register address specified as part of the command. The number of registers read will be one plus the second byte of the command. If the count exceeds the remaining registers, the addresses will wrap back to the beginning.

- **1st Command Byte: 0001 *rrrr* where *rrrr* is the address of the first register to read.**
- **2nd Command Byte: 0000 *nnnn* where *nnnn* is the number of bytes to read – 1.**

See the Timing Characteristics for the required delay between the end of the RREG command and the beginning of shifting data on DOUT: T6.

Figure 5-13. ADC Command Timing - RREG Command Example: Read Two Registers

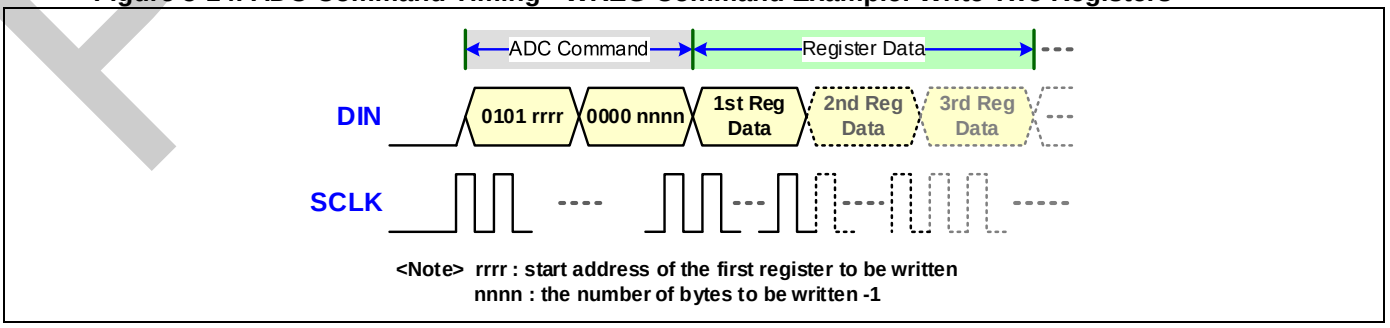


- **WREG: Write to Register**

Write to the registers starting with the register specified as part of the command. The number of registers that will be written is one plus the value of the second byte in the command.

- **1st Command Byte: 0001 *rrrr* where *rrrr* is the address of the first register to read.**
- **2nd Command Byte: 0000 *nnnn* where *nnnn* is the number of bytes to read – 1.**
- **Data Byte(s): data to be written to the registers.**

Figure 5-14. ADC Command Timing - WREG Command Example: Write Two Registers



- **SELFCAL: Self Offset and Gain Calibration**

  Performs a self-offset and self-gain calibration. The Offset Calibration Register (OFC) and Full-Scale Calibration Register (FSC) are updated after this operation. $\overline{\text{DRDY}}$ goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until $\overline{\text{DRDY}}$ goes low indicating that the calibration is complete.

- **SELFOCAL: Self Offset Calibration**

  Performs a self-offset calibration. The Offset Calibration Register (OFC) is updated after this operation. $\overline{\text{DRDY}}$ goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until $\overline{\text{DRDY}}$ goes low indicating that the calibration is complete.

- **SELFGCAL: Self Gain Calibration**

  Performs a self-gain calibration. The Full-Scale Calibration Register (FSC) is updated with new values after this operation. $\overline{\text{DRDY}}$ goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until $\overline{\text{DRDY}}$ goes low indicating that the calibration is complete.

- **SYSOCAL: System Offset Calibration**

  Performs a system offset calibration. The Offset Calibration Register (OFC) is updated after this operation. $\overline{\text{DRDY}}$ goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until $\overline{\text{DRDY}}$ goes low indicating that the calibration is complete.

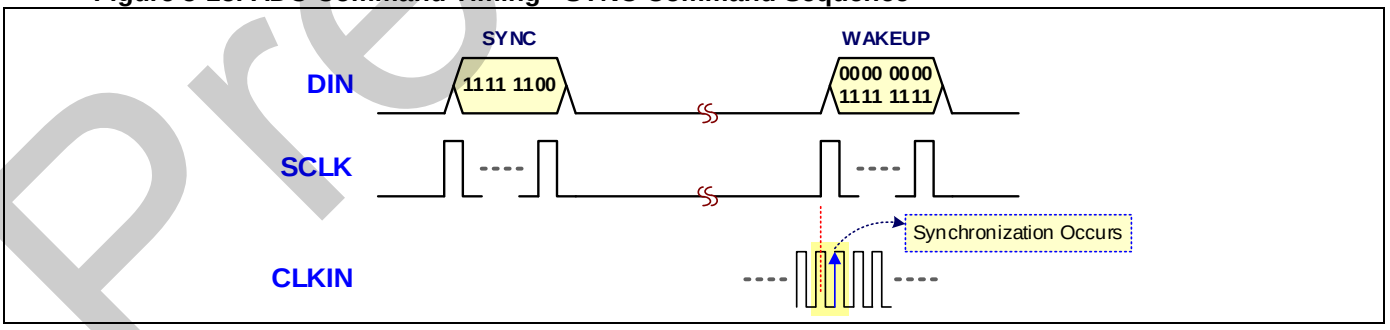
- **SYSGCAL: System Gain Calibration**

  Performs a system gain calibration. The Full-Scale Calibration Register (FSC) is updated after this operation. $\overline{\text{DRDY}}$ goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until $\overline{\text{DRDY}}$ goes low indicating that the calibration is complete.

- **SYNC: Synchronize the A/D Conversion**

  This command synchronizes the A/D conversion. To use, first shift in the command. Then shift in the WAKEUP command. Synchronization occurs on the first CLKIN rising edge after the first SCLK used to shift in the WAKEUP command.

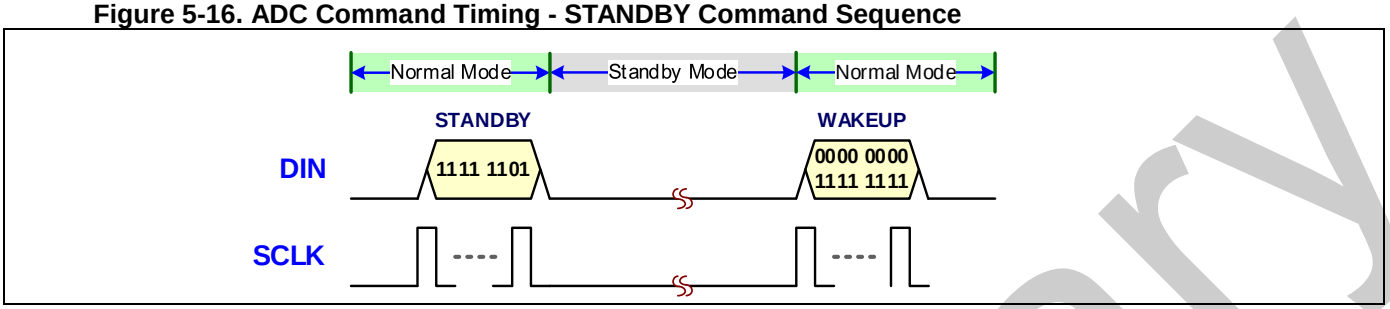
Figure 5-15. ADC Command Timing - SYNC Command Sequence



- **STANDBY: Standby Mode / One-Shot Mode**

This command puts the ADC into a low-power Standby mode. After issuing the STANDBY command, make sure there is no more activity on SCLK while CS is low, as this will interrupt Standby mode. If CS is high, SCLK activity is allowed during Standby mode. To exit Standby mode, issue the WAKEUP command. This command can also be used to perform single conversions.

Figure 5-16. ADC Command Timing - STANDBY Command Sequence



- **WAKEUP: Complete Synchronization or Exit Standby Mode**

Used in conjunction with the SYNC and STANDBY commands. Two values (all zeros or all ones) are available for this command.

- **RESET: Reset Registers to Default Values**

Returns all registers except the CLK0 and CLK1 bits in the ADCON register to their default values. This command will also stop the Read Continuous mode: in this case, issue the RESET command after $\overline{\text{DRDY}}$ goes low.

6. Function Registers

6.1. SADC Register Map

SADC Register Map

Offset	Register	7	6	5	4	3	2	1	0
0x00	SADC_STATUS	SADC_ID[3:0]				SADC_ORDER	SADC_ACAL	SADC_BUFEN	$\overline{\text{SADC\_DRDYF}}$
Reset	0x30	0	0	1	1	0	0	0	0
0x01	SADC_MUX	SADC_PSEL[3:0]				SADC_NSEL[3:0]			
Reset	0x10	0	0	0	1	0	0	0	0
0x02	SADC_ADCON	Reserved	SADC_CLK[1:0]		SADC_SDCS[1:0]		SADC_PGA[2:0]		
Reset	0x20	0	0	1	0	0	0	0	0
0x03	SADC_DRATE	SADC_DR[7:0]							
Reset	0x00	0	0	0	0	0	0	0	0
0x04	SADC_IO	SADC_DIR3	SADC_DIR2	SADC_DIR1	SADC_DIR0	SADC_DIO3	SADC_DIO2	SADC_DIO1	SADC_DIO
Reset	0xF0	1	1	1	1	0	0	0	0
0x05	SADC_OFC0	SADC_OFC0[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0
0x06	SADC_OFC1	SADC_OFC1[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0
0x07	SADC_OFC2	SADC_OFC2[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0
0x08	SADC_FSC0	SADC_FSC0[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0
0x09	SADC_FSC1	SADC_FSC1[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0
0x0A	SADC_FSC2	SADC_FSC2[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0

6.2. SADC Control Registers

6.2.1. SADC status register

SADC_STATUS	SADC status register		
Offset Address :	0x00	Reset Value :	0x30

Bit	Attr	Bit Name	Description	Reset
7..4	r	SADC_ID	ADC version ID. It is fixed 0x03	0x03
3	rw	SADC_ORDER	ADC output data order Lsb first enable. Input data is always shifted in most significant byte and bit first. Output data is always shifted out most significant byte first. This bit only controls the bit order of the output data within the byte. 0 = Disable : Most Significant Bit First 1 = Enable : Least Significant Bit First	0x00
2	rw	SADC_ACAL	ADC Auto-Calibration enable. 0 = Disable 1 = Enable	0x00
1	rw	SADC_BUFEN	ADC input buffer enable. 0 = Disable 1 = Enable	0x00
0	r	SADC_DRDYF	ADC data ready output status. 0 = No : data not ready 1 = Ready : data ready	0x00

6.2.2. SADC input channel multiplexer register

SADC_MUX	SADC input channel multiplexer register		
Offset Address :	0x01	Reset Value :	0x01

Bit	Attr	Bit Name	Description	Reset
7..4	rw	SADC_PSEL	ADC positive-ended input AINP channel Mux selection. When register value >= 8, the AINP Mux is always selected AINCOM pin. 0x0 = AIN0 0x1 = AIN1 0x2 = AIN2 0x3 = AIN3 0x4 = AIN4 0x5 = AIN5 0x6 = AIN6 0x7 = AIN7 0x8 = AINCOM	0x01
3..0	rw	SADC_NSEL	ADC negative-ended input AINN channel Mux selection. When register value >= 8, the AINP Mux is always selected AINCOM pin. 0x0 = AIN0 0x1 = AIN1 0x2 = AIN2 0x3 = AIN3 0x4 = AIN4 0x5 = AIN5 0x6 = AIN6 0x7 = AIN7 0x8 = AINCOM	0x00

6.2.3. SADC control register

SADC_ADCON	SADC control register		
Offset Address :	0x02	Reset Value :	0x20

Bit	Attr	Bit Name	Description	Reset
7	-	Reserved	Reserved	0x00
6..5	rw	SADC_CLK	D0/CLKOUT clock out rate select.0x0 = OFF : Clock out off0x1 = DIV1 : Clock out frequency equals fCLKIN0x2 = DIV2 : Clock out frequency equals fCLKIN/20x3 = DIV4 : Clock out frequency equals fCLKIN/4	0x01
4..3	rw	SADC_SDCS	Sensor detect current sources select. 0x0 = OFF : Sensor detect off 0x1 = DIV1 : Sensor detect current equals 0.5μA 0x2 = DIV2 : Sensor detect current equals 2μA 0x3 = DIV4 : Sensor detect current equals 10μA	0x00
2..0	rw	SADC_PGA	ADC input PGA gain adjust bits. 0x0 = X1 : multiplied by 1 0x1 = X2 : multiplied by 2 0x2 = X4 : multiplied by 4 0x3 = X8 : multiplied by 8 0x4 = X16 : multiplied by 16 0x5 = X32 : multiplied by 32 0x6 = X64 : multiplied by 64 0x7 = X64A : multiplied by 64	0x00

6.2.4. SADC data rate register

SADC_DRATE	SADC data rate register		
Offset Address :	0x03	Reset Value :	0xF0

Bit	Attr	Bit Name	Description	Reset
7..0	rw	SADC_DR	ADC data rate select. 0x03 = SPS2P5 : SPS 2.5Hz 0x13 = SPS5 : SPS 5Hz 0x23 = SPS10 : SPS 10Hz 0x33 = SPS15 : SPS 15Hz 0x43 = SPS25 : SPS 25Hz 0x53 = SPS30 : SPS 30Hz 0x63 = SPS50 : SPS 50Hz 0x72 = SPS60 : SPS 60Hz 0x82 = SPS80 : SPS 100Hz 0x92 = SPS160 : SPS 500Hz 0xA1 = SPS1000 : SPS 1000Hz 0xB0 = SPS2000 : SPS 2000Hz 0xC0 = SPS3750 : SPS 3750Hz 0xD0 = SPS7500 : SPS 7500Hz 0xE0 = SPS15000 : SPS 15000Hz 0xF0 = SPS30000 : SPS 3000Hz	0x00

6.2.5. SADC control register 2

SADC_IO	SADC control register 2		
Offset Address :	0x04	Reset Value :	0xE0

Bit	Attr	Bit Name	Description	Reset
7	rw	SADC_DIR3	ADC D3 pin IO direction select. 0 = Output 1 = Input	0x01

6	rw	SADC_DIR2	ADC D2 pin IO direction select. 0 = Output 1 = Input	0x01
5	rw	SADC_DIR1	ADC D1 pin IO direction select. 0 = Output 1 = Input	0x01
4	rw	SADC_DIR0	ADC D0 pin IO direction select. This pin is also able to do as clock out CLKOUT. 0 = Output 1 = Input	0x01
3	rw	SADC_DIO3	ADC status of D3 pin. This bit is reading to indicate the state of the D3 pin. When the digital I/O pin is configured as output pin by the SADC_DIR3 bit, writing to this bit will set the output state. When the digital I/O pin is configured as an input by the SADC_DIR3 bit, writing to this bit will be no effect.	0x00
2	rw	SADC_DIO2	ADC status of D2 pin. This bit is reading to indicate the state of the D2 pin. When the digital I/O pin is configured as output pin by the SADC_DIR2 bit, writing to this bit will set the output state. When the digital I/O pin is configured as an input by the SADC_DIR2 bit, writing to this bit will be no effect.	0x00
1	rw	SADC_DIO1	ADC status of D1 pin. This bit is reading to indicate the state of the D1 pin. When the digital I/O pin is configured as output pin by the SADC_DIR1 bit, writing to this bit will set the output state. When the digital I/O pin is configured as an input by the SADC_DIR1 bit, writing to this bit will be no effect.	0x00
0	rw	SADC_DIO	ADC status of D0 pin. This bit is reading to indicate the state of the D0 pin. When the digital I/O pin is configured as output pin by the SADC_DIR0 bit, writing to this bit will set the output state. When the digital I/O pin is configured as an input by the SADC_DIR0 bit, writing to this bit will be no effect. When the digital I/O pin is configured as an output and CLKOUT is enabled by SADC_CLK bits, writing to this bit will be no effect.	0x00

6.2.6. SADC offset calibration byte 0

SADC_OFC0	SADC offset calibration byte 0		
Offset Address :	0x05	Reset Value :	0x00000000

Bit	Attr	Bit Name	Description	Reset
7..0	rw	SADC_OFC0	ADC offset calibration result OFC[7:0] (byte-0, least significant byte).	0x00

6.2.7. SADC offset calibration byte 1

SADC_OFC1	SADC offset calibration byte 1		
Offset Address :	0x06	Reset Value :	0x00000000

Bit	Attr	Bit Name	Description	Reset
7..0	rw	SADC_OFC1	ADC offset calibration result OFC[15:8] (byte-1).	0x00

6.2.8. SADC offset calibration byte 2

SADC_OFC2	SADC offset calibration byte 2		
Offset Address :	0x07	Reset Value :	0x00000000

Bit	Attr	Bit Name	Description	Reset

7..0	rw	SADC_OFC2	ADC offset calibration result OFC[23:16] (byte-2, most significant byte).	0x00

6.2.9. SADC full−scale calibration byte 0

SADC_FSC0	SADC full−scale calibration byte 0		
Offset Address :	0x08	Reset Value :	0x00000000

Bit	Attr	Bit Name	Description	Reset
7..0	rw	SADC_FSC0	ADC full−scale calibration result FSC[7:0] (byte-0, least significant byte).	0x00

6.2.10. SADC full−scale calibration byte 1

SADC_FSC1	SADC full−scale calibration byte 1		
Offset Address :	0x09	Reset Value :	0x00000000

Bit	Attr	Bit Name	Description	Reset
7..0	rw	SADC_FSC1	ADC full−scale calibration result FSC[15:8] (byte-1).	0x00

6.2.11. SADC full−scale calibration byte 2

SADC_FSC2	SADC full−scale calibration byte 2		
Offset Address :	0x0A	Reset Value :	0x00000000

Bit	Attr	Bit Name	Description	Reset
7..0	rw	SADC_FSC2	ADC full−scale calibration result FSC[23:16] (byte-2, most significant byte).	0x00

7. Application Notes

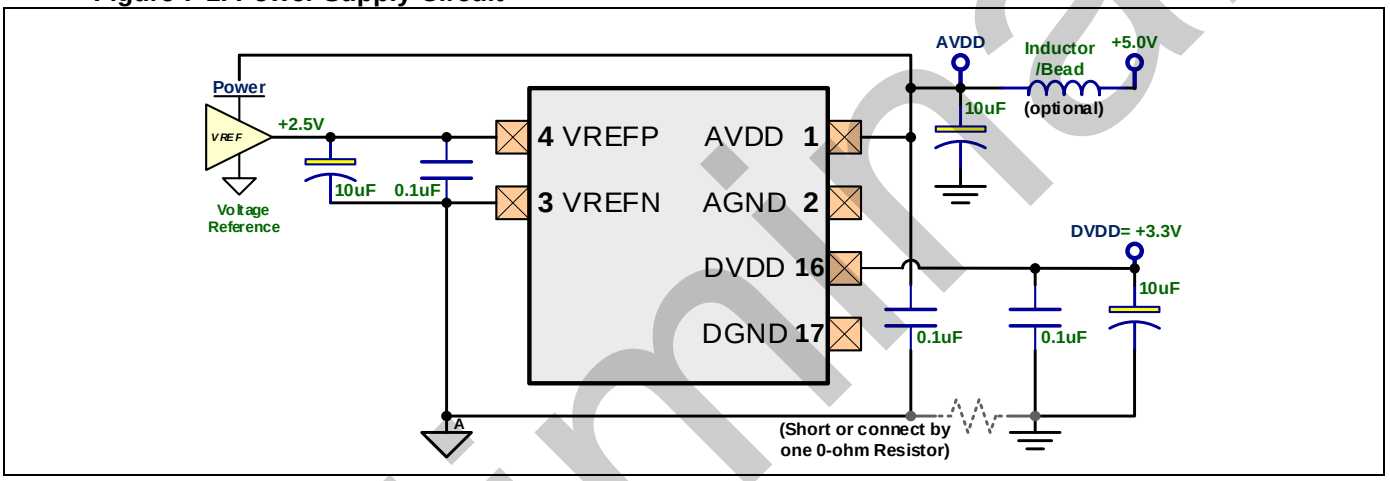
7.1. Power Supply Circuit

To have the chip work with power supply varying from 4.75V to 5.25V for AVDD and 1.8V to 3.6V for DVDD. Adding some external decoupling and bypass capacitors is necessary on **AVDD/AVSS** analog power pins and **DVDD/DVSS** digital power pins, as shown in following figure.

The ADC reference voltage source can be from external quiet reference voltage source. It must add some bypass and decoupling capacitors, as shown in following figure. AVDD voltage is coming from DVDD by through a ferrite bead or resister. Suggests to separate analog and digital ground areas on PCB to reduce the digital signals' interference to analog ADC. User can connect these two ground areas through a resister or short on PCB at a single point. Please place the related components of **VREFP**, **VREFN**, **AVDD**, **AINn** and **AINCOM** pins on analog ground area. Please place the related components of **DVDD**, **SCLK**, **DIN**, **DOUT** and other digital IO pins on digital ground area.

The following figure is showing the power supply suggestion circuit.

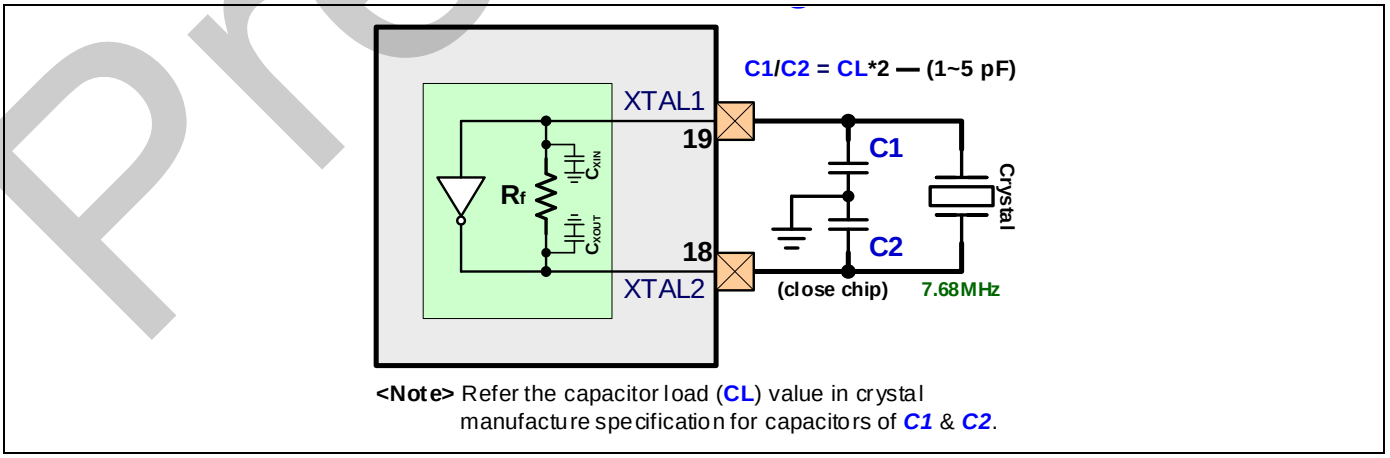
Figure 7-1. Power Supply Circuit



7.2. Crystal Oscillating Circuit

To achieve successful and exact oscillating (7.68MHz), the capacitors ***C1*** and ***C2*** are necessary, as shown in following figure. Normally, ***C1*** and ***C2*** have the same value. Refer the capacitor load (**CL**) value in crystal manufacture specification for the final matching capacitor of ***C1*** & ***C2***.

Figure 7-2. Crystal Oscillating Circuit



<Note> Refer the capacitor load (**CL**) value in crystal manufacture specification for capacitors of ***C1*** & ***C2***.

7.3. ADC Analog Input Circuit

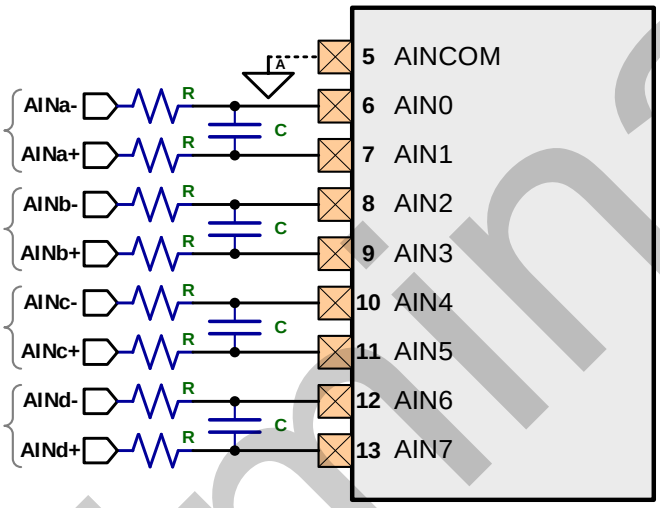
7.3.1. Analog Input – Differential Mode

When ADC inputs as analog differential voltage input on application, each two pins of **AIN0** to **AIN7** are able to do as a couple of differential input pair. For the differential mode, the **AINCOM** pin is not used.

To achieve the analog input circuit successful, the analog input filter circuit is strongly suggested to add before the external analog signal input to the **AIN0** ~ **AIN7** pins. The suggested analog filter circuit is used two identified series-connection resistors ***R*** in each differential input path with one parallel-connection common-mode rejection capacitor ***C.*** It can filter the aliasing during the ADC sampling and reduce external coupling noise.

The following figure is showing the analog input circuit with differential mode.

Figure 7-3. Analog Input – Differential Mode



<Note> The resistor **R** is suggested 100~1K ohm and **C** is suggested 0.1uF by actual application request.

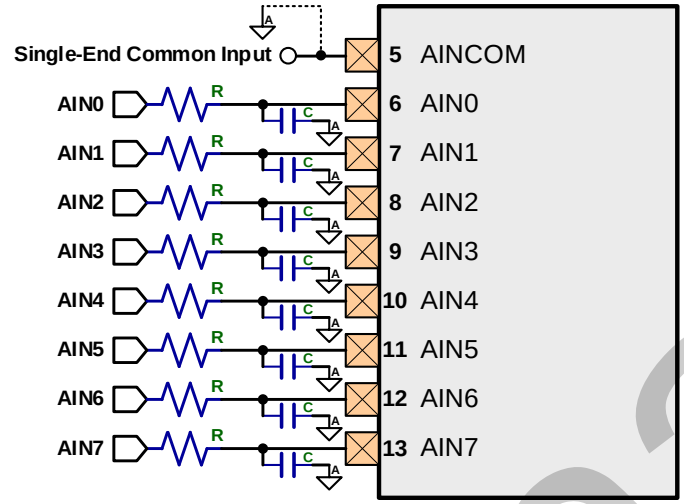
7.3.2. Analog Input – Single-End Mode

When ADC inputs as analog single-end voltage input on application, each one pin of **AIN0** to **AIN7** and **AINCOM** pins are able to do analog input with single-end mode. For the single-end mode, the **AINCOM** pin is used the common input. Usually, It is can be tied to ground for most application.

To achieve the analog input circuit successful, the analog input filter circuit is strongly suggested to add before the external analog signal input to the **AIN0** ~ **AIN7** and **AINCOM** pins. The suggested analog filter circuit is used a series-connection resistors ***R*** in each input path with one parallel-connection to ground capacitor ***C.*** It can filter the aliasing during the ADC sampling and reduce external coupling noise.

The following figure is showing the analog input circuit with differential mode.

Figure 7-4. Analog Input – Single-End Mode



<Note> The resistor **R** is suggested 100~1K ohm and **C** is suggested 0.1uF by actual application request.

For Test Chip:

(In Single-End Mode) User needs to control **SADC_MUX** (Address **0x01**) to write **0x80~0x87** to select which channel and convert the output to a positive value.

1. **SADC_PSEL** is fixed at **0x8**.
2. **SADC_NSEL** accepts value from **0x0** to **0x7**. (0x0 means **AIN0**, 0x1 means **AIN1** … 0x7 means **AIN7**.)

SADC_MUX	SADC input channel multiplexer register		
Offset Address :	**0x01**	**Reset Value :**	**0x10**

Bit	Attr	Bit Name	Description	Reset
7..4	rw	SADC_PSEL	ADC positive-ended input AINP channel Mux selection. When register value >= 8, the AINP Mux is always selected AINCOM pin. 0x0 = AIN0 0x1 = AIN1 0x2 = AIN2 0x3 = AIN3 0x4 = AIN4 0x5 = AIN5 0x6 = AIN6 0x7 = AIN7 0x8 = AINCOM	0x01
3..0	rw	SADC_NSEL	ADC negative-ended input AINN channel Mux selection. When register value >= 8, the AINP Mux is always selected AINCOM pin. 0x0 = AIN0 0x1 = AIN1 0x2 = AIN2 0x3 = AIN3 0x4 = AIN4 0x5 = AIN5 0x6 = AIN6 0x7 = AIN7 0x8 = AINCOM	0x00

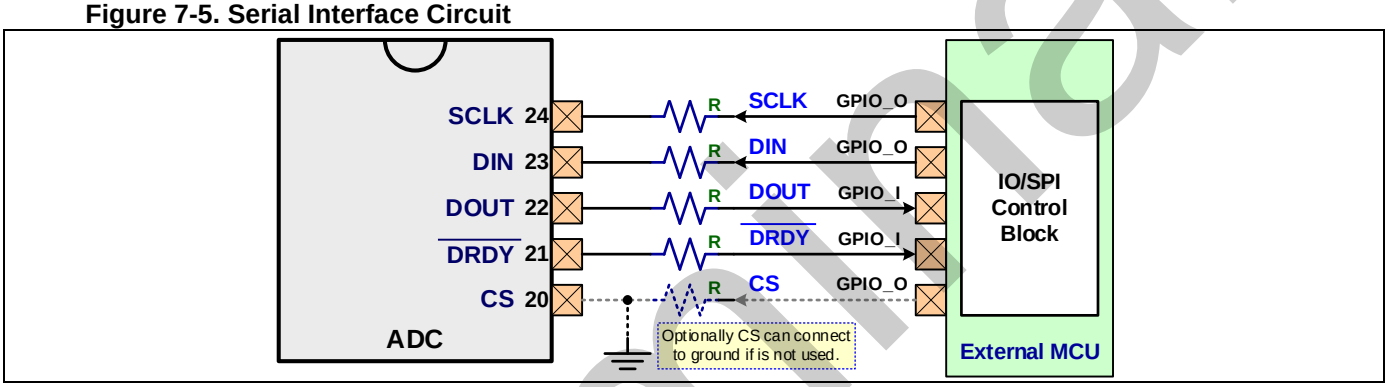
7.4. Serial Interface Circuit

The ADC communication is handled by a SPI compatible serial interface to get ADC code and control the ADC settings from external MCU device. The **SCLK**, **DIN**, **DOUT** and **CS** pins are using as SPI compatible serial interface. When the ADC communication is a simple one MCU (master) with one ADC (slave) on user application, the **CS** pin can be not used optionally. It can directly connect to digital ground. The $\overline{\text{DRDY}}$ pin is an output signal to indicate the ADC data is ready. ADC output the signal to notify MCU ADC has converted one ADC sample and MCU can get the ADC code.

For the ADC communication signals voltage level, the ADC DVDD voltage is same as MCU VDD power voltage generally. An inductor, ferrite bead or resistor is suggested to connect between DVDD and MCU VDD with a 0.1uF capacitor and a 10uF capacitor. These parts are used as the low pass filter to filter the digital noise from ADC outside.

The following figure is showing the ADC serial interface circuit example diagram.

Figure 7-5. Serial Interface Circuit

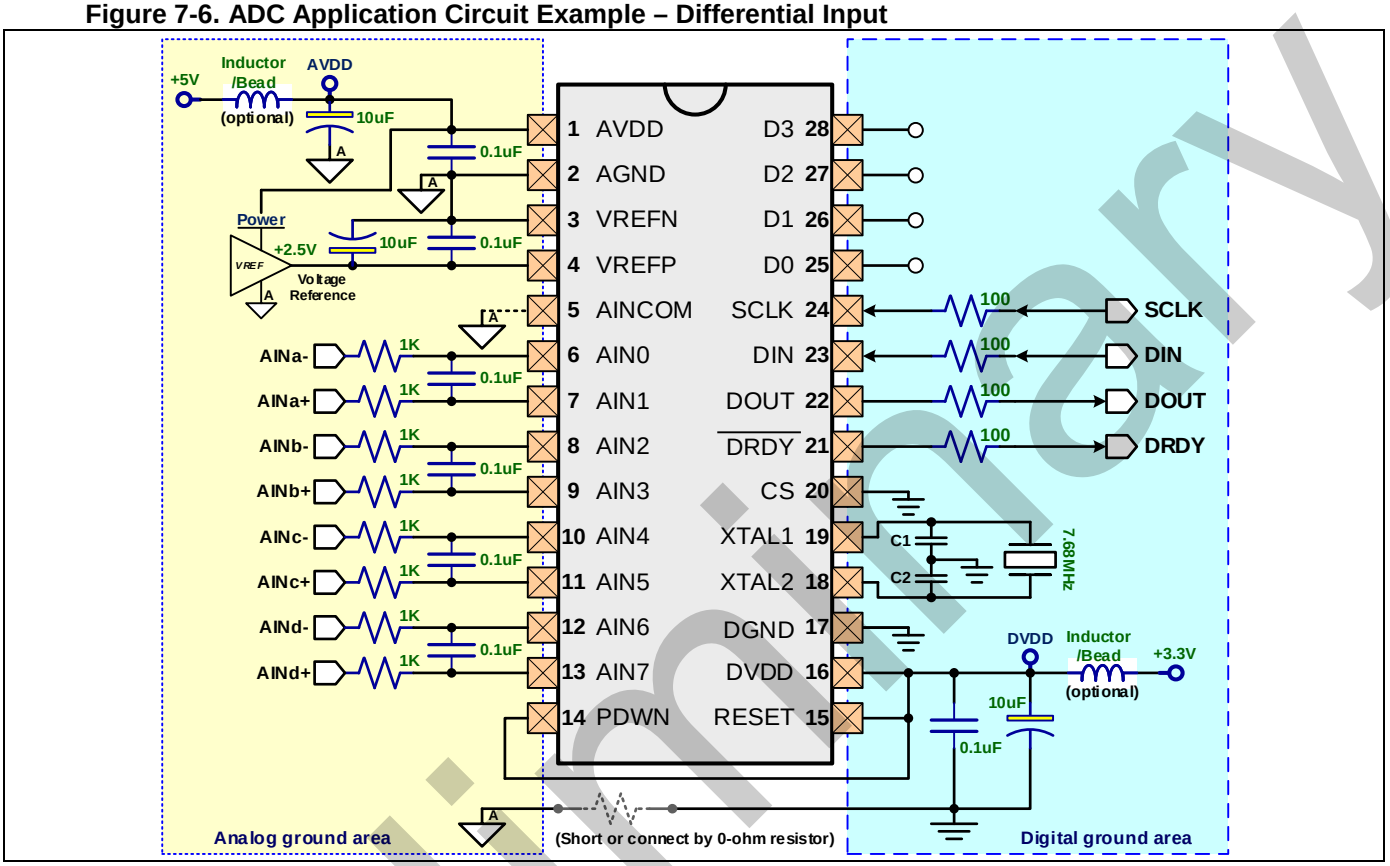


7.5. Application Circuit Example

7.5.1. ADC Application Circuit Example – Differential Input

The following figure is an ADC application circuit example with analog differential input. The ADC have the power supply varying from 4.75V to 5.25V for AVDD and 1.8V to 3.6V for DVDD.

Figure 7-6. ADC Application Circuit Example – Differential Input



8. Electrical Characteristics

8.1. Parameter Glossary

Table 8-1. Parameter Glossary

Symbol	Definition	Descriptions
Abbreviations for electrical characteristics		
Min	Minimum value	Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value.
Max	Maximum value	Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value.
Typ	Typical value	Unless otherwise specified, the value is based on TA=25 °C, AVDD=+5V, DVDD=+1.8V.
AVDD DVDD	Power supply voltage	The voltage range is specified in characteristics table or conditions column.
AGND DGND	Power reference voltage	Unless otherwise specified, all voltages are referred to AGND for analog parameters and DGND for digital parameters.
TA	Ambient temperature	The temperature range is specified in characteristics table or conditions column.

8.2. Absolute Maximum Rating

Table 8-2. Absolute Maximum Rating

Parameter	Rating	Unit
AVDD to AGND	−0.3 to +6	**Volt**
DVDD to DGND	−0.3 to +3.6	**Volt**
AGND to DGND	−0.3 to +0.3	**Volt**
Input Current	100, Momentary	**mA**
	10, Continuous	**mA**
Analog inputs to AGND	−0.3 to AVDD + 0.3	**Volt**
Digital inputs: D0, D1, D2, D3, XTAL1 to DGND	−0.3 to DVDD + 0.3	**Volt**
Digital inputs: DIN, SCLK, CS, RESET, PDWN to DGND	−0.3 to +6	**Volt**
Operating Temperature Range	-40 ~ +105	**°C**
Storage Temperature Rang	-60 ~ +150	**°C**

Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

8.3. ADC Characteristics

Table 8-3. ADC Characteristics

AVDD=5.0V, DVDD=1.8V, fCLKIN=7.68MHz, PGA=1, VREF=+2.5V, TA= -40 ~ +85 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
AVDD	Analog Supply Voltage		**4.75**		**5.25**	**Volt**

DVDD	Digital Supply Voltage		**1.8**		**3.6**	**Volt**
TEMP	Operation Temperature		**-40**		**85**	**°C**
Analog Inputs						
V_{Diff}	Full scale differential input range	AINP-AINN voltage	**-2VREF/PGA**		**+2VREF/PGA**	**Volt**
V_{CM}	Absolute input voltage (Common mode input range)	Buffer Off	**AGND-0.1**		**AVDD+0.1**	**Volt**
		Buffer On	**AGND**		**AVDD-2.0**	**Volt**
PGA	Programmable gain amplifier gain ratio		**1**		**64**	
R_{InDiff}	Differential input impedance	Buffer Off, PGA=1,2,4,8,16		**150/PGA**		**KOhm**
		Buffer Off, PGA=32,64		**5**		**KOhm**
		Buffer On		**10**		**MOhm**
I_{SDC}	Sensor detect current sources	SADC_SDCS = 1		**0.5**		**uA**
		SADC_SDCS = 2		**2**		**uA**
		SADC_SDCS = 3		**10**		**uA**
System Performance						
Bits	Resolution			**24**		**bits**
F_{DATA}	Data rate (fDATA)	fCLKIN = 7.68MHz	**2.5**		**30000**	**SPS**
INL	Integral nonlinearity (INL)	Differential input, PGA = 1		**±0.001**		**%FSR**
		Differential input, PGA = 64		**±0.002**		**%FSR**
E_{OFFSET}	Offset error	After calibration	On the level of the noise			
D_{OFFSET}	Offset drift	PGA = 1		**±106**		**nV/°C**
		PGA = 64		**±6**		**nV/°C**
E_{GAIN}	Gain error	After calibration, PGA = 1, Buffer on		**±0.01**		**%**
		After calibration, PGA = 64, Buffer on		**±0.05**		**%**
D_{GAIN}	Gain drift	PGA = 1 to 64		**±1**		**ppm/°C**
	Common mode rejection			**105**		**dB**
ENOB	Effective number of bits	2.5 SPS, PGA=1		**23.14**		**bits**
		2.5 SPS, PGA=64		**20.92**		**bits**
		10 SPS, PGA=1		**21.82**		**bits**
		10 SPS, PGA=64		**20.17**		**bits**
		30 SPS, PGA=1		**21.23**		**bits**
		30 SPS, PGA=64		**20.09**		**bits**
		1000 SPS, PGA=1		**18.61**		**bits**
		1000 SPS, PGA=64		**17.57**		**bits**
		30K SPS, PGA=1		**16.91**		**bits**
		30K SPS, PGA=64		**16.14**		**bits**
Voltage Reference						
V_{REF}	Reference Input Voltage	VREF = VREFP − VREFN	**0.5**	**2.5**	**2.6**	**Volt**
V_{REFN}	Negative reference input	Buffer Off	**AGND-0.1**		**V_{REFP} -0.5**	**Volt**
		Buffer On	**AGND**		**V_{REFP} -0.5**	**Volt**
V_{REFP}	Positive reference input	Buffer Off	**V_{REFN} +0.5**		**AVDD+0.1**	**Volt**
		Buffer On	**V_{REFN} +0.5**		**AVDD-2.0**	**Volt**
R_{VREF}	Voltage reference impedance	fCLKIN = 7.68MHz		**20.0**		**Kohm**
IO Characteristics						
V_{IH}	Input High voltage	DIN, SCLK, XTAL1, PDWN, CS, RESET	**0.5 DVDD**		**5.25**	**Volt**
		D0, D1, D2, D3	**0.4 DVDD**		**DVDD**	**Volt**

V_{IL}	Input Low voltage		DGND		0.5 DVDD	Volt
V_{OH}	Output High voltage	I_{OH} = 5mA	0.8 DVDD			mA
V_{OL}	Output Low voltage	I_{OL} = 5mA			0.2 DVDD	mA
F_{CLKIN}	Master clock rate (fCLKIN)	External crystal (XTAL1, XTAL2)	2	7.68	10	MHz
		External oscillator driving CLKIN	0.1	7.68	10	MHz
Current Consumption						
I_{AVDD}	Analog Current	Power-down mode			0.009	uA
		Standby mode		15		uA
		Normal mode, PGA=1, Buffer off		7		mA
		Normal mode, PGA=64, Buffer off		16		mA
		Normal mode, PGA=1, Buffer on		14		mA
		Normal mode, PGA=64, Buffer on		30		mA
I_{DVDD}	Digital Current	Power-down mode			3.8	uA
		Standby mode, CLKOUT off, DVDD = 3.3V		210		uA
		Normal mode, CLKOUT off, DVDD = 3.3V			2	mA

1. SPS = samples per second, FSR = full-scale range = 4VREF/PGA.

8.4. AC Timing Characteristics

Table 8-4. AC Timing Characteristics

DVDD= 1.8V ~ 3.6V, DGND= 0V, TA = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Serial Interface Timing						
T1	SCLK period		4			T_{CLKIN}
					10	T_{DATA}
T2H	SCLK pulse width high time		200			ns
					9	T_{DATA}
T2L	SCLK pulse width low time		200			ns
T3	CS low to first SCLK: setup time (CS can be tied low)		0			ns
T4	Valid DIN to SCLK falling edge: setup time		50			ns
T5	Valid DIN to SCLK falling edge: hold time		50			ns
T6	Delay from last SCLK falling edge for DIN to first SCLK rising edge for DOUT: RDATA, RDATAC, RREG Commands		50			T_{CLKIN}
T7	SCLK rising edge to valid new DOUT: propagation delay (DOUT load = 20pF ‖ 100kΩ to DGND)				50	ns
T8	SCLK rising edge to DOUT invalid: hold time		0			ns
T9	Last SCLK falling edge to DOUT high impedance (DOUT goes high impedance immediately when CS goes high)		6		10	T_{CLKIN}
T10	CS low after final SCLK falling edge		8			T_{CLKIN}

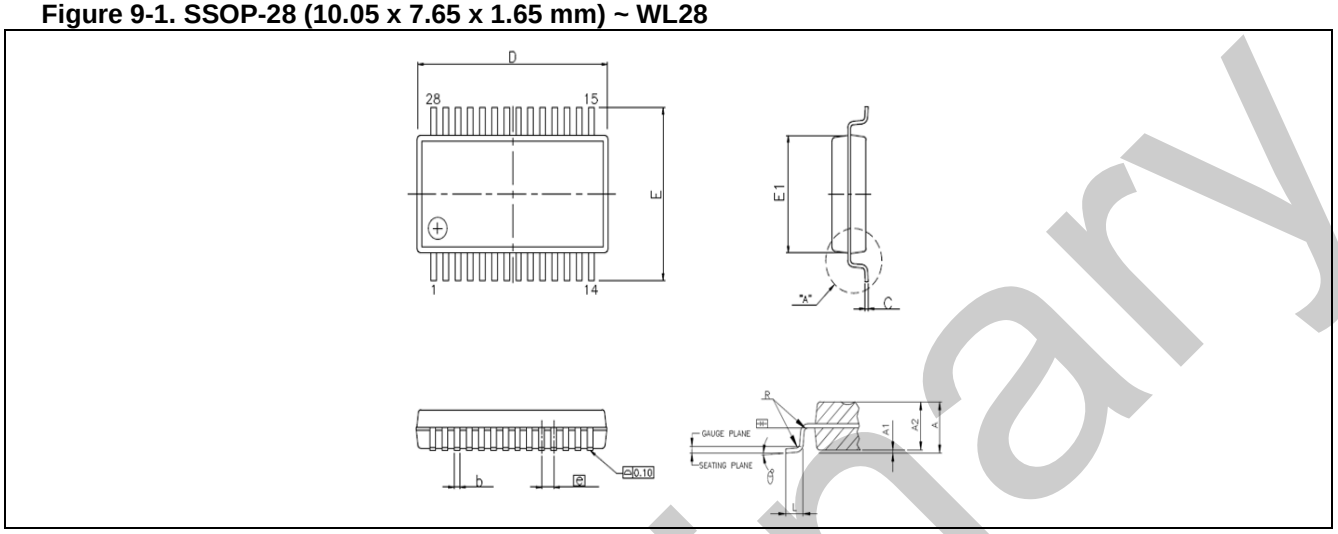
T11	Final SCLK falling edge of command to first SCLK rising edge of next command.	RREG, WREG, RDATA	**4**			**T_{CLKIN}**
		RDATAC, SYNC	**24**			**T_{CLKIN}**
		RDATAC, RESET, STANDBY, SELFOCAL, SYSOCAL, SELFGCAL, SYSGCAL, SELFCAL	**Wait for $\overline{DRDY}$ to go low**			.
SCLK Reset Timing						
T12	SCLK reset pattern, first high pulse		**300**		**500**	**T_{CLKIN}**
T13	SCLK reset pattern, low pulse		**5**			**T_{CLKIN}**
T14	SCLK reset pattern, second high pulse		**550**		**750**	**T_{CLKIN}**
T15	SCLK reset pattern, third high pulse		**1050**		**1250**	**T_{CLKIN}**
RESET and PDWN Timing						
T16	RESET, PDWN pulse width		**4**			**T_{CLKIN}**
T16B	PDWN rising edge to CLKIN rising edge		**-25**		**25**	**ns**
$\overline{DRDY}$ Update Timing						
T17	Conversion data invalid while being updated ($\overline{DRDY}$ shown with no data retrieval)		**16**			**T_{CLKIN}**

T_{CLKIN} : master clock period = 1/fCLKIN; T_{DATA} : output data period 1/fDATA.

9. Package Dimension

9.1. SSOP-28W

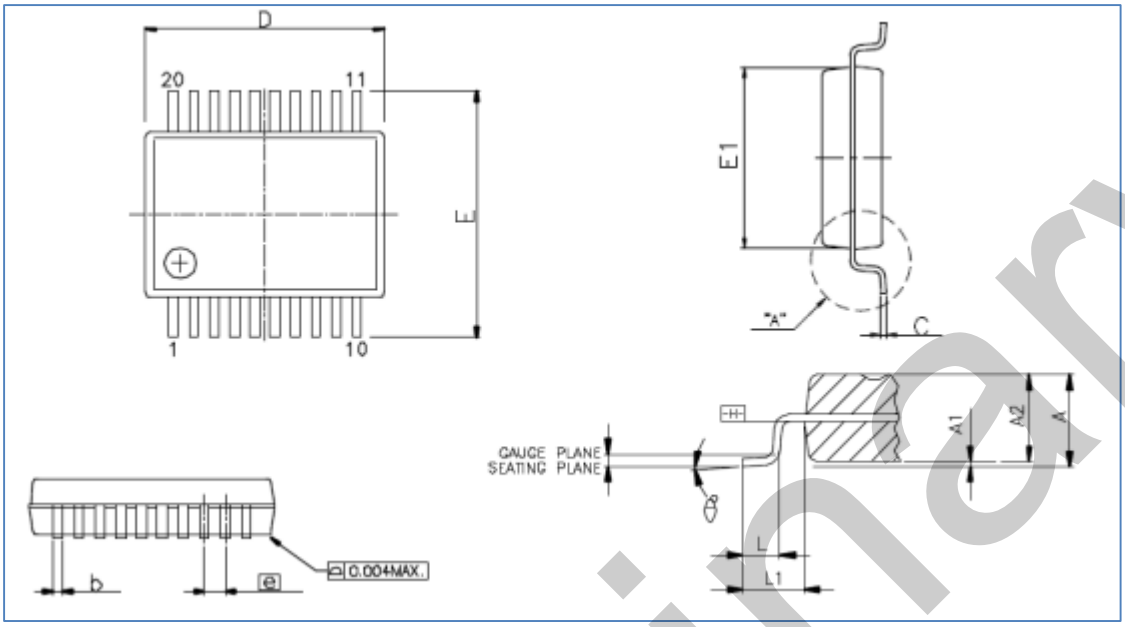
Figure 9-1. SSOP-28 (10.05 x 7.65 x 1.65 mm) ~ WL28



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	----	----	2.00	----	----	0.079
A1	0.05	----	----	0.002	----	----
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	----	0.38	0.009	----	0.015
C	0.09	----	0.25	0.004	----	0.010
D	10.05	10.20	10.50	0.396	0.405	0.413
E	7.65	7.80	7.90	0.301	0.306	0.311
E1	5.00	5.30	5.60	0.197	0.209	0.220
e	0.65 BASIC			0.026 BASIC		
L	0.55	0.75	0.95	0.022	0.029	0.037
R	0.09	----	----	0.004	----	----
θ°	0∘	4∘	8∘	0∘	4°	8°

9.2. SSOP-20W

Figure 9-2. SSOP-20 (7.2 x 7.8 x 1.75 mm) ~ WL20



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	----	----	2.00	----	----	0.079
A1	0.05	----	----	0.002	----	----
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	----	0.38	0.009	----	0.015
C	0.09	----	0.21	0.004	----	0.010
D	6.90	7.20	7.50	0.396	0.405	0.413
E	7.40	7.80	8.20	0.301	0.306	0.311
E1	5.00	5.30	5.60	0.197	0.209	0.220
e		0.65 BASIC			0.026 BASIC	
L	0.55	0.75	0.95	0.022	0.029	0.037
R	----	1.25	----	0.004	----	----
θ°	0°	4°	8°	0°	4°	8°

10. Revision History

Revision V0.17 (2026_0908)		**Chapter**
1	Add package SSOP 20	4.9
Revision V0.16 (2026_0506)		**Chapter**
1	Title add preliminary	All
Revision V0.15 (2026_0330)		**Chapter**
1	Add pin define AIN5~AIN7	1
Revision V0.14 (2026_0327)		**Chapter**
1	Add ENOB temperature line chart.	6.2
Revision V0.13 (2026_0129)		**Chapter**
1	Modify SADC Control Registers – Reset value.	6.2
Revision V0.12 (2026_0108)		**Chapter**
1	Replace DRDY by $\overline{\text{DRDY}}$.	All
2	Modify ENOB & Noise Free bits table.	5.4.6
3	Modify Single-End mode parameters.	7.3.2
Revision V0.11 (2025_1229)		**Chapter**
1	Preliminary version.	

11. Disclaimers

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