MG32L003xx

32-bit ARM® Cortex™-M0+ MCU

Up to 64KB Flash / 4KB SRAM, 10 TIMs, 12-bit ADC, 6 comm.interfaces

Features

- Core:32-bit ARM ® Cortex™-M0+ MCU
  - 24 MHz maximum frequency
  - support 0 wait state access
- Memories
  - 64Kbytes Flash
  - 4KB SRAM
- Power Supply: 2.5V~5.5V
- Operation temperature : (-40~85°C)
- Low Voltage Detector（LVD）/Voltage Comparator（VCMP）
- Clock management
  - 4 ~24MHz External high speed clock（HSE）
  - 4 ~24MHz Internal high speed clock（HSI）
  - 32.768KHz External low speed clock（LSE）
  - 38.4/32.768KHz Internal low speed clock（LSI）
- Three operation: run mode, sleep mode, deep sleep mode
- Maximum 28 I/O ports
- Debug mode
  - Serial wire debug (SWD) , 2 watch points/4 break points
- 128-bit unique ID
- 6 communication interfaces
  - Up to 2 UART
  - 1 LPUART
  - 1 SPI
  - 1 I2C
  - one 1-wire
- Buzzer generator
- Up to 10 timers
  - 1 16-bit advanced timers， 3 pairs of complementary outputs
  - 1 16-bit general purpose timer
  - 1 16-bit programmable timer
  - Up to two 16/32bit basic timer
  - 2 watchdog timers (Independent and Window)
  - one 16-bit low power timer
  - 1 SysTick timer
  - 1 8-bit automatic wake-up timer
- RTC clock counter(record the year, month, day, hour, minute and second)
- One 12-bit ADC(SAR)
  - Max convert rate: 1Msps
  - Maximum 16 channels
- CRC-16 calculation Unit

Contents

1 Introduction

The MG32L003xx microcontroller incorporate the ARM ® Cortex™-M0+ core, operating at a 24MHz frequency, extensive range of enhanced , large-capacity Flash and SRAM. The MG32L003xx operate in the- 40 to +85 °C temperature range from a 2.5 to 5.5V power supply.

The MG32L003xx family products have TSSOP20, QFN20 , , LQFP32 ,QFN32 packages, different packages have different peripherals.

This series and other series of datasheets, reference manuals, product selection tables, etc. are from the website(http://www.megawin.com.tw/).

2 Overview

2.1 Product features and peripheral counts

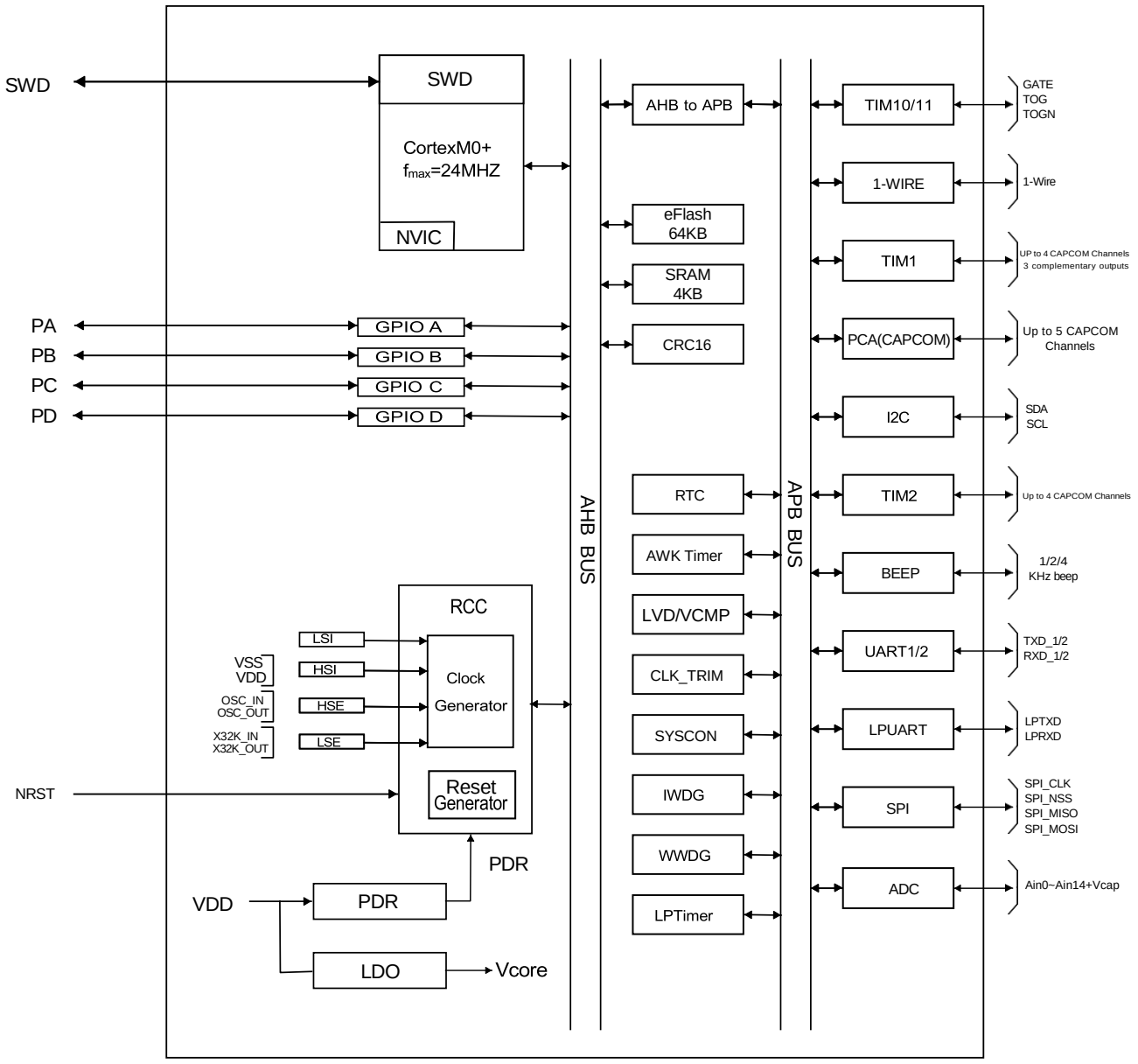
Tab2.1- 1 shows the features and peripheral counts, package and characteristic parameters of this series of products.

Tab 2.1-1 **Product features and peripheral counts**

Name / Function	MG32L003F8	MG32L003K8
Pin count	20	32
CPU Frequency	24MHz	
Voltage operating (V)	2.5V~5.5V	
Temperature range(Ta, °C)	-40~+85	
Flash Protection	YES	
Number of GPIOs	16	28
External Interrupt	16	28
Advanced Timer(TIM1)	1	
General purpose(TIM2)	1	
Timer array(PCA)	1	
TIM10/11	2	
ADC channels	15	
Flash(KB)	64	
SRAM(KB)	4	
IWDG	1	
WWDG	1	
1-WIRE	1	
CRC16	1	
UART	2	
LPUART	1	
SPI	1(12Mbps)	
I2C	1	
Buzzer	1	
AWK	1	
RTC	1	
LVD/VCMP	YES	
Packages	TSSOP20, QFN20	LQFP32,QFN32

2.2 Block Diagram

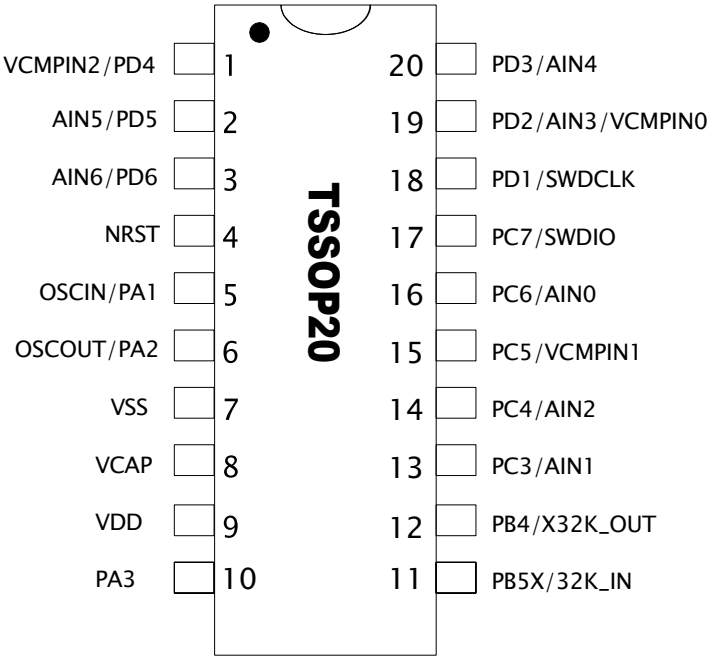
Fig 2.2-1 **Block Diagram**



3 Pinouts and pin descriptions

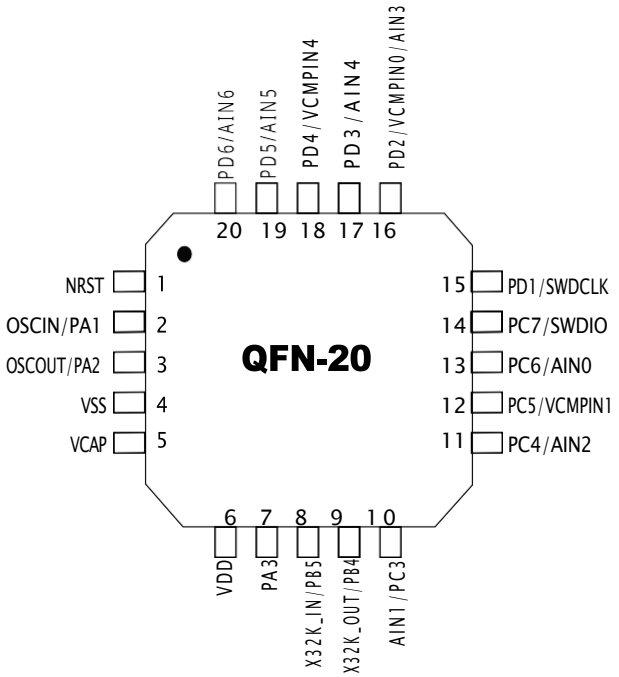
3.1 TSSOP20 Pinout

Fig 3.1-1 **TSSOP20 Pinout**



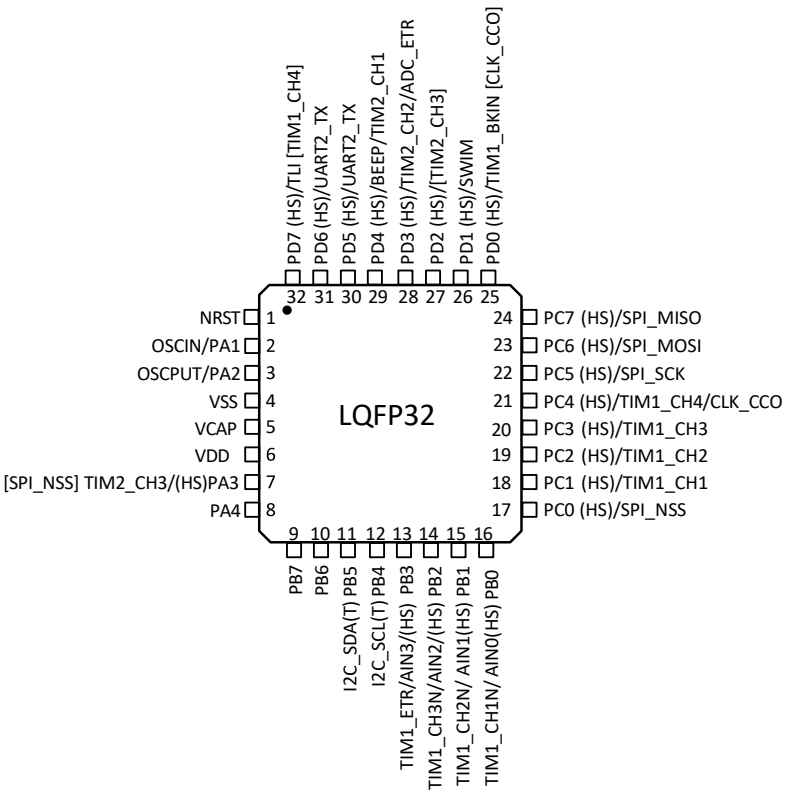
3.2 QFN-20 Pinout

Fig 3.2-1 **QFN-20 Pinout**



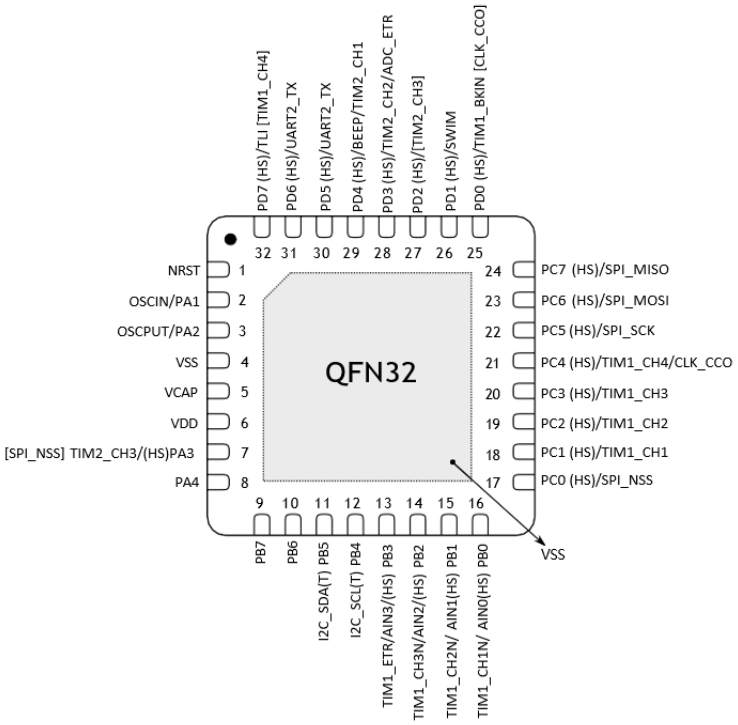
3.3 LQFP-32 Pinout

Fig 3.3- 1 LQFP- 32 Pinout



3.4 QFN-32 Pinout

Fig 3.4- 1 QFN- 32 Pinout



Tab 3.4- 1 GPIO multiplexing of TSSOP20 , QFN20 ,LQFP32/QFN32

Package			GPIO Multiplexing												
LQFP32/QFN32	TSSOP20	QFPN20	name	0	1	2	3	4	5	6	7	8	9	F
29	1	18		PD4	TIM1_CH1	PCA_CH0	RTC_1HZ	TIM10_TOG	UART1_TXD	TIM10_EXT	BEEP	TIM2_CH1		VCMPIN2
30	2	19		PD5	TIM1_CH1N	PCA_CH4	SPI_MISO	I2C_SCL	UART2_TXD	TIM10_GATE	UART1_TXD	TIM2_CH4		AIN5
31	3	20		PD6	TIM1_CH2	PCA_CH3	SPI_MOSI	I2C_SDA	UART2_RXD	LPTIM_EXT	UART1_RXD	TIM2_CH2		AIN6
1	4	1	NRST											
2	5	2		PA1	TIM1_CH2N		SPI_CLK	I2C_SDA	UART1_RXD	TIM10_TOG	UART2_RXD			OSC_IN
3	6	3		PA2	TIM1_CH3		SPI_NSS	I2C_SCL	UART1_TXD	TIM10_TOGN	UART2_TXD	TIM2_CH2		OSC_OUT
4	7	4	VSS											
5	8	5	VCAP											
6	9	6	VDD											
7	10	7		PA3	TIM1_CH3N	PCA_CH2	SPI_NSS	RTC_1HZ	LPUART_RXD	PCA_ECI	VCMP0_OUT	TIM2_CH3	UART2_TXD	
11	11	8		PB5	TIM1_BKIN	PCA_CH4	SPI_CLK	I2C_SDA	UART1_RXD	TIM11_TOG	LVD_OUT	TIM2_CH1		X32K_IN
12	12	9		PB4	LPTIM_GATE	PCA_ECI	SPI_NSS	I2C_SCL	UART1_TXD	TIM11_TOGN				X32K_OUT
20	13	10		PC3	TIM1_CH3	TIM1_CH1N		I2C_SDA	UART2_TXD	PCA_CH1	1- WIRE	TIM2_CH3		AIN1
21	14	11		PC4	TIM1_CH4	TIM1_CH2N		I2C_SCL	UART2_RXD	PCA_CH0	CLK_MCO	TIM2_CH4		AIN2
22	15	12		PC5	TIM1_BKIN	PCA_CH0	SPI_CLK		LPUART_TXD	TIM11_GATE	LVD_OUT	TIM2_CH1		VCMPIN1
23	16	13		PC6	TIM1_CH1	PCA_CH3	SPI_MOSI		LPUART_RXD	TIM11_EXT	CLK_MCO	TIM2_CH4		AIN0
24	17	14	SWDIO	PC7	TIM1_CH2	PCA_CH4	SPI_MISO		UART2_RXD	LSI_OUT	LSE_OUT			
26	18	15	SWDCLK	PD1		PCA_ECI			UART2_TXD	HSE_OUT	VCMP0_OUT			
27	19	16		PD2	TIM1_CH2	PCA_CH2	SPI_MISO	RTC_1HZ	LPUART_TXD	LPTIM_TOG	1- WIRE	TIM2_CH3		AIN3/ VCMPIN0
28	20	17		PD3	TIM1_CH3N	PCA_CH1	SPI_MOSI	LSE_OUT	UART1_RXD	LPTIM_TOGN		TIM2_CH2		AIN4
8				PA4	TIM1_CH2N		SPI_CLK	I2C_SDA	UART1_RXD	TIM10_TOG	UART2_RXD			AIN14
9				PB7	TIM1_CH3N	PCA_CH2	SPI_NSS	RTC_1HZ	LPUART_RXD	PCA_ECI	VCMP0_OUT	TIM2_CH3		AIN8
10				PB6	TIM1_CH1N	PCA_CH4	SPI_MISO	I2C_SCL	UART2_TXD	TIM10_GATE	UART1_TXD	TIM2_CH4		AIN9
13				PB3	TIM1_CH2	PCA_CH3	SPI_MOSI	I2C_SDA	UART2_RXD	LPTIM_EXT	UART1_RXD	TIM2_CH2		AIN10
14				PB2	TIM1_CH3N	PCA_CH1	SPI_MOSI	LSE_OUT	UART1_RXD	LPTIM_TOGN		TIM2_CH2		AIN11
15				PB1	TIM1_CH1	PCA_CH0	RTC_1HZ	TIM10_TOG	UART1_TXD	TIM10_EXT	BEEP	TIM2_CH1	TIM1_CH2N	AIN12
16				PB0	TIM1_CH3	TIM1_CH1N		I2C_SDA	UART2_TXD	PCA_CH1	1- WIRE	TIM2_CH3		AIN13
17				PC0	TIM1_CH3		SPI_NSS	I2C_SCL	UART1_TXD	TIM10_TOGN	UART2_TXD	TIM2_CH2	TIM1_CH1N	AIN15
18				PC1	TIM1_CH1	PCA_CH3	SPI_MOSI		LPUART_RXD	TIM11_EXT	CLK_MCO	TIM2_CH4	TIM1_CH2N	
19				PC2	TIM1_CH2	PCA_CH2	SPI_MISO	RTC_1HZ	LPUART_TXD	LPTIM_TOG	1- WIRE	TIM2_CH3	TIM1_CH3N	
25				PD0	TIM1_BKIN	PCA_CH0	SPI_CLK		LPUART_TXD	TIM11_GATE	LVD_OUT	TIM2_CH1		
32				PD7	TIM1_CH4	TIM1_CH2N	I2C_SCL		UART2_RXD	PCA_CH0	CLK_MCO	TIM2_CH4		

Tab 3.4- 2 TSSOP20,QFN20,LQFP32/QFN32 pins

Pin			Name	Type	Function
LQFP32, QFN32	TSSOP20	QFN20			
29	1	18	PD4	PD4	PD4 GPIO
				TIM1_CH1	TIM1 PWM output 1
				PCA_CH0	PCA Input capture/Output compare 0
				RTC_1HZ	RTC 1HZ output
				TIM10_TOG	TIM10 Toggle output
				UART1_TX	UART1 TX
				TIM10_EXT	TIM10 External pulse
				BEEP	Buzzer output
				TIM2_CH1	TIM2 Input capture/Output compare 1
				VCMPIN2	VCMP input channel 2
30	2	19	PD5	PD5	PD5 GPIO
				TIM1_CH1N	TIM1 PWM output 1 Inverting
				PCA_CH4	PCA Input capture/Output compare 4
				SPI_MISO	SPI module host input slave output signal
				I2C_SCL	I2C clock
				UART2_TX	UART2_TX
				TIM10_GATE	TIM10 gating
				UART1_TX	UART1 TX
				TIM2_CH4	TIM2 Input capture/Output compare 4
				AIN5	ADC Analog input channel 5
31	3	20	PD6	PD6	PD6 GPIO
				TIM1_CH2	TIM1 PWM output 2
				PCA_CH3	PCA Input capture/Output compare 3
				SPI_MOSI	SPI module host output slave input signal
				I2C_SDA	I2C data
				UART2_RX	UART2 RX
				LPTIM_EXT	LPTIM External pulse input
				UART1_RX	UART1 RX
				TIM2_CH2	TIM2 Input capture/Output compare 2
				AIN6	ADC Analog input channel 6
1	4	1	NRST	NRST	Reset input port, low valid, chip reset
2	5	2	PA1	OSC_IN	External clock source input
				PA1	PA1 GPIO
				TIM1_CH2N	TIM1 PWM output 2 Inverting
				SPI_CLK	SPI Module clock signal
				I2C_SDA	I2C data
				UART1_RX	UART1 RX

Pin			Name	Type	Function
LQFP32, QFN32	TSSOP20	QFN20			
				TIM10_TOG	TIM10 Toggle output
				UART2_RX	UART2 RX
3	6	3	PA2	OSC_OUT	External clock source output
				PA2	PA2 GPIO
				TIM1_CH3	TIM1 PWM output 3
				SPI_NSS	SPI module slave chip selects signals
				I2C_SCL	I2C clock
				UART1_TX	UART1 TX
				TIM10_TOGN	TIM10 Toggle inverting output
				UART2_TX	UART2 TX
				TIM2_CH2	TIM2 Input capture/Output compare 2
4	7	4	VSS	GND	Ground
5	8	5	VCAP	Power	LDO kernel power supply (internal circuit use, external capacitor)
6	9	6	VDD	Power	power
7	10	7	PA3	PA3	PA3 GPIO
				TIM1_CH3N	TIM1 PWM output 3 Inverting
				PCA_CH2	PCA Input capture/Output compare 2
				SPI_NSS	SPI module slave chip selects signals
				RTC_1HZ	RTC 1HZ output
				LPUART_RX	LPUART RX
				PCA_ECI	PCA External clock
				VCMP0_OUT	Voltage comparator 0 output
				TIM2_CH3	TIM2 Input capture/Output compare 3
8			PA4	AIN14	ADC Analog input channel 14
				PA4	PA4 GPIO
				TIM1_CH2N	TIM1 PWM output 2 Inverting
				SPI_CLK	SPI Module clock signal
				I2C_SDA	I2C data
				UART1_RX	UART1 RX
				TIM10_TOG	TIM10 Toggle output
				UART2_RX	UART2 RX
9			PB7	PB7	PB7 GPIO
				TIM1_CH3N	TIM1 PWM output 3 Inverting
				PCA_CH2	PCA Input capture/Output compare 2
				SPI_NSS	SPI module slave chip selects signals
				RTC_1HZ	RTC 1HZ output
				LPUART_RX	LPUART RX
				PCA_ECI	PCA External clock

Pin			Name	Type	Function
LQFP32, QFN32	TSSOP20	QFN20			
				VC0_OUT	Voltage comparator 0 output
				TIM2_CH3	TIM2 Input capture/Output compare 3
				AIN8	ADC Analog input channel 8
10			PB6	PB6	PB6 GPIO
				TIM1_CH1N	TIM1 PWM output 1 Inverting
				PCA_CH4	PCA Input capture/Output compare 4
				SPI_MISO	SPI module host input slave output signal
				I2C_SCL	I2C clock
				UART2_TX	UART2_TX
				TIM10_GATE	TIM10 gating
				UART1_TX	UART1 TX
				TIM2_CH4	TIM2 Input capture/Output compare 4
				AIN9	ADC Analog input channel 9
11	11	8	PB5	X32K_IN	External 32K Clock source input
				PB5	PB5 GPIO
				TIM1_BKIN	TIM1 Brake signal input
				PCA_CH4	PCA Input capture/Output compare 4
				SPI_CLK	SPI Module clock signal
				I2C_SDA	I2C data
				UART1_RX	UART1 RX
				TIM11_TOG	TIM11 Toggle output
				LVD_OUT	LVD comparator output
				TIM2_CH1	TIM2 Input capture/Output compare 1
12	12	9	PB4	X32K_OUT	External 32K Clock source output
				PB4	PB4 GPIO
				LPTIM_GATE	LPTIM gating
				PCA_ECI	PCA External clock
				SPI_NSS	SPI module slave chip selects signals
				I2C_SCL	I2C clock
				UART1_TX	UART1 TX
				TIM11_TOGN	TIM11 Toggle inverting output
13			PB3	PB3	PB3 GPIO
				TIM1_CH2	TIM1 PWM output 2
				PCA_CH3	PCA Input capture/Output compare 3
				I2C_SDA	I2C data
				SPI_MOSI	SPI module host output slave input signal
				UART2_RXD	UART2 RXD
				LPTIM_EXT	LPTIM External pulse input
				UART1_RXD	UART1 RXD

Pin			Name	Type	Function
LQFP32, QFN32	TSSOP20	QFN20			
				TIM2_CH2	TIM2 Input capture/Output compare 2
				AIN10	ADC Analog input channel 10
14			PB2	PB2	PB2 GPIO
				TIM1_CH3N	TIM1 PWM output 3 Inverting
				PCA_CH1	PCA Input capture/Output compare 1
				SPI_MOSI	SPI module host output slave input signal
				LSE_OUT	External high frequency crystal output
				UART1_RX	UART1 RX
				LPTIM_TOGN	LPTIM Toggle inverting output
				TIM2_CH2	TIM2 Input capture/Output compare 2
				AIN11	ADC Analog input channel 11
15			PB1	PB1	PB1 GPIO
				TIM1_CH1	TIM1 PWM output 1
				PCA_CH0	PCA Input capture/Output compare 0
				RTC_1HZ	RTC 1HZ output
				TIM10_TOG	TIM10 Toggle output
				UART1_TXD	UART1 TXD
				TIM10_EXT	TIM10 External pulse
				BEEP	Buzzer output
				TIM2_CH1	TIM2 Input capture/Output compare 1
				VCIN12	VC input channel 12
				TIM1_CH2N	TIM1 PWM output 2 Inverting
16			PB0	PB0	PB0 GPIO
				TIM1_CH3	TIM1 PWM output 3
				TIM1_CH1N	TIM1 PWM output 1 Inverting
				I2C_SDA	I2C data
				UART2_TX	UART2 TX
				PCA_CH1	PCA Input capture/Output compare 1
				1- WIRE	1- wire Input/output
				TIM2_CH3	TIM2 Input capture/Output compare 3
				AIN13	ADC Analog input channel 13
17			PC0	PC0	PC0 GPIO
				TIM1_CH3	TIM1 PWM output 3
				SPI_NSS	SPI module slave chip selects signals
				I2C_SCL	I2C clock
				UART1_TXD	UART1 TXD
				TIM10_TOGN	TIM10 Toggle inverting output
				UART2_TXD	UART2 TXD
				TIM2_CH2	TIM2 Input capture/Output compare 2

Pin			Name	Type	Function
LQFP32, QFN32	TSSOP20	QFN20			
				TIM1_CH1N	TIM1 PWM output 1 Inverting
				AIN15	ADC Analog input channel 15
18			PC1	PC1	PC1 GPIO
				TIM1_CH1	TIM1 PWM output 1
				PCA_CH3	PCA Input capture/Output compare 3
				SPI_MOSI	SPI module host output slave input signal
				LPUART_RX	LPUART RX
				TIM11_EXT	TIM11 External pulse input
				CLK_MCO	CPU Clock output
				TIM2_CH4	TIM2 Input capture/Output compare 4
				TIM1_CH2N	TIM1 PWM output 2 Inverting
18			PC2	PC2	PC2 GPIO
				TIM1_CH2	TIM1 PWM output 2
				PCA_CH2	PCA Input capture/Output compare 2
				SPI_MISO	SPI module host input slave output signal
				RTC_1HZ	RTC 1HZ output
				LPUART_TX	LPUART TX
				LPTIM_TOG	LPTIM Toggle output
				1- WIRE	1- wire Input/output
				TIM2_CH3	TIM2 Input capture/Output compare 3
				TIM2_CH3N	TIM1 PWM output 3 Inverting
20	13	10	PC3	PC3	PC3 GPIO
				TIM1_CH3	TIM1 PWM output 3
				TIM1_CH1N	TIM1 PWM output 1 Inverting
				I2C_SDA	I2C data
				UART2_TX	UART2 TX
				PCA_CH1	PCA Input capture/Output compare 1
				1- WIRE	1- wire Input/output
				TIM2_CH3	TIM2 Input capture/Output compare 3
				AIN1	ADC Analog input channel 1
21	14	11	PC4	PC4	PC4 GPIO
				TIM1_CH4	TIM1 PWM output 4
				TIM1_CH2N	TIM1 PWM output 2 Inverting
				I2C_SCL	I2C clock
				UART2_RX	UART2 RX
				PCA_CH0	PCA Input capture/Output compare 0
				CLK_MCO	CPU Clock output
				TIM2_CH4	TIM2 Input capture/Output compare 4

Pin			Name	Type	Function
LQFP32, QFN32	TSSOP20	QFN20			
				AIN2	ADC Analog input channel 2
22	15	12	PC5	PC5	PC5 GPIO
				TIM1_BKIN	TIM1 Brake signal input
				PCA_CH0	PCA Input capture/Output compare 0
				SPI_CLK	SPI Module clock signal
			PC5	LPUART_TX	LPUART TX
				TIM11_GATE	TIM11 gating
				LVD_OUT	Low voltage detection comparator output
				TIM2_CH1	TIM2 Input capture/Output compare 1
				VCMPIN1	Analog input
23	16	13	PC6	PC6	PC6 GPIO
				TIM1_CH1	TIM1 PWM output 1
				PCA_CH3	PCA Input capture/Output compare 3
				SPI_MOSI	SPI module host output slave input signal
			PC6	LPUART_RX	LPUART RX
				TIM11_EXT	TIM11 External pulse input
				CLK_MCO	CPU Clock output
				TIM2_CH4	TIM2 Input capture/Output compare 4
				AIN0	ADC Analog input channel 0
24	17	14	PC7	SWDIO	SWD IO
				PC7	PC7 GPIO
				TIM1_CH2	TIM1 PWM output 2
				PCA_CH4	PCA Input capture/Output compare 4
				SPI_MISO	SPI module host input slave output signal
			PC7	UART2_RX	UART2 RX
				LSI_OUT	Internal low frequency RC clock 38.4KHZ output
				X32K_OUT	External low frequency crystal output
25			PD0	PC0	PC0 GPIO
				TIM1_BKIN	TIM1 Brake signal input
				PCA_CH0	PCA Input capture/Output compare 0
				SPI_CLK	SPI Module clock signal
				LPUART_TXD	LPUART TXD
				TIM11_GATE	TIM11 gating
				LVD_OUT	Low voltage detection comparator output
				TIM2_CH1	TIM2 Input capture/Output compare 1
26	18	15	PD1	SWDCLK	SWD clock
				PD1	PD1 GPIO
				PCA_ECI	PCA External clock

Pin			Name	Type	Function
LQFP32, QFN32	TSSOP20	QFN20			
				UART2_TX	UART2 TX
				HSE_OUT	Internal high frequency RC clock 24MHZ output
				VCMP0_OUT	VCMP0 output
27	19	16	PD2	PD2	PD2 GPIO
				TIM1_CH2	TIM1 PWM output 2
				PCA_CH2	PCA Input capture/Output compare 2
				SPI_MISO	SPI module host input slave output signal
				RTC_1HZ	RTC 1HZ output
				LPUART_TX	LPUART TX
				LPTIM_TOG	LPTIM Toggle output
				1- WIRE	1- wire Input/output
				TIM2_CH3	TIM2 Input capture/Output compare 3
				VCMPIN0	VCMP input channel 0
				AIN3	ADC Analog input channel 3
28	20	17	PD3	PD3	PD3 GPIO
				TIM1_CH3N	TIM1 PWM output 3 Inverting
				PCA_CH1	PCA Input capture/Output compare 1
				SPI_MOSI	SPI module host output slave input signal
				LSE_OUT	External high frequency crystal output
				UART1_RX	UART1 RX
				LPTIM_TOGN	LPTIM Toggle inverting output
				TIM2_CH2	TIM2 Input capture/Output compare 2
				AIN4	ADC Analog input channel 4
29			PD4	PD4	PD4 GPIO
				TIM1_CH1	TIM1 PWM output 1
				PCA_CH0	PCA Input capture/Output compare 0
				RTC_1HZ	RTC 1HZ output
				TIM10_TOG	TIM10 Toggle output
				UART1_RX	UART1 RX
				TIM10_EXT	TIM10 External pulse
				BEEP	Buzzer output
				TIM2_CH1	TIM2 Input capture/Output compare 1
				VCIN2	VC input channel 2
30			PD5	PD5	PD5 GPIO
				TIM1_CH1N	TIM1 PWM output 1 Inverting
				PCA_CH4	PCA Input capture/Output compare 4
				SPI_MISO	SPI module host input slave output signal
				I2C_SCL	I2C clock

Pin			Name	Type	Function
LQFP32, QFN32	TSSOP20	QFN20			
				UART2_TX	UART2 TX
				TIM10_GATE	TIM10 gating
				UART1_TX	UART01 TX
				TIM2_CH4	TIM2 Input capture/Output compare 4
				AIN5	ADC Analog input channel5
31			PD6	PD6	PD6 GPIO
				TIM1_CH2	TIM1 PWM output 2
				PCA_CH3	PCA Input capture/Output compare 3
				SPI_MOSI	SPI module host output slave input signal
				I2C_SDA	I2C data
				UART2_RX	UART2 RX
				LPTIM_EXT	LPTIM External pulse input
				UART1_RX	UART1 RX
				AIN6	ADC Analog input channel 6
32			PD7	PD7	PD7 GPIO
				TIM1_CH4	TIM1 PWM output 4
				TIM1_CH2N	TIM1 PWM output 2 Inverting
				I2C_SCL	I2C clock
				UART2_RX	UART2 RX
				PCA_CH0	PCA Input capture/Output compare 0
				CLK_MCO	CPU Clock output
				TIM2_CH4	TIM2 Input capture/Output compare 4

Tab 3.4-3 **MG32L003xx Memory Map**

Bus	range	size	module
	0xE000_0000 - 0xE00F_FFFF	1MB	M0+ peripheral
	0x4003_0000 - 0xDFFF_FFFF		Reserve
AHB	0x4002_1000 - 0x4002_1FFF	1K	GPIOD
	0x4002_1000 - 0x4002_1BFF	1K	GPIOC
	0x4002_1000 - 0x4002_17FF	1K	GPIOB
	0x4002_1000 - 0x4002_13FF	1K	GPIOA
	0x4002_0C00 - 0x4002_0FFF	1K	Reserve
	0x4002_0800 - 0x4002_0BFF	1K	CRC16
	0x4002_0400 - 0x4002_07FF	1K	FMC
	0x4002_0000 - 0x4002_03FF	1K	RCC
	0x4000_5400 - 0x4001_FFFF		Reserve
APB	0x4000_5000 - 0x4000_53FF	1K	LPUART
	0x4000_4C00 - 0x4000_4FFF	1K	DEBUG
	0x4000_4800 - 0x4000_4BFF	1K	BEEP
	0x4000_4400 - 0x4000_47FF	1K	LPTIM
	0x4000_4000 - 0x4000_43FF	1K	LVD/VCMP
	0x4000_3C00 - 0x4000_3FFF	1K	TIM2
	0x4000_3800 - 0x4000_3BFF	1K	OWIER
	0x4000_3400 - 0x4000_37FF	1K	CLKTRIM
	0x4000_3000 - 0x4000_33FF	1K	RTC
	0x4000_2C00 - 0x4000_2FFF	1K	ADC
	0x4000_2800 - 0x4000_2BFF	1K	AWK
	0x4000_2400 - 0x4000_27FF	1K	IWDT
	0x4000_2000 - 0x4000_23FF	1K	WWDT
	0x4000_1C00 - 0x4000_1FFF	1K	SYSCON
	0x4000_1800 - 0x4000_1BFF	1K	TIM10/11
	0x4000_1400 - 0x4000_17FF	1K	PCA

	0x4000_1000 - 0x4000_13FF	1K	TIM1
	0x4000_0C00 - 0x4000_0FFF	1K	I2C
	0x4000_0800 - 0x4000_0BFF	1K	SPI
	0x4000_0400 - 0x4000_07FF	1K	UART2
	0x4000_0000 - 0x4000_03FF	1K	UART1
AHB	0x2000_1000 - 0x3FFF_FFFF		Reserve
	0x2000_0000 - 0x2000_0FFF	4K	SRAM
	0x1800_0100 - 0x1FFF_FFFF		Reserve
	0x1800_0000 - 0x1800_00FF	256	system configuration
	0x0800_0200 - 0x17FF_FFFF		Reserve
	0x0800_0000 - 0x0800_01FF	512	Byte option
	0x0001_0000 - 0x07FF_FFFF		Reserve
	0x0000_0000 - 0x0000_FFFF	64K	Main Flash Memory

4 Device description

4.1 Core with Embedded Flash and SRAM

The ARM ® Cortex™- M0+ is a new processor of ARM company, it provides a reliable platform for MCU to achieve high performance and low power consumption, and integrates rich IO and advanced interrupt control system.

The MG32L003xx embedded 64KB Flash memory for storing user application code and data. The core can operate up to 24Mhz, Flash does not need wait cycles.

The MG32L003xx embeds 4KB of SRAM memory

4.2 CRC Calculation unit

The CRC calculation unit uses a fixed polynomial generator (according to the polynomial F(x) = X16 + X12 + X5 + 1 given in ISO/IEC13239). used to generate CRC codes for 32- bit data. In many applications, CRC technology is used to verify the integrity of data transmission and storage, it provides a means to verify storage errors in flash memory, calculate the signature of the software in real time, and compare the signatures generated during software execution.

4.3 Nested Vectored Interrupt Controller (NVIC)

The MG32L003 embeds a nested vectored interrupt controller(NVIC), capable of real- time control and interrupt processing.

- Up to 32 interrupt requests(IRQ)Input
- 4 interrupt priority levels
- Provide low- latency interrupt handling.
- The entry address of the interrupt vector leads directly to the core.
- Tightly coupled NVIC interface.
- Early processing of interrupts.
- Handle late- arriving higher- level interrupts.

Tab 4.3-1 **Interrupt Controller**

External Interrupt	Address	Interrupt source	Name	Wake up from sleep	Wake up from deep sleep
0	0x0000 0040	GPIO_PA	GPIOA Interrupt	Yes	Yes
1	0x0000 0044	GPIO_PB	GPIOB Interrupt	Yes	Yes
2	0x0000 0048	GPIO_PC	GPIOC Interrupt	Yes	Yes
3	0x0000 004C	GPIO_PD	GPIOD Interrupt	Yes	Yes
4	0x0000 0050	Flash	Flash Interrupt	NO	NO
5	0x0000 0054	Reserve			
6	0x0000 0058	UART1	UART0 Interrupt	Yes	NO
7	0x0000 005C	UART2	UART1 Interrupt	Yes	NO
8	0x0000 0060	LPUART	LPUART Interrupt	Yes	Yes

9	0x0000 0064	Reserve			
10	0x0000 0068	SPI	SPI Interrupt	Yes	NO
11	0x0000 006C	Reserve			

External Interrupt	Address	Interrupt source	Name	Wake up from sleep	Wake up from deep sleep
12	0x0000 0070	I2C	I2C Interrupt	Yes	NO
13	0x0000 006C	Reserve			
14	0x0000 0078	TIM10	TIM10 Interrupt	Yes	NO
15	0x0000 007C	TIM11	TIM11 Interrupt	Yes	NO
16	0x0000 0080	LPTIM	LPTIM Interrupt	Yes	Yes
17	0x0000 007C	Reserve			
18	0x0000 0088	TIM1	TIM1 Interrupt	Yes	NO
19	0x0000 008C	TIM2	TIM2 Interrupt	Yes	NO
20	0x0000 0088	Reserve			
21	0x0000 0094	PCA	PCA Interrupt	Yes	NO
22	0x0000 0098	WWDG	WWDG Interrupt	Yes	NO
23	0x0000 009C	IWDG	IWDG Interrupt	Yes	Yes
24	0x0000 00A0	ADC	ADC Interrupt	Yes	NO
25	0x0000 00A4	LVD	LVD Interrupt	Yes	Yes
26	0x0000 00A8	VCMP	VCMP Interrupt	Yes	Yes
27	0x0000 00A4	Reserve			
28	0x0000 00B0	AWK	AWK Interrupt	Yes	Yes
29	0x0000 00B4	OWIRE	1WIRE Interrupt	Yes	NO
30	0x0000 00B8	RTC	RTC Interrupt	Yes	Yes
31	0x0000 00BC	CLKTRIM	CLKTRIM Interrupt	Yes	Yes

4.4 System Reset

The MG32L003 has 9 reset sources, each reset source can trigger the system reset which reset most of the registers, the program counter will point to the reset address(0x0000 0000)

- power- on reset (POR) and power- down reset (PDR)
- External Reset Pin reset
- Independent watchdog reset
- Window watchdog reset
- Software reset
- Low voltage Detect(LVD)Reset

- Lockout Reset
- CPURST Reset
- MCURST Reset

4.5 Clock

- 4M~24MHz external high- speed crystal oscillator (HSE)
- 32.768KHz external low- speed crystal oscillator(LSE)
- 4M~24MHz internal high speed clock (HSI)
- 32.768KHz/38.4KHz internal low speed clock (LSI)

Internal RC Frequency deviation over full voltage and full temperature range<±2.5%.

System clock selection is performed on startup, however the internal high speed oscillator is selected as default CPU clock on reset.

4.6 Power supply scheme

VDD=2.5V~5.5V

External power supplies all IO and internal voltage regulators provided externally through VDD pin.

4.7 Power supply supervisors(POR/BOR/LVD)

The MG32L003xx integrates power- on reset (POR) and power- down reset (BOR) detection circuits, which are always on to ensure proper operation above a threshold of 2.5V. If the power supply is lower than the threshold VPOR/VBOR, the system is always in reset state, without the need for an external reset circuit. The product also integrates a programmable voltage detector (LVD) for monitoring power supply voltage. Can generate interrupt or reset according to rising/falling edge. With hardware delay circuit and configurable software antishake function.

4.8 Voltage regulator (LDO)

The voltage regulator powers the internal circuitry and the VCAP capacitor is connected externally.

4.9 Power mode

The MG32L003 supports 3 working modes：

1 Run mode: The CPU core and peripheral modules continue to operate.
2 Sleep mode: In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
3 Deep- sleep mode: The CPU core is halt, the main clock is turned off, and the low- power modules continue to operate.

In sleep mode, the core clock is turned off, and other peripherals can still operate, and the core can be woken up through an interrupt. In deep sleep mode, the main clock is turned off, and most modules stop operate. The system operate on the built- in 38.4KHz/32.768KHz low- speed clock, which can be interrupted by RTC, AWK interrupt or external interrupt to wake up the chip device. In the normal operate mode, you can choose to work in frequency division mode or turn off the clock of some unused peripherals to achieve flexible switching between power consumption and performance.

4.10 Real Time Clock （RTC）

The real- time clock provides a set of continuous counting counters, which can be configured by software to provide clock calendar functions, and can also provide warning interrupts and periodic interrupts.

4.11 Timers and Watchdogs

The MG32L003xx product includes 1 advanced timer,1 general purpose timer,1 programmable counter,2 basic timer,1 low power timer,1 window watchdog,1 stand- alone watchdog and 1 systick(SysTick)Timer.

Tab 4.11-1 **Timers and Watchdogs**

Timer Type	Name	Counter	Prescaler	Counting direction	Complementary output	PWM	Capture Compare channel
Advanced	TIM1	16 bits	1/2/4/8/16/ 64/256/1024	increase , decrease, increase/decrease	3pairs	Yes	4
Universal	TIM2	16 bits	1/2/4/8/16/ 64/256/1024	increase , decrease, increase/decrease	No	Yes	4
PCA	PCA	16 bits	2/4/8/16/32	increase	No	Yes	5
low power consumption	LPTIM	16 bits	No	increase	No	No	No
Basic	TIM10	16/32 bits	1/2/4/8/16/32/64/128	increase	No	No	No
	TIM11	16/32 bits	1/2/4/8/16/32/64/128	increase	No	No	No

4.11.1 Advanced Timer（TIM1）

1 advanced control timer(TIM1) can be seen as a three- phase PWM generator assigned to 6 channels, It has a complementary PWM output with dead- time insertion and can also be used as a complete general-purpose timer. Four independent channels can be used for:

- Input capture
- Output comparison
- Generate PWM (edge or center aligned)
- Single- shot pulse output TIM1 the same function as TIM2 timer when configured as 16- bit general- purpose timer. It has full modulation capability(0~100%)when configured as 16- bit PWM generator.

In debug mode, the timers can be frozen and the PWM outputs disabled, cutting off the power switches controlled by these outputs. Most functions of the advanced timer are the same as the general timer, and the same internal structure, so it can work together with the TIM timer through the timer link function to provide synchronization or event link.

4.11.2 General purpose timer（TIM2）

The MG32L003xx has a 16- bit autoload up/down counter, a 16- bit prescaler and 4 independent channels, each channel can be used for input capture, output compare,PWM and single- pulse mode output, they can also work with advanced control timers through the timer link function, providing Synchronization or event chaining functionality. In debug mode, the counter can be frozen and any general purpose timer can be used to generate PWM outputs

4.11.3 Programmable Counter Array(PCA)

PCA (Programmable Counter Array) supports up to five 16- bit capture/comparison modules. The timing/counters can be used as a general- purpose clock counting/event counters for capture/comparison functions. Each channel of the PCA can be independently programmed to provide input capture/output compare or pulse width modulation.

4.11.4 Low Power Timer(LPTIM)

The low power timers are 16- bit selectable . After the system clock is turned off, it can still be clocked by LSI or LSE, and the system can be woken up in low power mode by interrupt.

4.11.5 Basic timer(TIM10/11)

The basic timer consists of 2 16/32 bit selectable timers TIM10/11. TIM10/11 have exactly the same function, they are all synchronous timer, you can choose to work in heavy load mode or non- heavy load mode. TIM10/11 can count external pulses or implement system timer.

4.11.6 Independent Watchdog(IWDG)

The independent watchdog is a 20- bit down counter. It is clocked by an internal independent LSI; since the internal LSI is independent of the main clock, it can operate in shutdown and standby modes. It can be used either as a watchdog to reset the device if the CPU runs away, or as a free- running timer to provide time- out management for the application. In debug mode, the counters can be frozen.

4.11.7 System Watchdog(WWDG)

The system window watchdog is based on a 8- bit down- counter, supporting a 20- bit prescaler, which is driven by the APB clock(PCLK) provides the action clock. It can be used as a watchdog to reset the device in case of system problems, it has an early warning interrupt function, and the counters can be frozen in debug mode.

4.11.8 SysTick timer(SysTick)

The systick timer is dedicated to real- time operating systems, but can also be used as a standard down counter. It has the following properties:

- 24- bit down counter
- Auto- reload function
- Generate a maskable system interrupt when the counter counts to 0
- Programmable clock source(HCLK or HCLK/4)

4.12 I2C Bus

I²C bus interfaces can operate in multimaster and slave modes. They can support standard, fast and high speed modes, the maximum data transmission speed can reach 1Mbps.

4.13 Universal Asynchronous Transceiver (UART1/UART2)

The MG32L003 has 2 Universal Asynchronous Transceivers for asynchronous communication.

4.14 Low Power Universal Asynchronous Transceiver (LPUART)

The MG32L003 has 1 Universal Asynchronous Transceiver that can work in low power mode, providing asynchronous communication.

4.15 Serial Peripheral Interface(SPI)

The SPI is capable of communicating at rates up to 12Mb/s in full- duplex and simplex communication modes, master and slave modes.

4.16 General purpose input and output (GPIO)

Each GPIO can be software configured as a push- pull or open- drain output, as an input with or without pull- up/pull- down, or as an alternate peripheral function. Each port is controlled by an independent control register bit. Supports edge- triggered interrupts and level- triggered interrupts, can wake up MCU from various low power consumption modes to work mode, support Schmitt trigger input filtering function. The output drive capability is configurable, and the maximum drive current is 12mA. Generic IO supports external asynchronous interrupts.

4.17 Analog to Digital Converter(ADC)

The sampling rate of a 12- bit sequential approximation ADC can reach 1Msps when operating under a 16MHz ADC clock. Power supply can be selected as reference voltage. The 20 Pin package contains 7 external channels, and the 32 Pin package contains 16 external channels.Can achieve single, scan, cycle conversion. Automatically converts on a selected set of analog inputs in scan/loop mode.

- Input voltage range:0 to VCC
- Conversion cycles:16/20 clock cycles
- Support trigger ADC from external terminals, internal TIM1,TIM2,TIM10/11, voltage comparator, etc
- End of Conversion(EOC)Interrupt

4.18 Voltage Comparator(VCMP)

Total 3 configurable positive/negative external input channels;1 internal bandgap reference voltage (MG32L003F8 = 2.5V , MG32L003K8 = 1.57V) . VCMP output available for timers TIM1,TIM10/11,LPTIM and PCA Capture, Gating, External Count usage. Asynchronous interrupt can be generated according to rising/falling edge, wake up MCU from low power mode.

4.19 Buzzer(BEEP)

A 1/2/4KHz BEEP signal can be generated on the BEEP pin, which is used to drive the external buzzer. 2 basic timers TIM10/11 and 1 LPTIM can function as multiplexed outputs to provide programmable clock source for buzzers Frequency, can support complementary output.

4.20 Automatic wake-up timer(AWK)

AWK is used to provide an internal wake- up time reference when MCU enters low power mode. The time base is clocked by the internal low speed RC oscillator clock(LSI) or by the prescaled HSE crystal clock.

4.21 Clock Trim/Monitoring Module(CLKTRIM)

The MG32L003xx embeds clock calibration circuit, can be used to calibrate the internal RC clock through the external precise crystal oscillator clock, or use the internal RC clock to detect whether the external crystal oscillator clock works fine.

4.22 Unique ID (UID)

The MG32L003xx are shipped with a unique 16 byte device identification number.(0x180000F0- 0x180000FF)

4.23 Embedded Debug System

The embedded debugging solution provides a full- featured real- time debugger, which cooperates with standard mature Keil/IAR and other debugging and development software.

Supports 4 hard breakpoints and multiple soft breakpoints.

4.24 Embedded Debug (DBG)

An encrypted embedded debugging solution that provides a full- featured real- time debugger.

5 Electrical Characteristics

5.1 Test conditions

All voltages are referenced to VSS unless otherwise specified.

5.1.1 Minimum and maximum

Unless otherwise specified, the minimum and maximum values tested at 25°C ambient temperature and VDD=3.3V conditions. The characteristic values in the table are based on design simulation, process characteristics, not tested in mass production.

5.2 Typical value

Unless otherwise specified, typical values are based on 25°C ambient temperature and VDD=3.3V conditions.

5.3 Absolute maximum ratings

Permanent damage to the product may result if the load applied to the product exceeds the absolute maximum. The maximum load that can be tolerated here does not mean that the functional operation of the product is correct under this condition, and the reliability of the product will be affected if the product works under the maximum value for a long time.

Tab 5.3-1 **Absolute maximum ratings**

Symbol	Parameter	Min	Typical	Max	Unit
VDD	voltage	2.5		5.5	V
VIO	pin voltage	-0.3		VDD+0.3	V
$T_{storage}$	storage temperature	-40	25	150	℃
$T_{operation}$	Operating temperature	-40	25	85	℃
f_{CPU}	CPU Operating frequency	32.768K	4M	24M	Hz
$V_{ESD,HBM}$		8			KV
$T_{ESD,CDM}$		2			KV
LU	TA = +85 °C conforming to JESD78A	±300mA			

[1] Temperature test：- 40°C tests only in laboratory and Production Quality Qualification

[2] Frequency Test：CP test at 24MHz

5.4 Recommended Operating Conditions

5.4.1 Recommended Operating Conditions

Tab 5.4-1 **Recommended Operating Conditions**

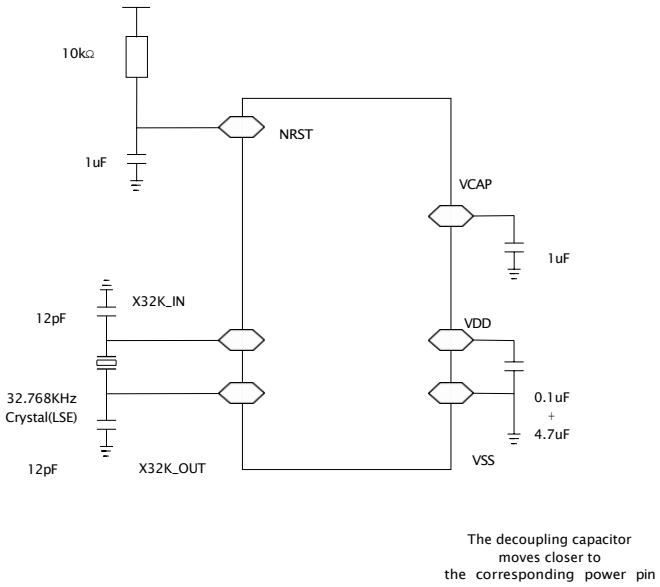
Parameter	Symbol	Min	Typical	Max	reference
Voltage	VDD	2.5	5.5	V	
VCAP Capacitance	C_S	0.47	2.2	μF	1.0μF
Operating temperature	T_{OP}	-40	85	℃	

[1] Recommended working conditions are the conditions to ensure the normal operation of the chip device. All specification values for electrical characteristics are guaranteed within the range of recommended operating conditions. Use outside this condition may affect product reliability

[2]Our company does not make any guarantees for the use of items, conditions of use, or logical combinations that are not described in this data sheet

5.5 Typical application block diagram

Fig 5.5-1 **Typical application block diagram**



5.6 DC supply characteristics

5.6.1 DC supply characteristics

Tab 5.6-1 **DC supply characteristics**

Symbol	parameter	Condition			Typical	Max	Unit
I_{DD}(active mode)	Peripheral clock on, code runs from Flash	VDD=3.3V	HSI clock source	4M	468	542	μA
				8M	839	966	
				16M	1575	1811	
				24M	2298	2549	
	Peripheral clock off, code runs from Flash	VDD=3.3V	HSI clock source	4M	397	698	μA
				8M	696	1246	
				16M	1291	1442	
				24M	1871	2377	
	Peripheral clock on, code runs from Flash	VDD=3.3V	LSE 32.768KHz clock source	Ta=-40 to 25°C	34	46	μA
				Ta=85°C	41	54	
	Peripheral clock off, code runs from Flash	VDD=3.3V	LSE 32.768KHz clock source	Ta=-40 to 25°C	34	51	μA
				Ta=85°C	44	56	
	Peripheral clock on, code runs from Flash	VDD=3.3V	HSE clock source	Ta=-40 to 25°C	2556	2960	μA
	Peripheral clock off, code runs from Flash	VDD=3.3V	HSE clock source	Ta=-40 to 25°C	2145	2725	μA
I_{DD}(sleep mode)	Peripheral clock on	VDD=3.3V	HSI clock source	4M	181	211	μA
				8M	282	324	
				16M	486	537	
				24M	689	813	
	Peripheral clock off	VDD=3.3V	HSI clock source	4M	122	147	μA
				8M	166	194	
				16M	252	296	
				24M	338	415	
	Peripheral clock on	VDD =3.3V	LSE 32.768KHz clock source	Ta=-40 to 25°C	26	41	μA
				Ta=85°C	32	44	
	Peripheral clock off	VDD =3.3V	LSE 32.768KHz clock source	Ta=-40 to 25°C	25	40	μA
				Ta=85°C	32	48	
	Peripheral clock on	VDD =3.3V	HSE 32.768KHz clock source	Ta=-40 to 25°C	884	1030	μA
	Peripheral clock off	VDD =3.3V	HSE 32.768KHz clock source	Ta=-40 to 25°C	534	643	μA
I_{DD}(Deep sleep mode)	Peripheral clock off, exclude AWK, IWDG, LTIM, RTC	VDD =3.3V	LSE 32.768KHz clock source	Ta=-40 to 25°C	1.20	1.28	μA
				Ta=85°C	3.04	3.44	
	Peripheral clock off, exclude IWDG	VDD =3.3V	LSE 32.768KHz clock source	Ta=-40 to 25°C	1.20	1.33	μA
				Ta=85°C	4.53	4.93	

symbol	parameter	Condition			Typical	Max	Unit
	Peripheral clock off, exclude LPTIM	VDD =3.3V	LSE 32.768KHz clock source	Ta=-40 to 25°C	1.18	1.31	μA
				Ta=85°C	4.46	4.85	
	Peripheral clock off, exclude RTC	VDD =3.3V	LSE 32.768KHz clock source	Ta=-40 to 25°C	1.19	1.59	μA
				Ta=85°C	6.74	7.98	
	Peripheral clock off	VDD =3.3V		Ta=-40 to 25°C	0.89	1.19	μA
				Ta=85°C	5.04	5.93	

[1] Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V.

[2] At LSE 32.768KHz, a 3MΩ resistor is required to connect the external crystal oscillator in parallel.

[3] Based on laboratory test results, not tested in production

5.6.2 Power-on/Power-down reset

Tab 5.6-2 **Power-on/Power-down reset**

Symbol	Parameter	Min	Typical	Max	Unit
V_{POR} V_{BOR}	POR voltage(power up) BOR voltage(brownout)	2.2	2.25	2.3	V

Note1: Guaranteed by design, not tested in production.

Note2: Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.7 AC supply current characteristics

5.7.1 AC supply current characteristics

Tab 5.7-1 **AC supply current characteristics**

Symbol	Parameter	Condition	Min	Max	Unit
V_{OH}	High level output source current	Source 4 mA, VDD = 3.3 V	VDD-0.2		V
		Source 6 mA, VDD = 3.3 V	VDD-0.3		
V_{OL}	Low level output sink current	sink 4 mA, VDD = 3.3 V		VSS+0.2	V
		sink 6 mA, VDD = 3.3 V		VSS+0.3	
V_{OHD}	High level output dual source current	Source 8 mA, VDD = 3.3 V	VDD-0.2		V
		Source 12 mA, VDD = 3.3 V	VDD-0.3		
V_{OLD}	Low level output dual current sink	sink 8 mA, VDD = 3.3 V		VSS+0.2	V
		sink 12 mA, VDD = 3.3 V		VSS+0.3	

Note1: Lab data, not tested in production.

Note2: Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.7.2 Port PA , PB , PC , PD

Tab 5.7-2 **Port PA , PB , PC , PD**

Symbol	Parameter	Condition	Min	Max	Typical	Unit
V_{IT+}	Positive Input Threshold Voltage	VDD=2.5	1.4			V
		VDD=3.3	1.8			V
		VDD=5.5	3			V
V_{IT-}	Reverse Input Threshold Voltage	VDD=2.5			0.9	V
		VDD=3.3			1.3	V
		VDD=5.5			2.4	V
V_{hys}	Input voltage hysteresis (VIT+ - VIT-)	VDD=2.5		0.5		V
		VDD=3.3		0.5		V
		VDD=5.5		0.6		V
$R_{pullhigh}$	Pull-up resistor	Pull-up enable	40	50	60	Kohm
C_{input}	input capacitance			5		pf

Note1: Lab data, not tested in production.

Note2: Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.7.3 Port characteristic - PA , PB , PC , PD

Tab 5.7-3 **Port characteristic - PA,PB,PC,PD**

Symbol	Parameter	Condition	VDD	Max	Unit
I_{lkg}	leakage current	V	2.5V / 3.6V	±50	nA

Note1: Lab data, not tested in production.

Note2: Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.7.4 Timer input sampling requirements

Tab 5.7-4 **Timer input sampling requirements**

Symbol	Parameter	Condition	Min	Max	Unit
T(int)	external interrupt	External trigger interrupt flag	30		ns
T(cap)	Timer capture time	TIM1/2 capture pulse width f_{system} =4MHz	0.5		μs
f_{EXT}	Timer clock frequency	TIM1/2/10/11 External clock input f_{system} =4MHz	0	$f_{TIMxCLK}/2$	MHz
$T_{(PCA)}$	PCA clock frequency	PCA External clock input f_{system} =4MHz	0	$f_{PCACLK}/2$	MHz

Note1: Lab data, not tested in production.

Note2: Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.7.5 Internal High Speed Oscillator (HSI)

Tab 5.7-5 **Internal High Speed Oscillator (HSI)**

Symbol	Parameter	Condition	Min	Typical	Max	Unit
F_{MCLK}	Internal Oscillator Frequency		4.0	16	24	MHz
T_{Mstart}	build time	F_{MCLK}=4MHz	2	2.4	4.7	μs
		F_{MCLK}=8MHz	1.15	1.47	3.01	μs
		F_{MCLK}=16MHz	1.04	1.31	2.74	μs
		F_{MCLK}=24MHz	1.1	1.30	2.71	μs
T_{MCLK}	current consumption	F_{MCLK}=4MHz	31	56	113	μA
		F_{MCLK}=8MHz	40	72	151	μA
		F_{MCLK}=16MHz	71	143	298	μA
		F_{MCLK}=24MHz	93	196	383	μA
DC_{MCLK}	duty cycle		45	50	55	%
D_{evM}	frequency deviation	VDD = 2.5V ~ 5.5V TAMP = -40°C ~ 85°C	-2.5	±1	+2.5	%
		VDD = 2.5V ~ 5.5V TAMP = -40°C ~ 50°C	-2.0	±1	+2.0	%

Note1: Lab data, not tested in production.

Note2: Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.7.6 Internal low-speed oscillator (LSI)

Tab 5.7-6 **Internal low-speed oscillator (LSI)**

Symbol	Parameter	Condition	Min	Typical	Max	Unit
F_{ACLK}	Internal Oscillator Frequency		37.8 32.21	38.4 32.766	38.7 33.26	KHz
T_{Astart}	build time		50	75	150	μs
I_{ACLK}	current consumption		0.2	0.25	0.35	μA
DC_{ACLK}	duty cycle		45	50	55	%
D_{evA}	frequency deviation	VDD = 2.5V ~ 5.5V TAMP = -40°C ~ 85°C	-2.0	±1	+2.0	%
		VDD = 2.5V ~ 5.5V TAMP = -40°C ~ 50°C	-1.5	±1	+1.5	%

Note1: Lab data, not tested in production.

Note2: Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.7.7 External low-speed crystal (LSE)

Tab 5.7-7 **External low-speed crystal (LSE)**

Symbol	Parameter	Condition	Min	Typical	Max	Unit
F_{SCLK}	Crystal frequency		32.75	32.768	32.78	KHz
ESR_{SCLK}	Equivalent resistance		40	65	85	KOhm
C_{SCLK}	Crystal external load			12[2]		pF
I_{dd}[1]	electric current	ESR=65kOhm C_{SCLK}=12pF	200	250	350	nA
DC_{SCLK}	duty cycle		40	50	60	%
T_{start}	build time	ESR=65kOhm C_{SCLK}=12pF 40%- 60% duty cycle		2		s

[1]. RCC_CR.DRV=0011, ESR=65K

[2] Lab data, not tested in production.

[3] Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.7.8 External High Speed Crystal (HSE)

Tab 5.7-8 **External High Speed Crystal (HSE)**

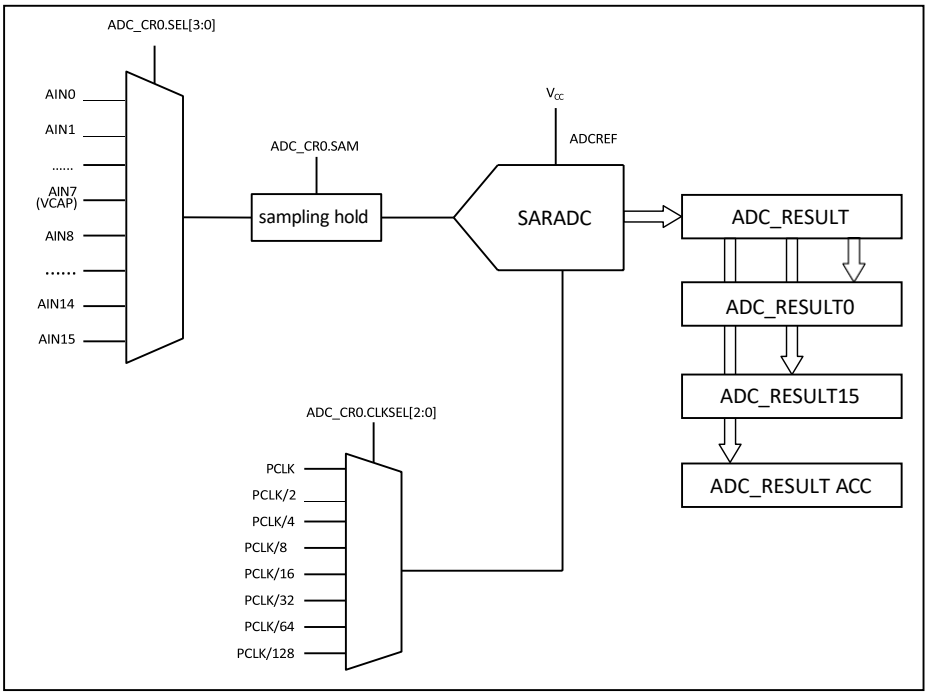
Symbol	Parameter	Condition	Min	Typical	Max	Unit
F_{FCLK}	Crystal frequency		4	16	24	MHz
ESR_{FCLK}	Equivalent resistance		30	60	1500	Ohm
C_{FCLK}	Crystal external load			12		pF
I_{dd}	electric current	24MHz Crystal ESR=30Ohm C_{FCLK}=12pF		300		μA
D_{CFCLK}	duty cycle		40	50	60	%
T_{start}	build time	4M~24MHz		250		μs

[1]. Lab data, not tested in production.

[2] Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.8 12bit A/D Converter

Fig 5.8-1 **12 bit A/D Converter**



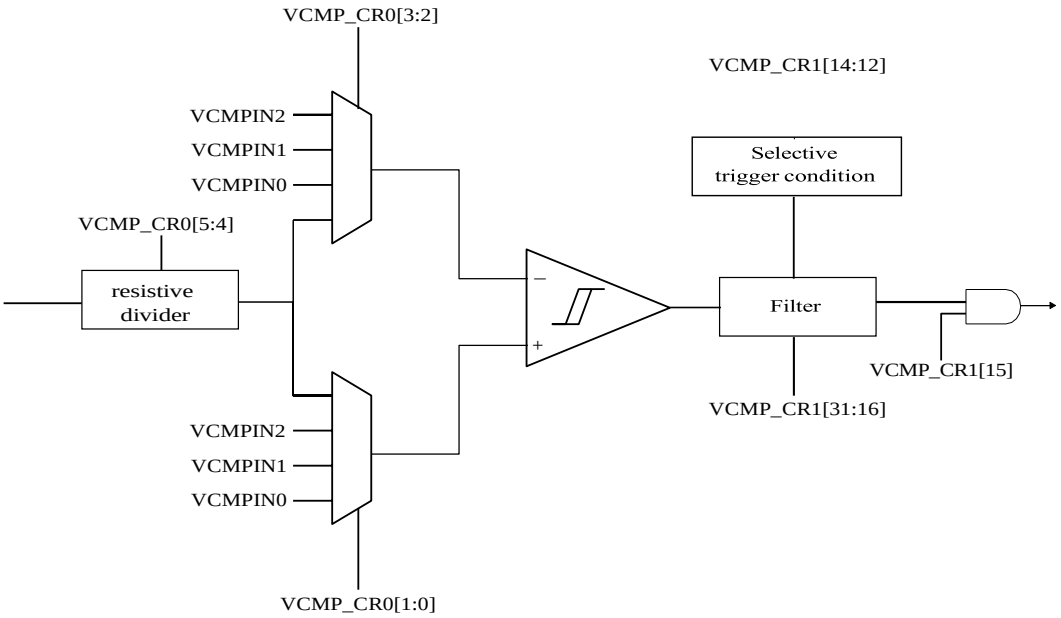
Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{ADCIN}	Input voltage range	single ended	0		VDD	V
V_{REF}	reference voltage			VDD		V
I_{ADC}	ADC current		0.65	0.9	1.23	mA
C_{ADCIN}	input resistance		3.5	4	4.5	pF
F_{ADCCLK}	Clock frequency		0.5	4	16	MHz
$T_{ADCSTART}$	Bias Current Settling Time		2	3	4	μs
$T_{ADCCONV}$	conversion time		16	16	20	cycle
ENOB	Effective Numbers of Bits		10	10.5	11	Bit
DNL	differential nonlinearity		-1.5	±1	1.5	LSB
INL	integral nonlinearity		-2	±1	2	LSB
E_o	bias error		-2	±1	2	LSB
E_g	gain error		-2	±1	2	LSB

[1]. Lab data, not tested in production.

[2] Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.9 Analog Voltage Comparator

Tab 5.9-1 **Analog Voltage Comparator**



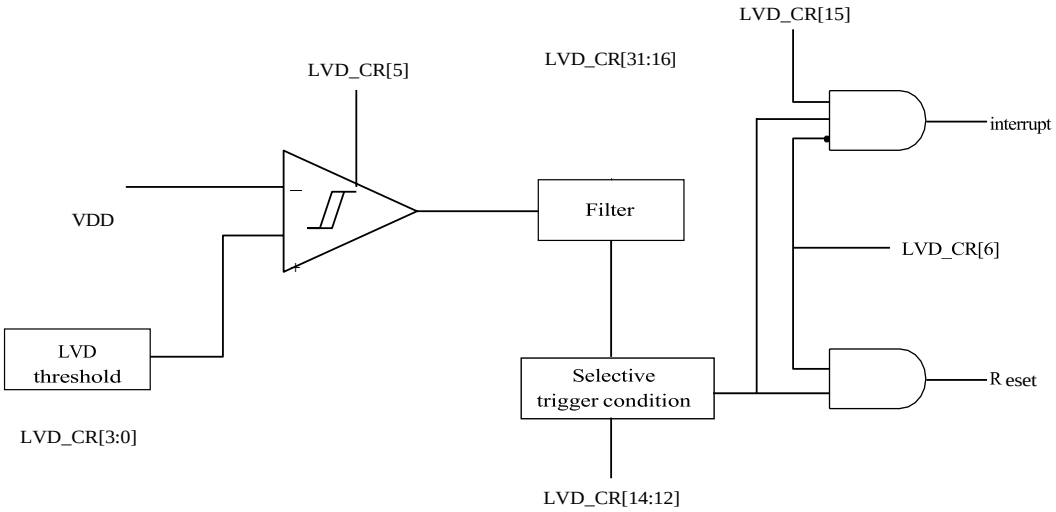
Symbol	Parameter	Min	Typical	Max	Unit
V_{in}	Input voltage range	0		5.5	V
V_{incom}	Input Common Mode Range	0		5.5	V
V_{offset}	input bias	-10	±5	+10	mV
I_{comp}	comparator current		12		μA
$T_{response}$	Comparator Response		5		μs

[1]. Lab data, not tested in production.

[2] Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.10 Low voltage detection characteristics

Fig 5.10-1 **Low voltage detection characteristics**



Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{level}	VDD detectable Threshold (TSSOP20,QFN20)	LVD_CR[3:0] = 0000 LVD_CR[3:0] = 0001 LVD_CR[3:0] = 0010 LVD_CR[3:0] = 0011 LVD_CR[3:0] = 0100 LVD_CR[3:0] = 0101 LVD_CR[3:0] = 0110 LVD_CR[3:0] = 0111	Typ - 0.1	4.4 4.0 3.6 3.3 3.1 2.9 2.7 2.5	Typ + 0.1	V
V_{level}	VDD detectable Threshold (LQFP32 QFN32)	LVD_CR[3:0] = 0000 LVD_CR[3:0] = 0001 LVD_CR[3:0] = 0010 LVD_CR[3:0] = 0011 LVD_CR[3:0] = 0100 LVD_CR[3:0] = 0101 LVD_CR[3:0] = 0110 LVD_CR[3:0] = 0111 LVD_CR[3:0] = 1000 LVD_CR[3:0] =1001 LVD_CR[3:0] = 1010 LVD_CR[3:0] = 1011 LVD_CR[3:0] = 1100 LVD_CR[3:0] = 1101 LVD_CR[3:0] =1110 LVD_CR[3:0] =1111	Typ - 0.1	4.6 4.4 4.2 4.0 3.8 3.6 3.4 3.2 3.0 2.8 2.6 Reserved Reserved Reserved Reserved Reserved	Typ + 0.1	V
I_{comp}	Detection current		1	1.5	2	μA
$T_{response}$	VDD response time of monitor after falling below or above threshold		30	50	80	μs
T_{setup}	Monitor build time		3	5	10	μs

[1]. Lab data, not tested in production.

[2] Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.11 Flash memory characteristics

Tab 5.11-1 **Flash memory characteristics**

Symbol	Parameter	Min	Typical	Max	Unit
EC_{flash}	block erase	20K			one
RET_{flash}	data retention	20			year
T_{prog}	byte programming			20	μs
$T_{Sector-erase}$	block erase			8	ms
$T_{Chip-erase}$	Full Chip Erase	20		40	ms

Note: Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

5.12 Low power mode wakeup

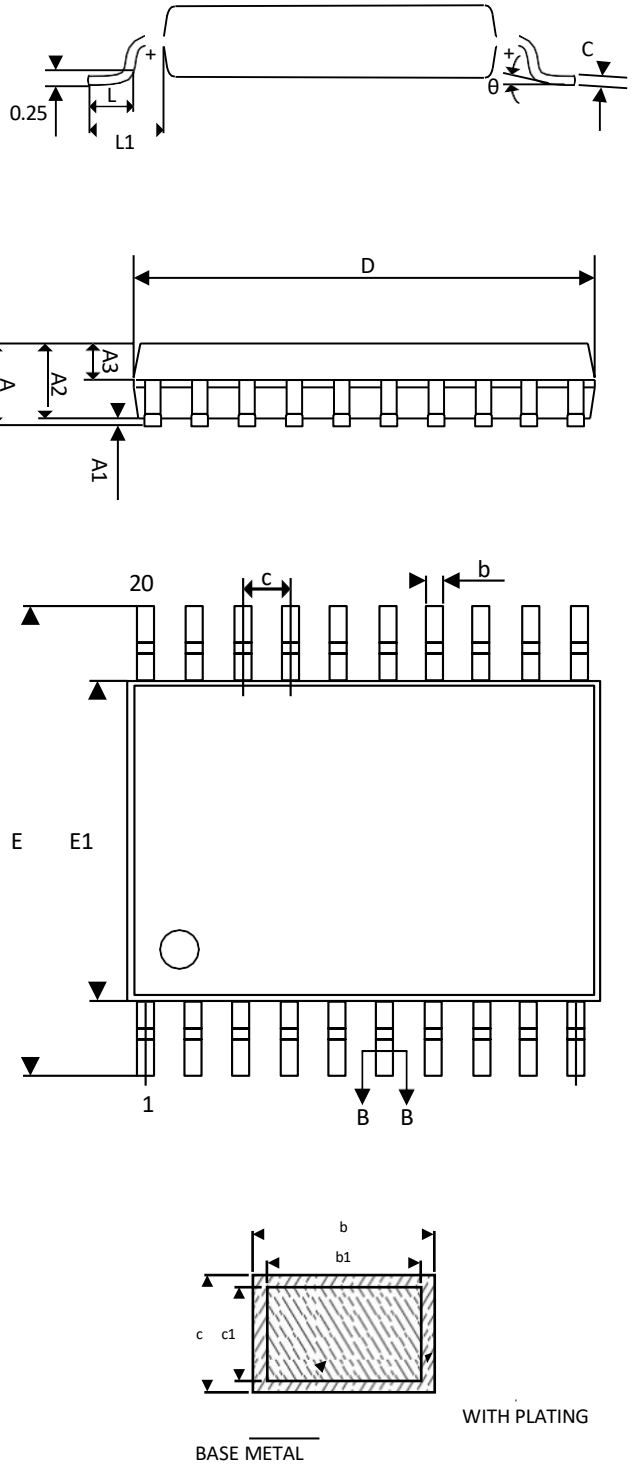
Tab 5.12-1 **Low power mode wakeup**

Symbol	Parameter	Condition	Min	Typical	Max	Unit
T_{wakeup}	Deep Sleep to operation	4M	11.8	12.5	12.8	μs
		8M	11.3	11.6	12.5	
		16M	11.2	11.4	12.0	
		24M	10.5	11.3	11.8	

Note: Unless otherwise noted, typical values (Typ) are tested at Ta=25℃ and VDD=3.3V

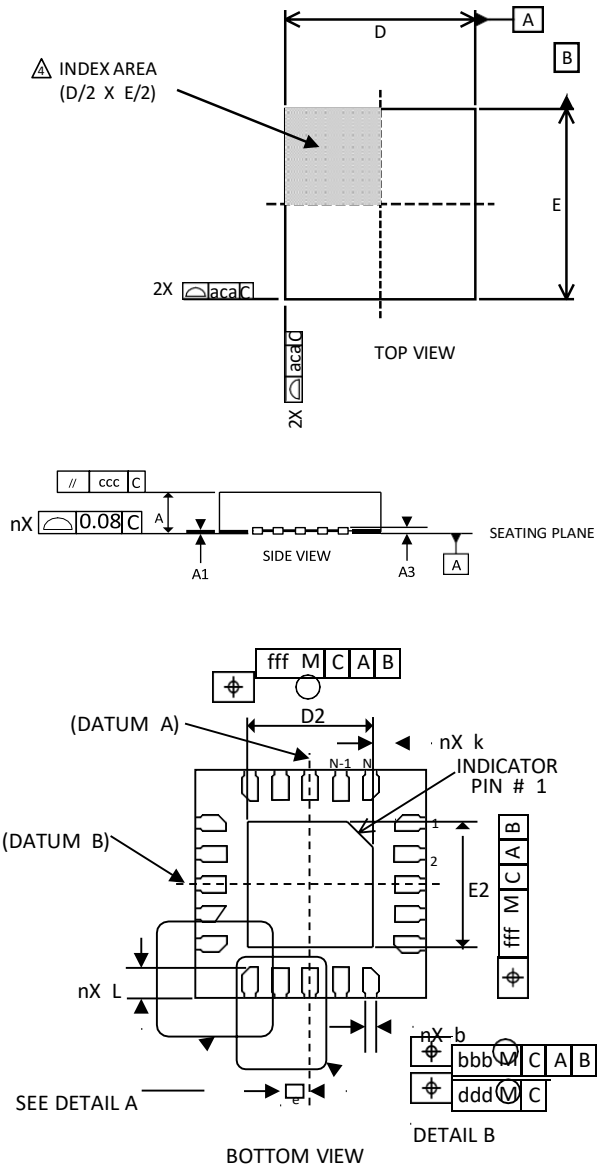
6 Package characteristics

6.1 TSSOP20

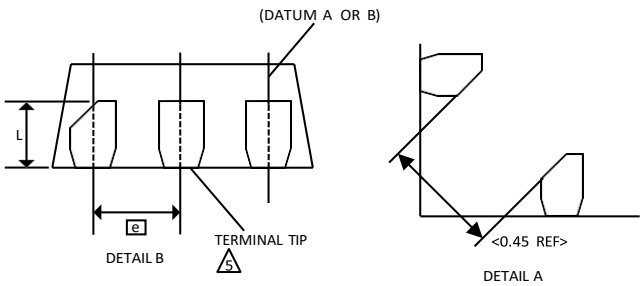


TSSOP20			
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.19	-	0.3
b1	0.19	0.22	0.25
c	0.09	-	0.2
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.25	6.40	6.55
e	0.65 BSC.		
L	0.45	0.60	0.75
L1	1.00 REF.		
θ	0	-	8°

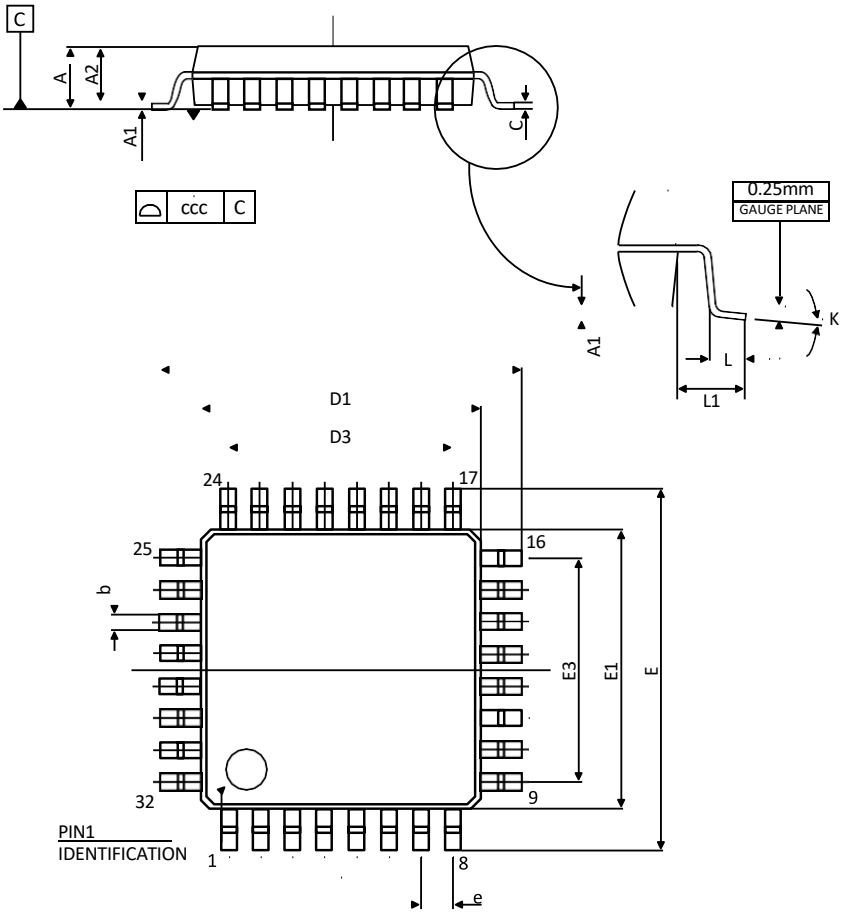
6.2 QFN20



QFN20			
Symbol	Min	Typical	Max
A	0.70	0.75	0.80
b	0.15	0.20	0.25
D		3.00 BSC.	
D2	1.55	1.65	1.75
E		3.00 BSC.	
E2	1.55	1.65	1.75
e		0.40 BSC.	
L	0.30	0.40	0.50
n		20	
nD		5	
nE		5	
A1	0	0.02	0.05
A3		0.203 REF.	
K	0.20	-	-
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	

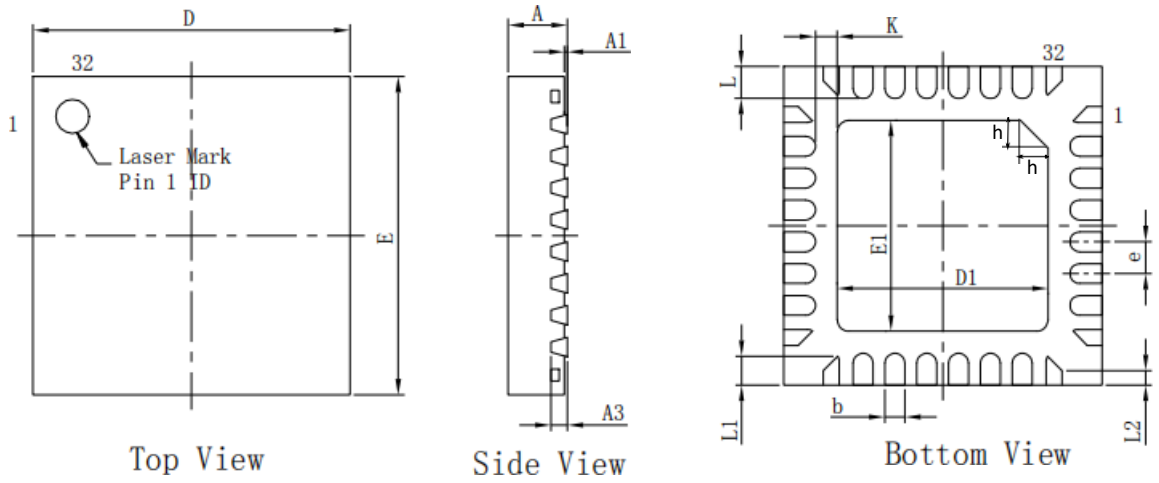


6.3 LQFP32 7x7mm



Symbol	millimeters		
	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.320	-	0.430
c	0.130	-	0.180
D	8.800	9.000	9.200
D1	6.900	7.000	7.100
D3	-	5.600	-
E	8.800	9.000	9.200
E1	6.900	7.000	7.100
E3	-	5.600	-
e	-	0.800	-
L	0.450	0.600	0.750
L1	-	1.000	-
k	0°	3.5°	7°
ccc	-	-	0.100

6.4 QFN32 4x4mm

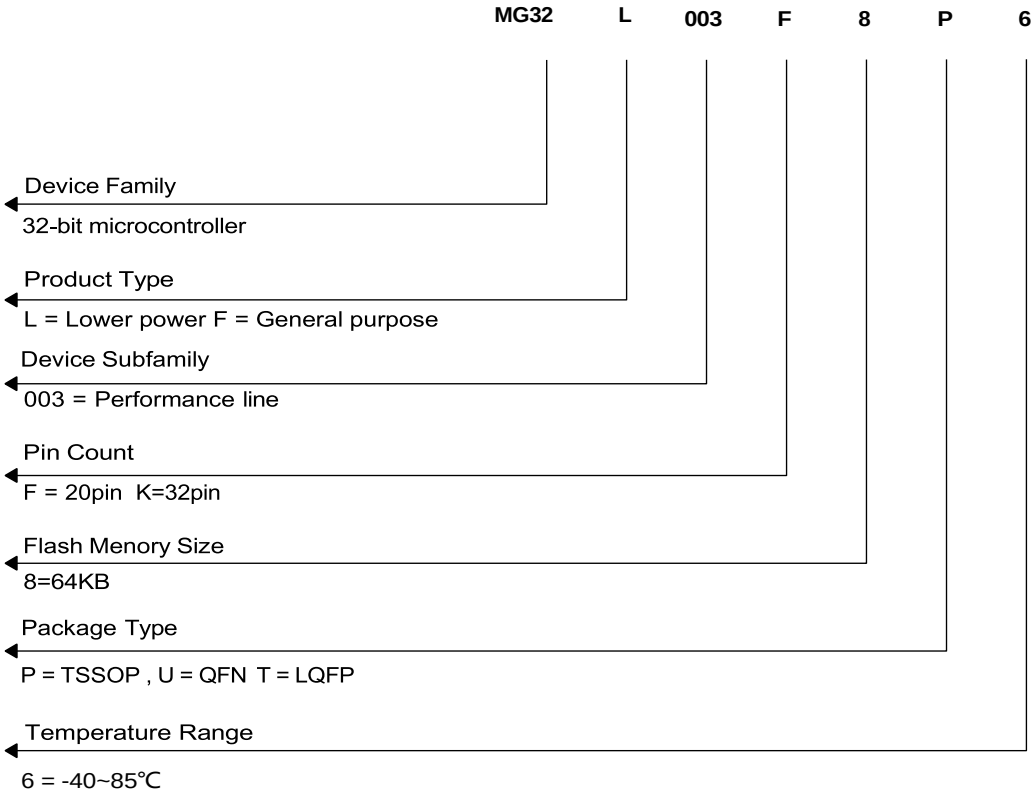


Note:*Drawing is not to scale.*

Symbol	millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A_1	-	0.02	0.05
A_3		0.203	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D_1	2.65	2.70	2.75
E_1	2.65	2.70	2.75
e		0.40	
K	0.25	0.30	0.30
L	0.30	0.35	0.40
h	0.30	0.35	0.40

7 Ordering information

Fig 7.0-1 **Ordering information**



8 Revision history

Version	Revision date	Summary of revisions
0.0	2023/1/07	draft version
0.1	2023/3/1	Add LQFP32 QFN32
0.2	2023/7/6	Add DC supply characteristics max value
0.3	2023/9/28	Remove SOP20

9 IMPORTANT EXPLANATION

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