megawin
make you win

M0+ Cost-Efficient MCU

MG32F04A064

Arm® Cortex®-M0+ based 32-bit Microcontrollers

Data Sheet

Preliminary Version: 0.01

Features

- Core 32-bit Arm® Cortex®-M0+, frequency up to 48MHz.
- Memory
  - **64KB** embedded Flash storage.
  - **1KB Data Flash Memory.**
  - **4KB** SRAM.
- Operating voltage range is from 2.0V to 5.5V.
- Power-on and Power-down reset (POR/PDR), Programmable voltage detector (PVD).
- Built-in **40KHz** LSI low-speed oscillator.
- Built-in **48MHz** HSI high-speed oscillator.
- External clock input frequency is up to 48MHz (HSE, through OSCIN pin).
- Multiple low power modes including Sleep mode, Stop mode and Deep Stop mode.
- **5 timers**:
  - One 16-bit 4-channel advanced timer (TIM1), capable of generating four PWM outputs or three complementary PWM pairs, support center- or edge-aligned PWM mode, support hardware dead time insertion and fault brake, support PWM phase-shift output mode.
  - One 16-bit 4-channel general purpose timer (TIM3), capable of generating four PWM outputs or capture four channel input signals, support decode of hall sensor and quadrature encoder, support infrared decode.
  - One 16-bit basic timer (TIM14), capable of generating one PWM output or capture one channel input signal.
  - One watchdog timer equipped with independent clock source (IWDG).
  - One 24-bit Systick timer.
- Up to 22 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts.
  - All I/O ports can accept input or generate output signal voltage level is not higher than V_{DD}.
- Two USART (support SPI mode).
- One I2C.
- One SPI.
- One **12-bit** ADC (Analog-to-Digital converter) supports **1M** SPS conversion rate, with 12 external inputs and 1 internal input that can sample on-chip voltage sensor.
- Embedded CRC engine
- One COMP
- 96bit unique chip ID (UID)
- Serial Wire Debug (SWD) for debug function.
- Operating temperature range includes -40°C ~ 105°C industrial tier.
- Available in SSOP28 packages

Contents

Tables

Figures

1 Introduction

Overview

The MG32F04A064 microcontrollers are based on Arm® Cortex®-M0+ core. These devices have a maximum clocked frequency of 48MHz, built-in 64KB Flash storage, and contain an extensive range of peripherals and I/O ports. These devices contain one 12-bit ADC, one 16-bit advanced timer, one 16-bit general purpose timer and one 16-bit basic timer, as well as communication interfaces including two USART, one SPI and one I2C.

The operating voltage of this product series is 2.0V to 5.5V, and the operating temperature range (ambient temperature) is -40°C to 105°C extended industrial tier. Multiple sets of power-saving modes make the design of low-power applications possible.

The target applications of this product series include:

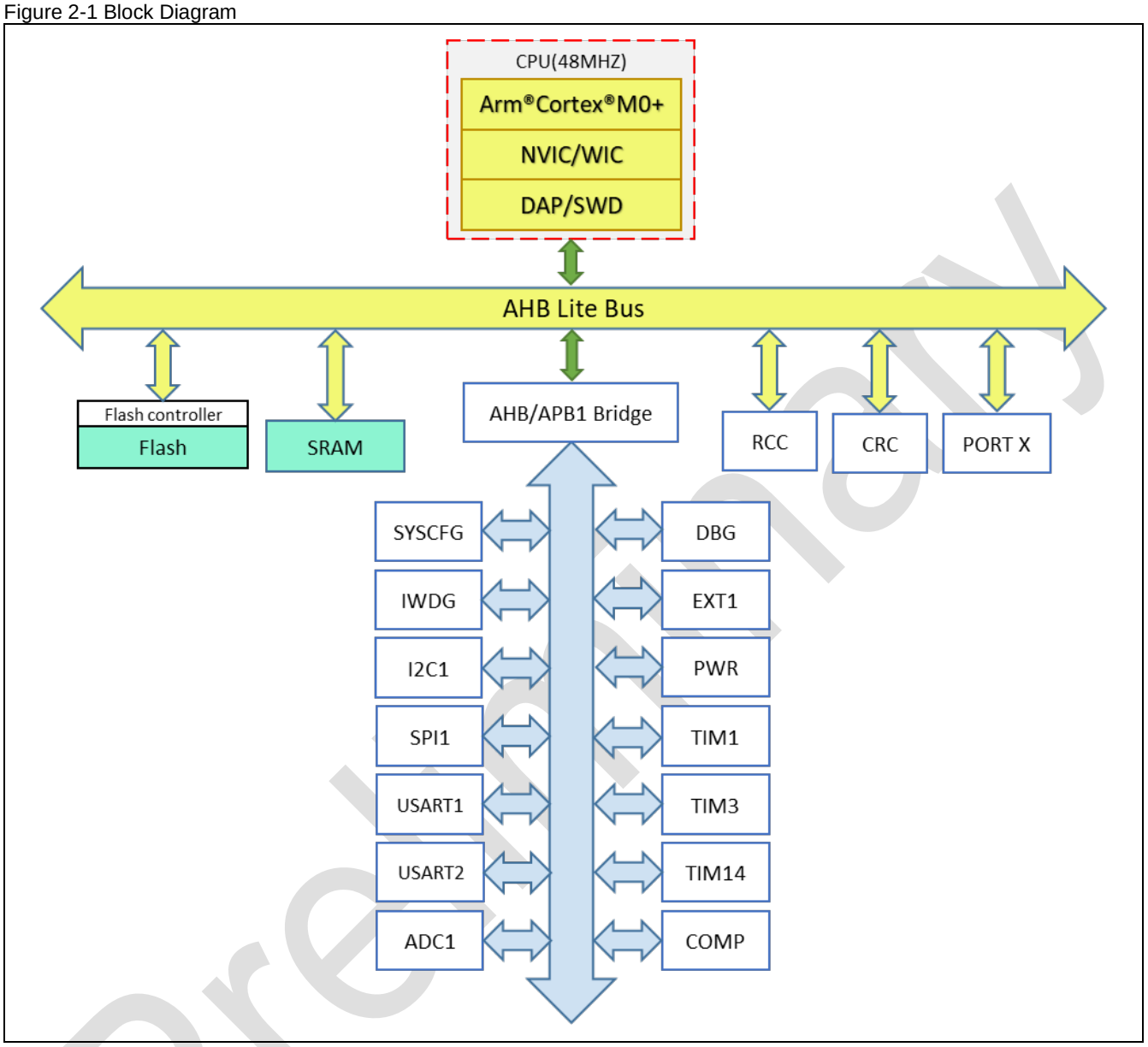
- Wireless charging
- Motor control
- Node control
- Toys
- Lighting circuit
- Fire-fighting devices
- 8/16-bit MCU Replacement

These devices are available in SSOP28 packages.

2 Function Introduction

2.1 Block diagram

Figure 2-1 Block Diagram



2.2 Core Overview

The Arm® Cortex®-M0+ processor is the latest generation of embedded Arm processors, providing a low-cost platform for MCU requirements with reduced pin count, lower system power consumption, and delivering exceptional computational performance along with an advanced interrupt system response.

The Arm® Cortex®-M0+ is a 32-bit RISC processor that offers additional code efficiency, leveraging the high performance of the Arm core within the memory footprint typically occupied by 8-bit and 16-bit systems.

With the built-in Arm core, this product is fully compatible with all Arm tools and software.

2.3 Bus Overview

The bus matrix includes an AHB interconnect matrix, one AHB bus, and a bridged APB bus. AHB peripherals (such as RCC and CRC) are connected to the system bus via the AHB interconnect matrix. Data exchange between the APB and AHB buses is performed through an AHB-to-APB bridge. When accessing 8-bit or 16-bit APB registers, the APB automatically widens the access to 32 bits. Similarly, the AHB-to-APB bridge also features automatic width extension.

2.4 Flash

This product provides up to 64 KB of embedded Flash memory for storing programs and data.

2.5 Data Flash

This product provides up to 1 KB of embedded Flash memory for storing programs and data.

2.6 SRAM

This product provides up to 4KB embedded SRAM.

2.7 NVIC

This product incorporates a Nested Vectored Interrupt Controller (NVIC) capable of handling multiple maskable interrupt channels and 4 programmable priority levels.

- Tightly coupled NVIC enables low-latency interrupt response processing
- Direct entry of interrupt vector addresses into the core
- Tightly coupled NVIC interface
- Allows early handling of interrupts
- Supports handling of late-arriving higher-priority interrupts
- Enables interrupt tail-chaining
- Automatically saves processor state
- Automatically restores state upon interrupt return without extra instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.。

2.8 EXTI

The External Interrupt/Event Controller (EXTI) includes multiple edge detectors that capture level changes from I/O pins and generate interrupt/event requests. All I/O pins can be connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled, and configured with its own trigger mode (rising edge, falling edge, or both edges). A pending status register maintains the state of all interrupt requests.

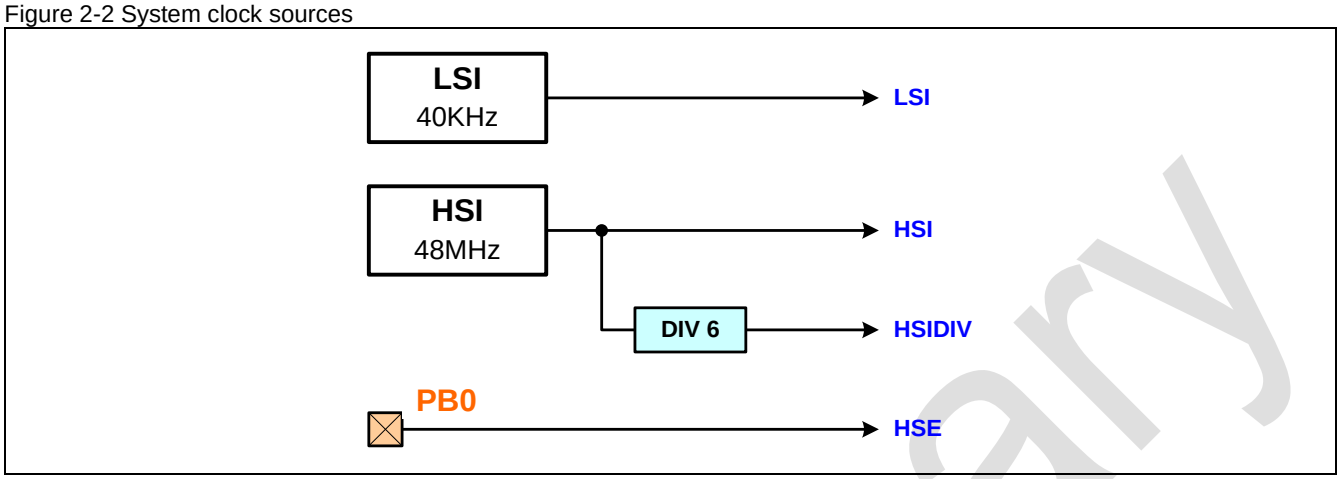
The EXTI can detect pulse widths shorter than the internal APB bus clock cycle.

2.9 Clock and Startup

As shown in Figure 2-2, this product contains the following internal or external clock sources:

- HSI 48MHz
- LSI 40KHz
- HSE

Figure 2-2 System clock sources



The system clock can be selected from the following internal or external clock sources:

- HSI – HSI 48MHz output from the internal high-speed oscillator
- HSIDIV – 6-divided output of the 48 MHz HSI, providing an 8 MHz output.
- LSI – 40KHz output from the LSI
- HSE – External clock input from the OSC_IN (PB0) pin.

The system clock, after division, serves as the clock for the CPU and AHB bus. The maximum operating frequency for both the CPU and the AHB bus is 48 MHz. The maximum operating frequency of the APB bus is the same as that of the AHB bus.

After reset, the HSIDIV (8 MHz) is used as the default system clock. Subsequently, the clock source can be switched to HSI, LSI, or HSE.

2.10 Boot mode

Boot from on-chip Flash.

2.11 Power Supply Scheme

- Powered via the VDD pin for I/O pins and the internal regulator. The operating voltage range for VDD is 2.0V to 5.5V.
- This product does not have a separate VDDA pin. VDDA and VDD are internally connected. VDDA supplies power to the analog sections of the ADC, reset module, oscillators, and PLL. For the specific operating voltage range of analog components, please refer to the Electrical Characteristics section.

2.12 Voltage Regulator

The on-chip voltage regulator converts the external supply voltage to the operating voltage required by the internal logic circuits. The voltage regulator is active after the chip is reset (POR).

2.13 Power Supply Supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage,

and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enabled.

2.14 Low Power Mode

The product supports low-power modes, achieving an optimal balance between low power requirements, short startup times, and multiple wake-up events.

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals remain operational and can wake up the CPU when an interrupt/event occurs.

Stop mode

Stop mode achieves lower power consumption while retaining SRAM and register contents. In Stop mode, the HSI oscillator and HSE crystal oscillator are turned off. The microcontroller can be woken up from Stop mode by any EXTI signal, which can be one of the 16 external I/O ports or the wake-up signal from the PVD output.

Deep Stop mode

This mode maintains the same state as Stop mode but achieves even lower power consumption.

The peripheral status in each low-power mode is shown in Table 2-1, please note:

- Power Down indicates that the module is powered off and all data except Flash is lost.
- Optional indicates that the peripheral can be turned on or off through software configuration.
- ON means work.
- OFF indicates that the function is turned off.
- Retention indicates that data is retained but not operational.

Table 2-1 Peripheral status in different power modes

Module/Mode	Run	Sleep	Stop	Deep Stop
Max. Freq.	48MHz	48MHz	40KHz	40KHz
PVD	Optional	Optional	Optional	Optional
POR	ON	ON	ON	ON
CPU	ON	OFF	OFF	OFF
SRAM	ON	ON	Retention	Retention
Flash	ON	Standby	Standby	Deep Standby
HSI	Optional	Optional	OFF	Power Down
LSI	Optional	Optional	Optional	Optional
IWDG	Optional	Optional	Optional	Optional
ADC	Optional	Optional	OFF	OFF
Other Peripherals	Optional	Optional	OFF	OFF
I/O	Optional	Optional	Retention	Retention

2.15 Timers and watchdogs

This product has one advanced timer, one general purpose timer, one basic timer, one watchdog timer and one Systick timer. The table below compares the features of advanced, general purpose and basic timers.

Table 2-2 Feature summary of advanced, general purpose and basic timers

Type	Instance	Resolution	Counter direction	pre-divider	DMA request	Capture/compare channels	Complementary output
Advanced	TIM1	16-bit	up, down, up/down	1 to 65536	No	4 (no capture)	3
General purpose	TIM3	16-bit	up, down, up/down	1 to 65536	No	4	No
Basic	TIM14	16-bit	up	1 to 65536	No	1	No

Advanced timer (TIM1)

The advanced timer includes a 16-bit counter, four capture/compare channels and three phases complementary PWM generator. This timer supports hardware dead-time insertion when using as complementary PWM generator. This timer can also be used as a full-function general purpose timer. This timer has four independent channels, each channel can be used for:

- Output compare
- PWM generator (center- or edge-aligned)
- Single pulse output

When this timer is used as a general-purpose timer, it has the same function as the TIM3. When this timer is used as a 16-bit PWM generator, it can be configured to a broad duty cycle range from 0% to 100%.

In debug mode, the counter can be frozen.

The advanced timer has lots of identical features and internal structures as the general-purpose timer, in this way the advanced timer can work together with the general-purpose timer through the link function, to provide synchronization and event trigger function.

General-purpose timer (TIM3)

This product has one general-purpose timer (TIM3). The timer has a 16-bit counter, support both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output. These general-purpose timers can also work together through the timer link function, to provide synchronization between timers and event trigger function.

These timers can also be used to decode incremental encoder signals and can also be used to decode one to four Hall sensors' digital output. Any general-purpose timer can be used to generate PWM output or work as basic timer.

In debug mode, the counter can be frozen.

Basic timer (TIM14)

This product has one 16-bit basic timer (TIM14). Each timer has one 16-bit counter, supporting only up counting, with automatically reload. The timer also has one 16-bit frequency pre-divider and one independent channel. Each channel can be used as input capture, output compare, PWM or one pulse mode output.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 40KHz oscillator. As it is independent of the main clock, it can run in shutdown and standby modes. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter can be frozen.

System tick timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a general down counter. It

has the following features:

- 24-bit down counter
- Auto-reload capability
- A maskable interrupt can be generated when counter value is 0
- Programmable clock source

2.16 GPIO

Each GPIO pin can be configured by software as an output (push-pull or open-drain), input (with or without pull-up/pull-down), or alternate function peripheral pin. Most GPIO pins are shared with digital or analog alternate peripherals.

- When required, the peripheral function of an I/O pin can be locked through a specific operation to prevent accidental writes to the I/O registers.

The chip can drive up to five 8-segment common-cathode LED digit tubes to reduce external hardware overhead. Up to five specific I/Os in GPIOA can be configured as sink-current mode (max. 80 mA) to control the digit tube cathodes, while up to eight specific I/Os can be configured as constant current source mode (configurable in four levels: 2.5 / 5 / 7.5 / 10 mA) to control the segment selection of the digit tubes.

2.17 USART

The product integrates two Universal Synchronous/Asynchronous Receiver/Transmitter (USART) interfaces. These modules support a wide range of baud rates (including integer and fractional settings) through an integrated baud rate generator. They support LSB-first and MSB-first transmission modes, programmable data lengths of 8 or 9 bits, and stop bit configurations of 0.5/1/1.5/2 bits. The interfaces also support synchronous or asynchronous unidirectional communication and half-duplex single-wire communication. In SPI mode, a maximum baud rate of 6 Mbps is supported.

2.18 I2C

This product has one I2C interface. The I2C bus interface can work in multi-master mode or slave mode and supports standard mode (100Kbps) and fast mode (400Kbps). The I2C interface supports 7-bit or 10-bit addressing.

2.19 SPI

This product has one SPI interfaces. The SPI interface can be configured as 1 to 32 bits per frame in master or slave mode, allowing up to 24 Mbps in master mode and 12 Mbps in slave mode.

2.20 ADC

The product incorporates one 12-bit Analog-to-Digital Converter (ADC) supporting a conversion rate of up to 1 MSPS, configured with 12 external channels and 1 internal channel. It supports single, single-cycle, and continuous scan conversion modes. The ADC also features flexible sequence sampling, allowing sampling channels to be arranged in any order. Each external and internal conversion channel is equipped with an independent channel data register. The internal channel is used to sample the internal reference voltage, enabling calculation of the chip's power supply voltage based on the converted value in applications.

The analog watchdog function allows highly precise monitoring of one or all selected channels. An interrupt is generated when the monitored signal exceeds predefined thresholds.

Events generated by general-purpose timers and advanced-control timers are internally connected to the ADC trigger source selection, enabling precise control over ADC sampling timing.

2.21 CRC

The CRC (Cyclic Redundancy Check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In numerous applications, CRC-based techniques are employed to verify the integrity of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a means to detect Flash memory errors. The CRC calculation unit can be used to compute a software signature in real time and compare it with the signature generated during the software's linking and build process.

2.22 COMP

The product incorporates one analog comparator (COMP) that can operate independently (available on all terminal I/O pins) or in conjunction with timers. The COMP supports various functions, including: wake-up events from low-power modes triggered by analog signals; brake events for fast PWM shutdown; capture events; or OCref_clr events for cycle-by-cycle current control. The COMP features programmable hysteresis voltage. These comparators share an 8-bit reference voltage source (CRV), where the CRV reference can be selected between VDDA and the 1.2V VREF output. The reference voltage for each comparator can be selected from an I/O port or the CRV output.

2.23 SWD

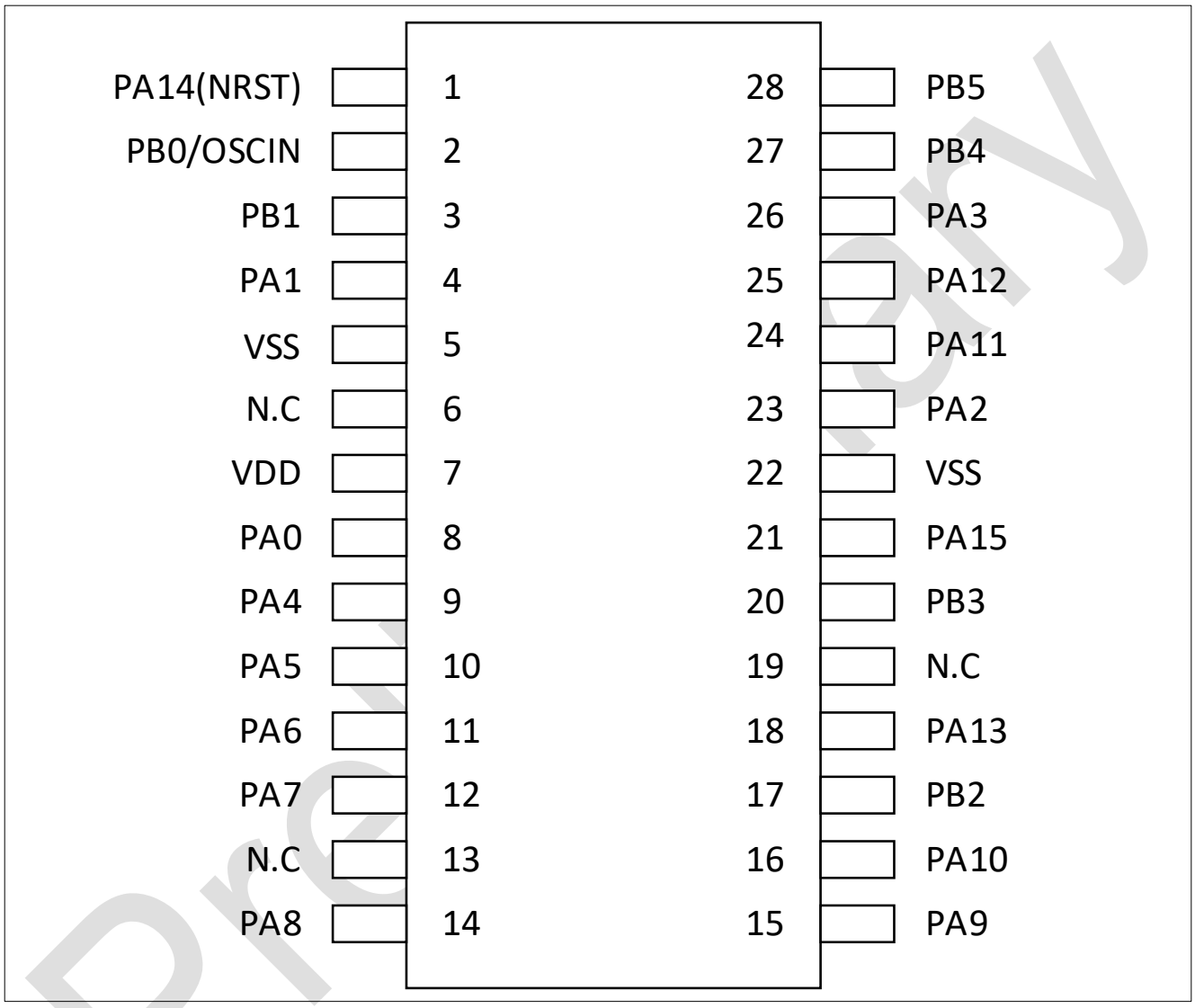
The product incorporates Arm's standard two-wire Serial Wire Debug (SW-DP) interface.

3 Pinout and assignment

3.1 Pinout diagram

3.1.1 SSOP28 pinout

Figure 3-1 SSOP28 pinout diagram



3.2 Pin assignment

Table 3-1 Pin assignment table

SSOP28	Name	Type [1]	I/O level [2]	Main function	Multiplex function	Additional function
1	PA14 (NRST) [3]	I/O	TC[2]	PA14 (NRST)	SWCLK USART1_TX USART2_TX SPI1_SCK	-
2	PB0/ OSCIN	I/O	TC	PB0	USART2_SCK TIM14_CH1 USART1_NCTS SPI1_NSS	ADC1_VIN[1]
3	PB1	I/O	TC	PB1	USART2_RX UASRT1_NRTS	ADC1_VIN[0]
4	PA1	I/O	TC	PA1	USART1_SCK USART2_TX I2C1_SDA SPI1_MOSI	COMP1_INP3
5	VSS	S	-	VSS	-	-
6	-	-	-	-	-	-
7	VDD	S	-	VDD	-	-
8	PA0	I/O	TC+HS[2]	PA0	SPI1_NSS USART1_RX TIM1_CH3N I2C1_SCL TIM3_CH3 COMP1_OUT	-
9	PA4	I/O	TC+HS	PA4	TIM1_CH4 TIM1_BKIN I2C1_SDA TIM3_CH4	COMP1_INM2
10	PA5	I/O	TC+HS	PA5	SPI1_SCK TIM1_CH1N I2C1_SCL	-
11	PA6	I/O	TC+HS	PA6	SPI1_MOSI TIM1_CH1 TIM1_CH1N SPI1_MISO TIM1_CH3	-
12	PA7	I/O	TC+HS	PA7	SPI1_MISO TIM1_CH1N TIM1_CH2N MCO TIM1_CH4	ADC1_VIN[7]
13	-	-	-	-	-	-
14	PA8	I/O	TC+CC[2]	PA8	SPI1_SCK TIM1_CH2 I2C1_SDA TIM3_CH1	-
15	PA9	I/O	TC+CC	PA9	SPI1_MOSI TIM1_CH2N TIM1_CH1 TIM14_CH1 TIM1_CH3N	-
16	PA10	I/O	TC+CC	PA10	SPI1_MISO TIM1_CH3 TIM1_CH2 MCO USART1_TX	-
17	PB2	I/O	TC	PB2	USART1_TX SPI1_NSS I2C1_SCL TIM3_CH1	ADC1_VIN[8] COMP1_INM1

SSOP28	Name	Type (1)	I/O level (2)	Main function	Multiplex function	Additional function
18	PA13	I/O	TC	PA13	SWDIO USART1_RX USART2_RX I2C1_SCL SPI1_MISO	-
19	-	-	-	-	-	-
20	PB3	I/O	TC	PB3	USART1_RX SPI1_SCK I2C1_SDA TIM3_CH2	ADC1_VIN[9] COMP1_INP0
21	PA15	I/O	TC+CC	PA15	SPI1_NSS TIM1_CH3N SPI1_MOSI TIM3_CH3	ADC1_VIN[6]
22	VSS	S	-	VSS	-	-
23	PA2	I/O	TC+CC	PA2	USART2_NCTS TIM1_CH2N SPI1_MISO TIM3_CH2	ADC1_VIN[5]
24	PA11	I/O	TC+CC	PA11	USART2_NRTS USART1_SCK TIM1_CH2 TIM14_CH1 TIM3_CH1	ADC1_VIN[4]
25	PA12	I/O	TC+CC	PA12	USART1_TX	ADC1_VIN[3] COMP1_INM3
26	PA3	I/O	TC+CC	PA3	USART1_RX USART2_SCK SPI1_NSS	ADC1_VIN[2] COMP1_INM0
27	PB4	I/O	TC	PB4	I2C1_SDA SPI1_MOSI USART2_RX TIM3_CH3	ADC1_VIN[10] COMP1_INP1
28	PB5	I/O	TC	PB5	I2C1_SCL SPI1_MISO USART2_TX TIM3_CH4	ADC1_VIN[11] COMP1_INP2

1. I = input, O = output, S = power pins, HiZ = high resistance state.
2. TC: standard IO. Input signal level should not exceed VDD.
   CC: I/O configurable as Constant Current source mode
   HS: I/O configurable as High Sink mode
3. When SFT_NRST_RMP bit of RCC_SYSCFG is set to 1, PA14 is mapped as an NRST external reset.

3.3 Pin Alternate Functions

Table 3-2 PA port multiplexing AF0-AF5

Pin	AF0	AF1	AF2	AF3	AF4	AF5
PA0	SPI1_NSS	USART1_RX	TIM1_CH3N	I2C1_SCL	TIM3_CH3	COMP1_OUT
PA1	-	USART1_SCK	USART2_TX	I2C1_SDA	SPI1_MOSI	-
PA2	USART2_NCTS	-	TIM1_CH2N	SPI1_MISO	TIM3_CH2	-
PA3	-	USART1_RX	USART2_SCK	-	SPI1_NSS	-
PA4	-	TIM1_CH4	TIM1_BKIN	I2C1_SDA	TIM3_CH4	-
PA5	SPI1_SCK	TIM1_CH1N	-	I2C1_SCL	-	-
PA6	SPI1_MOSI	TIM1_CH1	TIM1_CH1N	SPI1_MISO	TIM1_CH3	-
PA7	SPI1_MISO	TIM1_CH1N	TIM1_CH2N	MCO	TIM1_CH4	-

Pin	AF0	AF1	AF2	AF3	AF4	AF5
PA8	SPI1_SCK	TIM1_CH2	-	I2C1_SDA	TIM3_CH1	-
PA9	SPI1_MOSI	TIM1_CH2N	TIM1_CH1	TIM14_CH1	TIM1_CH3N	-
PA10	SPI1_MISO	TIM1_CH3	TIM1_CH2	MCO	USART1_TX	-
PA11	USART2_NRTS	USART1_SCK	TIM1_CH2	TIM14_CH1	TIM3_CH1	-
PA12	-	USART1_TX	-	-	-	-
PA13	SWDIO	USART1_RX	USART2_RX	I2C1_SCL	SPI1_MISO	-
PA14	SWCLK	USART1_TX	USART2_TX	-	SPI1_SCK	-
PA15	SPI1_NSS	TIM1_CH3N	-	SPI1_MOSI	TIM3_CH3	-

Table 3-3 PB port multiplexing AF0-AF5

Pin	AF0	AF1	AF2	AF3	AF4	AF5
PB0	-	USART2_SCK	TIM14_CH1	USART1_NCTS	SPI1_NSS	-
PB1	-	-	USART2_RX	USART1_NRTS	-	-
PB2	USART1_TX	SPI1_NSS	I2C1_SCL		TIM3_CH1	-
PB3	USART1_RX	SPI1_SCK	I2C1_SDA		TIM3_CH2	-
PB4	I2C1_SDA	SPI1_MOSI	USART2_RX		TIM3_CH3	-
PB5	I2C1_SCL	SPI1_MISO	USART2_TX		TIM3_CH4	-

4 Electrical Characteristics

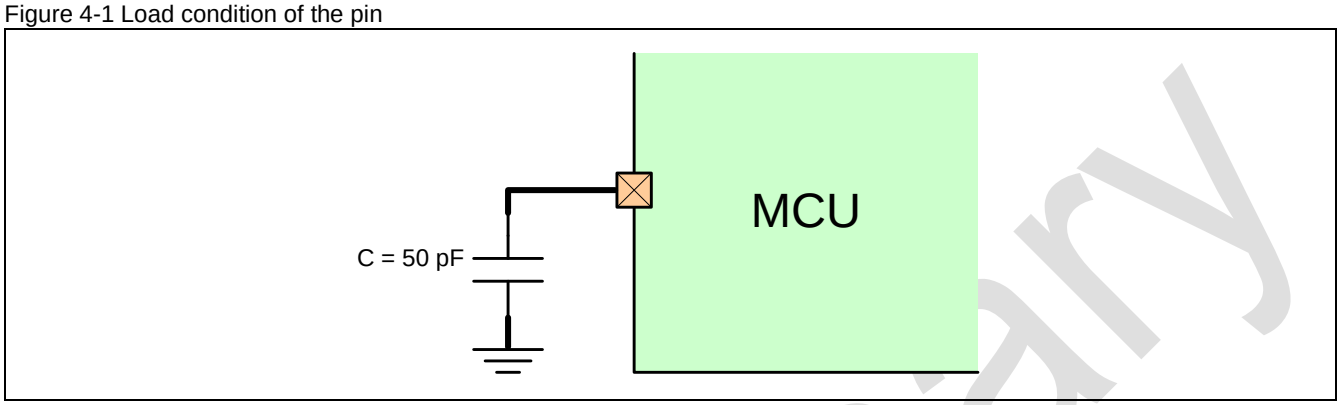
4.1 Test condition

Unless otherwise specified, all voltages are referenced to V_{SS}.

4.1.1 Load Capacitance

The load conditions for measuring pin parameters are shown in the Figure 4-1.

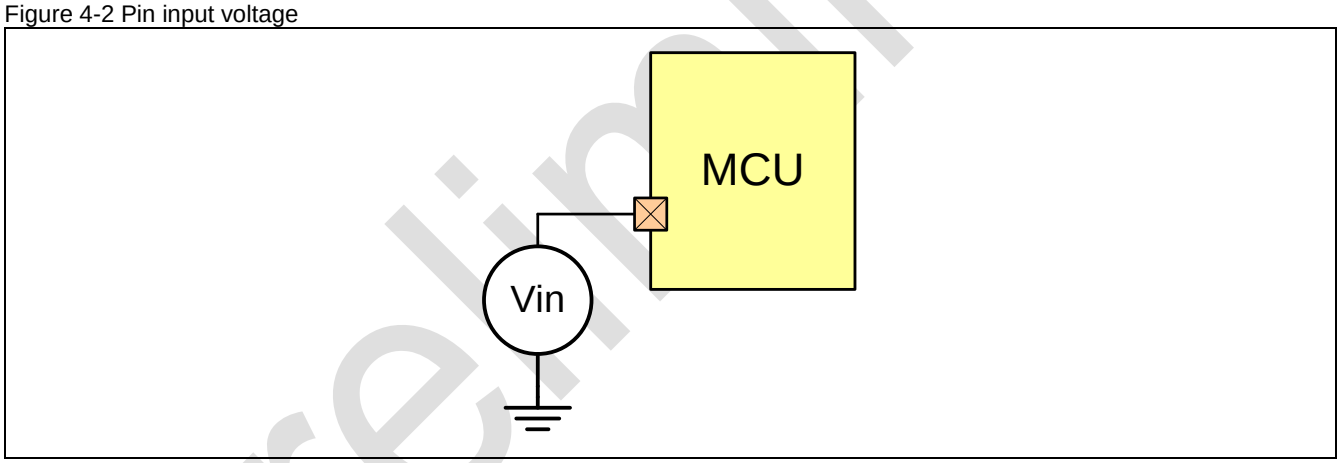
Figure 4-1 Load condition of the pin



4.1.2 I/O input voltage

The measurement method for the input voltage on pins is shown in Figure 4-2.

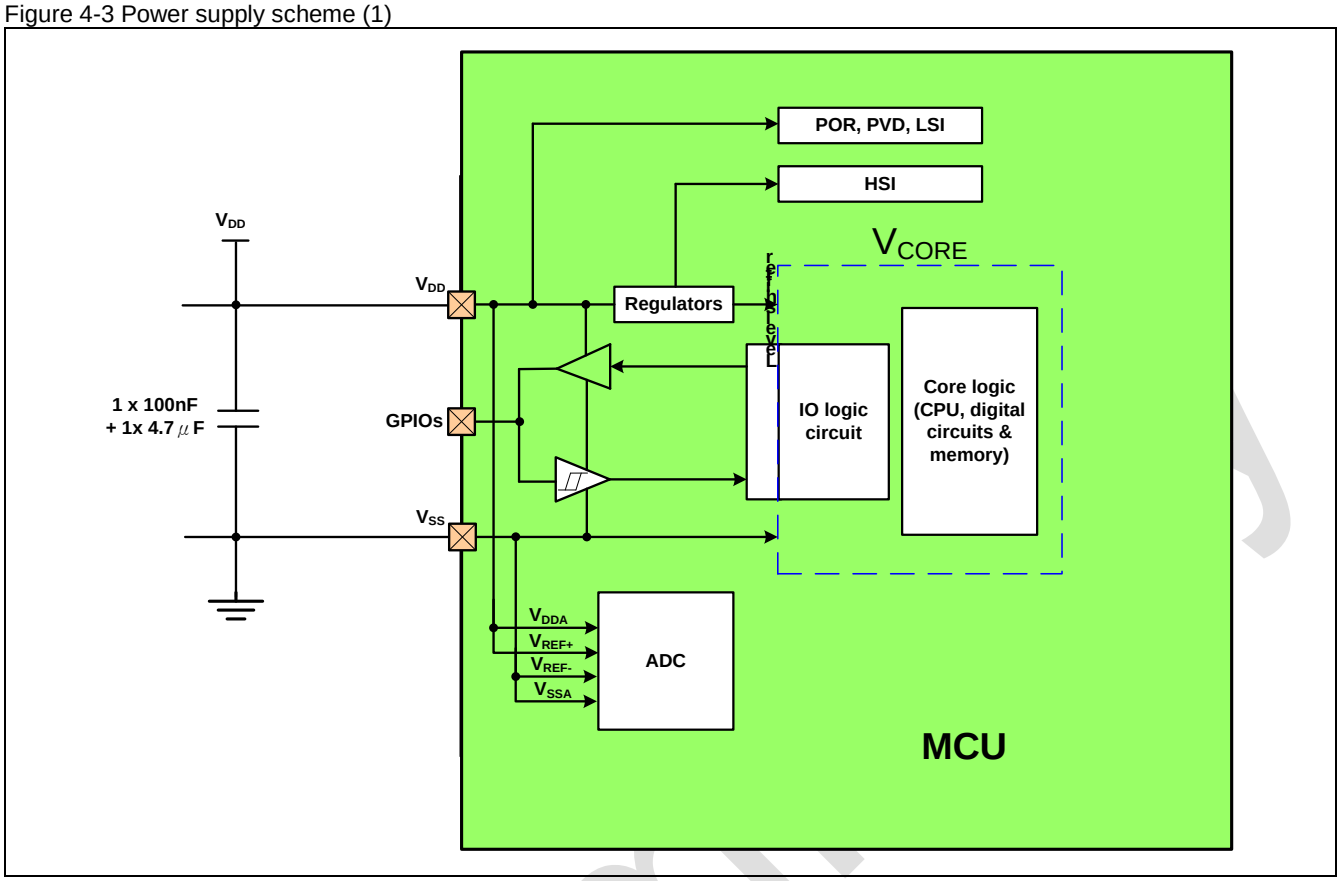
Figure 4-2 Pin input voltage



4.1.3 Power Supply scheme

The power supply design scheme is shown in Figure 4-3.

Figure 4-3 Power supply scheme (1)



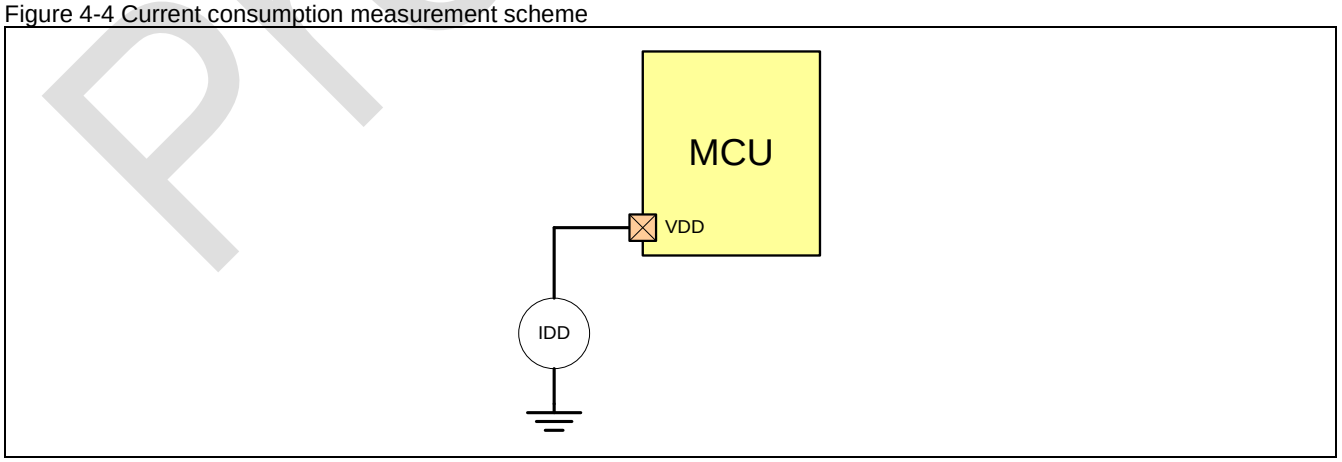
Notes:

1. For optimal chip performance, it is recommended to use the filtering ceramic capacitors shown in the figure above for decoupling between power pair (VDD, VSS)
2. For this product, the V_{DD}, V_{DDA}, and V_{REF+} are all connected to the VDD pin inside the chip, and V_{SS}, V_{SSA}, and V_{REF-} are all connected to the VSS pin inside the chip.

4.1.4 Current consumption measurement

The measurement of the current consumption on the pin is shown in Figure 4-4.

Figure 4-4 Current consumption measurement scheme



4.2 Absolute maximum rating

Stresses above the absolute maximum ratings given in "Absolute Group Maximum Ratings" list (Table 4-1, Table 4-2) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Voltage characteristics

Symbol	Description	Minimum	Maximum	Unit
V_{DDx}-V_{SSx}	External main supply voltage	-0.3	5.8	V
V_{IN} (2)	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	

1. All power (VDD) and ground (VSS) pins must always be connected to the external power supply system within the permitted range.
2. The maximum value of V_{IN} must be respected. Refer to the table below for the maximum allowed injected current values.

Table 4-2 Current characteristics

Symbol	Description	Maximum	Unit
I_{VDD}	Total current through V_{DD} power pins (supply current) (1)	+100	mA
I_{VSS} (1)	Total current through V_{SS} ground pins (outflow current) (1)	-100	
I_{IO}	Output sink current on any I/O and control pins	+20	
	Output source current on any I/O and control pins	-20	
	Output sink current on high sink mode I/O	+80	
$I_{INJ(PIN)}$ (2)(3)	NRST pin injection current	±5	
	HSE OSC_IN pin injection current	±5	
$\sum I_{INJ(PIN)}$ (5)	Other pins injection current (3)	±25	

1. All main power (V_{DD}) and ground (V_{SS}) pins must always be connected to an external power source within the permissible range.
2. Reverse injection current can interfere with the analog performance of the device. It must be ensured that VIN < VDD +0.3V, and VIN > VSS -0.3V。
3. When $V_{IN} > V_{DD}$, forward injection current is generated; when $V_{IN} < V_{SS}$, a reverse injected current is generated. The $I_{INJ(PIN)}$ limit must not be exceeded.
4. When there is simultaneous injection current for multiple inputs, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse injection current (instantaneous value).

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-3 General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	-	48	
V_{DD}	Digital and Analog circuit operating voltage (Analog performance is not guaranteed)	-	2.0	-	2.5	V
	Analog circuit operating voltage (Performance is guaranteed)		2.5	3.3	5.5	
T_A	Ambient temperature (Industrial level)	-	40	-	85	℃
	Ambient temperature (Extended industrial level)	-	-40	-	105	
T_J	Junction temperature (1) (Industrial level)	-	-40	-	105	℃
	Junction temperature (1) (Extended industrial level)	-	-40	-	125	

1. Under conditions of lower power dissipation, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

4.3.2 Operating conditions at power-up/power-down

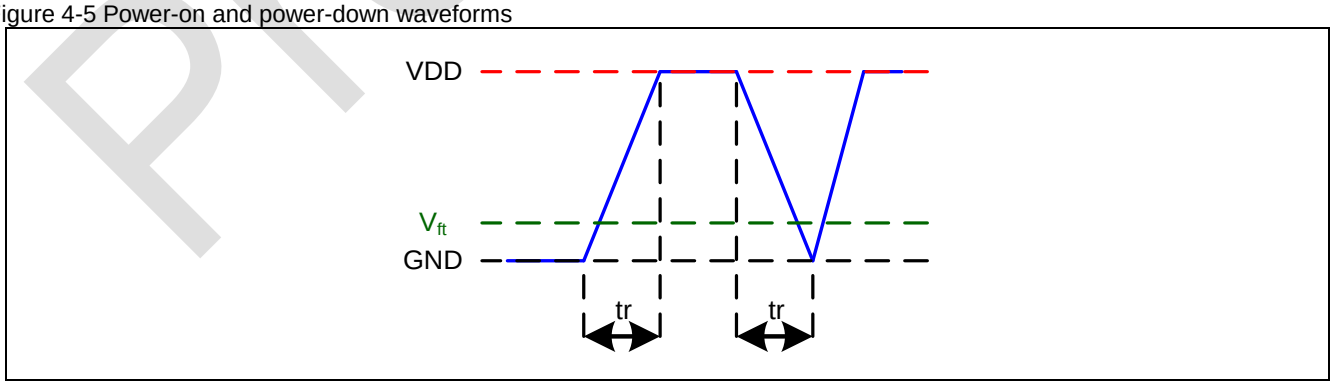
The parameters provided in the table below are tested under the general operating conditions specified in Table 4-3.

Table 4-4 Operating conditions during power-up and power-down

Symbol	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time t_r	2	-	500000	us
	V_{DD} fall time t_f	300	-	-	
V_{ft} (3)	Power-down threshold voltage	-	200	-	mV

1. Data based on characterization results, not tested in production.
2. The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phased in the following waveform diagram, and no power-down is allowed during power-on process.
3. Note: To ensure the reliability of chip power-on, all power-on sequences must start from a voltage below 200 mV.

Figure 4-5 Power-on and power-down waveforms



4.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 4-3.

Table 4-5 Embedded reset and power control block characteristics

Symbol	Parameter	Condition	Min. (3)	Typ.	Max. (3)	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3:0]=0000 (Rising edge)	-	-	-	V
		PLS[3:0]=0000 (Falling edge)	-	-	-	
		PLS[3:0]=0001 (Rising edge)	-	2.13	-	
		PLS[3:0]=0001 (Falling edge)	-	2.03	-	
		PLS[3:0]=0010 (Rising edge)	-	2.43	-	
		PLS[3:0]=0010 (Falling edge)	-	2.33	-	
		PLS[3:0]=0011 (Rising edge)	-	2.73	-	
		PLS[3:0]=0011 (Falling edge)	-	2.63	-	
		PLS[3:0]=0100 (Rising edge)	-	3.04	-	
		PLS[3:0]=0100 (Falling edge)	-	2.93	-	
		PLS[3:0]=0101 (Rising edge)	-	3.34	-	
		PLS[3:0]=0101 (Falling edge)	-	3.23	-	
		PLS[3:0]=0110 (Rising edge)	-	3.64	-	
		PLS[3:0]=0110 (Falling edge)	-	3.54	-	
		PLS[3:0]=0111 (Rising edge)	-	3.94	-	
		PLS[3:0]=0111 (Falling edge)	-	3.84	-	
		PLS[3:0]=1000 (Rising edge)	-	4.24	-	
		PLS[3:0]=1000 (Falling edge)	-	4.14	-	
		PLS[3:0]=1001 (Rising edge)	-	4.55	-	
		PLS[3:0]=1001 (Falling edge)	-	4.44	-	
		PLS[3:0]=1010 (Rising edge)	-	4.85	-	
		PLS[3:0]=1010 (Falling edge)	-	4.74	-	
V_{POR} (1)	Power-on reset threshold	-	-	1.805	-	V
V_{PDR}(1)	Power-down reset threshold	-	-	1.763	-	V
V_{hyst_PDR}	PDR hysteresis	-	-	42	-	mV
$T_{RSTTEMPO}$ (2)	Reset duration	-	-	3.6	-	ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.
3. Determined through comprehensive characterization.

Note: The reset duration is measured from the moment of power-on (POR reset) until the first I/O toggle occurs in the user application code.

4.3.4 Internal Reference Voltage

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 4-3.

Table 4-6 Build-in voltage reference

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Built-in voltage reference	-40°C < T_A < 105°C	-	1.2	-	V
$T_{s\_vrefint}$ (1)	ADC sampling time when readout build-in voltage reference	-	-	2	-	us

1. The sampling time is obtained through multiple tests

4.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and connected to a static level - V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting cycle, 24 ~ 48 MHz is 1 waiting cycle).
- The instruction prefetching function is on. When the peripherals are enabled: $f_{HCLK} = f_{PCLK}$.

Note: The instruction prefetching function must be set before setting the clock and bus divider.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 4-3.

Table 4-7 Typical current consumption in Run mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled						Typical All peripherals disabled						Unit
				-40°C	0°C	25°C	55°C	85°C	105°C	-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DD}	Supply current in Run mode	HSI is clock source	48M	4.46	4.53	4.60	4.70	4.83	4.98	3.16	3.22	3.29	3.39	3.53	3.67	mA
			24M	2.99	3.06	3.13	3.23	3.37	3.52	2.16	2.23	2.30	2.40	2.54	2.69	
			12M	2.05	2.12	2.19	2.30	2.43	2.58	1.64	1.70	1.78	1.88	2.02	2.17	
			6M	1.58	1.64	1.72	1.82	1.96	2.11	1.37	1.44	1.51	1.62	1.75	1.90	
			3M	1.34	1.41	1.48	1.59	1.72	1.87	1.24	1.30	1.38	1.49	1.62	1.77	
			750K	1.16	1.23	1.30	1.41	1.59	1.70	1.14	1.20	1.28	1.38	1.57	1.67	
			375K	1.13	1.20	1.27	1.38	1.57	1.67	1.12	1.19	1.26	1.37	1.55	1.65	
			187.5K	1.12	1.18	1.26	1.36	1.55	1.65	1.11	1.18	1.25	1.36	1.54	1.65	
			93.75K	1.11	1.18	1.25	1.36	1.49	1.64	1.11	1.17	1.25	1.35	1.49	1.64	
		HSIDIV is clock source	8M	1.63	1.70	1.77	1.88	2.02	2.17	1.42	1.48	1.56	1.66	1.80	1.95	
			4M	1.38	1.45	1.52	1.63	1.76	1.92	1.24	1.31	1.38	1.49	1.63	1.78	
			2M	1.23	1.29	1.37	1.47	1.61	1.76	1.15	1.22	1.30	1.40	1.54	1.69	

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled						Typical All peripherals disabled						Unit
				-40°C	0°C	25°C	55°C	85°C	105°C	-40°C	0°C	25°C	55°C	85°C	105°C	
			1M	1.15	1.21	1.29	1.39	1.53	1.68	1.11	1.18	1.04	1.10	1.16	1.20	
			500K	1.11	1.17	1.25	1.35	1.49	1.65	1.09	1.16	1.23	1.34	1.47	1.65	
			31.25K	1.07	1.14	1.21	1.32	1.45	1.61	1.07	1.14	1.21	1.32	1.45	1.60	
		LSI is clock source	40K	0.57	0.64	0.72	0.83	0.97	1.13	0.56	0.64	0.72	0.83	0.97	1.13	

Table 4-8 Typical current consumption in Sleep mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled						Typical All peripherals disabled						Unit
				-40°C	0°C	25°C	55°C	85°C	105°C	-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DD}	Supply current in Sleep mode	HSI is clock source	48M	3.13	3.20	3.28	3.38	3.52	3.67	1.82	1.89	1.97	2.07	2.21	2.36	mA
			24M	2.30	2.37	2.44	2.55	2.69	2.84	1.47	1.54	1.61	1.72	1.86	2.01	
			12M	1.71	1.78	1.85	1.96	2.09	2.25	1.29	1.36	1.43	1.54	1.68	1.83	
			6M	1.41	1.47	1.55	1.65	1.79	1.94	1.20	1.27	1.34	1.45	1.58	1.73	
			3M	1.25	1.32	1.40	1.50	1.64	1.79	1.15	1.22	1.29	1.40	1.53	1.69	
			750K	1.14	1.21	1.28	1.39	1.52	1.67	1.11	1.18	1.26	1.36	1.50	1.65	
			375K	1.12	1.19	1.26	1.37	1.55	1.65	1.11	1.18	1.25	1.35	1.54	1.64	
			187.5K	1.11	1.18	1.25	1.36	1.55	1.65	1.10	1.17	1.25	1.35	1.54	1.64	
			93.75K	1.11	1.17	1.25	1.35	1.49	1.64	1.10	1.17	1.25	1.35	1.49	1.64	
		HSIDIV is clock source	8M	1.40	1.47	1.55	1.65	1.79	1.94	1.19	1.25	1.33	1.44	1.57	1.72	
			4M	1.27	1.33	1.41	1.51	1.65	1.80	1.13	1.20	1.27	1.38	1.51	1.67	
			2M	1.17	1.23	1.31	1.42	1.55	1.70	1.10	1.17	1.24	1.35	1.48	1.64	
			1M	1.12	1.19	1.26	1.37	1.50	1.65	1.08	1.15	1.22	1.33	1.47	1.62	
			500K	1.09	1.16	1.23	1.34	1.47	1.63	1.07	1.14	1.22	1.32	1.46	1.61	
			125K	1.07	1.14	1.21	1.32	1.46	1.61	1.07	1.14	1.21	1.32	1.45	1.60	
			62.5K	1.07	1.13	1.21	1.32	1.45	1.60	1.06	1.13	1.21	1.32	1.45	1.60	
			31.25K	1.40	1.47	1.55	1.65	1.79	1.94	1.19	1.25	1.33	1.44	1.57	1.72	
		LSI is clock source	40K	0.56	0.64	0.72	0.83	0.97	1.13	0.56	0.63	0.72	0.83	0.97	1.13	

Table 4-9 Typical current consumption in stop mode (1)

Symbol	Parameter	Conditions	Typical						Unit
			-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DD}	Supply current in Stop mode	Enter Stop mode after reset, V_{DD}=3.3V	38.1	52.8	56.3	60.8	57.4	75.8	μA
	Supply current in Deep Stop mode	Enter Deep Stop mode after reset, V_{DD}=3.3V	1.32	1.86	2.02	2.39	3.65	7.63	

1. The I/O state is an analog input.
2. Determined by characterization, not tested in production.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under

the following conditions:

- All I/O pins are in analog input mode and connected to a static level - V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise specified.
- The given value is calculated by measuring the current consumption.
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient operating temperature and V_{DD} supply voltage conditions are listed in Table 4-3.

Table 4-10 On-chip peripheral current consumption (1)

Symbol	Parameter	Bus	Typical	Unit
I_{DD}	CRC	AHB	0.14	uA/MHz
	GPIOA		0.04	
	GPIOB		0.04	
	TIM1	APB1	0.99	
	TIM3		0.54	
	Tim14		0.85	
	ADC1		7.24	
	SPI1		1.68	
	USART1		0.19	
	USART2		0.16	
	I2C1		2.60	
	COMP		5.41	
	PWR		2.55	
	DBG		4.28	
	SYSCFG		1.14	

1. f_{HCLK} = 48MHz，f_{APB1} = f_{HCLK}, the prescale coefficient of each peripheral is the default value.

Wake up time from low power mode

The wake-up time listed in the table below is measured during the wake-up process of the internal clock HSI. The clock source used to wake up the chip depends on the current operating mode:

- Stop or Standby mode: the clock source is the oscillator
- Sleep mode: the clock source is the clock used when entering the Sleep mode.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 4-3.

Table 4-11 Wake up time from low power mode

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wake up from Sleep mode	System clock is HSIDIV	3.3	μs
t_{WUSTOP}	Wake up from Stop mode	System clock is HSIDIV	16.3	μs
$t_{WUDEEPSTOP}$	Wake up from Deep Stop mode	System clock is HSIDIV	22.6	μs

4.3.6 External clock source characteristics

High-speed external user clock generated from an external source

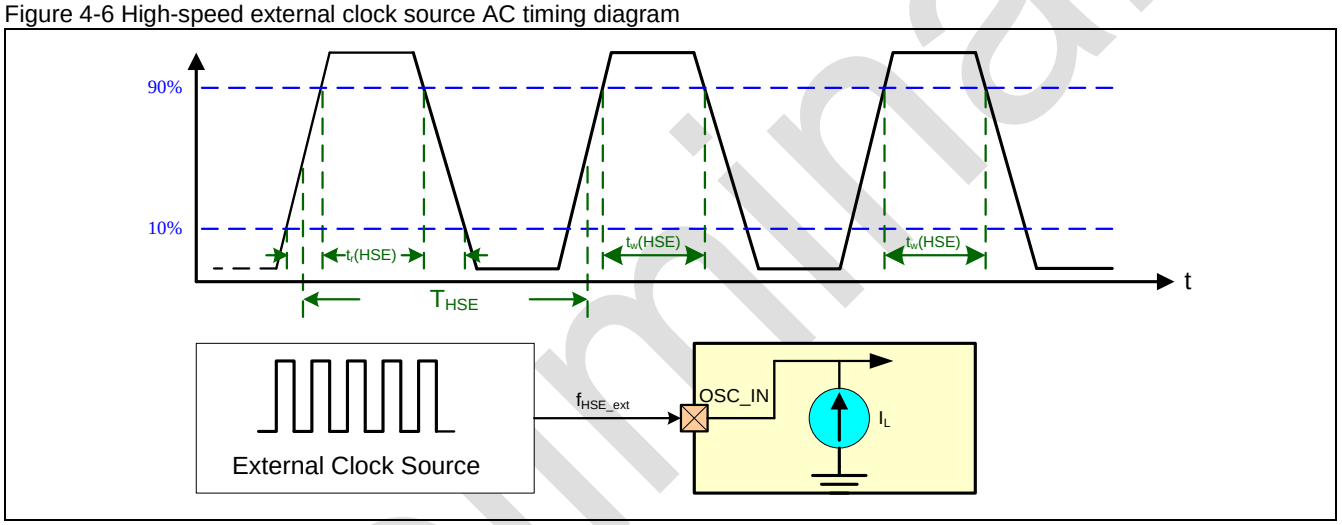
The characteristic parameters given in the following table are measured by a high-speed external clock source, and the ambient temperature and power supply voltage meet General operating conditions.

Table 4-12 High-speed external user clock characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock source frequency (1)	-	-	8	48	MHz
V_{HSEH}	OSC_IN input high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time (1)	-	20	-	-	ns

1. Guaranteed by design, not tested in production

Figure 4-6 High-speed external clock source AC timing diagram



4.3.7 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 4-13 HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
ACC_{HSI} (3)	HSI oscillator deviation	T_A = 25°C	-1	-	+1	%
		T_A = 0°C ~ 85°C	-2	-	+2	%
		T_A = -20°C ~ 105°C	-2.5	-	+2.5	%
		T_A = -40°C ~ 105°C	-3.5	-	+3.5	%
$T_{stab(HSI)}$ (2)	HSI oscillator startup time	-	-	-	18	μs
$I_{DD(HSI)}$ (2)	HSI oscillator power consumption	-	-	496	-	μA

1. V_{DD} = 3.3V, TA = - 40°C ~ 105°C, unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Drawn from comprehensive evaluation.

Low-speed internal (LSI) oscillator

Table 4-14 LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	-	-	40	-	KHz
ACC_{LSI} (3)	LSI oscillator deviation	T_A = 0°C ~ 55°C	-10	-	+10	%
		T_A = -40°C ~ 105°C	-20	-	+20	%
$T_{stab(LSI)}$ (2)	LSI oscillator startup time	-	-	-	50	μs
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	-	-	0.3	-	μA

1. V_{DD} = 3.3V, T_A = -40°C ~ 105°C, unless otherwise stated.
2. Guaranteed by design, not tested in production.
3. Drawn from comprehensive evaluation.

4.3.8 Memory characteristics

Table 4-15 Flash memory characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	32-bit programming time	-	-	25	-	μs
t_{ERASE}	Page (1024 bytes) erase time	-	-	2	-	ms
t_{ME}	Mass erase time	-	-	8	-	ms

Table 4-16 Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{END}	Endurance	-	100000	-	-	Cycles
T_{DR}	Data retention	T_A = 85°C	25	-	-	Years

4.3.9 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the following table.

Table 4-17 EMS characteristics

Symbol	Parameter	Conditions	Level/Type
V_{FESD}	Voltage limit applied to any I/O pin, resulting in malfunction	V_{DD} = 3.3V, T_A = +25°C, f_{HCLK} = 48MHz. Conforming to IEC61000-4-2	2A
V_{FEFT}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	V_{DD} = 3.3V, T_A = +25°C, f_{HCLK} = 48MHz. Conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software.

Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for this application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

4.3.10 Functional EMS (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Static latch-up

Two complementary static latch-up tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output, and configurable I/O pin

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 4-18 ESD & LU characteristics

Symbol	Parameter	Conditions	Maximum	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to ESDA/JEDEC JS-001-2024	±5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = 25°C, conforming to ESDA/JEDEC JS-002-2025	±2000	V
I_{LU}	Latch-up current	T_A = 25°C, conforming to JESD78F	±300	mA
I_{LU}	Latch-up current	T_A = 105°C, conforming to JESD78F	±150	mA

4.3.11 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 4-3 are used for tests. All I/O ports are CMOS compatible.

Table 4-19 I/O static characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low level input voltage	-	-	-	0.3 * V_{DD}	V
V_{IH}	High level input voltage	-	0.7 * V_{DD}	-	-	V
V_{hy}	Schmitt trigger hysteresis (1)	-	0.1 * V_{DD}	-	-	V
I_{lkg}	Input leakage current (2)	-	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor (3)	V_{IN} = V_{SS}	-	52.7	-	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)	V_{IN} = V_{DD}	-	56	-	kΩ
C_{IO}	I/O pin capacitance	-	-	-	10	pF

1. Drawn from comprehensive evaluation, not tested in production.
2. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are poly resistors.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

In the user application, the number of I/O pins must ensure that the drive current must be limited to respect the absolute maximum rating specified in Table 4-1:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum operating current that the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

The chip can drive up to five 8-segment common-cathode LED digit tubes to minimize external hardware overhead. In GPIOA, up to five specific I/Os can be configured in high-sink mode (max. 80 mA) to control the digit tube cathodes, while up to eight specific I/Os can be configured in constant-current source mode (configurable in four levels: 2.5/5/7.5/10 mA) to control the segment selection of the digit tubes.

Output current

Unless otherwise stated, the parameters listed in the table below are provided under the ambient temperature and VDD supply voltage in accordance with the conditions summarized in Table 4-3. All I/O ports are CMOS compatible.

Table 4-20 Output voltage characteristics (3)

Symbol	Parameter	Condition	Typical		Unit
			General mode	High Sink mode	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=6mA, V_{DD}=2.0V	0.19	0.06	V
V_{OH} (2)	Output high voltage		1.71	1.7	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=8mA, V_{DD}=2.0V	0.27	0.07	
V_{OH} (2)	Output high voltage		1.58	1.58	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=20mA, V_{DD}=2.0V	V_{DD}	0.21	
V_{OH} (2)	Output high voltage		0	0	
V_{OL} (1)	Output low current	$\|I_{IO}\|$=40mA, V_{DD}=2.0V	-	0.47	
V_{OH} (2)	Output high voltage		-	0	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=60mA, V_{DD}=2.0V	-	0.87	
V_{OH} (2)	Output high voltage		-	0	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=80mA, V_{DD}=2.0V	-	V_{DD}	
V_{OH} (2)	Output high voltage		-	0	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=6mA, V_{DD}=3.3V	0.13	0.05	V
V_{OH} (2)	Output high voltage		3.12	3.12	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=8mA, V_{DD}=3.3V	0.17	0.07	
V_{OH} (2)	Output high voltage		3.06	3.05	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=20mA, V_{DD}=3.3V	0.46	0.16	
V_{OH} (2)	Output high voltage		2.64	2.6	
V_{OL} (1)	Output low current	$\|I_{IO}\|$=40mA, V_{DD}=3.3V	-	0.33	
V_{OH} (2)	Output high voltage		-	0.79	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=60mA, V_{DD}=3.3V	-	0.49	
V_{OH} (2)	Output high voltage		-	0	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=80mA, V_{DD}=3.3V	-	0.68	
V_{OH} (2)	Output high voltage		-	0	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=6mA, V_{DD}=5.5V	0.11	0.06	V
V_{OH} (2)	Output high voltage		5.36	5.36	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=8mA, V_{DD}=5.5V	0.14	0.07	
V_{OH} (2)	Output high voltage		5.32	5.31	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=20mA, V_{DD}=5.5V	0.34	0.15	

Symbol	Parameter	Condition	Typical		Unit
			General mode	High Sink mode	
V_{OH} (2)	Output high voltage		5.04	5.02	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=40mA, V_{DD}=5.5V	-	0.29	
V_{OH} (2)	Output high voltage		-	4.5	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=60mA, V_{DD}=5.5V	-	0.42	
V_{OH} (2)	Output high voltage		-	3.81	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$=80mA, V_{DD}=5.5V	-	0.56	
V_{OH} (2)	Output high voltage		-	2.74	

1. The current sunk by the chip, I_{IO} must always adhere to the absolute maximum ratings specified in the table. Additionally, the sum of I_{IO} (across all I/O and control pins) must not exceed I_{VSS}.
2. The current sourced by the chip, I_{IO} must always adhere to the absolute maximum ratings specified in the table. Furthermore, the sum of I_{IO} (across all I/O and control pins) must not exceed I_{VDD}.
3. Resulted from comprehensive evaluation.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in the following figure and table, respectively.

Unless otherwise stated, the parameters listed in the following table are provided under the ambient temperature and supply voltage in accordance with the condition Table 4-3.

Table 4-21 I/O AC characteristics (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
$t_{f(IO)out}$	Output fall time	C_L = 50pF V_{DD}=3.3V	5.8	ns
$t_{r(IO)out}$	Output rise time		7.7	ns

1. The maximum frequency is defined in Figure 4-7.
2. Guaranteed by design, not tested in production.

Figure 4-7 I/O AC characteristics

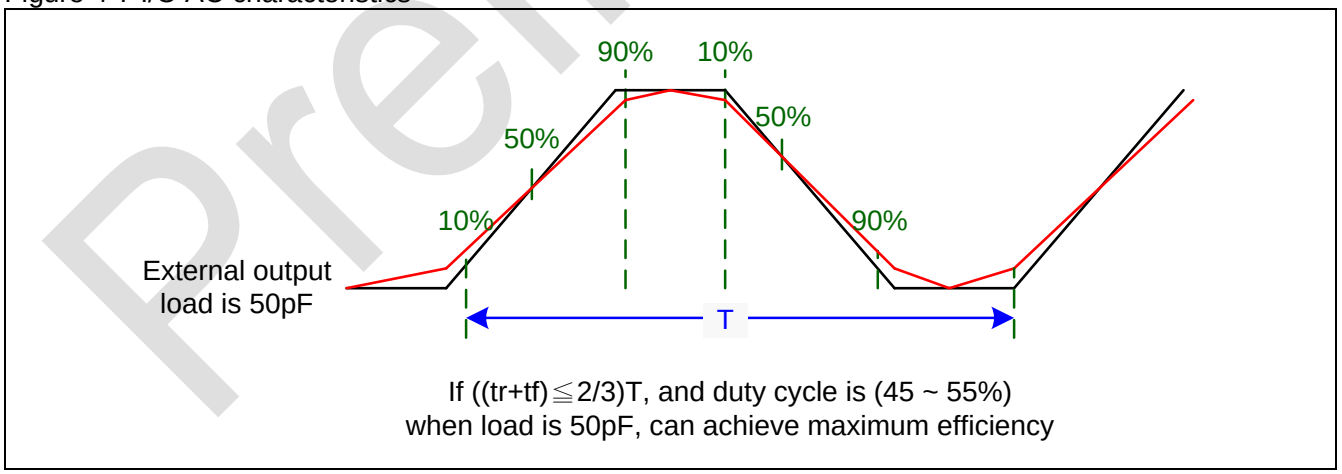


Table 4-22 Constant Current Source Mode Drive Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{OH}	LEDIO Output current	V_{DD}=2.7~5.5V,V_{OH}=VDD~1.0, LEDIOCR Range 0	-	2.5	-	mA
		V_{DD}=2.7~5.5V,V_{OH}=VDD~1.0, LEDIOCR Range 1	-	5.0	-	mA
		V_{DD}=2.7~5.5V,V_{OH}=VDD~1.0, LEDIOCR Range 2	-	7.5	-	mA

		V_{DD}=2.7~5.5V,V_{OH}=VDD~1.0, LEDIOCR Range 3	-	10.0	-	mA
Accuracy	Current accuracy	V_{DD}=5V, T_A=25℃, LEDIOCR Range 3 (10 mA)	-	-	TBD	-
△I1	Line Regulation	T_A= 25 ℃，LEDIOCR Range 3 (10 mA). When V_{DD}=5 V, the current is I1，and when V_{DD}= 4.5 V, the current is I2. The value is calculated as : ((I1-I2)/I1)*2	-	-	TBD	-
△I2	Load Regulation	TA= 25 ℃，LEDIOCR Range 3 (10 mA)，Across the VDD range of 4.5V to 5.5V, measure current I1 when the output is at VDD -1V and current I2 when the output is at VDD -2V by adjusting the load. Then calculate (I1-I2)/I1	-	-	TBD	-
T_{coeff}	Temperature coefficient	T_A=-40 ~ 105 ℃	-	-	TBD	

4.3.12 Timer characteristics

The parameters listed in the following table are guaranteed by design.

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see section 4.3.11 I/O port characteristics.

Table 4-23 TIMx (1) characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	20.8	-	ns
f_{EXT}	External clock frequency of channel 1 to 4	-	0	-	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0208	1365.3	us
t_{MAX_COUNT}	Maximum possible counter value (TIM_PSC adjustable)	-	-	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	-	1365.3	us
t_{MAX_IN}	TIM maximum input frequency	-	-	48	MHz

1. Guaranteed by design, not tested in production.

4.3.13 I2C interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and supply voltage conditions summarized in Table 4-3.

The I2C interface conforms to the standard I2C communication protocol but has the following limitations: SDA and SCL are not true open-drain pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} is disabled, but still present.

The I2C characteristics are listed in the following table. Refer to section 4.3.11 I/O port characteristics for details on the characteristics of input/output alternate function pins (SDA and SCL).

Table 4-24 I2C characteristics

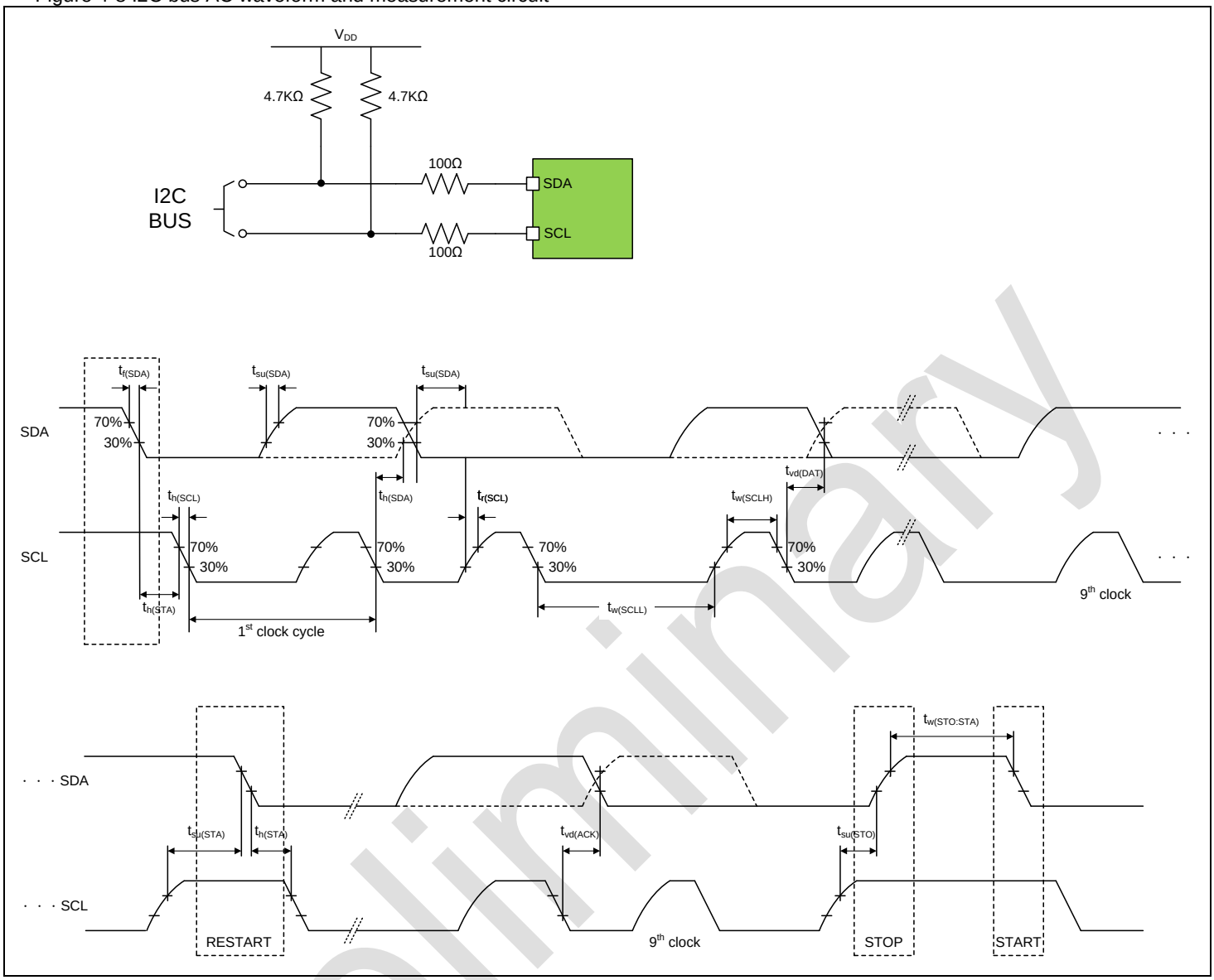
Symbol	Parameter	Standard I2C (1)		Fast mode I2C (1)		Unit
		Minimum	Maximum	Minimum	Maximum	
$t_{w(SCLL)}$	SCL clock low time	8*t_{PCLK}	-	8*t_{PCLK}	-	us
$t_{w(SCLH)}$	SCL clock high time	8*t_{PCLK}	-	8*t_{PCLK}	-	us
$t_{su(SDA)}$	SDA setup time	1*t_{PCLK}	-	1*t_{PCLK}	-	ns
$t_{h(SDA)}$	SDA data retention time	0 (2)	-	0 (2)	-	ns
$t_{r(SDA)}$/ $t_{r(SCL)}$	SDA and SCL rising time	-	1000	20	300	ns
$t_{f(SDA)}$ /$t_{f(SCL)}$	SDA and SCL fall time	-	300	20	300	ns
$t_{vd(DAT)}$ (3)	Data valid time	-	7*t_{PCLK}	-	7*t_{PCLK}	us
$t_{vd(ACK)}$ (4)	Data valid acknowledge time	-	7*t_{PCLK}	-	7*t_{PCLK}	us
$t_{h(STA)}$	Start condition hold time	4*t_{PCLK}	-	4*t_{PCLK}	-	us
$t_{su(STA)}$	Start condition setup time	8*t_{PCLK}	-	8*t_{PCLK}	-	us
$t_{su(STO)}$	Stop condition setup time	12*t_{PCLK}	-	12*t_{PCLK}	-	us
$t_{w(STO:STA)}$	Time from Stop condition to Start condition (bus idle)	7*t_{PCLK}	-	7*t_{PCLK}	-	us
C_b	Capacitive load of each bus	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. Before SDA enters the indeterminate range of 0.3 VDD to 0.7VDD, ensure that SCL falls below 0.3 VDD on its falling edge.

NOTE: For controllers that cannot observe the SCL falling edge then independent measurement of the time for the SCL transition from static high (V_{DD}) to 0.3V_{DD} should be used to insert a delay of the SDA transition with respect to SCL.

3. $t_{vd(DAT)}$ = time for data signal from SCL LOW to SDA output.
4. $t_{vd(ACK)}$ = time for Acknowledgement signal from SCL LOW to SDA output.

Figure 4-8 I2C bus AC waveform and measurement circuit (1)



1. Measurement point is set to the CMOS level： $0.3V_{DD}$ and $0.7V_{DD}$.

4.3.14 SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 4-3.

Refer to section 4.3.11 I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 4-25 SPI characteristics (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode, T_A = 25°C	-	24 (4)	MHz
		Slave mode, T_A = 25°C	-	12	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	6	ns
$t_{f(SCK)}$	SPI clock fall time	Load capacitance: C = 15pF	-	6	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	10	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	10	-	ns
$t_{w(SCKH)}$ (1)	SCK high time	-	$t_{c(SCK)}/2$ - 6	$t_{c(SCK)}/2$ + 6	ns
$t_{w(SCKL)}$ (1)	SCK low time	-	$t_{c(SCK)}/2$ - 6	$t_{c(SCK)}/2$ + 6	ns
$t_{su(MI)}$ (1)	Data input setup time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	15	-	ns
$t_{su(SI)}$ (1)		Slave mode	5	-	ns
$t_{h(MI)}$ (1)	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	0	-	ns
$t_{h(SI)}$ (1)		Slave mode	5	-	ns
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	15	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	15	ns

1. Data based on characterization results. Not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.
4. When the SPI operates at its maximum rated speed, it is recommended to series a matching resistor in the SCK line to ensure signal integrity, and to keep the SCK connection between the SPI Master and SPI Slave as short as possible.

Figure 4-9 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1

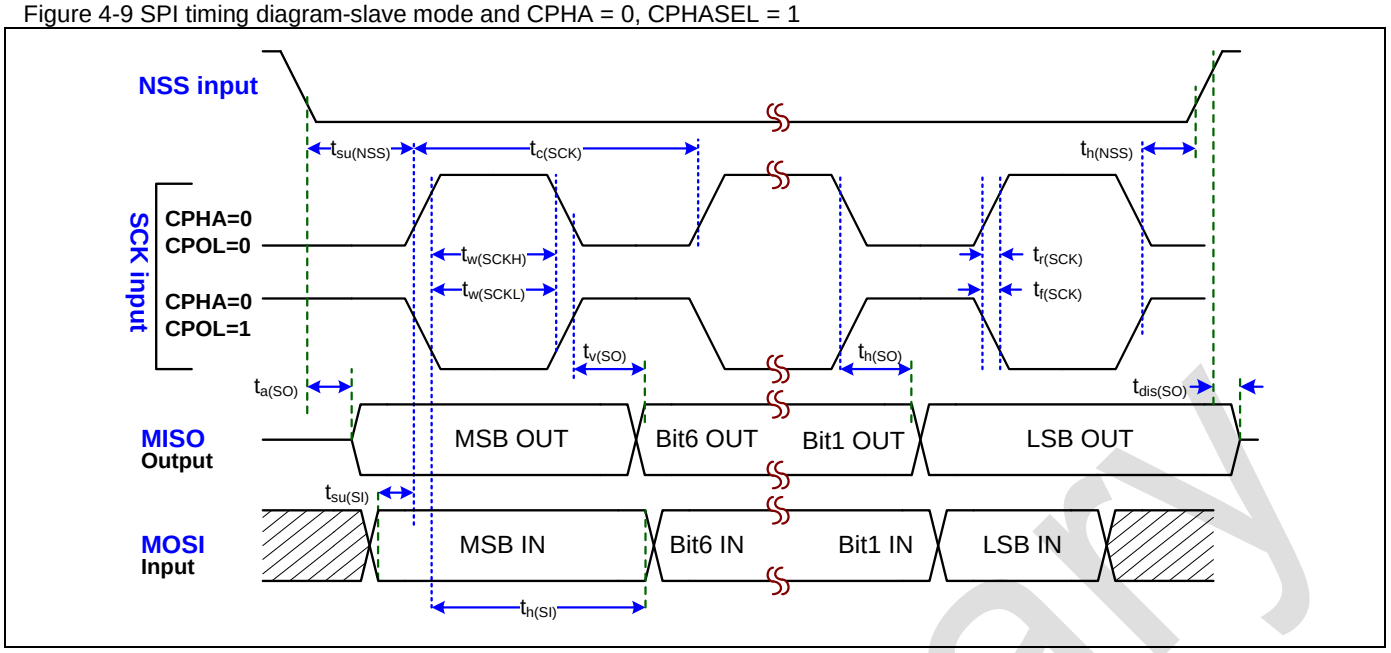
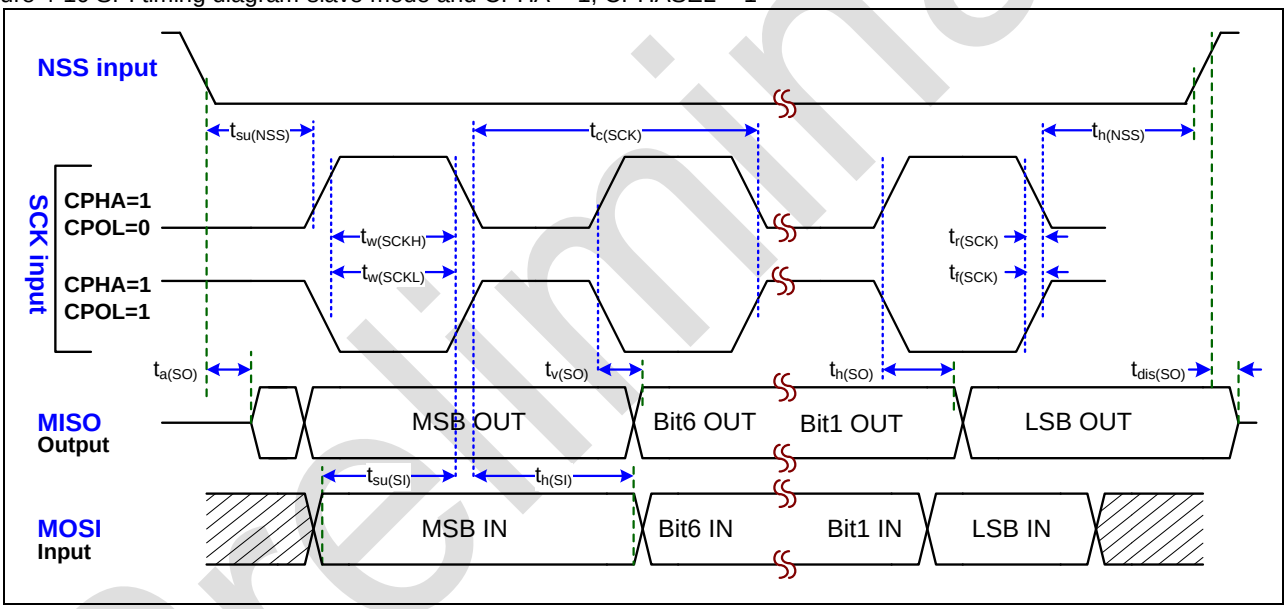
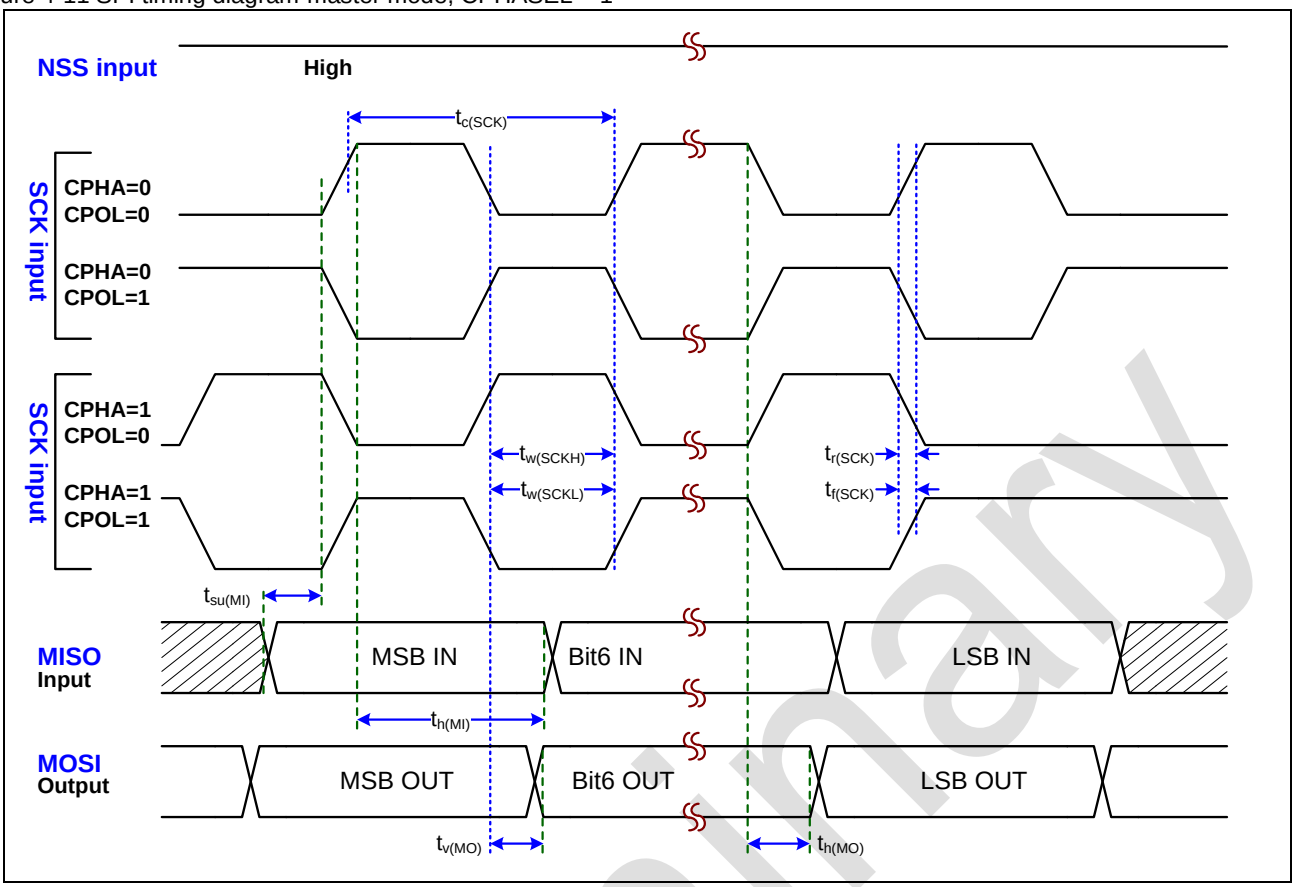


Figure 4-10 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1 (1)



1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$

Figure 4-11 SPI timing diagram-master mode, CPHASEL = 1 (1)



1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

4.3.15 USART characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 4-3.

Refer to section 4.3.11 I/O port characteristics for more details on the input/output alternate function characteristics (SCLK, TX, RX).

Table 4-26 USART characteristics (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
f_{SCLK} $1/t_{c(SCLK)}$	USART clock frequency	Master mode, T_A = 25°C	-	6	MHz
		Slave mode, T_A = 25°C	-	6	
$t_{r(SCLK)}$	SCLK clock rise time	Load capacitance: C = 15pF	-	6	ns
$t_{f(SCLK)}$	SCLK clock fall time	Load capacitance: C = 15pF	-	6	ns
$t_{w(SCLKH)}$ (1)	SCLK high time	-	$t_{c(SCLK)}/2$ - 6	$t_{c(SCLK)}/2$ + 6	ns
$t_{w(SCLKL)}$ (1)	SCLK low time	-	$t_{c(SCLK)}/2$ - 6	$t_{c(SCLK)}/2$ + 6	ns
$t_{su(MI)}$ (1)	Data input setup time	Master mode, f_{PCLK} = 48MHz, prescaler = 8	5	-	ns
$t_{su(SI)}$ (1)		Slave mode	5	-	ns
$t_{h(MI)}$ (1)	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler = 8	5	-	ns
$t_{h(SI)}$ (1)		Slave mode	5	-	ns
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	10	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	26	ns

1. Guaranteed by design, not tested in production.

4.3.16 ADC characteristics

Unless otherwise specified, the parameters in the table below are measured under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions summarized in Table 4-3.

Table 4-27 ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S (1)	Sampling frequency	-	-	-	1	MHz
f_{TRIG} (1)	External trigger frequency (3)	f_{ADC} = 16MHz	-	-	1	MHz
		-	-	-	16	$1/f_{ADC}$
V_{AIN} (2)	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN} (1)	External input impedance	-	See equation 2			kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	1.0	kΩ
C_{ADC} (1)	Internal sample and hold capacitance	-	-	-	5	pF
t_{STAB} (1)	Stabilization time	-	-	-	10	μs
t_{latr} (1)	Delay between trigger and conversion start	-	-	-	-	$1/f_{ADC}$
t_S (1)	Sampling time	f_{ADC} = 16MHz	0.156	-	15.031	μs
		-	2.5	-	240.5	$1/f_{ADC}$
t_{CONV} (1)	Total conversion time (including sampling time)	f_{ADC} = 16MHz	0.9375	-	15.8125	μs
		-	15 ~ 253 (sampling t_S + successive approximation 12.5)			$1/f_{ADC}$
ENOB	Effective number of bits	-	-	10.8	-	bit

1. Guaranteed based on test during characterization. Not tested in production.
2. Guaranteed by design, not tested in production.
3. In this product, VREF+ is internally connected to VDDA， VREF− is internally connected to VSSA.
4. Guaranteed by design, not tested in production.
5. For external trigger, a delay of $1/f_{ADC}$ must be added.

AIN Input impedance

Equation 2

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The formula above is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (12-bit resolution).

Table 4-28 Maximum R_{AIN} at f_{ADC} = 16MHz (1)

T_S (cycles)	t_S (μs)	Maximum R_{AIN} (kΩ)
2.5	0.156	2.2
8.5	0.531	9.9
14.5	0.906	17.7
29.5	1.844	37.0
42.5	2.656	53.7
56.5	3.531	71.8
72.5	4.531	92.4
240.5	15.031	308.8

1. Guaranteed by design. Not tested in production.

Table 4-29 ADC static parameters (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
ET	Comprehensive error	f_{PCLK1} = 48MHz, f_{ADC} = 16MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C	-3.1 ~ 3.8	LSB
EO	Offset error		-2.1 ~1.4	
EG	Gain error		-0.6 ~ 1.3	
ED	Differential linearity error		-1.0 ~ 1.6	
EL	Integral linearity error		-2.3 ~ 2.3	

1. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in section 4.2 Absolute maximum rating does not affect the ADC accuracy.
2. Guaranteed based on characterization. Not tested in production.

The implications of the ADC static parameters are seen below, and the corresponding schematic diagram is shown in Figure 4-12.

- ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.
- EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.
- EG = Gain error: The deviation between the last ideal transition and the last actual transition.
- ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.
- EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

Figure 4-12 Schematic diagram of ADC static parameters

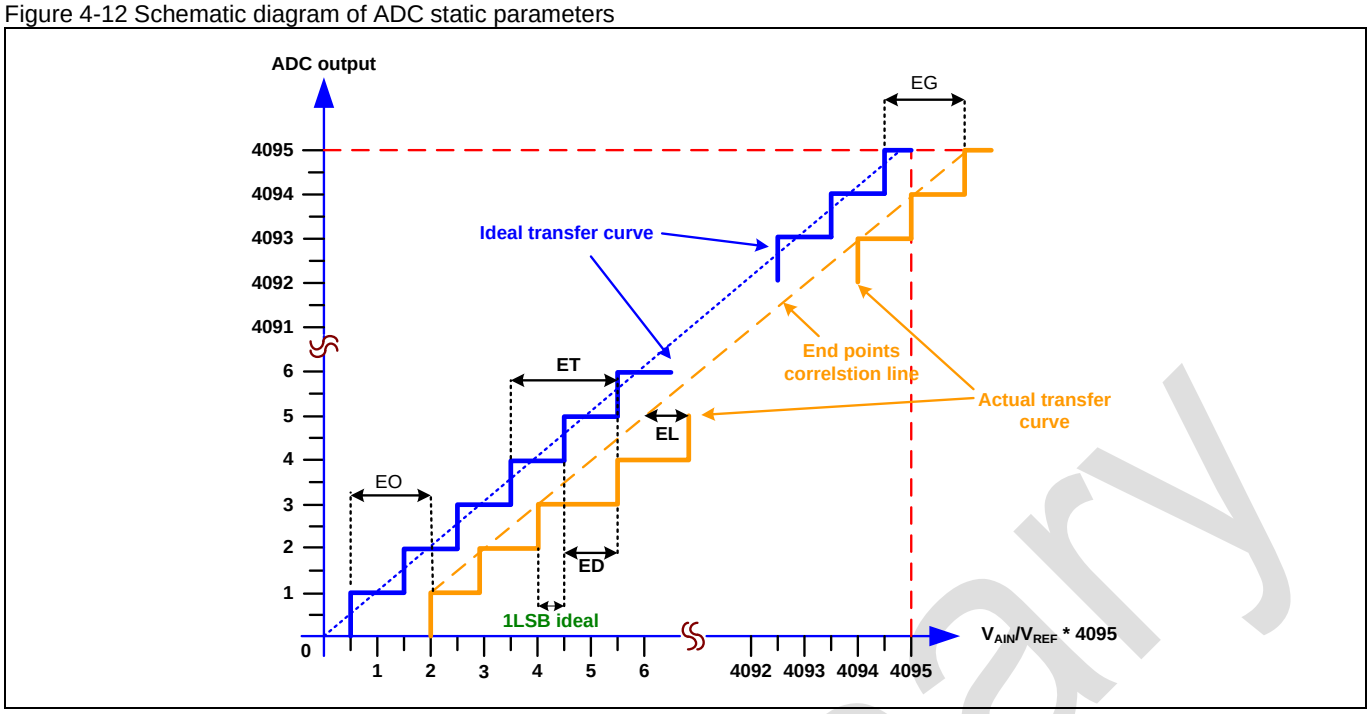
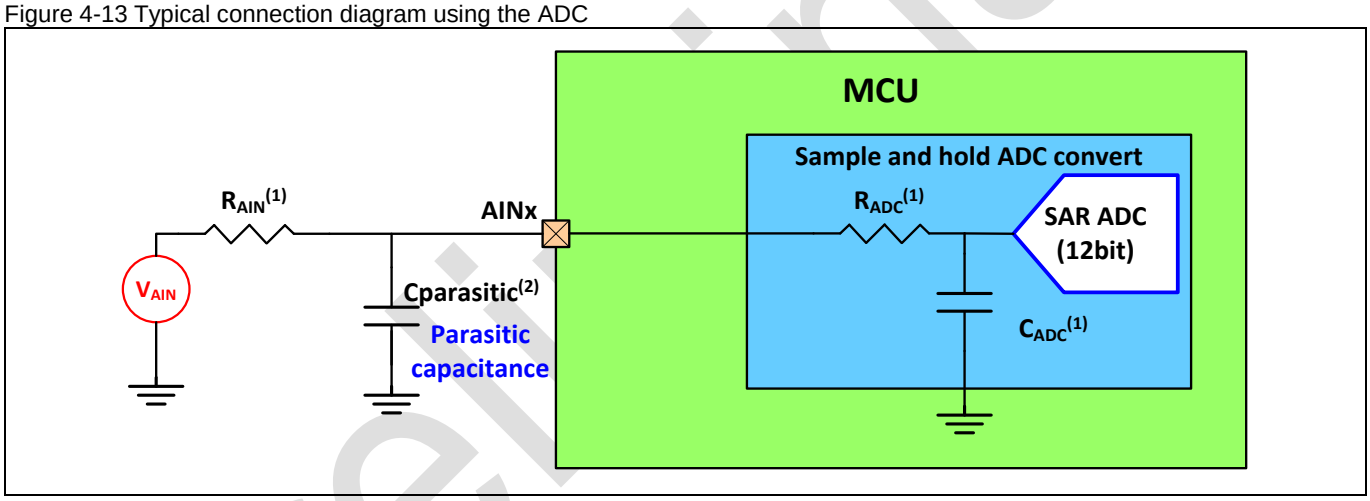


Figure 4-13 Typical connection diagram using the ADC

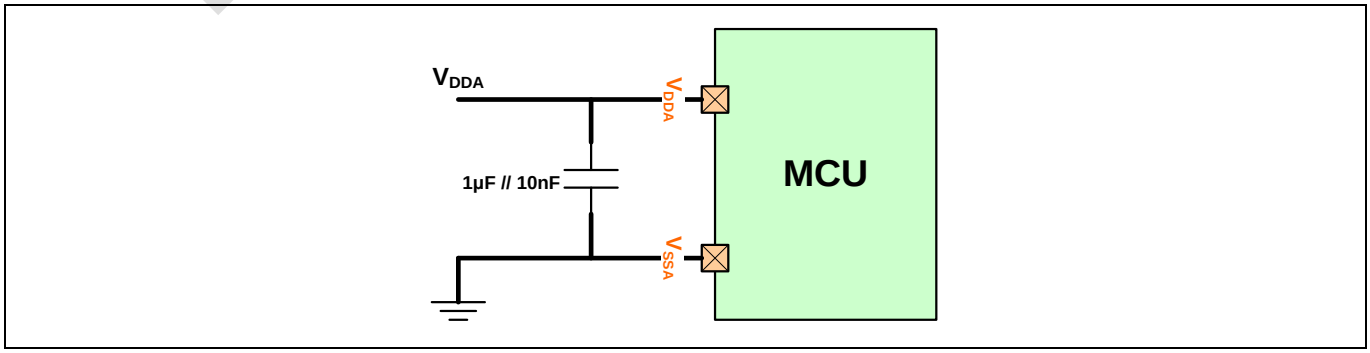


1. See Table 4-26 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply must be connected as shown below. The 10nF capacitor in the figure must be a ceramic capacitor (good quality) , and they should be as close as possible to the MCU chip.

Figure 4-14 Power supply and reference power supply decoupling circuit



4.3.17 Temperature Sensor Characteristics

The temperature is calculated by the sensor using the following formula:

Temperature Formula

$$TS_{adc} = 25 + \frac{Value * V_{DDA} - offset * 3300}{4096 * Avg\_Slope}$$

V_{DDA} : The V_{DDA} voltage during the current ADC sampling, in units of mV.
Offset : The conversion result data at 25°C, stored in Flash address 0x1FFFF7FA.
Value : The conversion result data of the current ADC sampling.
Avg_Slope : The average slope of the temperature-voltage curve (expressed in mV/°C).

Table 4-30 Temperature Sensor Characteristics (3)(4)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}	Supply voltage	2.5	3.3	5.5	V
Avg_Slope (1)	Average slope	-	-4.18	-	mV/°C
t_{S_temp} (2)	ADC sampling time when reading temperature	-	2	-	us

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The minimum sampling time can be determined by the application through multiple iterations.
4. VDD = 3.3V

4.3.18 Comparator Characteristics

Table 4-31 Comparator Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{DD}	Supply voltage	-	2.0	3.3	5.5	V
V_{CM}	Common mode range	-	0.6	-	V_{DD}-1V	V
V_{HYST}	Hysteresis	HYST = 10	44	60	90	mV
		HYST = 11	76	110	155	mV
V_{offset}	Offset	HYST = 00	-	±6	-	mV
t_{DELAY}	Propagation delay	HYST = 00	10	20	50	ns
I_q	Average working current	-	32	56	133	uA

5 Package dimensions

5.1 SSOP 28P (150mil)(10.2x5.3x175)

Figure 5-1 SSOP28 package dimension

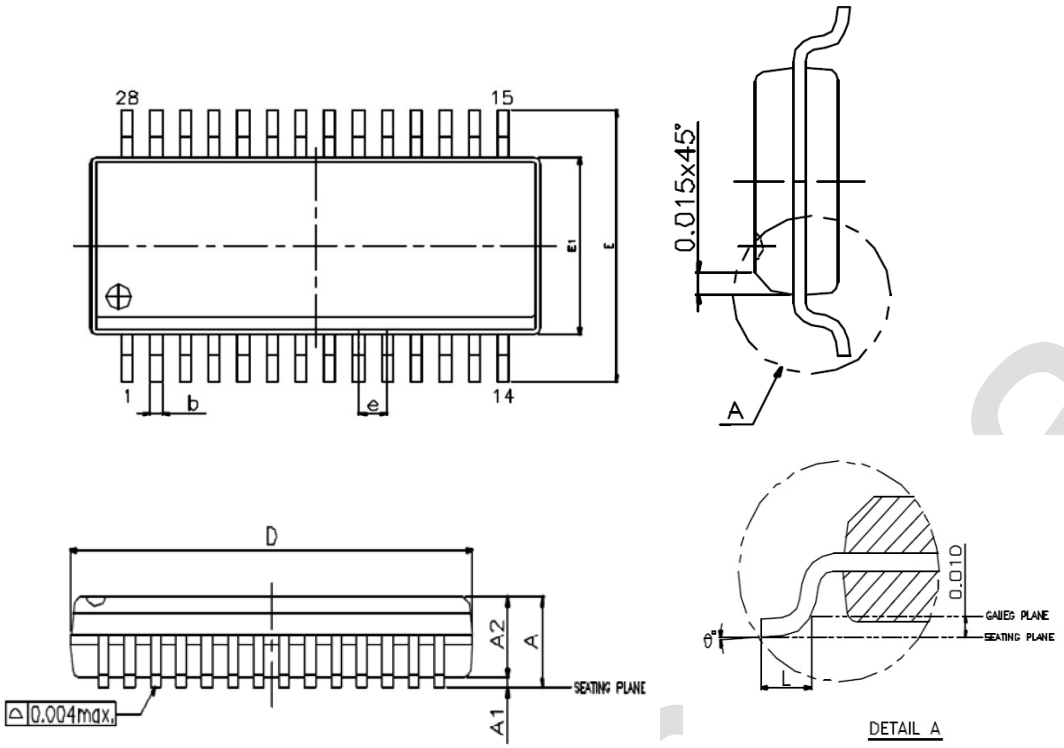


Table 5-1 SSOP28 Dimension

Unit	mm		inch	
Symbols	Min.	Max.	Min.	Max.
A	1.346	1.752	0.053	0.069
A1	0.101	0.254	0.004	0.010
A2	----	1.498	----	0.059
b	0.203	0.304	0.008	0.012
D	9.804	10.007	0.386	0.394
E1	3.810	3.987	0.150	0.157
e	0.635 BASIC		0.025 BASIC	
E	5.791	6.198	0.228	0.244
L	0.406	1.270	0.016	0.050
θ °	0	8	0°	8°

6 Revision history

Table 6-1 Revision history

Rev	Descriptions	Date
V0.01	1. Initial Version	2026/07/27

7 Disclaimers

Herein, Megawin stands for "***Megawin Technology Co., Ltd.***"

Life Support — This product is not designed for use in medical, life-saving or life-sustaining applications, or systems where malfunction of this product can reasonably be expected to result in personal injury. Customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify Megawin for any damages resulting from such improper use or sale.

Right to Make Changes — Megawin reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in mass production, relevant changes will be communicated via an Engineering Change Notification (ECN).