MG32F02N128

Data Sheet

Version: 1.11

Features

❖ CPU Core

- ARM 32-bit Cortex-M0 CPU
- Operation frequency up to 48MHz
- Built-in one NVIC for 32 external interrupt inputs with 4-level priority
- Built-in one 24-bit system tick timer
- Built-in one single-cycle 32-bit multiplier
- Built-in one SWD serial wire debugger with 2 watch points and 4 breakpoints

❖ Flash Memory

- Built-in embedded max. 128K bytes flash memory for application code
- Support ICP (In-circuit program) for ISP boot code update through SWD interface
- Support ISP (In-system program) for application code update
  - Support programmable ISP flash memory size for ISP boot code
- Support IAP (In-application program) for application data update
  - Support programmable IAP flash memory size

❖ SRAM Memory

- Built-in embedded max. 16K bytes SRAM
  - Support private 2K bytes for DMA to improve CPU access performance

❖ Power

- Built-in one embedded regulator for core logic power
- Built-in brown-out detectors
  - BOD0 detect 1.4V
  - BOD1 detect by selected level 4.2V/3.6V/2.4V/2.0V
  - BOD2 detect 1.7V
- Built-in a power management controller with power-down and wakeup control
- Support three power operation modes
  - ON(Normal) mode and SLEEP , STOP power down modes
- Support wake-up from SLEEP/STOP modes via multiple sources

❖ Reset

- Built-in embedded POR (power-on reset) circuit
- Built-in one reset source controller
  - Programmable chip cold reset and warm reset for reset source
  - Independent software reset control for internal modules
- Provide multiple reset source
  - POR/BOD/External reset pin input/Software force reset
  - IWDT/WWDT/ADC/Analog Comparator
  - Illegal address error reset/Flash access protect error reset
  - Missing clock detect (MCD) reset

❖ Clock

- Built-in embedded ILRCO (internal low frequency RC oscillator) by 32KHz
- Built-in embedded IHRCO (internal high frequency RC oscillator)
  - Trimmed to 11.059 or 12MHz ±1% at +25℃
- Built-in embedded PLL clock output for system clock
  - Programmable multiplication factor from 4 to 32
- Built-in embedded XOSC oscillator with MCD for external 32KHz and 4 ~ 25MHz Xtal
- Support external clock input up to 36MHz
- Built-in a clock source controller with independent clock enable control for modules
- Support internal XOSC oscillator and internal ILRCO/IHRCO clock output

❖ DMA (Direct Memory Access)

- 5 independently configurable channels with dedicated hardware DMA requests
  - Access to Memory, APB and AHB Peripherals as source and destination
  - Support SRAM/Flash as memory source and SRAM as memory destination
- DMA transfer management type
  - memory-to-memory (channel 0,3 only)
  - peripheral-to-memory
  - memory-to-peripheral
  - peripheral-to-peripheral
- Built-in two type of priority control between channel requests
  - Channel request by Round Robin
  - Software configurable priority level
- Programmable transfer number of data and up to 131072
- Programmable burst length 1,2,4
- Support transfer loop mode and start address auto reload control
- Provide single/block/demand mode for external pin trigger request

❖ GPIO

- Support general purpose IO pins for application
  - Maximum 73 GPIO pins for LQFP80 package
  - Maximum 59 GPIO pins for LQFP64 package
  - Maximum 44 GPIO pins for LQFP48 package
  - Maximum 29 GPIO pins for QFN32 package
- Provide selectable IO modes by pin independent
  - Push-Pull output
  - Quasi bidirectional (PC pins only)
  - Open-drain output
  - Digital Input with high impedance
  - Analog IO
- Flexible pin alternate function selection
- Support programmable drive strength by pin independent
- Support IO deglitch filter by pin independent
- Support input inverse selection by pin independent
- Support pull-high option by pin independent
- Support high speed option by pin independent except RSTN, XIN
- GPIO pin state and IO mode setting keep optional after reset

❖ Interrupt Support

- Built-in one EXIC (external interrupt controller) for NVIC connection
  - Independent high/low level and rising/falling edge trigger selection
- Built-in one WIC (wakeup interrupt controller) for wakeup event control
- All GPIO pins can be configured as interrupt source and key pad input
  - Support port OR logic for interrupt function
  - Support port AND logic for KBI function
- Support external pins for CPU NMI/RXEV/TXEV function

❖ Timer

- Provide seven timers/counters: TM00,TM01,TM10,TM16,TM20,TM26,TM36
- Timer module common functions
  - Selectable Full-counter, Cascade, Separate timer operation modes
  - Multiple internal and external signals as timer clock source or trigger source
  - Support timer reset, trigger start and clock gating for trigger source function
  - Timer overflow as clock output to external pin output

- Auto-stop mode by main counter counting

- **Provide TM36 timer module**
  - 16-bit timer with 16-bit prescaler
  - 4 CCP (input Capture/output Compare/PWM) channels
  - 3 CCP channels with OCN (complementary output compare)
  - PWM function with center/edge-align, dead time control and break control
  - QEI(Quadrature Encoder Interface) support
  - Two IC and three OC with DMA capability
  - Extra repetition counter for auto-stop mode
  - Support duty capture function
  - Up to 96MHz clock source for PWM output
- **Provide TM2x timer modules (TM20,TM26)**
  - 16-bit timer with 16-bit prescaler
  - 2 CCP (input Capture/output Compare/PWM) channels
  - 2 CCP channels with OCN (complementary output compare)
  - PWM function with edge-align
  - QEI(Quadrature Encoder Interface) support (TM26 only)
  - Extra repetition counter for auto-stop mode
  - Support duty capture function
- **Provide TM1x timer modules (TM10,TM16)**
  - 16-bit timer with 16-bit prescaler
- **Provide TM0x timer modules (TM00,TM01)**
  - 8-bit timer with 8-bit prescaler

❖ RTC

- **Built-in 32-bit counter with selectable clock source**
- **Support alarm function and time-stamp function**
- **Support wakeup from STOP mode**
- **Support periodic timer tick interrupt or wakeup**

❖ Watchdog Timer

- **Built-in one IWDT (Independent Watch Dog Timer)**
  - 8-bit down counter with 12-bit prescaler and clocked by ILRCO clock
  - Operating capability in SLEEP and STOP modes
  - Selectable reset or interrupt when the counter underflow
  - Support two early wakeup comparators with interrupt
- **Built-in one WWDT (Window Watch Dog Timer)**
  - 10-bit counter with 1 or 256 divider , 1/2/4~/128 divider
  - Configurable time-window to detect abnormally late or early application behavior
  - Selectable reset or interrupt when the counter is underflow or reloaded outside the window
  - Support warning interrupt

❖ I2C

- **Provide two identical I2c modules: I2C0 , I2C1**
- **I2C module common functions**
  - Support master and slave mode
  - Support programmable clock rate control and clock rate up to 1 MHz
  - Support programmable high/low period control for master mode
  - Support clock stretching for slave mode
  - Support general call function
  - Support multi-master processing capability
  - Support both Byte mode and Buffer mode flow control

- Support Byte mode bus event code for simplex firmware control
- Support Buffer mode 4-byte data buffer and 32-bit data register for high speed communication
- Received and transmitted data are buffered with DMA capability
- Support slave address hardware detection wakeup from STOP mode
- Support SMBus timeout detection

❖ UART

- **Provide seven UART modules: URT0~2, URT4~7**
- **UART module common functions**
  - Provide precise UART baud-rate control by programmable oversampling rate
  - Support baud rate up to 6 Mbit/s
  - Programmable data word length - 7 or 8 bits
  - Programmable 4~32 oversampling rate
  - Hardware parity checking and parity generation
  - Swappable TX/RX pin configuration
  - Separate signal polarity control for transmission and reception
- **Provide URT0/1/2 advanced UART modules**
  - Support UART, Synchronous, SPI master/slave, SmartCard, LIN, Multi-processor modes
  - Selectable MSB or LSB first data order
  - Configurable stop bits - 0.5,1,1.5 or 2 stop bits
  - Support a timeout timer for Idle/RX/Break/Calibration timeout detection
  - Support 4-byte data buffer and 32-bit data register for high speed communication
  - Support auto baud-rate detection and calibration
  - Support multiprocessor communication for master and slave mode - Idle-Line , Address-Bit
  - Support low speed UART-like frame format IrDA
  - Support transceiver hardware flow control by CTS/RTS signals only
  - Provide driver enable signal to activate the transmission for bidirectional communication
  - Support transmission-error hardware detection and auto resent control for Smart-card application
  - Support receiving parity error hardware detection and auto retry control for Smart-card application
  - Received and transmitted data are buffered with DMA capability
- **Provide URT4/5/6/7 basic UART modules**
  - Support fundamental UART mode
  - Support TX/RX independent 8-bit data register for simplex firmware control
  - Configurable stop bits - 1 or 2 stop bits

❖ SPI

- **Provide four modules for SPI communication: SPI0, URT0, URT1, URT2**
  - Provide one advanced SPI module: SPI0
  - Provide three configurable SPI modules: URT0, URT1, URT2 (Refer to UART features)
- **Support master and slave mode**
  - Support full duplex , half duplex or simplex communication mode
  - Support data communication without NSS(slave select signal)
  - Support master data input sampling delay half of SPI clock
  - Support slave data output advance half of SPI clock
- **Support programmable clock rate control**
  - Support clock rate up to 24 MHz for master/slave
- **Selectable 4~32-bit frame size**
  - Support 4-byte data buffer and 32-bit data register for high speed communication
- **Received and transmitted data are buffered with DMA capability**
- **Support multi-master processing capability**
- **Selectable clock polarity and phase**
- **Selectable MSB or LSB first data order**

- NSS line management by hardware or software for master mode
- Configurable data transfer modes
  - Standard SPI mode (separated transmit and receive line)
  - Single/Dual/Quad/Octal SPI mode with bidirectional data transfer
- Data transmit/receive overrun detect

❖ CAN

- Supports full CAN 2.0 – both 2.0A and 2.0B
  - Supports both 11-bit and 29-bit identifiers
  - Upwards compatible with the CAN FD protocol
- Supports bit rates up to 1Mbit/s
- Three transmit message buffer
  - Configurable transmit priority by request sequence or message identifier order
- Two sets of receive message FIFO
  - Three stage receive message buffer for each FIFO
  - Support one combined message FIFO from all message buffers
- Six sets of acceptance filter with identifier mask
  - Configurable Mask or List mode for each acceptance filter
  - Configurable single 32-bit filter or dual 16-bit filters for each acceptance filter
- Error manage with interrupts
- Support silent and loop-back mode for self-test operation

❖ LCD Display Driver

- Support external power input, internal VDD or internal charge pump voltage source
  - VDD voltage range 2.0V to 5.5V for internal charge pump
  - External LCD_VT voltage range 1.8V to 5.5V for external power input
  - Internal charge pump with adjustable contrast adjustment
- Embedded LCD bias reference ladder
  - LCD power rails (LCD_V1, LCD_V2, LCD_V3, LCD_VT) with external decoupling capability
  - Support external resistor ladder optional
- Provide maximum 8 common/40 segment and total 44 pins with GPIO alternate function
  - Up to drive 160 (40x4), 228 (38x6) or 288 (36x8) LCD dots
  - Support configurable common or segment for each LCD pins
  - Support hardware phase inversion
- Support Static,1/2, 1/3 and 1/4 bias voltage
- Support Static,1/2, 1/3, 1/4, 1/5, 1/6, 1/7 and 1/8 duty
- Supports Type-A or Type-B frame control mode
  - Configurable LCD frame frequency
- Embedded LCD data RAM
- Programmable dead time between frames or duty phases.
- Support LCD blinking display
- LCD start frame interrupt for LCD data RAM update
- Support LCD display on SLEEP and STOP modes

❖ ADC

- 12-bit SAR ADC with 1.5Msps
  - Configurable resolution : 12/10/8-bit
  - Configurable sampling time
- Provide external 16 channels and internal 8 channels input
  - Internal extra channel: VBUF, VSSA, LDO_VCAP, 1/4VDD, LCD_V1, OP0_P0, TS out
- Support auto-sampling and trigger by external pin, internal events and software bit
- Data alignment for output code left/right justify

- Built-in input buffer stage with bypass option
  - PGA with programmable gain : 1~128
- Optional ADC top voltage reference from external VREF+ or internal IVR24
- Interrupt generation at the end of sampling, end of conversion, end of sequence conversion
- Support voltage window detection and output code limitation
- Built-in three channel independent hardware accumulators for ADC output code
- Support one-shot/channel scan/loop scan
- ADC data are buffered with DMA capability
- Support wait mode to prevent ADC overrun

❖ Temperature Sensor

- Built-in a temperature sensor in ADC macro
- Temperature resolution : +/- 2 °C (Typical)
- Temperature operation range : -40°C ~ 125°C

❖ Analog Comparator

- Provide 2 fast comparators
- Programmable 64-step threshold of internal voltage reference
- Provide external total 6 channels input for all comparators
  - Two common and two independent external channels, two internal channels
- Programmable input hysteresis voltage
- Programmable response time for optimal current consumption
- Selectable compare output polarity
- Support wakeup from SLEEP and STOP modes
- Support analog watch dog as a reset source

❖ OPA (Operational Amplifier)

- Embedded one operational amplifier
- Provide two external inputs and one output for one OPA
  - Provide internal ADC PGA output and VBUF voltage connection
  - Support OPA output to ADC and CMP internal channel input
- Support low power mode for optimal current consumption

❖ GPL (General Purpose Logic)

- Support data inverse, bit order change, byte order change and parity check
  - Data bit order change for 8/16/32-bit reverse
  - Data byte order change between Little endian and Big endian for 16/32-bit range
  - Parity Check for 8/16/32 bit range
- Support CRC (Cyclic Redundancy Check) calculation
  - Programmable CRC initial value
  - CRC output bit order change
- CRC with fixed common polynomial
  - CRC8 polynomial 0x07
  - CRC16 polynomial 0x8005
  - CCITT16 polynomial 0x1021
  - CRC32(IEEE 802.3) polynomial 0x4C11DB7
- Input data are buffered with DMA capability

❖ Misc.

- Timer synchronous enable global control
- OBM(Output Signal Break and Modulation) control
  - Support two sets of OBM for output signal break and modulation control
- NCO(Numerically Controlled Oscillator) output with FDC and PF modes
- Support two sets of CCL(Configurable Custom Logic)
- ASB(ARGB Serial Bus) for addressable RGB LED display

- 32-bit non-reset backup register
- Provide on chip 16 bytes Unique ID code

❖ Operating

- Operating voltage range 1.8V ~ 5.5V
- Operating temperature range -40℃ ~ 105℃ (**1)
- Operating frequency range up to 48MHz

❖ Package Types

- LQFP80 / LQFP64 / LQFP48 / QFN32

(1): Tested by sampling.**

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1. General Description

The **MG32F02N** is a single-chip 32-bit microcontroller based on a high performance Core ARM® 32-bit Cortex®-M0 CPU with embedded Nested Vectored Interrupt Controller (NVIC).

The **MG32F02N** has up to **128K** bytes of embedded main flash memory for code and data, programmable memory size of embedded system flash memory for boot load code and 64 bytes of embedded option-byte flash memory for chip configuration. The all flash memory can be programmed either in serial writer mode (ICP, In-Circuit-Programming). Also, the main flash memory can be programmed in ISP (In-System Programming) mode or SRAM (Boot on SRAM) mode. ICP and ISP allow the user to download new code without removing the microcontroller from the actual end product; IAP means that the device can write non-volatile data in the flash memory while the application program is running. There needs no external high voltage for programming due to its built-in charge-pumping circuitry.

The **MG32F02N** retains all features of the ARM® 32-bit Cortex®-M0 with **16K** bytes of SRAM, **5** I/O ports, **32** external interrupts source with 4-level interrupt controller and seven 8/16-bits timer/counters. In addition, the **MG32F02N** has a System Tick Timer, two Watchdog Timers, three Advance timer modules with IC/OC, four Basic timer modules for universal using, on-chip crystal oscillator for 32.768 KHz or 4 to 25MHz, two high precision internal oscillators IHRCO for 11.059/12MHz and ILRCO for 32 KHz, one 12-bit ADC with one temperature sensor, two programmable threshold comparators and one Operational Amplifier.

Also, the **MG32F02N** support multiple and flexible communicate interface for production application. It provides alternate function pins those are including of GPIO, I2C, SPI, UART, CAN, ASB(ARGB Serial Bus), Timer with IC/PWM, ADC, Analog Comparator, NCO, CCL and SWD(on chip debug). It has maximum **73** GPIO pins and provides programmable IO type - quasi-bidirectional , push-pull output , open-drain output , input only(Hi-z) with optional pull-high. In addition, it is built-in internal de-bounce circuit to deglitch noise for worse signals.

One direct memory access (DMA) controller is used to improve data transfer between peripherals and memory and memory to memory. The data can be transfer by DMA controller and does not cost any CPU time.

One Liquid Crystal Display (LCD) controller is used to drive external STN LCD with embedded LCD data RAM and supports LCD display on SLEEP and STOP modes. It provides maximum 8 lines of common and 40 lines of segment those are total 44 pins with GPIO alternate function. It supports 1/2, 1/3, 1/4 bias voltage and 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, 1/8 duty control. The controller can operate type-A or type-B frame control mode optionally with programmable dead time between frames or duty phases. Also it supports LCD blinking display.

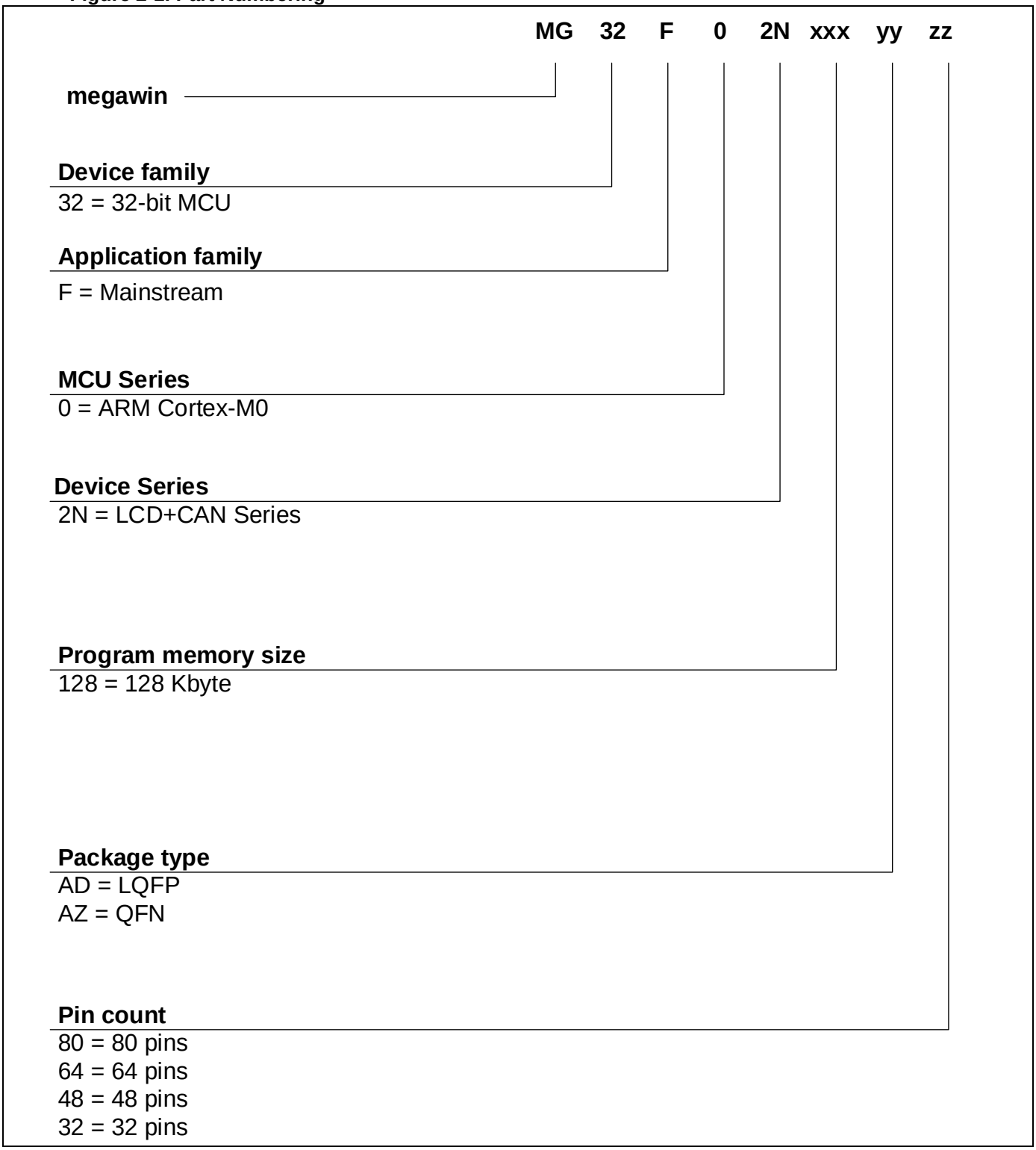
For power management and reset control, the **MG32F02N** is built-in a power supervisor including of a Low Voltage Detector(LVD), three Brown-out Detectors(BOD0/BOD1/BOD2), a Power-On Reset(POR) , a Low-voltage Reset(LVR). The **MG32F02N** has multiple power-down modes to reduce the current consumption: Sleep mode and Stop mode.

In the Sleep mode the CPU is frozen while the peripherals and the interrupt system are still operating. In the Stop mode the RAM and SFRs' value are saved and all other functions are inoperative; most importantly, in the Sleep mode the chip can be waked up by many interrupt or reset sources(POR/LVR/BOD0/BOD1/BOD2).

2. Order Information

Please contact the megawin sales for available options (memory size, package …) and more information about this device.

Figure 2-1. Part Numbering



- **Chip Selection**

Table 2-1. Chip Selection Table

Chip Functions	MG32F02N128	Comment
Flash ROM	128KB	memory space of AP+IAP+ISP
SRAM	16KB	Upper 2K-byte suggestion for DMA
Package	LQFP80/64; LQFP64/48; QFN32	
IO Number	73/59; 59/44; 29	IO number by package
Max. CPU Frequency	48MHz	
Internal Clock Source	ILRCO+IHRCO	12MHz(default) & 11.059MHz option for IHRCO
Voltage Detector	LVR+BOD0/1/2	Low Voltage Reset (LVR), BOD1: 4.2/3.7/2.4/2.0V, BOD2: 1.7V
Timers	16-bit*2: TM00/01 32-bit*5: TM1x/2x/36	support Full-Counter, Cascade , Separate modes
IC/OC/PWM Channels	8-CH (16-bit) or 16-CH(8-bit)	IC: Input Capture, OC: Output Compare (support normal + complement output)
WDT	IWDT+WWDT	IWDT: Independent Watch Dog Timer, WWDT: System Window Watch Dog Timer
RTC	32-Bit	
ADC	12-Bit , 16-CH 1.5Msps	at room temperature
ACMP Units	2	fast rail-to-rail analog comparators with two R-ladder voltage reference
OPA Units	1	
I2C Units	2	optional Byte/Buffer mode, with/without clock stretching
UART Units	Advanced *3 Basic *4	URT0~3 can configurable to UART, Multi-processor, SPI, IrDA, LIN, ISO-7816 (SmartCard) and support Hardware flow control; URT4~7 are basic UART.
UART as SPI	Master/Slave *3	configurable and shared in advanced UART module
UART SPI mode Max. Clock Rate (3.3V/1.8V)	Master: 18/16 MHz Slave: 12/12 MHz	VDD (5~3.3V / 3.3~1.8V)
SPI Units	1	master/slave mode with or without NSS control
SPI Max. Clock Rate (3.3V/1.8V)	Master: 24/16 MHz Slave: 16/12 MHz	VDD (5~3.3V / 3.3~1.8V)
CAN Units	CAN 2.0 A/B 1Mbit/s *1	
CAN Message Buffer	TX *3/ RX *6	
CAN Acceptance Filter	6	
LCD	Configurable 44 Pins COM or SEG	4COM*40SEG, 6COM*38SEG, 8COM*36SEG
LCD Duty	Static, 1/2, 1/3, 1/4, 1/8	
LCD Bias	Static, 1/2, 1/3, 1/4	
LCD Power	VDD, CP, EXT	CP: Charge Pump
DMA Channels	5-CH	single/block/demand mode for external pin trigger
CRC	CRC8+16+32	CRC8/CRC16/CCITT16/CRC32 fixed polynomial
OBM Units	2	Output Signal Break and Modulation
NCO Units	1	numerically controlled oscillator, Output frequency <= 1/2 Input frequency
CCL Units	2	configurable custom logic
ASB Units	4-CH	ARGB LED serial bus
Operation Voltage	1.8~5.5V	
Operating Temperature	-40~105°C	test by sampling
Flash Regions	AP,IAP,ISP	Application flash, In-Application-Programming data flash, In-System-Programming flash (ISPD: In-System-Programming data flash)

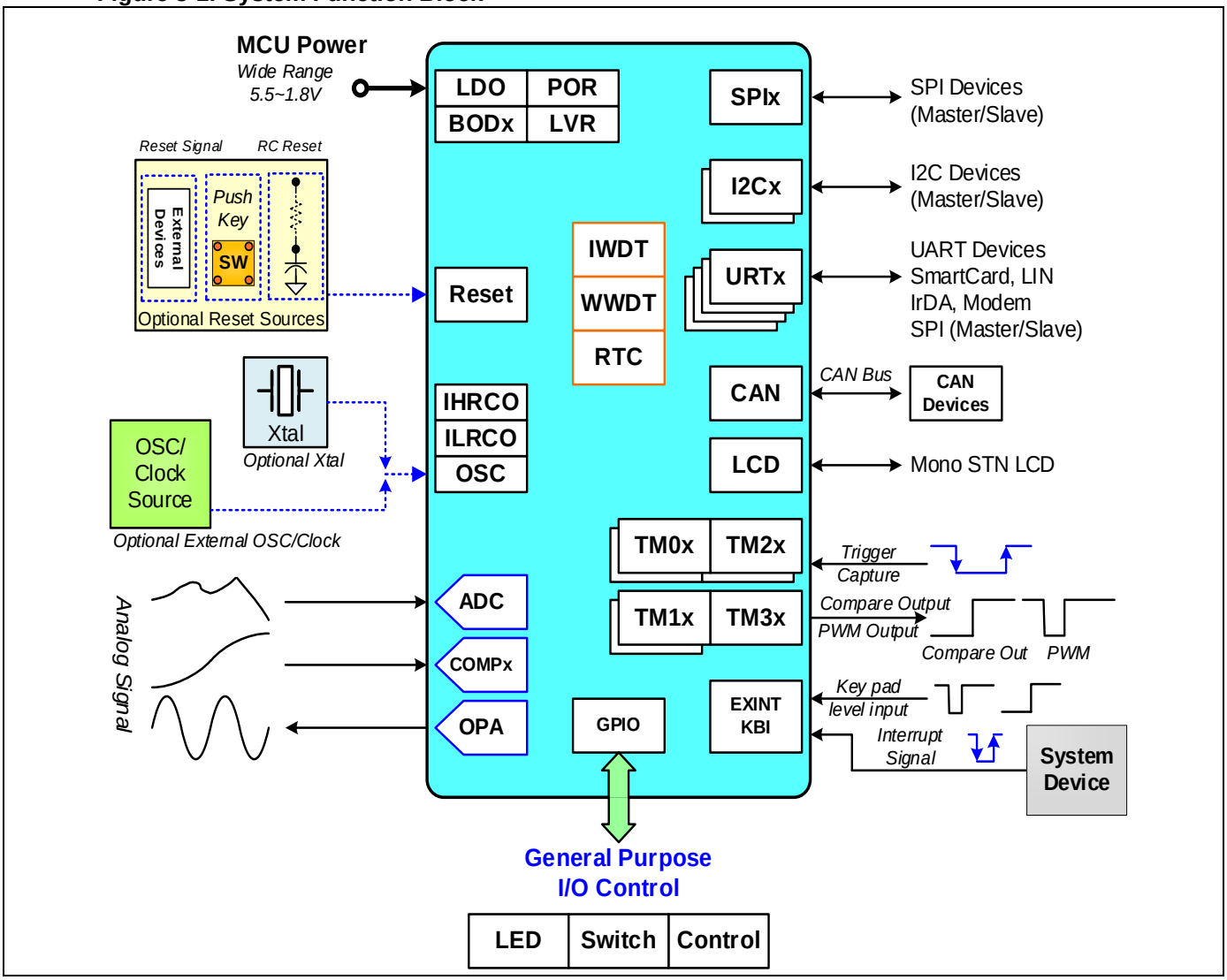
- **Part Number List**
  - **MG32F02N128AD80 : LQFP80 (10mm x 10mm), 128KB Flash**
  - **MG32F02N128AD64 : LQFP64 (7mm x 7mm), 128KB Flash**
  - **MG32F02N128AD48 : LQFP48 (7mm x 7mm), 128KB Flash**
  - **MG32F02N128AZ32 : QFN32 (4mm x 4mm), 128KB Flash**

3. Block Diagram

3.1. System Function Block

The following diagram is showing the system function block for application.

Figure 3-1. System Function Block

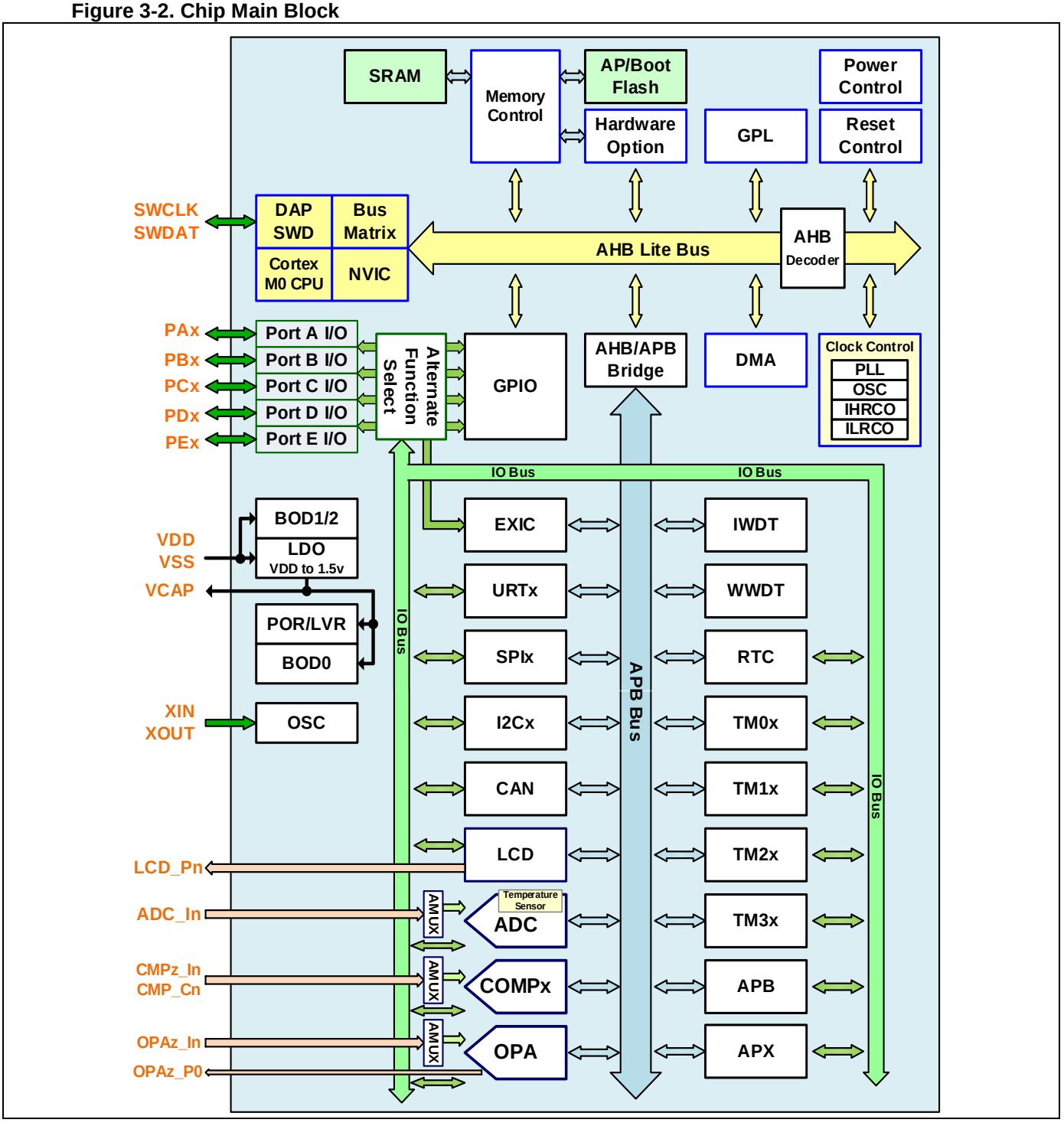


3.2. Chip Main Block

The following diagram is showing the block of internal devices in the chip.

There are one embedded ARM® Cortex®-M0 processor with NVIC (Nested Vectored Interrupt Controller) and DAP (Debug Access Port); AHB lite bus with SRAM/Flash memory, Power/Reset/Clock system controllers, Liquid Crystal Display (LCD) controller, GPIO control blocks and GPL (General Purpose Logic); APB bus with UART / SPI / I2C / CAN communication controllers, timers of general timer / IWDT / WWDT / RTC and analog control block of ADC / analog comparators / Operational Amplifier; analog devices of POR (power on reset), BOD0/BOD1/BOD2 (Brown-Out Detectors), ILRCO (Internal Low-frequency RC Oscillator)/IHRCO Internal High-frequency RC Oscillator)/PLL.

Figure 3-2. Chip Main Block



4. Pin Description

4.1. Pin Outline

4.1.1. LQFP80 Package Pinout

Figure 4-1. LQFP80 Package Pinout

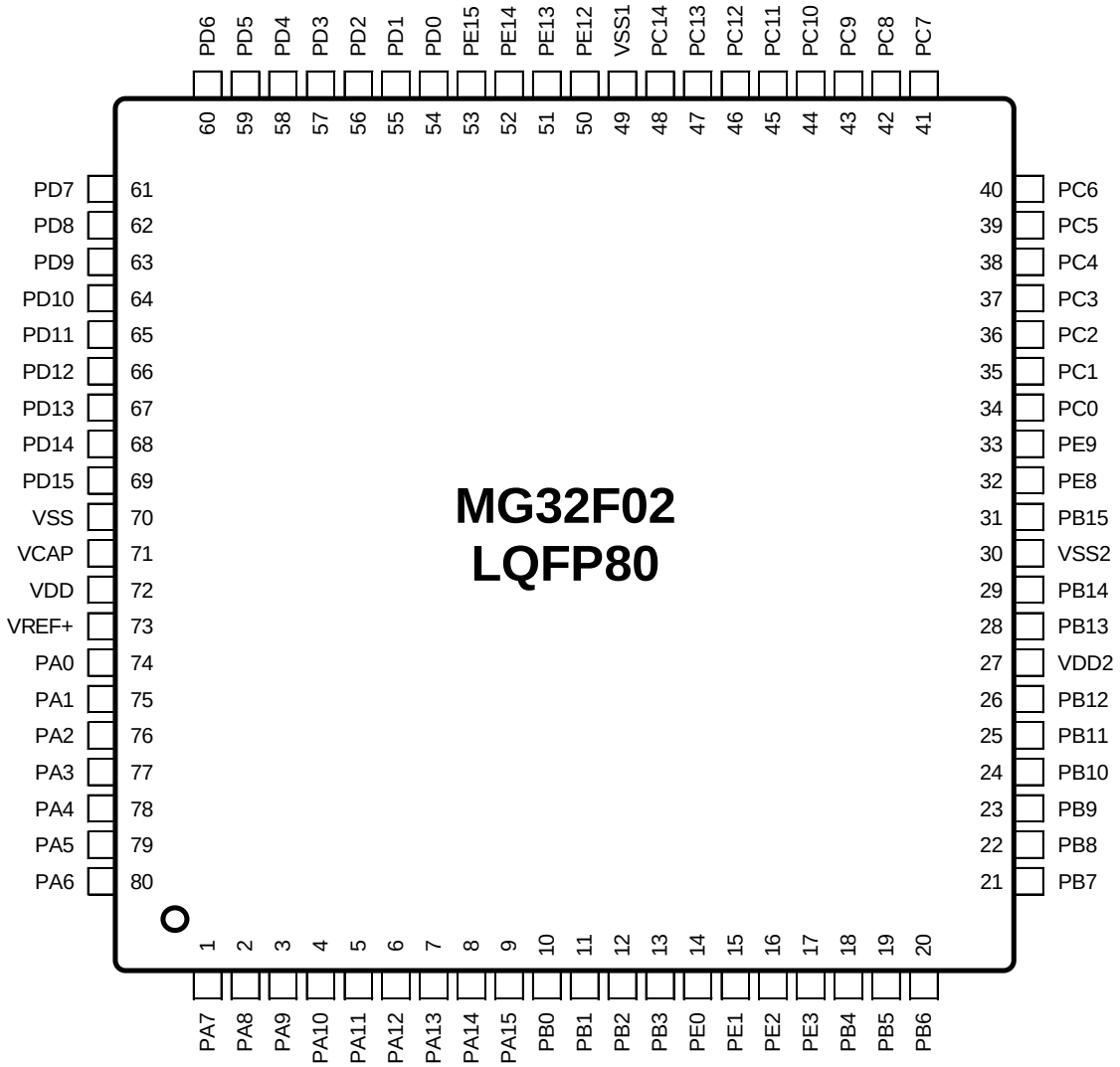


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Table 4-1. LQFP80 Pin AFS List

Pin	Name	Pin AFS List	Analog Function
1	PA7	GPA7, ASB_P3, SPI0_D2, TM20_OC1H, URT0_NSS, LCD_P6	ADC_I7
2	PA8	GPA8, DMA_TRG0, ASB_P0, I2C0_SCL, URT2_BRO, SDT_I0, TM20_IC0, SPI0_NSS, TM36_OC0H, URT4_TX, LCD_P7	ADC_I8, CMP0_I0, VBG_OUT
3	PA9	GPA9, DMA_TRG1, ASB_P1, I2C1_SCL, URT2_TMO, ASB_CK0, TM20_IC1, SPI0_MISO, TM36_OC1H, URT5_TX, LCD_P8	ADC_I9, CMP0_I1
4	PA10	GPA10, TM36_BK0, SPI0_D2, I2C0_SDA, URT2_CTS, SDT_I1, TM26_IC0, SPI0_CLK, TM36_OC2H, URT4_RX, LCD_P9	ADC_I10, CMP1_I0
5	PA11	GPA11, SPI0_D3, I2C1_SDA, URT2_RTS, TM20_OC1N, TM26_IC1, SPI0_MOSI, TM36_OC3H, URT5_RX, LCD_P10	ADC_I11, CMP1_I1
6	PA12	GPA12, MF_S0, URT1_BRO, TM10_ETR, TM36_IC0, SPI0_D5, TM26_OC00, URT6_TX, LCD_P11	ADC_I12

7	PA13	GPA13, CPU_TXEV, MF_S1, URT0_BRO, URT1_TMO, TM10_TRGO, TM36_IC1, SPI0_D6, TM26_OC10, URT6_RX, LCD_P12	ADC_I13, ADC_PGA
8	PA14	GPA14, CPU_RXEV, OBM_I0, URT0_TMO, URT1_CTS, TM16_ETR, TM36_IC2, SPI0_D7, TM26_OC0H, URT7_TX, LCD_P13	ADC_I14
9	PA15	GPA15, CPU_NMI, OBM_I1, URT0_DE, URT1_RTS, TM16_TRGO, TM36_IC3, SPI0_D4, TM26_OC1H, URT7_RX, LCD_P14	ADC_I15
10	PB0	GPB0, I2C1_SCL, SPI0_NSS, TM01_ETR, TM00_CKO, TM16_ETR, TM26_IC0, TM36_ETR, URT1_NSS, URT2_NSS, URT6_TX, LCD_P15	CMP_C0
11	PB1	GPB1, I2C1_SDA, SPI0_MISO, TM01_TRGO, TM10_CKO, TM16_TRGO, TM26_IC1, TM36_TRGO, TM00_TRGO, URT1_RX, URT2_CLK, URT6_RX, LCD_P16	CMP_C1
12	PB2	GPB2, ADC0_TRG, SPI0_CLK, TM01_CKO, URT2_TX, TM16_CKO, TM26_OC0H, I2C0_SDA, TM10_TRGO, URT1_CLK, URT0_TX, URT7_TX, LCD_P17	
13	PB3	GPB3, ADC0_OUT, SPI0_MOSI, NCO_P0, URT2_RX, TM36_CKO, TM26_OC1H, I2C0_SCL, TM20_TRGO, URT1_TX, URT0_RX, URT7_RX, LCD_P18	
14	PE0	GPE0, OBM_I0, URT0_TX, SPI0_NSS, TM20_OC00, TM26_OC00, URT4_TX	
15	PE1	GPE1, OBM_I1, URT0_RX, DMA_TRG1, SPI0_MISO, TM20_OC01, TM26_OC01, TM36_OC0H, URT4_RX	
16	PE2	GPE2, OBM_P0, I2C1_SCL, URT1_TX, NCO_P0, SPI0_CLK, TM20_OC02, TM26_OC02, TM36_OC1H, URT5_TX	
17	PE3	GPE3, OBM_P1, I2C1_SDA, URT1_RX, NCO_CK0, SPI0_MOSI, TM20_OC0N, TM26_OC0N, URT5_RX	
18	PB4	GPB4, TM01_CKO, SPI0_D3, TM26_TRGO, URT2_CLK, TM20_IC0, TM36_IC0, LCD_P19	
19	PB5	GPB5, TM16_CKO, SPI0_D2, TM26_ETR, URT2_NSS, TM20_IC1, TM36_IC1, LCD_P20	
20	PB6	GPB6, CPU_RXEV, SPI0_NSSI, URT0_BRO, URT2_CTS, TM20_ETR, TM36_IC2, CAN0_TX, URT2_TX, LCD_P21	
21	PB7	GPB7, CPU_TXEV, URT0_TMO, URT2_RTS, TM20_TRGO, TM36_IC3, CAN0_RX, URT2_RX, LCD_P22	
22	PB8	GPB8, CMP0_P0, RTC_OUT, URT0_TX, URT2_BRO, TM20_OC01, TM36_OC01, SPI0_D3, SDT_P0, OBM_P0, URT4_TX	
23	PB9	GPB9, CMP1_P0, RTC_TS, URT0_RX, URT2_TMO, TM20_OC02, TM36_OC02, SPI0_D2, OBM_P1, URT4_RX	
24	PB10	GPB10, I2C0_SCL, URT0_NSS, URT2_DE, TM20_OC11, TM36_OC11, URT1_TX, SPI0_NSSI, TM00_ETR, LCD_P23	
25	PB11	GPB11, I2C0_SDA, URT0_DE, IR_OUT, TM20_OC12, TM36_OC12, URT1_RX, DMA_TRG0, URT0_CLK, LCD_P24	
26	PB12	GPB12, DMA_TRG0, NCO_P0, MF_S0, ASB_P0, URT1_CLK, URT5_TX, LCD_P25	
27	VDD2		
28	PB13	GPB13, TM00_ETR, URT0_CTS, TM20_ETR, TM36_ETR, URT0_CLK, CCL_P0, URT4_RX, LCD_P26	
29	PB14	GPB14, DMA_TRG0, TM00_TRGO, URT0_RTS, TM20_TRGO, TM36_BK0, URT0_NSS, CCL_P1, URT4_TX, LCD_P27	
30	VSS2		
31	PB15	GPB15, IR_OUT, NCO_CK0, MF_S1, ASB_P1, URT1_NSS, URT2_NSS, URT5_RX, LCD_P28	
32	PE8	GPE8, CPU_TXEV, OBM_I0, URT2_TX, SDT_I0, TM36_CKO, TM20_CKO, TM26_CKO, SPI0_D3, URT4_TX	
33	PE9	GPE9, CPU_RXEV, OBM_I1, URT2_RX, SDT_I1, TM36_TRGO, TM20_TRGO, TM26_TRGO, SPI0_D2, URT4_RX	
34	PC0	GPC0, ICKO, TM00_CKO, URT0_CLK, URT2_CLK, TM20_OC00, TM36_OC00, I2C0_SCL, URT0_TX, URT5_TX, TM36_IC0	
35	PC1	GPC1, ADC0_TRG, TM01_CKO, TM36_IC0, URT1_CLK, TM20_OC0N, TM36_OC0N, I2C0_SDA, URT0_RX, URT5_RX, LCD_P29	
36	PC2	GPC2, ADC0_OUT, TM10_CKO, OBM_P0, URT2_CLK, TM20_OC10, TM36_OC10, SDT_I0, MF_S0, LCD_P30	
37	PC3	GPC3, OBM_P1, TM16_CKO, URT0_CLK, URT1_CLK, TM20_OC1N, TM36_OC1N, SDT_I1, MF_S1, LCD_P31	
38	PC4	GPC4, SWCLK, I2C0_SCL, URT0_RX, URT1_RX, TM36_IC2, TM36_OC2, SDT_I0, SDT_P0, URT6_RX	
39	PC5	GPC5, SWDIO, I2C0_SDA, URT0_TX, URT1_TX, TM36_IC3, TM36_OC3, SDT_I1, URT6_TX	
40	PC6	GPC6, RSTN, RTC_TS, URT0_NSS, URT1_NSS, TM20_ETR, TM26_ETR, TM36_OC1N	
41	PC7	GPC7, ADC0_TRG, RTC_OUT, URT0_DE, URT1_NSS, ASB_P2, TM36_TRGO, LCD_P32	
42	PC8	GPC8, ADC0_OUT, I2C0_SCL, URT0_BRO, URT1_TX, TM20_OC0H, TM36_OC0H, TM36_OC0N, CCL_P0, URT6_TX, LCD_P33	
43	PC9	GPC9, CMP0_P0, I2C0_SDA, URT0_TMO, URT1_RX, TM20_OC1H, TM36_OC1H, TM36_OC1N, CCL_P1, URT6_RX, LCD_P34	
44	PC10	GPC10, CMP1_P0, I2C1_SCL, URT0_TX, URT2_TX, URT1_TX, TM36_OC2H, TM36_OC2N, CAN0_TX, URT7_TX, LCD_P35	
45	PC11	GPC11, I2C1_SDA, URT0_RX, URT2_RX, URT1_RX, TM36_OC3H, TM26_OC01, CAN0_RX, URT7_RX, LCD_P36	
46	PC12	GPC12, IR_OUT, URT1_DE, TM10_TRGO, TM36_OC3, TM26_OC02, SDT_P0, URT1_CLK, LCD_P37	
47	PC13	GPC13, XIN, URT1_NSS, URT0_CTS, URT2_RX, TM10_ETR, TM26_ETR, TM36_OC00, TM20_IC0, SDT_I0, TM36_IC1, URT6_RX	
48	PC14	GPC14, XOUT, URT1_TMO, URT0_RTS, URT2_TX, TM10_CKO, TM26_TRGO, TM36_OC10, TM20_IC1, SDT_I1, SDT_P0, URT6_TX	
49	VSS1		
50	PE12	GPE12, ADC0_TRG, MF_S0, TM01_CKO, TM16_CKO, TM20_OC10, TM26_OC10, URT6_TX	
51	PE13	GPE13, ADC0_OUT, MF_S1, TM01_TRGO, TM16_TRGO, TM20_OC11, TM26_OC11, TM36_OC2H, URT6_RX	

52	**PE14**	GPE14, RTC_OUT, I2C1_SCL, CAN0_TX, TM01_ETR, TM16_ETR, TM20_OC12, TM26_OC12, CCL_P0, TM36_OC3H, URT7_TX	
53	**PE15**	GPE15, RTC_TS, I2C1_SDA, CAN0_RX, TM36_BK0, TM36_ETR, TM20_OC1N, TM26_OC1N, CCL_P1, URT7_RX	
54	**PD0**	GPD0, OBM_I0, TM10_CKO, URT0_CLK, TM26_OC1N, TM20_CKO, TM36_OC2, SPI0_NSS, TM36_IC3, URT2_NSS	LCD_C1
55	**PD1**	GPD1, OBM_I1, TM16_CKO, URT0_CLK, NCO_CK0, TM26_CKO, TM36_OC2N, SPI0_CLK, TM36_IC2, URT2_CLK	LCD_C2
56	**PD2**	GPD2, MF_S0, TM00_CKO, URT1_CLK, TM26_OC00, TM20_CKO, TM36_CKO, SPI0_MOSI, TM36_IC1, URT2_TX	LCD_VT
57	**PD3**	GPD3, MF_S1, TM01_CKO, URT1_CLK, SPI0_MISO, TM26_CKO, SPI0_D3, TM36_TRGO, URT2_RX	LCD_V1
58	**PD4**	GPD4, TM00_TRGO, TM01_TRGO, URT1_TX, TM26_OC00, SPI0_D2, URT2_TX, LCD_P38	
59	**PD5**	GPD5, TM00_ETR, I2C0_SCL, URT1_RX, TM26_OC01, SPI0_MISO, URT2_RX, LCD_P39	
60	**PD6**	GPD6, CPU_NMI, I2C0_SDA, URT1_NSS, SPI0_NSSI, TM26_OC02, SPI0_NSS, SDT_P0, URT2_NSS, LCD_P40	
61	**PD7**	GPD7, TM00_CKO, TM01_ETR, URT1_DE, SPI0_MISO, TM26_OC0N, SPI0_D4, TM36_IC0, TM36_OC3	LCD_V2
62	**PD8**	GPD8, CPU_TXEV, TM01_TRGO, URT1_RTS, SPI0_D2, TM26_OC10, SPI0_D7, TM36_IC1, SPI0_CLK, LCD_P41	
63	**PD9**	GPD9, CPU_RXEV, TM00_TRGO, URT1_CTS, SPI0_NSSI, TM26_OC11, SPI0_D6, TM36_IC2, SPI0_NSS	LCD_V3
64	**PD10**	GPD10, CPU_NMI, TM00_ETR, URT1_BRO, RTC_OUT, TM26_OC12, SPI0_D5, TM36_IC3, SPI0_MOSI, LCD_P42	
65	**PD11**	GPD11, CPU_NMI, DMA_TRG1, URT1_TMO, SPI0_D3, TM26_OC1N, SPI0_NSS, ASB_P3, LCD_P43	
66	**PD12**	GPD12, CMP0_P0, TM10_CKO, OBM_P0, TM00_CKO, SPI0_CLK, TM20_OC0H, TM26_OC0H, URT1_CLK, URT2_CLK	
67	**PD13**	GPD13, CMP1_P0, TM10_TRGO, OBM_P1, TM00_TRGO, NCO_CK0, TM20_OC1H, TM26_OC1H, ASB_P0	
68	**PD14**	GPD14, TM10_ETR, TM00_ETR, TM36_OC2, TM20_IC0, TM26_IC0, CCL_P0, URT5_TX	
69	**PD15**	GPD15, NCO_P0, IR_OUT, DMA_TRG0, TM36_OC3, TM20_IC1, TM26_IC1, CCL_P1, URT5_RX	
70	**VSS**		
71	**VCAP**		
72	**VDD**		
73	**VREF+**		
74	**PA0**	GPA0, ASB_P0, NCO_P0, TM20_CKO, SDT_P0, CCL_P0, TM36_OC00, URT4_TX	ADC_I0, OP0_P0
75	**PA1**	GPA1, CPU_NMI, ASB_P1, NCO_CK0, URT1_BRO, TM20_OC10, CCL_P1, TM36_OC10, URT4_RX, LCD_P0	ADC_I1
76	**PA2**	GPA2, CPU_RXEV, ASB_P2, ASB_CK0, URT1_CTS, CAN0_TX, SDT_I0, SPI0_CLK, TM36_OC2, URT5_TX, LCD_P1	ADC_I2
77	**PA3**	GPA3, CPU_TXEV, ASB_P3, ASB_CK1, URT1_RTS, CAN0_RX, SDT_I1, SPI0_MOSI, TM36_OC2N, URT5_RX, LCD_P2	ADC_I3
78	**PA4**	GPA4, ASB_CK0, TM20_OC00, URT0_TX, LCD_P3	ADC_I4, OP0_I0
79	**PA5**	GPA5, ASB_CK1, TM20_OC10, URT0_RX, LCD_P4	ADC_I5, OP0_I1
80	**PA6**	GPA6, ASB_P2, SPI0_D3, TM20_OC0H, URT0_CLK, LCD_P5	ADC_I6

4.1.2. LQFP64 Package Pinout

Figure 4-2. LQFP64 Package Pinout

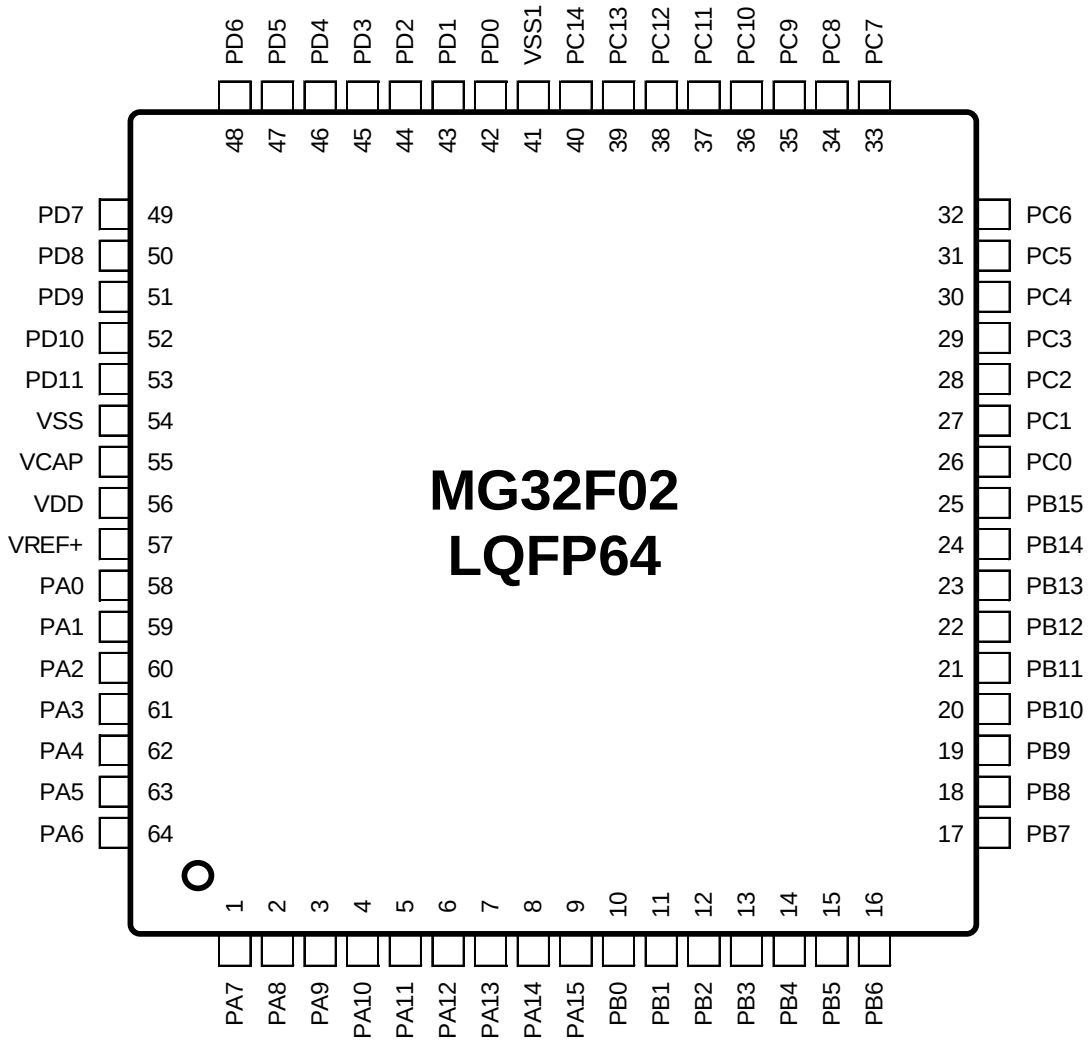

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Table 4-2. LQFP64 Pin AFS List

Pin	Name	Pin AFS List	Analog Function
1	PA7	GPA7, ASB_P3, SPI0_D2, TM20_OC1H, URT0_NSS, LCD_P6	ADC_I7
2	PA8	GPA8, DMA_TRG0, ASB_P0, I2C0_SCL, URT2_BRO, SDT_I0, TM20_IC0, SPI0_NSS, TM36_OC0H, URT4_TX, LCD_P7	ADC_I8, CMP0_I0, VBG_OUT
3	PA9	GPA9, DMA_TRG1, ASB_P1, I2C1_SCL, URT2_TMO, ASB_CK0, TM20_IC1, SPI0_MISO, TM36_OC1H, URT5_TX, LCD_P8	ADC_I9, CMP0_I1
4	PA10	GPA10, TM36_BK0, SPI0_D2, I2C0_SDA, URT2_CTS, SDT_I1, TM26_IC0, SPI0_CLK, TM36_OC2H, URT4_RX, LCD_P9	ADC_I10, CMP1_I0
5	PA11	GPA11, SPI0_D3, I2C1_SDA, URT2_RTS, TM20_OC1N, TM26_IC1, SPI0_MOSI, TM36_OC3H, URT5_RX, LCD_P10	ADC_I11, CMP1_I1
6	PA12	GPA12, MF_S0, URT1_BRO, TM10_ETR, TM36_IC0, SPI0_D5, TM26_OC00, URT6_TX, LCD_P11	ADC_I12
7	PA13	GPA13, CPU_TXEV, MF_S1, URT0_BRO, URT1_TMO, TM10_TRGO, TM36_IC1, SPI0_D6, TM26_OC10, URT6_RX, LCD_P12	ADC_I13, ADC_PGA
8	PA14	GPA14, CPU_RXEV, OBM_I0, URT0_TMO, URT1_CTS, TM16_ETR, TM36_IC2, SPI0_D7, TM26_OC0H, URT7_TX, LCD_P13	ADC_I14
9	PA15	GPA15, CPU_NMI, OBM_I1, URT0_DE, URT1_RTS, TM16_TRGO, TM36_IC3, SPI0_D4, TM26_OC1H, URT7_RX, LCD_P14	ADC_I15

10	**PB0**	GPB0, I2C1_SCL, SPI0_NSS, TM01_ETR, TM00_CKO, TM16_ETR, TM26_IC0, TM36_ETR, URT1_NSS, URT2_NSS, URT6_TX, LCD_P15	CMP_C0
11	**PB1**	GPB1, I2C1_SDA, SPI0_MISO, TM01_TRGO, TM10_CKO, TM16_TRGO, TM26_IC1, TM36_TRGO, TM00_TRGO, URT1_RX, URT2_CLK, URT6_RX, LCD_P16	CMP_C1
12	**PB2**	GPB2, ADC0_TRG, SPI0_CLK, TM01_CKO, URT2_TX, TM16_CKO, TM26_OC0H, I2C0_SDA, TM10_TRGO, URT1_CLK, URT0_TX, URT7_TX, LCD_P17	
13	**PB3**	GPB3, ADC0_OUT, SPI0_MOSI, NCO_P0, URT2_RX, TM36_CKO, TM26_OC1H, I2C0_SCL, TM20_TRGO, URT1_TX, URT0_RX, URT7_RX, LCD_P18	
14	**PB4**	GPB4, TM01_CKO, SPI0_D3, TM26_TRGO, URT2_CLK, TM20_IC0, TM36_IC0, LCD_P19	
15	**PB5**	GPB5, TM16_CKO, SPI0_D2, TM26_ETR, URT2_NSS, TM20_IC1, TM36_IC1, LCD_P20	
16	**PB6**	GPB6, CPU_RXEV, SPI0_NSSI, URT0_BRO, URT2_CTS, TM20_ETR, TM36_IC2, CAN0_TX, URT2_TX, LCD_P21	
17	**PB7**	GPB7, CPU_TXEV, URT0_TMO, URT2_RTS, TM20_TRGO, TM36_IC3, CAN0_RX, URT2_RX, LCD_P22	
18	**PB8**	GPB8, CMP0_P0, RTC_OUT, URT0_TX, URT2_BRO, TM20_OC01, TM36_OC01, SPI0_D3, SDT_P0, OBM_P0, URT4_TX	
19	**PB9**	GPB9, CMP1_P0, RTC_TS, URT0_RX, URT2_TMO, TM20_OC02, TM36_OC02, SPI0_D2, OBM_P1, URT4_RX	
20	**PB10**	GPB10, I2C0_SCL, URT0_NSS, URT2_DE, TM20_OC11, TM36_OC11, URT1_TX, SPI0_NSSI, TM00_ETR, LCD_P23	
21	**PB11**	GPB11, I2C0_SDA, URT0_DE, IR_OUT, TM20_OC12, TM36_OC12, URT1_RX, DMA_TRG0, URT0_CLK, LCD_P24	
22	**PB12**	GPB12, DMA_TRG0, NCO_P0, MF_S0, ASB_P0, URT1_CLK, URT5_TX, LCD_P25	
23	**PB13**	GPB13, TM00_ETR, URT0_CTS, TM20_ETR, TM36_ETR, URT0_CLK, CCL_P0, URT4_RX, LCD_P26	
24	**PB14**	GPB14, DMA_TRG0, TM00_TRGO, URT0_RTS, TM20_TRGO, TM36_BK0, URT0_NSS, CCL_P1, URT4_TX, LCD_P27	
25	**PB15**	GPB15, IR_OUT, NCO_CK0, MF_S1, ASB_P1, URT1_NSS, URT2_NSS, URT5_RX, LCD_P28	
26	**PC0**	GPC0, ICKO, TM00_CKO, URT0_CLK, URT2_CLK, TM20_OC00, TM36_OC00, I2C0_SCL, URT0_TX, URT5_TX, TM36_IC0	
27	**PC1**	GPC1, ADC0_TRG, TM01_CKO, TM36_IC0, URT1_CLK, TM20_OC0N, TM36_OC0N, I2C0_SDA, URT0_RX, URT5_RX, LCD_P29	
28	**PC2**	GPC2, ADC0_OUT, TM10_CKO, OBM_P0, URT2_CLK, TM20_OC10, TM36_OC10, SDT_I0, MF_S0, LCD_P30	
29	**PC3**	GPC3, OBM_P1, TM16_CKO, URT0_CLK, URT1_CLK, TM20_OC1N, TM36_OC1N, SDT_I1, MF_S1, LCD_P31	
30	**PC4**	GPC4, SWCLK, I2C0_SCL, URT0_RX, URT1_RX, TM36_IC2, TM36_OC2, SDT_I0, SDT_P0, URT6_RX	
31	**PC5**	GPC5, SWDIO, I2C0_SDA, URT0_TX, URT1_TX, TM36_IC3, TM36_OC3, SDT_I1, URT6_TX	
32	**PC6**	GPC6, RSTN, RTC_TS, URT0_NSS, URT1_NSS, TM20_ETR, TM26_ETR, TM36_OC1N	
33	**PC7**	GPC7, ADC0_TRG, RTC_OUT, URT0_DE, URT1_NSS, ASB_P2, TM36_TRGO, LCD_P32	
34	**PC8**	GPC8, ADC0_OUT, I2C0_SCL, URT0_BRO, URT1_TX, TM20_OC0H, TM36_OC0H, TM36_OC0N, CCL_P0, URT6_TX, LCD_P33	
35	**PC9**	GPC9, CMP0_P0, I2C0_SDA, URT0_TMO, URT1_RX, TM20_OC1H, TM36_OC1H, TM36_OC1N, CCL_P1, URT6_RX, LCD_P34	
36	**PC10**	GPC10, CMP1_P0, I2C1_SCL, URT0_TX, URT2_TX, URT1_TX, TM36_OC2H, TM36_OC2N, CAN0_TX, URT7_TX, LCD_P35	
37	**PC11**	GPC11, I2C1_SDA, URT0_RX, URT2_RX, URT1_RX, TM36_OC3H, TM26_OC01, CAN0_RX, URT7_RX, LCD_P36	
38	**PC12**	GPC12, IR_OUT, URT1_DE, TM10_TRGO, TM36_OC3, TM26_OC02, SDT_P0, URT1_CLK, LCD_P37	
39	**PC13**	GPC13, XIN, URT1_NSS, URT0_CTS, URT2_RX, TM10_ETR, TM26_ETR, TM36_OC00, TM20_IC0, SDT_I0, TM36_IC1, URT6_RX	
40	**PC14**	GPC14, XOUT, URT1_TMO, URT0_RTS, URT2_TX, TM10_CKO, TM26_TRGO, TM36_OC10, TM20_IC1, SDT_I1, SDT_P0, URT6_TX	
41	**VSS1**		
42	**PD0**	GPD0, OBM_I0, TM10_CKO, URT0_CLK, TM26_OC1N, TM20_CKO, TM36_OC2, SPI0_NSS, TM36_IC3, URT2_NSS	LCD_C1
43	**PD1**	GPD1, OBM_I1, TM16_CKO, URT0_CLK, NCO_CK0, TM26_CKO, TM36_OC2N, SPI0_CLK, TM36_IC2, URT2_CLK	LCD_C2
44	**PD2**	GPD2, MF_S0, TM00_CKO, URT1_CLK, TM26_OC00, TM20_CKO, TM36_CKO, SPI0_MOSI, TM36_IC1, URT2_TX	LCD_VT
45	**PD3**	GPD3, MF_S1, TM01_CKO, URT1_CLK, SPI0_MISO, TM26_CKO, SPI0_D3, TM36_TRGO, URT2_RX	LCD_V1
46	**PD4**	GPD4, TM00_TRGO, TM01_TRGO, URT1_TX, TM26_OC00, SPI0_D2, URT2_TX, LCD_P38	
47	**PD5**	GPD5, TM00_ETR, I2C0_SCL, URT1_RX, TM26_OC01, SPI0_MISO, URT2_RX, LCD_P39	
48	**PD6**	GPD6, CPU_NMI, I2C0_SDA, URT1_NSS, SPI0_NSSI, TM26_OC02, SPI0_NSS, SDT_P0, URT2_NSS, LCD_P40	
49	**PD7**	GPD7, TM00_CKO, TM01_ETR, URT1_DE, SPI0_MISO, TM26_OC0N, SPI0_D4, TM36_IC0, TM36_OC3	LCD_V2
50	**PD8**	GPD8, CPU_TXEV, TM01_TRGO, URT1_RTS, SPI0_D2, TM26_OC10, SPI0_D7, TM36_IC1, SPI0_CLK, LCD_P41	
51	**PD9**	GPD9, CPU_RXEV, TM00_TRGO, URT1_CTS, SPI0_NSSI, TM26_OC11, SPI0_D6, TM36_IC2, SPI0_NSS	LCD_V3
52	**PD10**	GPD10, CPU_NMI, TM00_ETR, URT1_BRO, RTC_OUT, TM26_OC12, SPI0_D5, TM36_IC3, SPI0_MOSI, LCD_P42	
53	**PD11**	GPD11, CPU_NMI, DMA_TRG1, URT1_TMO, SPI0_D3, TM26_OC1N, SPI0_NSS, ASB_P3, LCD_P43	
54	**VSS**		
55	**VCAP**		

56	**VDD**		
57	**VREF+**		
58	**PA0**	GPA0, ASB_P0, NCO_P0, TM20_CKO, SDT_P0, CCL_P0, TM36_OC00, URT4_TX	ADC_I0, OP0_P0
59	**PA1**	GPA1, CPU_NMI, ASB_P1, NCO_CK0, URT1_BRO, TM20_OC10, CCL_P1, TM36_OC10, URT4_RX, LCD_P0	ADC_I1
60	**PA2**	GPA2, CPU_RXEV, ASB_P2, ASB_CK0, URT1_CTS, CAN0_TX, SDT_I0, SPI0_CLK, TM36_OC2, URT5_TX, LCD_P1	ADC_I2
61	**PA3**	GPA3, CPU_TXEV, ASB_P3, ASB_CK1, URT1_RTS, CAN0_RX, SDT_I1, SPI0_MOSI, TM36_OC2N, URT5_RX, LCD_P2	ADC_I3
62	**PA4**	GPA4, ASB_CK0, TM20_OC00, URT0_TX, LCD_P3	ADC_I4, OP0_I0
63	**PA5**	GPA5, ASB_CK1, TM20_OC10, URT0_RX, LCD_P4	ADC_I5, OP0_I1
64	**PA6**	GPA6, ASB_P2, SPI0_D3, TM20_OC0H, URT0_CLK, LCD_P5	ADC_I6

4.1.3. LQFP48 Package Pinout

Figure 4-3. LQFP48 Package Pinout

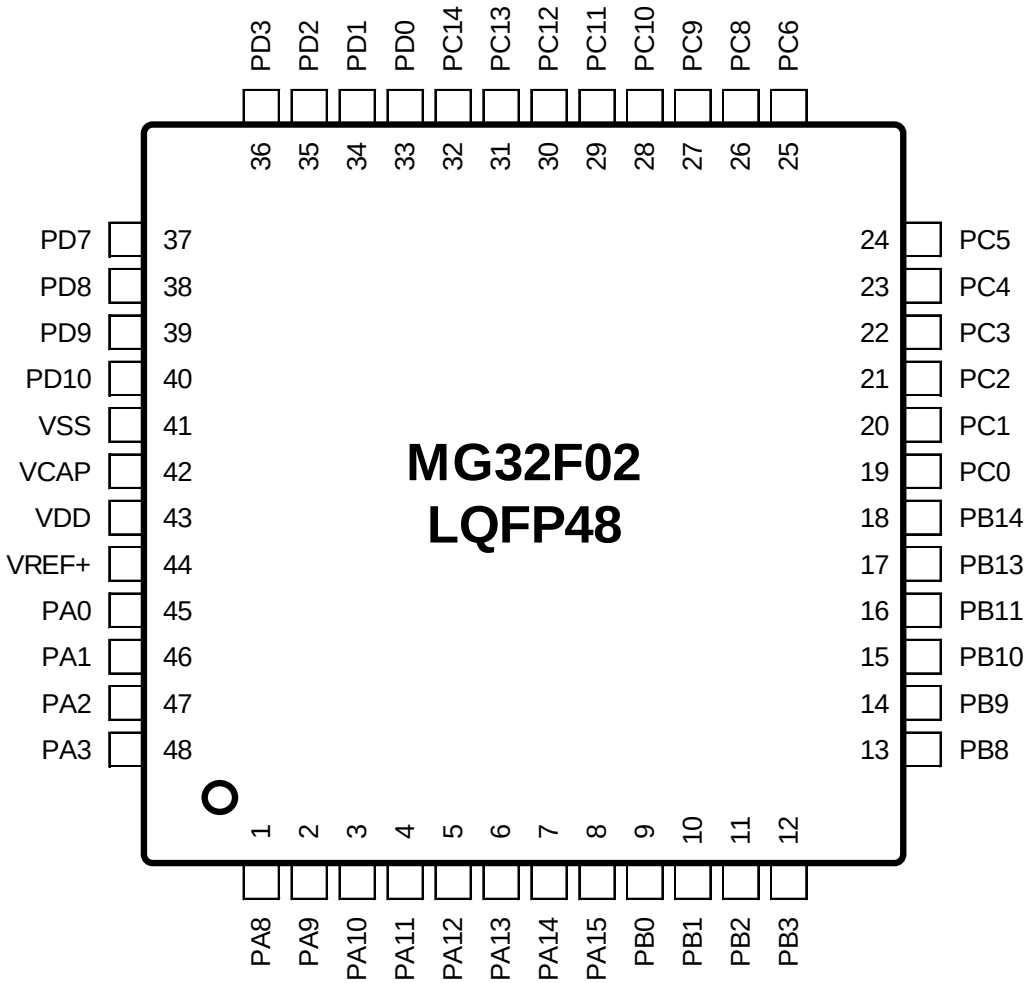

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Table 4-3. LQFP48 Pin AFS List

Pin	Name	Pin AFS List	Analog Function
1	PA8	GPA8, DMA_TRG0, ASB_P0, I2C0_SCL, URT2_BRO, SDT_I0, TM20_IC0, SPI0_NSS, TM36_OC0H, URT4_TX, LCD_P7	ADC_I8, CMP0_I0, VBG_OUT
2	PA9	GPA9, DMA_TRG1, ASB_P1, I2C1_SCL, URT2_TMO, ASB_CK0, TM20_IC1, SPI0_MISO, TM36_OC1H, URT5_TX, LCD_P8	ADC_I9, CMP0_I1
3	PA10	GPA10, TM36_BK0, SPI0_D2, I2C0_SDA, URT2_CTS, SDT_I1, TM26_IC0, SPI0_CLK, TM36_OC2H, URT4_RX, LCD_P9	ADC_I10, CMP1_I0
4	PA11	GPA11, SPI0_D3, I2C1_SDA, URT2_RTS, TM20_OC1N, TM26_IC1, SPI0_MOSI, TM36_OC3H, URT5_RX, LCD_P10	ADC_I11, CMP1_I1
5	PA12	GPA12, MF_S0, URT1_BRO, TM10_ETR, TM36_IC0, SPI0_D5, TM26_OC00, URT6_TX, LCD_P11	ADC_I12
6	PA13	GPA13, CPU_TXEV, MF_S1, URT0_BRO, URT1_TMO, TM10_TRGO, TM36_IC1, SPI0_D6, TM26_OC10, URT6_RX, LCD_P12	ADC_I13, ADC_PGA
7	PA14	GPA14, CPU_RXEV, OBM_I0, URT0_TMO, URT1_CTS, TM16_ETR, TM36_IC2, SPI0_D7, TM26_OC0H, URT7_TX, LCD_P13	ADC_I14
8	PA15	GPA15, CPU_NMI, OBM_I1, URT0_DE, URT1_RTS, TM16_TRGO, TM36_IC3, SPI0_D4, TM26_OC1H, URT7_RX, LCD_P14	ADC_I15
9	PB0	GPB0, I2C1_SCL, SPI0_NSS, TM01_ETR, TM00_CKO, TM16_ETR, TM26_IC0, TM36_ETR, URT1_NSS, URT2_NSS, URT6_TX, LCD_P15	CMP_C0

10	**PB1**	GPB1, I2C1_SDA, SPI0_MISO, TM01_TRGO, TM10_CKO, TM16_TRGO, TM26_IC1, TM36_TRGO, TM00_TRGO, URT1_RX, URT2_CLK, URT6_RX, LCD_P16	CMP_C1
11	**PB2**	GPB2, ADC0_TRG, SPI0_CLK, TM01_CKO, URT2_TX, TM16_CKO, TM26_OC0H, I2C0_SDA, TM10_TRGO, URT1_CLK, URT0_TX, URT7_TX, LCD_P17	
12	**PB3**	GPB3, ADC0_OUT, SPI0_MOSI, NCO_P0, URT2_RX, TM36_CKO, TM26_OC1H, I2C0_SCL, TM20_TRGO, URT1_TX, URT0_RX, URT7_RX, LCD_P18	
13	**PB8**	GPB8, CMP0_P0, RTC_OUT, URT0_TX, URT2_BRO, TM20_OC01, TM36_OC01, SPI0_D3, SDT_P0, OBM_P0, URT4_TX	
14	**PB9**	GPB9, CMP1_P0, RTC_TS, URT0_RX, URT2_TMO, TM20_OC02, TM36_OC02, SPI0_D2, OBM_P1, URT4_RX	
15	**PB10**	GPB10, I2C0_SCL, URT0_NSS, URT2_DE, TM20_OC11, TM36_OC11, URT1_TX, SPI0_NSSI, TM00_ETR, LCD_P23	
16	**PB11**	GPB11, I2C0_SDA, URT0_DE, IR_OUT, TM20_OC12, TM36_OC12, URT1_RX, DMA_TRG0, URT0_CLK, LCD_P24	
17	**PB13**	GPB13, TM00_ETR, URT0_CTS, TM20_ETR, TM36_ETR, URT0_CLK, CCL_P0, URT4_RX, LCD_P26	
18	**PB14**	GPB14, DMA_TRG0, TM00_TRGO, URT0_RTS, TM20_TRGO, TM36_BK0, URT0_NSS, CCL_P1, URT4_TX, LCD_P27	
19	**PC0**	GPC0, ICKO, TM00_CKO, URT0_CLK, URT2_CLK, TM20_OC00, TM36_OC00, I2C0_SCL, URT0_TX, URT5_TX, TM36_IC0	
20	**PC1**	GPC1, ADC0_TRG, TM01_CKO, TM36_IC0, URT1_CLK, TM20_OC0N, TM36_OC0N, I2C0_SDA, URT0_RX, URT5_RX, LCD_P29	
21	**PC2**	GPC2, ADC0_OUT, TM10_CKO, OBM_P0, URT2_CLK, TM20_OC10, TM36_OC10, SDT_I0, MF_S0, LCD_P30	
22	**PC3**	GPC3, OBM_P1, TM16_CKO, URT0_CLK, URT1_CLK, TM20_OC1N, TM36_OC1N, SDT_I1, MF_S1, LCD_P31	
23	**PC4**	GPC4, SWCLK, I2C0_SCL, URT0_RX, URT1_RX, TM36_IC2, TM36_OC2, SDT_I0, SDT_P0, URT6_RX	
24	**PC5**	GPC5, SWDIO, I2C0_SDA, URT0_TX, URT1_TX, TM36_IC3, TM36_OC3, SDT_I1, URT6_TX	
25	**PC6**	GPC6, RSTN, RTC_TS, URT0_NSS, URT1_NSS, TM20_ETR, TM26_ETR, TM36_OC1N	
26	**PC8**	GPC8, ADC0_OUT, I2C0_SCL, URT0_BRO, URT1_TX, TM20_OC0H, TM36_OC0H, TM36_OC0N, CCL_P0, URT6_TX, LCD_P33	
27	**PC9**	GPC9, CMP0_P0, I2C0_SDA, URT0_TMO, URT1_RX, TM20_OC1H, TM36_OC1H, TM36_OC1N, CCL_P1, URT6_RX, LCD_P34	
28	**PC10**	GPC10, CMP1_P0, I2C1_SCL, URT0_TX, URT2_TX, URT1_TX, TM36_OC2H, TM36_OC2N, CAN0_TX, URT7_TX, LCD_P35	
29	**PC11**	GPC11, I2C1_SDA, URT0_RX, URT2_RX, URT1_RX, TM36_OC3H, TM26_OC01, CAN0_RX, URT7_RX, LCD_P36	
30	**PC12**	GPC12, IR_OUT, URT1_DE, TM10_TRGO, TM36_OC3, TM26_OC02, SDT_P0, URT1_CLK, LCD_P37	
31	**PC13**	GPC13, XIN, URT1_NSS, URT0_CTS, URT2_RX, TM10_ETR, TM26_ETR, TM36_OC00, TM20_IC0, SDT_I0, TM36_IC1, URT6_RX	
32	**PC14**	GPC14, XOUT, URT1_TMO, URT0_RTS, URT2_TX, TM10_CKO, TM26_TRGO, TM36_OC10, TM20_IC1, SDT_I1, SDT_P0, URT6_TX	
33	**PD0**	GPD0, OBM_I0, TM10_CKO, URT0_CLK, TM26_OC1N, TM20_CKO, TM36_OC2, SPI0_NSS, TM36_IC3, URT2_NSS	LCD_C1
34	**PD1**	GPD1, OBM_I1, TM16_CKO, URT0_CLK, NCO_CK0, TM26_CKO, TM36_OC2N, SPI0_CLK, TM36_IC2, URT2_CLK	LCD_C2
35	**PD2**	GPD2, MF_S0, TM00_CKO, URT1_CLK, TM26_OC00, TM20_CKO, TM36_CKO, SPI0_MOSI, TM36_IC1, URT2_TX	LCD_VT
36	**PD3**	GPD3, MF_S1, TM01_CKO, URT1_CLK, SPI0_MISO, TM26_CKO, SPI0_D3, TM36_TRGO, URT2_RX	LCD_V1
37	**PD7**	GPD7, TM00_CKO, TM01_ETR, URT1_DE, SPI0_MISO, TM26_OC0N, SPI0_D4, TM36_IC0, TM36_OC3	LCD_V2
38	**PD8**	GPD8, CPU_TXEV, TM01_TRGO, URT1_RTS, SPI0_D2, TM26_OC10, SPI0_D7, TM36_IC1, SPI0_CLK, LCD_P41	
39	**PD9**	GPD9, CPU_RXEV, TM00_TRGO, URT1_CTS, SPI0_NSSI, TM26_OC11, SPI0_D6, TM36_IC2, SPI0_NSS	LCD_V3
40	**PD10**	GPD10, CPU_NMI, TM00_ETR, URT1_BRO, RTC_OUT, TM26_OC12, SPI0_D5, TM36_IC3, SPI0_MOSI, LCD_P42	
41	**VSS**		
42	**VCAP**		
43	**VDD**		
44	**VREF+**		
45	**PA0**	GPA0, ASB_P0, NCO_P0, TM20_CKO, SDT_P0, CCL_P0, TM36_OC00, URT4_TX	ADC_I0, OP0_P0
46	**PA1**	GPA1, CPU_NMI, ASB_P1, NCO_CK0, URT1_BRO, TM20_OC10, CCL_P1, TM36_OC10, URT4_RX, LCD_P0	ADC_I1
47	**PA2**	GPA2, CPU_RXEV, ASB_P2, ASB_CK0, URT1_CTS, CAN0_TX, SDT_I0, SPI0_CLK, TM36_OC2, URT5_TX, LCD_P1	ADC_I2
48	**PA3**	GPA3, CPU_TXEV, ASB_P3, ASB_CK1, URT1_RTS, CAN0_RX, SDT_I1, SPI0_MOSI, TM36_OC2N, URT5_RX, LCD_P2	ADC_I3

4.1.4. QFN32 Package Pinout

Figure 4-4. QFN32 Package Pinout

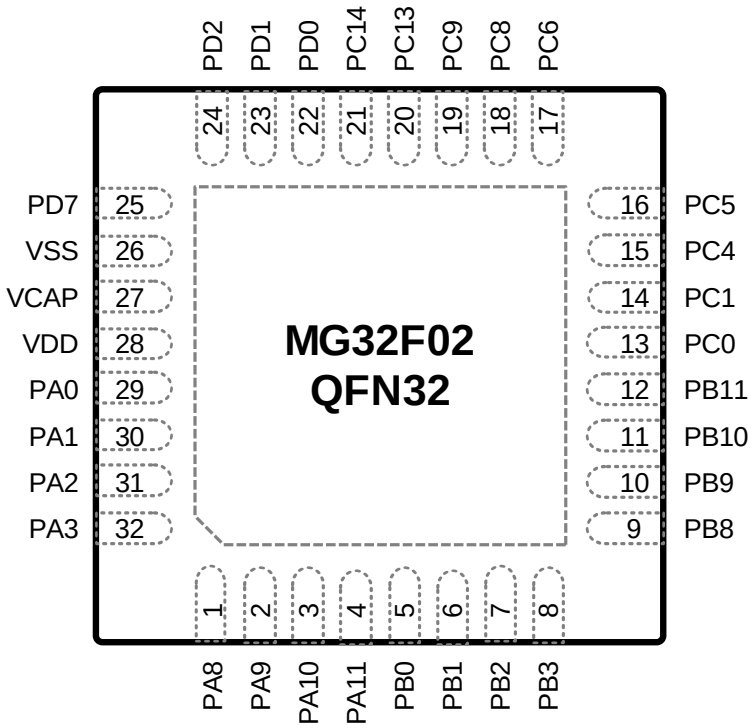

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Table 4-4. QFN32 Pin AFS List

Pin	Name	Pin AFS List	Analog Function
1	PA8	GPA8, DMA_TRG0, ASB_P0, I2C0_SCL, URT2_BRO, SDT_I0, TM20_IC0, SPI0_NSS, TM36_OC0H, URT4_TX, LCD_P7	ADC_I8, CMP0_I0, VBG_OUT
2	PA9	GPA9, DMA_TRG1, ASB_P1, I2C1_SCL, URT2_TMO, ASB_CK0, TM20_IC1, SPI0_MISO, TM36_OC1H, URT5_TX, LCD_P8	ADC_I9, CMP0_I1
3	PA10	GPA10, TM36_BK0, SPI0_D2, I2C0_SDA, URT2_CTS, SDT_I1, TM26_IC0, SPI0_CLK, TM36_OC2H, URT4_RX, LCD_P9	ADC_I10, CMP1_I0
4	PA11	GPA11, SPI0_D3, I2C1_SDA, URT2_RTS, TM20_OC1N, TM26_IC1, SPI0_MOSI, TM36_OC3H, URT5_RX, LCD_P10	ADC_I11, CMP1_I1
5	PB0	GPB0, I2C1_SCL, SPI0_NSS, TM01_ETR, TM00_CKO, TM16_ETR, TM26_IC0, TM36_ETR, URT1_NSS, URT2_NSS, URT6_TX, LCD_P15	CMP_C0
6	PB1	GPB1, I2C1_SDA, SPI0_MISO, TM01_TRGO, TM10_CKO, TM16_TRGO, TM26_IC1, TM36_TRGO, TM00_TRGO, URT1_RX, URT2_CLK, URT6_RX, LCD_P16	CMP_C1
7	PB2	GPB2, ADC0_TRG, SPI0_CLK, TM01_CKO, URT2_TX, TM16_CKO, TM26_OC0H, I2C0_SDA, TM10_TRGO, URT1_CLK, URT0_TX, URT7_TX, LCD_P17	
8	PB3	GPB3, ADC0_OUT, SPI0_MOSI, NCO_P0, URT2_RX, TM36_CKO, TM26_OC1H, I2C0_SCL, TM20_TRGO, URT1_TX, URT0_RX, URT7_RX, LCD_P18	
9	PB8	GPB8, CMP0_P0, RTC_OUT, URT0_TX, URT2_BRO, TM20_OC01, TM36_OC01, SPI0_D3, SDT_P0, OBM_P0, URT4_TX	
10	PB9	GPB9, CMP1_P0, RTC_TS, URT0_RX, URT2_TMO, TM20_OC02, TM36_OC02, SPI0_D2, OBM_P1, URT4_RX	
11	PB10	GPB10, I2C0_SCL, URT0_NSS, URT2_DE, TM20_OC11, TM36_OC11, URT1_TX, SPI0_NSSI, TM00_ETR, LCD_P23	
12	PB11	GPB11, I2C0_SDA, URT0_DE, IR_OUT, TM20_OC12, TM36_OC12, URT1_RX, DMA_TRG0, URT0_CLK, LCD_P24	
13	PC0	GPC0, ICKO, TM00_CKO, URT0_CLK, URT2_CLK, TM20_OC00, TM36_OC00, I2C0_SCL, URT0_TX, URT5_TX, TM36_IC0	

14	**PC1**	GPC1, ADC0_TRG, TM01_CKO, TM36_IC0, URT1_CLK, TM20_OC0N, TM36_OC0N, I2C0_SDA, URT0_RX, URT5_RX, LCD_P29	
15	**PC4**	GPC4, SWCLK, I2C0_SCL, URT0_RX, URT1_RX, TM36_IC2, TM36_OC2, SDT_I0, SDT_P0, URT6_RX	
16	**PC5**	GPC5, SWDIO, I2C0_SDA, URT0_TX, URT1_TX, TM36_IC3, TM36_OC3, SDT_I1, URT6_TX	
17	**PC6**	GPC6, RSTN, RTC_TS, URT0_NSS, URT1_NSS, TM20_ETR, TM26_ETR, TM36_OC1N	
18	**PC8**	GPC8, ADC0_OUT, I2C0_SCL, URT0_BRO, URT1_TX, TM20_OC0H, TM36_OC0H, TM36_OC0N, CCL_P0, URT6_TX, LCD_P33	
19	**PC9**	GPC9, CMP0_P0, I2C0_SDA, URT0_TMO, URT1_RX, TM20_OC1H, TM36_OC1H, TM36_OC1N, CCL_P1, URT6_RX, LCD_P34	
20	**PC13**	GPC13, XIN, URT1_NSS, URT0_CTS, URT2_RX, TM10_ETR, TM26_ETR, TM36_OC00, TM20_IC0, SDT_I0, TM36_IC1, URT6_RX	
21	**PC14**	GPC14, XOUT, URT1_TMO, URT0_RTS, URT2_TX, TM10_CKO, TM26_TRGO, TM36_OC10, TM20_IC1, SDT_I1, SDT_P0, URT6_TX	
22	**PD0**	GPD0, OBM_I0, TM10_CKO, URT0_CLK, TM26_OC1N, TM20_CKO, TM36_OC2, SPI0_NSS, TM36_IC3, URT2_NSS	LCD_C1
23	**PD1**	GPD1, OBM_I1, TM16_CKO, URT0_CLK, NCO_CK0, TM26_CKO, TM36_OC2N, SPI0_CLK, TM36_IC2, URT2_CLK	LCD_C2
24	**PD2**	GPD2, MF_S0, TM00_CKO, URT1_CLK, TM26_OC00, TM20_CKO, TM36_CKO, SPI0_MOSI, TM36_IC1, URT2_TX	LCD_VT
25	**PD7**	GPD7, TM00_CKO, TM01_ETR, URT1_DE, SPI0_MISO, TM26_OC0N, SPI0_D4, TM36_IC0, TM36_OC3	LCD_V2
26	**VSS**		
27	**VCAP**		
28	**VDD**		
29	**PA0**	GPA0, ASB_P0, NCO_P0, TM20_CKO, SDT_P0, CCL_P0, TM36_OC00, URT4_TX	ADC_I0, OP0_P0
30	**PA1**	GPA1, CPU_NMI, ASB_P1, NCO_CK0, URT1_BRO, TM20_OC10, CCL_P1, TM36_OC10, URT4_RX, LCD_P0	ADC_I1
31	**PA2**	GPA2, CPU_RXEV, ASB_P2, ASB_CK0, URT1_CTS, CAN0_TX, SDT_I0, SPI0_CLK, TM36_OC2, URT5_TX, LCD_P1	ADC_I2
32	**PA3**	GPA3, CPU_TXEV, ASB_P3, ASB_CK1, URT1_RTS, CAN0_RX, SDT_I1, SPI0_MOSI, TM36_OC2N, URT5_RX, LCD_P2	ADC_I3

4.2. Pin Definition

Table 4-5. Abbreviations for pin definition

IO Type		IO Structure	
P	Power/Ground pin	I	Digital Input
B	Bidirectional	P	Output Push-pull capability
I	Input	O	Output Open drain capability
O	Output	Q	Quasi-bidirectional
A	Analog I/O	A	Analog I/O (Digital I/O disable)
AO	Analog output only	U	Internal pull-up
AI	Analog input only	H	High Speed
Q	Quasi-bidirectional	C2	Programmable 2-level driving strength
-		C4	Programmable 4-level driving strength
-		CF	Fixed driving strength(GPIO mode)

Table 4-6. Pin Descriptions

Pin Name	Pin Number				IO Type	Default		IO Structure	Alternate Functions	Description
	LQFP80	LQFP64	LQFP48	QFN32		Type	Value			
PA0	74	58	45	29	B	A		A,I,P,O,U,H,C2	GPA0	GPIO/Interrupt/KBI Port-A function pin-0
									ASB_P0	ASB output signal-0
									NCO_P0	NCO clock output signal-0
									TM20_CKO	TM20 timer overflow output signal
									SDT_P0	SDT output signal-0
									CCL_P0	CCL output signal-0
									TM36_OC00	TM36 output compare/PWM channel-00
									URT4_TX	URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.
									ADC_I0	ADC analog single-end input channel 0
									OP0_P0	OPA OP0 analog output channel 0
PA1	75	59	46	30	B	A		A,I,P,O,U,H,C2	GPA1	GPIO/Interrupt/KBI Port-A function pin-1
									CPU_NMI	CPU NMI external pin input
									ASB_P1	ASB output signal-1
									NCO_CK0	NCO external clock input signal-0
									URT1_BRO	URT1 baud-rate timer overflow output signal
									TM20_OC10	TM20 output compare/PWM channel-10
									CCL_P1	CCL output signal-1
									TM36_OC10	TM36 output compare/PWM channel-10
									URT4_RX	URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.
									LCD_P0	LCD drive pin
									ADC_I1	ADC analog single-end input channel 1
PA2	76	60	47	31	B	A		A,I,P,O,U,H,C2	GPA2	GPIO/Interrupt/KBI Port-A function pin-2
									CPU_RXEV	CPU wakeup event input
									ASB_P2	ASB output signal-2
									ASB_CK0	ASB clock output signal-0
									URT1_CTS	URT1 CTS input control signal
									CAN0_TX	CAN0 transmit TX signal. CAN0_RX and

										CAN0_TX can be swapped by register setting.
									SDT_I0	State detect input signal-0
									SPI0_CLK	SPI0 clock signal
									TM36_OC2	TM36 output compare/PWM channel-2
									URT5_TX	URT5 transmit TX signal. URT5_RX and URT5_TX can be swapped by register setting.
									LCD_P1	LCD drive pin
									ADC_I2	ADC analog single-end input channel 2
PA3	77	61	48	32	B	A		A,I,P,O,U,H,C2	GPA3	GPIO/Interrupt/KBI Port-A function pin-3
									CPU_TXEV	CPU wakeup event output
									ASB_P3	ASB output signal-3
									ASB_CK1	ASB clock output signal-1
									URT1_RTS	URT1 RTS output control signal
									CAN0_RX	CAN0 receive RX signal. CAN0_RX and CAN0_TX can be swapped by register setting.
									SDT_I1	State detect input signal-1
									SPI0_MOSI	SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
									TM36_OC2N	TM36 output compare/PWM complement channel-2
									URT5_RX	URT5 receive RX signal. URT5_RX and URT5_TX can be swapped by register setting.
									LCD_P2	LCD drive pin
									ADC_I3	ADC analog single-end input channel 3
PA4	78	62			B	A		A,I,P,O,U,H,C2	GPA4	GPIO/Interrupt/KBI Port-A function pin-4
									ASB_CK0	ASB clock output signal-0
									TM20_OC00	TM20 output compare/PWM channel-00
									URT0_TX	URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting.
									LCD_P3	LCD drive pin
									ADC_I4	ADC analog single-end input channel 4
									OP0_I0	OPA OP0 analog input channel 0
PA5	79	63			B	A		A,I,P,O,U,H,C2	GPA5	GPIO/Interrupt/KBI Port-A function pin-5
									ASB_CK1	ASB clock output signal-1
									TM20_OC10	TM20 output compare/PWM channel-10
									URT0_RX	URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting.
									LCD_P4	LCD drive pin
									ADC_I5	ADC analog single-end input channel 5
									OP0_I1	OPA OP0 analog input channel 1
PA6	80	64			B	A		A,I,P,O,U,H,C2	GPA6	GPIO/Interrupt/KBI Port-A function pin-6
									ASB_P2	ASB output signal-2
									SPI0_D3	SPI0 data-3 signal for 4-I/O mode
									TM20_OC0H	TM20 output compare/PWM high channel-0
									URT0_CLK	URT0 clock signal

									LCD_P5	LCD drive pin
									ADC_I6	ADC analog single-end input channel 6
PA7	1	1			B	A		A,I,P,O,U,H,C2	GPA7	GPIO/Interrupt/KBI Port-A function pin-7
									ASB_P3	ASB output signal-3
									SPI0_D2	SPI0 data-2 signal for 4-I/O mode
									TM20_OC1H	TM20 output compare/PWM high channel-1
									URT0_NSS	URT0 SPI NSS input/output signal
									LCD_P6	LCD drive pin
									ADC_I7	ADC analog single-end input channel 7
PA8	2	2	1	1	B	A		A,I,P,O,U,H,C2	GPA8	GPIO/Interrupt/KBI Port-A function pin-8
									DMA_TRG0	DMA external trigger pin-0 input
									ASB_P0	ASB output signal-0
									I2C0_SCL	I2C0 SCL signal
									URT2_BRO	URT2 baud-rate timer overflow output signal
									SDT_I0	State detect input signal-0
									TM20_IC0	TM20 input capture channel-0
									SPI0_NSS	SPI0 slave select input/output signal
									TM36_OC0H	TM36 output compare/PWM high channel-0
									URT4_TX	URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.
									LCD_P7	LCD drive pin
									ADC_I8	ADC analog single-end input channel 8
									CMP0_I0	Comparator-0 analog input channel 0
									VBG_OUT	Bandgap voltage output
PA9	3	3	2	2	B	A		A,I,P,O,U,H,C2	GPA9	GPIO/Interrupt/KBI Port-A function pin-9
									DMA_TRG1	DMA external trigger pin-1 input
									ASB_P1	ASB output signal-1
									I2C1_SCL	I2C1 SCL signal
									URT2_TMO	URT2 timeout timer overflow output signal
									ASB_CK0	ASB clock output signal-0
									TM20_IC1	TM20 input capture channel-1
									SPI0_MISO	SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
									TM36_OC1H	TM36 output compare/PWM high channel-1
									URT5_TX	URT5 transmit TX signal. URT5_RX and URT5_TX can be swapped by register setting.
									LCD_P8	LCD drive pin
									ADC_I9	ADC analog single-end input channel 9
									CMP0_I1	Comparator-0 analog input channel 1
PA10	4	4	3	3	B	A		A,I,P,O,U,H,C2	GPA10	GPIO/Interrupt/KBI Port-A function pin-10
									TM36_BK0	TM36 break input signal
									SPI0_D2	SPI0 data-2 signal for 4-I/O mode
									I2C0_SDA	I2C0 SDA signal
									URT2_CTS	URT2 CTS input control signal
									SDT_I1	State detect input signal-1
									TM26_IC0	TM26 input capture channel-0
									SPI0_CLK	SPI0 clock signal

									TM36_OC2H	TM36 output compare/PWM high channel-2
									URT4_RX	URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.
									LCD_P9	LCD drive pin
									ADC_I10	ADC analog single-end input channel 10
									CMP1_I0	Comparator-1 analog input channel 0
PA11	5	5	4	4	B	A		A,I,P,O,U,H,C2	GPA11	GPIO/Interrupt/KBI Port-A function pin-11
									SPI0_D3	SPI0 data-3 signal for 4-I/O mode
									I2C1_SDA	I2C1 SDA signal
									URT2_RTS	URT2 RTS output control signal
									TM20_OC1N	TM20 output compare/PWM complement channel-1
									TM26_IC1	TM26 input capture channel-1
									SPI0_MOSI	SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
									TM36_OC3H	TM36 output compare/PWM high channel-3
									URT5_RX	URT5 receive RX signal. URT5_RX and URT5_TX can be swapped by register setting.
									LCD_P10	LCD drive pin
									ADC_I11	ADC analog single-end input channel 11
									CMP1_I1	Comparator-1 analog input channel 1
PA12	6	6	5		B	A		A,I,P,O,U,H,C2	GPA12	GPIO/Interrupt/KBI Port-A function pin-12
									MF_S0	Multi-Function signal-0 output
									URT1_BRO	URT1 baud-rate timer overflow output signal
									TM10_ETR	TM10 external trigger/clock input signal
									TM36_IC0	TM36 input capture channel-0
									SPI0_D5	SPI0 data-1 signal for 2nd SPI device 4-I/O mode
									TM26_OC00	TM26 output compare/PWM channel-00
									URT6_TX	URT6 transmit TX signal. URT6_RX and URT6_TX can be swapped by register setting.
									LCD_P11	LCD drive pin
									ADC_I12	ADC analog single-end input channel 12
PA13	7	7	6		B	A		A,I,P,O,U,H,C2	GPA13	GPIO/Interrupt/KBI Port-A function pin-13
									CPU_TXEV	CPU wakeup event output
									MF_S1	Multi-Function signal-1 output
									URT0_BRO	URT0 baud-rate timer overflow output signal
									URT1_TMO	URT1 timeout timer overflow output signal
									TM10_TRGO	TM10 trigger output signal
									TM36_IC1	TM36 input capture channel-1
									SPI0_D6	SPI0 data-2 signal for 2nd SPI device 4-I/O mode
									TM26_OC10	TM26 output compare/PWM channel-10
									URT6_RX	URT6 receive RX signal. URT6_RX and URT6_TX can be swapped by register setting.
									LCD_P12	LCD drive pin
									ADC_I13	ADC analog single-end input channel 13

									ADC_PGA	ADC PGA voltage output
PA14	8	8	7		B	A		A,I,P,O,U,H,C2	GPA14	GPIO/Interrupt/KBI Port-A function pin-14
									CPU_RXEV	CPU wakeup event input
									OBM_I0	Output signal break control input signal-0
									URT0_TMO	URT0 timeout timer overflow output signal
									URT1_CTS	URT1 CTS input control signal
									TM16_ETR	TM16 external trigger/clock input signal
									TM36_IC2	TM36 input capture channel-2
									SPI0_D7	SPI0 data-3 signal for 2nd SPI device 4-I/O mode
									TM26_OC0H	TM26 output compare/PWM high channel-0
									URT7_TX	URT7 transmit TX signal. URT7_RX and URT7_TX can be swapped by register setting.
									LCD_P13	LCD drive pin
									ADC_I14	ADC analog single-end input channel 14
PA15	9	9	8		B	A		A,I,P,O,U,H,C2	GPA15	GPIO/Interrupt/KBI Port-A function pin-15
									CPU_NMI	CPU NMI external pin input
									OBM_I1	Output signal break control input signal-1
									URT0_DE	URT0 external drive enable output signal
									URT1_RTS	URT1 RTS output control signal
									TM16_TRGO	TM16 trigger output signal
									TM36_IC3	TM36 input capture channel-3
									SPI0_D4	SPI0 data-0 signal for 2nd SPI device 4-I/O mode
									TM26_OC1H	TM26 output compare/PWM high channel-1
									URT7_RX	URT7 receive RX signal. URT7_RX and URT7_TX can be swapped by register setting.
									LCD_P14	LCD drive pin
									ADC_I15	ADC analog single-end input channel 15
PB0	10	10	9	5	B	A		A,I,P,O,U,H,C4	GPB0	GPIO/Interrupt/KBI Port-B function pin-0
									I2C1_SCL	I2C1 SCL signal
									SPI0_NSS	SPI0 slave select input/output signal
									TM01_ETR	TM01 external trigger/clock input signal
									TM00_CKO	TM00 timer overflow output signal
									TM16_ETR	TM16 external trigger/clock input signal
									TM26_IC0	TM26 input capture channel-0
									TM36_ETR	TM36 external trigger/clock input signal
									URT1_NSS	URT1 SPI NSS input/output signal
									URT2_NSS	URT2 SPI NSS input/output signal
									URT6_TX	URT6 transmit TX signal. URT6_RX and URT6_TX can be swapped by register setting.
									LCD_P15	LCD drive pin
									CMP_C0	Comparator analog input common channel 0
PB1	11	11	10	6	B	A		A,I,P,O,U,H,C4	GPB1	GPIO/Interrupt/KBI Port-B function pin-1
									I2C1_SDA	I2C1 SDA signal
									SPI0_MISO	SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.

									TM01_TRGO	TM01 trigger output signal
									TM10_CKO	TM10 timer overflow output signal
									TM16_TRGO	TM16 trigger output signal
									TM26_IC1	TM26 input capture channel-1
									TM36_TRGO	TM36 trigger output signal
									TM00_TRGO	TM00 trigger output signal
									URT1_RX	URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.
									URT2_CLK	URT2 clock signal
									URT6_RX	URT6 receive RX signal. URT6_RX and URT6_TX can be swapped by register setting.
									LCD_P16	LCD drive pin
									CMP_C1	Comparator analog input common channel 1
PB2	12	12	11	7	B	A		A,I,P,O,U,H,C4	GPB2	GPIO/Interrupt/KBI Port-B function pin-2
									ADC0_TRG	ADC trigger start input
									SPI0_CLK	SPI0 clock signal
									TM01_CKO	TM01 timer overflow output signal
									URT2_TX	URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting.
									TM16_CKO	TM16 timer overflow output signal
									TM26_OC0H	TM26 output compare/PWM high channel-0
									I2C0_SDA	I2C0 SDA signal
									TM10_TRGO	TM10 trigger output signal
									URT1_CLK	URT1 clock signal
									URT0_TX	URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting.
									URT7_TX	URT7 transmit TX signal. URT7_RX and URT7_TX can be swapped by register setting.
									LCD_P17	LCD drive pin
PB3	13	13	12	8	B	A		A,I,P,O,U,H,C4	GPB3	GPIO/Interrupt/KBI Port-B function pin-3
									ADC0_OUT	ADC threshold window compare output
									SPI0_MOSI	SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
									NCO_P0	NCO clock output signal-0
									URT2_RX	URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.
									TM36_CKO	TM36 timer overflow output signal
									TM26_OC1H	TM26 output compare/PWM high channel-1
									I2C0_SCL	I2C0 SCL signal
									TM20_TRGO	TM20 trigger output signal
									URT1_TX	URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting.

									URT0_RX	URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting.
									URT7_RX	URT7 receive RX signal. URT7_RX and URT7_TX can be swapped by register setting.
									LCD_P18	LCD drive pin
PB4	18	14			B	A		A,I,P,O,U,H,C4	GPB4	GPIO/Interrupt/KBI Port-B function pin-4
									TM01_CKO	TM01 timer overflow output signal
									SPI0_D3	SPI0 data-3 signal for 4-I/O mode
									TM26_TRGO	TM26 trigger output signal
									URT2_CLK	URT2 clock signal
									TM20_IC0	TM20 input capture channel-0
									TM36_IC0	TM36 input capture channel-0
									LCD_P19	LCD drive pin
PB5	19	15			B	A		A,I,P,O,U,H,C4	GPB5	GPIO/Interrupt/KBI Port-B function pin-5
									TM16_CKO	TM16 timer overflow output signal
									SPI0_D2	SPI0 data-2 signal for 4-I/O mode
									TM26_ETR	TM26 external trigger/clock input signal
									URT2_NSS	URT2 SPI NSS input/output signal
									TM20_IC1	TM20 input capture channel-1
									TM36_IC1	TM36 input capture channel-1
									LCD_P20	LCD drive pin
PB6	20	16			B	A		A,I,P,O,U,H,C2	GPB6	GPIO/Interrupt/KBI Port-B function pin-6
									CPU_RXEV	CPU wakeup event input
									SPI0_NSSI	SPI0 slave select input only signal
									URT0_BRO	URT0 baud-rate timer overflow output signal
									URT2_CTS	URT2 CTS input control signal
									TM20_ETR	TM20 external trigger/clock input signal
									TM36_IC2	TM36 input capture channel-2
									CAN0_TX	CAN0 transmit TX signal. CAN0_RX and CAN0_TX can be swapped by register setting.
									URT2_TX	URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting.
									LCD_P21	LCD drive pin
PB7	21	17			B	A		A,I,P,O,U,H,C2	GPB7	GPIO/Interrupt/KBI Port-B function pin-7
									CPU_TXEV	CPU wakeup event output
									URT0_TMO	URT0 timeout timer overflow output signal
									URT2_RTS	URT2 RTS output control signal
									TM20_TRGO	TM20 trigger output signal
									TM36_IC3	TM36 input capture channel-3
									CAN0_RX	CAN0 receive RX signal. CAN0_RX and CAN0_TX can be swapped by register setting.
									URT2_RX	URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.
									LCD_P22	LCD drive pin
PB8	22	18	13	9	B	A		A,I,P,O,U,H,C4	GPB8	GPIO/Interrupt/KBI Port-B function pin-8

									CMP0_P0	Comparator-0 data output
									RTC_OUT	RTC selection output signal
									URT0_TX	URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting.
									URT2_BRO	URT2 baud-rate timer overflow output signal
									TM20_OC01	TM20 output compare/PWM channel-01
									TM36_OC01	TM36 output compare/PWM channel-01
									SPI0_D3	SPI0 data-3 signal for 4-I/O mode
									SDT_P0	SDT output signal-0
									OBM_P0	Output signal break control output signal-0
									URT4_TX	URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.
PB9	23	19	14	10	B	A		A,I,P,O,U,H,C4	GPB9	GPIO/Interrupt/KBI Port-B function pin-9
									CMP1_P0	Comparator-1 data output
									RTC_TS	RTC time stamp input signal
									URT0_RX	URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting.
									URT2_TMO	URT2 timeout timer overflow output signal
									TM20_OC02	TM20 output compare/PWM channel-02
									TM36_OC02	TM36 output compare/PWM channel-02
									SPI0_D2	SPI0 data-2 signal for 4-I/O mode
									OBM_P1	Output signal break control output signal-1
									URT4_RX	URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.
PB10	24	20	15	11	B	A		A,I,P,O,U,H,C2	GPB10	GPIO/Interrupt/KBI Port-B function pin-10
									I2C0_SCL	I2C0 SCL signal
									URT0_NSS	URT0 SPI NSS input/output signal
									URT2_DE	URT2 external drive enable output signal
									TM20_OC11	TM20 output compare/PWM channel-11
									TM36_OC11	TM36 output compare/PWM channel-11
									URT1_TX	URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting.
									SPI0_NSSI	SPI0 slave select input only signal
									TM00_ETR	TM00 external trigger/clock input signal
									LCD_P23	LCD drive pin
PB11	25	21	16	12	B	A		A,I,P,O,U,H,C2	GPB11	GPIO/Interrupt/KBI Port-B function pin-11
									I2C0_SDA	I2C0 SDA signal
									URT0_DE	URT0 external drive enable output signal
									IR_OUT	IR output signal
									TM20_OC12	TM20 output compare/PWM channel-12
									TM36_OC12	TM36 output compare/PWM channel-12
									URT1_RX	URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.
									DMA_TRG0	DMA external trigger pin-0 input

									URT0_CLK	URT0 clock signal
									LCD_P24	LCD drive pin
PB12	26	22			B	A		A,I,P,O,U,H,C2	GPB12	GPIO/Interrupt/KBI Port-B function pin-12
									DMA_TRG0	DMA external trigger pin-0 input
									NCO_P0	NCO clock output signal-0
									MF_S0	Multi-Function signal-0 output
									ASB_P0	ASB output signal-0
									URT1_CLK	URT1 clock signal
									URT5_TX	URT5 transmit TX signal. URT5_RX and URT5_TX can be swapped by register setting.
									LCD_P25	LCD drive pin
PB13	28	23	17		B	A		A,I,P,O,U,H,C2	GPB13	GPIO/Interrupt/KBI Port-B function pin-13
									TM00_ETR	TM00 external trigger/clock input signal
									URT0_CTS	URT0 CTS input control signal
									TM20_ETR	TM20 external trigger/clock input signal
									TM36_ETR	TM36 external trigger/clock input signal
									URT0_CLK	URT0 clock signal
									CCL_P0	CCL output signal-0
									URT4_RX	URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.
									LCD_P26	LCD drive pin
PB14	29	24	18		B	A		A,I,P,O,U,H,C2	GPB14	GPIO/Interrupt/KBI Port-B function pin-14
									DMA_TRG0	DMA external trigger pin-0 input
									TM00_TRGO	TM00 trigger output signal
									URT0_RTS	URT0 RTS output control signal
									TM20_TRGO	TM20 trigger output signal
									TM36_BK0	TM36 break input signal
									URT0_NSS	URT0 SPI NSS input/output signal
									CCL_P1	CCL output signal-1
									URT4_TX	URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.
									LCD_P27	LCD drive pin
PB15	31	25			B	A		A,I,P,O,U,H,C2	GPB15	GPIO/Interrupt/KBI Port-B function pin-15
									IR_OUT	IR output signal
									NCO_CK0	NCO external clock input signal-0
									MF_S1	Multi-Function signal-1 output
									ASB_P1	ASB output signal-1
									URT1_NSS	URT1 SPI NSS input/output signal
									URT2_NSS	URT2 SPI NSS input/output signal
									URT5_RX	URT5 receive RX signal. URT5_RX and URT5_TX can be swapped by register setting.
									LCD_P28	LCD drive pin
PC0	34	26	19	13	B	A		A,I,P,O,Q,U,H,C2	GPC0	GPIO/Interrupt/KBI Port-C function pin-0
									ICKO	Internal clock source clock output
									TM00_CKO	TM00 timer overflow output signal
									URT0_CLK	URT0 clock signal
									URT2_CLK	URT2 clock signal
									TM20_OC00	TM20 output compare/PWM channel-00

									TM36_OC00	TM36 output compare/PWM channel-00
									I2C0_SCL	I2C0 SCL signal
									URT0_TX	URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting.
									URT5_TX	URT5 transmit TX signal. URT5_RX and URT5_TX can be swapped by register setting.
									TM36_IC0	TM36 input capture channel-0
PC1	35	27	20	14	B	A		A,I,P,O,Q,U,H,C2	GPC1	GPIO/Interrupt/KBI Port-C function pin-1
									ADC0_TRG	ADC trigger start input
									TM01_CKO	TM01 timer overflow output signal
									TM36_IC0	TM36 input capture channel-0
									URT1_CLK	URT1 clock signal
									TM20_OC0N	TM20 output compare/PWM complement channel-0
									TM36_OC0N	TM36 output compare/PWM complement channel-0
									I2C0_SDA	I2C0 SDA signal
									URT0_RX	URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting.
									URT5_RX	URT5 receive RX signal. URT5_RX and URT5_TX can be swapped by register setting.
									LCD_P29	LCD drive pin
PC2	36	28	21		B	A		A,I,P,O,Q,U,H,C2	GPC2	GPIO/Interrupt/KBI Port-C function pin-2
									ADC0_OUT	ADC threshold window compare output
									TM10_CKO	TM10 timer overflow output signal
									OBM_P0	Output signal break control output signal-0
									URT2_CLK	URT2 clock signal
									TM20_OC10	TM20 output compare/PWM channel-10
									TM36_OC10	TM36 output compare/PWM channel-10
									SDT_I0	State detect input signal-0
									MF_S0	Multi-Function signal-0 output
									LCD_P30	LCD drive pin
PC3	37	29	22		B	A		A,I,P,O,Q,U,H,C2	GPC3	GPIO/Interrupt/KBI Port-C function pin-3
									OBM_P1	Output signal break control output signal-1
									TM16_CKO	TM16 timer overflow output signal
									URT0_CLK	URT0 clock signal
									URT1_CLK	URT1 clock signal
									TM20_OC1N	TM20 output compare/PWM complement channel-1
									TM36_OC1N	TM36 output compare/PWM complement channel-1
									SDT_I1	State detect input signal-1
									MF_S1	Multi-Function signal-1 output
									LCD_P31	LCD drive pin
PC4	38	30	23	15	B	Q	H	A,I,P,O,Q,U,H,C2	GPC4	GPIO/Interrupt/KBI Port-C function pin-4
									SWCLK	Serial wire debug clock signal

									I2C0_SCL	I2C0 SCL signal
									URT0_RX	URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting.
									URT1_RX	URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.
									TM36_IC2	TM36 input capture channel-2
									TM36_OC2	TM36 output compare/PWM channel-2
									SDT_I0	State detect input signal-0
									SDT_P0	SDT output signal-0
									URT6_RX	URT6 receive RX signal. URT6_RX and URT6_TX can be swapped by register setting.
PC5	39	31	24	16	B	Q	H	A,I,P,O,Q,U,H,C2	GPC5	GPIO/Interrupt/KBI Port-C function pin-5
									SWDIO	Serial wire debug data signal
									I2C0_SDA	I2C0 SDA signal
									URT0_TX	URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting.
									URT1_TX	URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting.
									TM36_IC3	TM36 input capture channel-3
									TM36_OC3	TM36 output compare/PWM channel-3
									SDT_I1	State detect input signal-1
									URT6_TX	URT6 transmit TX signal. URT6_RX and URT6_TX can be swapped by register setting.
PC6	40	32	25	17	B	Q	H	A,I,P,O,Q,U,H,CF	GPC6	GPIO/Interrupt/KBI Port-C function pin-6
									RSTN	External hardware reset input
									RTC_TS	RTC time stamp input signal
									URT0_NSS	URT0 SPI NSS input/output signal
									URT1_NSS	URT1 SPI NSS input/output signal
									TM20_ETR	TM20 external trigger/clock input signal
									TM26_ETR	TM26 external trigger/clock input signal
									TM36_OC1N	TM36 output compare/PWM complement channel-1
PC7	41	33			B	A		A,I,P,O,Q,U,H,C2	GPC7	GPIO/Interrupt/KBI Port-C function pin-7
									ADC0_TRG	ADC trigger start input
									RTC_OUT	RTC selection output signal
									URT0_DE	URT0 external drive enable output signal
									URT1_NSS	URT1 SPI NSS input/output signal
									ASB_P2	ASB output signal-2
									TM36_TRGO	TM36 trigger output signal
									LCD_P32	LCD drive pin
PC8	42	34	26	18	B	A		A,I,P,O,Q,U,H,C2	GPC8	GPIO/Interrupt/KBI Port-C function pin-8
									ADC0_OUT	ADC threshold window compare output
									I2C0_SCL	I2C0 SCL signal
									URT0_BRO	URT0 baud-rate timer overflow output signal

									URT1_TX	URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting.
									TM20_OC0H	TM20 output compare/PWM high channel-0
									TM36_OC0H	TM36 output compare/PWM high channel-0
									TM36_OC0N	TM36 output compare/PWM complement channel-0
									CCL_P0	CCL output signal-0
									URT6_TX	URT6 transmit TX signal. URT6_RX and URT6_TX can be swapped by register setting.
									LCD_P33	LCD drive pin
PC9	43	35	27	19	B	A		A,I,P,O,Q,U,H,C2	GPC9	GPIO/Interrupt/KBI Port-C function pin-9
									CMP0_P0	Comparator-0 data output
									I2C0_SDA	I2C0 SDA signal
									URT0_TMO	URT0 timeout timer overflow output signal
									URT1_RX	URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.
									TM20_OC1H	TM20 output compare/PWM high channel-1
									TM36_OC1H	TM36 output compare/PWM high channel-1
									TM36_OC1N	TM36 output compare/PWM complement channel-1
									CCL_P1	CCL output signal-1
									URT6_RX	URT6 receive RX signal. URT6_RX and URT6_TX can be swapped by register setting.
									LCD_P34	LCD drive pin
PC10	44	36	28		B	A		A,I,P,O,Q,U,H,C2	GPC10	GPIO/Interrupt/KBI Port-C function pin-10
									CMP1_P0	Comparator-1 data output
									I2C1_SCL	I2C1 SCL signal
									URT0_TX	URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting.
									URT2_TX	URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting.
									URT1_TX	URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting.
									TM36_OC2H	TM36 output compare/PWM high channel-2
									TM36_OC2N	TM36 output compare/PWM complement channel-2
									CAN0_TX	CAN0 transmit TX signal. CAN0_RX and CAN0_TX can be swapped by register setting.
									URT7_TX	URT7 transmit TX signal. URT7_RX and URT7_TX can be swapped by register setting.
									LCD_P35	LCD drive pin
PC11	45	37	29		B	A		A,I,P,O,Q,U,H,C2	GPC11	GPIO/Interrupt/KBI Port-C function pin-11
									I2C1_SDA	I2C1 SDA signal

									URT0_RX	URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting.
									URT2_RX	URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.
									URT1_RX	URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.
									TM36_OC3H	TM36 output compare/PWM high channel-3
									TM26_OC01	TM26 output compare/PWM channel-01
									CAN0_RX	CAN0 receive RX signal. CAN0_RX and CAN0_TX can be swapped by register setting.
									URT7_RX	URT7 receive RX signal. URT7_RX and URT7_TX can be swapped by register setting.
									LCD_P36	LCD drive pin
PC12	46	38	30		B	A		A,I,P,O,Q,U,H,C2	GPC12	GPIO/Interrupt/KBI Port-C function pin-12
									IR_OUT	IR output signal
									URT1_DE	URT1 external drive enable output signal
									TM10_TRGO	TM10 trigger output signal
									TM36_OC3	TM36 output compare/PWM channel-3
									TM26_OC02	TM26 output compare/PWM channel-02
									SDT_P0	SDT output signal-0
									URT1_CLK	URT1 clock signal
									LCD_P37	LCD drive pin
PC13	47	39	31	20	B	A		A,I,P,O,Q,U,CF	GPC13	GPIO/Interrupt/KBI Port-C function pin-13
									XIN	External Xtal/OSC input
									URT1_NSS	URT1 SPI NSS input/output signal
									URT0_CTS	URT0 CTS input control signal
									URT2_RX	URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.
									TM10_ETR	TM10 external trigger/clock input signal
									TM26_ETR	TM26 external trigger/clock input signal
									TM36_OC00	TM36 output compare/PWM channel-00
									TM20_IC0	TM20 input capture channel-0
									SDT_I0	State detect input signal-0
									TM36_IC1	TM36 input capture channel-1
									URT6_RX	URT6 receive RX signal. URT6_RX and URT6_TX can be swapped by register setting.
PC14	48	40	32	21	B	A		A,I,P,O,Q,U,H,CF	GPC14	GPIO/Interrupt/KBI Port-C function pin-14
									XOUT	External Xtal output
									URT1_TMO	URT1 timeout timer overflow output signal
									URT0_RTS	URT0 RTS output control signal
									URT2_TX	URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting.
									TM10_CKO	TM10 timer overflow output signal

									TM26_TRGO	TM26 trigger output signal
									TM36_OC10	TM36 output compare/PWM channel-10
									TM20_IC1	TM20 input capture channel-1
									SDT_I1	State detect input signal-1
									SDT_P0	SDT output signal-0
									URT6_TX	URT6 transmit TX signal. URT6_RX and URT6_TX can be swapped by register setting.
PD0	54	42	33	22	B	A		A,I,P,O,U,H,C4	GPD0	GPIO/Interrupt/KBI Port-D function pin-0
									OBM_I0	Output signal break control input signal-0
									TM10_CKO	TM10 timer overflow output signal
									URT0_CLK	URT0 clock signal
									TM26_OC1N	TM26 output compare/PWM complement channel-1
									TM20_CKO	TM20 timer overflow output signal
									TM36_OC2	TM36 output compare/PWM channel-2
									SPI0_NSS	SPI0 slave select input/output signal
									TM36_IC3	TM36 input capture channel-3
									URT2_NSS	URT2 SPI NSS input/output signal
									LCD_C1	LCD charge pump capacitor pin
PD1	55	43	34	23	B	A		A,I,P,O,U,H,C4	GPD1	GPIO/Interrupt/KBI Port-D function pin-1
									OBM_I1	Output signal break control input signal-1
									TM16_CKO	TM16 timer overflow output signal
									URT0_CLK	URT0 clock signal
									NCO_CK0	NCO external clock input signal-0
									TM26_CKO	TM26 timer overflow output signal
									TM36_OC2N	TM36 output compare/PWM complement channel-2
									SPI0_CLK	SPI0 clock signal
									TM36_IC2	TM36 input capture channel-2
									URT2_CLK	URT2 clock signal
									LCD_C2	LCD charge pump capacitor pin
PD2	56	44	35	24	B	A		A,I,P,O,U,H,C4	GPD2	GPIO/Interrupt/KBI Port-D function pin-2
									MF_S0	Multi-Function signal-0 output
									TM00_CKO	TM00 timer overflow output signal
									URT1_CLK	URT1 clock signal
									TM26_OC00	TM26 output compare/PWM channel-00
									TM20_CKO	TM20 timer overflow output signal
									TM36_CKO	TM36 timer overflow output signal
									SPI0_MOSI	SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
									TM36_IC1	TM36 input capture channel-1
									URT2_TX	URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting.
									LCD_VT	LCD power top rail
PD3	57	45	36		B	A		A,I,P,O,U,H,C4	GPD3	GPIO/Interrupt/KBI Port-D function pin-3
									MF_S1	Multi-Function signal-1 output

									TM01_CKO	TM01 timer overflow output signal
									URT1_CLK	URT1 clock signal
									SPI0_MISO	SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
									TM26_CKO	TM26 timer overflow output signal
									SPI0_D3	SPI0 data-3 signal for 4-I/O mode
									TM36_TRGO	TM36 trigger output signal
									URT2_RX	URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.
									LCD_V1	LCD power rail 1
PD4	58	46			B	A		A,I,P,O,U,H,C4	GPD4	GPIO/Interrupt/KBI Port-D function pin-4
									TM00_TRGO	TM00 trigger output signal
									TM01_TRGO	TM01 trigger output signal
									URT1_TX	URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting.
									TM26_OC00	TM26 output compare/PWM channel-00
									SPI0_D2	SPI0 data-2 signal for 4-I/O mode
									URT2_TX	URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting.
									LCD_P38	LCD drive pin
PD5	59	47			B	A		A,I,P,O,U,H,C4	GPD5	GPIO/Interrupt/KBI Port-D function pin-5
									TM00_ETR	TM00 external trigger/clock input signal
									I2C0_SCL	I2C0 SCL signal
									URT1_RX	URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.
									TM26_OC01	TM26 output compare/PWM channel-01
									SPI0_MISO	SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
									URT2_RX	URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.
									LCD_P39	LCD drive pin
PD6	60	48			B	A		A,I,P,O,U,H,C2	GPD6	GPIO/Interrupt/KBI Port-D function pin-6
									CPU_NMI	CPU NMI external pin input
									I2C0_SDA	I2C0 SDA signal
									URT1_NSS	URT1 SPI NSS input/output signal
									SPI0_NSSI	SPI0 slave select input only signal
									TM26_OC02	TM26 output compare/PWM channel-02
									SPI0_NSS	SPI0 slave select input/output signal
									SDT_P0	SDT output signal-0
									URT2_NSS	URT2 SPI NSS input/output signal
									LCD_P40	LCD drive pin

PD7	61	49	37	25	B	A		A,I,P,O,U,H,C4	GPD7	GPIO/Interrupt/KBI Port-D function pin-7
									TM00_CKO	TM00 timer overflow output signal
									TM01_ETR	TM01 external trigger/clock input signal
									URT1_DE	URT1 external drive enable output signal
									SPI0_MISO	SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
									TM26_OC0N	TM26 output compare/PWM complement channel-0
									SPI0_D4	SPI0 data-0 signal for 2nd SPI device 4-I/O mode
									TM36_IC0	TM36 input capture channel-0
									TM36_OC3	TM36 output compare/PWM channel-3
									LCD_V2	LCD power rail 2
PD8	62	50	38		B	A		A,I,P,O,U,H,C4	GPD8	GPIO/Interrupt/KBI Port-D function pin-8
									CPU_TXEV	CPU wakeup event output
									TM01_TRGO	TM01 trigger output signal
									URT1_RTS	URT1 RTS output control signal
									SPI0_D2	SPI0 data-2 signal for 4-I/O mode
									TM26_OC10	TM26 output compare/PWM channel-10
									SPI0_D7	SPI0 data-3 signal for 2nd SPI device 4-I/O mode
									TM36_IC1	TM36 input capture channel-1
									SPI0_CLK	SPI0 clock signal
									LCD_P41	LCD drive pin
PD9	63	51	39		B	A		A,I,P,O,U,H,C2	GPD9	GPIO/Interrupt/KBI Port-D function pin-9
									CPU_RXEV	CPU wakeup event input
									TM00_TRGO	TM00 trigger output signal
									URT1_CTS	URT1 CTS input control signal
									SPI0_NSSI	SPI0 slave select input only signal
									TM26_OC11	TM26 output compare/PWM channel-11
									SPI0_D6	SPI0 data-2 signal for 2nd SPI device 4-I/O mode
									TM36_IC2	TM36 input capture channel-2
									SPI0_NSS	SPI0 slave select input/output signal
									LCD_V3	LCD power rail 3
PD10	64	52	40		B	A		A,I,P,O,U,H,C2	GPD10	GPIO/Interrupt/KBI Port-D function pin-10
									CPU_NMI	CPU NMI external pin input
									TM00_ETR	TM00 external trigger/clock input signal
									URT1_BRO	URT1 baud-rate timer overflow output signal
									RTC_OUT	RTC selection output signal
									TM26_OC12	TM26 output compare/PWM channel-12
									SPI0_D5	SPI0 data-1 signal for 2nd SPI device 4-I/O mode
									TM36_IC3	TM36 input capture channel-3
									SPI0_MOSI	SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.

									LCD_P42	LCD drive pin
PD11	65	53			B	A		A,I,P,O,U,H,C2	GPD11	GPIO/Interrupt/KBI Port-D function pin-11
									CPU_NMI	CPU NMI external pin input
									DMA_TRG1	DMA external trigger pin-1 input
									URT1_TMO	URT1 timeout timer overflow output signal
									SPI0_D3	SPI0 data-3 signal for 4-I/O mode
									TM26_OC1N	TM26 output compare/PWM complement channel-1
									SPI0_NSS	SPI0 slave select input/output signal
									ASB_P3	ASB output signal-3
									LCD_P43	LCD drive pin
PD12	66				B	A		A,I,P,O,U,H,C2	GPD12	GPIO/Interrupt/KBI Port-D function pin-12
									CMP0_P0	Comparator-0 data output
									TM10_CKO	TM10 timer overflow output signal
									OBM_P0	Output signal break control output signal-0
									TM00_CKO	TM00 timer overflow output signal
									SPI0_CLK	SPI0 clock signal
									TM20_OC0H	TM20 output compare/PWM high channel-0
									TM26_OC0H	TM26 output compare/PWM high channel-0
									URT1_CLK	URT1 clock signal
									URT2_CLK	URT2 clock signal
PD13	67				B	A		A,I,P,O,U,H,C2	GPD13	GPIO/Interrupt/KBI Port-D function pin-13
									CMP1_P0	Comparator-1 data output
									TM10_TRGO	TM10 trigger output signal
									OBM_P1	Output signal break control output signal-1
									TM00_TRGO	TM00 trigger output signal
									NCO_CK0	NCO external clock input signal-0
									TM20_OC1H	TM20 output compare/PWM high channel-1
									TM26_OC1H	TM26 output compare/PWM high channel-1
									ASB_P0	ASB output signal-0
PD14	68				B	A		A,I,P,O,U,H,C2	GPD14	GPIO/Interrupt/KBI Port-D function pin-14
									TM10_ETR	TM10 external trigger/clock input signal
									TM00_ETR	TM00 external trigger/clock input signal
									TM36_OC2	TM36 output compare/PWM channel-2
									TM20_IC0	TM20 input capture channel-0
									TM26_IC0	TM26 input capture channel-0
									CCL_P0	CCL output signal-0
									URT5_TX	URT5 transmit TX signal. URT5_RX and URT5_TX can be swapped by register setting.
PD15	69				B	A		A,I,P,O,U,H,C2	GPD15	GPIO/Interrupt/KBI Port-D function pin-15
									NCO_P0	NCO clock output signal-0
									IR_OUT	IR output signal
									DMA_TRG0	DMA external trigger pin-0 input
									TM36_OC3	TM36 output compare/PWM channel-3
									TM20_IC1	TM20 input capture channel-1
									TM26_IC1	TM26 input capture channel-1
									CCL_P1	CCL output signal-1

									URT5_RX	URT5 receive RX signal. URT5_RX and URT5_TX can be swapped by register setting.
PE0	14				B	A		A,I,P,O,U,H,C4	GPE0	GPIO/Interrupt/KBI Port-E function pin-0
									OBM_I0	Output signal break control input signal-0
									URT0_TX	URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting.
									SPI0_NSS	SPI0 slave select input/output signal
									TM20_OC00	TM20 output compare/PWM channel-00
									TM26_OC00	TM26 output compare/PWM channel-00
									URT4_TX	URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.
PE1	15				B	A		A,I,P,O,U,H,C4	GPE1	GPIO/Interrupt/KBI Port-E function pin-1
									OBM_I1	Output signal break control input signal-1
									URT0_RX	URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting.
									DMA_TRG1	DMA external trigger pin-1 input
									SPI0_MISO	SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
									TM20_OC01	TM20 output compare/PWM channel-01
									TM26_OC01	TM26 output compare/PWM channel-01
									TM36_OC0H	TM36 output compare/PWM high channel-0
									URT4_RX	URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.
PE2	16				B	A		A,I,P,O,U,H,C4	GPE2	GPIO/Interrupt/KBI Port-E function pin-2
									OBM_P0	Output signal break control output signal-0
									I2C1_SCL	I2C1 SCL signal
									URT1_TX	URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting.
									NCO_P0	NCO clock output signal-0
									SPI0_CLK	SPI0 clock signal
									TM20_OC02	TM20 output compare/PWM channel-02
									TM26_OC02	TM26 output compare/PWM channel-02
									TM36_OC1H	TM36 output compare/PWM high channel-1
									URT5_TX	URT5 transmit TX signal. URT5_RX and URT5_TX can be swapped by register setting.
PE3	17				B	A		A,I,P,O,U,H,C4	GPE3	GPIO/Interrupt/KBI Port-E function pin-3
									OBM_P1	Output signal break control output signal-1
									I2C1_SDA	I2C1 SDA signal
									URT1_RX	URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.
									NCO_CK0	NCO external clock input signal-0
									SPI0_MOSI	SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and

										SPI0_MISO can be swapped by register setting.
									TM20_OC0N	TM20 output compare/PWM complement channel-0
									TM26_OC0N	TM26 output compare/PWM complement channel-0
									URT5_RX	URT5 receive RX signal. URT5_RX and URT5_TX can be swapped by register setting.
PE8	32				B	A		A,I,P,O,U,H,C2	GPE8	GPIO/Interrupt/KBI Port-E function pin-8
									CPU_TXEV	CPU wakeup event output
									OBM_I0	Output signal break control input signal-0
									URT2_TX	URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting.
									SDT_I0	State detect input signal-0
									TM36_CKO	TM36 timer overflow output signal
									TM20_CKO	TM20 timer overflow output signal
									TM26_CKO	TM26 timer overflow output signal
									SPI0_D3	SPI0 data-3 signal for 4-I/O mode
									URT4_TX	URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.
PE9	33				B	A		A,I,P,O,U,H,C2	GPE9	GPIO/Interrupt/KBI Port-E function pin-9
									CPU_RXEV	CPU wakeup event input
									OBM_I1	Output signal break control input signal-1
									URT2_RX	URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.
									SDT_I1	State detect input signal-1
									TM36_TRGO	TM36 trigger output signal
									TM20_TRGO	TM20 trigger output signal
									TM26_TRGO	TM26 trigger output signal
									SPI0_D2	SPI0 data-2 signal for 4-I/O mode
									URT4_RX	URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.
PE12	50				B	A		A,I,P,O,U,H,C2	GPE12	GPIO/Interrupt/KBI Port-E function pin-12
									ADC0_TRG	ADC trigger start input
									MF_S0	Multi-Function signal-0 output
									TM01_CKO	TM01 timer overflow output signal
									TM16_CKO	TM16 timer overflow output signal
									TM20_OC10	TM20 output compare/PWM channel-10
									TM26_OC10	TM26 output compare/PWM channel-10
									URT6_TX	URT6 transmit TX signal. URT6_RX and URT6_TX can be swapped by register setting.
PE13	51				B	A		A,I,P,O,U,H,C2	GPE13	GPIO/Interrupt/KBI Port-E function pin-13
									ADC0_OUT	ADC threshold window compare output
									MF_S1	Multi-Function signal-1 output
									TM01_TRGO	TM01 trigger output signal
									TM16_TRGO	TM16 trigger output signal

									TM20_OC11	TM20 output compare/PWM channel-11
									TM26_OC11	TM26 output compare/PWM channel-11
									TM36_OC2H	TM36 output compare/PWM high channel-2
									URT6_RX	URT6 receive RX signal. URT6_RX and URT6_TX can be swapped by register setting.
PE14	52				B	A		A,I,P,O,U,H,C2	GPE14	GPIO/Interrupt/KBI Port-E function pin-14
									RTC_OUT	RTC selection output signal
									I2C1_SCL	I2C1 SCL signal
									CAN0_TX	CAN0 transmit TX signal. CAN0_RX and CAN0_TX can be swapped by register setting.
									TM01_ETR	TM01 external trigger/clock input signal
									TM16_ETR	TM16 external trigger/clock input signal
									TM20_OC12	TM20 output compare/PWM channel-12
									TM26_OC12	TM26 output compare/PWM channel-12
									CCL_P0	CCL output signal-0
									TM36_OC3H	TM36 output compare/PWM high channel-3
									URT7_TX	URT7 transmit TX signal. URT7_RX and URT7_TX can be swapped by register setting.
PE15	53				B	A		A,I,P,O,U,H,C2	GPE15	GPIO/Interrupt/KBI Port-E function pin-15
									RTC_TS	RTC time stamp input signal
									I2C1_SDA	I2C1 SDA signal
									CAN0_RX	CAN0 receive RX signal. CAN0_RX and CAN0_TX can be swapped by register setting.
									TM36_BK0	TM36 break input signal
									TM36_ETR	TM36 external trigger/clock input signal
									TM20_OC1N	TM20 output compare/PWM complement channel-1
									TM26_OC1N	TM26 output compare/PWM complement channel-1
									CCL_P1	CCL output signal-1
									URT7_RX	URT7 receive RX signal. URT7_RX and URT7_TX can be swapped by register setting.
VSS	70	54	41	26	P					IO/Core/ADC ground
VSS2	30				P					IO ground
VSS1	49	41			P					IO ground
VCAP	71	55	42	27	AO	AO				Core power supply/LDO output (place 0.1uF+4.7uF capacitors and close pin)
VDD	72	56	43	28	P					IO power supply/LDO input (place 0.1uF+10uF capacitors and close pin)
VDD2	27				P					IO power supply (place 0.1uF+10uF capacitors and close pin)
VREF+	73	57	44		AI	AI				ADC voltage reference (place 0.1uF+4.7uF capacitors and close pin)

4.3. Pin AFS Summary Table

The following table is the AFS signal list of the related IO pin for all pins' summary. (AFS=n, n: I/O pin AFS setting value)

Table 4-7. Pin AFS Summary Table

Pin	AFS=0	AFS=1	AFS=2	AFS=3	AFS=4	AFS=5	AFS=6	AFS=7	AFS=8	AFS=9	AFS=10	AFS=11	AFS=12
PA0	GPA0		ASB_P0	NCO_P0		TM20_CKO	SDT_P0	CCL_P0			TM36_OC00	URT4_TX	
PA1	GPA1	CPU_NMI	ASB_P1	NCO_CK0	URT1_BRO	TM20_OC10		CCL_P1			TM36_OC10	URT4_RX	LCD_P0
PA2	GPA2	CPU_RXEV	ASB_P2	ASB_CK0	URT1_CTS	CAN0_TX	SDT_I0	SPI0_CLK			TM36_OC2	URT5_TX	LCD_P1
PA3	GPA3	CPU_TXEV	ASB_P3	ASB_CK1	URT1_RTS	CAN0_RX	SDT_I1	SPI0_MOSI			TM36_OC2N	URT5_RX	LCD_P2
PA4	GPA4		ASB_CK0								TM20_OC00	URT0_TX	LCD_P3
PA5	GPA5		ASB_CK1								TM20_OC10	URT0_RX	LCD_P4
PA6	GPA6		ASB_P2					SPI0_D3			TM20_OC0H	URT0_CLK	LCD_P5
PA7	GPA7		ASB_P3					SPI0_D2			TM20_OC1H	URT0_NSS	LCD_P6
PA8	GPA8	DMA_TRG0	ASB_P0	I2C0_SCL	URT2_BRO	SDT_I0	TM20_IC0	SPI0_NSS			TM36_OC0H	URT4_TX	LCD_P7
PA9	GPA9	DMA_TRG1	ASB_P1	I2C1_SCL	URT2_TMO	ASB_CK0	TM20_IC1	SPI0_MISO			TM36_OC1H	URT5_TX	LCD_P8
PA10	GPA10	TM36_BK0	SPI0_D2	I2C0_SDA	URT2_CTS	SDT_I1	TM26_IC0	SPI0_CLK			TM36_OC2H	URT4_RX	LCD_P9
PA11	GPA11		SPI0_D3	I2C1_SDA	URT2_RTS	TM20_OC1N	TM26_IC1	SPI0_MOSI			TM36_OC3H	URT5_RX	LCD_P10
PA12	GPA12		MF_S0		URT1_BRO	TM10_ETR	TM36_IC0	SPI0_D5			TM26_OC00	URT6_TX	LCD_P11
PA13	GPA13	CPU_TXEV	MF_S1	URT0_BRO	URT1_TMO	TM10_TRGO	TM36_IC1	SPI0_D6			TM26_OC10	URT6_RX	LCD_P12
PA14	GPA14	CPU_RXEV	OBM_I0	URT0_TMO	URT1_CTS	TM16_ETR	TM36_IC2	SPI0_D7			TM26_OC0H	URT7_TX	LCD_P13
PA15	GPA15	CPU_NMI	OBM_I1	URT0_DE	URT1_RTS	TM16_TRGO	TM36_IC3	SPI0_D4			TM26_OC1H	URT7_RX	LCD_P14
PB0	GPB0	I2C1_SCL	SPI0_NSS	TM01_ETR	TM00_CKO	TM16_ETR	TM26_IC0	TM36_ETR		URT1_NSS	URT2_NSS	URT6_TX	LCD_P15
PB1	GPB1	I2C1_SDA	SPI0_MISO	TM01_TRGO	TM10_CKO	TM16_TRGO	TM26_IC1	TM36_TRGO	TM00_TRGO	URT1_RX	URT2_CLK	URT6_RX	LCD_P16
PB2	GPB2	ADC0_TRG	SPI0_CLK	TM01_CKO	URT2_TX	TM16_CKO	TM26_OC0H	I2C0_SDA	TM10_TRGO	URT1_CLK	URT0_TX	URT7_TX	LCD_P17
PB3	GPB3	ADC0_OUT	SPI0_MOSI	NCO_P0	URT2_RX	TM36_CKO	TM26_OC1H	I2C0_SCL	TM20_TRGO	URT1_TX	URT0_RX	URT7_RX	LCD_P18
PB4	GPB4	TM01_CKO	SPI0_D3	TM26_TRGO	URT2_CLK	TM20_IC0	TM36_IC0						LCD_P19
PB5	GPB5	TM16_CKO	SPI0_D2	TM26_ETR	URT2_NSS	TM20_IC1	TM36_IC1						LCD_P20
PB6	GPB6	CPU_RXEV	SPI0_NSSI	URT0_BRO	URT2_CTS	TM20_ETR	TM36_IC2	CAN0_TX				URT2_TX	LCD_P21
PB7	GPB7	CPU_TXEV		URT0_TMO	URT2_RTS	TM20_TRGO	TM36_IC3	CAN0_RX				URT2_RX	LCD_P22
PB8	GPB8	CMP0_P0	RTC_OUT	URT0_TX	URT2_BRO	TM20_OC01	TM36_OC01	SPI0_D3		SDT_P0	OBM_P0	URT4_TX	
PB9	GPB9	CMP1_P0	RTC_TS	URT0_RX	URT2_TMO	TM20_OC02	TM36_OC02	SPI0_D2			OBM_P1	URT4_RX	
PB10	GPB10		I2C0_SCL	URT0_NSS	URT2_DE	TM20_OC11	TM36_OC11	URT1_TX			SPI0_NSSI	TM00_ETR	LCD_P23
PB11	GPB11		I2C0_SDA	URT0_DE	IR_OUT	TM20_OC12	TM36_OC12	URT1_RX			DMA_TRG0	URT0_CLK	LCD_P24
PB12	GPB12	DMA_TRG0	NCO_P0	MF_S0		ASB_P0		URT1_CLK				URT5_TX	LCD_P25
PB13	GPB13		TM00_ETR	URT0_CTS		TM20_ETR	TM36_ETR	URT0_CLK			CCL_P0	URT4_RX	LCD_P26
PB14	GPB14	DMA_TRG0	TM00_TRGO	URT0_RTS		TM20_TRGO	TM36_BK0	URT0_NSS			CCL_P1	URT4_TX	LCD_P27
PB15	GPB15	IR_OUT	NCO_CK0	MF_S1		ASB_P1		URT1_NSS			URT2_NSS	URT5_RX	LCD_P28
PC0	GPC0	ICKO	TM00_CKO	URT0_CLK	URT2_CLK	TM20_OC00	TM36_OC00	I2C0_SCL			URT0_TX	URT5_TX	TM36_IC0
PC1	GPC1	ADC0_TRG	TM01_CKO	TM36_IC0	URT1_CLK	TM20_OC0N	TM36_OC0N	I2C0_SDA			URT0_RX	URT5_RX	LCD_P29
PC2	GPC2	ADC0_OUT	TM10_CKO	OBM_P0	URT2_CLK	TM20_OC10	TM36_OC10	SDT_I0			MF_S0		LCD_P30
PC3	GPC3	OBM_P1	TM16_CKO	URT0_CLK	URT1_CLK	TM20_OC1N	TM36_OC1N	SDT_I1			MF_S1		LCD_P31
PC4	GPC4	SWCLK	I2C0_SCL	URT0_RX	URT1_RX	TM36_IC2	TM36_OC2	SDT_I0			SDT_P0	URT6_RX	
PC5	GPC5	SWDIO	I2C0_SDA	URT0_TX	URT1_TX	TM36_IC3	TM36_OC3	SDT_I1				URT6_TX	
PC6	GPC6	RSTN	RTC_TS	URT0_NSS	URT1_NSS	TM20_ETR	TM26_ETR					TM36_OC1N	
PC7	GPC7	ADC0_TRG	RTC_OUT	URT0_DE	URT1_NSS	ASB_P2	TM36_TRGO						LCD_P32
PC8	GPC8	ADC0_OUT	I2C0_SCL	URT0_BRO	URT1_TX	TM20_OC0H	TM36_OC0H	TM36_OC0N			CCL_P0	URT6_TX	LCD_P33
PC9	GPC9	CMP0_P0	I2C0_SDA	URT0_TMO	URT1_RX	TM20_OC1H	TM36_OC1H	TM36_OC1N			CCL_P1	URT6_RX	LCD_P34
PC10	GPC10	CMP1_P0	I2C1_SCL	URT0_TX	URT2_TX	URT1_TX	TM36_OC2H	TM36_OC2N			CAN0_TX	URT7_TX	LCD_P35
PC11	GPC11		I2C1_SDA	URT0_RX	URT2_RX	URT1_RX	TM36_OC3H	TM26_OC01			CAN0_RX	URT7_RX	LCD_P36
PC12	GPC12		IR_OUT		URT1_DE	TM10_TRGO	TM36_OC3	TM26_OC02		SDT_P0	URT1_CLK		LCD_P37
PC13	GPC13	XIN	URT1_NSS	URT0_CTS	URT2_RX	TM10_ETR	TM26_ETR	TM36_OC00	TM20_IC0	SDT_I0	TM36_IC1	URT6_RX	

PC14	GPC14	XOUT	URT1_TMO	URT0_RTS	URT2_TX	TM10_CKO	TM26_TRGO	TM36_OC10	TM20_IC1	SDT_I1	SDT_P0	URT6_TX	
PD0	GPD0	OBM_I0	TM10_CKO	URT0_CLK	TM26_OC1N	TM20_CKO	TM36_OC2	SPI0_NSS			TM36_IC3	URT2_NSS	
PD1	GPD1	OBM_I1	TM16_CKO	URT0_CLK	NCO_CK0	TM26_CKO	TM36_OC2N	SPI0_CLK			TM36_IC2	URT2_CLK	
PD2	GPD2	MF_S0	TM00_CKO	URT1_CLK	TM26_OC00	TM20_CKO	TM36_CKO	SPI0_MOSI			TM36_IC1	URT2_TX	
PD3	GPD3	MF_S1	TM01_CKO	URT1_CLK		SPI0_MISO	TM26_CKO	SPI0_D3			TM36_TRGO	URT2_RX	
PD4	GPD4	TM00_TRGO	TM01_TRGO	URT1_TX			TM26_OC00	SPI0_D2				URT2_TX	LCD_P38
PD5	GPD5	TM00_ETR	I2C0_SCL	URT1_RX			TM26_OC01	SPI0_MISO				URT2_RX	LCD_P39
PD6	GPD6	CPU_NMI	I2C0_SDA	URT1_NSS		SPI0_NSSI	TM26_OC02	SPI0_NSS		SDT_P0		URT2_NSS	LCD_P40
PD7	GPD7	TM00_CKO	TM01_ETR	URT1_DE		SPI0_MISO	TM26_OC0N	SPI0_D4			TM36_IC0	TM36_OC3	
PD8	GPD8	CPU_TXEV	TM01_TRGO	URT1_RTS		SPI0_D2	TM26_OC10	SPI0_D7			TM36_IC1	SPI0_CLK	LCD_P41
PD9	GPD9	CPU_RXEV	TM00_TRGO	URT1_CTS		SPI0_NSSI	TM26_OC11	SPI0_D6			TM36_IC2	SPI0_NSS	
PD10	GPD10	CPU_NMI	TM00_ETR	URT1_BRO		RTC_OUT	TM26_OC12	SPI0_D5			TM36_IC3	SPI0_MOSI	LCD_P42
PD11	GPD11	CPU_NMI	DMA_TRG1	URT1_TMO		SPI0_D3	TM26_OC1N	SPI0_NSS			ASB_P3		LCD_P43
PD12	GPD12	CMP0_P0	TM10_CKO	OBM_P0	TM00_CKO	SPI0_CLK	TM20_OC0H	TM26_OC0H			URT1_CLK	URT2_CLK	
PD13	GPD13	CMP1_P0	TM10_TRGO	OBM_P1	TM00_TRGO	NCO_CK0	TM20_OC1H	TM26_OC1H			ASB_P0		
PD14	GPD14		TM10_ETR		TM00_ETR	TM36_OC2	TM20_IC0	TM26_IC0			CCL_P0	URT5_TX	
PD15	GPD15		NCO_P0	IR_OUT	DMA_TRG0	TM36_OC3	TM20_IC1	TM26_IC1			CCL_P1	URT5_RX	
PE0	GPE0	OBM_I0		URT0_TX		SPI0_NSS	TM20_OC00	TM26_OC00				URT4_TX	
PE1	GPE1	OBM_I1		URT0_RX	DMA_TRG1	SPI0_MISO	TM20_OC01	TM26_OC01			TM36_OC0H	URT4_RX	
PE2	GPE2	OBM_P0	I2C1_SCL	URT1_TX	NCO_P0	SPI0_CLK	TM20_OC02	TM26_OC02			TM36_OC1H	URT5_TX	
PE3	GPE3	OBM_P1	I2C1_SDA	URT1_RX	NCO_CK0	SPI0_MOSI	TM20_OC0N	TM26_OC0N				URT5_RX	
PE8	GPE8	CPU_TXEV	OBM_I0	URT2_TX	SDT_I0	TM36_CKO	TM20_CKO	TM26_CKO			SPI0_D3	URT4_TX	
PE9	GPE9	CPU_RXEV	OBM_I1	URT2_RX	SDT_I1	TM36_TRGO	TM20_TRGO	TM26_TRGO			SPI0_D2	URT4_RX	
PE12	GPE12	ADC0_TRG	MF_S0		TM01_CKO	TM16_CKO	TM20_OC10	TM26_OC10				URT6_TX	
PE13	GPE13	ADC0_OUT	MF_S1		TM01_TRGO	TM16_TRGO	TM20_OC11	TM26_OC11			TM36_OC2H	URT6_RX	
PE14	GPE14	RTC_OUT	I2C1_SCL	CAN0_TX	TM01_ETR	TM16_ETR	TM20_OC12	TM26_OC12		CCL_P0	TM36_OC3H	URT7_TX	
PE15	GPE15	RTC_TS	I2C1_SDA	CAN0_RX	TM36_BK0	TM36_ETR	TM20_OC1N	TM26_OC1N		CCL_P1		URT7_RX	
Pin	AFS=0	AFS=1	AFS=2	AFS=3	AFS=4	AFS=5	AFS=6	AFS=7	AFS=8	AFS=9	AFS=10	AFS=11	AFS=12

[Package Pin Group Indication by Background Color]

Light Purple Color : Not supported High Speed Pins

4.4. Analog Function Pin Table

The following table is the analog signal pin list for all the analog function.

Table 4-8. Analog Function Pin Table

Pin Name	ANA0	ANA1	ANA2
PA0	ADC_I0		OP0_P0
PA1	ADC_I1		
PA2	ADC_I2		
PA3	ADC_I3		
PA4	ADC_I4		OP0_I0
PA5	ADC_I5		OP0_I1
PA6	ADC_I6		
PA7	ADC_I7		
PA8	ADC_I8	CMP0_I0	
PA9	ADC_I9	CMP0_I1	
PA10	ADC_I10	CMP1_I0	
PA11	ADC_I11	CMP1_I1	
PA12	ADC_I12		
PA13	ADC_I13		ADC_PGA
PA14	ADC_I14		
PA15	ADC_I15		
PB0		CMP_C0	
PB1		CMP_C1	
PD0		LCD_C1	
PD1		LCD_C2	
PD2		LCD_VT	
PD3		LCD_V1	
PD7		LCD_V2	
PD9		LCD_V3	

4.5. Alternate Functions Pin List

The following table is the pin list of the related AFS IO signal for all AFS signals' summary.

Table 4-9. Alternate Functions Pin List

No.	AFS List		Pin List for the AFS IO ([ ] : AFS setting value)							
	Group	AFS Name	Pin-1 Name	Pin-2 Name	Pin-3 Name	Pin-4 Name	Pin-5 Name	Pin-6 Name	Pin-7 Name	Pin-8 Name
1	GPA	GPA0	PA0 [0]							
2		GPA1	PA1 [0]							
3		GPA2	PA2 [0]							
4		GPA3	PA3 [0]							
5		GPA4	PA4 [0]							
6		GPA5	PA5 [0]							
7		GPA6	PA6 [0]							
8		GPA7	PA7 [0]							
9		GPA8	PA8 [0]							
10		GPA9	PA9 [0]							
11		GPA10	PA10 [0]							
12		GPA11	PA11 [0]							
13		GPA12	PA12 [0]							
14		GPA13	PA13 [0]							
15		GPA14	PA14 [0]							
16		GPA15	PA15 [0]							
17	GPB	GPB0	PB0 [0]							
18		GPB1	PB1 [0]							
19		GPB2	PB2 [0]							
20		GPB3	PB3 [0]							
21		GPB4	PB4 [0]							
22		GPB5	PB5 [0]							
23		GPB6	PB6 [0]							
24		GPB7	PB7 [0]							
25		GPB8	PB8 [0]							
26		GPB9	PB9 [0]							
27		GPB10	PB10 [0]							
28		GPB11	PB11 [0]							
29		GPB12	PB12 [0]							
30		GPB13	PB13 [0]							
31		GPB14	PB14 [0]							
32		GPB15	PB15 [0]							
33	GPC	GPC0	PC0 [0]							
34		GPC1	PC1 [0]							
35		GPC2	PC2 [0]							
36		GPC3	PC3 [0]							
37		GPC4	PC4 [0]							
38		GPC5	PC5 [0]							
39		GPC6	PC6 [0]							
40		GPC7	PC7 [0]							
41		GPC8	PC8 [0]							

42		GPC9	PC9 [0]							
43		GPC10	PC10 [0]							
44		GPC11	PC11 [0]							
45		GPC12	PC12 [0]							
46		GPC13	PC13 [0]							
47		GPC14	PC14 [0]							
48	GPD	GPD0	PD0 [0]							
49		GPD1	PD1 [0]							
50		GPD2	PD2 [0]							
51		GPD3	PD3 [0]							
52		GPD4	PD4 [0]							
53		GPD5	PD5 [0]							
54		GPD6	PD6 [0]							
55		GPD7	PD7 [0]							
56		GPD8	PD8 [0]							
57		GPD9	PD9 [0]							
58		GPD10	PD10 [0]							
59		GPD11	PD11 [0]							
60		GPD12	PD12 [0]							
61		GPD13	PD13 [0]							
62		GPD14	PD14 [0]							
63		GPD15	PD15 [0]							
64	GPE	GPE0	PE0 [0]							
65		GPE1	PE1 [0]							
66		GPE2	PE2 [0]							
67		GPE3	PE3 [0]							
68		GPE8	PE8 [0]							
69		GPE9	PE9 [0]							
70		GPE12	PE12 [0]							
71		GPE13	PE13 [0]							
72		GPE14	PE14 [0]							
73		GPE15	PE15 [0]							
74	Chip	SWCLK	PC4 [1]							
75		SWDIO	PC5 [1]							
76		RSTN	PC6 [1]							
77		ICKO	PC0 [1]							
78		XIN	PC13 [1]							
79		XOUT	PC14 [1]							
80		CPU_TXEV	PA3 [1]	PA13 [1]	PB7 [1]	PD8 [1]	PE8 [1]			
81		CPU_RXEV	PA2 [1]	PA14 [1]	PB6 [1]	PD9 [1]	PE9 [1]			
82		CPU_NMI	PA1 [1]	PA15 [1]	PD6 [1]	PD10 [1]	PD11 [1]			
83	ANAIO	ADC0_TRG	PB2 [1]	PC1 [1]	PC7 [1]	PE12 [1]				
84		ADC0_OUT	PB3 [1]	PC2 [1]	PC8 [1]	PE13 [1]				
85		CMP0_P0	PB8 [1]	PC9 [1]	PD12 [1]					
86		CMP1_P0	PB9 [1]	PC10 [1]	PD13 [1]					
87	I2C0	I2C0_SCL	PA8 [3]	PB3 [7]	PB10 [2]	PC0 [7]	PC4 [2]	PC8 [2]	PD5 [2]	
88		I2C0_SDA	PA10 [3]	PB2 [7]	PB11 [2]	PC1 [7]	PC5 [2]	PC9 [2]	PD6 [2]	
89	I2C1	I2C1_SCL	PA9 [3]	PB0 [1]	PC10 [2]	PE2 [2]	PE14 [2]			

90		I2C1_SDA	PA11 [3]	PB1 [1]	PC11 [2]	PE3 [2]	PE15 [2]			
91	URT0	URT0_TX	PA4 [11]	PB2 [10]	PB8 [3]	PC5 [3]	PC10 [3]	PE0 [3]	PC0 [10]	
92		URT0_RX	PA5 [11]	PB3 [10]	PB9 [3]	PC4 [3]	PC11 [3]	PE1 [3]	PC1 [10]	
93		URT0_CLK	PA6 [11]	PC0 [3]	PC3 [3]	PD0 [3]	PD1 [3]	PB11 [11]	PB13 [7]	
94		URT0_NSS	PA7 [11]	PB10 [3]	PC6 [3]	PB14 [7]				
95		URT0_BRO	PA13 [3]	PB6 [3]	PC8 [3]					
96		URT0_TMO	PA14 [3]	PB7 [3]	PC9 [3]					
97		URT0_DE	PA15 [3]	PB11 [3]	PC7 [3]					
98		URT0_CTS	PB13 [3]	PC13 [3]						
99		URT0_RTS	PB14 [3]	PC14 [3]						
100	URT1	URT1_TX	PB3 [9]	PB10 [7]	PC5 [4]	PC8 [4]	PC10 [5]	PD4 [3]	PE2 [3]	
101		URT1_RX	PB1 [9]	PB11 [7]	PC4 [4]	PC9 [4]	PC11 [5]	PD5 [3]	PE3 [3]	
102		URT1_CLK	PB2 [9]	PB12 [7]	PC1 [4]	PC3 [4]	PC12 [10]	PD2 [3]	PD3 [3]	PD12 [10]
103		URT1_NSS	PB0 [9]	PB15 [7]	PC6 [4]	PC7 [4]	PC13 [2]	PD6 [3]		
104		URT1_BRO	PA1 [4]	PA12 [4]	PD10 [3]					
105		URT1_TMO	PA13 [4]	PC14 [2]	PD11 [3]					
106		URT1_DE	PD7 [3]	PC12 [4]						
107		URT1_CTS	PA2 [4]	PA14 [4]	PD9 [3]					
108		URT1_RTS	PA3 [4]	PA15 [4]	PD8 [3]					
109	URT2	URT2_TX	PB2 [4]	PC10 [4]	PC14 [4]	PD2 [11]	PD4 [11]	PE8 [3]	PB6 [11]	
110		URT2_RX	PB3 [4]	PC11 [4]	PC13 [4]	PD3 [11]	PD5 [11]	PE9 [3]	PB7 [11]	
111		URT2_CLK	PB1 [10]	PB4 [4]	PC0 [4]	PC2 [4]	PD1 [11]	PD12 [11]		
112		URT2_NSS	PB0 [10]	PB5 [4]	PB15 [10]	PD0 [11]	PD6 [11]			
113		URT2_BRO	PA8 [4]	PB8 [4]						
114		URT2_TMO	PA9 [4]	PB9 [4]						
115		URT2_DE	PB10 [4]							
116		URT2_CTS	PA10 [4]	PB6 [4]						
117		URT2_RTS	PA11 [4]	PB7 [4]						
118	URT4567	URT4_TX	PA0 [11]	PA8 [11]	PB8 [11]	PB14 [11]	PE0 [11]	PE8 [11]		
119		URT4_RX	PA1 [11]	PA10 [11]	PB9 [11]	PB13 [11]	PE1 [11]	PE9 [11]		
120		URT5_TX	PA2 [11]	PA9 [11]	PB12 [11]	PC0 [11]	PD14 [11]	PE2 [11]		
121		URT5_RX	PA3 [11]	PA11 [11]	PB15 [11]	PC1 [11]	PD15 [11]	PE3 [11]		
122		URT6_TX	PA12 [11]	PB0 [11]	PC5 [11]	PC8 [11]	PC14 [11]	PE12 [11]		
123		URT6_RX	PA13 [11]	PB1 [11]	PC4 [11]	PC9 [11]	PC13 [11]	PE13 [11]		
124		URT7_TX	PA14 [11]	PB2 [11]	PC10 [11]	PE14 [11]				
125		URT7_RX	PA15 [11]	PB3 [11]	PC11 [11]	PE15 [11]				
126	SPI0	SPI0_CLK	PA2 [7]	PB2 [2]	PD12 [5]	PE2 [5]	PA10 [7]	PD1 [7]	PD8 [11]	
127		SPI0_MOSI	PA3 [7]	PB3 [2]	PE3 [5]	PA11 [7]	PD2 [7]	PD10 [11]		
128		SPI0_MISO	PB1 [2]	PD3 [5]	PD7 [5]	PE1 [5]	PA9 [7]	PD5 [7]		
129		SPI0_NSS	PB0 [2]	PD0 [7]	PE0 [5]	PA8 [7]	PD6 [7]	PD11 [7]	PD9 [11]	
130		SPI0_D2	PA10 [2]	PB5 [2]	PB9 [7]	PD8 [5]	PE9 [10]	PA7 [7]	PD4 [7]	
131		SPI0_D3	PA11 [2]	PB4 [2]	PB8 [7]	PD11 [5]	PE8 [10]	PA6 [7]	PD3 [7]	
132		SPI0_NSSI	PB6 [2]	PB10 [10]	PD6 [5]	PD9 [5]				
133		SPI0_D4	PA15 [7]	PD7 [7]						
134		SPI0_D5	PA12 [7]	PD10 [7]						
135		SPI0_D6	PA13 [7]	PD9 [7]						
136		SPI0_D7	PA14 [7]	PD8 [7]						
137	TM00	TM00_CKO	PB0 [4]	PC0 [2]	PD2 [2]	PD7 [1]	PD12 [4]			

138		TM00_TRGO	PB1 [8]	PB14 [2]	PD4 [1]	PD9 [2]	PD13 [4]			
139		TM00_ETR	PB10 [11]	PB13 [2]	PD5 [1]	PD10 [2]	PD14 [4]			
140	TM01	TM01_CKO	PB2 [3]	PB4 [1]	PC1 [2]	PD3 [2]	PE12 [4]			
141		TM01_TRGO	PB1 [3]	PD4 [2]	PD8 [2]	PE13 [4]				
142		TM01_ETR	PB0 [3]	PD7 [2]	PE14 [4]					
143	TM10	TM10_CKO	PB1 [4]	PC2 [2]	PC14 [5]	PD0 [2]	PD12 [2]			
144		TM10_TRGO	PA13 [5]	PB2 [8]	PC12 [5]	PD13 [2]				
145		TM10_ETR	PA12 [5]	PC13 [5]	PD14 [2]					
146	TM16	TM16_CKO	PB2 [5]	PB5 [1]	PC3 [2]	PD1 [2]	PE12 [5]			
147		TM16_TRGO	PA15 [5]	PB1 [5]	PE13 [5]					
148		TM16_ETR	PA14 [5]	PB0 [5]	PE14 [5]					
149	TM20	TM20_CKO	PA0 [5]	PD0 [5]	PD2 [5]	PE8 [6]				
150		TM20_TRGO	PB3 [8]	PB7 [5]	PB14 [5]	PE9 [6]				
151		TM20_ETR	PB6 [5]	PB13 [5]	PC6 [5]					
152		TM20_IC0	PA8 [6]	PB4 [5]	PC13 [8]	PD14 [6]				
153		TM20_IC1	PA9 [6]	PB5 [5]	PC14 [8]	PD15 [6]				
154		TM20_OC00	PA4 [10]	PC0 [5]	PE0 [6]					
155		TM20_OC01	PB8 [5]	PE1 [6]						
156		TM20_OC02	PB9 [5]	PE2 [6]						
157		TM20_OC0N	PC1 [5]	PE3 [6]						
158		TM20_OC10	PA1 [5]	PA5 [10]	PC2 [5]	PE12 [6]				
159		TM20_OC11	PB10 [5]	PE13 [6]						
160		TM20_OC12	PB11 [5]	PE14 [6]						
161		TM20_OC1N	PA11 [5]	PC3 [5]	PE15 [6]					
162		TM20_OC0H	PA6 [10]	PC8 [5]	PD12 [6]					
163		TM20_OC1H	PA7 [10]	PC9 [5]	PD13 [6]					
164	TM26	TM26_CKO	PD1 [5]	PD3 [6]	PE8 [7]					
165		TM26_TRGO	PB4 [3]	PC14 [6]	PE9 [7]					
166		TM26_ETR	PB5 [3]	PC6 [6]	PC13 [6]					
167		TM26_IC0	PA10 [6]	PB0 [6]	PD14 [7]					
168		TM26_IC1	PA11 [6]	PB1 [6]	PD15 [7]					
169		TM26_OC00	PA12 [10]	PD2 [4]	PD4 [6]	PE0 [7]				
170		TM26_OC01	PC11 [7]	PD5 [6]	PE1 [7]					
171		TM26_OC02	PC12 [7]	PD6 [6]	PE2 [7]					
172		TM26_OC0N	PD7 [6]	PE3 [7]						
173		TM26_OC10	PA13 [10]	PD8 [6]	PE12 [7]					
174		TM26_OC11	PD9 [6]	PE13 [7]						
175		TM26_OC12	PD10 [6]	PE14 [7]						
176		TM26_OC1N	PD0 [4]	PD11 [6]	PE15 [7]					
177		TM26_OC0H	PA14 [10]	PB2 [6]	PD12 [7]					
178		TM26_OC1H	PA15 [10]	PB3 [6]	PD13 [7]					
179	TM36	TM36_CKO	PB3 [5]	PD2 [6]	PE8 [5]					
180		TM36_TRGO	PB1 [7]	PC7 [6]	PD3 [10]	PE9 [5]				
181		TM36_ETR	PB0 [7]	PB13 [6]	PE15 [5]					
182		TM36_IC0	PA12 [6]	PB4 [6]	PD7 [10]	PC0 [12]	PC1 [3]			
183		TM36_IC1	PA13 [6]	PB5 [6]	PD8 [10]	PC13 [10]	PD2 [10]			
184		TM36_IC2	PA14 [6]	PB6 [6]	PD9 [10]	PC4 [5]	PD1 [10]			
185		TM36_IC3	PA15 [6]	PB7 [6]	PD10 [10]	PC5 [5]	PD0 [10]			

186		TM36_OC00	PA0 [10]	PC0 [6]	PC13 [7]					
187		TM36_OC01	PB8 [6]							
188		TM36_OC02	PB9 [6]							
189		TM36_OC0N	PC1 [6]	PC8 [7]						
190		TM36_OC10	PA1 [10]	PC2 [6]	PC14 [7]					
191		TM36_OC11	PB10 [6]							
192		TM36_OC12	PB11 [6]							
193		TM36_OC1N	PC3 [6]	PC6 [11]	PC9 [7]					
194		TM36_OC2	PA2 [10]	PC4 [6]	PD0 [6]	PD14 [5]				
195		TM36_OC2N	PA3 [10]	PD1 [6]	PC10 [7]					
196		TM36_OC3	PC5 [6]	PC12 [6]	PD15 [5]	PD7 [11]				
197		TM36_OC0H	PA8 [10]	PC8 [6]	PE1 [10]					
198		TM36_OC1H	PA9 [10]	PC9 [6]	PE2 [10]					
199		TM36_OC2H	PA10 [10]	PC10 [6]	PE13 [10]					
200		TM36_OC3H	PA11 [10]	PC11 [6]	PE14 [10]					
201		TM36_BK0	PB14 [6]	PA10 [1]	PE15 [4]					
202	RTC+DMA	RTC_OUT	PB8 [2]	PC7 [2]	PD10 [5]	PE14 [1]				
203		RTC_TS	PB9 [2]	PC6 [2]	PE15 [1]					
204		DMA_TRG0	PA8 [1]	PB11 [10]	PB12 [1]	PB14 [1]	PD15 [4]			
205		DMA_TRG1	PA9 [1]	PD11 [2]	PE1 [4]					
206	LCD	LCD_P0	PA1 [12]							
207		LCD_P1	PA2 [12]							
208		LCD_P2	PA3 [12]							
209		LCD_P3	PA4 [12]							
210		LCD_P4	PA5 [12]							
211		LCD_P5	PA6 [12]							
212		LCD_P6	PA7 [12]							
213		LCD_P7	PA8 [12]							
214		LCD_P8	PA9 [12]							
215		LCD_P9	PA10 [12]							
216		LCD_P10	PA11 [12]							
217		LCD_P11	PA12 [12]							
218		LCD_P12	PA13 [12]							
219		LCD_P13	PA14 [12]							
220		LCD_P14	PA15 [12]							
221		LCD_P15	PB0 [12]							
222		LCD_P16	PB1 [12]							
223		LCD_P17	PB2 [12]							
224		LCD_P18	PB3 [12]							
225		LCD_P19	PB4 [12]							
226		LCD_P20	PB5 [12]							
227		LCD_P21	PB6 [12]							
228		LCD_P22	PB7 [12]							
229		LCD_P23	PB10 [12]							
230		LCD_P24	PB11 [12]							
231		LCD_P25	PB12 [12]							
232		LCD_P26	PB13 [12]							
233		LCD_P27	PB14 [12]							

234		LCD_P28	PB15 [12]							
235		LCD_P29	PC1 [12]							
236		LCD_P30	PC2 [12]							
237		LCD_P31	PC3 [12]							
238		LCD_P32	PC7 [12]							
239		LCD_P33	PC8 [12]							
240		LCD_P34	PC9 [12]							
241		LCD_P35	PC10 [12]							
242		LCD_P36	PC11 [12]							
243		LCD_P37	PC12 [12]							
244		LCD_P38	PD4 [12]							
245		LCD_P39	PD5 [12]							
246		LCD_P40	PD6 [12]							
247		LCD_P41	PD8 [12]							
248		LCD_P42	PD10 [12]							
249		LCD_P43	PD11 [12]							
250	CAN	CAN0_TX	PA2 [5]	PB6 [7]	PC10 [10]	PE14 [3]				
251		CAN0_RX	PA3 [5]	PB7 [7]	PC11 [10]	PE15 [3]				
252	Other	IR_OUT	PB11 [4]	PB15 [1]	PC12 [2]	PD15 [3]				
253		MF_S0	PC2 [10]	PA12 [2]	PB12 [3]	PD2 [1]	PE12 [2]			
254		MF_S1	PC3 [10]	PA13 [2]	PB15 [3]	PD3 [1]	PE13 [2]			
255		ASB_P0	PA0 [2]	PA8 [2]	PB12 [5]	PD13 [10]				
256		ASB_P1	PA1 [2]	PA9 [2]	PB15 [5]					
257		ASB_P2	PA2 [2]	PA6 [2]	PC7 [5]					
258		ASB_P3	PA3 [2]	PA7 [2]	PD11 [10]					
259		ASB_CK0	PA4 [2]	PA2 [3]	PA9 [5]					
260		ASB_CK1	PA5 [2]	PA3 [3]						
261		OBM_I0	PA14 [2]	PD0 [1]	PE0 [1]	PE8 [2]				
262		OBM_I1	PA15 [2]	PD1 [1]	PE1 [1]	PE9 [2]				
263		OBM_P0	PB8 [10]	PC2 [3]	PD12 [3]	PE2 [1]				
264		OBM_P1	PB9 [10]	PC3 [1]	PD13 [3]	PE3 [1]				
265		CCL_P0	PA0 [7]	PB13 [10]	PC8 [10]	PD14 [10]	PE14 [9]			
266		CCL_P1	PA1 [7]	PB14 [10]	PC9 [10]	PD15 [10]	PE15 [9]			
267		SDT_I0	PA2 [6]	PC2 [7]	PC4 [7]	PC13 [9]	PE8 [4]	PA8 [5]		
268		SDT_I1	PA3 [6]	PC3 [7]	PC5 [7]	PC14 [9]	PE9 [4]	PA10 [5]		
269		SDT_P0	PA0 [6]	PB8 [9]	PC12 [9]	PD6 [9]	PC4 [10]	PC14 [10]		
270		NCO_P0	PA0 [3]	PB3 [3]	PB12 [2]	PD15 [2]	PE2 [4]			
271		NCO_CK0	PA1 [3]	PB15 [2]	PD1 [4]	PD13 [5]	PE3 [4]			

5. Memory Map

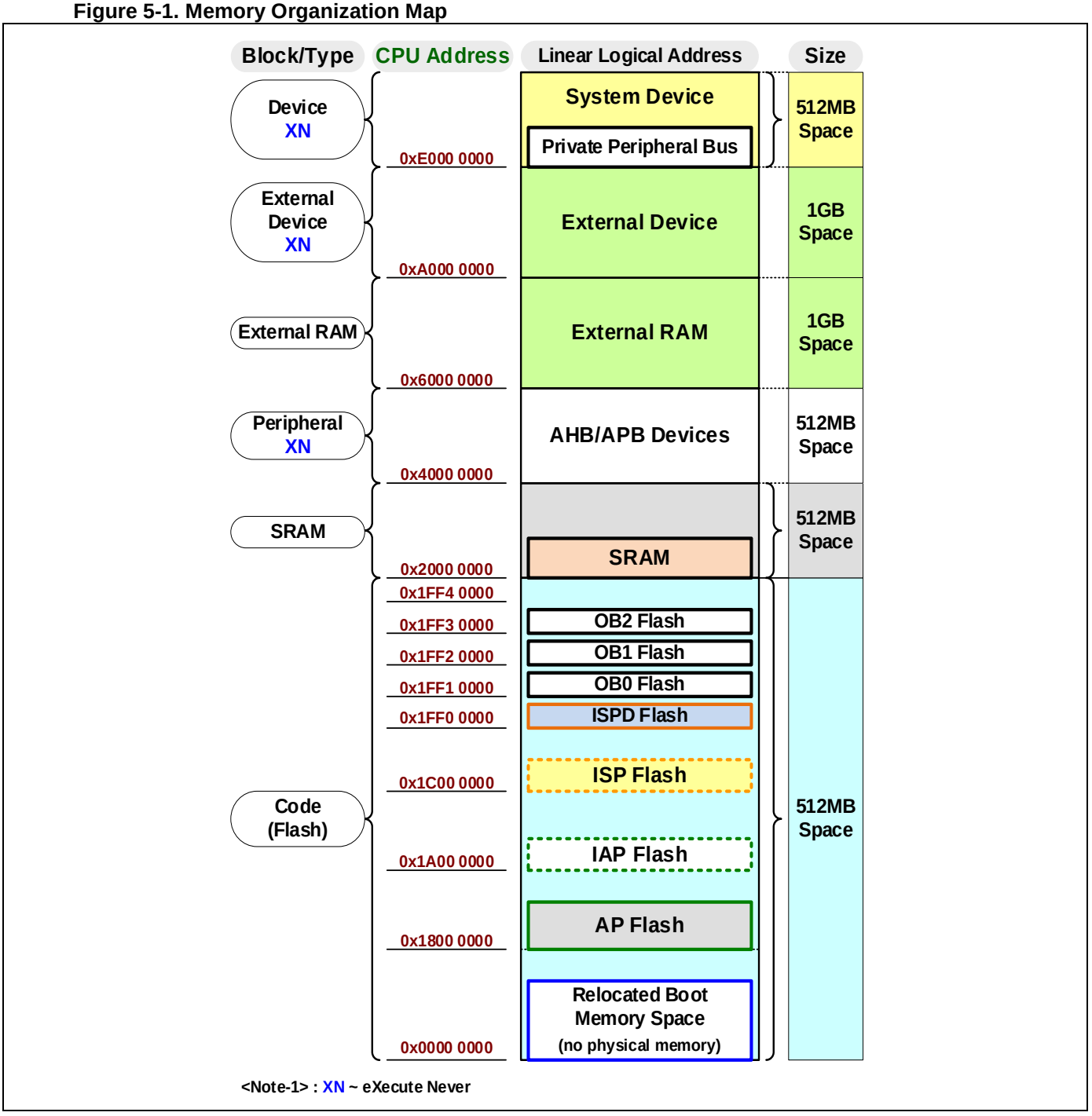
5.1. Memory Organization

There are up to ***16K*** bytes of SRAM built in the chip. The chip has up to ***128K*** bytes of embedded main flash memory for code and data, programmable memory size of embedded system flash memory for boot load code and 64 bytes of embedded option-byte (***OB***) flash memory for chip configuration. Others, there are many module independent hardware control registers and locate at the memory space of AHB/APB devices.

User can configure the whole flash to store for his Application Program (AP) code, In-System-Program (ISP) code and In-Application-Program (IAP) memory. User can adjust the size for the three flash memories.

The following diagram is showing the memory organization map. There are separated eight memory blocks and the memory size is 512M-byte for each block. The block is signed “XN” which is not able to execute code.

Figure 5-1. Memory Organization Map



5.2. CPU Memory Map

The following table is showing the memory address map of CPU. The block is signed “XN” which is not able to execute code.

Table 5-1. CPU Memory Address Map

Block Index	Block Name	XN	Boundary address		Size	Address Space	Note
			Start address	End address			
7	System Device	XN	0xE010 0000	0xFFFF FFFF	511MB	VENDOR_SYS	
			0xE000 0000	0xE00F FFFF	1MB	Private Peripheral Bus(PPB)	M0 Reserved Cortex M0 internal peripherals
6	External Device	XN	0xC000 0000	0xDFFF FFFF	512MB	Reserved	External memory (SRAM, Flash)
5	External Device	XN	0xA000 0000	0xBFFF FFFF	512MB	Reserved	External memory (SRAM, Flash)
4	External RAM		0x8000 0000	0x9FFF FFFF	512MB	Reserved	External memory (SRAM, Flash)
3	External RAM		0x6000 0000	0x7FFF FFFF	512MB	Reserved	External memory (SRAM, Flash)
2	Peripheral	XN	0x4000 0000	0x5FFF FFFF	512MB	APB/AHB	APB/AHB modules
1	SRAM		0x3000 0200	0x3FFF FFFF	256MB	Reserved	
			0x2000 4000	0x3FFF FFFF	512MB	Reserved	
			0x2000 3800	0x2000 3FFF	2KB	**SRAM (*2)**	Upper 2K-byte suggestion for DMA
			0x2000 0000	0x2000 37FF	14KB		14/8KB for flash size 128/64KB chip
0	Code		0x1FF3 0200	0x1FFF FFFF	832KB	Reserved	
			0x1FF3 0040	0x1FF3 01FF	448B	**OB Flash-2**	
			0x1FF3 0000	0x1FF3 003F	64B		Hardware Option byte-2 (64-byte)
			0x1FF2 0200	0x1FF2 FFFF	64KB	Reserved	
			0x1FF2 0050	0x1FF2 01FF	432B	**OB Flash-1**	
			0x1FF2 0040	0x1FF2 004F	16B		Unique ID (16-byte)
			0x1FF2 0000	0x1FF2 003F	64B		Hardware Option byte-1 (64-byte)
			0x1FF1 0200	0x1FF1 FFFF	64KB	Reserved	
			0x1FF1 0040	0x1FF1 01FF	448B	**OB Flash-0**	
			0x1FF1 0000	0x1FF1 003F	64B		Hardware Option byte-0 (64-byte)
			0x1FF0 0200	0x1FF0 FFFF	64KB	Reserved	
			0x1FF0 0000	0x1FF0 01FF	512B	**ISPD Flash**	ISP data flash
			0x1C02 0000	0x1FEF FFFF	63MB	Reserved	
			0x1C00 0000	0x1C01 FFFF	128KB	**ISP Flash (*2)**	Boot Flash memory (configurable size)
			0x1A02 0000	0x1BFF FFFF	32MB	Reserved	
			0x1A00 0000	0x1A01 FFFF	128KB	**IAP Flash (*2)**	Data Flash memory (configurable size)
			0x1802 0000	0x19FF FFFF	32MB	Reserved	
			0x1800 0000	0x1801 FFFF	128KB	**AP Flash (*2)**	Application Flash memory (configurable size by chip option)
			0x0002 0000	0x17FF FFFF	384MB	Reserved	
			0x0000 0000	0x0001 FFFF	128KB	Relocated memory space (*1)	Interrupt Vector 0x0000 00C0~0x0000 0000

XN: eXecute Never , 1 Block = 512MB

*1: Relocated memory space : Main flash memory, Boot flash memory or SRAM depending on BOOT configuration

*2: The table lists the maximum value. Refer the chip “Chip Selection Table” about actual memory size.

5.3. Peripheral Memory Boundary

Table 5-2. Peripheral Memory Boundary Address

Address Type	Boundary address		Size	Sections / Groups Peripheral	Module	Note
	Start address	End address				
APB	0x5F01 0100	0x5FFF FFFF	16MB	APB	Reserved	
	0x5F01 0000	0x5F01 00FF	256B		**APX**	APB module extended control
	0x5F00 0100	0x5F00 FFFF	64KB		Reserved	
	0x5F00 0000	0x5F00 00FF	256B		**APB**	APB module global control
	0x5E00 0000	0x5EFF FFFF	16MB	Reserved	Reserved	
	0x5D04 0100	0x5DFF FFFF	16MB	WDT/RTC	Reserved	
	0x5D04 0000	0x5D04 00FF	256B		**RTC**	Real Time Clock
	0x5D01 0100	0x5D03 FFFF	192KB		Reserved	
	0x5D01 0000	0x5D01 00FF	256B		**WWDT**	Window WatchDog Timer
	0x5D00 0100	0x5D00 FFFF	64KB		Reserved	
	0x5D00 0000	0x5D00 00FF	256B		**IWDT**	Independent WatchDog Timer
	0x5C00 0100	0x5CFF FFFF	16MB	CMP/DAC	Reserved	
	0x5C00 0000	0x5C00 00FF	256B		**CMP**	Analog Comparator 0,1
	0x5B00 0100	0x5BFF FFFF	16MB	ADC	Reserved	
	0x5B00 0000	0x5B00 00FF	256B		**ADC0**	Analog-to-Digital controller
	0x5A08 0100	0x5AFF FFFF	15MB	OPA	Reserved	
	0x5A08 0000	0x5A08 00FF	256B		**OPA**	Operational amplifier
	0x5A00 0100	0x5A07 FFFF	512KB	LCD	Reserved	
	0x5A00 0000	0x5A00 00FF	256B		**LCD**	Liquid Crystal Display controller
	0x5700 0000	0x59FF FFFF	48MB	Reserved	Reserved	
	0x5686 0100	0x56FF FFFF	8MB	TM2x/3x	Reserved	
	0x5686 0000	0x5686 00FF	256B		**TM36**	32-bit Timer with 4 IC/OC/PWM
	0x5606 0100	0x5685 FFFF	8MB		Reserved	
	0x5606 0000	0x5606 00FF	256B		**TM26**	32-bit Timer with 2 IC/OC/PWM
	0x5600 0100	0x5605 FFFF	384KB		Reserved	
	0x5600 0000	0x5600 00FF	256B		**TM20**	32-bit Timer with 2 IC/OC/PWM
	0x5586 0100	0x55FF FFFF	8MB	TM0x/1x	Reserved	
	0x5586 0000	0x5586 00FF	256B		**TM16**	Basic32-bit Timer/Counter
	0x5580 0100	0x5585 FFFF	384KB		Reserved	
	0x5580 0000	0x5580 00FF	256B		**TM10**	Basic32-bit Timer/Counter
	0x5501 0000	0x5501 00FF	256B		**TM01**	Basic 16-bit Timer/Counter
	0x5500 0100	0x5500 FFFF	64KB		Reserved	
	0x5500 0000	0x5500 00FF	256B		**TM00**	Basic 16-bit Timer/Counter
	0x5408 0100	0x54FF FFFF	15MB	CAN	Reserved	
	0x5408 0000	0x5408 00FF	256B		**CAN0**	Controller Area Network
	0x5300 0100	0x5407 FFFF	16MB	SPI	Reserved	
	0x5300 0000	0x5300 00FF	256B		**SPI0**	SPI bus controller with data buffer
	0x5207 0100	0x52FF FFFF	16MB	UART	Reserved	
	0x5207 0000	0x5207 00FF	256B		**URT7**	Basic UART bus controller
	0x5206 0100	0x5206 FFFF	64KB		Reserved	
	0x5206 0000	0x5206 00FF	256B		**URT6**	Basic UART bus controller
	0x5205 0100	0x5205 FFFF	64KB		Reserved	
	0x5205 0000	0x5205 00FF	256B		**URT5**	Basic UART bus controller
	0x5204 0100	0x5204 FFFF	64KB		Reserved	
	0x5204 0000	0x5204 00FF	256B		**URT4**	Basic UART bus controller
	0x5202 0100	0x5203 FFFF	128KB		Reserved	
	0x5202 0000	0x5202 00FF	256B		**URT2**	Advance UART bus controller
	0x5201 0100	0x5201 FFFF	64KB		Reserved	
	0x5201 0000	0x5201 00FF	256B		**URT1**	Advance UART bus controller
	0x5200 0100	0x5200 FFFF	64KB		Reserved	

	0x5200 0000	0x5200 00FF	256B		**URT0**	Advance UART bus controller
	0x5101 0100	0x51FF FFFF	16MB	I2C	Reserved	
	0x5101 0000	0x5101 00FF	256B		**I2C1**	I2C bus controller
	0x5100 0100	0x5100 FFFF	64KB		Reserved	
	0x5100 0000	0x5100 00FF	256B		**I2C0**	I2C bus controller
	0x5000 0100	0x50FF FFFF	16MB	EXT Interrupt	Reserved	
	0x5000 0000	0x5000 00FF	256B		**EXIC**	External Interrupt Controller
AHB	0x4FF0 0100	0x4FFF FFFF	1MB	Chip	Reserved	
	0x4FF0 0000	0x4FF0 00FF	256B		**CFG**	Hardware option (NVR0/1/2)
	0x4F00 0100	0x4FEF FFFF	15MB		Reserved	
	0x4F00 0000	0x4F00 00FF	256B		**WRI**	Writer Interface Control
	0x4E00 0000	0x4EFF FFFF	16MB	Reserved	Reserved	
	0x4D00 0100	0x4DFF FFFF	16MB	Memory	Reserved	
	0x4D00 0000	0x4D00 00FF	256B		**MEM**	Internal Memory Controller
	0x4C03 0100	0x4CFF FFFF	16MB	System	Reserved	
	0x4C03 0000	0x4C03 00FF	256B		**SYS**	System and Chip Control
	0x4C02 0100	0x4C02 FFFF	64KB		Reserved	
	0x4C02 0000	0x4C02 00FF	256B		**PW**	Power Management Controller
	0x4C01 0100	0x4C01 FFFF	64KB		Reserved	
	0x4C01 0000	0x4C01 00FF	256B		**CSC**	Clock Source Controller
	0x4C00 0100	0x4C00 FFFF	64KB		Reserved	
	0x4C00 0000	0x4C00 00FF	256B		**RST**	Reset Source Controller
	0x4BF0 0100	0x4BFF FFFF	1MB	General Purpose	Reserved	
	0x4BF0 0000	0x4BF0 00FF	256B		**DMA**	Direct memory access
	0x4B00 0100	0x4BEF FFFF	15MB		Reserved	
	0x4B00 0000	0x4B00 00FF	256B		**GPL**	General Purpose Logic
	0x4500 0000	0x4AFF FFFF	96MB	Reserved	Reserved	Reserved for future design
	0x4404 0100	0x44FF FFFF	16MB	IO Configure	Reserved	
	0x4404 0000	0x4404 00FF	256B		**PE**	
	0x4403 0100	0x4403 FFFF	64KB		Reserved	
	0x4403 0000	0x4403 00FF	256B		**PD**	
	0x4402 0100	0x4402 FFFF	64KB		Reserved	
	0x4402 0000	0x4402 00FF	256B		**PC**	
	0x4401 0100	0x4401 FFFF	64KB		Reserved	
	0x4401 0000	0x4401 00FF	256B		**PB**	
	0x4400 0100	0x4400 FFFF	64KB		Reserved	
	0x4400 0000	0x4400 00FF	256B		**PA**	
	0x4100 0200	0x43FF FFFF	48MB	Reserved		Reserved for future design
	0x4100 0000	0x4100 01FF	512B	GPIO	**IOP**	IO Port Input/Output
	0x4000 0000	0x40FF FFFF	16MB	Reserved		Reserved for future design

5.4. Boot Modes

During chip startup, the hardware configuration option-byte (***OB***) is used to select one of the three boot options:

- **Boot from User Application Program (AP) Flash**
- **Boot from In-System-Program (ISP)**
- **Boot from embedded SRAM**

6. Functional Description

6.1. CPU Core

6.1.1. Introduction

The chip is embedded a CPU core of Cortex®™-M0 processor. The processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional DAP hardware debug functionality.

The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

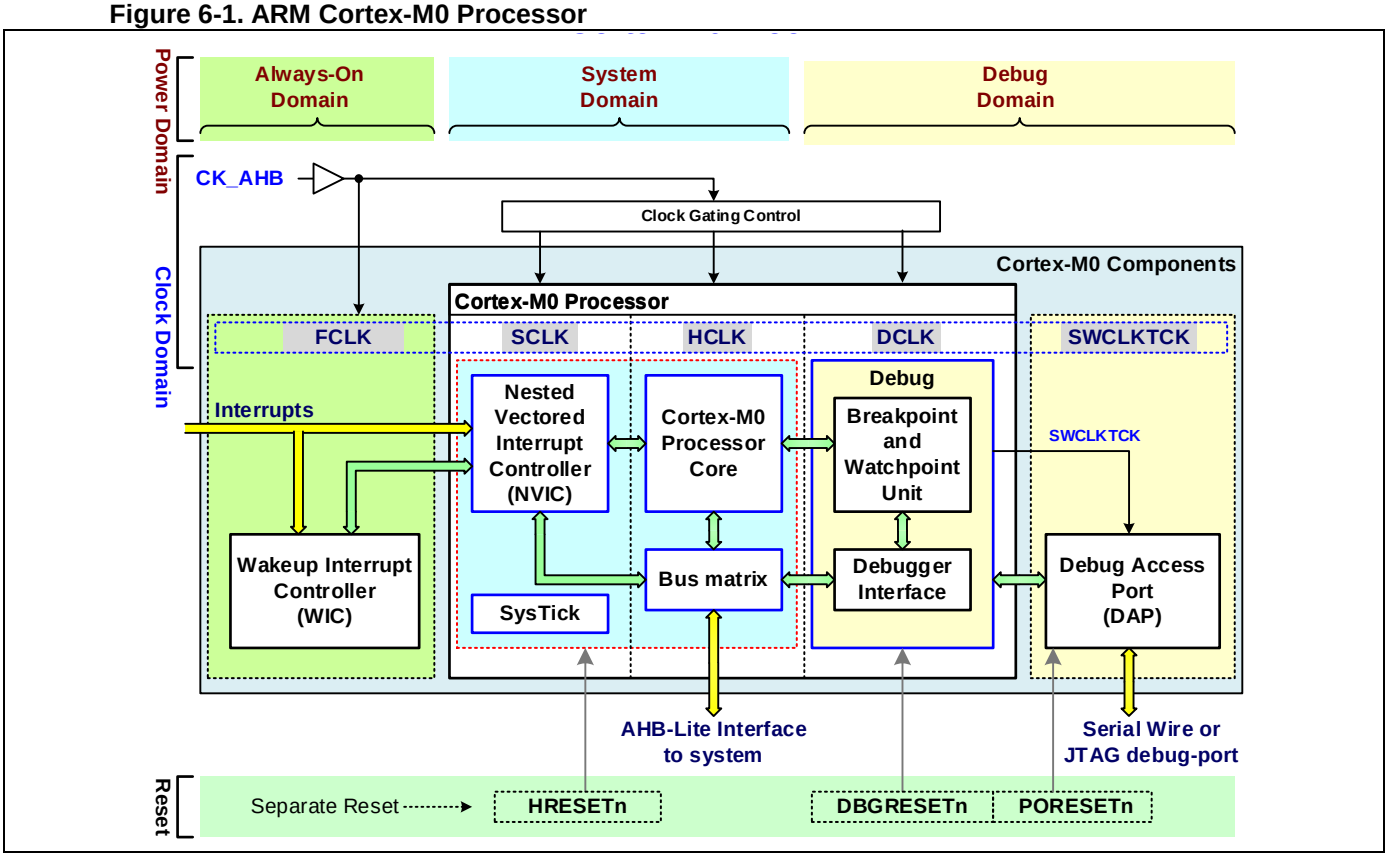
6.1.2. CPU Features

- **ARM® 32-bit Cortex®-M0 CPU**
- **Operation frequency up to 48MHz**
- **Built-in one NVIC for 32 external interrupt inputs with 4-level priority**
- **Built-in one 24-bit system tick timer**
- **Built-in one single-cycle 32-bit multiplier**
- **Built-in one SWD serial wire debugger with 2 watch points and 4 breakpoint**
- **The ARMv6-M Thumb® instruction set**

6.1.3. ARM Cortex-M0 Processor

The following diagram is showing the block of ARM® Cortex®-M0 Processor.

Figure 6-1. ARM Cortex-M0 Processor



6.2. Power Management

6.2.1. Introduction

The chip power is implemented only by single power supply input and embedded one LDO to supply the internal core logic power. The chip supports one power controller (PW) to manage Power-on reset (POR) circuit, Low-voltage reset (LVR) circuit, Brown-Out Detectors (BOD0/1/2), power down control and wakeup control.

It supports power-down modes: ***SLEEP*** mode and ***STOP*** modes. The power-down modes reduce chip power and provide the different power-saving scheme for chip application.

6.2.2. Chip Power Features

- **Built-in one embedded regulator for core logic power**
- **Built-in brown-out detectors**
  - **BOD0 detect 1.4V**
  - **BOD1 detect by selected level 4.2V/3.6V/2.4V/2.0V**
  - **BOD2 detect 1.7V**
- **Built-in a power management controller with power-down and wakeup control**
- **Support three power operation modes**
  - **ON(Normal) mode and SLEEP , STOP power down modes**
- **Support wake-up from SLEEP/STOP modes via multiple sources**
  - **Wake-up sources come from GPIO pins, IWDT, RTC, analog comparator, I2C, BODn**

6.2.3. Power Operation Mode

There are three power operation modes of ***ON***, ***SLEEP***, ***STOP*** to be supported in the power controller.

- **ON mode**

In ***ON*** mode, the CPU is able running in full speed. All peripheral modules can use full power to do normally full function operation. These modules can enable or disable independent to save current consumption.

- **SLEEP mode**

In ***SLEEP*** mode, only the CPU is stopped and entering CPU sleep mode. All peripheral modules can be configurable to continue to operate or sleep.

In this mode, the chip can be waked up by the related interrupt or event occurs.

- **STOP mode**

The ***STOP*** mode provides the lowest current consumption. The different from SLEEP mode is that CPU is entering CPU deep-sleep mode and all peripheral modules are disabled except some special modules or devices. These modules or devices can be configurable to continue to operate in STOP mode or not. They include of IWDT, RTC, CMP modules and LVR, BOD0, BOD1, BOD2 devices. The internal voltage regulator is also running in low power mode.

In this mode, the chip can be waked up by some of the external input lines (GPIO) and some events detection.

6.2.4. Power Supply

The chip power is implemented only by single power supply input for easy application PCB design. It is embedded one internal low dropout linear regulator (LDO) to generate the +1.5 volt voltage power VDDC for core logic power supply.

The **VDD** pin(s) is/are using for IO power supply input and internal LDO input. The **VSS** pin(s) is/are used to connect the external ground for internal reference ground of internal LDO, hard macros and digital logic. The **VCAP** pin is the LDO output and it needs to connect bypass capacitors for normal operation. The **+VREFF** pin is the input of ADC reference voltage which can connect to **VDD** pin for general application.

6.2.5. CPU Power Down

For chip entering power down mode, the firmware must execute WFI or WFE instruction to force the CPU enters sleep mode or deep sleep mode. Then the chip will enter the power down mode of ***SLEEP*** or ***STOP***. User can configure the CPU sleep mode by setting CPU register of SLEEPDEEP after firmware executes WFI or WFE instruction.

Table 6-1. Power-Down Mode Selection

CPU	System	CPU Register
		SLEEPDEEP
Run	ON	x
sleep	SLEEP	0
deep sleep	STOP	1

6.3. System Reset

6.3.1. Introduction

During reset, all Registers are set to their initial values, and the program starts execution from the Reset Vector. The chip includes a reset source controller (RST) to manage multiple sources of reset and generates Warm reset and Cold reset signals to chip system and internal modules. This controller also provides the reset event flags for firmware, which are used to recognize the reset occurred source.

6.3.2. Chip Reset Features

- **Built-in embedded POR(power-on reset)/LVR(low-voltage reset) circuit**
- **Built-in one reset source controller**
  - **Programmable chip cold reset and warm reset for reset source**
  - **Independent software reset control for internal modules**
- **Provide multiple reset sources**
  - **POR/LVR/BOD/External reset pin input/Software force reset**
  - **IWDT/WWDT/ADC/Comparator**
  - **IAR(Illegal address error reset)/Flash access protect error reset**
  - **Missing clock detect (MCD) reset**

6.3.3. Chip Reset Levels

The chip provides three reset levels – POR reset, Cold reset and Warm reset. POR reset is the highest priority reset and is generated by chip hardware. Cold reset is the 2nd priority and Warm reset is the lowest priority reset.

When POR reset occurred, it will cause to generate Cold reset to chip. Also when Cold reset occurred, it will cause to generate Warm reset to chip.

- **Power-On Reset**

Power-on reset (***POR***) is used to internally reset the chip and also the CPU during power-up. The chip will keep in reset state and will not start to work until the VDD power rises above the voltage of Power-On Reset. And, the reset state is activated again whenever the VDD power falls below the POR threshold voltage. During a power off cycle, VDD must fall below the POR threshold voltage before power is reapplied in order to ensure a power-on reset.

- **Cold Reset**

Cold reset is the 2nd priority reset. The Cold reset is also generated and caused by POR reset occurred. It sends to some modules like as IWDT, WWDT … to do deep level module reset. It will cause to reload all hardware configurations ***OB*** and disable the register lock function for the modules which are support the register lock function.

- **Warm Reset**

Warm reset is the lowest priority reset. The Warm reset is also generated and caused by Cold reset occurred. It sends to all modules to clear flags and hardware circuit. It will cause to reload some hardware configuration ***OB*** and reset the registers of module to default value if the module is unlocked or not supported lock function. It will clear Warm reset source enable bits in RST controller if the RST controller is unlocked.

6.3.4. External Reset

The chip provides an external hardware reset input from **RSTN** pin, which is accomplished by holding low level for the **RSTN** pin. The **RSTN** pin is configured to as external reset pin or others (GPIO …) by hardware configuration ***OB***. To ensure a reliable power-up reset, then the hardware reset from **RSTN** pin is necessary.

6.3.5. Module Reset

For each AHB or APB control module, it can receive the system Warm reset signal to reset the module's control flags, registers and logical circuit. For some modules of IWDT, WWDT, RTC, PW, CSC and MEM, they can receive the Cold reset to unlock the register locked function and reset the module.

6.4. System Clock

6.4.1. Introduction

The chip builds in a clock source controller (CSC) for system clock source management. There are four clock sources for the system application: Internal High-frequency RC Oscillator (***IHRCO***), Internal crystal oscillator (***XOSC***), Internal Low-frequency RC Oscillator (***ILRCO***) and External Clock Input (***EXTCK***). The built-in ***IHRCO*** provides two kinds of frequency for software selected. One is 12MHz and another frequency is 11.059MHz.

One ***XOSC*** oscillator is embedded for external crystal circuit with **XIN** and **XOUT** pins. One PLL is embedded to multiply the frequency of clock source and output clock for CPU and other peripheral modules. One missing clock detector (***MCD***) is built-in to monitor the clock of external Xtal or external clock source.

6.4.2. Chip Clock Features

- **Built-in embedded ILRCO (internal low frequency RC oscillator) by 32KHz**
- **Built-in embedded IHRCO (internal high frequency RC oscillator)**
  - **Trimmed to 11.059 or 12MHz ±1% at +25℃**
- **Built-in embedded PLL clock output for system clock**
- **Built-in embedded XOSC oscillator with MCD for external 32KHz and 4 to 25MHz crystal**
- **Support external clock input up to 36MHz**
- **Built-in a clock source controller with clock enable control for modules**
- **Support internal XOSC oscillator and internal ILRCO/IHRCO clock output**

6.4.3. System Clock Source

There are four clock sources for the system application: Internal High-frequency RC Oscillator (***IHRCO***), Internal crystal oscillator (***XOSC***), Internal Low-frequency RC Oscillator (***ILRCO***) and External Clock Input (***EXTCK***). Software can select the one of the four clock sources by application required and switches them on the fly. But software needs to settle the clock source stably before clock switching.

6.4.4. PLL Clock

One PLL is embedded to multiply the frequency of system clock source from ***IHRCO***, ***ILRCO***, ***XOSC*** and ***EXTCK***. The PLL multiplication value can be from 4 to 32. The PLL input frequency range is about 4~8 MHz and PLL VCO output frequency is up to over 150MHz. Usually, the PLL output frequency should be divided to do as CPU or others clock source. Refer the Electrical Characteristics chapter for detail specification about PLL.

6.4.5. Module Process Clock Control

The CSC module is able to do the process clock enable setting and select the process clock source for internal modules. User must select the module process clock and enable the module process clock before configure the module for operation normal.

6.5. System Common Control

6.5.1. Introduction

The chip embeds one system control (SYS) module for system common control. It is including of one system event interrupt global enable control, chip manufacture identification code.

6.5.2. Features

- **System interrupt global enable control for system interrupt source**
- **Chip manufacture identification code - Device ID, Product ID, User ID, Module Options**

6.6. Memory Access

6.6.1. Introduction

The chip has separate address spaces for program and data memory. The logical separation of program and data memory allows the memory to be accessed by 32bit addresses, which can be quickly stored and manipulated by the CPU. The chip supports one memory controller (MEM) to manage the internal flash memory and SRAM access operation.

6.6.2. Features

❖ **Embedded Memory**

- **Built-in embedded max. 128K bytes flash memory for application code**
  - **Optional 64K/128K bytes flash memory by different product**
- **Built-in embedded max. 16K bytes SRAM**
  - **Support private 2K bytes for DMA to improve CPU access performance**

❖ **Memory Controller Features**

- **Support ICP (In-circuit program) for ISP boot code update through SWD interface**
- **Support ISP (In-system program) for application code update**
  - **Support programmable ISP flash memory size for ISP boot code**
  - **Provide fixed 512 bytes ISPD flash memory as ISP private data**
- **Support IAP (In-application program) for application data update**
  - **Support programmable IAP flash memory size**
- **Support flash memory page erase in 512 bytes**

6.6.3. Memory Controller

A memory controller is supported to access on chip flash memory, SRAM on AHB bus. It includes ***ICP*** (In-Circuit Programming)/ ***ISP*** (In-System Programming)/ ***IAP*** (In-Application Programming) circuits for flash memory accessing, option byte loader for hardware option registers loading and an external memory bus EMB interface with the capability of accessing external program memory.

The chip has up to **128K** bytes of embedded main flash memory for code and data, programmable memory size of embedded system flash memory for boot load code and 64 bytes of embedded option-byte flash memory for chip configuration.

The memory controller (MEM) supports to Read/ Program (Write)/ Erase the flash memory. User can directly read the data from flash memory by CPU read instruction commands and do not need through any register. For “Program” mode, MEM provides the 32-bit data write operation into flash memory for new data updated. For “Erase” mode, the Erase address is only valid at low 9-bit CPU address=0 (X...XX0 0000 0000B) and is addressing 512-byte alignment. If the low 9-bit address of erased start address is not all ‘0’, this erased process is no effect.

6.6.4. ICP/ISP/IAP for Flash Memory

There are 3 flash access modes are provided in chip for ICP, ISP and IAP application: program mode and read mode. ICP is allowed to update the entire contents of the flash memory by using the hardware SWD interface and no any firmware request. Others, User can use these two modes of ISP and IAP to update new data into flash storage and get flash content by a firmware flash memory access handler.

6.6.5. Hardware Option Byte Flash Memory

There can be up to **64** bytes of on-chip Option Bytes Flash memory. It is used to store the hardware option configuration setting.

The embedded option-byte (***OB***) flash memory will load into the hardware configuration option-byte register (***OR***) after power-on reset. The hardware configuration ***OR*** are designed to configure the clock source from

internal RC oscillator or crystal oscillator; the booted memory selection from AP, ISP flash memory or SRAM; the memory size of IAP flash memory; other chip configurations … etc.

6.7. GPIO

6.7.1. Introduction

The chip has following I/O ports: **PA[15:0]**, **PB[15:0]**, **PC[14:0]**, **PD[15:0]** and **PE[3:0][9:8][15:12]** . Support maximum 73 GPIO pins for LQFP80 package. **RSTN** pin is an alternated function pin on **PC6**. If select external crystal oscillator as system clock input, **PC13** and **PC14** are configured to **XIN** and **XOUT**. The exact number of I/O pins available depends upon the package types.

The chip has built in several IO mode control **(PA/PB/PC/PD/PE)** modules for each GPIO port. These modules are used for GPIO pin IO mode control, alternated function selection, driver strength setting, input inverse selection, pull-high enable, deglitch filter setting and high speed enable. Also one IO Port access control **(IOP)** module is built-in to control the input and output state of GPIO mode for all GPIO ports.

6.7.2. Features

- **Support general purpose IO pins for application**
  - **Maximum 73 GPIO pins for LQFP80 package**
  - **Maximum 59 GPIO pins for LQFP64 package**
  - **Maximum 44 GPIO pins for LQFP48 package**
- **Provide selectable IO modes by pin independent**
  - **Push-Pull output**
  - **Quasi bidirectional**
  - **Open-drain output**
  - **Input only with high impedance**
  - **Analog IO**
- **Flexible pin alternate function selection**
- **Support programmable drive strength by pin independent**
- **Support IO deglitch filter by pin independent**
- **Support input inverse selection by pin independent**
- **Support pull-high option by pin independent**
- **Support high speed option by pin independent except RSTN,XIN**
- **GPIO pin state and IO mode setting keep optional after reset**

6.7.3. GPIO Control Block

The GPIO Control block includes IOM (IO pad Mode control), IOP (IO Port access control) and AFS (Alternate Function Select) blocks.

- **IO Operation Mode**

The IO operating modes are supported analog IO, digital input, push-pull output, and open-drain output, quasi-bidirectional. Provide selectable IO modes by pin independent.

The IO mode control block supports programmable IO operation modes, output high speed option, pull-high option, output drive strength, IO deglitch filter and input inverse selection by pin independent.

- **IO Port Access**

When the AFS setting is set GPIO function mode for any IO pin, user can directly set the logical output or get the logical input for the IO pin. There is one independent data out register bit to store the output logic value for each GPIO pin. Also user can directly read the input data register bit to get the GPIO pin logical state for each GPIO pin.

For firmware control, there are one set control bit to set the data out register bit and one clear control bit to clear the data out register bit for each GPIO pin.

The chip provides one set-or-clear register control bit to set, clear the data out register bit or read pin status for each GPIO pin. The register bit is written 1 to set data bit and written 0 to clear data. Read the register bit to get the GPIO pin status. As this register bit is cost eight bit memory space, firmware is easy to control single GPIO pin by CPU byte-access instruction command. It is like the bit access IO control of 8051 MCU.

- **Alternate Function Select Control**

User can configure the alternate function between module function IO and IO pins through the AFS matrix for each GPIO pin independently. Usually the AFS default setting is GPIO function for each GPIO pin except the **XIN/XOUT**, **SWCLK/SWDIO** and **RSTN** function pins. These pins may be changed by hardware configuration ***OB***.

6.8. Interrupt

6.8.1. Introduction

After reset, the CPU begins execution from the location of reset interrupt vector (0x00000004) addressing, where should be the starting of the user's application code. To service the interrupts, the interrupt service locations (called interrupt vectors) should be located in the address 0x000000BF~0x00000000.

The chip is built-in Arm® cortex M0 CPU and is embedded a NVIC (Nested Vectored Interrupt Controller) for 32 external interrupt inputs with 4-level priority. Also builds in an EXIC (External Interrupt Controller) module and connects to NVIC.

6.8.2. Interrupt Features

- **Built-in one NVIC for 32 external interrupt inputs with 4-level priority**
- **Built-in one EXIC (external interrupt controller) for NVIC connection**
  - **Independent high/low level and rising/falling edge trigger selection**
- **Built-in one WIC (wakeup interrupt controller) for wakeup event control**
- **All GPIO pins can be configured as interrupt source and key pad input**
  - **Support port OR logic for interrupt function**
  - **Support port AND logic for KBI function**
- **Support external pins for CPU NMI/RXEV/TXEV function**
  - **Configurable pin for CPU NMI input function**
  - **Configurable pin for CPU RXEV input function**
  - **Configurable pin for CPU TXEV output function**

6.8.3. Interrupt Structure

Each interrupt is assigned a fixed location in the program memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. NMI interrupt, for example, is assigned to location 0x00000008. If NMI is going to be used, its service routine must begin at location 0x00000008.

The interrupt service locations are spaced at an interval of 4 bytes: 0x00000004 for Reset Interrupt, 0x00000008 for ***NMI***, 0x0000000C for ***Hard-Fault***, 0x0000002C for ***SVCall***, 0x00000038 for ***PendSV***, 0x0000003C for ***SysTick***, etc.

- **Exception types**

The NVIC has 7 exception types: ***Reset***, ***NMI***, ***HardFault***, ***SVCall***, ***PendSV***, ***SysTick*** and Interrupt (IRQ). The NVIC supports 32 external interrupt input. An interrupt is an exception signaled by a peripheral or generated by a software request. The four priority level interrupt structure allows great flexibility in handling these interrupt sources.

- **Interrupt Sources**

The 'Pending Bits' are the interrupt flags that will generate an interrupt if it is enabled by setting the 'Set Enable Bit'. The 'Pending Bits' can be set or cleared by software, with the same result as though it had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled in software. The 'Priority Bits' determine the priority level for each interrupt. The 'Priority within Level' is the polling sequence used to resolve simultaneous requests of the same priority level. The 'Vector Address' is the entry point of an interrupt service routine in the program memory.

Table 6-2. Interrupt Source Table

NVIC						Comment
Exception No.	IRQ No.	Interrupt Name	Priority	Activation	Exception handlers	
0	-	Initial	-			
1	-	Reset	-3	Asynchronous		Reset exception
2	-14	NMI	-2	Asynchronous	System handlers	Non Maskable Interrupt
3	-13	HardFault	-1	Synchronous	Fault handler	Cortex-M0 Hard Fault Interrupt
4~10	-	Reserved	-			
11	-5	SVC	Configurable	Synchronous	System handlers	Cortex-M0 SV Call Interrupt
12~13	-	Reserved	-			
14	-2	PendSV	Configurable	Asynchronous	System handlers	Cortex-M0 Pend SV Interrupt
15	-1	SysTick	Configurable	Asynchronous	System handlers	Cortex-M0 System Tick Interrupt
16~47	0~31	-	Configurable	Asynchronous	ISRs	Peripheral Interrupts
Configurable : Programmable priority level 0~3						

- **Interrupt Priority**

The priority scheme for servicing the interrupts has four interrupt levels. The priority bits in CPU registers, IPR0-7, SHPR2 and SHPR3, determine the priority level of each interrupt.

The interrupt priority registers provide an 8-bit priority field for each interrupt and each register holds four priority fields. The processor implements only bits [7:6] of each field, bits [5:0] read as zero and ignore writes.

Higher-priority interrupt will be not interrupted by lower-priority interrupt request. If two interrupt requests of different priority levels are received simultaneously, the request of higher priority is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determine which request is serviced. The table of “interrupt sources” shows the internal polling sequence in the same priority level and the interrupt vector address. The lower exception number gets the higher priority.

6.8.4. Nested Vectored Interrupt Controller

The Cortex®-M0 processor integrates a configurable Nested Vectored Interrupt Controller (NVIC) that supports low latency interrupt processing and includes a non-mask interrupt (***NMI***). The NVIC provides a zero-jitter interrupt option and four interrupt priority levels.

Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with sleep mode. Optionally, sleep mode support can include a deep sleep function that enables the entire device to be rapidly powered down.

6.8.5. Wakeup Interrupt Controller

The chip includes a Wakeup Interrupt Controller (WIC) which can detect an interrupt or wakeup event from EXIC and wake the processor from deep sleep mode. The WIC is enabled only when the DEEPSLEEP bit in the CPU register of SCR is set to 1. The WIC is not programmable, and does not have any registers or user interface. It operates entirely from hardware signals.

6.8.6. External Interrupt Controller

The External Interrupt Controller (EXIC) includes four external port interrupt blocks (EXINT) to manage the external pin input interrupt events, one wakeup control block for wakeup event control and control the NMI/RXEV events. The EXIC also do as the interface controller between internal modules and NVIC for the interrupt and wakeup events management.

6.9. General Purpose Logic

6.9.1. Introduction

The chip builds in one general purpose logic (GPL) module. It provides the combined functions of Data Order Change, Parity Check, Data Inverse and CRC.

6.9.2. Features

- **Support data inverse, bit order change, byte order change and parity check**
  - **Data bit order change for 8/16/32-bit reverse**
  - **Data byte order change between Little endian and Big endian for 16/32-bit range**
  - **Parity Check for 8/16/32 bit range**
- **Support CRC (Cyclic Redundancy Check) calculation**
  - **Programmable CRC initial value**
  - **CRC output bit order change**
- **CRC with fixed common polynomial**
  - **CRC8 polynomial 0x07**
  - **CRC16 polynomial 0x8005**
  - **CCITT16 polynomial 0x1021**
  - **CRC32(IEEE 802.3) polynomial 0x4C11DB7**
- **Input data are buffered with DMA capability**

6.9.3. GPL Control Block

- **Byte Order Change**

The GPL can change the byte order of input data for big or little endian format for 32-bit range or 16-bit range.

- **Bit Order Change**

The GPL can change the bit order of input data for 8/16/32-bit reversion. This process is able to select data size of 8-bit, 16-bit and 32-bit.

- **Data Invert**

The GPL can invert the data value from input data.

- **Parity Check**

The GPL can set the parity check polarity by odd or even and calculate parity.

- **CRC Calculation**

The CRC (cyclic redundancy check) block is used to get an 8/16/32-bit CRC data code and calculates the result. The CRC block can process continuously with sequent CRC code and store the last result into data buffer always.

- **Hardware Arithmetic Divider**

The GPL module is including a 32-bit hardware arithmetic divider. The arithmetic divider is general using for firmware development. The hardware divider is supported both unsigned and signed arithmetic calculation by register setting.

6.10. Direct Memory Access

6.10.1. Introduction

The chip is built-in a direct memory access controller (DMA) which is used to improve the performance of data transfer between peripheral and memory, memory to memory and peripheral to peripheral. Data can be quickly transfer by through DMA without costing any CPU resources.

Notify: The sign of (n= DMA channel index number) is using for Registers, Signals and Pins/Ports in the descriptions of this chapter.

6.10.2. Features

- **5 independently configurable channels with dedicated hardware DMA requests**
  - **Access to Memory, APB and AHB Peripherals as source and destination**

  - **Support SRAM/Flash as memory source and SRAM as memory destination**
  - **Peripheral is including of ADC0, I2Cx, URTx, SPIx, TM36, APX(ASB) and GPL modules**
- **DMA transfer management type**
  - **memory-to-memory (channel 0,3 only)**
  - **peripheral-to-memory**
  - **memory-to-peripheral**
  - **peripheral-to-peripheral**
- **Built-in two type priority control between channel requests**
  - **Channel request by Round Robin**
  - **Software configurable priority level**
- **Programmable transfer number of data and up to 131072**
- **Programmable burst length 1,2,4**
- **Support transfer loop mode and start address auto reload control**
- **Provide single/block/demand mode for external pin trigger request**

6.10.3. DMA Control

The DMA controller (DMA) is used to transfer data between these sources and destinations of AHB peripheral, APB peripheral, SRAM and external memory. Two external pins of **DMA_TRG0** and **DMA_TRG1** are able to input as the trigger signal of DMA data transfer.

Each DMA channel is able to process the transfer types of peripheral-to-memory, memory-to-peripheral and peripheral-to-peripheral. The transfer type of memory-to-memory is only support for channel-0 and channel-3. The transferred memory sources can be embedded SRAM or Flash.

6.11. APB Common Control

6.11.1. Introduction

The chip builds in one APB (APB bus common control) module for the common control of APB devices.

6.11.2. Features

- **Timer synchronous enable global control**
- **OBM(Output Signal Break and Modulation) control**
  - **Support two sets of OBM for output signal break and modulation control**
- **NCO(Numerically Controlled Oscillator) output with FDC and PF modes**
- **Infrared Remote Modulation Output**

6.11.3. APB Control Block

- **Timer Common Control**

The TMx modules supports two timer enable control bits of **TMx_EN** and **TMx_EN2** to enable the Main timer and 2nd timer separately for each TMx module.

In APB module, there are the same control bits of **APB_TMx_EN** and **APB_TMx_EN2** as the timer enable bits of **TMx_EN** and **TMx_EN2**. These control register bits are built in one 32-bit register and can be enabled or disabled synchronously by setting **APB_TMx_EN** or **APB_TMx_EN2** registers for firmware easy control. (x = Timer module index).

The ITR6 and the ITR7 are used as the common signals of trigger event or clock signal for all timer modules. User can select the trigger source signal by register setting. The **APB_ITR6** and **APB_ITR7** signals can be selected from others TMx timer, URTx, ADC0, RTC modules and EXIC global interrupt events.

- **OBM Control**

The APB module is including of two identical sets of output signal break and modulation (OBM) block. The OBM block is used to break one of the output signals or do signal modulation.

- **IR Control**

The APB module is including of one IR (Infrared Remote) modulation block. This block is used to do signal modulation for the transmission of IR control.

- **NCO Control**

The APB module is including of one Numerically Controlled Oscillator (NCO) block. The NCO block is used to generate a divided frequency with a decimal clock signal from input clock signal. It is useful for the accurate frequency clock requested application.

The NCO block supports two output modes, one is fixed duty cycle mode (FDC) and another is pulse frequency mode (PFM). The NCO output signal can be outputted to external pin or internal other modules. It can send to UART modules to do as clock source input. Also it can output to do as the common trigger event or clock signal ITR7 for Timer modules. There are one output pin **NCO_P0** to output the NCO output signal and this output signal can be inverted by setting register for application request.

6.12. APX

6.12.1. Introduction

The chip builds in one APX module for the extended function control of APB devices.

6.12.2. Features

- **Support two sets of CCL(Configurable Custom Logic)**
- **SDT(State Detector) for two-line sequential state detection**
- **ASB(ARGB Serial Bus) with 4 channels for addressable RGB LED application**

6.12.3. APX Control Block

- **CCL Control**

The APX module is including of two sets of Configurable Custom Logic (CCL) block. Each CCL block can be connected to the device pins or other internal peripherals' signal. The CCL can eliminate external extra logic gate devices for simple glue logic functions on user application. It supports the L-to-H signal detected event flag and the interrupt.

- **SDT Control**

The APX module is including of one Sequential State Detector (SDT) block for two-line sequential state detection. The SDT can be connected to the device pins and detect the sequential stats for special procedures. It supports the related detected event flag and the interrupt for different procedure. The SDT block is including of six state procedure control logic, state compare logic, output event control logic and IO pin output mode control logic.

- **ASB Control**

The APX module is including of one ARGB Serial Bus (ASB) block for ARGB (addressable RGB) LED display application. The ASB block can support to connect and control maximum four channels of ARGB LED chain. It also supports the related data transmission control flags and the interrupts for independent channel control. Each channel can use one IO pin to control multiple ARGB LEDs to simplify the circuit design and PCB layout.

The ASB block is implemented both asynchronous ARGB mode and synchronous Shift mode with DMA capability for RGB LED application. It is designed the programmable ARGB data code-0/1 high time and RESET code time control for flexible ARGB timing. It also can set the code level of ARGB RESET code, IDLE code and SYNC code by firmware register control.

6.13. I2C

6.13.1. Introduction

The I2C interface is a two-wire, bi-directional serial bus. It is ideally suited for typical microcontroller applications. The I2C protocol allows the systems designer to interconnect up to 128 different devices using only two bi-directional bus lines, one for clock (SCL) and one for data (SDA). The I2C bus provides control of SDA, SCL generation and synchronization, arbitration logic, and START/STOP control and generation. The only external hardware needed to implement this bus is a single pull-up resistor for each of the I2C bus lines. All devices connected to the bus have individual addresses, and mechanisms for resolving bus contention are inherent in the I2C protocol.

The I2C module builds in the shadow buffer and data register to improve transmit and receive communication performance.

6.13.2. Features

- **Provide two identical I2c modules : I2C0 , I2C1**
- **Support master and slave mode**
- **Support programmable clock rate control and clock rate up to 1 MHz**
- **Support programmable high/low period control for master mode**
- **Support clock stretching for slave mode**
- **Support general call function**
- **Support multi-master processing capability**
- **Support both Byte mode and Buffer mode flow control**
- **Support Byte mode bus event code for simplex firmware control**
- **Support Buffer mode 4-byte data buffer and 32-bit data register for high speed communication**
- **Received and transmitted data are buffered with DMA capability**
- **Support slave address hardware detection wakeup from STOP mode**
- **Support SMBus timeout detection**

6.13.3. I2C Control

- **I2C Data Byte Mode Control**

  The module is provides one bus event register to get the I2C Event Code for software byte-mode simplex control. An 8-bit shift buffer and an 8-bit data register are using for the I2C data Byte mode.

- **I2C Data Buffer Mode Control**

  The module implements an 8-bit shift buffer, a 32-bit shadow buffer and a 32-bit data register for data flow control of data Buffer mode.

- **I2C Master Timing Control**

  Two timing control registers are simply used to configure the I2C timing of high and low cycle time.

- **I2C Timeout Timer Control**

  The module is provides one 8-bit timeout timer (TMO) for I2C access time-out control.

6.14. UART

6.14.1. Introduction

There are two types of UART module, one is advanced UART modules and another is basic UART modules. The advanced UART modules are including of URT0 ~ URT2. The basic UART modules are including of URT4 ~ URT7 those are only support standard asynchronous communication mode through RX and TX two pins.

The advanced UART module support full-duplex transmission, meaning it can transmit and receive simultaneously. The module builds in the shadow buffer and data register by transmit and receive independently to improve transmit and receive communication performance. It can commence reception of a second byte before a previously received byte has been read from the register. However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.

The advanced UART module can operate in multiple modes: asynchronous communication, synchronous communication, SPI master, ***SmartCard***, ***LIN***, multi-processor mode. The asynchronous communication operates as a full-duplex Universal Asynchronous Receiver and Transmitter (UART), which can transmit and receive simultaneously and at different baud rates.

6.14.2. Features

- **Provide seven UART modules : URT0~2, URT4~7**
- **UART module common functions**
  - **Provide precise UART baud-rate control by programmable oversampling rate**
  - **Support baud rate up to 6 Mbit/s**
  - **Programmable data word length - 7 or 8 bits**

- Hardware parity checking and parity generation
- Programmable 4~32 oversampling rate
- Swappable TX/RX pin configuration
- Separate signal polarity control for transmission and reception

- Provide URT0/1/2 advanced UART module
  - Support UART, Synchronous, SPI master/slave, SmartCard, LIN, Multi-processor modes
  - Selectable MSB or LSB first data order
  - Configurable stop bits - 0.5,1,1.5 or 2 stop bits
  - Support a timeout timer for Idle/RX/Break/Calibration timeout detection
  - Support 4-byte data buffer and 32-bit data register for high speed communication
  - Support auto baud-rate detection and calibration
  - Support multiprocessor communication for master and slave mode - Idle-Line , Address-Bit
  - Support low speed UART-like frame format IrDA
  - Support transceiver hardware flow control by CTS/RTS signals only
  - Provide driver enable signal to activate the transmission for bidirectional communication
  - Support transmission-error hardware detection and auto resent control for Smart-card application
  - Support receiving parity error hardware detection and auto retry control for Smart-card application
  - Received and transmitted data are buffered with DMA capability
- Provide URT4/5/6/7 basic UART modules
  - Support TX/RX independent 8-bit data register for simplex firmware control
  - Configurable stop bits - 1 or 2 stop bits

6.14.3. Module Functions

The following table is showing the implemented functions of UART modules.

Table 6-3. UART Module Function Table

Module Functions	URT0/1/2	URT4/5/6/7	Comment
UART - asynchronous	yes	yes	
Synchronous - SPI Master mode	yes		Synchronous - Master 2 data lines
Synchronous - SPI Slave mode	yes		Synchronous - Slave 2 data lines
SmartCard - ISO7816-3	yes		
LIN	yes		
Multiprocessor - Address Bit	yes		
Multiprocessor - Idle Line	yes		
IrDA - UART Like	yes		low speed UART-like frame format IrDA (SIR Normal Mode)
Hardware flow control	yes		only support CTS/RTS
External Clock pin	1		
Timer BRO,TMO pins	2		
Shadow Buffer	4-byte		
Data 7-bit option	yes	yes	
TX parity bit generation	yes	yes	hardware auto generate the parity bit from the data byte
Msb/Lsb transfer option	yes		
Configurable stop bits	0.5, 1, 1.5, 2	1, 2	programmable Stop bit length
Auto Baud-Rate calibration	yes		auto Baud-Rate detection and calibration
Mute mode auto enter/exit	yes		enter mute mode if address match does not occur
Break condition detect	yes		
Idle line detect	yes		
Programmable over sampling number	4~32	4~32	
Programmable clock phase/polarity	yes		for synchronous mode

General timer control	**yes**	**yes**	baud-rate timer and timeout timer as general timer
Drive enable	**yes**		Drive enable signal of the transmission mode for the external transceiver.
RX parity error detect	**yes**	**yes**	checks parity of received data byte
Frame error detect	**yes**	**yes**	
Data overrun detect	**yes**	**yes**	receive buffer over threshold level; transmit buffer empty
TX error detect	**yes**		SmartCard/LIN
Noise character detect	**yes**		skip or not for noise character
Idle timeout detect	**yes**		for SmartCard application
RX timeout detect	**yes**		aging character detection
Break timeout detect	**yes**		for LIN application
Calibration timeout detect	**yes**		for LIN application
DMA request capability	**yes**		

6.14.4. UART Control

The UART module is able to configure the control mode from one of UART (asynchronous mode), SYNC (synchronous mode), IDLE (multi-processor idle mode) and ADR (multi-processor address-bit mode).

The UART module implements two operation modes of Idle-Line mode or Address-Bit mode for multi-processor communication.

- **UART Data Buffer**

The UART module implements two 8-bit shift buffers, two 32-bit shadow buffer and two 32-bit data register for data flow control and reduce the CPU overhead.

- **UART Data Character Format Setting**

The UART character is defined as the data unit for UART transaction. Generally, the character is including of one Start bit, 8-bit or 7-bit data bits and one Stop bit. Others, it also can insert one parity bit (PAR) and one address bit (ADR) for multi-processor mode.

- **UART TMO Timeout Control**

The module is provides one 16-bit timeout timer (TMO) for UART access time-out control. It can configure as an UART timeout timer or a general using timer by register. When the TMO timer is configured as a general using timer, there is one reload register for the timer.

The TMO timer can use to detect Idle Line condition, Break Timeout, RX Timeout, Idle Timeout and Baud-Rate Calibration Timeout.

- **UART Baud-Rate Control**

The Baud-Rate timer (BR) can configure as an UART Baud-Rate generator or a general using timer. The Baud-Rate timer generator is able to output the internal clock for UART communication Baud-Rate control.

- **UART Mute Mode Control**

The UART module is support a mute mode to disable receiving data character but the shift buffer is still operation for status detection. When the UART is entering mute mode, the RX shadow buffer is never load into data from shift buffer. The mute mode is useful for multi-processor communication.

The mute mode can be automatic by hardware detection to enter or exit by register configuration. Also it can be directly forced to enter or exit by register setting and user can manual to control the mute mode entering and exiting.

- **UART IrDA Control**

The UART module is built an IrDA encoder and an IrDA decoder in the data interface for IrDA communication.

- **UART DE Control**

The UART module provides one data enable signal of **URTx_DE**. This signal is used to indicate the data transmitted period and can output to external signal drive device. The external signal drive device can receive the UART TX signal and drive it with a signal enhanced buffer to the target of UART receiver for long distance communication.

- **UART Hardware Flow Control**

The UART supports a hardware flow control function for data transaction and provides two control signals of **URTx_CTS** (Clear to Send) and **URTx_RTS** (Request to Send) for the hardware flow control.

6.15. SPI

6.15.1. Introduction

The chip provides a high-speed serial peripheral interface (SPI). SPI is a full-duplex, high-speed and synchronous communication bus with two operation modes: Master mode and Slave mode. The SPI clock rate can be up to 24 MHz for Master mode and up to 16 MHz for Slave mode under a 48MHz APB clock.

The SPI module builds in the shadow buffer and data register by transmit and receive independently to improve transmit and receive communication performance.

6.15.2. Features

- **Support master and slave mode**
  - **Support full duplex , half duplex or simplex communication mode**
  - **Support data communication without NSS(slave select signal)**
  - **Support master data input sampling delay half of SPI clock**
  - **Support slave data output advance half of SPI clock**
  - **Support configurable idle state for SPI master standard mode data output**
  - **Support asynchronous clock mode for SPI slave standard mode**
- **Support programmable clock rate control**
- **Selectable 4~32-bit frame size**
  - **Support 4-byte data buffer and 32-bit data register for high speed communication**
- **Received and transmitted data are buffered with DMA capability**
- **Support multi-master processing capability**
- **Selectable clock polarity and phase**
- **Selectable MSB or LSB first data order**
- **NSS line management by hardware or software for master mode**
- **Configurable data transfer modes**
  - **Standard SPI mode (separated transmit and receive line)**
  - **Single/Dual/Quad/Octal SPI mode with bidirectional data transfer**
- **Support DTR (Double Transfer Rate) mode**
- **Data transmit/receive overrun detect**
- **Support hardware master mode failure detection and auto slave mode change**

6.15.3. Module Functions

The following table is showing the implemented functions of SPI0 modules.

Table 6-4. SPI0 Module Function Table

Module Functions	SPI0	Comment
SPI Standard Mode	Master/Slave	2 data line full-duplex communication
SPI 1/2/4-Line Mode	yes	1/2/4 data lines, half-duplex communication
SPI 4-Line Duplicate	-	8 data lines with two duplicated 4 data lines, half-duplex communication
SPI 8-Line Mode	-	8 data lines, half-duplex communication
Slave asynchronous mode	yes	Slave mode process with asynchronous clock input
Master data sampling delay	yes	Master data input sampling delay 1/2 SPI clock time
Slave data output advance	yes	Slave data output advance 1/2 SPI clock time for Mode 0,3
Data line copy mode	yes	all data lines with same data for 2/4 data lines mode
DTR mode	yes	dual transfer rate mode
Swappable MOSI/MISO	yes	
Master mode	yes	
Slave mode	yes	

Msb/Lsb transfer option	**yes**	
Programmable data bit size	**4~32 bits**	4~32 bits
Programmable clock phase and polarity	**yes**	
Hardware NSS control	**yes**	control by hardware for both master and slave
NSS pulse mode	**yes**	optional pulse between two sequent data frame
Programmable NSS pulse width	**yes**	
Back-to-Back Data Transfer	**yes**	when NSS pulse disable
Mode fault detect	**yes**	master mode failure/change detect
Bus Idle detect	**yes**	slave mode bus idle detect
Receive overrun detect	**yes**	
Transmit underrun detect	**yes**	slave mode data transmit underrun
Transmit write error detect	**yes**	slave mode NSS invalid termination; Bit count error
DMA request capability	**yes**	

6.15.4. SPI Control

- **SPI Data Buffer Mode Control**

The module implements two 32-bit shift buffers, two 32-bit shadow buffer and two 32-bit data register for data flow control and reduce the CPU overhead.

- **SPI Data Frame**

User can set the data frame bit size from 4-bit to 32-bit by register. Also user can configure the frame data order by Lsb first or Msb first.

- **SPI Data Modes**

The SPI module provides several data modes and can be configured to one of the modes of standard SPI, 1-Line SPI, 2-Line SPI, 4-Line SPI, two duplicated 4-Line SPI or 8-Line SPI for flexible SPI application.

6.16. CAN (Controller Area Network)

6.16.1. Introduction

The chip provides a Controller Area Network (CAN) interface with bitrates up to 1 Mbit/s. It is a serial communications protocol which supports full CAN 2.0 and distributed real time control with a very high level of security. Its domain of application ranges from high speed networks to low cost multiplex wiring.

The CAN module builds in the receive message FIFOs, transmit message buffers and data register to improve transmit and receive communication performance.

6.16.2. Features

- **Supports full CAN 2.0 – both 2.0A and 2.0B**
  - **Supports both 11-bit and 29-bit identifiers**
  - **Upwards compatible with the CAN FD protocol**
- **Supports bit rates from less than 125Kbit/s to more than 1Mbit/s**
- **Three transmit message buffer**
  - **Configurable transmit priority by request sequence or message identifier order**
- **Two sets of receive message FIFO**
  - **Three stage receive message buffer for each FIFO**
  - **Support one combined message FIFO from all message buffers**
- **Six sets of acceptance filter with identifier mask**
  - **Configurable Mask or List mode for each acceptance filter**
  - **Configurable single 32-bit filter or dual 16-bit filters for each acceptance filter**
- **Error manage with interrupts**
- **Support silent and loop-back mode for self-test operation**

6.16.3. CAN Control

- **CAN Data Buffer Control**

The module implements two receiving message RX FIFOs with separated three message buffer and three independent transmission TX message buffer. Each message buffer are implemented with four 32-bit data registers. The module is implemented the message buffer combined function that all message buffers are combined as one RX message FIFO.

- **Operation Mode**

The module implements three operation modes of ***Initial*** mode, ***Normal*** mode and ***Low Power*** mode. The module will automatically enter ***Initial*** mode after chip reset. Also user can select the three mode by registers setting.

- **CAN Error Mode**

The module implements three error modes of ***Error-Active*** mode, ***Error-Passive*** mode and ***Bus-Off*** mode. There are one transmit error counter register and one receive error counter register those are used to record the number of transmission errors and receiving errors.

- **CAN Test Mode**

The module implements three test modes of ***Silent*** mode, ***Loop Back*** mode and ***Loop Back combined with Silent*** mode. User can set the test mode by register setting.

- **CAN Message Frames**

The module supports standard and extended data frames, standard and extended remote frames, error frame and overload frame as defined message frames in the CAN 2.0B specification

- **CAN Bit Timing**

The CAN module can generate the CAN time quantum clock by register setting for bit timing control. Also user can set the time segment 1, 2 and synchronization jump width to configure the CAN bit timing by registers setting. These registers can only be written in CAN ***Initial*** Mode.

- **CAN RX Acceptance Filter**

The CAN module provides six configurable CAN receiving RX acceptance filters for filtering the incoming message data. Each RX acceptance filter has independent registers to define the acceptance filter code and code mask. User can configure to enable or disable for each the RX acceptance filter by setting the independent register. Also each the RX acceptance filter can configure for using RX message FIFO0 or FIFO1 by setting independent register.

Each RX acceptance filter can be configure to one single 32-bit filter or dual 16-bit filters. Also each RX acceptance filter can be configure to ‘Mask’ mode or ‘List’ mode.

6.17. Timer

6.17.1. Introduction

The chip has seven Timer/Counter modules: TM00, TM01, TM10, TM16, TM20, TM26 and TM36. All of them can be configured as timers or event counters.

TM0x has an 8-bit timer/counter with 8-bit prescaler. TM1x has a 16-bit timer/counter with 16-bit prescaler. TM2x has a 16-bit timer/counter with 16-bit prescaler and embeds two input capture/output compare channels. TM36 has a 16-bit timer/counter with 16-bit prescaler and embeds four input capture/output compare channels.

6.17.2. Features

- **Provide seven timers/counters : TM00,TM01,TM10,TM16,TM20,TM26,TM36**
- **Timer module common functions**
  - **Selectable Full-counter , Cascade , Separate modes**
  - **Multiple internal and external signals as timer clock source or trigger source**
  - **Internal timer events output to pin or other modules as input trigger event**
  - **Support timer reset , trigger start and clock gating for trigger source function**
  - **Timer overflow as clock output to external pin output**
  - **Programmable counter auto-stop mode**
  - **Main counter support up/down control (TM16/TM26/TM36 only)**
  - **2nd counter support up/down control (Separate mode)**

- Provide TM36 timer module
  - 32-bit timer/counter
  - 4 CCP (input Capture/output Compare/PWM) channels
  - 3 CCP channels with OCN (complementary output compare)
  - PWM function with center-align, dead time control and break control
  - Support OC comparator split to two separated comparators mode
  - QEI(Quadrature Encoder Interface) support
  - Two IC and three OC with DMA capability
  - Extra repetition counter for auto-stop mode
  - Support duty capture function
  - Up to 96MHz clock source for PWM output
- Provide TM2x timer modules
  - 32-bit timer/counter
  - 2 CCP (input Capture/output Compare/PWM) channels
  - 2 CCP channels with OCN (complementary output compare)
  - PWM function with edge-align
  - Support OC comparator split to two separated comparators mode
  - QEI(Quadrature Encoder Interface) support (TM26 only)
  - Extra repetition counter for auto-stop mode
- Provide TM1x timer modules (TM10,TM16)
  - 32-bit timer/counter
- Provide TM0x timer modules (TM00,TM01)
  - 16-bit timer/counter

6.17.3. Module Functions

The following table is showing the implemented functions of Timer modules.

Table 6-5. Timer Module Function Table

Module Functions	TM00/01	TM10	TM16	TM20	TM26	TM36
Timer/Counter total bits	16	32	32	32	32	32
Timer Cascade Mode	yes	yes	yes	yes	yes	yes
Timer Separate Mode	yes	yes	yes	yes	yes	yes
Timer Full-Counter Mode	yes	yes	yes	yes	yes	yes
Independent channels				2	2	4
Internal TRGI lines	8	8	8	8	8	8
External TRGI lines	1	1	1	1	1	1
Output TRGO lines	1	1	1	1	1	1
Output CKO lines	1	1	1	1	1	1
Input Capture IC lines				2	2	4
Output OC/OCN/OCH lines				2/2/2	2/2/2	4/4/4
Input Break lines						1
PWM separated two				yes	yes	yes
PWM edge-align				yes	yes	yes
PWM center-align						yes
Dead-time generator						yes
Up/Down of 1st Timer	U	U	U/D	U	U/D	U/D
Up/Down of 2nd Timer	U/D	U/D	U/D	U/D	U/D	U/D
Timer auto Stop	yes	yes	yes	yes	yes	yes
Repetition Counter				yes	yes	yes
QEI timer U/D control					yes	yes
3-input XOR to CH-0						yes
NCO output as clock	yes	yes	yes	yes	yes	yes

Channel output delay				yes	yes	yes
PWM 96MHz clock						yes
DMA request capability						yes

<Note> 1. Timer Cascade Mode ~ 16-bit_counter+16-bit_prescaler or 8-bit_counter+8-bit_prescaler
2. Timer Separate Mode ~ two 16-bit_counter or 8-bit_counter
3. Timer Full-Counter Mode ~ 32-bit_counter or 16-bit counter

6.17.4. Timer Control Block

The TMx module is including of a Trigger/Clock control block, a Counter Stage, an Capture/Compare control block and Input/Output Stages of channel I/O control (TM2x,TM3x only) and a Break control block (TM36 only). TMx support three timer operation modes: (1) Cascade Mode (2) Separate Mode (3) Full-Counter Mode.

- **Trigger Control Block**

The Trigger Control block has two functions, one is to control the timer trigger input events and another is to control the timer trigger output events.

The timer trigger input events are including of Reset Timer, Gated Clock and Timer-Start Trigger for Main Timer and 2nd Timer. The input source of the timer trigger input events is selected from external trigger signal, internal trigger signals or external channel input signal of **TMx_IN0**/**TMx_IN1**.

The source of the timer trigger output events are able to come from many internal events or signals of this timer module. Also user can use the software register to set the trigger output directly. This source of output event can select and invert the output signal by registers.

- **Timer Input/Output Channels**

The following table is showing the channel input signals for each timer module. TM0x and TM1x modules are no channel input selection function as the input capture/output compare is not support. Each channel has four input lines.

- **Timer Input Capture and Output Compare**

The input capture (IC) and output compare (OC) functions are only supported for TM2x and TM3x modules. TM0x and TM1x modules are no the functions of the input capture/output compare.

User can configure each of the timer IC/OC channel independently as input capture, output compare or PWM mode.

- **PWM Dead-Time Control**

The Dead Time Generator (DTG) is only support for TM36 module. User can use with the DTG function and configure the timer channel as 16bit PWM mode or Two 8bit PWMs mode.

- **Break Control Block**

The break control block is only support for TM36 module. The module can input the break events from internal events, external events or software register to break the timer output signals.

- **QEI Control Block**

The QEI (Quadrature Encoder Interface) control block is only support for TM26 and TM36 modules. The QEI block can input from two external signals to control the Main Timer up or down counting. The QEI block provides five control modes and user can enable QEI control and configure the QEI control mode by register.

When the QEI control block is enabled, the timer will reset during up counting or reload the auto-reload value during down counting if detect the index signal active pulse.

6.18. IWDT

6.18.1. Introduction

The chip has one independent Watch-dog timer to use as a recovery method in situations where the CPU may be subjected to software upset. It will trigger system reset when the counter reaches a given timeout value.

6.18.2. Features

- **8-bit down counter with 12-bit prescaler and clocked by its own CK_ILRCO**
- **Operating capability in SLEEP and STOP modes**
- **Selectable reset or interrupt when the counter underflow**

- **Support two early wakeup comparators with interrupt**
- **Support register key-protected and reset-locked functions**

6.18.3. IWDT Control

The IWDT watch-dog timer consists of a 12-bit prescaler and an 8-bit timer. When the watch-dog timer is enabled, software should always reset the timer before the timer is timeout. When the watch-dog timer is reset, the timer will be reloaded 0xFF value to restart counting.

If the chip is out of control by any disturbance, the firmware may miss to reset the timer and the timer timeout will be coming. It makes the IWDT generating a reset event and sends it to Reset Source Controller (RST) to do as the warm reset events or cold reset events.

The IWDT is able to record default initialized value in hardware option byte (***OB***) about IWDT on/off, input clock divider value, IWDT registers write protection.

The IWDT is able to operate in ***STOP*** mode and the APB clock is stopped and the module is asynchronous control for all logic.

The IWDT supports to wakeup chip in ***STOP*** mode by the events of watch-dog timer underflow and early wakeup-0/1 detection. When the chip is entering ***STOP*** mode and any of these IWDT wakeup events is happened, the IWDT will send the wakeup event to Power Controller (PW) to do as the system wakeup events.

6.19. WWDT

6.19.1. Introduction

The system window watchdog is used to detect the occurrence of a software fault which causes the application program abnormal. The watchdog circuit generates a system reset when the counter reaches a given timeout value.

The WWDT has a configurable time-window that can be programmed to detect abnormally late or early application behavior.

6.19.2. Features

- **10-bit counter with 1 or 256 divider , 1/2/4~/128 divider**
- **Configurable time-window to detect abnormally late or early application behavior**
- **Selectable reset or interrupt when the counter is underflow or reloaded outside the window**
- **Support warning interrupt**
- **Support register key-protected and reset-locked functions**

6.19.3. WWDT Control

The WWDT watch-dog timer consists of one /1 or /256 clock prescaler, one 7-bit clock divider and one 10-bit timer. When the watch-dog timer is enabled, software should always reset the timer before the timer is timeout. When the watch-dog timer is reset, the timer will reload the value to restart counting.

When the firmware is out of control, which may miss to reset the timer and the timer timeout will be coming. It makes the WWDT generating a reset event and sends it to Reset Source Controller (RST) to do as the warm reset events or cold reset events. If the firmware reset the timer and the counter value is over the threshold value of window compare threshold in the same time, it also makes the WWDT generating a reset event.

6.20. RTC

6.20.1. Introduction

The real-time clock is an independent 32-bit timer. The RTC provides a time clock with programmable alarm interrupt. User can use as a calendar with software programmable alarm seconds, minutes, hours, day, and date.

The RTC provides a wakeup flag to perform auto wakeup from power down mode with interrupt.

6.20.2. Features

- **Built-in 32-bit counter with selectable clock source**
- **Support alarm function and time-stamp function**

- **Support alarm function with 32-bit programmable compare register**
- **Support wakeup from Stop mode**
- **Support periodic timer tick interrupt or wakeup**
- **Support register key-protected and reset-locked functions**

6.20.3. RTC Control

The RTC supports an alarm function and one register to sets the RTC alarm compare value. When the RTC timer value is matched with RTC alarm compare value, the RTC alarm flag is asserted and generates an interrupt. Also the RTC can capture from the 32-bit timer value or reload value to the 32-bit timer.

The RTC supports a time stamp function by external input. User can select input trigger edge of rising edge, falling edge or dual-edge. When an external input signal is matched, the RTC time stamp flag is asserted and generates an interrupt.

One **RTC_OUT** output is able to output the RTC internal signals to internal modules or external pin. There are four signals of timer overflow signal toggle output, time stamp trigger event, timer input periodic clock signal and alarm compare output event which can be selected and sent from **RTC_OUT** output.

The RTC is able to operate in ***STOP*** mode and the APB clock is stopped and the module is asynchronous control for all logic.

The RTC supports to wakeup chip in ***STOP*** mode by the events of timer overflow, timer input periodic clock and alarm compare output. When the chip is entering ***STOP*** mode and any of these RTC wakeup events is happened, the RTC will send the wakeup event to Power Controller (PW) to do as the system wakeup events.

6.21. LCD (Liquid Crystal Display)

6.21.1. Introduction

The chip is built-in a LCD module which is including of the LCD controller, charge pump, bias generator and IO voltage drivers. The IO voltage drivers can directly drive the external monochrome passive LCD panel. It supports total 44 LCD driver lines with configurable LCD common or segment for maximum 8 common (COM) lines and 40 segment (SEG) lines. It supports static,1/2, 1/3, 1/4 bias voltage and static,1/2, 1/3, 1/4, 1/5, 1/6, 1/7, 1/8 duty.

The LCD controller can directly drive LCD displays and automatically generate the requested voltage waveform to avoid an electrophoresis effect for each configured common pin and segment pin. It is embedded the LCD display memory with blinking display function. It also supports both type-A and type-B frame timing mode with dead time control.

6.21.2. Features

- **Support external power input, internal VDD or internal charge pump voltage source**
  - **VDD voltage range 2.0V to 5.5V for internal charge pump**
  - **External LCD_VT voltage range 1.8V to 5.5V for external power input**
  - **Internal charge pump with adjustable contrast adjustment**
- **Embedded LCD bias reference ladder**
  - **LCD power rails (LCD_V1, LCD_V2, LCD_V3, LCD_VT) with external decoupling capability**
  - **Support external resistor ladder optional**
- **Provide maximum 8 common/40 segment and total 44 pins with GPIO alternate function**
  - **Up to drive 160 (40x4), 228 (38x6) or 288 (36x8) LCD dots**
  - **Support configurable common or segment for each LCD pins**
  - **Support hardware phase inversion**
- **Support Static,1/2, 1/3 and 1/4 bias voltage**
- **Support Static,1/2, 1/3, 1/4, 1/5, 1/6, 1/7 and 1/8 duty**
- **Supports Type-A or Type-B frame control mode**
  - **Configurable LCD frame frequency**
- **Embedded LCD data RAM**
- **Programmable dead time between frames or duty phases.**
- **Support LCD blinking display**

- **LCD start frame interrupt for LCD data RAM update**
- **Support LCD display on SLEEP and STOP modes**

6.21.3. LCD Control

- **LCD Analog Control**

The LCD module is built-in charge pump, bias generator and IO voltage drivers. The IO voltage drivers can directly drive the external monochrome passive LCD panel.

User can select the LCD power source as the operation voltage of bias generator from internal AVDD (through **VDD**), external voltage from **LCD_VT** pin or internal charge pump.

When the internal charge pump is used, a suggested 0.01uF capacitor must be connected between the **LCD_C1** and **LCD_C2** pins.

The bias generator supports static,1/2, 1/3, 1/4 bias voltage. There are four pins of **LCD_VT**, **LCD_V1**, **LCD_V2** and **LCD_V3** can be independent configuration to connect internal bias power rail to external capacitor for LCD bias voltage stability. These external capacitors are suggested to use 0.1uF capacitor. When LCD power is selected internal charge pump, user can set the bias generator operation top voltage level for contrast control by register setting.

The module can support to use internal resister ladder or external resister ladder to generate bias voltage. Also it can provide high drive strength function and select the driving mode.

- **LCD Display Data Control**

The module is embedded the LCD display memory and implements an independent 8-bit data register for each LCD pins. Each of the 8-bit data register bits can use to do display data bits or COM selection bits.

- **LCD Dead Timing**

The LCD controller supports LCD timing with dead time control in LCD frame period or phase duty period. When user selects TYPE-B LCD timing, user is only able to set dead time control in LCD frame period.

Also user can set LCD output dead time period width by register setting. The dead time period setting unit is one **CK_LCD_PHS** (LCD phase period) for using 'frame period ' or one **CK_LCD_INT** period for using 'phase duty period'. During the dead time, all COM and SEG pins are driven to ground.

- **LCD Blinking Control**

The LCD controller supports LCD timing with blinking function. A blinking clock divider is used to divide the LCD frame clock **CK_LCD_FRM** to generate the LCD blinking clock **CK_LCD_BLK**.

When user enables the LCD blinking function, the LCD controller will continuously toggle the LCD display between normal display and blank display at the calculated blinking frequency.

- **LCD Drive Timing Inverse**

The LCD controller supports LCD timing with output waveform inverse control. When user enables the LCD output waveform inverse function, all COM and SEG waveform outputs are inverted.

6.22. OPA (Operational Amplifier)

6.22.1. Introduction

The chip builds in one OPA module which embeds one general purpose operational amplifier of OP0 with two inputs and one output. It also can be configured as one general purpose analog comparator. The OPA output can be connected to internal input channel of ADC and CMP modules.

6.22.2. Features

- **Embedded one operational amplifier**
- **Provide two external inputs and one output for one OPA**
  - **Provide internal ADC PGA output and VBUF voltage connection**
  - **Support OPA output to ADC and CMP internal channel input**
- **Support low power mode for optimal current consumption**

6.22.3. OPA Control

- **Low Power mode**

The OPA can support the low power mode for optimal current consumption. For analog comparator function, it is also control the response time of comparator for different applications.

6.23. ADC

6.23.1. Introduction

The chip builds in one ADC0 module which embeds one 12-bit successive approximation ADC (analog-to-digital converter), one PGA (programmable gain amplifier) with gain 1~128 and digital logic for output code control. It supports the configurable multiplexed channels those include 16 external and 7 internal sources. The analog-to-digital conversion can be performed in one-shot, continuous, one-loop scan or continuous loop scan modes.

The ADC is embedded one temperature sensor to measure the internal thermal of chip for product application.

6.23.2. Features

- **12-bit SAR ADC with 1.5Msps**
  - **Configurable resolution : 12/10/8-bit**
  - **Configurable sampling time**
- **Provide external 16 channels and internal 7 channels input**
  - **Internal channel source : VBUF, VSSA , LDO VCAP, 1/4VDD, LCD_V1, OP0_P0, TS out**
- **Support auto-sampling and trigger by external pin , internal events and software bit**
- **Data alignment for output code left/right justify**
- **Built-in input buffer stage with bypass option**
- **PGA with programmable gain : 1~128**
- **Provide internal voltage source VBUF 1.4V**
- **Optional ADC top voltage reference from external VREF+ or internal IVR24**
- **Interrupt generation at the end of sampling, end of conversion, end of sequence conversion**
- **Support voltage window detect and output code limitation**
  - **Two level programmable window threshold**
- **Built-in three channel independent hardware accumulator for ADC output code**
- **Support one-shot/channel scan/loop scan**
- **ADC data are buffered with DMA capability**
- **Support wait mode**
  - **Prevents ADC overrun in application with low frequency**
- **Support auto off mode**
  - **ADC auto power off except during the active conversion phase**
- **Built-in a temperature sensor**
  - **Temperature resolution : +/- 2 °C (Typical)**
  - **Temperature operation range : -40°C ~ 125°C**

6.23.3. ADC Control Block

The ADC control block consists of an analog multiplexer (AMUX) with 16 input channels, a **1.5M**sps/**12**-bit SAR (successive-approximation-register) ADC, reference voltage circuit, ADC conversion trigger start control block and change scan control block.

- **ADC Input Channels**

The analog multiplexer (AMUX) selects the inputs to the ADC, allowing any of the input pins to be measured in single-ended mode.

The analog input pins used for the A/D converters also have its I/O pins for digital input and output function. In order to give the proper analog performance, a pin that is being used with the ADC should have its digital output as disabled. It is done by putting the port pin into the input-only mode. And when an analog signal is applied to the **ADC_In** pin and the digital input from this pin is not needed, software could set the corresponding pin to AIO mode to turn off the digital input buffer to reduce current consumption.

- **Single-End Mode**

The ADC supports single-end operation modes. The ADC can convert the ADC output to unsigned code for single-end mode.

- **ADC Sampling Time**

  For input signal quality and conversion speedy issue, user can adjust the ADC sampling time. Usually user can increase the ADC sampling time to get more stable voltage and better ADC performance if the conversion rate and signal bandwidth are reasonable and valid for actual application.

- **ADC Conversion Mode**

  The ADC is supported three conversion modes of One Shot, Channel Scan and Loop Scan.

- **ADC Output Control**

  When an ADC conversion is complete, the ADC raw code is generated and sends to the ADC output control blocks those are including of Digital Offset Adjuster, Signed Code Converter, Digital Resolution Adjuster, Voltage Window Detector, Code Limiter and Data Alignment Adjuster.

  The ADC output code will be adjusted by the ADC output control blocks and store the conversion result date to the ADC data register.

- **Voltage Window Detect and Code Limit**

  The ADC can compare the input voltage by a threshold window. Also the ADC output code can be compared by a code limit area to skip or clamp the code by the same threshold window.

- **ADC Data Sum Accumulate**

  The ADC built-in one hardware accumulator for ADC output code. The accumulator is used to accumulate the sequential ADC data with programmable data number and records the sum to the summary registers. User can set the accumulated ADC data number. The ADC is supported three sum data registers and user can get the accumulated sum from these registers.

- **ADC Wait and Auto-Off**

  The ADC supports a wait mode function to prevent ADC overrun in application with low frequency ADC sampling clock. Also ADC supports an auto off mode function to force the ADC auto entering power-off except during the active conversion phase.

- **Embedded Temperature Sensor**

  The ADC module is embedded a temperature sensor which can be enabled and output voltage through ADC internal channel to the SAR ADC. User can get temperature information from the ADC output code to calculate the chip temperature.

6.24. Analog Comparator

6.24.1. Introduction

The chip builds in one CMP module which embeds two general purpose analog comparators with flexible input multiplexer, two internal voltage references of R-ladder and independent digital synchronized filter for each analog comparator. These analog comparators can be configured to two standalone comparators or a combined window comparator. The module provides the comparator output result status bit and the interrupt flags of rising edge or falling edge change. Also the output result can be output to external pin or internal other modules for trigger event.

6.24.2. Features

- **Provide 2 fast comparators**
- **Programmable 64-step threshold of internal voltage reference**
  - **Selectable top reference voltage from VDD or LDO_VCAP**
- **Provide external total 6 channels input for all comparators**
- **Provide flexible 6 channels input for each +/- input path selection**
- **Programmable response time for optimal current consumption**
- **Combined window comparator from two comparators**
- **Selectable compare output polarity**
- **Support wakeup from SLEEP and STOP modes**
- **Compare output to I/O , interrupt or as internal module trigger event**
  - **Timer internal trigger, Capture events, or Break events**

- **Support analog watch dog as a reset source**

6.24.3. CMP Control Block

The CMP module includes two general purpose analog comparators CMP0~1 by the same design structure and two internal voltage references ***IVREF***/***IVREF2*** by R-ladder structure. Each one is with the independent input multiplexer, digital synchronized filter and digital output circuit. The ***IVREF*** is only using for CMP0 and the ***IVREF2*** is only using for CMP1.

The analog comparator is built-in two internal voltage references – ***IVREF*** and ***IVREF2*** with 64-steps R-ladder structure. They can use as one of the analog comparator input and compare with another input from external source.

Each the analog multiplexer (AMUX) of the positive or negative input of any analog comparator has flexible 6 channels input. These channels are including of two common external channels, two comparator independently external channels and two common internal channels.

The two common external channels are from **CMP_C0** and **CMP_C1** pins those can input to all analog comparators. The two independent external channels are from **CMPn_I0** and **CMPn_I1** pins those can input to the analog comparator CMP0/1. The two common internal channels are from internal voltage reference of ***IVREF*** or ***IVREF2*** and internal LDO output (**LDO_VCAP**) those can input to all analog comparators.

The analog input pins used for the comparators also have its I/O port's digital input and output function. In order to give the proper analog performance, a pin that is being used should have its digital output as disabled. It is done by putting the port pin into the digital input mode. And when an analog signal is applied to the analog input pin and the digital input from this pin is not needed, software could set the corresponding pin to AIO mode to reduce current consumption in the digital input buffer.

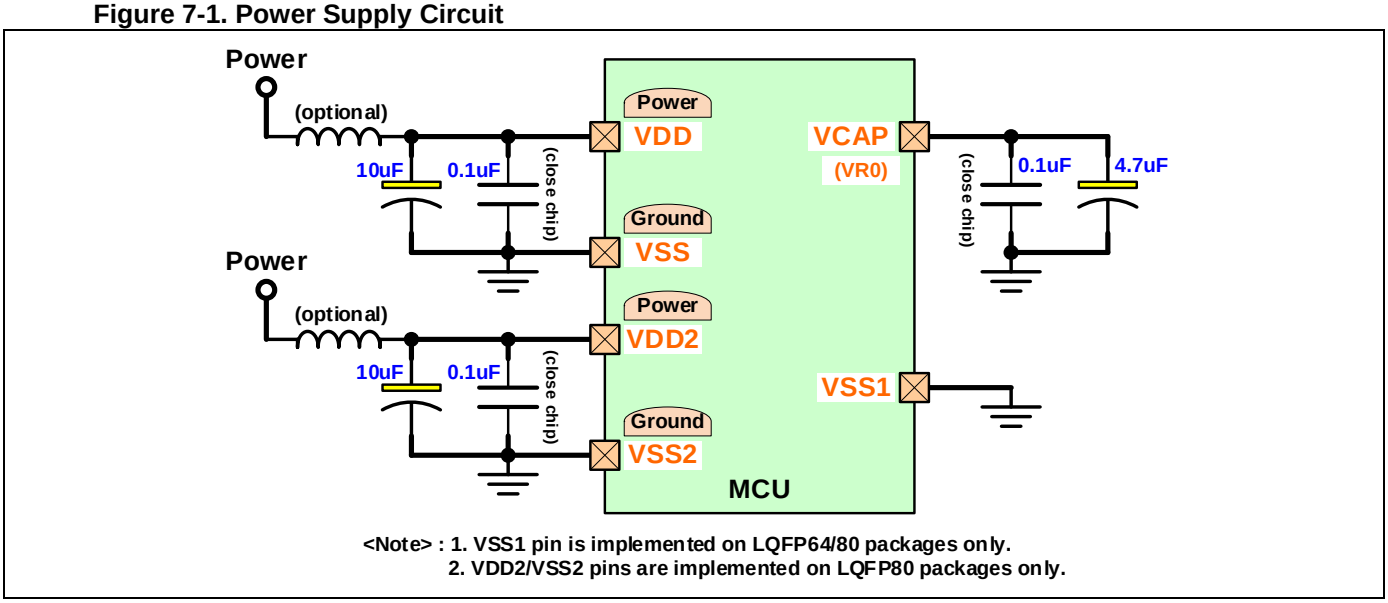
7. Application Notes

7.1. Power Supply Circuit

To have the chip work with power supply varying from 1.8V to 5.5V, adding some external decoupling and bypass capacitors is necessary on **VDD/VSS** power pins, as shown in following figure. Also the same application suggestion on **VDD2/VSS2** power pins for LQFP80 package. The **VCAP** pin is the embedded LDO voltage output as internal core logic power supply. It needs to place one 0.1uF capacitor and one 4.7uF capacitor to be closed the pin.

The following figure is showing the power supply suggestion circuit.

Figure 7-1. Power Supply Circuit



<Note> : 1. VSS1 pin is implemented on LQFP64/80 packages only.
2. VDD2/VSS2 pins are implemented on LQFP80 packages only.

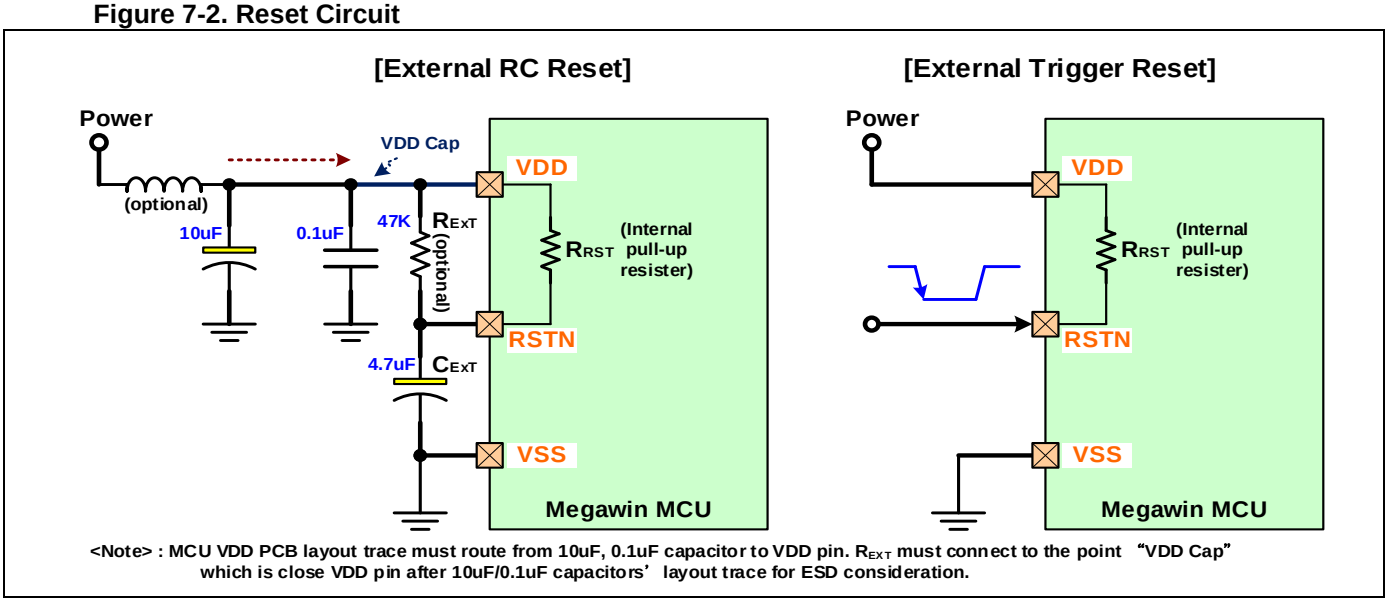
7.2. Reset Circuit

Normally, the power-on reset can be successfully generated during power-up. However, to further ensure the MCU a reliable reset during power-up, the external reset is necessary. The following figure shows the external reset circuit, which consists of a capacitor ***CEXT*** connected to **VSS** (ground) and a resistor ***REXT*** connected to **VDD** (power supply).

In general, ***REXT*** is optional because the **RSTN** pin has an internal pull-high resistor (***RRST***). This internal diffused resistor to **VDD** permits a power-up reset using only an external capacitor ***CEXT*** to **VSS**.

Strongly suggestion, the **RSTN** pin must set to output mode if it is used to do as both chip reset and GPIO functions in application. In this condition, the pin input low may make chip reset locked error if it set to GPIO input mode.

Figure 7-2. Reset Circuit

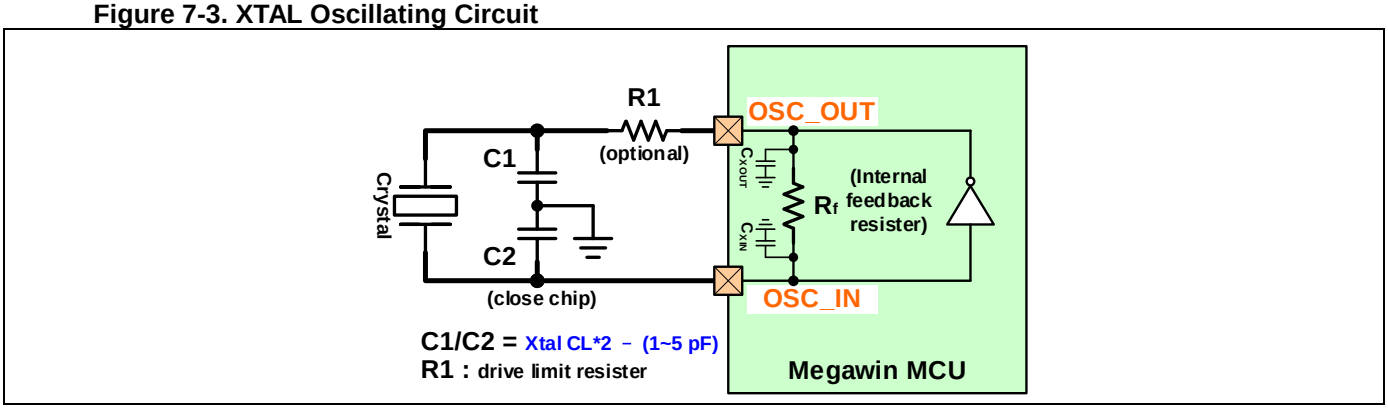


<Note> : MCU VDD PCB layout trace must route from 10uF, 0.1uF capacitor to VDD pin. R_{EXT} must connect to the point "VDD Cap" which is close VDD pin after 10uF/0.1uF capacitors' layout trace for ESD consideration.

7.3. Xtal Oscillating Circuit

To achieve successful and exact oscillating (up to 25MHz), the capacitors ***C1*** and ***C2*** are necessary, as shown in following figure. Normally, ***C1*** and ***C2*** have the same value. Refer the capacitor load (**CL**) value in Xtal manufacture specification for the final matching capacitor of ***C1*** & ***C2***.

Figure 7-3. XTAL Oscillating Circuit



❖ Xtal Capacitor Selection

C_{XIN} / C_{XOUT}: Chip internal total equivalent capacitance of internal oscillator circuit, bounding pad, bounding wire and lead frame.

Table 7-1. Internal Total Equivalent Capacitance for XOSC circuit

Component	Capacitance Value (VDD=5.0V)
C_{XOUT}	0.85pF (0.82~0.94pF)
C_{XIN}	0.85pF (0.82~0.93pF)

The XTAL Load Capacitance CL = C11 // C22 + Cp

C11 = C1 + C_{XOUT}

C22 = C2 + C_{XIN}

Cp: the distribution/stray capacitance that is generated by PCB layout path

= 1.18 pF/in for 2-layer FR4 PCB (Trace width=12mil, PCB height= 1.6mm)

= 3.16 pF/in for 4-layer FR4 PCB (Trace width=10mil, Subtract height=6mil)

The following table lists the suggested ***C1*** & ***C2*** value for the different capacitor load (**CL**) crystal application.

Table 7-2. Reference Capacitance of C1 & C2 for crystal oscillating circuit

Crystal C Load	C1, C2 Capacitance
12.5pF	20pF (18~22pF)
20pF	36pF (33~39pF)
32pF	62pF (56~62pF)

❖ Xtal Capacitor Value Calculation Example

- **C1/C2 Capacitor Selection Example-1**

If CL = 12.5 pF (get from Xtal manufacture specification),

Cp = 1~2pF, then C11//C22 = 10.5 ~ 11.5 pF

$$\frac{C11 * C22}{C11 + C22} = 10.5 \sim 11.5\ pF$$

C11 and C22 are symmetric, we can get C11 = C22 = 21 ~ 23 pF.

Then C1 = C11 - C_{XOUT} = 20.06pF ~ 22.18pF → 20pF

C2 = C22 - C_{XIN} = 20.07F ~ 22.18pF → 20pF

- **C1/C2 Capacitor Selection Example-2**

If CL = 20 pF (get from Xtal manufacture specification),

Cp = 1~2pF, then C11//C22 = 18 ~ 19 pF

$$\frac{C11 * C22}{C11 + C22} = 18 \sim 19\ pF$$

C11 and C22 are symmetric, we can get C11 = C22 = 36 ~ 38 pF.

Then C1 = C11 - C_{XOUT} = 35.06pF ~ 37.18pF → 36pF

C2 = C22 - C_{XIN} = 35.07pF ~ 37.18pF → 36pF

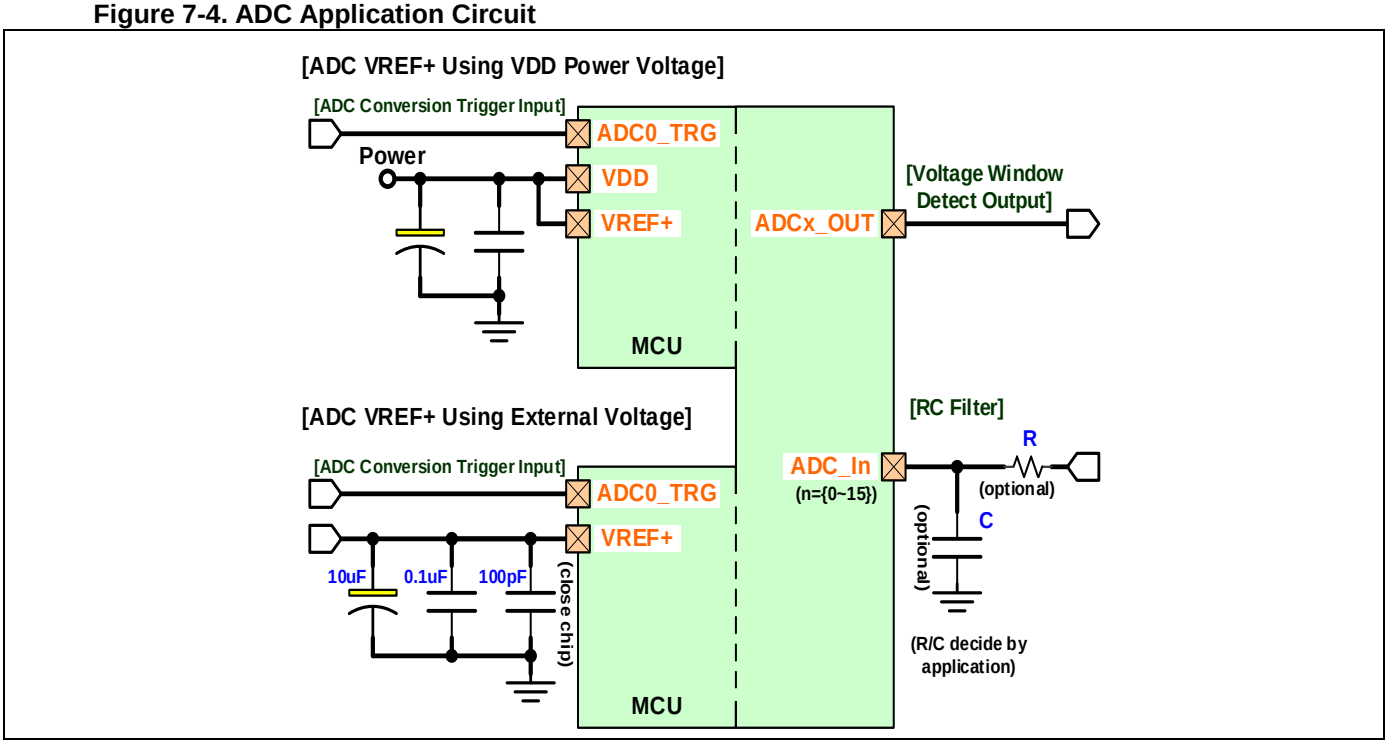
7.4. ADC Application Circuit

The ADC reference voltage source can be from (1) VDD power by connecting **+VREF** pin to **VDD** pin directly (2) external quiet reference voltage source.

When uses the VDD power as the ADC reference voltage, it must connect **+VREF** pin trace to the point which is at current flow behind the power capacitor(s). When uses the external reference voltage source as the ADC reference voltage, it must add some decoupling and bypass capacitors, as shown in following figure.

An optional **ADCx_TRG** pin is able to input the trigger signal for ADC input conversion and an optional **ADCx_OUT** pin is used to output the internal ADC window detection status.

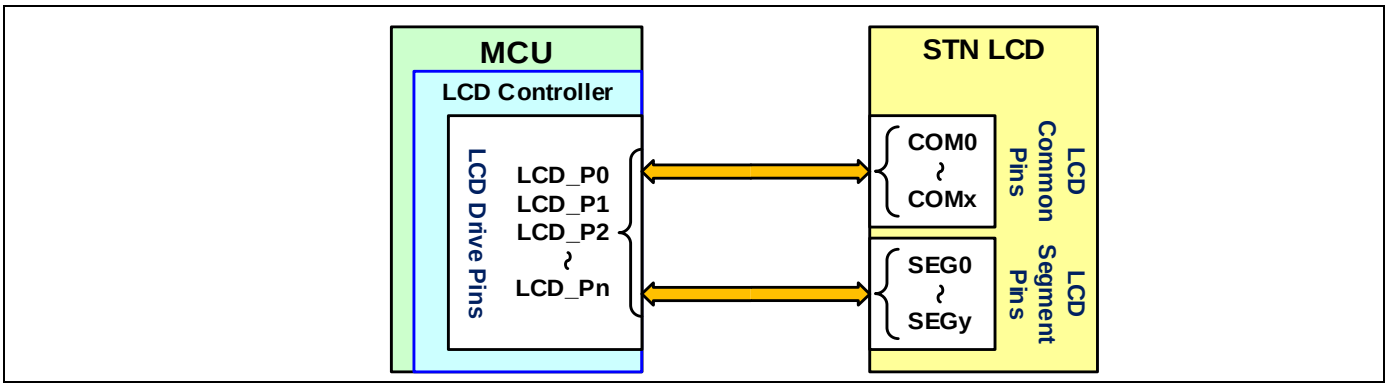
Figure 7-4. ADC Application Circuit



7.5. LCD Application Circuit

The LCD module can directly connect and drive the external monochrome passive LCD panel through the configured LCD **LCD_P[43:0]** pins to the necessary COM and SEG lines of external LCD panel. The following diagram is showing the LCD application connection.

Figure 7-5. LCD COM/SEG Connection

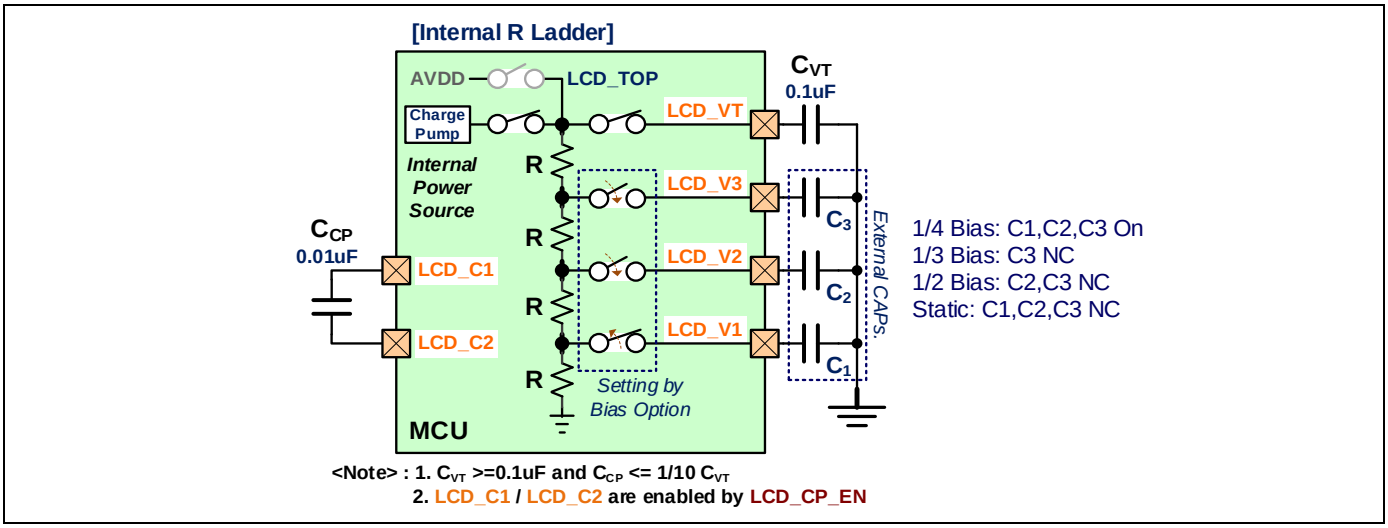


7.5.1. LCD Bias with Internal Charge Pump

When **LCD_VS_SEL** is selected internal charge pump, user needs connect internal bias power rail to external capacitor through **LCD_VT**, **LCD_V1**, **LCD_V2** and **LCD_V3** pins for selected bias voltage by setting independently **LCD_VT_CTL**, **LCD_V1_CTL**, **LCD_V2_CTL** and **LCD_V3_CTL** registers. These external capacitors are suggested to use 0.1uF capacitor. For internal charge pump using, a suggested 0.01uF capacitor must be connected between the **LCD_C1** and **LCD_C2** pins.

The following diagram is showing the application connection of LCD Bias with internal Charge Pump.

Figure 7-6. LCD Bias with Internal Charge Pump

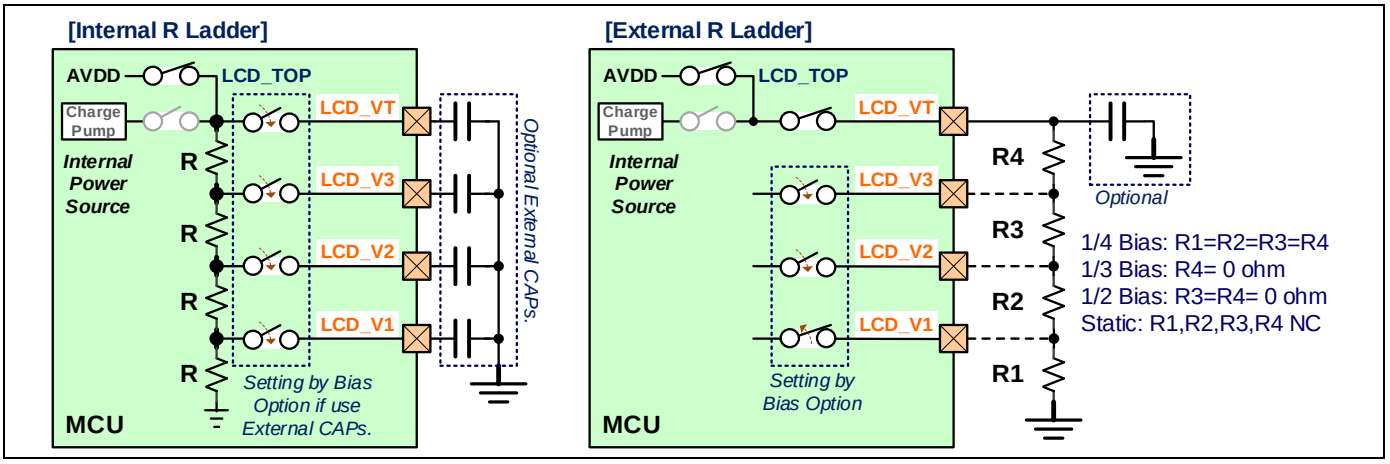


7.5.2. LCD Bias with Internal AVDD

When **LCD_VS_SEL** is selected internal AVDD, user can optionally connect internal bias power rail to external capacitor through **LCD_VT**, **LCD_V1**, **LCD_V2** and **LCD_V3** pins for selected bias voltage by setting independently **LCD_VT_CTL**, **LCD_V1_CTL**, **LCD_V2_CTL** and **LCD_V3_CTL** registers. User can select internal resister ladder or external resister ladder to generate bias voltage by setting **LCD_RL_SEL** register.

The following diagram is showing the application connection of LCD Bias with internal AVDD.

Figure 7-7. LCD Bias with Internal AVDD

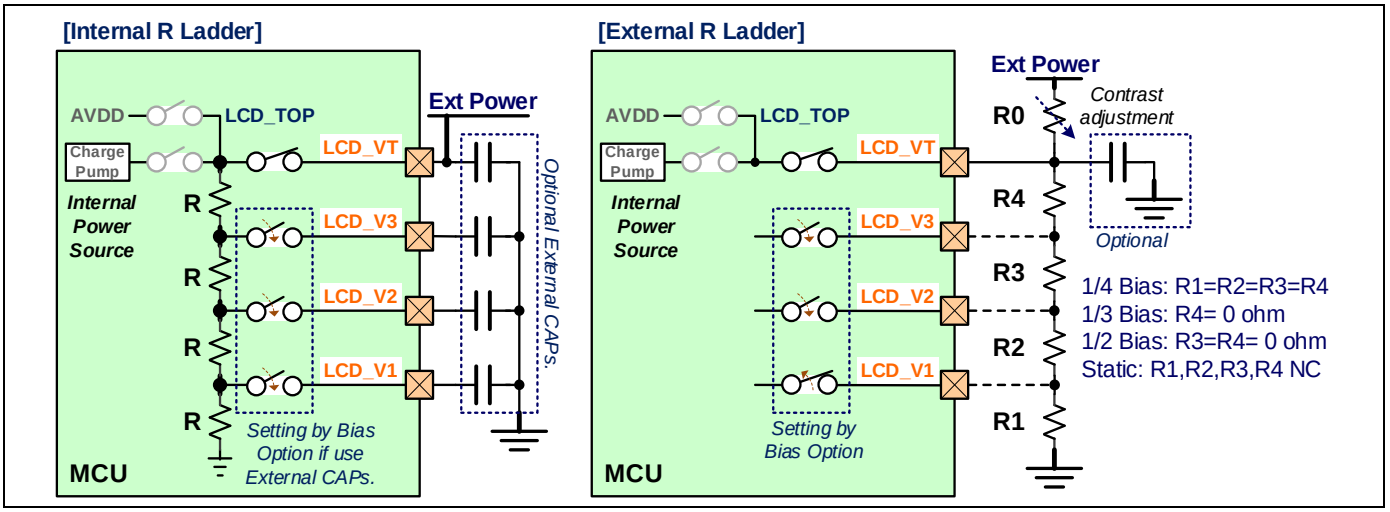


7.5.3. LCD Bias with External Power

When **LCD_VS_SEL** is selected external power voltage, user can optionally connect internal bias power rail to external capacitor through **LCD_VT**, **LCD_V1**, **LCD_V2** and **LCD_V3** pins for selected bias voltage by setting independently **LCD_VT_CTL**, **LCD_V1_CTL**, **LCD_V2_CTL** and **LCD_V3_CTL** registers. User can select internal resister ladder or external resister ladder to generate bias voltage by setting **LCD_RL_SEL** register.

The following diagram is showing the application connection of LCD Bias with external power.

Figure 7-8. LCD Bias with External Power



8. Electrical Characteristics

8.1. Parameter Glossary

Table 8-1. Parameter Glossary

Symbol	Definition	Descriptions
Abbreviations for electrical characteristics		
Min	Minimum value	Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value.
Max	Maximum value	Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value.
Typ	Typical value	Unless otherwise specified, the value is based on TA=25 °C, VDD=5V.
VDD	Power supply voltage	The voltage range is specified in characteristics table or conditions column.
VSS	Power reference voltage	Unless otherwise specified, all voltages are referred to VSS.
TA	Ambient temperature	The temperature range is specified in characteristics table or conditions column.
T_{PC}	Peripheral clock cycle time	The peripheral input clock source may select APB, SYS or other clock. This clock frequency needs lower than 1/2 of the module process clock frequency.

8.2. Absolute Maximum Rating

Table 8-2. Absolute Maximum Rating

Parameter	Rating	Unit
Ambient temperature under bias	-40 ~ +105	**°C**
Storage temperature	-65 ~ + 150	**°C**
Voltage on any Port I/O Pin or RST with respect to VSS	-0.5 ~ VDD + 0.5	**Volt**
Voltage on VDD with respect to VSS	-0.5 ~ +6.0	**Volt**
Maximum total current through VDD and VSS	200	**mA**
Maximum output current sunk by any I/O pin	40	**mA**

Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

8.3. DC Characteristics

Table 8-3. DC Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25 °C and execute NOP for each CPU cycle (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
	Current Consumption (VDD=5.0V)					
I_{OP1}	ON(normal) mode operating current	TL1 (APB=AHB=32KHz) dhrystone		0.11		mA
I_{OP2}		TL2 (APB=AHB=12MHz) dhrystone		2.52		mA
I_{OP3}		TL3 (APB=AHB=24MHz) dhrystone + IP		7.5		mA
I_{OP4}		TL4 (APB=AHB=24MHz - XTAL) dhrystone + IP		8.1		mA
I_{OP5}		TL5 (APB=AHB=24MHz - EXTCK) dhrystone + IP		7.2		mA
I_{OP6}		TL6 (APB=AHB=48MHz) dhrystone + all IP		13.5		mA
I_{SLP0}	SLEEP mode operating current (IWDT Enable)	SL0 (ILRCO on: IWDT Disable, APB=AHB=32KHz)		108		uA
I_{SLP1}		SL1 (IHRCO on: APB/AHB=6MHz/3MHz)		1140		uA
I_{SLP2}		SL2 (IHRCO on: APB=AHB=12MHz)		1417		uA
I_{SLP3}		SL3 (XTAL=12MHz: APB/AHB=6MHz/3MHz)		1700		uA
I_{SLP4}		SL4 (ILRCO on: APB=AHB=32KHz) with Low Power SLEEP mode		38.8		uA
I_{STP0}	STOP mode operating current (LVR/BOD0/BOD1 disabled)	ST0 (ILRCO off)		3.2		uA
I_{STP0LT}		ST0 (ILRCO off), LDO lowest power		1.05		uA
I_{STP1}		ST1 (IWDT Enable, ILRCO=32KHz)		4.5		uA
I_{STP2}		ST2 (RTC Enable, ILRCO=32KHz)		4.5		uA
	Current Consumption (VDD=3.3V)					
I_{OP1}	ON(normal) mode operating current	TL1 (APB=AHB=32KHz) dhrystone		0.11		mA
I_{OP2}		TL2 (APB=AHB=12MHz) dhrystone		2.52		mA
I_{OP3}		TL3 (APB=AHB=24MHz) dhrystone + IP		7.4		mA
I_{OP4}		TL4 (APB=AHB=24MHz - XTAL) dhrystone + IP		7.4		mA
I_{OP5}		TL5 (APB=AHB=24MHz - EXTCK) dhrystone + IP		7.0		mA
I_{OP6}		TL6 (APB=AHB=48MHz) dhrystone + all IP		13.3		mA
I_{SLP0}	SLEEP mode operating current (IWDT Enable)	SL0 (ILRCO on: IWDT Disable, APB=AHB=32KHz)		106		uA
I_{SLP1}		SL1 (IHRCO on: APB/AHB=6MHz/3MHz)		997		uA
I_{SLP2}		SL2 (IHRCO on: APB=AHB=12MHz)		1278		uA

I_{SLP3}		SL3 (XTAL=12MHz: APB/AHB=6MHz/3MHz)		950		uA
I_{SLP4}		SL4 (ILRCO on: APB=AHB=32KHz) with Low Power SLEEP mode		36.8		uA
I_{STP0}	STOP mode operating current (LVR/BOD0/BOD1 disabled)	ST0 (ILRCO off)		2.4		uA
I_{STP0LT}		ST0 (ILRCO off), LDO lowest power		0.5		uA
I_{STP1}		ST1 (IWDT Enable, ILRCO=32KHz)		3.6		uA
I_{STP2}		ST2 (RTC Enable, ILRCO=32KHz)		3.6		uA
Wakeup Time						
t_{WK_SLP0}	Wakeup from SLEEP mode (Normal SLEEP mode)	IHRCO/ILRCO on, wakeup by RTC event (RTC Clock= CK_APB= CK_IHRCO)		5	6	T_{PC}
t_{WK_SLP1}	Wakeup from SLEEP mode (Low Power SLEEP mode)	IHRCO/ILRCO on, wakeup by RTC event (RTC Clock= CK_APB= CK_IHRCO)	40			us
t_{WK_STP0}	Wakeup from STOP mode	ILRCO on, wakeup by RTC event	16	20		us
BOD Characteristics						
V_{LVR}	LVR detection level (VCAP)	TA = -40℃ to +105℃		1.29		Volt
V_{BOD0}	BOD0 detection level (VCAP)	TA = -40℃ to +105℃	1.36		1.41	Volt
$I_{BOD0+LVR}$	BOD0 and LVR Current Consumption	TA = 25℃		2.1		uA
V_{BOD10}	BOD1 detection level for 2.0V	TA = -40℃ to +105℃	1.8(*1)	2.0	2.2(*1)	Volt
V_{BOD11}	BOD1 detection level for 2.4V	TA = -40℃ to +105℃	2.22(*1)	2.4	2.62(*1)	Volt
V_{BOD12}	BOD1 detection level for 3.7V	TA = -40℃ to +105℃	3.40	3.6	3.80	Volt
V_{BOD13}	BOD1 detection level for 4.2V	TA = -40℃ to +105℃	3.89(*1)	4.2	4.59(*1)	Volt
V_{BOD2}	BOD2 detection level for 1.7V	TA = -40℃ to +105℃	1.63	1.70	1.75	Volt
I_{BOD1}	BOD1/2 Current Consumption	TA = 25℃		8.0		uA
Operating Condition						
V_{PSR}	Power-on Slope Rate (VDD 10uf + 0.1uf, VCAP 4.7uf + 0.1uf)	TA = -40℃ to +105℃	0.05		2.5	V/ms
V_{OP1}	CPU Operating Speed 0–48MHz	TA = -40℃ to +105℃	2.7		5.5	Volt
V_{OP2}	CPU Operating Speed 0–12MHz	TA = -40℃ to +105℃	1.8		5.5	Volt

(*1) Data based on characterization results, not tested in production.

T_{PC}: APB clock cycle time, IP: internal peripheral modules, **all IP**: all test modules

TL3 ~ TL6: Measure current with IO toggle, **SL4**: Refer the wakeup time t_{WK_SLP1} as the low power SLEEP mode

Table 8-4. Current Measurement Condition Level Definition Table

Chip Power State	ON Mode						SLEEP Mode					STOP Mode			
Test Level	TL1	TL2	TL3	TL4	TL5	TL6	SL0	SL1	SL2	SL3	SL4	ST0_LT	ST0	ST1	ST2
Symbol	I_{OP1}	I_{OP2}	I_{OP3}	I_{OP4}	I_{OP5}	I_{OP6}	I_{SLP0}	I_{SLP1}	I_{SLP2}	I_{SLP3}	I_{SLP4}	I_{STP0LT}	I_{STP0}	I_{STP1}	I_{STP2}
CPU State	Normal						Sleep					Deep Sleep			
CPU Code (*1)	dhrystone	dhrystone	dhrystone + normal code			dhrystone + heavy code	-	-	-	-	-	-	-	-	-
APB Clock	32KHz ILRCO	12MHz IHRCO	24MHz PLL/4	24MHz PLL/4	24MHz PLL/4	48MHz PLL/2	32KHz ILRCO	6MHz IHRCO/2	12MHz IHRCO	6MHz XTAL/2	32KHz ILRCO	-	-	32KHz ILRCO	32KHz ILRCO
AHB/CPU Clock	32KHz APB	12MHz APB	24MHz APB	24MHz APB	24MHz APB	48MHz APB	32KHz APB	3MHz APB/2	12MHz APB	3MHz APB/2	32KHz APB	-	-	32KHz APB	32KHz APB
ILRCO (32KHz)	V	V	V	V	V	V	V	V	V	V	V			V	V
IHRCO (12MHz)		V	V			V		V	V						
XTAL (12MHz)				Medium						Medium					
EXTCK (12MHz)					V										

PLL			V	V	V	V									
LDO (*2)	**Normal**						**Normal**					**Low Power**			
LVR	V	V	V	V	V	V	V	V	V	V	V				
BOD0	V	V	V	V	V	V	V	V	V	V	V				
BOD1			V	V	V	V									
SLEEP Mode (*3)							Normal	Normal	Normal	Normal	Low Power				
ADC0			CK_APB	CK_APB	CK_APB	CK_APB									
CMP			CK_APB	CK_APB	CK_APB	CK_APB		CK_APB	CK_APB	CK_APB					
RTC			CK_UT	CK_UT	CK_UT	CK_UT									CK_UT
IWDT	CK_ILRCO	CK_ILRCO	CK_ILRCO	CK_ILRCO	CK_ILRCO	CK_ILRCO		CK_ILRCO	CK_ILRCO	CK_ILRCO				CK_ILRCO	
WWDT			CK_APB	CK_APB	CK_APB	CK_APB									
TM00	CK_APB	CK_APB	CK_APB	CK_APB	CK_APB	CK_APB		CK_APB	CK_APB	CK_APB					
TM01						CK_APB									
TM10			CK_APB	CK_APB	CK_APB	CK_APB									
TM16						CK_APB									
TM20						CK_APB									
TM26						CK_APB									
TM36			CK_APB	CK_APB	CK_APB	CK_APB									
I2C0			CK_APB	CK_APB	CK_APB	CK_APB									
I2C1						CK_APB									
URT0			CK_APB	CK_APB	CK_APB	CK_APB									
URT1						CK_APB									
URT2						CK_APB									
URT4						CK_APB									
URT5						CK_APB									
URT6						CK_APB									
URT7						CK_APB									
SPI0						CK_APB									
GPL						CK_APB									
CAN						CK_APB									
OPA						CK_APB									
LCD						CK_APB									
IO Pins	all Push-Pull Low		IO Toggle				all Push-Pull Low					all Push-Pull Low			

Note: (*1) **[CPU Code]**
dhrystone: CPU runs "Dhrystone" benchmarks code.
normal code: Set CK_APB and CK_AHB frequency by table. The module clock divider can be /4, /8 or others.
heavy code: 1. Set CK_APB and CK_AHB frequency by table. The module clock set the highest frequency (module clock DIV=/2).
2. Let the module operates as busy as possible and fills full data through the buffer. (EX: transfer 4 bytes for one transaction)

(*2) Normal: PW_LDO_ON=0, Low Power: PW_LDO_STP=1

(*3) Normal: PW_WKSLP_MDS=0, Low Power: PW_WKSLP_MDS=1

8.4. IO Characteristics

Table 8-5. IO Characteristics

VSS=0V, TA = 25 °C and execute NOP for each CPU cycle (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	Input High voltage	Except RSTN,XIN pins	0.6			VDD
V_{IH_XOSC}	Input High voltage (XIN)	XIN pin GPIO mode	0.75			VDD
V_{IH_RST}	Input High voltage (RSTN)	RSTN pin reset/GPIO mode	0.75			VDD
V_{IL}	Input Low voltage	Except RSTN,XIN pins			0.15	VDD
V_{IL_XOSC}	Input Low voltage (XIN)	XIN pin GPIO mode			0.2	VDD
V_{IL_RST}	Input Low voltage (RSTN)	RSTN pin reset/GPIO mode			0.2	VDD
	VDD=5.0V					
I_{IH}	Input High Leakage current	V_{PIN} = VDD		0.03	0.1	uA

I_{IL}	Input Low Leakage current	V_{PIN} = 0.4V		0.03	0.1	uA
I_{H2L}	Logic 1 to 0 input transition current (quasi-bidirectional or input mode with on-chip pull-up resistor)	V_{PIN} = 2.2V (V_{IH} voltage)		254	500	uA
I_{OH1}	Output High current (push-pull output mode & Full level)	VDD=5.0V, V_{PIN} = 2.4V		36.9		mA
I_{OH2}	Output High current (push-pull output mode & 1/2 level)	VDD=5.0V, V_{PIN} = 2.4V		19.0		mA
I_{OH3}	Output High current (push-pull output mode & 1/4 level)	VDD=5.0V, V_{PIN} = 2.4V		9.7		mA
I_{OH4}	Output High current (push-pull output mode & 1/8 level)	VDD=5.0V, V_{PIN} = 2.4V		4.9		mA
I_{OL1}	Output Low current(Full level)	VDD=5.0V, V_{PIN} = 0.4V		31.9		mA
I_{OL2}	Output Low current(1/2 level)	VDD=5.0V, V_{PIN} = 0.4V		16.2		mA
I_{OL3}	Output Low current(1/4 level)	VDD=5.0V, V_{PIN} = 0.4V		8.2		mA
I_{OL4}	Output Low current(1/8 level)	VDD=5.0V, V_{PIN} = 0.4V		4.2		mA
R_{VWeak}	IO pin very weak pull-high resistance			250		Kohm
R_{PU}	IO pin pull-high resistance	Except RSTN		12		Kohm
R_{RST}	Internal reset pull-high resistance	RSTN pin		260		Kohm
TR1	IO rising time (Normal mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		7.2		ns
TR2	IO rising time (Normal mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		22.3		ns
TR3	IO rising time (High speed mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		5.3		ns
TR4	IO rising time (High speed mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		21.5		ns
TR5	IO rising time (XOUT GPIO mode)	C load=30pF		5.3		ns
TR6	IO rising time (XIN GPIO mode)	C load=30pF		5.3		ns
TR7	IO rising time (RSTIN GPIO mode)	C load=30pF		6.0		ns
TF1	IO falling time (Normal mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		5.1		ns
TF2	IO falling time (Normal mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		8.4		ns
TF3	IO falling time (High speed mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		3.2		ns
TF4	IO falling time (High speed mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		7.5		ns
TF5	IO falling time (XOUT GPIO mode)	C load=30pF		3.1		ns
TF6	IO falling time (XIN GPIO mode)	C load=30pF		3.1		ns

TF7	IO falling time (RSTIN GPIO mode)	C load=30pF		**3.5**		**ns**
	VDD=3.3V					
I_{IH}	Input High Leakage current	V_{PIN} = VDD		**0.03**	**0.1**	**uA**
I_{IL}	Input Low Leakage current	V_{PIN} = 0.4V		**0.04**	**0.1**	**uA**
I_{H2L}	Logic 1 to 0 input transition current (quasi-bidirectional or input mode with on-chip pull-up resistor)	V_{PIN} = 1.6V (V_{IH} voltage)		**112**	**150**	**uA**
I_{OH1}	Output High current (push-pull output mode & Full level)	VDD=3.3V, V_{PIN} = 2.4V		**12.6**		**mA**
I_{OH2}	Output High current (push-pull output mode & 1/2 level)	VDD=3.3V, V_{PIN} = 2.4V		**6.5**		**mA**
I_{OH3}	Output High current (push-pull output mode & 1/4 level)	VDD=3.3V, V_{PIN} = 2.4V		**3.3**		**mA**
I_{OH4}	Output High current (push-pull output mode & 1/8 level)	VDD=3.3V, V_{PIN} = 2.4V		**1.7**		**mA**
I_{OL1}	Output Low current(Full level)	VDD=3.3V, V_{PIN} = 0.4V		**23.0**		**mA**
I_{OL2}	Output Low current(1/2 level)	VDD=3.3V, V_{PIN} = 0.4V		**11.5**		**mA**
I_{OL3}	Output Low current(1/4 level)	VDD=3.3V, V_{PIN} = 0.4V		**5.9**		**mA**
I_{OL4}	Output Low current(1/8 level)	VDD=3.3V, V_{PIN} = 0.4V		**3.0**		**mA**
R_{VWeak}	IO pin very weak pull-high resistance			**420**		**Kohm**
R_{PU}	IO pin pull-high resistance	Except RSTN		**16.2**		**Kohm**
R_{RST}	Internal reset pull-high resistance	RSTN pin		**420**		**Kohm**
TR1	IO rising time (Normal mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		**10.5**		**ns**
TR2	IO rising time (Normal mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**29.5**		**ns**
TR3	IO rising time (High speed mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		**7.3**		**ns**
TR4	IO rising time (High speed mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**28.1**		**ns**
TR5	IO rising time (XOUT GPIO mode)	C load=30pF		**7.0**		**ns**
TR6	IO rising time (XIN GPIO mode)	C load=30pF		**7.4**		**ns**
TR7	IO rising time (RSTIN GPIO mode)	C load=30pF		**7.7**		**ns**
TF1	IO falling time (Normal mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		**6.3**		**ns**
TF2	IO falling time (Normal mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**10.6**		**ns**
TF3	IO falling time (High speed mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		**3.5**		**ns**
TF4	IO falling time (High speed mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**9.5**		**ns**

TF5	IO falling time (XOUT GPIO mode)	C load=30pF		**3.6**		**ns**
TF6	IO falling time (XIN GPIO mode)	C load=30pF		**3.7**		**ns**
TF7	IO falling time (RSTIN GPIO mode)	C load=30pF		**4.0**		**ns**
	VDD=1.8V					
I_{IH}	Input High Leakage current	V_{PIN} = VDD		**0.01**	**0.1**	**uA**
I_{IL}	Input Low Leakage current	V_{PIN} = 0.4V		**0.03**	**0.1**	**uA**
I_{H2L}	Logic 1 to 0 input transition current (quasi-bidirectional or input mode with on-chip pull-up resistor)	V_{PIN} = 1.1V (V_{IH} voltage)		**26**	**50**	**uA**
I_{OH1}	Output High current (push-pull output mode & Full level)	VDD=1.8V, V_{PIN} = 1.4V		**3.3**		**mA**
I_{OH2}	Output High current (push-pull output mode & 1/2 level)	VDD=1.8V, V_{PIN} = 1.4V		**1.7**		**mA**
I_{OH3}	Output High current (push-pull output mode & 1/4 level)	VDD=1.8V, V_{PIN} = 1.4V		**0.9**		**mA**
I_{OH4}	Output High current (push-pull output mode & 1/8 level)	VDD=1.8V, V_{PIN} = 1.4V		**0.5**		**mA**
I_{OL1}	Output Low current(Full level)	VDD=1.8V, V_{PIN} = 0.4V		**11.2**		**mA**
I_{OL2}	Output Low current(1/2 level)	VDD=1.8V, V_{PIN} = 0.4V		**5.6**		**mA**
I_{OL3}	Output Low current(1/4 level)	VDD=1.8V, V_{PIN} = 0.4V		**2.9**		**mA**
I_{OL4}	Output Low current(1/8 level)	VDD=1.8V, V_{PIN} = 0.4V		**1.5**		**mA**
R_{VWeak}	IO pin very weak pull-high resistance			**1080**		**Kohm**
R_{PU}	IO pin pull-high resistance	Except RSTN		**65**		**Kohm**
R_{RST}	Internal reset pull-high resistance	RSTN pin		**1100**		**Kohm**
TR1	IO rising time (Normal mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		**19.1**		**ns**
TR2	IO rising time (Normal mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**53.0**		**ns**
TR3	IO rising time (High speed mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		**13.6**		**ns**
TR4	IO rising time (High speed mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**50.9**		**ns**
TR5	IO rising time (XOUT GPIO mode)	C load=30pF		**14.1**		**ns**
TR6	IO rising time (XIN GPIO mode)	C load=30pF		**13.3**		**ns**
TR7	IO rising time (RSTIN GPIO mode)	C load=30pF		**13.5**		**ns**
TF1	IO falling time (Normal mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		**13.5**		**ns**
TF2	IO falling time (Normal mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**20.5**		**ns**
TF3	IO falling time (High speed mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		**5.4**		**ns**

TF4	IO falling time (High speed mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**16.6**		**ns**
TF5	IO falling time (XOUT GPIO mode)	C load=30pF		**6.1**		**ns**
TF6	IO falling time (XIN GPIO mode)	C load=30pF		**5.6**		**ns**
TF7	IO falling time (RSTIN GPIO mode)	C load=30pF		**6.0**		**ns**

8.5. External Clock Characteristics

Table 8-6. External Clock Characteristics

VDD=1.8V ~ 5.5V, VSS=0V, TA = -40°C ~ +105°C (unless otherwise specified)

Symbol	Parameter	Conditions	Crystal		External Clock		Unit
			Min	Max	Min	Max	
f_{XOSC}	Oscillator Frequency	VDD = 1.8V ~ 5.5V	**4**	**25**		**36**	**MHz**
t_{XOSC}	Clock Period		**40**		**27.7**		**ns**
t_{H_XOSC}	High Time		**0.4**	**0.6**	**0.4**	**0.6**	**txosc**
t_{L_XOSC}	Low Time		**0.4**	**0.6**	**0.4**	**0.6**	**txosc**
t_{r_XOSC}	Rise Time					**7**	**ns**
t_{f_XOSC}	Fall Time					**7**	**ns**
$t_{\_START12M}$	Start-up Time	Xtal = 12MHz, CL = 20pF		**1**			**ms**
$t_{\_START32K}$	Start-up Time	Xtal = 32KHz, CL = 12.5pF		**0.8**			**s**
$R_{\_FB12M}$	Feedback resistor value of crystal buffer	Xtal = 12MHz, CL = 20pF	**132**	**140**			**KΩ**

8.6. PLL Characteristics

Table 8-7. PLL Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25°C (unless otherwise specified)

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Voltage (VCAP)		**1.35**	**1.50**	**1.65**	**Volt**
Input Clock Frequency Range	TA = -40℃ to +105℃	**4.0 (*1)**		**9.0 (*1)**	**MHz**
Output Clock Frequency Range	TA = -40℃ to +105℃	**32**		**144**	**MHz**
PLL Locking Time	TA = +25℃		**19.0**		**us**
PLL Current Consumption	VCO frequency = 144MHz		**0.7**		**mA**
PLL Cycle-to-cycle(Peak-Peak) Jitter	TA = +25℃		**650**	**1200**	**ps**

(*1) Data guaranteed by design, not tested in production.

(*2) Data based on characterization results, not tested in production.

8.7. IHRCO Characteristics

Table 8-8. IHRCO Characteristics

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Voltage		**1.8**	**5.0**	**5.5**	**Volt**
IHRCO0 Frequency	TA = +25℃		**12**		**MHz**
IHRCO1 Frequency	TA = +25℃		**11.0592**		**MHz**
IHRCO0 Frequency Deviation	TA = +25℃	**-1.0**		**+1.0**	**%**
(factory calibrated) (VCAP= 1.5V~1.65V)	TA = -40℃ to +105℃	**-5.0(*1)**		**+3.0(*1)**	**%**

IHRCO1 Frequency Deviation	TA = +25℃	-1.0		+1.0	%
(factory calibrated) (VCAP= 1.5V~1.65V)	TA = -40℃ to +105℃	-5.0(*1)		+3.0(*1)	%
IHRCO Start-up Time	TA = 25℃			5(*1)	us
IHRCO Current Consumption	TA = +25℃, VDD=5.0V		0.45		mA

(*1) Data based on characterization results, not tested in production.

8.8. ILRCO Characteristics

Table 8-9. ILRCO Characteristics

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Voltage		1.8	5.0	5.5	Volt
ILRCO Frequency	TA = +25℃		32		KHz
ILRCO Frequency Deviation	TA = +25℃, VDD=5.0V	-4		+4	%
(factory calibrated)	TA = -40℃ to +105℃	-30(*1)		+20(*1)	%
ILRCO Current Consumption	TA = +25℃, VDD=5.0V			2	uA
Output Duty	TA = +25℃, VDD=5.0V	45	50	55	%

(1) Data based on characterization results, not tested in production.

8.9. LDO Characteristics

Table 8-10. LDO Characteristics

VDD=5.0V±10%, VSS=0V, TA = -40℃ ~ +105 °C

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
VDD	Supply Voltage	Normal Mode, IOUT=20mA	**1.8**	**5.0**	**5.5**	**V**
General						
VCAP	LDO Output Voltage (VCAP pin)	ON(Normal) mode		**1.55**		**Volt**
		Low power mode, IOUT=100uA, VDD=1.8V~5.5V, TA = -40 ℃ ~ +105 °C		**1.35**		**Volt**
		Lowest power mode, IOUT=10uA, VDD=1.8V~5.5V, TA = -40℃ ~ +105 °C		**0.98**		**Volt**
IQ	Current	VDD=1.7V~5.0V, Temp.= 25℃		**45.6**		**uA**
		VDD=1.7V~5.0V, Temp.= -40℃ ~ +105℃		**60(*1)**		**uA**
VDROP	Dropout Voltage (VDD-VCAP)	IOUT=10mA, VDD=2.0V~5.5V (VCAP =1.55V +/-5%)	**500**			**mV**
		IOUT=10mA, VDD=1.9V~5.5V (VCAP =1.55V +/-5%)	**400**			**mV**
		IOUT=10mA, VDD=1.8V~5.5V (VCAP =1.55V +/-5%)	**310**			**mV**
IOUT	Max output current	VDD=5.0V (VCAP voltage variation < ±5%)	**50**			**mA**
		VDD=3.6V (VCAP voltage variation < ±5%)	**50**			**mA**
		VDD=2.0V (VCAP voltage variation < ±5%)	**40**			**mA**
		VDD=1.8V (VCAP voltage variation < ±5%)	**20**			**mA**

(1) Data based on characterization results, not tested in production.

8.10. Flash Characteristics

Table 8-11. Flash Characteristics

VDD=5.0V±10%, VSS=0V, TA = -40℃ ~ +105 °C

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Voltage		**1.8**		**5.5**	**Volt**
Flash Write (Erase/Program) Voltage		**1.8**		**5.5**	**Volt**
Flash Erase/Program Cycle		**20000**			**Times**
Flash Data Retention	TA = +25℃	**100**			**Year**
Flash Chip Erase Time		**20**		**40**	**ms**
Flash Page Erase Time		**4**		**5**	**ms**
Flash Program Time	Program one 32-bit			**50**	**μs**

8.11. ADC Characteristics

Table 8-12. ADC Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C, C_{LOAD}=10pF, Gain=x1 (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
	Supply Range					
VDDA	Analog Supply Voltage		2.4	5.0	5.5	Volt
I_{ADC_ON}	Operation Current - normal			1200		uA
I_{ADC_OFF}	Operation Current - power-down			0.1		uA
	ADC Static Parameters					
Bits	Resolution				12	bits
INL	Integral nonlinearity (INL)	VREF = 5V, VDD = 5V, 1.5Msps Conversion Rate (sampling clock = 36 MHz/24 clocks)		±3		LSB
INL	Integral nonlinearity (INL)	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 24 MHz/24 clocks)		±3		LSB
INL	Integral nonlinearity (INL)	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 30 MHz/30 clocks)		±3		LSB
DNL	Differential nonlinearity (DNL)	VREF = 5V, VDD = 5V, 1.5Msps Conversion Rate (sampling clock = 36 MHz/24 clocks)	-1	3.2		LSB
DNL	Differential nonlinearity (DNL)	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 24 MHz/24 clocks)	-1	2.5		LSB
DNL	Differential nonlinearity (DNL)	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 30 MHz/30 clocks)	-1	2.8		LSB
E_{OFFSET}	Offset error	VREF = 5V, VDD = 5V, 1.5Msps Conversion Rate (sampling clock = 36 MHz/24 clocks)		±2		LSB
E_{OFFSET}	Offset error	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 24 MHz/24 clocks)		±2		LSB
E_{OFFSET}	Offset error	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 30 MHz/30 clocks)		±2		LSB
E_{FS}	Full scale error	VREF = 5V, VDD = 5V,		±5		LSB

		1.5Msps Conversion Rate (sampling clock = 36 MHz/24 clocks)				
E_{FS}	Full scale error	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 24 MHz/24 clocks)		±5		LSB
E_{FS}	Full scale error	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 30 MHz/30 clocks)		±5		LSB
	ADC Input and DC Characters					
V_{AIN}	ADC input voltage range (Single Ended)	gain = 1.0	0		Vref	Volt
C_{LOAD}	Input capacitance			4.3		pF
V_{XREF}	External ADC reference voltage		2.4		VDDA	Volt
VDD_{IREF}	Supply Voltage range for V_{IREF}		2.7		5.5	Volt
V_{IREF}	Internal ADC reference voltage	25 °C		2.40		Volt
	Internal ADC reference voltage spread over the temperature range	-40 °C < < 105 °C V_{IREF} =2.40V at 25°C		30		mV
V_{BUF}	Internal VBUF reference voltage	25 °C		1.40		Volt
	Internal VBUF reference voltage spread over the temperature range	-40 °C < < 105 °C V_{BUF} =1.40V at 25°C		30		mV
TADEN	ADC enable time			5		us
	ADC Conversion Parameters					
Fs	Sampling clock	24 clocks/One Conversion			36	MHz
		30 clocks/One Conversion			45	MHz
F_{Conv}	Conversion rate	VDDA = 5.5 ~ 2.4 V			1500	Ksps
T_{Conv}	Conversion time in conversion clock (not including acquisition time)	ADC0_CONV_TIME=0		24		clocks
		ADC0_CONV_TIME=1		30		clocks

8.12. ADC PGA Characteristics

Table 8-13. ADC PGA Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
	Supply Range					
VDDA	Analog Supply Voltage		2.4	5.0	5.5	Volt
	DC Characteristics					
V_{OS}	input offset voltage	With Calibration Gain=x1		±0.6	±1.0	mV
IQ	Quiescent current	VOUT=2V,Normal power mode	0.7	0.75	0.8	mA
		VOUT=2V,Low power mode	0.3	0.32	0.35	mA
V_{CM}	Common mode input voltage range (Normal mode & VSSA)	Gain=1, Normal mode		0.011		V
		Gain=2, Normal mode		0.020		V
		Gain=4, Normal mode		0.020		V
		Gain=8, Normal mode		0.030		V
		Gain=16, Normal mode		0.026		V

		Gain=32, 64, 128, Normal mode		0.012 0.005 0.003		V
V_{CM}	Common mode input voltage range (Normal mode & VDDA)	Gain=1, Normal mode		4.500		V
		Gain=2, Normal mode		2.490		V
		Gain=4, Normal mode		1.240		V
		Gain=8, Normal mode		0.620		V
		Gain=16, Normal mode		0.276		V
		Gain=32, 64, 128, Normal mode		0.154 0.076 0.037		V
V_{CM}	Common mode input voltage range (Low power mode & VSSA)	Gain=1, Low power mode		0.025		V
		Gain=2, Low power mode		0.033		V
		Gain=4, Low power mode		0.028		V
		Gain=8, Low power mode		0.028		V
		Gain=16, Low power mode		0.070		V
		Gain=32, 64, 128, Low power mode		0.032 0.014 0.013		V
V_{CM}	Common mode input voltage range (Low power mode & VDDA)	Gain=1, Low power mode		4.500		V
		Gain=2, Low power mode		2.490		V
		Gain=4, Low power mode		1.240		V
		Gain=8, Low power mode		0.620		V
		Gain=16, Low power mode		0.278		V
		Gain=32, 64, 128, Low power mode		0.154 0.077 0.038		V
	AC Characteristics					
SR	Slew rate	CLOAD =10pF, Gain=32,Normal mode		4.310		V/us
		CLOAD =10pF, Gain=32,Low power mode		1.780		V/us
BW	Bandwidth	CLOAD =10pF, Gain=1,Normal mode		2.2		MHz
		CLOAD =10pF, Gain=1,Low power mode		1.5		MHz
PSRR	power supply rejection ratio	VDD=2.4~5.5V,Gain=16		-48.24		dB

(*1) Data guaranteed by design, not tested in production.

(*2) The UGF will be divided by the GAIN setting. (ex: Ideal UGF will be 10MHz/4 when PGA gain=4)

8.13. Analog Comparator Characteristics

Table 8-14. Analog Comparator Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
VDDA	Analog Supply Voltage	-40°C ~ +105°C	2.0	5.0	5.5	Volt
I_{COMP0}	Operation Current - CMP0	High response time without IVREF (*1)		10		uA
		High response time with IVREF (*1)		210		uA
		Low response time		2		uA
I_{COMP1}	Operation Current - CMP1	High response time without IVREF (*1)		10		uA
		High response time with IVREF (*1)		210		uA
		Low response time		2		uA
Analog Comparator Core						
V_{OS}	Input Offset Voltage			±15		mV
V_{CM}	Input Common Mode Voltage		50		VDDA-50	mV
V_{HYS}	Comparator hysteresis	Disable Hysteresis		0		mV
	Input voltage range 50mV ~ VDD-50mV	High response time		10		mV
		Low response time		10		mV
T_{RT}	Response time	High response time - Falling		250		ns
		High response time - Rising		230		ns
		Low response time - Falling		0.9		us
		Low response time – Rising		0.9		us
t_{PWON}	Power on Time (from power-down)	High response time		550		ns
		Low response time		15		us
RU	Unit Resistance			390		ohm

(*1) IVREF : Internal voltage reference circuit

8.14. Temperature Sensor Characteristics

Table 8-15. Temperature Sensor Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
VDDA	Analog Supply Voltage	calculate VREF	2.4	5.0	5.5	Volt
Temperature Conversion Parameters						
T_{RANG}	Temperature range		-40		125	°C
$Slope_{AVG}$	Linearity (curve slope)		2.5		2.79	mV/°C
V_0	Voltage at 0 °C (*1)	TA = 0℃ (± 5 °C)	690	725	760	mv
	Accuracy		-2.5	±2	3	°C
t_{START}	Startup time		20	25	30	ms
I_{TEMP_ON}	Operation current (Vref pin)		47	51	53	uA

(*1) Data based on characterization results, not tested in production.

8.15. Operational Amplifier Characteristics

Table 8-16. Operational Amplifier Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
VDDA	Analog Supply Voltage	-40°C ~ +105°C	2.0		5.5	Volt
OPA Characteristics						
I_Q	Quiescent current	V_{SENSE} =0mV, Normal Power mode		0.7		mA
		V_{SENSE} =0mV, Low Power mode		0.3		mA
V_{os}	Input offset voltage	Zeroed		±0.6	±1.0	mA
V_{CM}	Common mode input voltage range (Normal Power and VSSA)	-40°C~105°C, Normal Power mode Error Gain =±0.5%		0.26		V
		-40°C~105°C, Normal Power mode Error Gain =±1.0%		0.15		V
V_{CM}	Common mode input voltage range (Low Power and VSSA)	-40°C~105°C, Low Power mode Error Gain =±0.5%		0.30		V
		-40°C~105°C, Low Power mode Error Gain =±1.0%		0.20		V
V_{CM}	Common mode input voltage range (Normal Power and VDDA)	-40°C~105°C, Normal Power mode Error Gain =±0.5%		4.99		V
		-40°C~105°C, Normal Power mode Error Gain =±1.0%		4.99		V
V_{CM}	Common mode input voltage range (Low Power and VDDA)	-40°C~105°C, Low Power mode Error Gain =±0.5%		4.99		V
		-40°C~105°C, Low Power mode Error Gain =±1.0%		4.99		V
V_{OL}	Minimum output voltage	-40°C~105°C, Normal Power mode ,RLOAD=2K to VDD	0.03	0.05	0.07	V
		-40°C~105°C, Low Power mode ,RLOAD=2K to VDD	0.03	0.05	0.07	V
V_{OH}	Maximum output voltage	-40°C~105°C, Normal Power mode ,RLOAD=2K to VDD	4.90	4.93	4.94	V
		-40°C~105°C, Low Power mode ,RLOAD=2K to VDD	4.90	4.93	4.94	V
BW	Bandwidth	R_{LOAD} =2K, C_{LOAD} =100pF		13		MHz
SR	Slew rate	R_{LOAD} =2K, C_{LOAD} =100pF, rising time		10.0		V/us
		R_{LOAD} =2K, C_{LOAD} =100pF, falling time		-7.5		V/us
CMRR	common-mode rejection ratio			-66		dB
PSRR	power supply rejection ratio			-73		dB

8.16. LCD Characteristics

Table 8-17. LCD Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits	Unit

			Min	Typ	Max	
Supply Range						
VDDA	Analog Supply Voltage	-40°C ~ +105°C	**2.0**		**5.5**	**Volt**
VT_{EXT}	LCD external voltage (LCD_VT pin)		**1.8**		**5.5**	**Volt**
VT_0	LCD internal CP top level-0 voltage	LCD_VT_SEL=0		**2.36**		**Volt**
VT_{MAX}	LCD internal CP top maximum voltage			**3.40**		**Volt**
VT_{STEP}	LCD internal CP top step voltage	LCD_VT_SEL=0 ~ 14	**55**	**80**	**110**	**mV**
$V_{3/4}$	COM/SEG 3/4 VT	1/4 Bias		**3/4 VT**		**Volt**
$V_{2/4}$	COM/SEG 2/4 VT	1/4 Bias		**2/4 VT**		**Volt**
$V_{1/4}$	COM/SEG 1/4 VT	1/4 Bias		**1/4 VT**		**Volt**
$V_{2/3}$	COM/SEG 2/3 VT	1/3 Bias		**2/3 VLT**		**Volt**
$V_{1/3}$	COM/SEG 1/3 VT	1/3 Bias		**1/3 VLT**		**Volt**
$V_{1/2}$	COM/SEG 1/2 VT	1/2 Bias		**1/2 VLT**		**Volt**
C_{EXT_VT}	LCD_VT external capacitance			**0.1**		**uF**
C_{EXT_CP}	LCD_C1, LCD_C2 external capacitance			**10**		**nF**
I_{CP}	Internal charge pump current	VDD = 5.0V		**7.0**		**uA**
I_{LCD_CP}	Supply current from internal charge pump with internal high drive R-ladder (*1) LCD_VT=3.0V	VDD = 3.6V, low drive mode		**5.6**		**uA**
		VDD = 5.5V, low drive mode		**6.3**		**uA**
		VDD = 3.6V, high drive mode		**25.4**		**uA**
		VDD = 5.5V, high drive mode		**27.0**		**uA**
I_{LCD_AVDD}	Supply current from internal AVDD with internal high drive R-ladder (*1)	VDD = 2.6V		**9.9**		**uA**
		VDD = 3.0V		**11.1**		**uA**
		VDD = 3.3V		**12.1**		**uA**
		VDD = 3.6V		**13.1**		**uA**
		VDD = 5.5V		**19.0**		**uA**
I_{LCD_EXT}	Supply current from external LCD_VT with internal high drive R-ladder (*1)	VDD = 1.8V, LCD_VT=3.5		**0.92**		**uA**
		VDD = 3.3V, LCD_VT=3.5		**0.93**		**uA**
		VDD = 3.6V, LCD_VT=3.5		**0.85**		**uA**
		VDD = 4.0V, LCD_VT=3.5		**0.92**		**uA**
		VDD = 5.0V, LCD_VT=3.5		**0.95**		**uA**
		VDD = 5.5V, LCD_VT=3.5		**0.91**		**uA**
R_{LCD_INT}	Internal LCD resistor (R-ladder) value	Low drive		**6.0**		**MΩ**
		High drive		**290**		**KΩ**

(*1) LCD set to 1/8 duty, 1/4 bias, 60 Hz frame rate, all pixels active, type B waveform, no LCD pane loading.

8.17. UART Characteristics

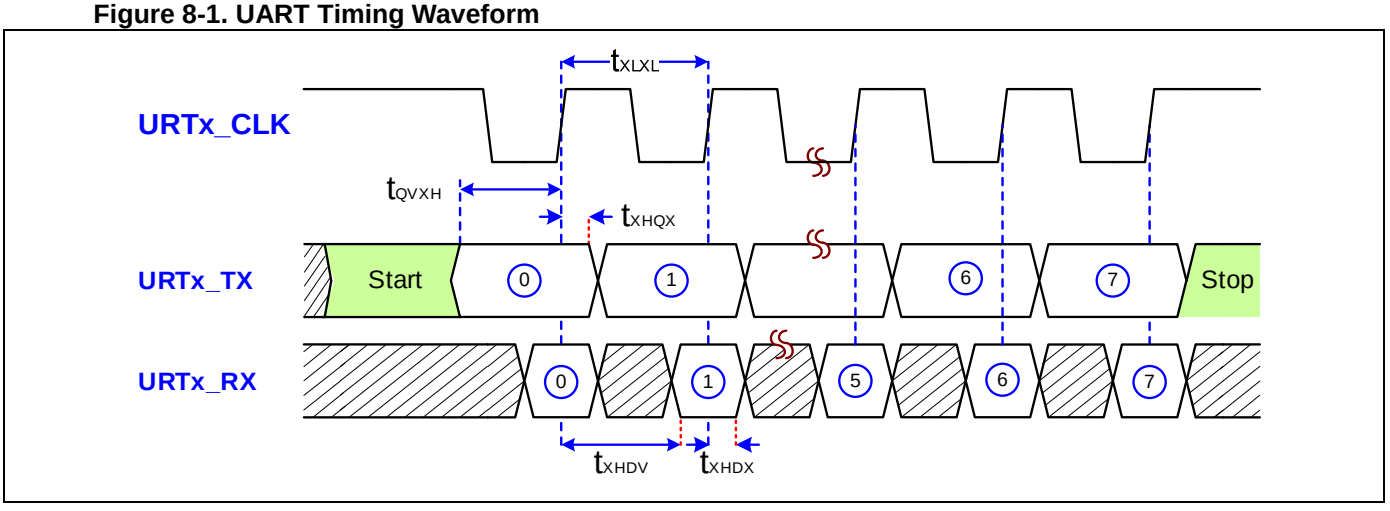
Table 8-18. UART Characteristics

VDD=5.0V±10%, VSS=0V, TA = -40°C ~ +105°C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
UART Mode						
f_{CK}	Serial Port Clock Frequency				6	MHz
t_{XLXL}	Serial Port Clock Cycle Time		4			T_{PC}
t_{QVXH}	Output Data Setup to Clock Rising Edge		T_{PC} -20			ns
t_{XHQX}	Output Data Hold after Clock Rising Edge		T_{PC} -10			ns
t_{XHDX}	Input Data Hold after Clock Rising Edge		0			ns
t_{XHDV}	Clock Rising Edge to Input Data Valid				T_{PC} -20	ns
SPI Master Mode (Synchronous Mode)						
f_{MCK}	SPI Output Clock Frequency	VDD=3.3V ~ 5.5V			22	MHz
		VDD=1.8V ~ 3.3V			16	MHz
t_{MCKH}	SPI Clock High Time		2			T_{PC}
t_{MCKL}	SPI Clock Low Time		2			T_{PC}
SPI Slave Mode (Synchronous Mode)						
f_{MCK}	SPI Input Clock Frequency	VDD=3.3V ~ 5.5V			14	MHz
		VDD=1.8V ~ 3.3V			12	MHz
t_{MCKH}	SPI Clock High Time		4			T_{PC}
t_{MCKL}	SPI Clock Low Time		4			T_{PC}

T_{PC} : APB clock or SYS clock cycle time

Figure 8-1. UART Timing Waveform



8.18. SPI Characteristics

Table 8-19. SPI Characteristics

VDD=5.0V±10%, VSS=0V, TA = -40°C ~ +105°C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Master Mode						
f_{MCK}	SPI Clock Frequency	VDD=3.3V ~ 5.5V			24	MHz
		VDD=1.8V ~ 3.3V			16	MHz
t_{MCKH}	SPI Clock High Time		2			T_{PC}
t_{MCKL}	SPI Clock Low Time		2			T_{PC}
t_{MIS}	D_{IN} Valid to SPI Clock Shift Edge		$2T_{PC}$ +20			ns
t_{MIH}	SPI Clock Shift Edge to D_{IN} Change		0			ns
t_{MOH}	SPI Clock Shift Edge to D_{OUT} Change				10	ns
Slave Mode						
f_{SCK}	SPI Clock Frequency	VDD=3.3V ~ 5.5V			16	MHz
		VDD=1.8V ~ 3.3V			12	MHz
t_{SE}	NSS Falling to First SPI Clock Edge		2			T_{PC}
t_{SD}	Last SPI Clock Edge to NSS Rising		2			T_{PC}
t_{SEZ}	NSS Falling to D_{OUT} Valid				4	T_{PC}
t_{SDZ}	NSS Rising to D_{OUT} High-Z				4	T_{PC}
t_{CKH}	SPI Clock High Time		3			T_{PC}
t_{CKL}	SPI Clock Low Time		3			T_{PC}
t_{SIS}	D_{IN} Valid to SPI Clock Sample Edge		2			T_{PC}
t_{SIH}	SPI Clock Sample Edge to D_{IN} Change		2			T_{PC}
t_{SOH}	SPI Clock Shift Edge to D_{OUT} Change				4	T_{PC}
t_{SLH}	Last SPI Clock Edge to D_{OUT} Change (CPHA = 1 only)		1		2	T_{PC}

T_{PC} : APB clock or SYS clock cycle time

D_{IN} : SPI input data signal

D_{OUT} : SPI output data signal

Figure 8-2. SPI Master Timing Waveform

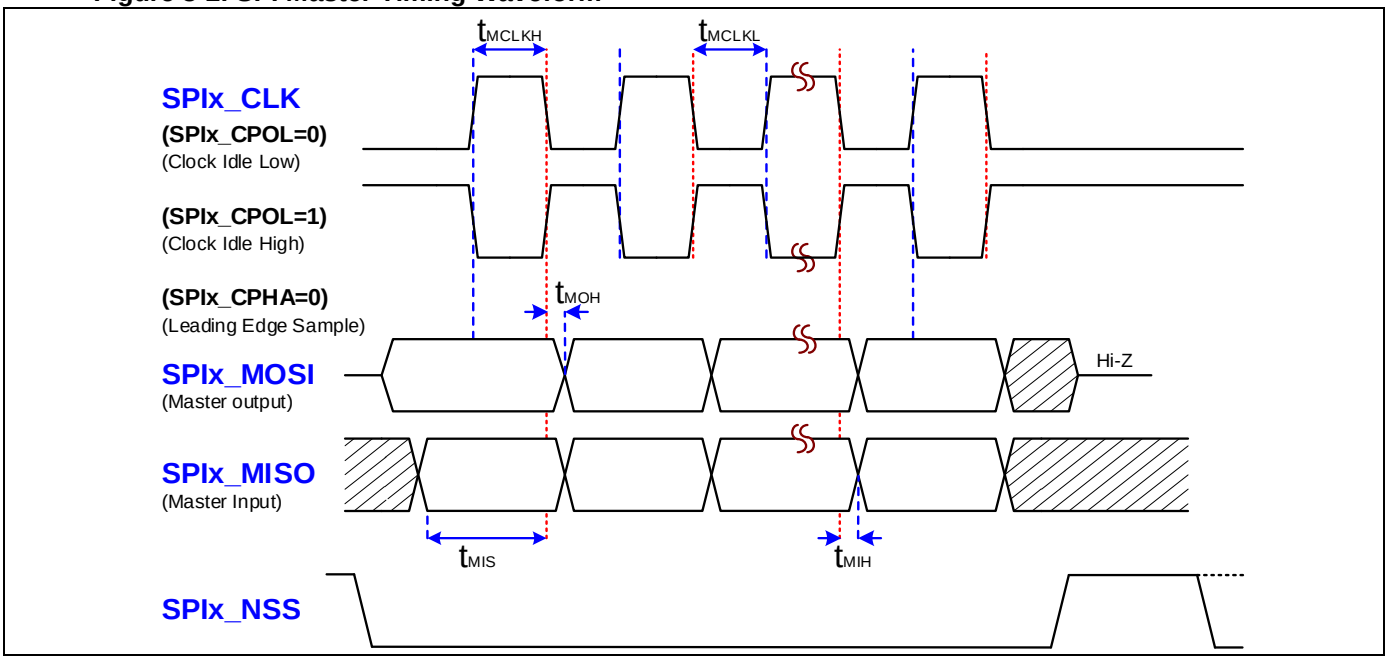
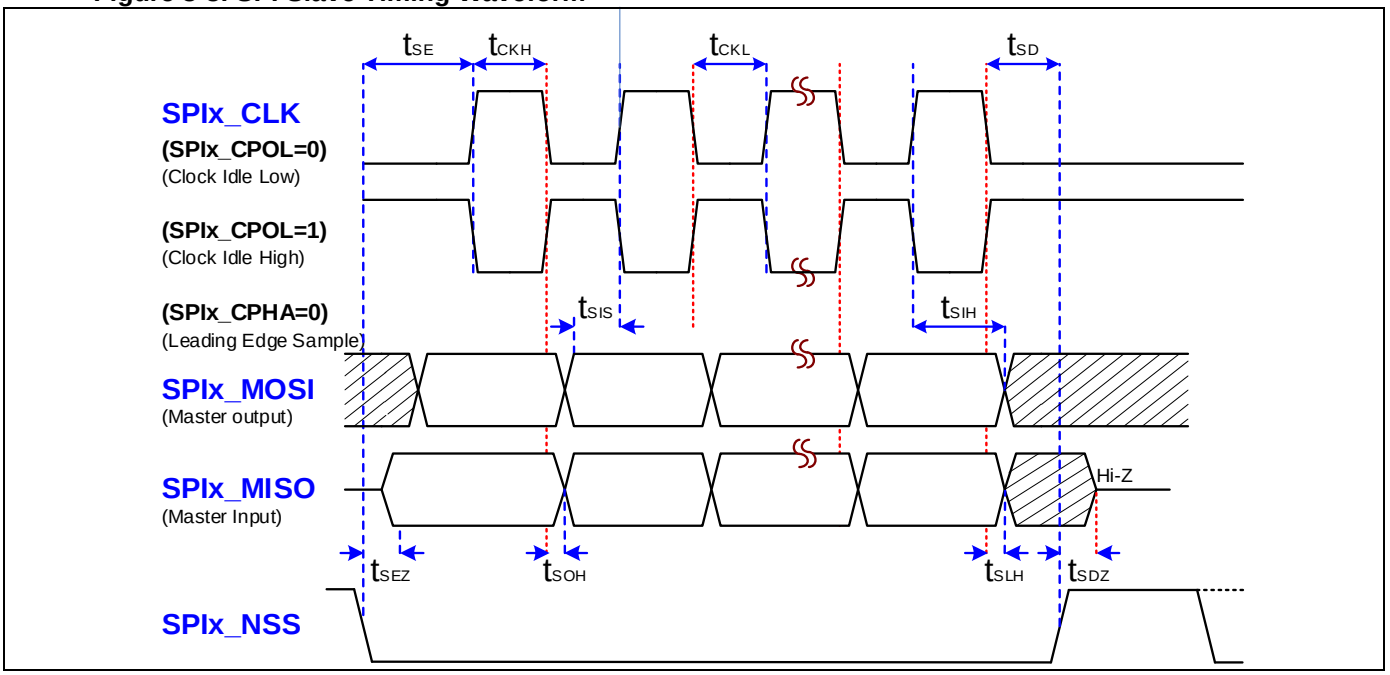


Figure 8-3. SPI Slave Timing Waveform



8.19. I2C Characteristics

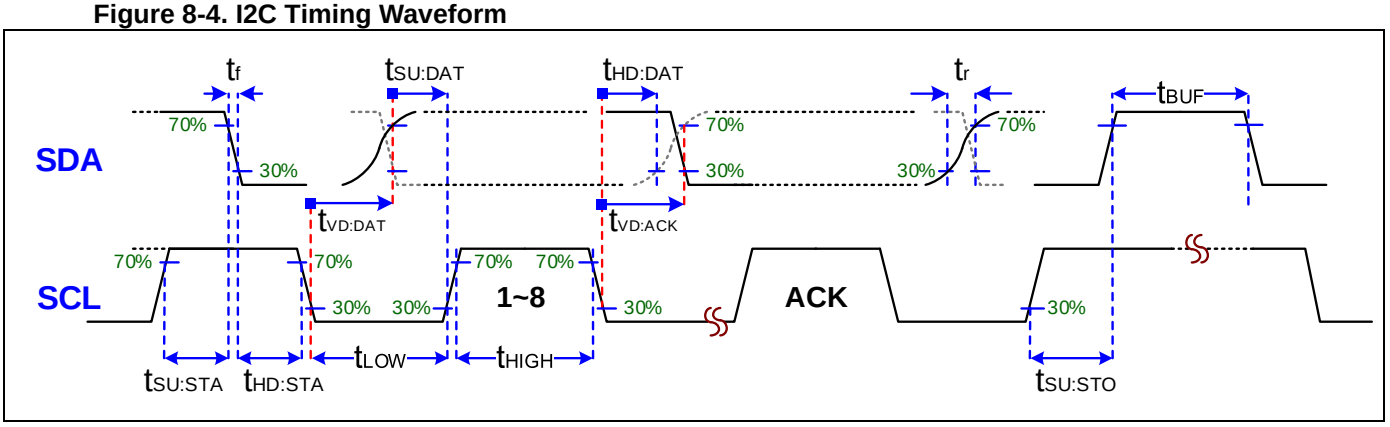
Table 8-20. I2C Characteristics

VDD=5.0V±10%, VSS=0V, TA = -40°C ~ +105°C (unless otherwise specified)

Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100	0	400	0	1000	KHz
t_{Low}	Low period of the SCL clock		4.7		1.3		0.5		us
t_{Low_M}	Low period of the SCL clock (Master Mode)		2		2		2		T_{PC}
t_{Low_S}	Low period of the SCL clock (Slave Mode)		4		4		4		T_{PC}
t_{High}	High period of the SCL clock		4.0		0.6		0.26		us
t_{High_M}	High period of the SCL clock (Master Mode)		3		3		3		T_{PC}
t_{High_S}	High period of the SCL clock (Slave Mode)		5		5		5		T_{PC}
$t_{HD;STA}$	Hold time for START condition		4.0		0.6		0.26		us
$t_{SU;STA}$	Setup time for START condition		4.7		0.6		0.26		us
$t_{HD;DAT}$	Data hold time		0		0		0		us
$t_{SU;DAT}$	Data setup time		250		100		50		ns
$t_{SU;STO}$	Setup time for STOP condition		4.0		0.6		0.26		us
t_{BUF}	Bus free time between a STOP and START		4.7		1.3		0.5		us
$t_{VD;DAT}$	Data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	Data valid acknowledge time			3.45		0.9		0.45	us
t_r	Rise time of both SDA and SCL signals			1000		300		120	ns
t_f	Fall time of both SDA and SCL signals			300	20x (VDD/5.5V)	300	20x (VDD/5.5V)	120	ns
C_i	Capacitive load for each IO pin			10		10		10	pF

T_{PC} : APB clock or SYS clock cycle time

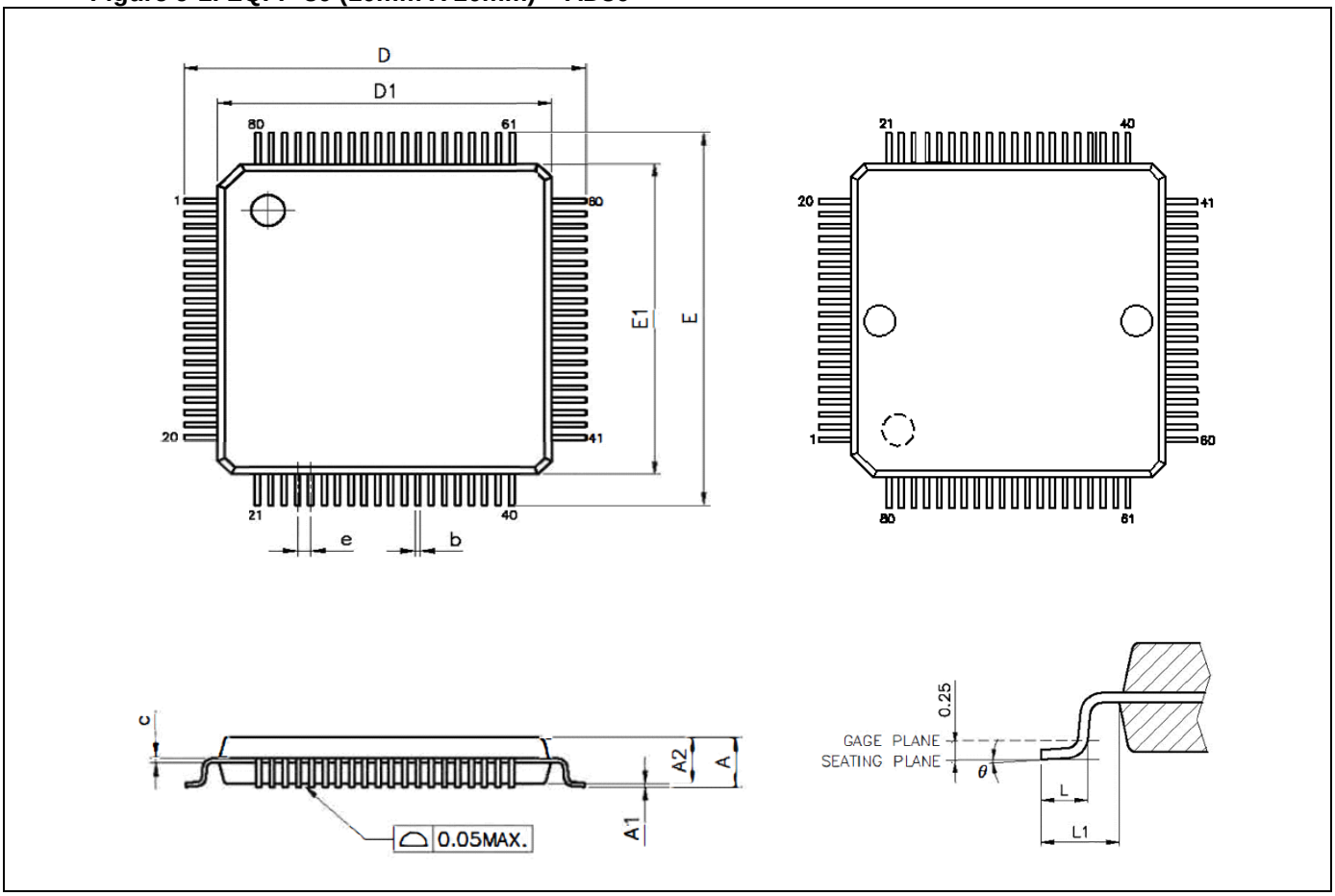
Figure 8-4. I2C Timing Waveform



9. Package Dimension

9.1. LQFP-80

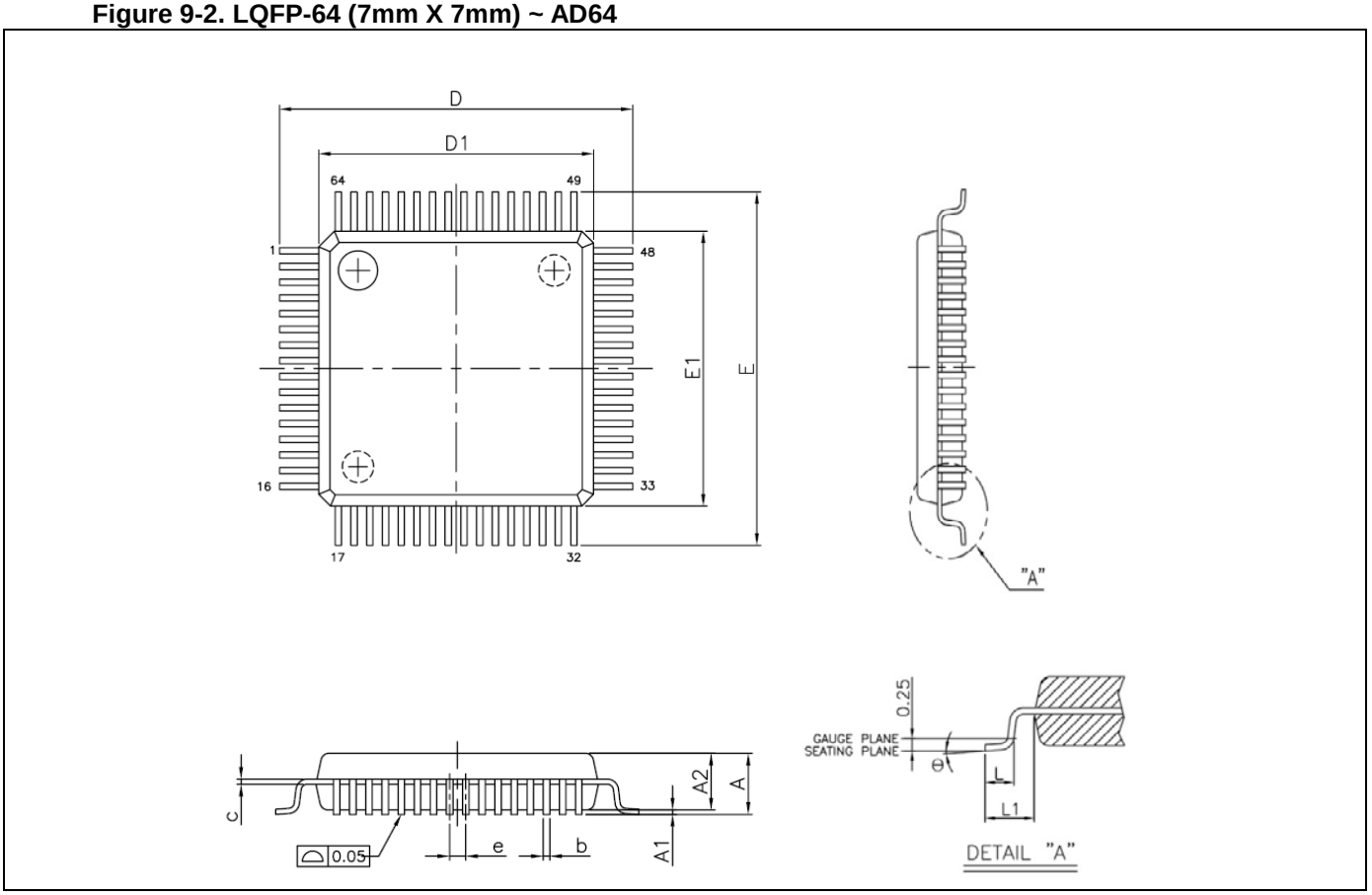
Figure 9-1. LQFP-80 (10mm X 10mm) ~ AD80



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	1.60	---	---	0.062
A1	0.05	---	0.15	0.001	---	0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
c	0.09	---	0.20	0.003	---	0.007
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.393 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.393 BSC		
e	0.40 BSC			0.015 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

9.2. LQFP-64

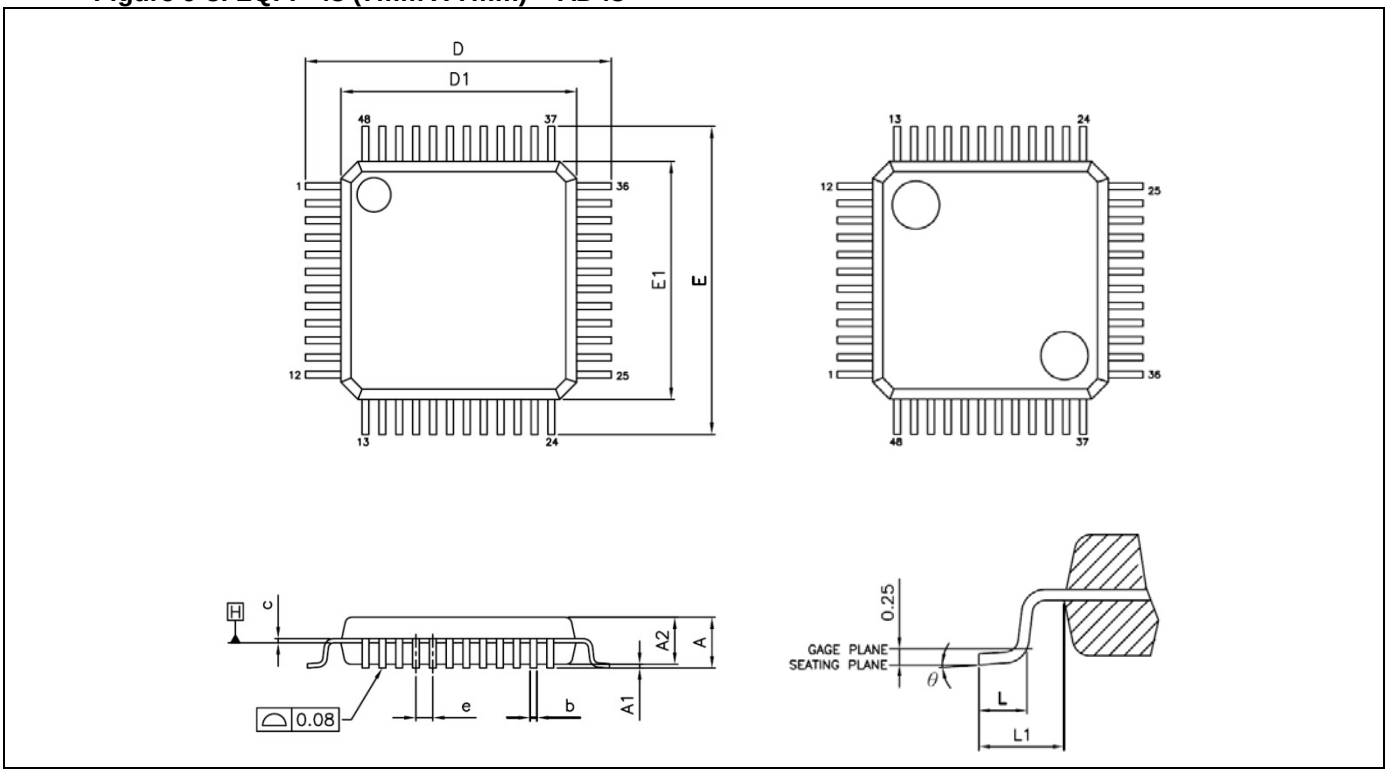
Figure 9-2. LQFP-64 (7mm X 7mm) ~ AD64



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	1.60	---	---	0.062
A1	0.05	---	0.15	0.001	---	0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
c	0.09	---	0.20	0.003	---	0.007
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.275 BSC		
e	0.40 BSC			0.015 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.275 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

9.3. LQFP-48

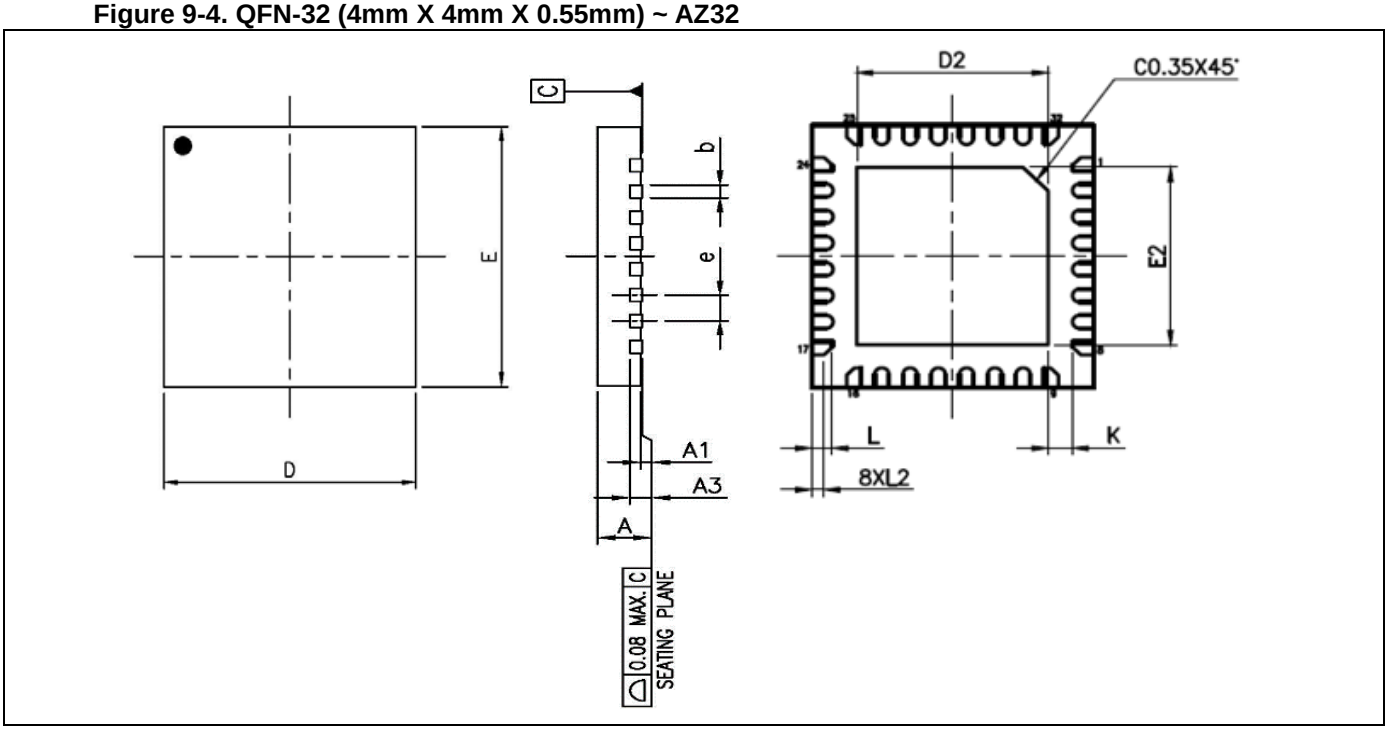
Figure 9-3. LQFP-48 (7mm X 7mm) ~ AD48



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	1.60	---	---	0.062
A1	0.05	---	0.15	0.001	---	0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.006	0.008	0.010
c	0.09	---	0.20	0.003	---	0.007
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.275 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.275 BSC		
e	0.50 BSC			0.019 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
ɵ	0˚	3.5˚	7˚	0˚	3.5˚	7˚

9.4. QFN-32

Figure 9-4. QFN-32 (4mm X 4mm X 0.55mm) ~ AZ32



Unit	mm			inch		
JEDEC	N/A			N/A		
PKG CODE	UQFN(W432)			UQFN(W432)		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.150 REF.			0.006 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	4.00 BSC			0.157 BSC		
E	4.00 BSC			0.157 BSC		
e	0.40 BSC			0.016 BSC		
L	0.25	0.30	0.35	0.010	0.012	0.014
L2	0.13	0.18	0.23	0.005	0.007	0.009
K	0.20	----	----	0.008	----	----
D2	----	----	2.75	----	----	0.108
E2	----	----	2.75	----	----	0.108

	LEAD FINISH		JEDEC CODE
PAD SIZE	Pure Tin	PPF	
122x12*MIL	V	X	N/A

10. Revision History

Revision V1.11 (2026_0804)		**Chapter**
1	Remove content for model MG32F02K	1, 2
2	Only the 128KB flash size specification is retained.	2
Revision V1.10 (2025_1127)		**Chapter**
1	Add QFN32 GPIO feature description.	Features
2	Update VDD 5.0V current consumption parameters in the table of “Table 10-1. DC Characteristics”.	8.3
3	Add VDD 3.3V current consumption parameters in the table of “Table 10-2. DC Characteristics”.	8.3
Revision V1.00 (2025_1022)		**Chapter**
1	Update CAN features.	Features
2	Remove MG32F02K064AZ32 QFN32 package in in “Order Information”.	2
3	Remove VBG_OUT in the tables of “Table 4-8. Analog Function Pin Table”.	4.4
4	Add SDT function descriptions in the section of “APX”.	6.12
5	Add “$\mathbf{I_{STP0LT}}$” parameter and update “$\mathbf{t_{WK\_STP0}}$” parameter in the table of “Table 8-3. DC Characteristics”.	8.3
6	Update the tables of “Table 10 3. DC Characteristics” and “Table 8-4. Current Measurement Condition Level Definition Table”.	8.3
7	Update “ILRCO Frequency Deviation” parameter in the tables of “Table 8-9. ILRCO Characteristics”.	8.8
8	Update “**IOUT**” parameter in the tables of “Table 8-10. LDO Characteristics”.	8.9
9	Update “$\mathbf{V_{OS}}$” and “$\mathbf{V_{CM}}$” parameters in the table of “Table 8-13. ADC PGA Characteristics”.	8.12
10	Update “$\mathbf{V_{OS}}$” and “**SR**” parameters in the table of “Table 8-16. Operational Amplifier Characteristics”.	8.15
11	Update the parameters in the table of “Table 10-4. LCD Characteristics”.	8.16
Revision V0.40 (2025_0219)		**Chapter**
1	Add QFN32 package in in “Order Information”, “Pin Description” and “Package Dimension” chapter.	2, 4, 9
2	Change OPA output OP0_P0 from PA6 to PA0 pin for new version chip in “Pin Description” chapter.	4.1 4.2 4.4
3	Add “Q” (Quasi-bidirectional) IO Type definition in the table of “Table 4-4. Abbreviations for pin definition”. Change “Default Type” of PC[0..3][7..14] from “Q” to “A” in the table of “Table 4-5. Pin Descriptions”.	4.2
4	Add R_{VWeak} parameter in the table of “Table 8-5. IO Characteristics”.	8.4
5	Update the table of “Table 8-17. LCD Characteristics”.	8.16
Revision V0.30 (2024_1111)		**Chapter**
1	Update the descriptions of the section of “CAN Data Buffer Control”.	6.16.3
2	Update the descriptions of the section of “LCD Control”.	6.21.3

3	Update the figure of “Figure 7-6. LCD Bias with Internal Charge Pump” about C_{CP}.	7.5.1
Revision V0.20 (2024_0920)		**Chapter**
1	Update the Electrical Characteristics chapter.	
Revision V0.10 (2024_0830)		**Chapter**
1	Preliminary version	

11. Disclaimers

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