

MG32F02D032

Data Sheet

Preliminary Version: 0.06

Features

❖ CPU Core

- ARM 32-bit Cortex-M0 CPU
- Operation frequency up to 24MHz
- Built-in one NVIC for 32 external interrupt inputs with 4-level priority
- Built-in one 24-bit system tick timer
- Built-in one single-cycle 32-bit multiplier
- Built-in one SWD serial wire debugger with 2 watch points and 4 breakpoints

❖ Flash Memory

- Built-in embedded 32K bytes flash memory for application code
- Built-in embedded 6K bytes flash memory for ISP code and IAP data
- Support ISP (In-system program) for application code update
 - Support programmable ISP flash memory size for ISP boot code
- Support IAP (In-application program) for application data update
 - Support programmable IAP flash memory size
- Support ICP (In-circuit program) for ISP boot code update through SWD interface
- Support flash memory page erase in 512 bytes

❖ SRAM Memory

- Built-in embedded 2K+128 bytes SRAM

❖ Power

- Built-in one embedded regulator for core logic power
- Built-in brown-out detectors
 - BOD1 detect by selected level 4.2V/3.6V/2.7V/2.4V
- Built-in a power management controller with power-down and wakeup control
- Support three power operation modes
 - ON(Normal) mode and SLEEP , STOP power down modes
- Support wake-up from SLEEP/STOP modes via multiple sources

❖ Reset

- Built-in embedded POR (power-on reset) circuit
- Built-in one reset source controller
 - Programmable chip cold reset and warm reset for reset source
 - Independent software reset control for internal modules
- Provide multiple reset source
 - POR/BOD/External reset pin input/Software force reset
 - IWDG
 - Illegal address error reset/Flash access protect error reset
 - Missing clock detect (MCD) reset

❖ Clock

- Built-in embedded ILRCO (internal low frequency RC oscillator) by 32KHz
- Built-in embedded IHRCO (internal high frequency RC oscillator)
 - Trimmed to 24MHz $\pm 1\%$ at +25°C
- Support external clock input up to 24MHz
- Built-in a clock source controller with independent clock enable control for modules

❖ GPIO

- Support general purpose IO pins for application
 - Maximum 13 GPIO pins for QFN20 package
- Provide selectable IO modes by pin independent
 - Push-Pull output
 - Quasi bidirectional (PC pins only)

- Open-drain output
- Digital Input with high impedance
- Analog IO
- Flexible pin alternate function selection
- Support programmable drive strength by pin independent
- Support IO deglitch filter by pin independent
- Support input inverse selection by pin independent
- Support pull-high option by pin independent
- Support high speed option by pin independent except RSTN, XIN
- GPIO pin state and IO mode setting keep optional after reset

❖ Interrupt Support

- Built-in one EXIC (external interrupt controller) for NVIC connection
 - Independent high/low level and rising/falling edge trigger selection
- Built-in one WIC (wakeup interrupt controller) for wakeup event control
- All GPIO pins can be configured as interrupt source and key pad input
 - Support port OR logic for interrupt function
- Support external pins for CPU NMI function

❖ Timer

- Provide six timers/counters : TM00,TM01,TM36
- Timer module common functions
 - Selectable Full-counter, Cascade, Separate timer operation modes
 - Multiple internal and external signals as timer clock source or trigger source
 - Support timer reset, trigger start and clock gating for trigger source function
 - Timer overflow as clock output to external pin output
 - Auto-stop mode by main counter counting
- Provide TM36 timer module
 - 16-bit timer with 16-bit prescaler
 - 2 CCP (input Capture/output Compare/PWM) channels
 - 2 CCP channels with OCN (complementary output compare)
 - PWM function with center/edge-align, dead time control and break control
 - Extra repetition counter for auto-stop mode
 - Support duty capture function
 - Up to 96MHz clock source for PWM output
- Provide TM0x timer modules (TM00,TM01)
 - 8-bit timer with 8-bit prescaler

❖ Watchdog Timer

- Built-in one IWDG (Independent Watch Dog Timer)
 - 8-bit down counter with 12-bit prescaler and clocked by ILRGO clock
 - Operating capability in SLEEP and STOP modes
 - Selectable reset or interrupt when the counter underflow
 - Support two early wakeup comparators with interrupt

❖ I2C

- Provide one I2C module: I2C0
- I2C module common functions
 - Support master and slave mode
 - Support programmable clock rate control and clock rate up to 400 KHz
 - Support programmable high/low period control for master mode
 - Support clock stretching for slave mode
 - Support general call function
 - Support multi-master processing capability

- Support both Byte mode and Buffer mode flow control
- Support Byte mode bus event code for simplex firmware control
- Support Buffer mode 4-byte data buffer and 32-bit data register for high speed communication
- Received and transmitted data are buffered with DMA capability
- Support slave address hardware detection wakeup from STOP mode
- Support SMBus timeout detection

❖ UART

- **Provide one UART modules: URT4**
- **UART module common functions**
 - Provide precise UART baud-rate control by programmable oversampling rate
 - Support baud rate up to 6 Mbit/s
 - Programmable data word length - 7 or 8 bits
 - Programmable 4~32 oversampling rate
 - Hardware parity checking and parity generation
 - Swappable TX/RX pin configuration
 - Separate signal polarity control for transmission and reception
 - Support fundamental UART mode
 - Support TX/RX independent 8-bit data register for simplex firmware control
 - Configurable stop bits - 1 or 2 stop bits

❖ SPI

- **Provide one modules for SPI communication: SPI0**
- **Support master and slave mode**
 - Support full duplex , half duplex or simplex communication mode
 - Support data communication without NSS(slave select signal)
 - Support master data input sampling delay half of SPI clock
 - Support slave data output advance half of SPI clock
- **Support programmable clock rate control**
 - Support clock rate up to 12 MHz for master/slave
- **Selectable 8/16/24/32-bit frame size**
 - Support 4-byte data buffer and 32-bit data register for high speed communication
- **Support multi-master processing capability**
- **Selectable clock polarity and phase**
- **Selectable MSB or LSB first data order**
- **NSS line management by hardware or software for master mode**
- **Configurable data transfer modes**
 - Standard SPI mode (separated transmit and receive line)
 - Single/Dual/Quad SPI mode with bidirectional data transfer
- **Data transmit/receive overrun detect**

❖ ADC

- **12-bit SAR ADC with 250 Ksps**
 - Configurable resolution : 12/10/8-bit
 - Configurable sampling time
- **Provide external 4 channels and internal 4 channels input**
 - Internal extra channel source : VBUF, VSSA, DAC_P0, DAC_P1
- **Data alignment for output code left/right justify**
- **Fixed ADC top voltage reference from internal VDD**
- **Interrupt generation at the end of sampling, end of conversion, end of sequence conversion**
- **Support voltage window detection and output code limitation**
- **Support one-shot/channel scan/loop scan**

❖ DAC

- Two 12-bit voltage DAC
 - Maximum conversion rate is 50 Ksps
- Conversion start trigger by register written, external pin and internal events
- Build in internal output buffer
- Support DAC output on SLEEP and STOP modes

❖ Misc.

- Timer synchronous enable global control
- 8-bit non-reset backup register
- Provide on chip 16 bytes Unique ID code

❖ Operating

- Operating temperature range -20°C ~ 85°C (**1)
- Operating frequency range up to 24MHz

❖ Package Types

- QFN20

(**1): Tested by sampling.

List of Contents

Features	3
List of Contents.....	7
List of Figures	10
List of Tables	11
1. General Description	12
2. Order Information.....	13
3. Block Diagram	15
3.1. System Function Block.....	15
3.2. Chip Main Block	16
4. Pin Description	17
4.1. Pin Outline.....	17
4.1.1. QFN20 Package Pinout	17
4.2. Pin Definition	18
4.3. Pin AFS Summary Table	21
4.4. Analog Function Pin Table.....	21
4.5. Alternate Functions Pin List.....	21
5. Memory Map	23
5.1. Memory Organization	23
5.2. CPU Memory Map.....	24
5.3. Peripheral Memory Boundary.....	25
5.4. Boot Modes	26
6. Functional Description	27
6.1. CPU Core.....	27
6.1.1. Introduction	27
6.1.2. CPU Features	27
6.1.3. ARM Cortex-M0 Processor	27
6.2. Power Management	28
6.2.1. Introduction	28
6.2.2. Chip Power Features	28
6.2.3. Power Operation Mode	28
6.2.4. Power Supply	28
6.2.5. CPU Power Down	29
6.3. System Reset.....	29
6.3.1. Introduction	29
6.3.2. Chip Reset Features	29
6.3.3. Chip Reset Levels.....	29
6.3.4. External Reset	30
6.3.5. Module Reset.....	30
6.4. System Clock	30
6.4.1. Introduction	30
6.4.2. Chip Clock Features.....	30
6.4.3. System Clock Source.....	30
6.4.4. Module Process Clock Control.....	30
6.5. System Common Control	30

6.5.1. Introduction	30
6.5.2. Features	30
6.6. Memory Access	30
6.6.1. Introduction	30
6.6.2. Features	30
6.6.3. Memory Controller	31
6.6.4. ICP/ISP/IAP for Flash Memory	31
6.6.5. Hardware Option Byte Flash Memory	31
6.7. GPIO	31
6.7.1. Introduction	31
6.7.2. Features	31
6.7.3. GPIO Control Block	32
6.8. Interrupt	32
6.8.1. Introduction	32
6.8.2. Interrupt Features	32
6.8.3. Interrupt Structure	33
6.8.4. Nested Vectored Interrupt Controller	34
6.8.5. Wakeup Interrupt Controller	34
6.8.6. External Interrupt Controller	34
6.9. APB Common Control	34
6.9.1. Introduction	34
6.9.2. Features	34
6.9.3. APB Control Block	34
6.10. I2C	34
6.10.1. Introduction	34
6.10.2. Features	35
6.10.3. I2C Control	35
6.11. UART	35
6.11.1. Introduction	35
6.11.2. Features	35
6.11.3. Module Functions	35
6.11.4. UART Control	36
6.12. SPI	36
6.12.1. Introduction	36
6.12.2. Features	36
6.12.3. Module Functions	37
6.12.4. SPI Control	37
6.13. Timer	38
6.13.1. Introduction	38
6.13.2. Features	38
6.13.3. Module Functions	38
6.13.4. Timer Control Block	39
6.14. ADC	40
6.14.1. Introduction	40
6.14.2. Features	40
6.14.3. Module Functions	40

6.14.4. ADC Control Block	41
6.15. DAC.....	41
6.15.1. Introduction	41
6.15.2. Features.....	41
6.15.3. Module Functions.....	42
6.15.4. DAC Control Block	42
7. Application Notes.....	43
7.1. Power Supply Circuit.....	43
7.2. Reset Circuit.....	43
7.3. ADC Application Circuit	44
7.4. DAC Application Circuit	44
8. Electrical Characteristics	45
8.1. Parameter Glossary	45
8.2. Absolute Maximum Rating	45
8.3. DC Characteristics	45
8.4. IO Characteristics.....	47
8.5. IHRCO Characteristics	48
8.6. ILRCO Characteristics.....	49
8.7. LDO Characteristics	49
8.8. LVR Characteristics.....	50
8.9. BOD1 Characteristics.....	51
8.10. Flash Characteristics.....	51
8.11. ADC Characteristics	51
8.12. DAC Characteristics	53
8.13. UART Characteristics	55
8.14. SPI Characteristics.....	56
8.15. I2C Characteristics.....	58
9. Package Dimension	59
9.1. QFN-20 (3x3x0.75).....	59
10. Revision History	60
11. Disclaimers	62

List of Figures

Figure 2-1. Part Numbering.....	13
Figure 3-1. System Function Block	15
Figure 3-2. Chip Main Block.....	16
Figure 4-1. QFN20 Package Pinout.....	17
Figure 5-1. Memory Organization Map	23
Figure 6-1. ARM Cortex-M0 Processor.....	27
Figure 7-1. Power Supply Circuit	43
Figure 7-2. Reset Circuit	43
Figure 7-3. ADC Application Circuit	44
Figure 7-4. DAC Application Circuit – Voltage DAC	44
Figure 8-1. UART Timing Waveform.....	55
Figure 8-2. SPI Master Timing Waveform.....	57
Figure 8-3. SPI Slave Timing Waveform.....	57
Figure 8-4. I2C Timing Waveform	58
Figure 9-1. QFN-20 (3mm X 3mm X 0.75mm) ~ AZ20	59

List of Tables

Table 2-1. Chip Selection Table	14
Table 4-1. QFN20 Pin AFS List.....	17
Table 4-2. Abbreviations for pin definition.....	18
Table 4-3. Pin Descriptions	18
Table 4-4. Pin AFS Summary Table	21
Table 4-5. Analog Function Pin Table.....	21
Table 4-6. Alternate Functions Pin List	21
Table 5-1. CPU Memory Address Map	24
Table 5-2. Peripheral Memory Boundary Address.....	25
Table 6-1. Power-Down Mode Selection.....	29
Table 6-2. Interrupt Source Table	33
Table 6-3. UART Module Function Table.....	36
Table 6-4. SPI0 Module Function Table.....	37
Table 6-5. Timer Module Function Table	38
Table 6-6. ADC0 Module Function Table.....	40
Table 6-7. DAC Module Function Table.....	42
Table 8-1. Parameter Glossary	45
Table 8-2. Absolute Maximum Rating	45
Table 8-3. DC Characteristics	45
Table 8-4. IO Characteristics	47
Table 8-6. IHRCO Characteristics.....	48
Table 8-7. ILRCO Characteristics	49
Table 8-8. LDO Characteristics	49
Table 8-9. LVR Characteristics	50
Table 8-10. BOD1 Characteristics	51
Table 8-11. Flash Characteristics	51
Table 8-12. ADC Characteristics.....	51
Table 8-13. DAC Characteristics.....	53
Table 8-14. UART Characteristics	55
Table 8-15. SPI Characteristics	56
Table 8-16. I2C Characteristics.....	58

1. General Description

The **MG32F02D032** is a single-chip 32-bit microcontroller based on a high performance Core Arm® 32-bit Cortex®-M0 CPU with embedded Nested Vectored Interrupt Controller (NVIC).

The **MG32F02D032** has fixed **32K** bytes of embedded main flash memory for application code and data. There is another fixed **6K** bytes of embedded flash memory is shared for In-System-Program (ISP) boot load code and In-Application-Program (IAP) memory. User can adjust the size for the two flash memories. Also the chip has extra 64 bytes of embedded option-byte flash memory for chip configuration.

The all flash memory can be programmed either in serial writer mode (ICP, In-Circuit-Programming). Also, the main flash memory can be programmed in ISP (In-System Programming) mode or SRAM (Boot on SRAM) mode. ICP and ISP allow the user to download new code without removing the microcontroller from the actual end product; IAP means that the device can write non-volatile data in the Flash memory while the application program is running. There needs no external high voltage for programming due to its built-in charge-pumping circuitry.

The **MG32F02D032** retains all features of the Arm® 32-bit Cortex®-M0 with **2176** bytes(2K+128) of SRAM, **2** I/O ports, **32** external interrupts source with 4-level interrupt controller and three 8/16-bits timer/counters. In addition, the **MG32F02D032** has a System Tick Timer, one Watchdog Timers, one Advance timer modules with IC/OC, two Basic timer modules for universal using, one high precision internal oscillators IHRCO for 24MHz and ILRCO for 32 KHz, one 12-bit ADC and two 12-bit voltage mode DAC.

Also, the **MG32F02D032** support multiple and flexible communicate interface for production application. It provides alternate function pins those are including of GPIO, I2C, SPI, UART, Timer with IC/PWM, ADC, DAC and SWD(on chip debug). It has maximum **13** GPIO pins and provides programmable IO type – quasi-bidirectional , push-pull output , open-drain output , input only(Hi-z) with optional pull-high. In addition, it is built-in internal de-bounce circuit to deglitch noise for worse signals.

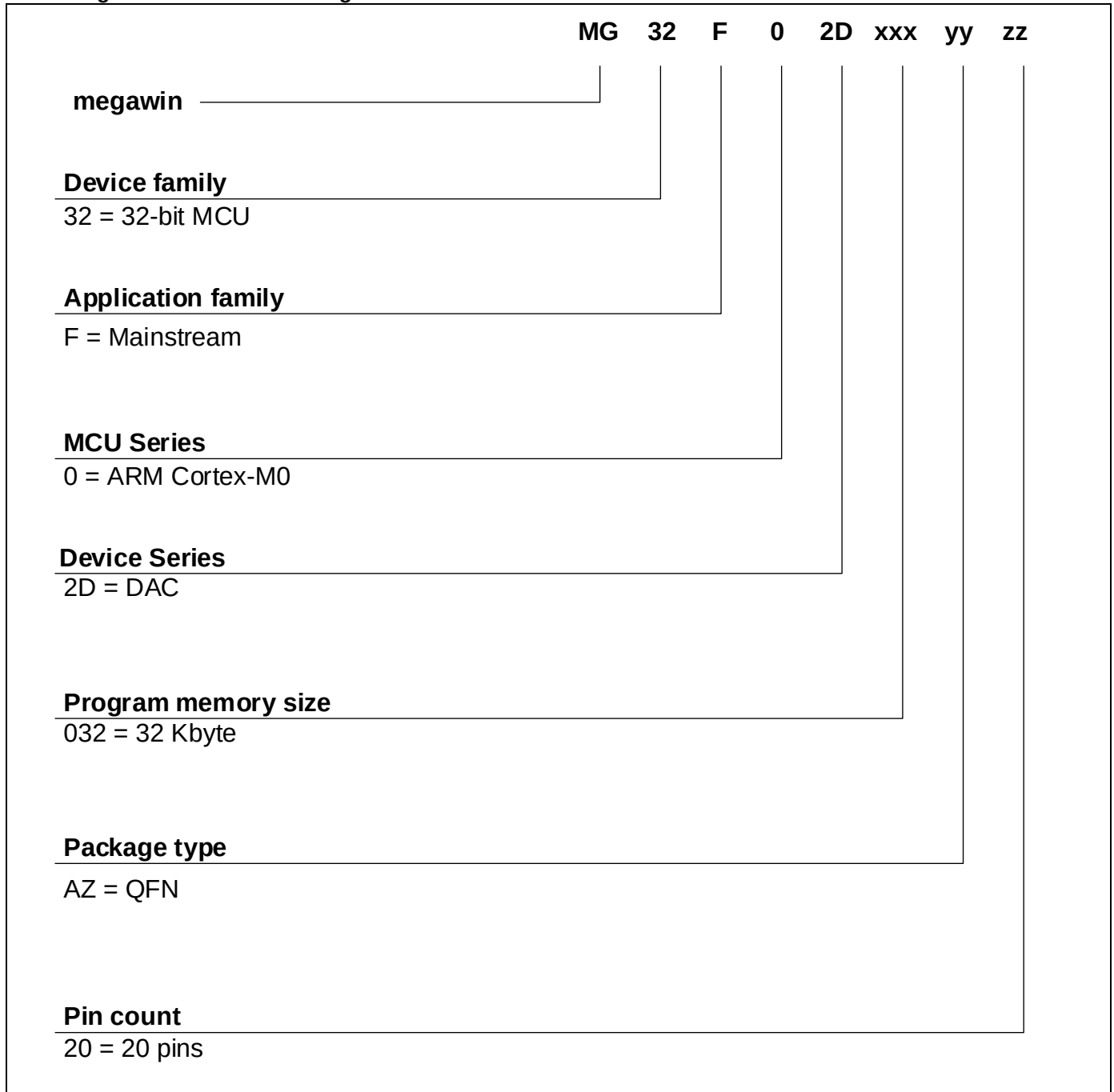
For power management and reset control, the **MG32F02D032** is built-in a power supervisor including of a Low Voltage Detector(LVD), one Brown-out Detectors(BOD1), a Power-On Reset(POR) , a Low-voltage Reset(LVR). The **MG32F02D032** has multiple power-down modes to reduce the power consumption: Sleep mode and Stop mode.

In the SLEEP mode the CPU is frozen while the peripherals and the interrupt system are still operating. In the STOP mode the RAM and SFRs' value are saved and all other functions are inoperative; most importantly, in the Sleep mode the chip can be waked up by many interrupt or reset sources(POR/LVR/ BOD1).

2. Order Information

Please contact the megawin sales for available options (memory size, package ...) and more information about this device.

Figure 2-1. Part Numbering



MG32F02D032

● Chip Selection

Table 2-1. Chip Selection Table

Chip Functions	MG32F02D032	Comment
Flash ROM	32KB	memory space of AP+IAP+ISP
SRAM	2KB+128B	
Package	QFN20	
IO Number	13	IO number by package
Max. CPU Frequency	24MHz	
Internal Clock Source	ILRCO+IHRCO	12MHz(default) & 11.059MHz option for IHRCO
Voltage Detector	LVR+BOD1	Low Voltage Reset (LVR), BOD1: 4.2/3.6/2.7/2.4V
Timers	16-bit*2: TM00/01 32-bit*1: TM36	support Full-Counter, Cascade , Separate modes
IC/OC/PWM Channels	2-CH (16-bit) or 4-CH(8-bit)	IC: Input Capture, OC: Output Compare (support normal + complement output)
WDT	IWDT	IWDT: Independent Watch Dog Timer
ADC	12-Bit , 4-CH 250Ksps	
DAC	12-Bit , 2-CH 50Ksps	
I2C Units	1	optional Byte/Buffer mode, with/without clock stretching
UART Units	Basic *1	
SPI Units	1	master/slave mode with or without NSS control
SPI Max. Clock Rate	Master: 12 MHz Slave: 12 MHz	slave 12MHz for asynchronous mode
Operation Voltage	2.7~5.5V	
Operating Temperature	-20~85°C	test by sampling
Flash Regions	AP,IAP,ISP	Application flash, In-Application-Programming data flash, In-System-Programming flash (ISP: In-System-Programming data flash)

● Part Number List

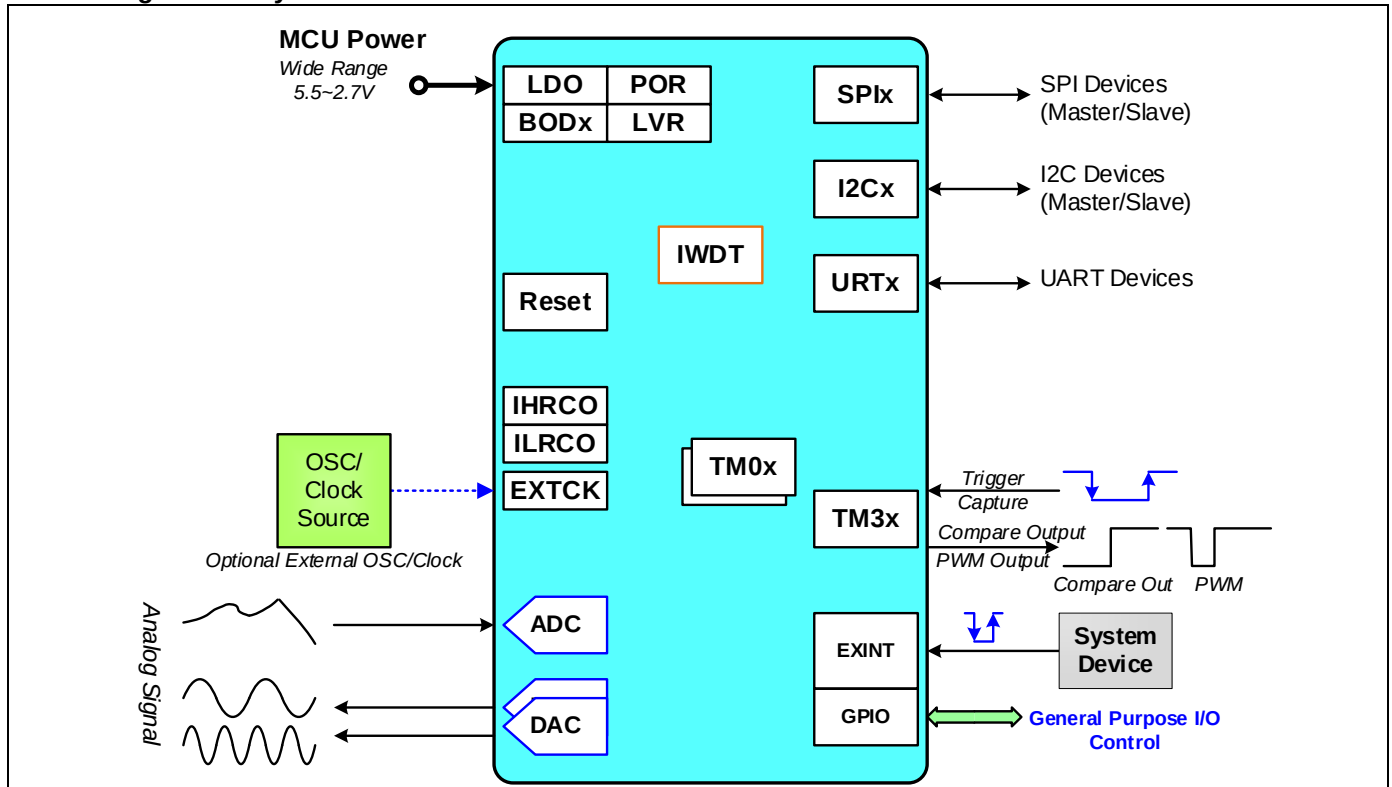
— MG32F02D032AZ20 : QFN20 (3mm x 3mm), 32KB Flash

3. Block Diagram

3.1. System Function Block

The following diagram is showing the system function block for application.

Figure 3-1. System Function Block

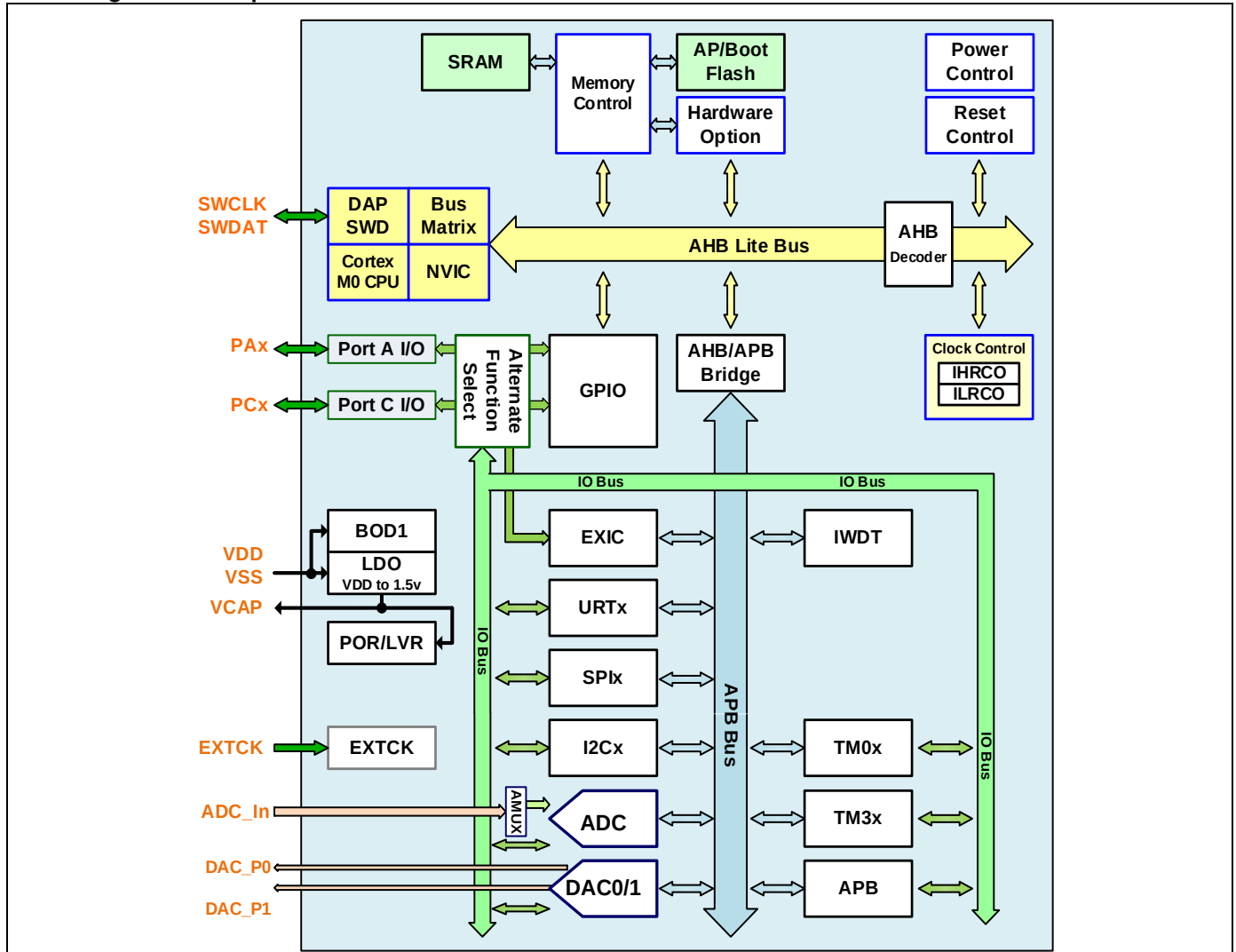


3.2. Chip Main Block

The following diagram is showing the block of internal devices in the chip.

There are one embedded ARM® Cortex®-M0 processor with NVIC (Nested Vectored Interrupt Controller) and DAP (Debug Access Port); AHB lite bus with SRAM/Flash memory, Power/Reset/Clock system controllers, and GPIO control blocks; APB bus with UART / SPI / I2C communication controllers, timers of general timer / IWDT and analog control block of ADC / DAC; analog devices of POR (power on reset), BOD1 (Brown-Out Detectors), ILRCO (Internal Low-frequency RC Oscillator)/IHRCO Internal High-frequency RC Oscillator).

Figure 3-2. Chip Main Block



4. Pin Description

4.1. Pin Outline

4.1.1. QFN20 Package Pinout

Figure 4-1. QFN20 Package Pinout

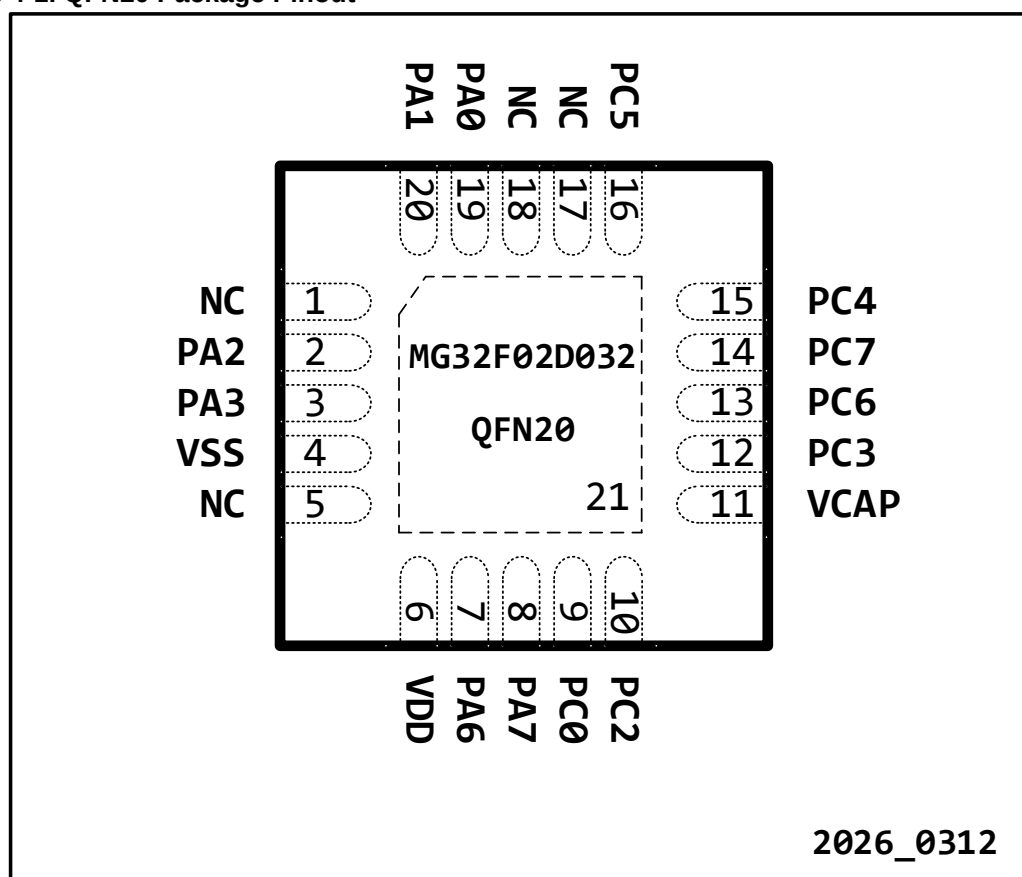


Table 4-1. QFN20 Pin AFS List

Pin	Name	Pin AFS List	Analog Function
1	NC		
2	PA2	GPA2, SPI0_CLK, TM36_OC00, I2C0_SCL, URT4_TX	ADC_I2
3	PA3	GPA3, RSTN, SPI0_MOSI, TM36_OC10, I2C0_SDA, URT4_RX	ADC_I3
4	VSS		
5	NC		
6	VDD		
7	PA6	GPA6, SPI0_NSS, TM36_OC00, I2C0_SCL	DAC_P0
8	PA7	GPA7, TM36_CKO, SPI0_MISO, TM36_OC10, I2C0_SDA	DAC_P1
9	PC0	GPC0, ICKO, TM00_CKO, TM36_OC00, I2C0_SCL, EXTCK, DAC_TRG0, TM36_IC0	
10	PC2	GPC2, ADC0_OUT, TM36_OC10, SPI0_NSS, I2C0_SCL, MF_S0, TM36_OC0N, DAC_TRG0	
11	VCAP		
12	PC3	GPC3, TM36_OC1N, SPI0_MISO, I2C0_SDA, MF_S1, TM36_IC1, DAC_TRG1	
13	PC6	GPC6, SPI0_CLK, TM36_OC1N, URT4_TX	
14	PC7	GPC7, ADC0_TRG, TM36_TRGO, SPI0_MOSI, URT4_RX	
15	PC4	GPC4, SWCLK, I2C0_SCL, TM36_OC00, TM01_CKO, URT4_TX	
16	PC5	GPC5, SWDIO, I2C0_SDA, TM36_OC10, SPI0_NSSI, DAC_TRG1, URT4_RX	
17	NC		
18	NC		
19	PA0	GPA0, TM36_OC00, URT4_TX	ADC_I0
20	PA1	GPA1, CPU_NMI, TM36_OC10, URT4_RX	ADC_I1, VBG_OUT
21	VSS		

4.2.

4.2. Pin Definition

Table 4-2. Abbreviations for pin definition

IO Type		IO Structure	
P	Power/Ground pin	I	Digital Input
B	Bidirectional	P	Output Push-pull capability
I	Input	O	Output Open drain capability
O	Output	Q	Quasi-bidirectional
A	Analog I/O	A	Analog I/O (Digital I/O disable)
AO	Analog output only	U	Internal pull-up
Q	Quasi-bidirectional	CF	Fixed driving strength(GPIO mode)

Table 4-3. Pin Descriptions

Pin Name	Pin Number	IO Type	Default		IO Structure	Alternate Functions	Description
	QFN20		Type	Value			
PA0	19	B	A		A,I,P,O,U,CF	GPA0	GPIO/Interrupt/KBI Port-A function pin-0
						TM36_OC00	TM36 output compare/PWM channel-00
						URT4_TX	URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.
						ADC_I0	ADC analog single-end input channel 0
PA1	20	B	A		A,I,P,O,U,CF	GPA1	GPIO/Interrupt/KBI Port-A function pin-1
						CPU_NMI	CPU NMI external pin input
						TM36_OC10	TM36 output compare/PWM channel-10
						URT4_RX	URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.
						ADC_I1	ADC analog single-end input channel 1
						VBG_OUT	Bandgap voltage output
PA2	2	B	A		A,I,P,O,U,CF	GPA2	GPIO/Interrupt/KBI Port-A function pin-2
						SPI0_CLK	SPI0 clock signal
						TM36_OC00	TM36 output compare/PWM channel-00
						I2C0_SCL	I2C0 SCL signal
						URT4_TX	URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.
						ADC_I2	ADC analog single-end input channel 2
PA3	3	B	A		A,I,P,O,U,CF	GPA3	GPIO/Interrupt/KBI Port-A function pin-3
						RSTN	External hardware reset input
						SPI0_MOSI	SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
						TM36_OC10	TM36 output compare/PWM channel-10
						I2C0_SDA	I2C0 SDA signal
						URT4_RX	URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.
						ADC_I3	ADC analog single-end input channel 3
PA6	7	B	A		A,I,P,O,Q,U,CF	GPA6	GPIO/Interrupt/KBI Port-A function pin-6
						SPI0_NSS	SPI0 slave select input/output signal

						TM36_OC00	TM36 output compare/PWM channel-00
						I2C0_SCL	I2C0 SCL signal
						DAC_P0	DAC analog output channel 0
PA7	8	B	A		A,I,P,O,Q,U,CF	GPA7	GPIO/Interrupt/KBI Port-A function pin-7
						TM36_CKO	TM36 timer overflow output signal
						SPI0_MISO	SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
						TM36_OC10	TM36 output compare/PWM channel-10
						I2C0_SDA	I2C0 SDA signal
						DAC_P1	DAC analog output channel 1
PC0	9	B	A		A,I,P,O,Q,U,CF	GPC0	GPIO/Interrupt/KBI Port-C function pin-0
						ICKO	Internal clock source clock output
						TM00_CKO	TM00 timer overflow output signal
						TM36_OC00	TM36 output compare/PWM channel-00
						I2C0_SCL	I2C0 SCL signal
						EXTCK	External clock source clock input
						DAC_TRG0	DAC trigger start input
PC2	10	B	A		A,I,P,O,Q,U,CF	TM36_IC0	TM36 input capture channel-0
						GPC2	GPIO/Interrupt/KBI Port-C function pin-2
						ADC0_OUT	ADC threshold window compare output
						TM36_OC10	TM36 output compare/PWM channel-10
						SPI0_NSS	SPI0 slave select input/output signal
						I2C0_SCL	I2C0 SCL signal
						MF_S0	Multi-Function signal-0 output
PC3	12	B	A		A,I,P,O,Q,U,CF	TM36_OC0N	TM36 output compare/PWM complement channel-0
						DAC_TRG0	DAC trigger start input
						GPC3	GPIO/Interrupt/KBI Port-C function pin-3
						TM36_OC1N	TM36 output compare/PWM complement channel-1
						SPI0_MISO	SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
						I2C0_SDA	I2C0 SDA signal
						MF_S1	Multi-Function signal-1 output
PC4	15	B	Q	H	A,I,P,O,Q,U,CF	TM36_IC1	TM36 input capture channel-1
						DAC_TRG1	DAC trigger start input
						GPC4	GPIO/Interrupt/KBI Port-C function pin-4
						SWCLK	Serial wire debug clock signal
						I2C0_SCL	I2C0 SCL signal
						TM36_OC00	TM36 output compare/PWM channel-00
						TM01_CKO	TM01 timer overflow output signal
PC5	16	B	Q	H	A,I,P,O,Q,U,CF	URT4_TX	URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.
						GPC5	GPIO/Interrupt/KBI Port-C function pin-5
						SWDIO	Serial wire debug data signal
						I2C0_SDA	I2C0 SDA signal

MG32F02D032

						TM36_OC10	TM36 output compare/PWM channel-10
						SPI0_NSSI	SPI0 slave select input only signal
						DAC_TRG1	DAC trigger start input
						URT4_RX	URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.
PC6	13	B	Q	H	A,I,P,O,Q,U,CF	GPC6	GPIO/Interrupt/KBI Port-C function pin-6
						SPI0_CLK	SPI0 clock signal
						TM36_OC1N	TM36 output compare/PWM complement channel-1
						URT4_TX	URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.
PC7	14	B	A		A,I,P,O,Q,U,CF	GPC7	GPIO/Interrupt/KBI Port-C function pin-7
						ADC0_TRG	ADC trigger start input
						TM36_TRGO	TM36 trigger output signal
						SPI0_MOSI	SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting.
						URT4_RX	URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.
VSS	4,21	P					IO/Core/ADC ground
VCAP	11	AO	AO				(VCAP) Core power supply/LDO output (place 0.1Uf+4.7Uf capacitors and close pin)
VDD	6	P					IO power supply/LDO input (place 0.1Uf+10Uf capacitors and close pin)
VCC1	NC	P					Hall sensor power supply
HOUT1	NC	AO	AO				Hall sensor output
VCC2	NC	P					Hall sensor power supply
HOUT2	NC	AO	AO				Hall sensor output

4.3. Pin AFS Summary Table

The following table is the AFS signal list of the related IO pin for all pins' summary. (AFS=n, n: I/O pin AFS setting value)

Table 4-4. Pin AFS Summary Table

Pin	AFS=0	AFS=1	AFS=2	AFS=3	AFS=4	AFS=5	AFS=6	AFS=7	AFS=8	AFS=9	AFS=10	AFS=11	AF12
PA0	GPA0										TM36_OC00	URT4_TX	
PA1	GPA1	CPU_NMI									TM36_OC10	URT4_RX	
PA2	GPA2							SPI0_CLK	TM36_OC00	I2C0_SCL			URT4_TX
PA3	GPA3	RSTN						SPI0_MOSI	TM36_OC10	I2C0_SDA			URT4_RX
PA6	GPA6						SPI0_NSS		TM36_OC00	I2C0_SCL			
PA7	GPA7			TM36_CKO			SPI0_MISO		TM36_OC10	I2C0_SDA			
PC0	GPC0	ICKO	TM00_CKO				TM36_OC00	I2C0_SCL	EXTCK	DAC_TRG0			TM36_IC0
PC2	GPC2	ADC0_OUT					TM36_OC10		SPI0_NSS	I2C0_SCL	MF_S0	TM36_OC0N	DAC_TRG0
PC3	GPC3						TM36_OC1N		SPI0_MISO	I2C0_SDA	MF_S1	TM36_IC1	DAC_TRG1
PC6	GPC6								SPI0_CLK			TM36_OC1N	URT4_TX
PC7	GPC7	ADC0_TRG					TM36_TRG0		SPI0_MOSI				URT4_RX
PC4	GPC4	SWCLK	I2C0_SCL						TM36_OC00	TM01_CKO			URT4_TX
PC5	GPC5	SWDIO	I2C0_SDA						TM36_OC10	SPI0_NSSI	DAC_TRG1		URT4_RX
Pin	AFS=0	AFS=1	AFS=2	AFS=3	AFS=4	AFS=5	AFS=6	AFS=7	AFS=8	AFS=9	AFS=10	AFS=11	AF12

4.4. Analog Function Pin Table

The following table is the analog signal pin list for all the analog function.

Table 4-5. Analog Function Pin Table

Pin Name	ANA0	ANA1	ANA2
PA0	ADC_I0		
PA1	ADC_I1		VBG_OUT
PA2	ADC_I2		
PA3	ADC_I3		
PA6			DAC_P0
PA7			DAC_P1

4.5. Alternate Functions Pin List

The following table is the pin list of the related AFS IO signal for all AFS signals' summary.

Table 4-6. Alternate Functions Pin List

No.	AFS List		Pin List for the AFS IO ([] : AFS setting value)					
	Group	AFS Name	Pin-1 Name	Pin-2 Name	Pin-3 Name	Pin-4 Name	Pin-5 Name	Pin-6 Name
1	GPA	GPA0	PA0 [0]					
2		GPA1	PA1 [0]					
3		GPA2	PA2 [0]					
4		GPA3	PA3 [0]					
5		GPA6	PA6 [0]					
6		GPA7	PA7 [0]					

MG32F02D032

7	GPC	GPC0	PC0 [0]					
8		GPC2	PC2 [0]					
9		GPC3	PC3 [0]					
10		GPC6	PC6 [0]					
11		GPC7	PC7 [0]					
12		GPC4	PC4 [0]					
13		GPC5	PC5 [0]					
14	Chip	SWCLK	PC4 [1]					
15		SWDIO	PC5 [1]					
16		RSTN	PA3 [1]					
17		ICKO	PC0 [1]					
18		CPU_NMI	PA1 [1]					
19	ANALIO	ADC0_TRG	PC7 [1]					
20		ADC0_OUT	PC2 [1]					
21		DAC_TRG0	PC0 [9]	PC2 [12]				
22		DAC_TRG1	PC3 [12]	PC5 [10]				
23	I2C0	I2C0_SCL	PA2 [9]	PA6 [9]	PC0 [7]	PC2 [9]	PC4 [2]	
24		I2C0_SDA	PA3 [9]	PA7 [9]	PC3 [9]	PC5 [2]		
25	URT4567	URT4_TX	PA0 [11]	PA2 [12]	PC6 [12]	PC4 [12]		
26		URT4_RX	PA1 [11]	PA3 [12]	PC7 [12]	PC5 [12]		
27	SPI0	SPI0_CLK	PA2 [7]	PC6 [8]				
28		SPI0_MOSI	PA3 [7]	PC7 [8]				
29		SPI0_MISO	PA7 [6]	PC3 [8]				
30		SPI0_NSS	PA6 [6]	PC2 [8]				
31		SPI0_NSSI	PC5 [9]					
32	TM00	TM00_CKO	PC0 [2]					
33	TM01	TM01_CKO	PC4 [9]					
34	TM36	TM36_CKO	PA7 [3]					
35		TM36_TRGO	PC7 [6]					
36		TM36_IC0	PC0 [12]					
37		TM36_IC1	PC3 [11]					
38		TM36_OC00	PA0 [10]	PC0 [6]	PA2 [8]	PA6 [8]	PC4 [8]	
39		TM36_OC0N	PC2 [11]					
40		TM36_OC10	PA1 [10]	PC2 [6]	PA3 [8]	PA7 [8]	PC5 [8]	
41		TM36_OC1N	PC3 [6]	PC6 [11]				
42	Other	MF_S0	PC2 [10]					
43		MF_S1	PC3 [10]					
44		EXTCK	PC0 [8]					

5. Memory Map

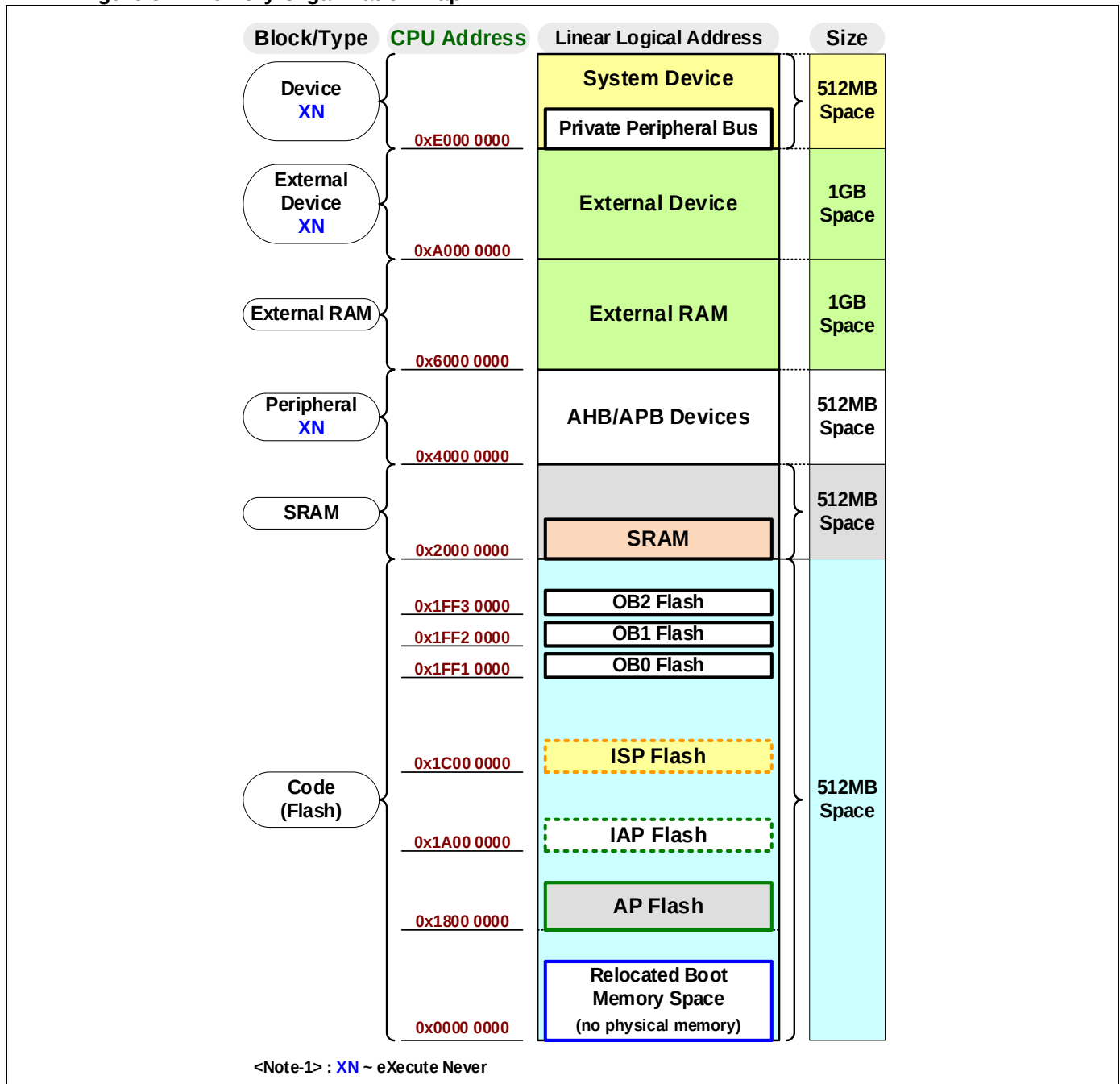
5.1. Memory Organization

There are up to **2176** bytes of SRAM built in the chip. The chip has up to **32K** bytes of embedded main flash memory for code and data, programmable memory size of embedded system flash memory for boot load code and 64 bytes of embedded option-byte (**OB**) flash memory for chip configuration. Others, there are many module independent hardware control registers and locate at the memory space of AHB/APB devices.

The fixed **32K** bytes of embedded main flash memory is used to store for Application Program (AP) code. There is another fixed **6K** bytes of embedded flash memory is shared for In-System-Program (ISP) code and In-Application-Program (IAP) memory. User can adjust the size for the two flash memories.

The following diagram is showing the memory organization map. There are separated eight memory blocks and the memory size is 512M-byte for each block. The block is signed “XN” which is not able to execute code.

Figure 5-1. Memory Organization Map



5.2. CPU Memory Map

The following table is showing the memory address map of CPU. The block is signed “XN” which is not able to execute code.

Table 5-1. CPU Memory Address Map

Block Index	Block Name	XN	Boundary address		Size	Address Space	Note
			Start address	End address			
7	System Device	XN	0Xe010 0000	0Xfff FFFF	511MB	VENDOR_SYS	
			0Xe000 0000	0Xe00F FFFF	1MB	Private Peripheral Bus(PPB)	M0 Reserved Cortex M0 internal peripherals
6	External Device	XN	0Xc000 0000	0Xdfff FFFF	512MB	Reserved	External memory (SRAM, Flash)
5	External Device	XN	0Xa000 0000	0Xbfff FFFF	512MB	Reserved	External memory (SRAM, Flash)
4	External RAM		0x8000 0000	0x9FFF FFFF	512MB	Reserved	External memory (SRAM, Flash)
3	External RAM		0x6000 0000	0x7FFF FFFF	512MB	Reserved	External memory (SRAM, Flash)
2	Peripheral	XN	0x4000 0000	0x5FFF FFFF	512MB	APB/AHB	APB/AHB modules
			0x2000 0880	0x3FFF FFFF	512MB	Reserved	
			0x2000 0000	0x2000 087F	2KB	SRAM (*2)	2KB+128B
0	Code		0x1FF3 0200	0x1FFF FFFF	832KB	Reserved	
			0x1FF3 0040	0x1FF3 01FF	448B	OB Flash-2	
			0x1FF3 0000	0x1FF3 003F	64B		Hardware Option byte-2 (64-byte)
			0x1FF2 0200	0x1FF2 FFFF	64KB	Reserved	
			0x1FF2 0050	0x1FF2 01FF	432B	OB Flash-1	
			0x1FF2 0040	0x1FF2 004F	16B		Unique ID (16-byte)
			0x1FF2 0000	0x1FF2 003F	64B		Hardware Option byte-1 (64-byte)
			0x1FF1 0200	0x1FF1 FFFF	64KB	Reserved	
			0x1FF1 0040	0x1FF1 01FF	448B	OB Flash-0	
			0x1FF1 0000	0x1FF1 003F	64B		Hardware Option byte-0 (64-byte)
			0x1C00 1800	0x1FF0 FFFF	63MB	Reserved	
			0x1C00 0000	0x1C00 17FF	6KB	ISP Flash (*2)	Boot Flash memory (configurable size, ISP+IAP max. 6KB)
			0x1A00 1800	0x1BFF FFFF	32MB	Reserved	
			0x1A00 0000	0x1A00 17FF	6KB	IAP Flash (*2)	Data Flash memory (configurable size, ISP+IAP max. 6KB)
			0x1800 8000	0x19FF FFFF	32MB	Reserved	
			0x1800 0000	0x1800 7FFF	32KB	AP Flash (*2)	Application Flash memory (fixed size)
			0x0000 8000	0x17FF FFFF	384MB	Reserved	
			0x0000 0000	0x0000 7FFF	32KB	Relocated memory space (*1)	Interrupt Vector 0x0000 00C0~0x0000 0000

XN: eXecute Never , 1 Block = 512MB

*1: Relocated memory space : Main flash memory, Boot flash memory or SRAM depending on BOOT configuration

*2: The table lists the maximum value. Refer the chip “Chip Selection Table” about actual memory size.

5.3. Peripheral Memory Boundary

Table 5-2. Peripheral Memory Boundary Address

Address Type	Boundary address		Size	Sections / Groups Peripheral	Module	Note
	Start address	End address				
APB	0x5F01 0100	0x5FFF FFFF	16MB	APB	Reserved	
	0x5F00 0000	0x5F00 00FF	256B		APB	APB module global control
	0x5E00 0000	0x5EFF FFFF	16MB	Reserved	Reserved	
	0x5D00 0100	0x5DFF FFFF	16MB	WDT/RTC	Reserved	
	0x5D00 0000	0x5D00 00FF	256B		IWDT	Independent WatchDog Timer
	0x5C08 0100	0x5CFF FFFF	15MB	DAC	Reserved	
	0x5C08 0000	0x5C08 00FF	256B		DAC	Digital-to-Analog controller
	0x5B00 0100	0x5C07 FFFF	16MB	ADC	Reserved	
	0x5B00 0000	0x5B00 00FF	256B		ADC0	Analog-to-Digital controller
	0x5700 0000	0x5AFF FFFF	64MB	Reserved	Reserved	
	0x5686 0100	0x56FF FFFF	8MB	TM2x/3x	Reserved	
	0x5686 0000	0x5686 00FF	256B		TM36	32-bit Timer with 4 IC/OC/PWM
	0x5501 0100	0x5685 FFFF	24MB		Reserved	
	0x5501 0000	0x5501 00FF	256B		TM01	Basic 16-bit Timer/Counter
	0x5500 0100	0x5500 FFFF	64KB		Reserved	
	0x5500 0000	0x5500 00FF	256B		TM00	Basic 16-bit Timer/Counter
	0x5300 0100	0x54FF FFFF	32MB	SPI	Reserved	
	0x5300 0000	0x5300 00FF	256B		SPI0	SPI bus controller with data buffer
	0x5204 0100	0x52FF FFFF	16MB	UART	Reserved	
	0x5204 0000	0x5204 00FF	256B		URT4	Basic UART bus controller
	0x5100 0100	0x5203 FFFF	16MB	I2C	Reserved	
	0x5100 0000	0x5100 00FF	256B		I2C0	I2C bus controller
	0x5000 0100	0x50FF FFFF	16MB	EXT Interrupt	Reserved	
	0x5000 0000	0x5000 00FF	256B		EXIC	External Interrupt Controller
AHB	0x4FF0 0100	0x4FFF FFFF	1MB	Chip	Reserved	
	0x4FF0 0000	0x4FF0 00FF	256B		CFG	Hardware option (NVR0/1/2)
	0x4F00 0100	0x4FEF FFFF	15MB		Reserved	
	0x4F00 0000	0x4F00 00FF	256B		WRI	Writer Interface Control
	0x4E00 0000	0x4EFF FFFF	16MB	Reserved	Reserved	
	0x4D00 0100	0x4DFF FFFF	16MB	Memory	Reserved	
	0x4D00 0000	0x4D00 00FF	256B		MEM	Internal Memory Controller
	0x4C03 0100	0x4CFF FFFF	16MB	System	Reserved	
	0x4C03 0000	0x4C03 00FF	256B		SYS	System and Chip Control
	0x4C02 0100	0x4C02 FFFF	64KB		Reserved	
	0x4C02 0000	0x4C02 00FF	256B		PW	Power Management Controller
	0x4C01 0100	0x4C01 FFFF	64KB		Reserved	
	0x4C01 0000	0x4C01 00FF	256B		CSC	Clock Source Controller
	0x4C00 0100	0x4C00 FFFF	64KB		Reserved	
	0x4C00 0000	0x4C00 00FF	256B		RST	Reset Source Controller
	0x4500 0000	0x4BFF FFFF	112MB	Reserved	Reserved	Reserved for future design
	0x4402 0100	0x44FF FFFF	16MB	IO Configure	Reserved	
	0x4402 0000	0x4402 00FF	256B		PC	
	0x4400 0100	0x4401 FFFF	128KB		Reserved	
	0x4400 0000	0x4400 00FF	256B		PA	
	0x4100 0200	0x43FF FFFF	48MB	Reserved		Reserved for future design
	0x4100 0000	0x4100 01FF	512B	GPIO	IOP	IO Port Input/Output
	0x4000 0000	0x40FF FFFF	16MB	Reserved		Reserved for future design

5.4. Boot Modes

During chip startup, the hardware configuration option-byte (**OB**) is used to select one of the three boot options:

- **Boot from User Application Program (AP) Flash**
- **Boot from In-System-Program (ISP)**
- **Boot from embedded SRAM**

6. Functional Description

6.1. CPU Core

6.1.1. Introduction

The chip is embedded a CPU core of Cortex®™-M0 processor. The processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional DAP hardware debug functionality.

The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes –Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

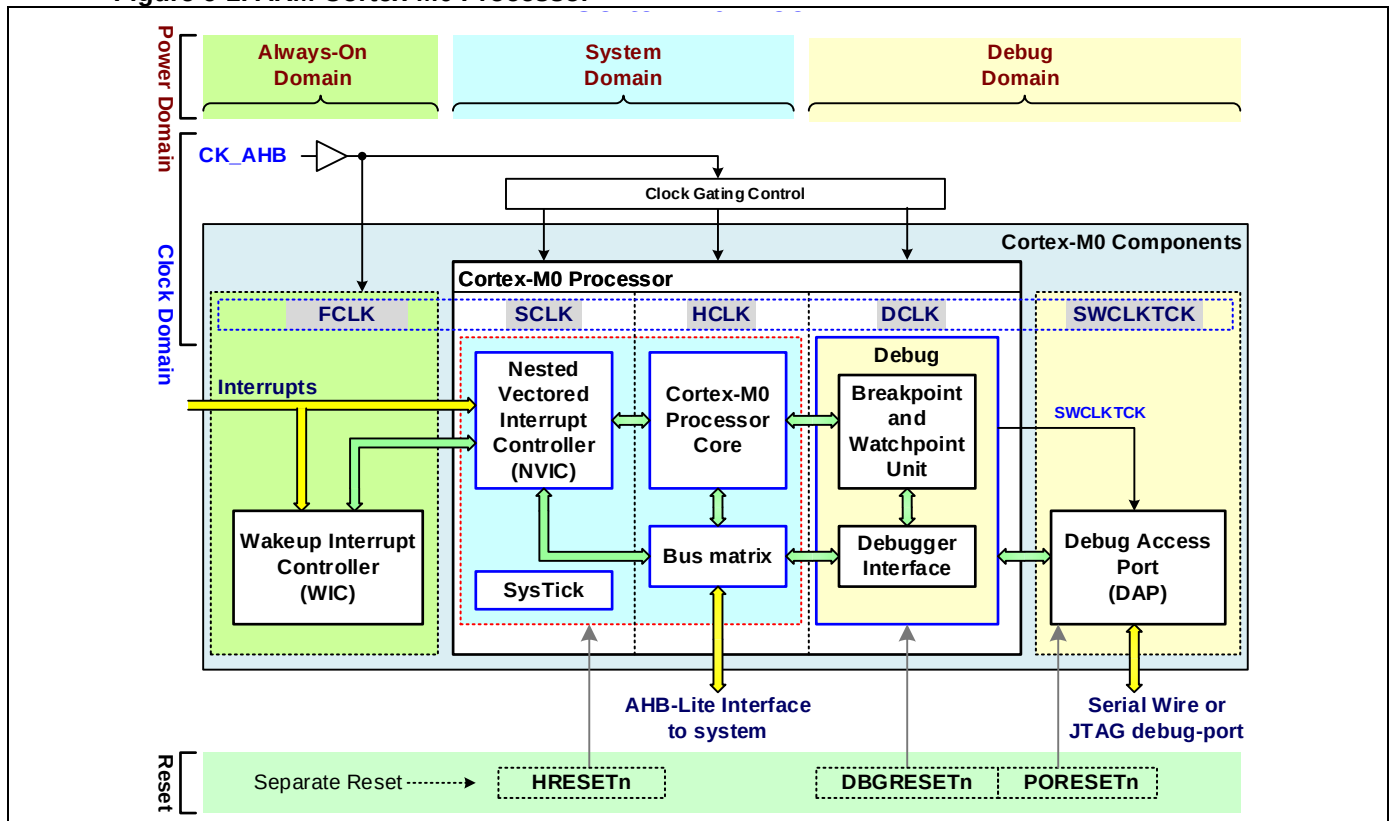
6.1.2. CPU Features

- ARM® 32-bit Cortex®-M0 CPU
- Operation frequency up to 24MHz
- Built-in one NVIC for 32 external interrupt inputs with 4-level priority
- Built-in one 24-bit system tick timer
- Built-in one single-cycle 32-bit multiplier
- Built-in one SWD serial wire debugger with 2 watch points and 4 breakpoint
- The ARMv6-M Thumb® instruction set

6.1.3. ARM Cortex-M0 Processor

The following diagram is showing the block of ARM® Cortex®-M0 Processor.

Figure 6-1. ARM Cortex-M0 Processor



6.2. Power Management

6.2.1. Introduction

The chip power is implemented only by single power supply input and embedded one LDO to supply the internal core logic power. The chip supports one power controller (PW) to manage Power-on reset (POR) circuit, Low-voltage reset (LVR) circuit, Brown-Out Detectors (BOD1), power down control and wakeup control.

It supports power-down modes: **SLEEP** mode and **STOP** modes. The power-down modes reduce chip power and provide the different power-saving scheme for chip application.

6.2.2. Chip Power Features

- Built-in one embedded regulator for core logic power
- Built-in brown-out detectors
 - BOD1 detect by selected level 4.2V/3.6V/2.7V/2.4V
- Built-in a power management controller with power-down and wakeup control
- Support three power operation modes
 - ON(Normal) mode and SLEEP , STOP power down modes
- Support wake-up from SLEEP/STOP modes via multiple sources
 - Wake-up sources come from GPIO pins, IWD1, I2C, BOD1

6.2.3. Power Operation Mode

There are three power operation modes of **ON**, **SLEEP**, **STOP** to be supported in the power controller.

- **ON mode**

In **ON** mode, the CPU is able running in full speed. All peripheral modules can use full power to do normally full function operation. These modules can enable or disable independent to save current consumption.

- **SLEEP mode**

In **SLEEP** mode, only the CPU is stopped and entering CPU sleep mode. All peripheral modules can be configurable to continue to operate or sleep.

In this mode, the chip can be waked up by the related interrupt or event occurs.

- **STOP mode**

The **STOP** mode provides the lowest current consumption. The different from SLEEP mode is that CPU is entering CPU deep-sleep mode and all peripheral modules are disabled except some special modules or devices. These modules or devices can be configurable to continue to operate in STOP mode or not. They include of IWD1 module and LVR, BOD1 devices. The internal voltage regulator is also running in low power mode.

In this mode, the chip can be waked up by some of the external input lines (GPIO) and some events detection.

6.2.4. Power Supply

The chip power is implemented only by single power supply input for easy application PCB design. It is embedded one internal low dropout linear regulator (LDO) to generate the +1.5 volt voltage power VDDC for core logic power supply.

The **VDD** pin(s) is/are using for IO power supply input and internal LDO input. The **VSS** pin(s) is/are used to connect the external ground for internal reference ground of internal LDO, hard macros and digital logic. The **VCAP** pin is the LDO output and it needs to connect bypass capacitors for normal operation.

6.2.5. CPU Power Down

For chip entering power down mode, the firmware must execute WFI or WFE instruction to force the CPU enters sleep mode or deep sleep mode. Then the chip will enter the power down mode of **SLEEP** or **STOP**. User can configure the CPU sleep mode by setting CPU register of SLEEPDEEP after firmware executes WFI or WFE instruction.

Table 6-1. Power-Down Mode Selection

CPU	System	CPU Register
		SLEEPDEEP
Run	ON	x
sleep	SLEEP	0
deep sleep	STOP	1

6.3. System Reset

6.3.1. Introduction

During reset, all Registers are set to their initial values, and the program starts execution from the Reset Vector. The chip includes a reset source controller (RST) to manage multiple sources of reset and generates Warm reset and Cold reset signals to chip system and internal modules. This controller also provides the reset event flags for firmware, which are used to recognize the reset occurred source.

6.3.2. Chip Reset Features

- Built-in embedded POR(power-on reset)/LVR(low-voltage reset) circuit
- Built-in one reset source controller
 - Programmable chip cold reset and warm reset for reset source
 - Independent software reset control for internal modules
- Provide multiple reset sources
 - POR/LVR/BOD1/External reset pin input/Software force reset
 - IWDG/ADC
 - IAR(Illegal address error reset)/Flash access protect error reset

6.3.3. Chip Reset Levels

The chip provides three reset levels – POR reset, Cold reset and Warm reset. POR reset is the highest priority reset and is generated by chip hardware. Cold reset is the 2nd priority and Warm reset is the lowest priority reset.

When POR reset occurred, it will cause to generate Cold reset to chip. Also when Cold reset occurred, it will cause to generate Warm reset to chip.

● Power-On Reset

Power-on reset (**POR**) is used to internally reset the chip and also the CPU during power-up. The chip will keep in reset state and will not start to work until the VDD power rises above the voltage of Power-On Reset. And, the reset state is activated again whenever the VDD power falls below the POR threshold voltage. During a power off cycle, VDD must fall below the POR threshold voltage before power is reapplied in order to ensure a power-on reset.

● Cold Reset

Cold reset is the 2nd priority reset. The Cold reset is also generated and caused by POR reset occurred. It sends to some modules like as IWDG, ... to do deep level module reset. It will cause to reload all hardware configurations **OB** and disable the register lock function for the modules which are support the register lock function.

● Warm Reset

Warm reset is the lowest priority reset. The Warm reset is also generated and caused by Cold reset occurred. It sends to all modules to clear flags and hardware circuit. It will cause to reload some hardware configuration **OB** and reset the registers of module to default value if the module is unlocked or not supported lock function. It will clear Warm reset source enable bits in RST controller if the RST controller is unlocked.

6.3.4. External Reset

The chip provides an external hardware reset input from **RSTN** pin, which is accomplished by holding low level for the **RSTN** pin. The **RSTN** pin is configured to as external reset pin or others (GPIO ...) by hardware configuration **OB**. To ensure a reliable power-up reset, then the hardware reset from **RSTN** pin is necessary.

6.3.5. Module Reset

For each AHB or APB control module, it can receive the system Warm reset signal to reset the module's control flags, registers and logical circuit. For some modules of IWDT, PW, CSC and MEM, they can receive the Cold reset to unlock the register locked function and reset the module.

6.4. System Clock

6.4.1. Introduction

The chip builds in a clock source controller (CSC) for system clock source management. There are four clock sources for the system application: Internal High-frequency RC Oscillator (**IHRCO**), Internal Low-frequency RC Oscillator (**ILRCO**) and External Clock Input (**EXTCK**).

6.4.2. Chip Clock Features

- Built-in embedded ILRCO (internal low frequency RC oscillator) by 32KHz
- Built-in embedded IHRCO (internal high frequency RC oscillator)
 - Trimmed to 24MHz $\pm 1\%$ at +25°C
- Support external clock input up to 24MHz
- Built-in a clock source controller with clock enable control for modules
- Support internal ILRCO/IHRCO clock output

6.4.3. System Clock Source

There are three clock sources for the system application: Internal High-frequency RC Oscillator (**IHRCO**), Internal Low-frequency RC Oscillator (**ILRCO**) and External Clock Input (**EXTCK**). Software can select the one of the four clock sources by application required and switches them on the fly. But software needs to settle the clock source stably before clock switching.

6.4.4. Module Process Clock Control

The CSC module is able to do the process clock enable setting and select the process clock source for internal modules. User must select the module process clock and enable the module process clock before configure the module for operation normal.

6.5. System Common Control

6.5.1. Introduction

The chip embeds one system control (SYS) module for system common control. It is including of one system event interrupt global enable control, chip manufacture identification code.

6.5.2. Features

- System interrupt global enable control for system interrupt source
- Chip manufacture identification code – Device ID, Product ID, User ID

6.6. Memory Access

6.6.1. Introduction

The chip has separate address spaces for program and data memory. The logical separation of program and data memory allows the memory to be accessed by 32bit addresses, which can be quickly stored and manipulated by the CPU. The chip supports one memory controller (MEM) to manage the internal flash memory and SRAM access operation.

6.6.2. Features

❖ **Embedded Memory**

- Built-in embedded 32K bytes flash memory for application code
- Built-in embedded 6K bytes flash memory for ISP code and IAP data
- Built-in embedded max. 2K+128 bytes SRAM

❖ **Memory Controller Features**

- Support ICP (In-circuit program) for ISP boot code update through SWD interface
- Support ISP (In-system program) for application code update
 - Support programmable ISP flash memory size for ISP boot code
- Support IAP (In-application program) for application data update
 - Support programmable IAP flash memory size
- Support flash memory page erase in 512 bytes

6.6.3. Memory Controller

A memory controller is supported to access on chip flash memory, SRAM on AHB bus. It includes **ICP** (In-Circuit Programming)/ **ISP** (In-System Programming)/ **IAP** (In-Application Programming) circuits for flash memory accessing, option byte loader for hardware option registers loading and an external memory bus EMB interface with the capability of accessing external program memory.

The chip has fixed **32K** bytes of embedded main flash memory for application code and data. There is another fixed **6K** bytes of embedded flash memory is shared for In-System-Program (ISP) boot load code and In-Application-Program (IAP) memory. User can adjust the size for the two flash memories. Also the chip has extra 64 bytes of embedded option-byte flash memory for chip configuration.

The memory controller (MEM) supports to Read/ Program (Write)/ Erase the flash memory. User can directly read the data from flash memory by CPU read instruction commands and do not need through any register. For “Program” mode, MEM provides the 32-bit data write operation into flash memory for new data updated. For “Erase” mode, the Erase address is only valid at low 9-bit CPU address=0 (X...XX0 0000 0000B) and is addressing 512-byte alignment. If the low 9-bit address of erased start address is not all '0', this erased process is no effect.

6.6.4. ICP/ISP/IAP for Flash Memory

There are 3 flash access modes are provided in chip for ICP, ISP and IAP application: program mode and read mode. ICP is allowed to update the entire contents of the flash memory by using the hardware SWD interface and no any firmware request. Others, User can use these two modes of ISP and IAP to update new data into flash storage and get flash content by a firmware flash memory access handler.

6.6.5. Hardware Option Byte Flash Memory

There can be up to **64** bytes of on-chip Option Bytes Flash memory. It is used to store the hardware option configuration setting.

The embedded option-byte (**OB**) flash memory will load into the hardware configuration option-byte register (**OR**) after power-on reset. The hardware configuration **OR** are designed to configure the clock source from internal RC oscillator or crystal oscillator; the booted memory selection from AP, ISP flash memory or SRAM; the memory size of IAP flash memory; other chip configurations ... etc.

6.7. GPIO**6.7.1. Introduction**

The chip has following I/O ports: **PA[3:0]**, **PA[7:6]**, **PC0**, **PC[7:2]**. Support maximum **13** GPIO pins for **QFN20** package. **RSTN** pin is an alternated function pin on **PA3**. The exact number of I/O pins available depends upon the package types.

The chip has built in several IO mode control (**PA/PC**) modules for each GPIO port. These modules are used for GPIO pin IO mode control, alternated function selection, driver strength setting, input inverse selection, pull-high enable, deglitch filter setting and high speed enable. Also one IO Port access control (**IOP**) module is built-in to control the input and output state of GPIO mode for all GPIO ports.

6.7.2. Features

- Support general purpose IO pins for application
 - Maximum 13 GPIO pins for QFN20 package
- Provide selectable IO modes by pin independent
 - Push-Pull output
 - Quasi bidirectional
 - Open-drain output
 - Input only with high impedance
 - Analog IO
- Flexible pin alternate function selection
- Support IO deglitch filter by pin independent
- Support input inverse selection by pin independent
- Support pull-high option by pin independent
- GPIO pin state and IO mode setting keep optional after reset

6.7.3. GPIO Control Block

The GPIO Control block includes IOM (IO pad Mode control), IOP (IO Port access control) and AFS (Alternate Function Select) blocks.

- **IO Operation Mode**

The IO operating modes are supported analog IO, digital input, push-pull output, and open-drain output, quasi-bidirectional. Provide selectable IO modes by pin independent.

The IO mode control block supports programmable IO operation modes, output high speed option, pull-high option, output drive strength, IO deglitch filter and input inverse selection by pin independent.

- **IO Port Access**

When the AFS setting is set GPIO function mode for any IO pin, user can directly set the logical output or get the logical input for the IO pin. There is one independent data out register bit to store the output logic value for each GPIO pin. Also user can directly read the input data register bit to get the GPIO pin logical state for each GPIO pin.

For firmware control, there are one set control bit to set the data out register bit and one clear control bit to clear the data out register bit for each GPIO pin.

The chip provides one set-or-clear register control bit to set, clear the data out register bit or read pin status for each GPIO pin. The register bit is written 1 to set data bit and written 0 to clear data. Read the register bit to get the GPIO pin status. As this register bit is cost eight bit memory space, firmware is easy to control single GPIO pin by CPU byte-access instruction command. It is like the bit access IO control of 8051 MCU.

- **Alternate Function Select Control**

User can configure the alternate function between module function IO and IO pins through the AFS matrix for each GPIO pin independently. Usually the AFS default setting is GPIO function for each GPIO pin except the **SWCLK/SWDIO** function pins. These pins may be changed by hardware configuration **OB**.

6.8. Interrupt

6.8.1. Introduction

After reset, the CPU begins execution from the location of reset interrupt vector (0x00000004) addressing, where should be the starting of the user's application code. To service the interrupts, the interrupt service locations (called interrupt vectors) should be located in the address 0x000000BF~0x00000000.

The chip is built-in Arm® cortex M0 CPU and is embedded a NVIC (Nested Vectored Interrupt Controller) for 32 external interrupt inputs with 4-level priority. Also builds in an EXIC (External Interrupt Controller) module and connects to NVIC.

6.8.2. Interrupt Features

- Built-in one NVIC for 32 external interrupt inputs with 4-level priority
- Built-in one EXIC (external interrupt controller) for NVIC connection
 - Independent high/low level and rising/falling edge trigger selection
- Built-in one WIC (wakeup interrupt controller) for wakeup event control

- All GPIO pins can be configured as interrupt source and key pad input
 - Support port OR logic for interrupt function
 - Support port AND logic for KBI function
- Support external pins for CPU NMI/RXEV/TXEV function
 - Configurable pin for CPU NMI input function

6.8.3. Interrupt Structure

Each interrupt is assigned a fixed location in the program memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. NMI interrupt, for example, is assigned to location 0x00000008. If NMI is going to be used, its service routine must begin at location 0x00000008.

The interrupt service locations are spaced at an interval of 4 bytes: 0x00000004 for Reset Interrupt, 0x00000008 for **NMI**, 0x0000000C for **Hard-Fault**, 0x0000002C for **SVCall**, 0x00000038 for **PendSV**, 0x0000003C for **SysTick**, etc.

● Exception types

The NVIC has 7 exception types: **Reset**, **NMI**, **HardFault**, **SVCall**, **PendSV**, **SysTick** and Interrupt (IRQ). The NVIC supports 32 external interrupt input. An interrupt is an exception signaled by a peripheral or generated by a software request. The four priority level interrupt structure allows great flexibility in handling these interrupt sources.

● Interrupt Sources

The 'Pending Bits' are the interrupt flags that will generate an interrupt if it is enabled by setting the 'Set Enable Bit'. The 'Pending Bits' can be set or cleared by software, with the same result as though it had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled in software. The 'Priority Bits' determine the priority level for each interrupt. The 'Priority within Level' is the polling sequence used to resolve simultaneous requests of the same priority level. The 'Vector Address' is the entry point of an interrupt service routine in the program memory.

Table 6-2. Interrupt Source Table

NVIC						Comment
Exception No.	IRQ No.	Interrupt Name	Priority	Activation	Exception handlers	
0	-	Initial	-			
1	-	Reset	-3	Asynchronous		Reset exception
2	-14	NMI	-2	Asynchronous	System handlers	Non Maskable Interrupt
3	-13	HardFault	-1	Synchronous	Fault handler	Cortex-M0 Hard Fault Interrupt
4~10	-	Reserved	-			
11	-5	SVC	Configurable	Synchronous	System handlers	Cortex-M0 SV Call Interrupt
12~13	-	Reserved	-			
14	-2	PendSV	Configurable	Asynchronous	System handlers	Cortex-M0 Pend SV Interrupt
15	-1	SysTick	Configurable	Asynchronous	System handlers	Cortex-M0 System Tick Interrupt
16~47	0~31	-	Configurable	Asynchronous	ISRs	Peripheral Interrupts
Configurable : Programmable priority level 0~3						

● Interrupt Priority

The priority scheme for servicing the interrupts has four interrupt levels. The priority bits in CPU registers, IPR0-7, SHPR2 and SHPR3, determine the priority level of each interrupt.

The interrupt priority registers provide an 8-bit priority field for each interrupt and each register holds four priority fields. The processor implements only bits [7:6] of each field, bits [5:0] read as zero and ignore writes.

Higher-priority interrupt will be not interrupted by lower-priority interrupt request. If two interrupt requests of different priority levels are received simultaneously, the request of higher priority is serviced. If interrupt

requests of the same priority level are received simultaneously, an internal polling sequence determine which request is serviced. The table of “interrupt sources” shows the internal polling sequence in the same priority level and the interrupt vector address. The lower exception number gets the higher priority.

6.8.4. Nested Vectored Interrupt Controller

The Cortex®-M0 processor integrates a configurable Nested Vectored Interrupt Controller (NVIC) that supports low latency interrupt processing and includes a non-mask interrupt (**NMI**). The NVIC provides a zero-jitter interrupt option and four interrupt priority levels.

Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with sleep mode. Optionally, sleep mode support can include a deep sleep function that enables the entire device to be rapidly powered down.

6.8.5. Wakeup Interrupt Controller

The chip includes a Wakeup Interrupt Controller (WIC) which can detect an interrupt or wakeup event from EXIC and wake the processor from deep sleep mode. The WIC is enabled only when the DEEPSLEEP bit in the CPU register of SCR is set to 1. The WIC is not programmable, and does not have any registers or user interface. It operates entirely from hardware signals.

6.8.6. External Interrupt Controller

The External Interrupt Controller (EXIC) includes four external port interrupt blocks (EXINT) to manage the external pin input interrupt events, one wakeup control block for wakeup event control and control the NMI/RXEV events. The EXIC also do as the interface controller between internal modules and NVIC for the interrupt and wakeup events management.

6.9. APB Common Control

6.9.1. Introduction

The chip builds in one APB (APB bus common control) module for the common control of APB devices.

6.9.2. Features

- **Timer synchronous enable global control**

6.9.3. APB Control Block

- **Timer Common Control**

The TMx modules supports two timer enable control bits of **TMx_EN** and **TMx_EN2** to enable the Main timer and 2nd timer separately for each TMx module.

In APB module, there are the same control bits of **APB_TMx_EN** and **APB_TMx_EN2** as the timer enable bits of **TMx_EN** and **TMx_EN2**. These control register bits are built in one 32-bit register and can be enabled or disabled synchronously by setting **APB_TMx_EN** or **APB_TMx_EN2** registers for firmware easy control. (x = Timer module index).

The ITR6 and the ITR7 are used as the common signals of trigger event or clock signal for all timer modules. User can select the trigger source signal by register setting. The **APB_ITR6** and **APB_ITR7** signals can be selected from others TMx timer, URTx, ADC0 modules and EXIC global interrupt events.

6.10. I2C

6.10.1. Introduction

The I2C interface is a two-wire, bi-directional serial bus. It is ideally suited for typical microcontroller applications. The I2C protocol allows the systems designer to interconnect up to 128 different devices using only two bi-directional bus lines, one for clock (SCL) and one for data (SDA). The I2C bus provides control of SDA, SCL generation and synchronization, arbitration logic, and START/STOP control and generation. The only external hardware needed to implement this bus is a single pull-up resistor for each of the I2C bus lines. All devices connected to the bus have individual addresses, and mechanisms for resolving bus contention are inherent in the I2C protocol.

The I2C module builds in the shadow buffer and data register to improve transmit and receive communication performance.

6.10.2. Features

- Provide one I2c modules : I2C0
- Support master and slave mode
- Support programmable clock rate control and clock rate up to 1 MHz
- Support programmable high/low period control for master mode
- Support clock stretching for slave mode
- Support general call function
- Support multi-master processing capability
- Support both Byte mode and Buffer mode flow control
- Support Byte mode bus event code for simplex firmware control
- Support Buffer mode 4-byte data buffer and 32-bit data register for high speed communication
- Support slave address hardware detection wakeup from STOP mode
- Support SMBus timeout detection

6.10.3. I2C Control

- **I2C Data Byte Mode Control**

The module provides one bus event register to get the I2C Event Code for software byte-mode simplex control. An 8-bit shift buffer and an 8-bit data register are used for the I2C data Byte mode.

- **I2C Data Buffer Mode Control**

The module implements an 8-bit shift buffer, a 32-bit shadow buffer and a 32-bit data register for data flow control of data Buffer mode.

- **I2C Master Timing Control**

Two timing control registers are simply used to configure the I2C timing of high and low cycle time.

- **I2C Timeout Timer Control**

The module provides one 8-bit timeout timer (TMO) for I2C access time-out control.

6.11. UART

6.11.1. Introduction

The chip supports the basic UART module. The basic UART module is only supported standard asynchronous communication mode through RX and TX two pins.

6.11.2. Features

- Provide one UART modules : URT4
- UART module common functions
 - Provide precise UART baud-rate control by programmable oversampling rate
 - Support baud rate up to 6 Mbit/s
 - Programmable data word length – 7 or 8 bits
 - Hardware parity checking and parity generation
 - Programmable 4~32 oversampling rate
 - Swappable TX/RX pin configuration
 - Separate signal polarity control for transmission and reception
 - Support TX/RX independent 8-bit data register for simplex firmware control
 - Configurable stop bits – 1 or 2 stop bits

6.11.3. Module Functions

The following table is showing the implemented functions of UART modules.

Table 6-3. UART Module Function Table

Module Functions	Module	URT4	Comment
UART – asynchronous		yes	
Data 7-bit option		yes	
TX parity bit generation		yes	hardware auto generate the parity bit from the data byte
Msb/Lsb transfer option		no	
Configurable stop bits		1, 2	programmable Stop bit length
Programmable over sampling number		4~32	
General timer control		yes	baud-rate timer and timeout timer as general timer
RX parity error detect		yes	checks parity of received data byte
Frame error detect		yes	
Data overrun detect		yes	receive buffer over threshold level; transmit buffer empty
DMA request capability		no	

6.11.4. UART Control

The UART module is able to configure the control mode from one of UART (asynchronous mode), SYNC (synchronous mode), IDLE (multi-processor idle mode) and ADR (multi-processor address-bit mode).

The UART module implements two operation modes of Idle-Line mode or Address-Bit mode for multi-processor communication.

- **UART Data Buffer**

The UART module implements two 8-bit shift buffers and two 8-bit data register for data flow control and reduce the CPU overhead.

- **UART Data Character Format Setting**

The UART character is defined as the data unit for UART transaction. Generally, the character is including of one Start bit, 8-bit or 7-bit data bits and one Stop bit. Others, it also can insert one parity bit (PAR).

- **UART Baud-Rate Control**

The Baud-Rate timer (BR) can configure as an UART Baud-Rate generator or a general using timer. The Baud-Rate timer generator is able to output the internal clock for UART communication Baud-Rate control.

6.12. SPI

6.12.1. Introduction

The chip provides a high-speed serial peripheral interface (SPI). SPI is a full-duplex, high-speed and synchronous communication bus with two operation modes: Master mode and Slave mode. The SPI clock rate can be up to 12 MHz for Master mode and up to 12 MHz for Slave mode under a 24MHz APB clock.

The SPI module builds in the shadow buffer and data register by transmit and receive independently to improve transmit and receive communication performance.

6.12.2. Features

- **Support master and slave mode**
 - Support full duplex , half duplex or simplex communication mode
 - Support data communication without NSS(slave select signal)
 - Support master data input sampling delay half of SPI clock
 - Support slave data output advance half of SPI clock
 - Support configurable idle state for SPI master standard mode data output
 - Support asynchronous clock mode for SPI slave standard mode
- **Support programmable clock rate control**
- **Selectable 8/16/24/32-bit frame size**
 - Support 4-byte data buffer and 32-bit data register for high speed communication
- **Support multi-master processing capability**

- Selectable clock polarity and phase
- Selectable MSB or LSB first data order
- NSS line management by hardware or software for master mode
- Configurable data transfer modes
 - Standard SPI mode (separated transmit and receive line)
 - Single/Dual SPI mode with bidirectional data transfer
- Support DTR (Double Transfer Rate) mode
- Data transmit/receive overrun detect
- Support hardware master mode failure detection and auto slave mode change

6.12.3. Module Functions

The following table is showing the implemented functions of SPI0 modules.

Table 6-4. SPI0 Module Function Table

Module Functions	SPI0	Comment
SPI Standard Mode	Master/Slave	2 data line full-duplex communication
SPI 1/2-Line Mode	yes	1/2 data lines, half-duplex communication
Slave asynchronous mode	yes	Slave mode process with asynchronous clock input
Master data sampling delay	yes	Master data input sampling delay 1/2 SPI clock time
Slave data output advance	yes	Slave data output advance 1/2 SPI clock time for Mode 0,3
Data line copy mode	yes	all data lines with same data for 2 data lines mode
DTR mode	yes	dual transfer rate mode
Swappable MOSI/MISO	yes	
Master mode	yes	
Slave mode	yes	
Msb/Lsb transfer option	yes	
Programmable data bit size	8/16/24/32 bits	
Programmable clock phase and polarity	yes	
Hardware NSS control	yes	control by hardware for both master and slave
NSS pulse mode	yes	optional pulse between two sequent data frame
Programmable NSS pulse width	yes	
Back-to-Back Data Transfer	yes	when NSS pulse disable
Mode fault detect	yes	master mode failure/change detect
Bus Idle detect	yes	slave mode bus idle detect
Receive overrun detect	yes	
Transmit underrun detect	yes	slave mode data transmit underrun
Transmit write error detect	yes	slave mode NSS invalid termination; Bit count error
DMA request capability	no	

6.12.4. SPI Control

● SPI Data Buffer Mode Control

The module implements two 32-bit shift buffers, two 32-bit shadow buffer and two 32-bit data register for data flow control and reduce the CPU overhead.

● SPI Data Frame

User can set the data frame bit size 8/16/24/32-bit by register. Also user can configure the frame data order by Lsb first or Msb first.

● SPI Data Modes

The SPI module provides several data modes and can be configured to one of the modes of standard SPI,

1-Line SPI, 2-Line SPI for flexible SPI application.

6.13. Timer

6.13.1. Introduction

The chip has three Timer/Counter modules: TM00, TM01 and TM36. All of them can be configured as timers or event counters.

TM0x has an 8-bit timer/counter with 8-bit prescaler. TM36 has a 16-bit timer/counter with 16-bit prescaler and embeds four input capture/output compare channels.

6.13.2. Features

- Provide three timers/counters : TM00, TM01, TM36
- Timer module common functions
 - Selectable Full-counter , Cascade , Separate modes
 - Multiple internal and external signals as timer clock source or trigger source
 - Internal timer events output to pin or other modules as input trigger event
 - Support timer reset , trigger start and clock gating for trigger source function
 - Timer overflow as clock output to external pin output
 - Programmable counter auto-stop mode
 - Main counter support up/down control (TM36 only)
 - 2nd counter support up/down control (Separate mode)
- Provide TM36 timer module
 - 32-bit timer/counter
 - 2 CCP (input Capture/output Compare/PWM) channels
 - 2 CCP channels with OCN (complementary output compare)
 - PWM function with center-align, dead time control and break control
 - Support OC comparator split to two separated comparators mode
 - Extra repetition counter for auto-stop mode
 - Support duty capture function
- Provide TM0x timer modules (TM00, TM01)
 - 8-bit timer with 8-bit prescaler

6.13.3. Module Functions

The following table is showing the implemented functions of Timer modules.

Table 6-5. Timer Module Function Table

Module	TM00/01	TM36	
Module Functions			
Timer/Counter total bits	16	32	
Timer Cascade Mode	yes	yes	16-bit_counter+16-bit_prescaler or 8-bit_counter+8-bit_prescaler
Timer Separate Mode	yes	yes	two 16-bit_counter or 8-bit_counter
Timer Full-Counter Mode	yes	yes	32-bit_counter or 16-bit counter
Independent channels		2	
Internal TRGI lines	8	8	
External TRGI lines			external pin input as clock source even internal clock disable
Output TRGO lines (*1)	1	1	support Timer Reset, Enable, Update event, Output state as trigger output
Output CKO lines	1	1	timer overflow as clock output to external pin output
Input Capture IC lines		2	
Output OC/OCN/OCH lines		2/2/0	OCN: complementary outputs, OCH: separated 8-bit compare-high outputs

Input Break lines			Break input to put the timer's output signals in hold state or a known (off) state
PWM separated two		yes	support OC comparator split to two separated Low/High 8-bit comparators mode
PWM edge-align		yes	
PWM center-align		yes	
Dead-time generator		yes	programmable dead-time control
Up/Down of 1 st Timer	U	U/D	Up/down counting
Up/Down of 2 nd Timer	U/D	U/D	Up/down counting
Timer auto Stop	yes	yes	programmable counter auto-stop one pulse mode
Repetition Counter		yes	extra repetition counter for auto-stop mode
QEI timer U/D control			
3-input XOR to CH-0			
Input duty capture		yes	

<Note> *1: It is supported from MF_S1 AFS.

6.13.4. Timer Control Block

The TMx module is including of a Trigger/Clock control block, a Counter Stage, an Capture/Compare control block and Input/Output Stages of channel I/O control (TM36 only) and a Break control block (TM36 only). TMx support three timer operation modes: (1) Cascade Mode (2) Separate Mode (3) Full-Counter Mode.

● Trigger Control Block

The Trigger Control block has two functions, one is to control the timer trigger input events and another is to control the timer trigger output events.

The timer trigger input events are including of Reset Timer, Gated Clock and Timer-Start Trigger for Main Timer and 2nd Timer. The input source of the timer trigger input events is selected from external trigger signal, internal trigger signals or external channel input signal of [TMx_IN0/TMx_IN1](#).

The source of the timer trigger output events are able to come from many internal events or signals of this timer module. Also user can use the software register to set the trigger output directly. This source of output event can select and invert the output signal by registers.

● Timer Input/Output Channels

The following table is showing the channel input signals for each timer module. TM0x modules are no channel input selection function as the input capture/output compare is not support. Each channel has four input lines.

● Timer Input Capture and Output Compare

The input capture (IC) and output compare (OC) functions are only supported for TM36 module. TM0x modules are no the functions of the input capture/output compare.

User can configure each of the timer IC/OC channel independently as input capture, output compare or PWM mode.

● PWM Dead-Time Control

The Dead Time Generator (DTG) is only support for TM36 module. User can use with the DTG function and configure the timer channel as 16bit PWM mode or Two 8bit PWMs mode.

● Break Control Block

The break control block is only support for TM36 module. The module can input the break events from internal events or software register to break the timer output signals.

6.14. ADC

6.14.1. Introduction

The chip builds in one ADC0 module which embeds one 12-bit successive approximation ADC (analog-to-digital converter) and digital logic for output code control. It supports the configurable multiplexed channels those include 4 external and 4 internal sources. The analog-to-digital conversion can be performed in one-shot, continuous, one-loop scan or continuous loop scan modes.

6.14.2. Features

- 12-bit SAR ADC with 250Ksps
 - Configurable resolution : 12/10/8-bit
 - Configurable sampling time
- Provide external 4 channels and internal 4 channels input
 - Internal channel source : VBUF, VSSA , DAC_P0, DAC_P1
- Support auto-sampling and trigger by external pin , internal events and software bit
- Data alignment for output code left/right justify
- Provide internal voltage source VBUF 1.4V
- Interrupt generation at the end of sampling, end of conversion, end of sequence conversion
- Support one-shot/channel scan/loop scan
- Support wait mode
 - Prevents ADC overrun in application with low frequency
- Support auto off mode
 - ADC auto power off except during the active conversion phase

6.14.3. Module Functions

The following table is showing the implemented functions of ADC0 module.

Table 6-6. ADC0 Module Function Table

Module Functions	ADC0	Comment
ADC Bit Resolution	12-bit	
ADC Max. Conversion Rate	250Ksps	
External Input Channels	4	
Internal Input Channels	4	
ADC Reference Top	VDD	
VBUF, AVSS as ADC Input	yes	internal VBG buffer output, ADC ground signal
VCAP Out as ADC Input	-	internal LDO output
DAC Out as ADC Input	yes	internal DAC output
Divided VDD as ADC Input	-	internal 1/2 VDD or 1/4 VDD
PGA with Gain	-	input buffer with gain ratio
Configurable sampling time	0~255	sampling clock time
Channel Scan Conversion	yes	
Hardware accumulators	-	
Voltage Window Detect	-	detect code by the high/low threshold
Output Code Limitation	-	clamp output code or skip the code
Code Left/Right Justify	yes	data alignment for output code
Signed Code Conversion	-	ADC output unsigned code
Wait Mode	yes	
Auto-Off Mode	yes	
ADC Calibration	Offset	
DMA request capability	-	

6.14.4. ADC Control Block

The ADC control block consists of an analog multiplexer (AMUX) with 8 input channels, a **250Ksps/12-bit** SAR (successive-approximation-register) ADC, reference voltage circuit, ADC conversion trigger start control block and change scan control block.

- **ADC Input Channels**

The analog multiplexer (AMUX) selects the inputs to the ADC, allowing any of the input pins to be measured in single-ended mode.

The analog input pins used for the A/D converters also have its I/O pins for digital input and output function. In order to give the proper analog performance, a pin that is being used with the ADC should have its digital output as disabled. It is done by putting the port pin into the input-only mode. And when an analog signal is applied to the **ADC_In** pin and the digital input from this pin is not needed, software could set the corresponding pin to AIO mode to turn off the digital input buffer to reduce current consumption.

- **Single-End Mode**

The ADC supports single-end operation modes. The ADC can convert the ADC output to unsigned code for single-end mode.

- **ADC Sampling Time**

For input signal quality and conversion speedy issue, user can adjust the ADC sampling time. Usually user can increase the ADC sampling time to get more stable voltage and better ADC performance if the conversion rate and signal bandwidth are reasonable and valid for actual application.

- **ADC Conversion Mode**

The ADC is supported three conversion modes of One Shot, Channel Scan and Loop Scan.

- **ADC Output Control**

When an ADC conversion is complete, the ADC raw code is generated and sends to the ADC output control blocks those are including of Digital Offset Adjuster, Digital Resolution Adjuster and Data Alignment Adjuster.

The ADC output code will be adjusted by the ADC output control blocks and store the conversion result data to the ADC data register.

- **ADC Wait and Auto-Off**

The ADC supports a wait mode function to prevent ADC overrun in application with low frequency ADC sampling clock. Also ADC supports an auto off mode function to force the ADC auto entering power-off except during the active conversion phase.

6.15. DAC

6.15.1. Introduction

The chip builds in one DAC module which embeds one 12-bit voltage mode DAC (digital-to-analog converter) and digital logic for input code control. The digital-to-analog conversion can be performed and start trigger by data register written, events (external pin input or internal events).

6.15.2. Features

- **One 12-bit voltage DAC**
 - Maximum conversion rate is 50KSPS
 - Analog output to ADC internal channel
- **Conversion start trigger by register written, external pin and internal events**
- **Build in internal output buffer**

6.15.3. Module Functions

The following table is showing the implemented functions of DAC module.

Table 6-7. DAC Module Function Table

Module Functions	DAC	
DAC Units	2	
DAC Bit Resolution	12	
DAC Type	Voltage	
Output Channels	2	
Max. Conversion Rate	50Ksps	
DAC Reference Top	VDD	
Internal Output Buffer	yes	Build in internal output buffer
Output to ADC	yes	DAC analog output to ADC internal channel
Output to ACMP	-	DAC analog output to ADC internal channel
Output Full Scale	VDD-0.2V	Programmable full-scale output current
Code Left/Right Justify	-	Data alignment for input code left/right justify
Code Width	12-bit	Fixed code width
Output on STOP	yes	Keep DAC output voltage on STOP mode
Conversion start trigger	Reg Written, External pin, Internal events	Conversion start trigger by register written, external pin and internal events
DMA request capability	-	

6.15.4. DAC Control Block

The DAC control block consists of a 50Ksps/**12**-bit voltage mode DAC, reference voltage circuit, a DAC conversion output register (**DAC_DOR0**) and DAC conversion trigger start control block.

The DAC output is programmable to full-scale output voltage from 0.2 volt to VDD-0.2 volt with DAC output buffer on. The voltage DAC output resistive load is minimum 10Kohm with DAC output buffer on.

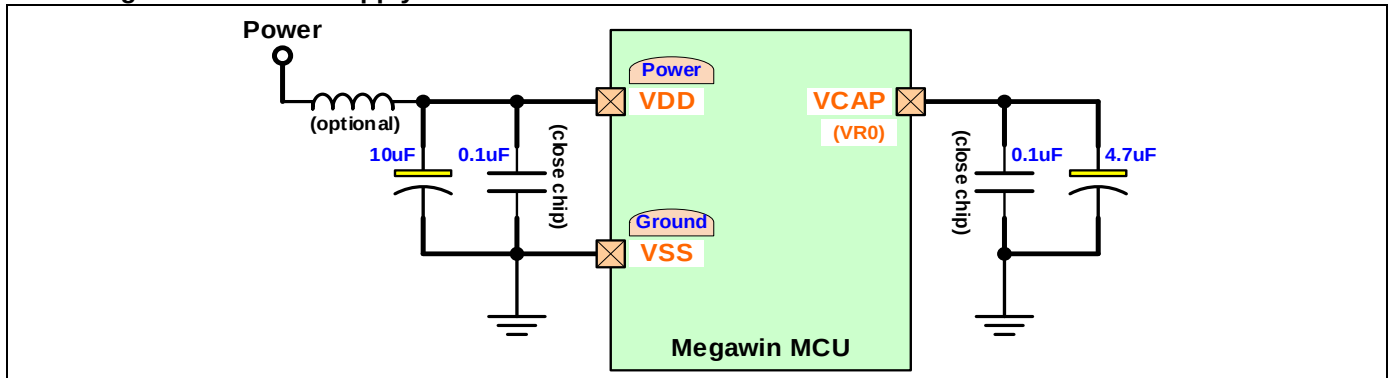
7. Application Notes

7.1. Power Supply Circuit

To have the chip work with power supply varying from 2.7V to 5.5V, adding some external decoupling and bypass capacitors is necessary on **VDD/VSS** power pins, as shown in following figure. The **VCAP** pin is the embedded LDO voltage output as internal core logic power supply. It needs to place one 0.1uF capacitor and one 4.7uF capacitor to be closed the pin.

The following figure is showing the power supply suggestion circuit.

Figure 7-1. Power Supply Circuit



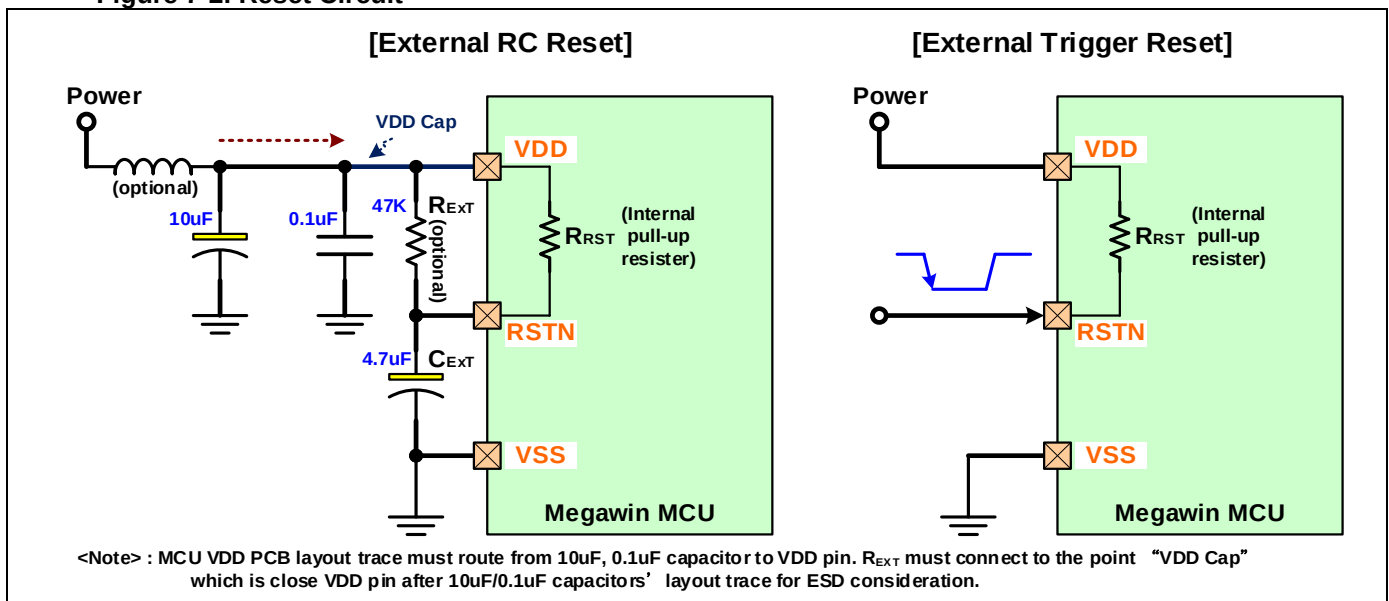
7.2. Reset Circuit

Normally, the power-on reset can be successfully generated during power-up. However, to further ensure the MCU a reliable reset during power-up, the external reset is necessary. The following figure shows the external reset circuit, which consists of a capacitor **C_{EXT}** connected to **VSS** (ground) and a resistor **R_{EXT}** connected to **VDD** (power supply).

In general, **R_{EXT}** is optional because the **RSTN** pin has an internal pull-down resistor (**R_{RST}**). This internal diffused resistor to **VDD** permits a power-up reset using only an external capacitor **C_{EXT}** to **VSS**.

Strongly suggestion, the **RSTN** pin must set to output mode if it is used to do as both chip reset and GPIO functions in application. In this condition, the pin input low may make chip reset locked error if it set to GPIO input mode.

Figure 7-2. Reset Circuit



8. Electrical Characteristics

8.1. Parameter Glossary

Table 8-1. Parameter Glossary

Symbol	Definition	Descriptions
Abbreviations for electrical characteristics		
Min	Minimum value	Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value.
Max	Maximum value	Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value.
Typ	Typical value	Unless otherwise specified, the value is based on TA=25 °C, VDD=5V.
VDD	Power supply voltage	The voltage range is specified in characteristics table or conditions column.
VSS	Power reference voltage	Unless otherwise specified, all voltages are referred to VSS.
TA	Ambient temperature	The temperature range is specified in characteristics table or conditions column.
T_{PC}	Peripheral clock cycle time	The peripheral input clock source may select APB, SYS or other clock. This clock frequency needs lower than 1/2 of the module process clock frequency.

8.2. Absolute Maximum Rating

Table 8-2. Absolute Maximum Rating

Parameter	Rating	Unit
Ambient temperature under bias	-20 ~ +85	°C
Storage temperature	-65 ~ +150	°C
Voltage on any Port I/O Pin or RST with respect to VSS	-0.5 ~ VDD + 0.5	Volt
Voltage on VDD with respect to VSS	-0.5 ~ +6.0	Volt
Maximum total current through VDD and VSS	200	mA
Maximum output current sunk by any I/O pin	20	mA

Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

8.3. DC Characteristics

Table 8-3. DC Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25 °C and execute NOP for each CPU cycle (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
	Current Consumption					
IOP1	ON(normal) mode operating current	TL1 (APB=AHB=32KHz) dhystone		0.11		mA
IOP2		TL2 (APB=AHB=12MHz) dhystone		2.52		mA
IOP3		TL3 (APB=AHB=24MHz) dhystone + IP		7.49		mA
IOP4		TL4 (APB=AHB=24MHz – XTAL) dhystone + IP		8.0		mA

I_{OP5}		TL5 (APB=AHB=24MHz – EXTCK) dhrystone + IP		6.9		mA
I_{OP6}		TL6 (APB=AHB=48MHz) dhrystone + all IP		13.4		mA
I_{SLP0}	SLEEP mode operating current (IWDT Enable)	SL0 (ILRCO on: IWDT Disable, APB=AHB=32KHz)		106		uA
I_{SLP1}		SL1 (IHRCO on: APB/AHB=6MHz/3MHz)		730		uA
I_{SLP2}		SL2 (IHRCO on: APB=AHB=12MHz)		990		uA
I_{SLP3}		SL3 (XTAL=12MHz: APB/AHB=6MHz/3MHz)		1407		uA
I_{SLP4}		SL4 (ILRCO on: APB=AHB=32KHz) with Low Power SLEEP mode		54		uA
I_{STP0}	STOP mode operating current	ST0 (ILRCO off)		3.2		uA
I_{STP1}	(LVR/BOD0/BOD1 disabled)	ST1 (IWDT Enable, ILRCO=32KHz)		4.5		uA
Wakeup Time						
t_{WK_SLP0}	Wakeup from SLEEP mode (Normal SLEEP mode)	IHRCO on, wakeup by IWDT event (RTC Clock= CK_APB= CK_IHRCO)		5	6	T_{PC}
t_{WK_SLP1}	Wakeup from SLEEP mode (Low Power SLEEP mode)	IHRCO/ILRCO on, wakeup by IWDT event (RTC Clock= CK_APB= CK_IHRCO)	40			us
t_{WK_STP0}	Wakeup from STOP mode	ILRCO on, wakeup by IWDT event	16	20		us
BOD Characteristics						
V_{LVR}	LVR detection level (VCAP)	TA = -20°C to +85°C				Volt
I_{LVR}	LVR Current Consumption	TA = 25°C		2.1		uA
V_{BOD10}	BOD1 detection level for 2.4V	TA = -20°C to +85°C				Volt
V_{BOD11}	BOD1 detection level for 2.7V	TA = -20°C to +85°C				Volt
V_{BOD12}	BOD1 detection level for 3.6V	TA = -20°C to +85°C				Volt
V_{BOD13}	BOD1 detection level for 4.2V	TA = -20°C to +85°C				Volt
Operating Condition						
V_{PSR}	Power-on Slope Rate (VDD 10uf + 0.1uf, VCAP 4.7uf + 0.1uf)	TA = -20°C to +85°C	0.05		2.5	V/ms
V_{OP1}	CPU Operating Speed 0–24MHz	TA = -20°C to +85°C	2.7		5.5	Volt

(*1) Data based on characterization results, not tested in production.

T_{PC}: APB clock cycle time, **IP**: internal peripheral modules, **all IP**: all test modules

TL3 ~ TL6: Measure current with IO toggle, **SL4**: Refer the wakeup time **t_{WK_SLP1}** as the low power SLEEP mode

8.4. IO Characteristics

Table 8-4. IO Characteristics

VSS=0V, TA = 25 °C and execute NOP for each CPU cycle (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	Input High voltage	Except RSTN,XIN pins	0.6			VDD
V_{IL}	Input Low voltage	Except RSTN,XIN pins			0.15	VDD
VDD=5.0V						
I_{IH}	Input High Leakage current	V _{PIN} = VDD		0.03	0.1	uA
I_{IL}	Input Low Leakage current	V _{PIN} = 0.4V		0.03	0.1	uA
I_{H2L}	Logic 1 to 0 input transition current (quasi-bidirectional or input mode with on-chip pull-up resistor)	V _{PIN} = 2.2V (V _{IH} voltage)		254	500	uA
I_{OH1}	Output High current (push-pull output mode)	VDD=5.0V, V _{PIN} = 0.85V				mA
I_{OL1}	Output Low current (push-pull output mode)	VDD=5.0V, V _{PIN} = 0.1V				mA
R_{Vweak}	IO pin very weak pull-high resistance			260		Kohm
R_{PU}	IO pin pull-high resistance	Except RSTN		12		Kohm
TR1	IO rising time	C load=30Pf		7.2		ns
TF1	IO falling time	C load=30Pf		5.1		ns
VDD=3.3V						
I_{IH}	Input High Leakage current	V _{PIN} = VDD		0.03	0.1	uA
I_{IL}	Input Low Leakage current	V _{PIN} = 0.4V		0.04	0.1	uA
I_{H2L}	Logic 1 to 0 input transition current (quasi-bidirectional or input mode with on-chip pull-up resistor)	V _{PIN} = 1.6V (V _{IH} voltage)		112	150	uA
I_{OH1}	Output High current (push-	VDD=3.3V, V _{PIN} = 2.4V				mA

MG32F02D032

	pull output mode & High sink level)					
I_{OL1}	Output Low current (push-pull output mode & High sink level)	VDD=3.3V, V _{PIN} = 0.4V				mA
R_{Vweak}	IO pin very weak pull-high resistance			420		Kohm
R_{PU}	IO pin pull-high resistance	Except RSTN		16.2		Kohm
TR1	IO rising time	C load=30Pf		10.5		ns
TF1	IO falling time	C load=30Pf		6.3		ns
VDD=2.7V						
I_{IH}	Input High Leakage current	V _{PIN} = VDD		0.01	0.1	uA
I_{IL}	Input Low Leakage current	V _{PIN} = 0.4V		0.03	0.1	uA
I_{H2L}	Logic 1 to 0 input transition current (quasi-bidirectional or input mode with on-chip pull-up resistor)	V _{PIN} = 1.1V (V _{IH} voltage)		26	50	uA
I_{OH1}	Output High current (push-pull output mode & High sink level)	VDD=1.8V, V _{PIN} = 1.4V				mA
I_{OL1}	Output Low current (push-pull output mode & High sink level)	VDD=1.8V, V _{PIN} = 0.4V				mA
R_{Vweak}	IO pin very weak pull-high resistance			1100		Kohm
R_{PU}	IO pin pull-high resistance	Except RSTN		65		Kohm
TR1	IO rising time	C load=30Pf		19.1		ns
TF1	IO falling time	C load=30Pf		13.5		ns

8.5. IHRCO Characteristics

Table 8-5. IHRCO Characteristics

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Voltage		2.7	5.0	5.5	Volt
IHRCO0 Frequency	TA = +25°C		24		MHz
	TA = +25°C	-1.0		+1.0	%

IHRCO0 Frequency Deviation (factory calibrated) (VCAP= 1.5V~1.65V)	TA = -20°C to +85°C				%
IHRCO Start-up Time	TA = +25°C			5(*1)	us
IHRCO Current Consumption	TA = +25°C, VDD=5.0V		0.45		mA

(*1) Data based on characterization results, not tested in production.

8.6. ILRCO Characteristics

Table 8-6. ILRCO Characteristics

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Voltage		2.7	5.0	5.5	Volt
ILRCO Frequency	TA = +25°C		32		KHz
ILRCO Frequency Deviation (factory calibrated)	TA = +25°C, VDD=5.0V	-4		+4	%
	TA = -20°C to +85°C	-30		+30	%
ILRCO Current Consumption	TA = +25°C, VDD=5.0V		1		uA
Output Duty	TA = +25°C, VDD=5.0V	45	50	55	%

(1) Data based on characterization results, not tested in production.

8.7. LDO Characteristics

Table 8-7. LDO Characteristics

VDD=5.0V±10%, VSS=0V, TA = -20°C ~ +85 °C

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
VDD	Supply Voltage	Normal Mode, IOU T =20Ma	2.7	5.0	5.5	V
General						
VCAP	LDO Output Voltage (VCAP pin)	ON(Normal) mode	1.52	1.57	1.62	Volt
		Low power mode, IOU T =100Ua, VDD=2.7V~5.5V, TA = -20℃ ~ +85℃		1.37		Volt
IQ	Current	VDD=2.7V~5.0V, Temp.= 25℃, Normal Mode		30		uA
		VDD=2.7V~5.0V, Temp.= 25℃, Low Power Mode		1		uA
		VDD=2.7V~5.0V, Temp.= -20℃ ~ +85℃				uA
VDROP	Dropout Voltage (VDD-VCAP)	IOU T =10Ma, VDD=2.7V~5.5V				mV

MG32F02D032

		(VCAP =1.57V +/-5%)				
IOUT	Max output current	VDD=5.0V (VCAP voltage variation < ±5%)	20			mA
		VDD=3.6V (VCAP voltage variation < ±5%)	20			mA
		VDD=2.7V (VCAP voltage variation < ±5%)	20			mA

(1) Data based on characterization results, not tested in production.

8.8. LVR Characteristics

Table 8-8. LVR Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25 °C

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Range					
Supply Voltage		2.7	—	5.5	V
General					
LVR Operation current	Only LVR turn on		6		uA
Power down current					uA
Target LVR voltage	Falling		1.95		V
	Rising		2.00		V
Detected voltage error	The trim target is LVR level				mV
LVR temperature coefficient of detected voltage	-20℃ ~ +85℃				%

8.9. BOD1 Characteristics

Table 8-9. BOD1 Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25 °C

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Range					
Supply Voltage		2.7	—	5.5	V
General					
Operation current (BOD1 + BOD2)			7		uA
Power down current					uA
Detected voltage error					mV
Detect voltage (-20℃ ~ 85℃)	2.4V		2.4		V
	2.7V		2.7		V
	3.6V		3.6		V
	4.2V		4.2		V
Detect hysteresis window	2.4V				mV
	2.7V				mV
	3.6V				mV
	4.2V				mV
Temperature coefficient of detected voltage	-20℃ ~ +85℃				%

8.10. Flash Characteristics

Table 8-10. Flash Characteristics

VDD=5.0V±10%, VSS=0V, TA = -20°C ~ +85 °C

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Voltage		2.7		5.5	Volt
Flash Write (Erase/Program) Voltage		2.7		5.5	Volt
Flash Erase/Program Cycle		20000			Times
Flash Data Retention	TA = +25°C	100			Year
Flash Chip Erase Time		20		40	ms
Flash Page Erase Time		4		5	ms
Flash Program Time	Program one 32-bit			50	µs

8.11. ADC Characteristics

Table 8-11. ADC Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C, C_{LOAD}=10Pf, Gain=x1 (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
VDDA	Analog Supply Voltage		2.7	5.0	5.5	Volt
IADC_ON	Operation Current – normal					uA
IADC_OFF	Operation Current – power-down					uA
ADC Static Parameters						

Bits	Resolution				12	bits
INL	Integral nonlinearity (INL)	VREF = 5V, VDD = 5V, 250Ksps Conversion Rate (sampling clock = 6 MHz/24 clocks)	-1.8		1.8	LSB
INL	Integral nonlinearity (INL)	VREF = 5V, VDD = 5V, 200Ksps Conversion Rate (sampling clock = 6 MHz/30 clocks)	-1.95		7	LSB
DNL	Differential nonlinearity (DNL)	VREF = 5V, VDD = 5V, 250Ksps Conversion Rate (sampling clock = 6 MHz/24 clocks)	-1		1.5	LSB
DNL	Differential nonlinearity (DNL)	VREF = 5V, VDD = 5V, 200Ksps Conversion Rate (sampling clock = 6 MHz/30 clocks)	-1		1.0	LSB
E _{OFFSET}	Offset error	VREF = 5V, VDD = 5V, 250Ksps Conversion Rate (sampling clock = 6 MHz/24 clocks)	1.6		2.7	LSB
E _{OFFSET}	Offset error	VREF = 5V, VDD = 5V, 200Ksps Conversion Rate (sampling clock = 6 MHz/30 clocks)	1.1		2.4	LSB
E _{FS}	Full scale error	VREF = 5V, VDD = 5V, 250Ksps Conversion Rate (sampling clock = 6 MHz/24 clocks)	-11		-7	LSB
E _{FS}	Full scale error	VREF = 5V, VDD = 5V, 200Ksps Conversion Rate (sampling clock = 6 MHz/30 clocks)	-11		-7	LSB

ADC Input and DC Characters						
V_{AIN}	ADC input voltage range	VDDA ≥ 4.0V	0.2		VDD-0.2	Volt
		VDDA < 4.0V	0.3		VDD-0.3	Volt
C_{LOAD}	Input capacitance					pF
V_{BUF}	Internal VBUF reference voltage	25 °C		1.40		Volt
	Internal VBUF reference voltage spread over the temperature range	-20 °C < < 85 °C V _{BUF} = 1.40V at 25°C	-7		8	mV
T_{VBUF}	Dynamic Stable time			2.85		us
T_{ADEN}	ADC enable stable time					us
ADC Conversion Parameters						
F_s	Sampling clock	24 clocks/One Conversion			6	MHz
		30 clocks/One Conversion			6	MHz
F_{conv}	Conversion rate	VDDA = 5.5 ~ 2.7 V			250	Ksps
T_{conv}	Conversion time in conversion clock (not including acquisition time)	ADC0_CONV_TIME=0		24		clocks
		ADC0_CONV_TIME=1		30		clocks

8.12. DAC Characteristics

Table 8-12. DAC Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C, TT case

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
VDDA	Analog Supply Voltage	VDD = 2.7V~5.5V	2.7		5.5	Volt
DAC Static Parameters						
	Resolution				12	bits
DNL	Differential nonlinearity (DNL)	DAC Buffer ON	-1.8		0.8	LSB
INL	Integral nonlinearity (INL)	DAC Buffer ON	-2		3.5	LSB
E _{OFFSET}	Offset error	DAC Buffer ON	-0.001		0.005	LSB
E _{GAIN}	Gain error (% of Full scale)	DAC Buffer ON	-0.001		0.001	%
ENOB	Effective Number Of Bits (ENOB)			10		LSB
	DAC DC Character					
FSR	Full scale range	DAC Buffer ON	0.2		VDD-0.2	Volt
R _{LOAD}	Resistive load with buffer ON		10			Kohm
R _o	Resistive load with buffer OFF	VDD=2.4V		TBD		Kohm
		VDD=3.3V		TBD		Kohm
		VDD=5.5V		TBD		Kohm
C _{LOAD}	Capacitive load				30	pF
I _{DAC}	DAC operation current	DAC Buffer ON		TBD		mA
I _{BUF}	DAC output buffer current	DAC Buffer ON		0.50		mA

I_{OFF}	DAC power-down current			TBD		uA
DAC Conversion Parameters						
F_{CONV}	Conversion Rate	C _{LOAD} ≤ 30 Pf, R _{LOAD} ≥ 10 KΩ DAC output change from input code I to i+1 LSB			50	Ksps
T_{SETTLING}	Settling Time	C _{LOAD} ≤ 30 Pf, R _{LOAD} ≥ 10 KΩ DAC output change from input code I to i+1 LSB		TBD		ns
		C _{LOAD} ≤ 30 Pf, R _{LOAD} ≥ 10 KΩ Input code transition between the lowest and the highest input codes when DAC output reaches final value +/- 1 LSB		TBD		us
T_{START}	Startup time after DAC ON			TBD		us

8.13. UART Characteristics

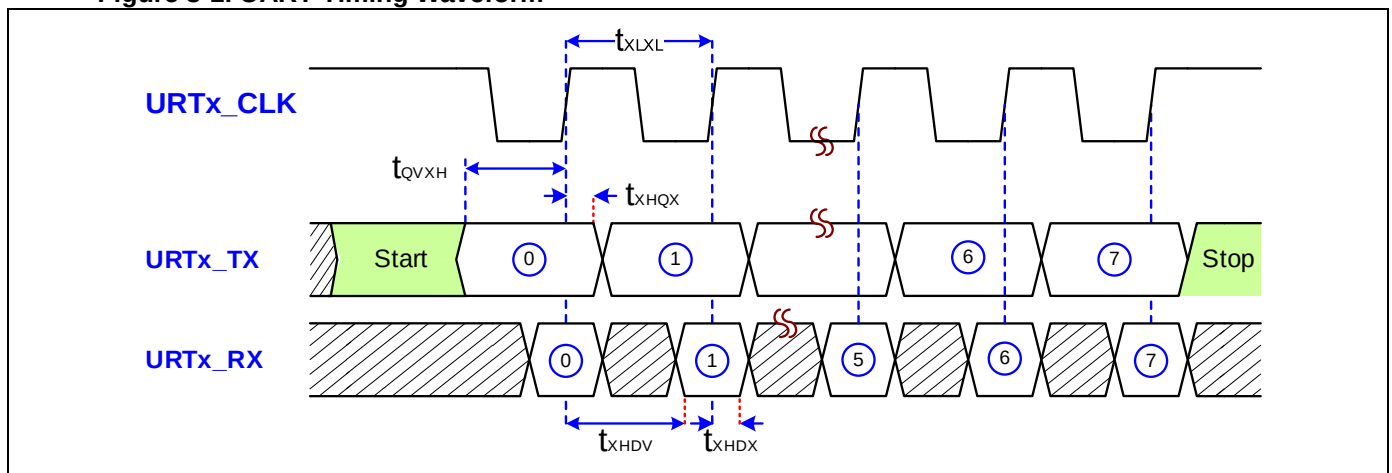
Table 8-13. UART Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
UART Mode						
f _{CK}	Serial Port Clock Frequency				6	MHz
t _{XLXL}	Serial Port Clock Cycle Time		4			T _{PC}
t _{QVXH}	Output Data Setup to Clock Rising Edge		T _{PC} -20			ns
t _{XHQX}	Output Data Hold after Clock Rising Edge		T _{PC} -10			ns
t _{XHDX}	Input Data Hold after Clock Rising Edge		0			ns
t _{XHDV}	Clock Rising Edge to Input Data Valid				T _{PC} -20	ns

T_{PC} : APB clock or SYS clock cycle time

Figure 8-1. UART Timing Waveform



8.14. SPI Characteristics

Table 8-14. SPI Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Master Mode						
f _{MCK}	SPI Clock Frequency	VDD=2.7V ~ 5.5V			12	MHz
T _{mckh}	SPI Clock High Time		2			T _{PC}
T _{mckl}	SPI Clock Low Time		2			T _{PC}
T _{mis}	D _{IN} Valid to SPI Clock Shift Edge		2T _{PC} +20			ns
T _{mih}	SPI Clock Shift Edge to D _{IN} Change		0			ns
T _{moh}	SPI Clock Shift Edge to D _{OUT} Change				10	ns
Slave Mode						
f _{SCK}	SPI Clock Frequency	VDD=2.7V ~ 5.5V, Asynchronous clock mode			12	MHz
		VDD=2.7V ~ 5.5V, Synchronous clock mode			8	MHz
t _{SE}	NSS Falling to First SPI Clock Edge		2			T _{PC}
t _{SD}	Last SPI Clock Edge to NSS Rising		2			T _{PC}
t _{SEZ}	NSS Falling to D _{OUT} Valid				4	T _{PC}
t _{SDZ}	NSS Rising to D _{OUT} High-Z				4	T _{PC}
t _{CKH}	SPI Clock High Time		3			T _{PC}
t _{CKL}	SPI Clock Low Time		3			T _{PC}
t _{sis}	D _{IN} Valid to SPI Clock Sample Edge		2			T _{PC}
t _{sih}	SPI Clock Sample Edge to D _{IN} Change		2			T _{PC}
t _{soh}	SPI Clock Shift Edge to D _{OUT} Change				4	T _{PC}
t _{SLH}	Last SPI Clock Edge to D _{OUT} Change (CPHA = 1 only)		1		2	T _{PC}

T_{PC} : APB clock or SYS clock cycle time

D_{IN} : SPI input data signal

D_{OUT} : SPI output data signal

Figure 8-2. SPI Master Timing Waveform

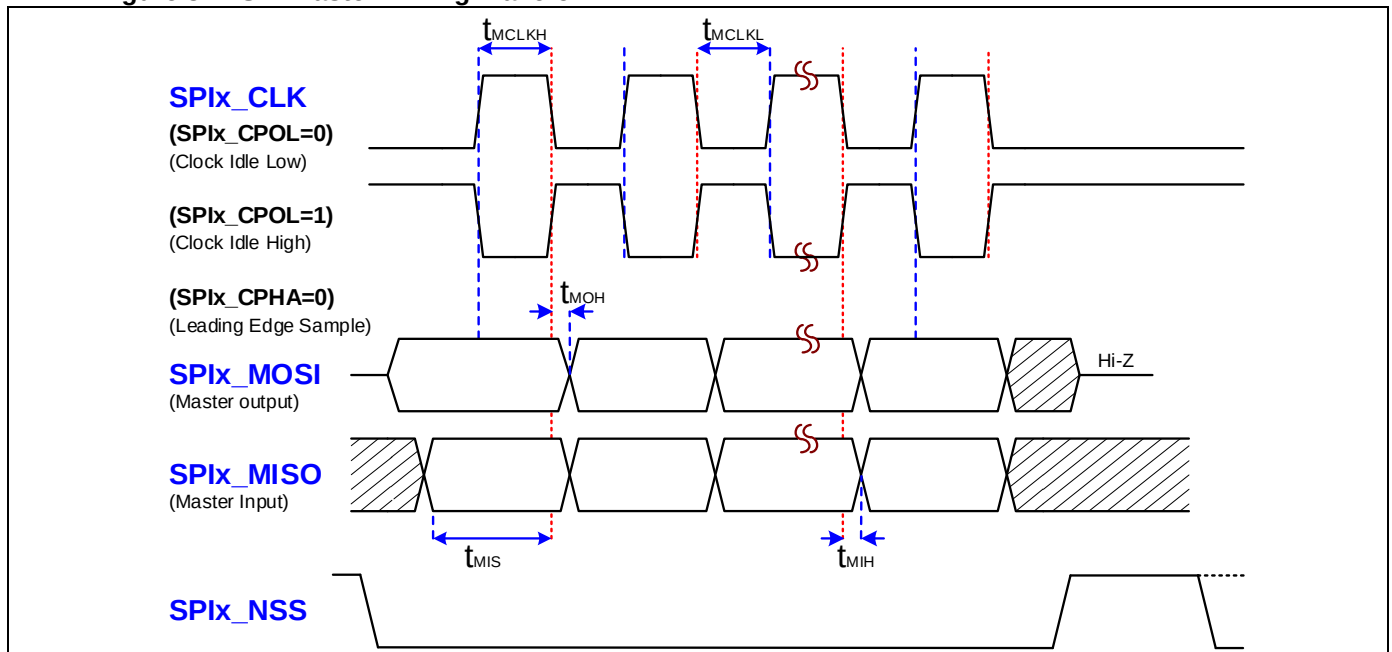
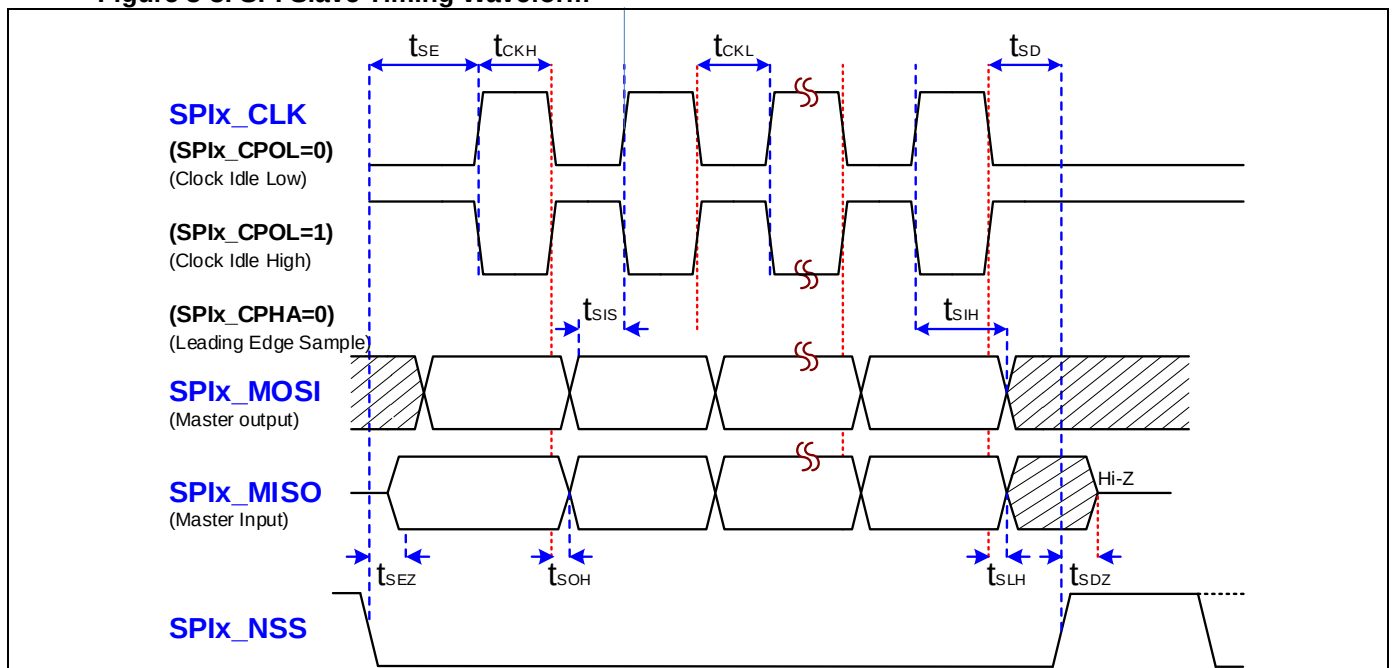


Figure 8-3. SPI Slave Timing Waveform



8.15. I2C Characteristics

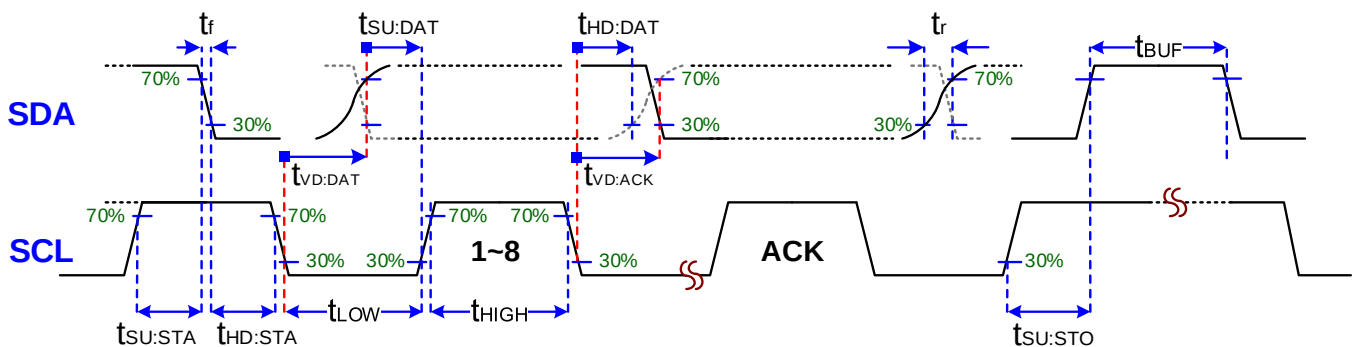
Table 8-15. I2C Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
f _{SCL}	SCL Clock Frequency		0	100	0	400	0	1000	KHz
t _{Low}	Low period of the SCL clock		4.7		1.3		0.5		us
t _{Low_M}	Low period of the SCL clock (Master Mode)		2		2		2		T _{PC}
t _{Low_S}	Low period of the SCL clock (Slave Mode)		4		4		4		T _{PC}
t _{High}	High period of the SCL clock		4.0		0.6		0.26		us
t _{High_M}	High period of the SCL clock (Master Mode)		3		3		3		T _{PC}
t _{High_S}	High period of the SCL clock (Slave Mode)		5		5		5		T _{PC}
t _{HD;STA}	Hold time for START condition		4.0		0.6		0.26		us
t _{SU;STA}	Setup time for START condition		4.7		0.6		0.26		us
t _{HD;DAT}	Data hold time		0		0		0		us
t _{SU;DAT}	Data setup time		250		100		50		ns
t _{SU;STO}	Setup time for STOP condition		4.0		0.6		0.26		us
t _{BUF}	Bus free time between a STOP and START		4.7		1.3		0.5		us
t _{VD;DAT}	Data valid time			3.45		0.9		0.45	us
t _{VD;ACK}	Data valid acknowledge time			3.45		0.9		0.45	us
t _r	Rise time of both SDA and SCL signals			1000		300		120	ns
t _f	Fall time of both SDA and SCL signals			300	20x (VDD/5.5V)	300	20x (VDD/5.5V)	120	ns
C _i	Capacitive load for each IO pin			10		10		10	pF

T_{PC} : APB clock or SYS clock cycle time

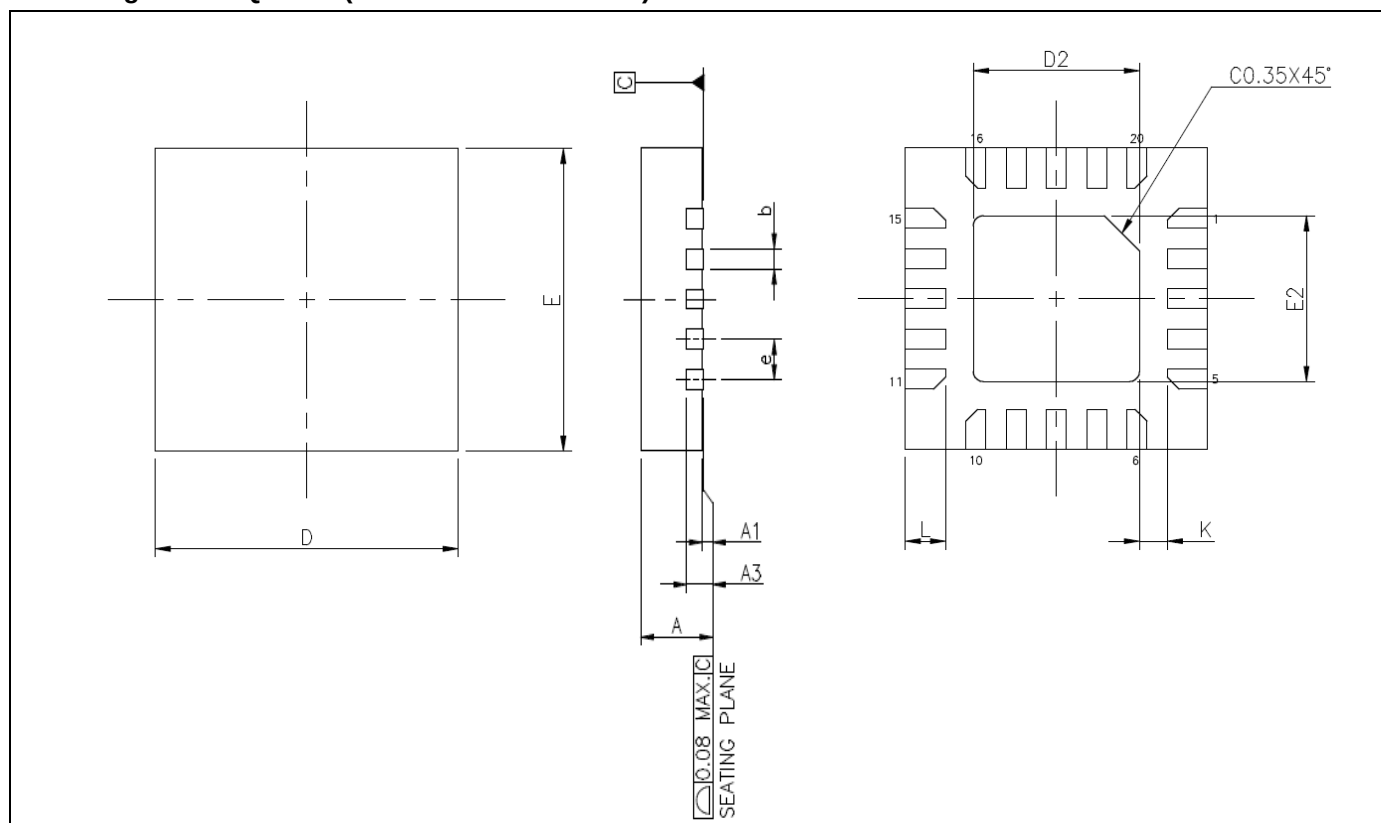
Figure 8-4. I2C Timing Waveform



9. Package Dimension

9.1. QFN-20 (3x3x0.75)

Figure 9-1. QFN-20 (3mm X 3mm X 0.75mm) ~ AZ20



Unit	mm			inch		
JEDEC	MO-220			MO-220		
PKG	WQFN(X319)			WQFN(X319)		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	0.02	0.05	0.000	0.000	0.001
A3	0.203 REF.			0.007 REF.		
b	0.15	0.20	0.25	0.005	0.007	0.009
D	3.00 BSC			0.118 BSC		
E	3.00 BSC			0.118 BSC		
e	0.40 BSC			0.015 BSC		
L	0.30	0.40	0.50	0.011	0.015	0.019
K	0.20	---	---	0.007	---	---
D2	1.60	1.65	1.70	0.062	0.064	0.066
E2	1.60	1.65	1.70	0.062	0.064	0.066

10. Revision History

Revision v0.06 (2026_0921)		Chapter
1	Modify 'Operating temperature ' of Features.	Features
2	Modify 'Operating temperature ' of Table 2-1.	Table 2-1.
3	Modify 'Ambient temperature under bias' rating	Table 8-2
4	Modify 'LVR temperature coefficient of detected voltage' conditions.	Table 8-9
5	Modify 'Temperature coefficient of detected voltage' conditions.	Table 8-10
6	Modify 'Internal VBUF reference voltage spread over the temperature range' conditions.	Table 8-12
7	Delete "External Clock Characteristics" chapter.	8-5
8	Modify "LDO Characteristics"'s TA temperature.	8-8
9	Modify "LDO Output Voltage (VCAP pin)" conditions.	Table 8-8
10	Modify "current" conditions.	Table 8-8
11	Modify "Flash Characteristics"'s TA temperature.	8-10
12	Modify "BOD Characteristics" conditions.	Table 8-3
13	Modify "Operating Condition " conditions.	Table 8-3
14	Modify "IHRCO0 Frequency Deviation (factory calibrated) (VCAP= 1.5V~1.65V)" conditions.	Table 8-6
15	Modify "ILRCO Frequency Deviation (factory calibrated)" conditions.	Table 8-7
16	Modify "Detect voltage" parameters.	Table 8-10
17	Modify from "AY20" to "AZ20"	Figure 9-1
18	Modify "Part Number List" that from "AY20" to "AZ20".	2
19	Delete "4.1.2 LQFP32 Package Pinout" chapter.	4.1.2
20	Delete GPIO LQFP32 package	Features
21	Delete LQFP32 Package tyoes	Features
22	Delete Package (LQFP32)	Table 2-1
23	Delete "MG32F02D032AD32 : LQFP32 (7mm x 7mm), 32KB Flash"	2
24	Delete LQFP32 column.	Table 4-3
25	Delete "LQFP32" package.	6.7.1
26	Delete "LQFP32" package.	6.7.2
27	Delete " LQFP-32" chapter.	9.2
28	Delete "LQFP" & "32" item	Figure 2-1
29	Modify from "AY20" to "AZ20"	Figure 2-1
Revision v0.05 (2026_0414)		Chapter

1	Modify BOD1 detect level.	Features
2	Modify BOD1 detect level.	Table 2-1
3	Modify BOD1 detect level.	6.2.2
4	Modify BOD1 detection level.	Table 8-3
5	Modify BOD1 Detect Voltage & Detect hysteresis window.	Table 8-10
Revision v0.04 (2026_0401)		Chapter
1	Add LQFP32 in GPIO of Features.	Features
2	Add LQFP32 in Package Types if Features	Features
3	Add LQFP32 in Table 2-1 in Part Number List	Table 2-1
4	Add LQFP32 package.	4.1.1
5	Add LQFP32 package dimension	9.2
6	Add LQFP32 Pin number in Table 4-3.	Table 4-2
7	Modify QFN20 Pin number in Table 4-3.	Table 4-2
8	Modify Table 8-12. ADC Characteristics	Table 8-12
9	Modify Table 8-13. DAC Characteristics	Table 8-13
Revision v0.03 (2026_0312)		Chapter
1	Modify QFN20 pin.	4.1.1
Revision v0.02 (2026_0310)		Chapter
1	Add QFN20 middle pad.	4.1.1
Revision v0.01 (2025_1209)		Chapter
1	Preliminary version for internal	

11. Disclaimers

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