

# **MG32F02A128 MG32F02A064**

## **Data Sheet**

**Version: 1.31**



## Features

### ❖ CPU Core

- ARM 32-bit Cortex-M0 CPU
- Operation frequency up to 48MHz
- Built-in one NVIC for 32 external interrupt inputs with 4-level priority
- Built-in one 24-bit system tick timer
- Built-in one single-cycle 32-bit multiplier
- Built-in one SWD serial wire debugger with 2 watch points and 4 breakpoints

### ❖ Flash Memory

- Built-in embedded max. 128K bytes flash memory for application code
- Support ICP (In-circuit program) for ISP boot code update through SWD interface
- Support ISP (In-system program) for application code update
  - Support programmable ISP flash memory size for ISP boot code
- Support IAP (In-application program) for application data update
  - Support programmable IAP flash memory size

### ❖ SRAM Memory

- Built-in embedded max. 16K bytes SRAM
  - Support private 2K bytes for DMA and 14K bytes for software to improve access performance

### ❖ Power

- Built-in one embedded regulator for core logic power
- Built-in brown-out detectors
  - BOD0 detect 1.4V
  - BOD1 detect by selected level 4.2V/3.7V/2.4V/2.0V
  - BOD2 detect 1.7V
- Built-in a power management controller with power-down and wakeup control
- Support three power operation modes
  - ON(Normal) mode and SLEEP , STOP power down modes
- Support wake-up from SLEEP/STOP modes via multiple sources

### ❖ Reset

- Built-in embedded POR (power-on reset) circuit
- Built-in one reset source controller
  - Programmable chip cold reset and warm reset for reset source
  - Independent software reset control for internal modules
- Provide multiple reset source
  - POR/BOD/External reset pin input/Software force reset
  - IWDG/WWDT/ADC/Analog Comparator
  - Illegal address error reset/Flash access protect error reset
  - Missing clock detect (MCD) reset

### ❖ Clock

- Built-in embedded ILRCO (internal low frequency RC oscillator) by 32KHz
- Built-in embedded IHRCO (internal high frequency RC oscillator)
  - Trimmed to 11.059 or 12MHz  $\pm 1\%$  at +25°C
- Built-in embedded PLL clock output for system clock
- Built-in embedded XOSC oscillator with MCD for external 32KHz and 4 ~ 25MHz Xtal
- Support external clock input up to 36MHz
- Built-in a clock source controller with independent clock enable control for modules
- Support internal XOSC oscillator and internal ILRCO/IHRCO clock output

### ❖ DMA (Direct Memory Access)

- **5 independently configurable channels with dedicated hardware DMA requests**
  - Access to Memory, APB and AHB Peripherals as source and destination
  - Support SRAM/Flash/EMB as memory source and SRAM/EMB as memory destination
- **DMA transfer management type**
  - memory-to-memory (channel 0,3 only)
  - peripheral-to-memory
  - memory-to-peripheral
  - peripheral-to-peripheral
- **Built-in two type of priority control between channel requests**
  - Channel request by Round Robin
  - Software configurable priority level
- **Programmable transfer number of data and up to 131072**
- **Programmable burst length 1,2,4**
- **Support transfer loop mode and start address auto reload control**
- **Provide single/block/demand mode for external pin trigger request**

### ❖ GPIO

- **Support general purpose IO pins for application**
  - Maximum 73 GPIO pins for LQFP80 package
  - Maximum 59 GPIO pins for LQFP64 package
  - Maximum 44 GPIO pins for LQFP48 package
- **Provide selectable IO modes by pin independent**
  - Push-Pull output
  - Quasi bidirectional (PC pins only)
  - Open-drain output
  - Digital Input with high impedance
  - Analog IO
- **Flexible pin alternate function selection**
- **Support programmable drive strength by pin independent**
- **Support IO deglitch filter by pin independent**
- **Support input inverse selection by pin independent**
- **Support pull-high option by pin independent**
- **Support high speed option by pin independent except RSTN, XIN**
- **GPIO pin state and IO mode setting keep optional after reset**

### ❖ Interrupt Support

- **Built-in one EXIC (external interrupt controller) for NVIC connection**
  - Independent high/low level and rising/falling edge trigger selection
- **Built-in one WIC (wake up interrupt controller) for wakeup event control**
- **All GPIO pins can be configured as interrupt source and key pad input**
  - Support port OR logic for interrupt function
  - Support port AND logic for KBI function
- **Support external pins for CPU NMI/RXEV/TXEV function**

### ❖ Timer

- **Provide seven timers/counters : TM00,TM01,TM10,TM16,TM20,TM26,TM36**
- **Timer module common functions**
  - Selectable Full-counter, Cascade, Separate timer operation modes
  - Multiple internal and external signals as timer clock source or trigger source
  - Support timer reset, trigger start and clock gating for trigger source function
  - Timer overflow as clock output to external pin output
  - Auto-stop mode by main counter counting
- **Provide TM36 timer module**

- 32-bit timer/counter
- 4 CCP (input Capture/output Compare/PWM) channels
- 3 CCP channels with OCN (complementary output compare)
- PWM function with center/edge-align, dead time control and break control
- QEI(Quadrature Encoder Interface) support
- One IC and three OC with DMA capability
- Extra repetition counter for auto-stop mode
- **Provide TM2x timer modules (TM20,TM26)**
  - 32-bit timer/counter
  - 2 CCP (input Capture/output Compare/PWM) channels
  - 2 CCP channels with OCN (complementary output compare)
  - PWM function with edge-align
  - QEI(Quadrature Encoder Interface) support(TM26 only)
  - Extra repetition counter for auto-stop mode
- **Provide TM1x timer modules (TM10,TM16)**
  - 32-bit timer/counter
- **Provide TM0x timer modules (TM00,TM01)**
  - 16-bit timer/counter

#### ❖ RTC

- **Built-in 32-bit counter with selectable clock source**
- **Support alarm function and time-stamp function**
- **Support wakeup from STOP mode**
- **Support periodic timer tick interrupt or wakeup**

#### ❖ Watchdog Timer

- **Built-in one IWDG (Independent Watch Dog Timer)**
  - 8-bit down counter with 12-bit prescaler and clocked by ILRGO clock
  - Operating capability in SLEEP and STOP modes
  - Selectable reset or interrupt when the counter underflow
  - Support two early wakeup comparators with interrupt
- **Built-in one WWDG (Window Watch Dog Timer)**
  - 10-bit counter with 1 or 256 divider , 1/2/4~128 divider
  - Configurable time-window to detect abnormally late or early application behavior
  - Selectable reset or interrupt when the counter is underflow or reloaded outside the window
  - Support warning interrupt

#### ❖ I2C

- **Provide two identical I2c modules : I2C0 , I2C1**
- **I2C module common functions**
  - Support master and slave mode
  - Support programmable clock rate control and clock rate up to 1 MHz
  - Support programmable high/low period control for master mode
  - Support clock stretching for slave mode
  - Support general call function
  - Support multi-master processing capability
  - Support both Byte mode and Buffer mode flow control
  - Support Byte mode bus event code for simplex firmware control
  - Support Buffer mode 4-byte data buffer and 32-bit data register for high speed communication
  - Received and transmitted data are buffered with DMA capability
  - Support slave address hardware detection wakeup from STOP mode
  - Support SMBus timeout detection

## ❖ UART

- Provide seven UART modules : URT0~2, URT4~7
- UART module common functions
  - Provide precise UART baud-rate control by programmable oversampling rate
  - Support baud rate up to 6 Mbit/s
  - Programmable data word length - 7 or 8 bits
  - Programmable 4~32 oversampling rate
  - Hardware parity checking and parity generation
  - Swappable TX/RX pin configuration
  - Separate signal polarity control for transmission and reception
- Provide URT0/1/2 advanced UART module
  - Support UART, Synchronous, SPI master/slave, SmartCard, LIN, Multi-processor modes
  - Selectable MSB or LSB first data order
  - Configurable stop bits - 0.5,1,1.5 or 2 stop bits
  - Support a timeout timer for Idle/RX/Break/Calibration timeout detection
  - Support 4-byte data buffer and 32-bit data register for high speed communication
  - Support auto baud-rate detection and calibration
  - Support multiprocessor communication for master and slave mode - Idle-Line , Address-Bit
  - Support low speed UART-like frame format IrDA
  - Support transceiver hardware flow control by CTS/RTS signals only
  - Provide driver enable signal to activate the transmission for bidirectional communication
  - Support transmission-error hardware detection and auto resent control for Smart-card application
  - Support receiving parity error hardware detection and auto retry control for Smart-card application
  - Received and transmitted data are buffered with DMA capability
- Provide URT4/5/6/7 basic UART modules
  - Support fundamental UART mode
  - Support TX/RX independent 8-bit data register for simplex firmware control
  - Configurable stop bits - 1 or 2 stop bits

## ❖ SPI

- Provide four modules for SPI communication: SPI0, URT0, URT1, URT2
  - Provide one advanced SPI module: SPI0
  - Provide three configurable SPI modules: URT0, URT1, URT2 (Refer to UART features)
- Support master and slave mode
  - Support full duplex , half duplex or simplex communication mode
  - Support data communication without NSS(slave select signal)
- Support programmable clock rate control
- Selectable 4~32-bit frame size
  - Support 4-byte data buffer and 32-bit data register for high speed communication
- Received and transmitted data are buffered with DMA capability
- Support multi-master processing capability
- Selectable clock polarity and phase
- Selectable MSB or LSB first data order
- NSS line management by hardware or software for master mode
- Configurable data transfer modes
  - Standard SPI mode (separated transmit and receive line)
  - Single/Dual/Quad/Octal SPI mode with bidirectional data transfer
- Data transmit/receive overrun detect

## ❖ EMB (External Memory Bus)

- Support SRAM, NOR/NAND-flash, LCD interface
- Support synchronous or asynchronous timing mode control

- Support multiple types of address and data multiplex mode
- Provide optional 16/24/30-bit address mode
  - Memory space 2G/32M/128K-byte for 16-bit data width
- Configurable time cycle for address latch time and data access time
- Received and transmitted data are buffered with DMA capability
- Allow running CPU code on external SRAM

#### ❖ ADC

- 12-bit SAR ADC with 1.5Msps
  - Configurable resolution : 12/10/8-bit
  - Configurable sampling time
- Provide external 16 channels and internal 7 channels input
  - Internal extra channel source : VBUF, VSSA, LDO VR0, DAC out, 1/2VDD, VPG, TS out
- Support auto-sampling and trigger by external pin, internal events and software bit
- Data alignment for output code left/right justify
- Built-in input buffer stage with bypass option
  - PGA with programmable gain : 1~4
- Optional ADC top voltage reference from external VREF+ or internal IVR24
- Interrupt generation at the end of sampling, end of conversion, end of sequence conversion
- Support voltage window detection and output code limitation
- Built-in three channel independent hardware accumulators for ADC output code
- Support one-shot/channel scan/loop scan
- ADC data are buffered with DMA capability
- Support wait mode to prevent ADC overrun

#### ❖ Analog Comparator

- Provide 2 fast Rail-to-rail comparators
- Programmable 64-step threshold of internal voltage reference
- Provide external total 6 channels input for all comparators
  - Two common and two independent external channels, two internal channels
- Programmable input hysteresis voltage
- Programmable response time for optimal current consumption
- Selectable compare output polarity
- Support wakeup from SLEEP and STOP modes
- Support analog watch dog as a reset source

#### ❖ DAC

- One 12-bit voltage DAC
  - Maximum conversion rate is 1Msps
- Conversion start trigger by register written, external pin and internal events
- Build in internal output buffer
- Data alignment for input code left/right justify
  - Configurable code width : 12/10/8-bit
- Output data are buffered with DMA capability

#### ❖ Temperature Sensor

- Built-in a temperature sensor in ADC macro
- Temperature resolution : +/- 2 °C (Typical)
- Temperature operation range : -40°C ~ 125°C

#### ❖ GPL (General Purpose Logic)

- Support data inverse, bit order change, byte order change and parity check
  - Data bit order change for 8/16/32-bit reverse
  - Data byte order change between Little endian and Big endian for 16/32-bit range

- Parity Check for 8/16/32 bit range
- **Support CRC (Cyclic Redundancy Check) calculation**
  - Programmable CRC initial value
  - CRC output bit order change
- **CRC with fixed common polynomial**
  - CRC8 polynomial 0x07
  - CRC16 polynomial 0x8005
  - CCITT16 polynomial 0x1021
  - CRC32(IEEE 802.3) polynomial 0x4C11DB7
- **Support signed/unsigned 32-bit divider**
  - Operation in 8 clock cycles
- **Input data are buffered with DMA capability**

### ❖ Misc.

- **Timer synchronous enable global control**
- **OBM(Output Signal Break and Modulation) control**
  - Support two sets of OBM for output signal break and modulation control
- **NCO(Numerically Controlled Oscillator) output with FDC and PF modes**
- **Support two sets of CCL(Configurable Custom Logic)**
- **32-bit non-reset backup register**
- **Provide on chip 16 bytes Unique ID code**

### ❖ Operating

- **Operating voltage range 1.8V ~ 5.5V**
- **Operating temperature range -40°C ~ 105°C (\*\*1)**
- **Operating frequency range up to 48MHz**

### ❖ Package Types

- **LQFP80 / LQFP64 / LQFP48**

(\*\*1): Tested by sampling.

## List of Contents

|                                        |           |
|----------------------------------------|-----------|
| <b>Features .....</b>                  | <b>3</b>  |
| <b>List of Contents.....</b>           | <b>9</b>  |
| <b>List of Figures .....</b>           | <b>13</b> |
| <b>List of Tables .....</b>            | <b>14</b> |
| <b>1. General Description .....</b>    | <b>15</b> |
| <b>2. Order Information.....</b>       | <b>16</b> |
| <b>3. Block Diagram .....</b>          | <b>18</b> |
| 3.1. System Function Block.....        | 18        |
| 3.2. Chip Main Block .....             | 19        |
| <b>4. Pin Description .....</b>        | <b>20</b> |
| 4.1. Pin Outline.....                  | 20        |
| 4.1.1. LQFP80 Package Pinout.....      | 20        |
| 4.1.2. LQFP64 Package Pinout.....      | 23        |
| 4.1.3. LQFP48 Package Pinout.....      | 26        |
| 4.2. Pin Definition .....              | 28        |
| 4.3. Pin AFS Summary Table .....       | 49        |
| 4.1. Analog Function Pin Table.....    | 51        |
| 4.2. Alternate Functions Pin List..... | 52        |
| <b>5. Memory Map .....</b>             | <b>59</b> |
| 5.1. Memory Organization .....         | 59        |
| 5.2. CPU Memory Map.....               | 60        |
| 5.3. Peripheral Memory Boundary.....   | 61        |
| 5.4. Boot Modes .....                  | 62        |
| <b>6. Functional Description .....</b> | <b>63</b> |
| 6.1. CPU Core.....                     | 63        |
| 6.1.1. Introduction .....              | 63        |
| 6.1.2. CPU Features .....              | 63        |
| 6.1.3. ARM Cortex-M0 Processor .....   | 63        |
| 6.2. Power Management .....            | 64        |
| 6.2.1. Introduction .....              | 64        |
| 6.2.2. Chip Power Features .....       | 64        |
| 6.2.3. Power Operation Mode .....      | 64        |
| 6.2.4. Power Supply .....              | 64        |
| 6.2.5. CPU Power Down .....            | 65        |
| 6.3. System Reset.....                 | 65        |
| 6.3.1. Introduction .....              | 65        |
| 6.3.2. Chip Reset Features .....       | 65        |
| 6.3.3. Chip Reset Levels .....         | 65        |
| 6.3.4. External Reset .....            | 66        |
| 6.3.5. Module Reset.....               | 66        |
| 6.4. System Clock .....                | 66        |
| 6.4.1. Introduction .....              | 66        |
| 6.4.2. Chip Clock Features .....       | 66        |
| 6.4.3. System Clock Source.....        | 66        |

|                                                   |    |
|---------------------------------------------------|----|
| 6.4.4. PLL Clock.....                             | 66 |
| 6.4.5. Module Process Clock Control.....          | 66 |
| 6.5. System Common Control .....                  | 66 |
| 6.5.1. Introduction .....                         | 66 |
| 6.5.2. Features.....                              | 66 |
| 6.6. Memory Access .....                          | 67 |
| 6.6.1. Introduction .....                         | 67 |
| 6.6.2. Features.....                              | 67 |
| 6.6.3. Memory Controller .....                    | 67 |
| 6.6.4. ICP/ISP/IAP for Flash Memory.....          | 67 |
| 6.6.5. Hardware Option Byte Flash Memory .....    | 67 |
| 6.7. External Memory Bus .....                    | 68 |
| 6.7.1. Features.....                              | 68 |
| 6.7.2. EMB Control Function.....                  | 68 |
| 6.8. GPIO .....                                   | 68 |
| 6.8.1. Introduction .....                         | 68 |
| 6.8.2. Features.....                              | 68 |
| 6.8.3. GPIO Control Block.....                    | 69 |
| 6.9. Interrupt.....                               | 69 |
| 6.9.1. Introduction .....                         | 69 |
| 6.9.2. Interrupt Features .....                   | 69 |
| 6.9.3. Interrupt Structure .....                  | 70 |
| 6.9.4. Nested Vectored Interrupt Controller ..... | 70 |
| 6.9.5. Wakeup Interrupt Controller .....          | 71 |
| 6.9.6. External Interrupt Controller.....         | 71 |
| 6.10. General Purpose Logic.....                  | 71 |
| 6.10.1. Introduction .....                        | 71 |
| 6.10.2. Features.....                             | 71 |
| 6.10.3. GPL Control Block .....                   | 71 |
| 6.11. APB Common Control .....                    | 72 |
| 6.11.1. Introduction .....                        | 72 |
| 6.11.2. Features.....                             | 72 |
| 6.11.3. APB Control Block .....                   | 72 |
| 6.12. APX.....                                    | 72 |
| 6.12.1. Introduction .....                        | 72 |
| 6.12.2. Features.....                             | 72 |
| 6.12.3. APX Control Block .....                   | 73 |
| 6.13. Direct Memory Access.....                   | 73 |
| 6.13.1. Introduction .....                        | 73 |
| 6.13.2. Features.....                             | 73 |
| 6.13.3. DMA Control .....                         | 73 |
| 6.14. ADC.....                                    | 74 |
| 6.14.1. Introduction .....                        | 74 |
| 6.14.2. Features.....                             | 74 |
| 6.14.3. ADC Control Block .....                   | 74 |
| 6.15. Analog Comparator .....                     | 75 |

|                                            |           |
|--------------------------------------------|-----------|
| 6.15.1. Introduction .....                 | 75        |
| 6.15.2. Features.....                      | 75        |
| 6.15.3. CMP Control Block.....             | 75        |
| 6.16. DAC.....                             | 76        |
| 6.16.1. Introduction .....                 | 76        |
| 6.16.2. Features.....                      | 76        |
| 6.16.3. DAC Control Block .....            | 76        |
| 6.17. IWDTC.....                           | 76        |
| 6.17.1. Introduction .....                 | 76        |
| 6.17.2. Features.....                      | 76        |
| 6.17.3. IWDTC Control .....                | 76        |
| 6.18. WWDT.....                            | 77        |
| 6.18.1. Introduction .....                 | 77        |
| 6.18.2. Features.....                      | 77        |
| 6.18.3. WWDT Control .....                 | 77        |
| 6.19. RTC.....                             | 77        |
| 6.19.1. Introduction .....                 | 77        |
| 6.19.2. Features.....                      | 77        |
| 6.19.3. RTC Control .....                  | 78        |
| 6.20. Timer .....                          | 78        |
| 6.20.1. Introduction .....                 | 78        |
| 6.20.2. Features.....                      | 78        |
| 6.20.3. Module Functions.....              | 79        |
| 6.20.4. Timer Control Block .....          | 79        |
| 6.21. I2C.....                             | 80        |
| 6.21.1. Introduction .....                 | 80        |
| 6.21.2. Features.....                      | 80        |
| 6.21.3. I2C Control.....                   | 80        |
| 6.22. UART .....                           | 81        |
| 6.22.1. Introduction .....                 | 81        |
| 6.22.2. Features.....                      | 81        |
| 6.22.3. Module Functions.....              | 82        |
| 6.22.4. UART Control.....                  | 82        |
| 6.23. SPI .....                            | 83        |
| 6.23.1. Introduction .....                 | 83        |
| 6.23.2. Features.....                      | 83        |
| 6.23.3. SPI Control.....                   | 84        |
| <b>7. Application Notes.....</b>           | <b>85</b> |
| 7.1. Power Supply Circuit .....            | 85        |
| 7.2. Reset Circuit.....                    | 86        |
| 7.3. Xtal Oscillating Circuit .....        | 86        |
| 7.4. ADC Application Circuit .....         | 88        |
| 7.5. DAC Application Circuit .....         | 88        |
| <b>8. Electrical Characteristics .....</b> | <b>89</b> |
| 8.1. Parameter Glossary .....              | 89        |
| 8.2. Absolute Maximum Rating .....         | 89        |

|            |                                          |            |
|------------|------------------------------------------|------------|
| 8.3.       | DC Characteristics .....                 | 90         |
| 8.4.       | IO Characteristics.....                  | 92         |
| 8.5.       | External Clock Characteristics .....     | 95         |
| 8.6.       | PLL Characteristics .....                | 95         |
| 8.7.       | IHRCO Characteristics.....               | 95         |
| 8.8.       | ILRCO Characteristics.....               | 96         |
| 8.9.       | LDO Characteristics .....                | 96         |
| 8.10.      | Flash Characteristics.....               | 96         |
| 8.11.      | ADC Characteristics .....                | 97         |
| 8.12.      | ADC PGA Characteristics.....             | 98         |
| 8.13.      | Analog Comparator Characteristics.....   | 99         |
| 8.14.      | Temperature Sensor Characteristics ..... | 99         |
| 8.15.      | DAC Characteristics .....                | 100        |
| 8.16.      | UART Characteristics .....               | 101        |
| 8.17.      | SPI Characteristics.....                 | 102        |
| 8.18.      | I2C Characteristics .....                | 104        |
| <b>9.</b>  | <b>Package Dimension .....</b>           | <b>105</b> |
| 9.1.       | LQFP-80.....                             | 105        |
| 9.2.       | LQFP-64.....                             | 106        |
| 9.3.       | LQFP-48.....                             | 107        |
| <b>10.</b> | <b>Revision History .....</b>            | <b>108</b> |
| <b>11.</b> | <b>Disclaimers .....</b>                 | <b>110</b> |

## List of Figures

|                                                |     |
|------------------------------------------------|-----|
| Figure 2-1. Part Numbering .....               | 16  |
| Figure 3-1. System Function Block .....        | 18  |
| Figure 3-2. Chip Main Block .....              | 19  |
| Figure 4-1. LQFP80 Package Pinout .....        | 20  |
| Figure 4-2. LQFP64 Package Pinout .....        | 23  |
| Figure 4-3. LQFP48 Package Pinout .....        | 26  |
| Figure 5-1. Memory Organization Map .....      | 59  |
| Figure 6-1. ARM Cortex-M0 Processor .....      | 63  |
| Figure 7-1. Power Supply Circuit .....         | 85  |
| Figure 7-2. Reset Circuit .....                | 86  |
| Figure 7-3. XTAL Oscillating Circuit .....     | 86  |
| Figure 7-4. ADC Application Circuit .....      | 88  |
| Figure 7-5. DAC Application Circuit .....      | 88  |
| Figure 8-1. UART Timing Waveform .....         | 101 |
| Figure 8-2. SPI Master Timing Waveform .....   | 103 |
| Figure 8-3. SPI Slave Timing Waveform .....    | 103 |
| Figure 8-4. I2C Timing Waveform .....          | 104 |
| Figure 9-1. LQFP-80 (10mm X 10mm) ~ AD80 ..... | 105 |
| Figure 9-2. LQFP-64 (7mm X 7mm) ~ AD64 .....   | 106 |
| Figure 9-3. LQFP-48 (7mm X 7mm) ~ AD48 .....   | 107 |

**List of Tables**

|                                                                                   |     |
|-----------------------------------------------------------------------------------|-----|
| Table 2-1. Chip Selection Table .....                                             | 17  |
| Table 4-1. LQFP80 Pin AFS List .....                                              | 21  |
| Table 4-2. LQFP64 Pin AFS List .....                                              | 24  |
| Table 4-3. LQFP48 Pin AFS List .....                                              | 26  |
| Table 4-4. Abbreviations for pin definition .....                                 | 28  |
| Table 4-5. Pin Descriptions .....                                                 | 28  |
| Table 4-6. Pin AFS Summary Table .....                                            | 49  |
| Table 4-7. Analog Function Pin Table .....                                        | 51  |
| Table 4-8. Alternate Functions Pin List .....                                     | 52  |
| Table 5-1. CPU Memory Address Map .....                                           | 60  |
| Table 5-2. Peripheral Memory Boundary Address .....                               | 61  |
| Table 6-1. Power-Down Mode Selection .....                                        | 65  |
| Table 6-2. Interrupt Source Table .....                                           | 70  |
| Table 6-3. Timer Module Function Table .....                                      | 79  |
| Table 6-4. UART Module Function Table .....                                       | 82  |
| Table 7-1. Internal Total Equivalent Capacitance for XOSC circuit .....           | 87  |
| Table 7-2. Reference Capacitance of C1 & C2 for crystal oscillating circuit ..... | 87  |
| Table 8-1. Parameter Glossary .....                                               | 89  |
| Table 8-2. Absolute Maximum Rating .....                                          | 89  |
| Table 8-3. DC Characteristics .....                                               | 90  |
| Table 8-4. Current Measurement Condition Level Definition Table .....             | 91  |
| Table 8-5. IO Characteristics .....                                               | 92  |
| Table 8-6. External Clock Characteristics .....                                   | 95  |
| Table 8-7. PLL Characteristics .....                                              | 95  |
| Table 8-8. IHRCO Characteristics .....                                            | 95  |
| Table 8-9. ILRCO Characteristics .....                                            | 96  |
| Table 8-10. LDO Characteristics .....                                             | 96  |
| Table 8-11. Flash Characteristics .....                                           | 96  |
| Table 8-12. ADC Characteristics .....                                             | 97  |
| Table 8-13. ADC PGA Characteristics .....                                         | 98  |
| Table 8-14. Analog Comparator Characteristics .....                               | 99  |
| Table 8-15. Temperature Characteristics .....                                     | 99  |
| Table 8-16. DAC Characteristics .....                                             | 100 |
| Table 8-17. UART Characteristics .....                                            | 101 |
| Table 8-18. SPI Characteristics .....                                             | 102 |
| Table 8-19. I2C Characteristics .....                                             | 104 |

## 1. General Description

The **MG32F02A** is a single-chip 32-bit microcontroller based on a high performance Core ARM® 32-bit Cortex®-M0 CPU with embedded Nested Vectored Interrupt Controller (NVIC).

The **MG32F02A** has up to **128K** bytes of embedded main flash memory for code and data, programmable memory size of embedded system flash memory for boot load code and 64 bytes of embedded option-byte flash memory for chip configuration. The all flash memory can be programmed either in serial writer mode (ICP, In-Circuit-Programming). Also, the main flash memory can be programmed in ISP (In-System Programming) mode or SRAM (Boot on SRAM) mode. ICP and ISP allow the user to download new code without removing the microcontroller from the actual end product; IAP means that the device can write non-volatile data in the flash memory while the application program is running. There needs no external high voltage for programming due to its built-in charge-pumping circuitry.

The **MG32F02A** retains all features of the ARM® 32-bit Cortex®-M0 with **16K** bytes of SRAM, **5** I/O ports, **32** external interrupts source with 4-level interrupt controller and seven 8/16-bits timer/counters. In addition, the **MG32F02A/U** has a System Tick Timer, two Watchdog Timers, three Advance timer modules with IC/OC, four Basic timer modules for universal using, on-chip crystal oscillator for 32.768 KHz to 25MHz, two high precision internal oscillators IHRCO for 11.059/12MHz and ILRCO for 32 KHz, one 12-bit ADC with one temperature sensor, two programmable threshold comparators and one 12-bit voltage mode DAC.

Also, the **MG32F02A** support multiple and flexible communicate interface for production application. It provides alternate function pins those are including of GPIO, I2C, SPI, UART, Timer with IC/PWM, ADC, Analog Comparator, DAC, EMB, NCO, CCL and SWD(on chip debug). It has maximum 73 GPIO pins and provides programmable IO type - quasi-bidirectional , push-pull output , open-drain output , input only(Hi-z) with optional pull-high. In addition, it is built-in internal de-bounce circuit to deglitch noise for worse signals.

One direct memory access (DMA) controller is used to improve data transfer between peripherals and memory and memory to memory. The data can be transfer by DMA controller and does not cost any CPU time.

One external memory bus (EMB) controller is used to access external SRAM, NOR/NAND flash or 8080 interface LCD display panel. It supports multiple address bus and data bus multiplex modes. Also it supports synchronous or asynchronous timing with programmable cycle time for external devices.

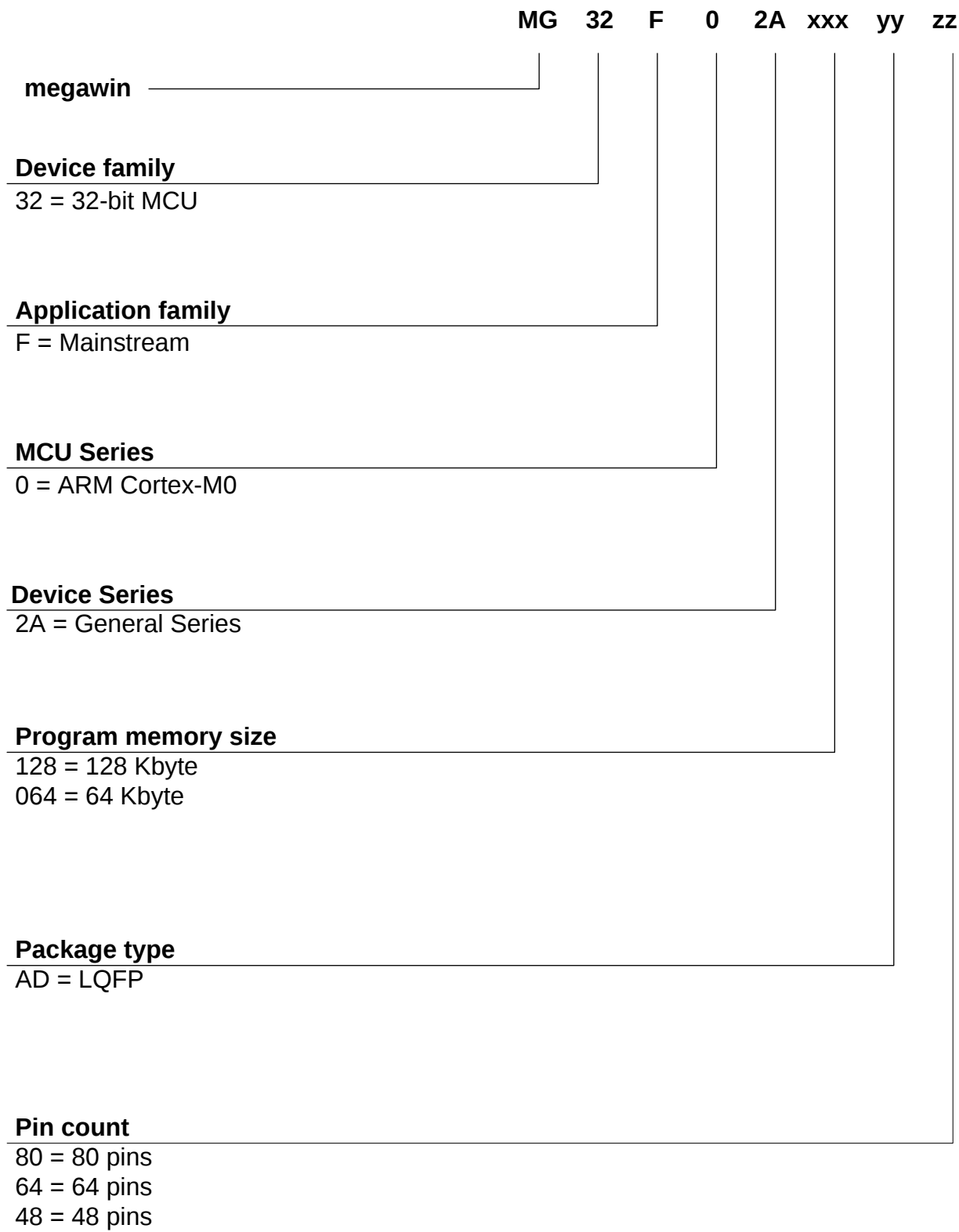
For power management and reset control, the **MG32F02A** is built-in a power supervisor including of a Low Voltage Detector(LVD), three Brown-out Detectors(BOD0/BOD1/BOD2), a Power-On Reset(POR) , a Low-voltage Reset(LVR). The **MG32F02A** has multiple power-down modes to reduce the current consumption: Sleep mode and Stop mode.

In the Sleep mode the CPU is frozen while the peripherals and the interrupt system are still operating. In the Stop mode the RAM and SFRs' value are saved and all other functions are inoperative; most importantly, in the Sleep mode the chip can be waked up by many interrupt or reset sources(POR/LVR/BOD0/BOD1/BOD2).

2. Order Information

Please contact the megawin sales for available options (memory size, package ...) and more information about this device.

Figure 2-1. Part Numbering



● **Chip Selection**

**Table 2-1. Chip Selection Table**

| Functions                                    | Chip | MG32F02A128                               | MG32F02A064                               | Comment                                                                                                                          |
|----------------------------------------------|------|-------------------------------------------|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| Flash ROM                                    |      | <b>128KB</b>                              | <b>64KB</b>                               | memory space of AP+IAP+ISP                                                                                                       |
| SRAM                                         |      | <b>16KB</b>                               | <b>10KB</b>                               |                                                                                                                                  |
| Package                                      |      | <b>LQFP80/64</b>                          | <b>LQFP64/48</b>                          |                                                                                                                                  |
| IO Number                                    |      | <b>73/59</b>                              | <b>59/44</b>                              | IO number by package                                                                                                             |
| Max. CPU Frequency                           |      | <b>48MHz</b>                              | <b>48MHz</b>                              |                                                                                                                                  |
| Internal Clock Source                        |      | <b>ILRCO+IHRCO</b>                        | <b>ILRCO+IHRCO</b>                        | 12MHz(default) & 11.059MHz option for IHRCO                                                                                      |
| Voltage Detector                             |      | <b>LVR+BOD0/1/2</b>                       | <b>LVR+BOD0/1/2</b>                       | Low Voltage Reset (LVR), BOD1: 4.2/3.7/2.4/2.0V                                                                                  |
| Timers                                       |      | 16-bit*2: TM00/01<br>32-bit*5: TM1x/2x/36 | 16-bit*2: TM00/01<br>32-bit*5: TM1x/2x/36 | support Full-Counter, Cascade , Separate modes                                                                                   |
| IC/OC/PWM Channels                           |      | 8-CH (16-bit) or<br>16-CH(8-bit)          | 8-CH (16-bit) or<br>16-CH(8-bit)          | IC: Input Capture, OC: Output Compare (support normal + complement output)                                                       |
| WDT                                          |      | <b>IWDT + WWDT</b>                        | <b>IWDT + WWDT</b>                        | IWDT: Independent Watch Dog Timer, WWDT: System Window Watch Dog Timer                                                           |
| RTC                                          |      | <b>32-Bit</b>                             | <b>32-Bit</b>                             |                                                                                                                                  |
| ADC                                          |      | <b>12-Bit , 16-CH<br/>1.5Msps</b>         | <b>12-Bit , 16-CH<br/>1.5Msps</b>         | embedded one input buffer with PGA<br>at room temperature                                                                        |
| ACMP Units                                   |      | <b>2</b>                                  | <b>2</b>                                  | fast rail-to-rail analog comparators with two R-ladder voltage reference                                                         |
| DAC                                          |      | <b>voltage DAC<br/>12-Bit , 1-CH</b>      | <b>voltage DAC<br/>12-Bit , 1-CH</b>      | 02V ~ VDD-0.2V full scale range with output buffer on                                                                            |
| UART Units                                   |      | <b>Advanced *3<br/>Basic *4</b>           | <b>Advanced *3<br/>Basic *4</b>           | URT0~3 can configurable to SPI, Multi-processor, IrDA, LIN, ISO-7816 (SmartCard) and<br>support Hardware flow control            |
| UART as SPI                                  |      | <b>Master/Slave *3</b>                    | <b>Master/Slave *3</b>                    | configurable and shared in advanced UART module                                                                                  |
| UART SPI mode Max.<br>Clock Rate (3.3V/1.8V) |      | Master: 18/16 MHz<br>Slave: 12/12 MHz     | Master: 18/16 MHz<br>Slave: 12/12 MHz     | VDD (5~3.3V / 3.3~1.8V)                                                                                                          |
| SPI Units                                    |      | <b>1</b>                                  | <b>1</b>                                  | master/slave mode with or without NSS control                                                                                    |
| SPI Max. Clock Rate<br>(3.3V/1.8V)           |      | Master: 22/16 MHz<br>Slave: 16/12 MHz     | Master: 22/16 MHz<br>Slave: 16/12 MHz     | VDD (5~3.3V / 3.3~1.8V)                                                                                                          |
| I2C Units                                    |      | <b>2</b>                                  | <b>2</b>                                  | optional Byte/Buffer mode, with/without clock stretching                                                                         |
| EMB                                          |      | <b>16/8-Bit Bus</b>                       | <b>16/8-Bit Bus</b>                       | support SRAM,NOR/NAND flash,8088 LCD IF                                                                                          |
| DMA Channels                                 |      | <b>5-CH</b>                               | <b>5-CH</b>                               | single/block/demand mode for external pin trigger                                                                                |
| CRC                                          |      | <b>CRC8+16+32</b>                         | <b>CRC8+16+32</b>                         | CRC8/CRC16/CCITT16/CRC32 fixed polynomial                                                                                        |
| HW Divider                                   |      | <b>32bit/32bit</b>                        | <b>32bit/32bit</b>                        | hardware divider with 8 clock cycles (Dividend/Divisor)                                                                          |
| OBM Units                                    |      | <b>2</b>                                  | <b>2</b>                                  | Output Signal Break and Modulation                                                                                               |
| NCO Units                                    |      | <b>1</b>                                  | <b>1</b>                                  | numerically controlled oscillator, Output frequency <= 1/2 Input frequency                                                       |
| CCL Units                                    |      | <b>2</b>                                  | <b>2</b>                                  | configurable custom logic                                                                                                        |
| Operation Voltage                            |      | <b>1.8~5.5V</b>                           | <b>1.8~5.5V</b>                           |                                                                                                                                  |
| Operating Temperature                        |      | <b>-40~105°C</b>                          | <b>-40~105°C</b>                          | test by sampling                                                                                                                 |
| Flash Regions                                |      | <b>AP,IAP,ISP</b>                         | <b>AP,IAP,ISP</b>                         | Application flash, In-Application-Programming data flash, In-System-Programming flash<br>(ISP: In-System-Programming data flash) |

● **Part Number List**

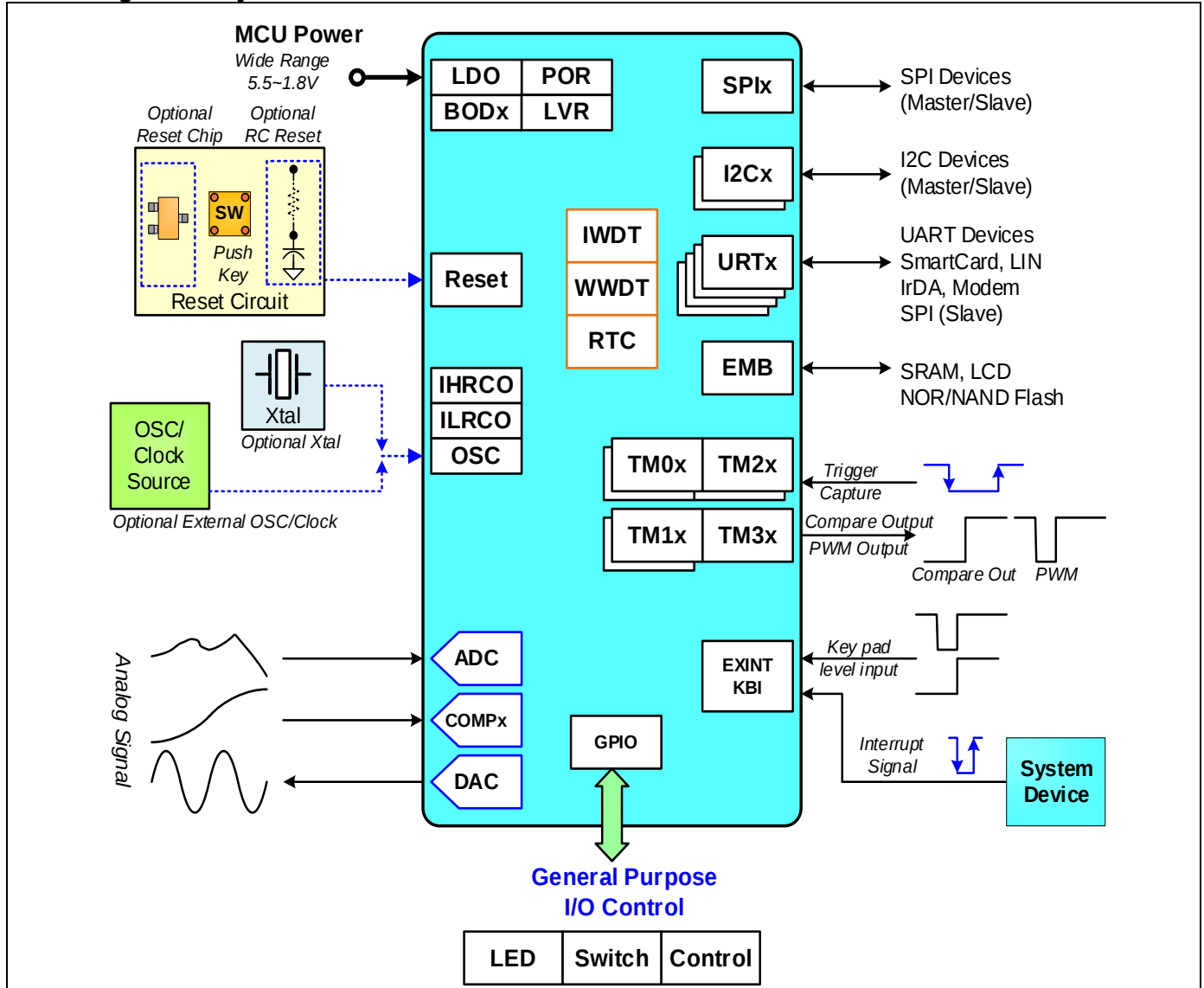
- **MG32F02A128AD80 : LQFP80 (10mm x 10mm), 128KB Flash**
- **MG32F02A128AD64 : LQFP64 (7mm x 7mm), 128KB Flash**
- **MG32F02A064AD64 : LQFP64 (7mm x 7mm), 64KB Flash**
- **MG32F02A064AD48 : LQFP48 (7mm x 7mm), 64KB Flash**

### 3. Block Diagram

#### 3.1. System Function Block

The following diagram is showing the system function block for application.

**Figure 3-1. System Function Block**

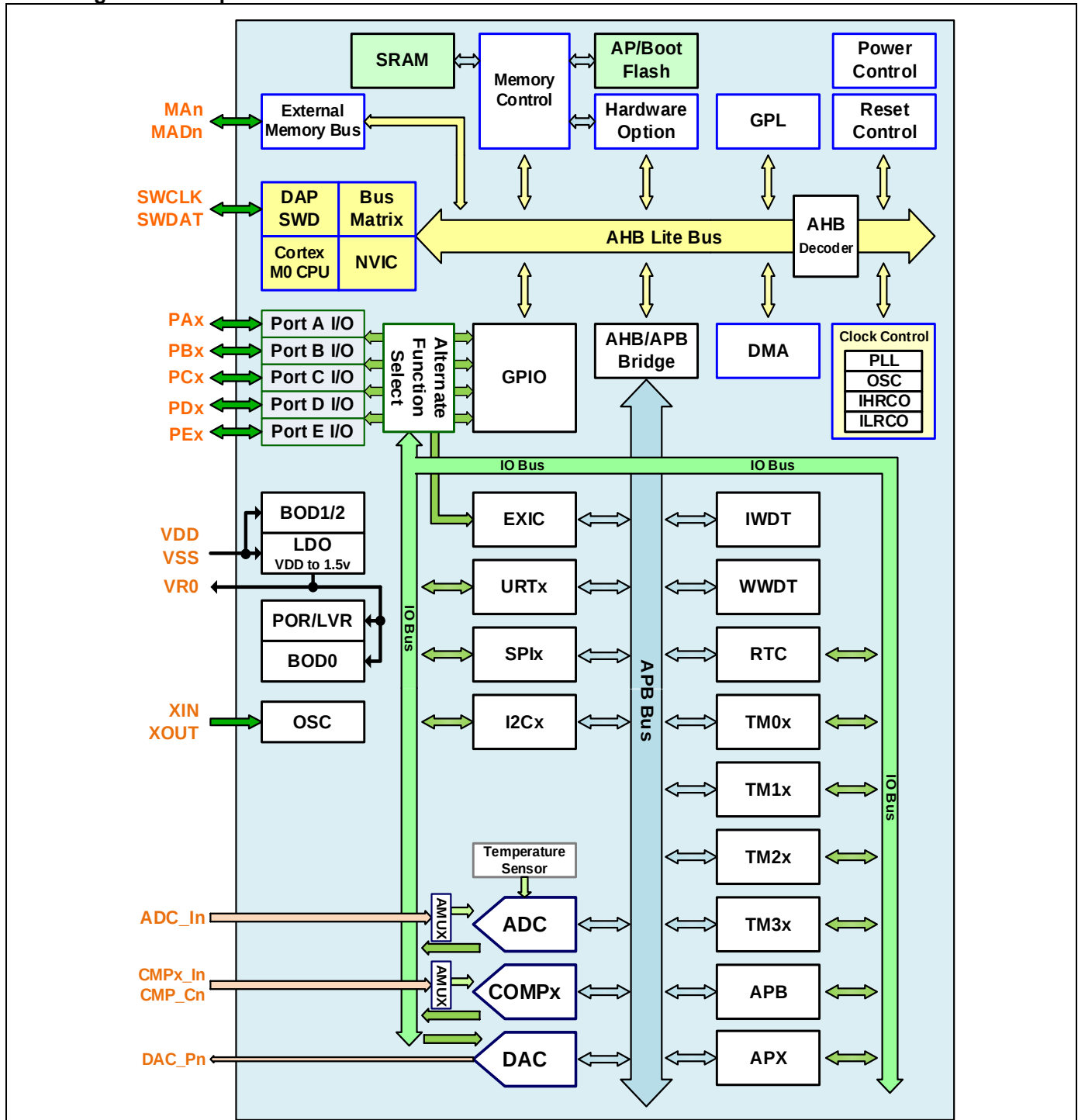


### 3.2. Chip Main Block

The following diagram is showing the block of internal devices in the chip.

There are one embedded ARM® Cortex®-M0 processor with NVIC (Nested Vectored Interrupt Controller) and DAP (Debug Access Port); AHB lite bus with SRAM/Flash memory, Power/Reset/Clock system controllers, EMB (External Memory Bus) controller, GPIO control blocks and GPL (General Purpose Logic); APB bus with UART/SPI/I2C communication controllers, timers of general timer / IWDG / WWDG / RTC and analog control block of ADC / analog comparators / DAC; analog devices of POR (power on reset), BOD0/BOD1/BOD2 (Brown-Out Detectors), ILRCO (Internal Low-frequency RC Oscillator)/IHRCO Internal High-frequency RC Oscillator)/PLL.

Figure 3-2. Chip Main Block

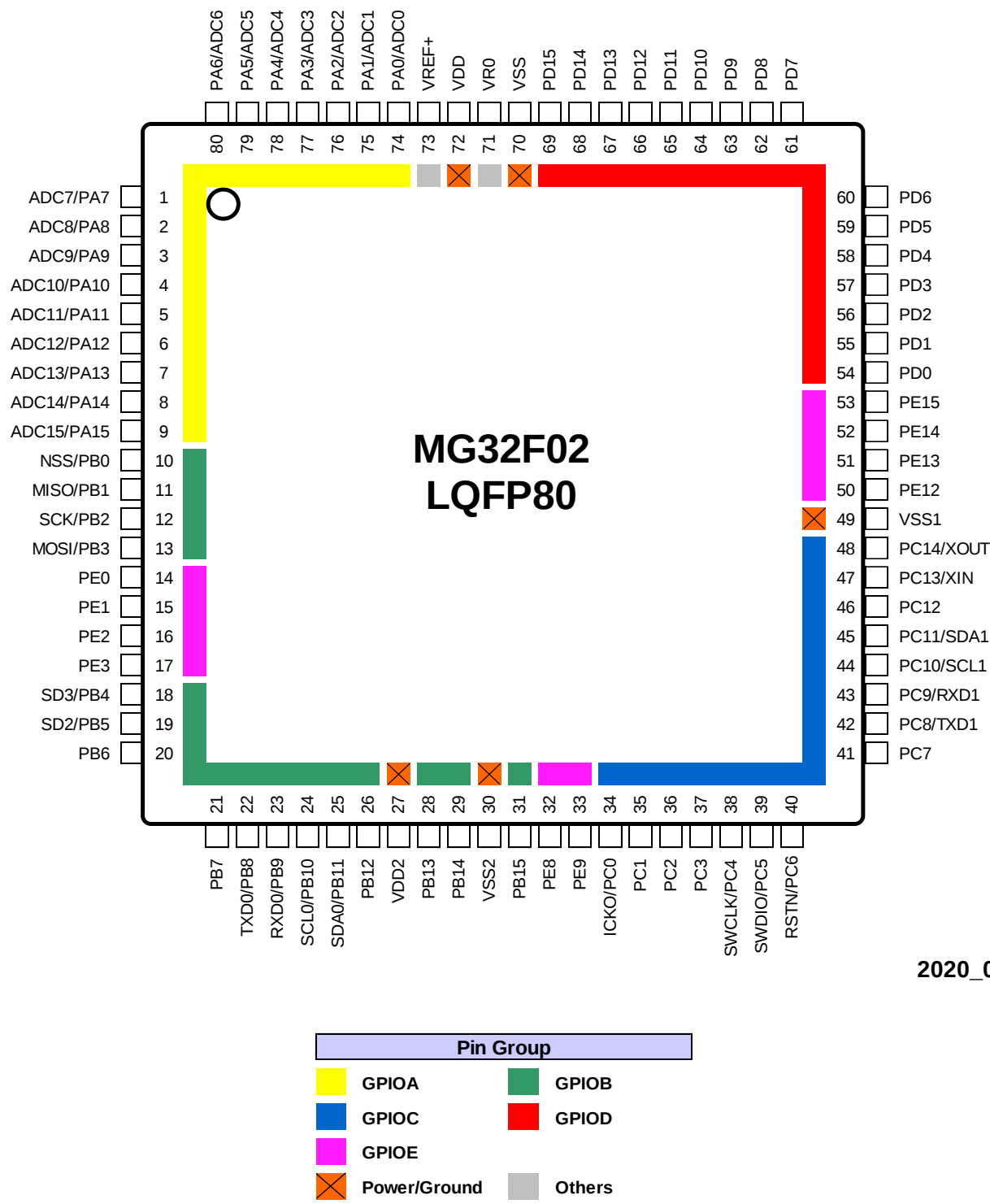


4. Pin Description

4.1. Pin Outline

4.1.1. LQFP80 Package Pinout

Figure 4-1. LQFP80 Package Pinout



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Table 4-1. LQFP80 Pin AFS List

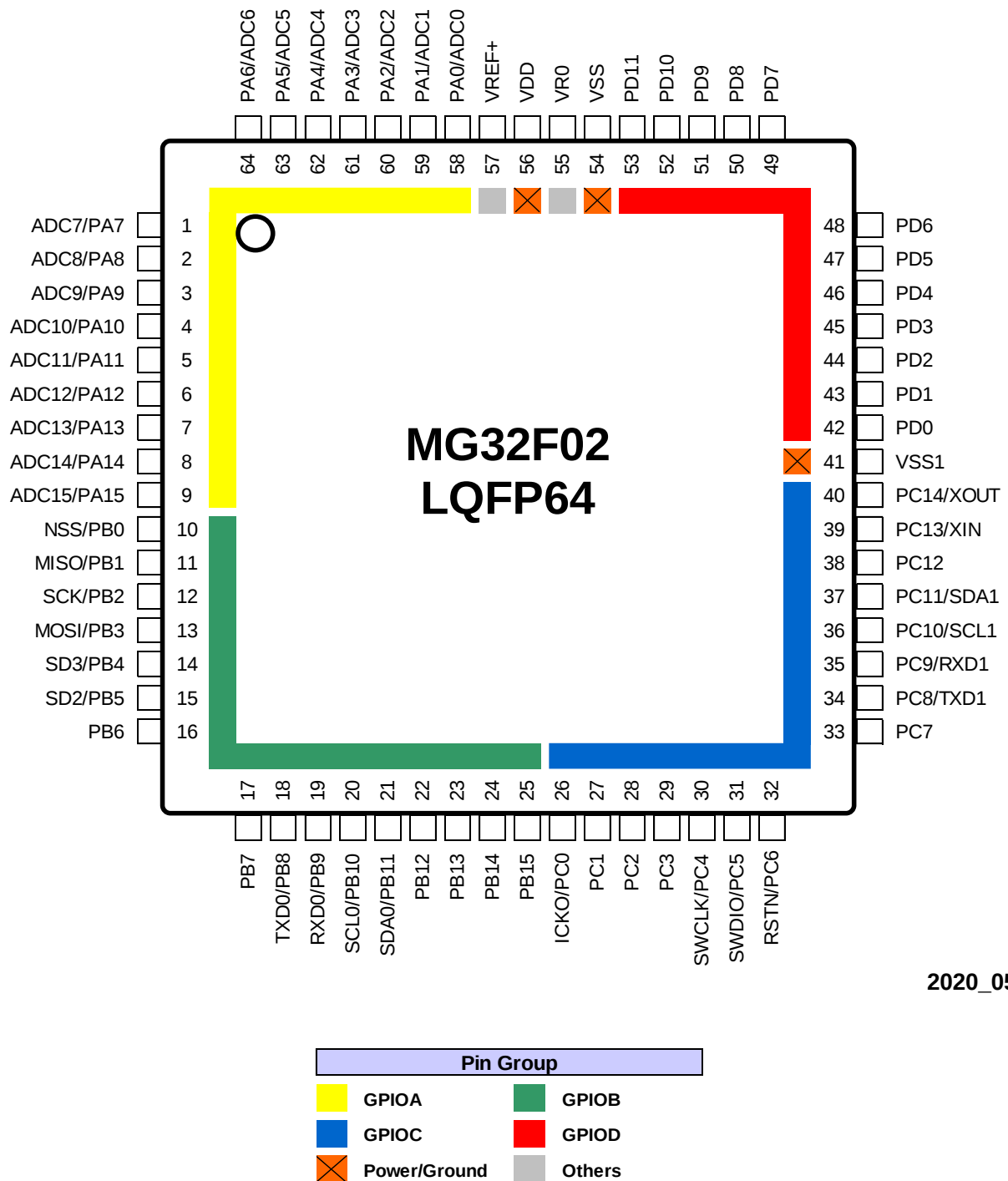
| Pin | Name | Pin AFS List                                                                                                | Analog Function           |
|-----|------|-------------------------------------------------------------------------------------------------------------|---------------------------|
| 1   | PA7  | GPA7, SPI0_D2, MA7, MAD7, TM20_OC1H, URT0_NSS                                                               | ADC_I7                    |
| 2   | PA8  | GPA8, DMA_TRG0, I2C0_SCL, URT2_BRO, SDT_I0, TM20_IC0, SPI0_NSS, MA8, MAD0, TM36_OC0H, URT4_TX               | ADC_I8, CMP0_I0, VBG_OUT  |
| 3   | PA9  | GPA9, DMA_TRG1, I2C1_SCL, URT2_TMO, TM20_IC1, SPI0_MISO, MA9, MAD1, TM36_OC1H, URT5_TX                      | ADC_I9, CMP0_I1           |
| 4   | PA10 | GPA10, TM36_BK0, SPI0_D2, I2C0_SDA, URT2_CTS, SDT_I1, TM26_IC0, SPI0_CLK, MA10, MAD2, TM36_OC2H, URT4_RX    | ADC_I10, CMP1_I0, ADC_PGA |
| 5   | PA11 | GPA11, DAC_TRG0, SPI0_D3, I2C1_SDA, URT2_RTS, TM26_IC1, SPI0_MOSI, MA11, MAD3, TM36_OC3H, URT5_RX           | ADC_I11, CMP1_I1          |
| 6   | PA12 | GPA12, URT1_BRO, TM10_ETR, TM36_IC0, SPI0_D5, MA12, MAD4, TM26_OC00, URT6_TX                                | ADC_I12                   |
| 7   | PA13 | GPA13, CPU_TXEV, URT0_BRO, URT1_TMO, TM10_TRGO, TM36_IC1, SPI0_D6, MA13, MAD5, TM26_OC10, URT6_RX           | ADC_I13                   |
| 8   | PA14 | GPA14, CPU_RXEV, OBM_I0, URT0_TMO, URT1_CTS, TM16_ETR, TM36_IC2, SPI0_D7, MA14, MAD6, TM26_OC0H, URT7_TX    | ADC_I14                   |
| 9   | PA15 | GPA15, CPU_NMI, OBM_I1, URT0_DE, URT1_RTS, TM16_TRGO, TM36_IC3, SPI0_D4, MA15, MAD7, TM26_OC1H, URT7_RX     | ADC_I15                   |
| 10  | PB0  | GPB0, I2C1_SCL, SPI0_NSS, TM01_ETR, TM00_CKO, TM16_ETR, TM26_IC0, TM36_ETR, MA15, URT1_NSS, URT6_TX         | CMP_C0                    |
| 11  | PB1  | GPB1, I2C1_SDA, SPI0_MISO, TM01_TRGO, TM10_CKO, TM16_TRGO, TM26_IC1, TM36_TRGO, URT1_RX, URT6_RX            | CMP_C1                    |
| 12  | PB2  | GPB2, ADC0_TRG, SPI0_CLK, TM01_CKO, URT2_TX, TM16_CKO, TM26_OC0H, I2C0_SDA, URT1_CLK, URT0_TX, URT7_TX      | DAC_P0                    |
| 13  | PB3  | GPB3, ADC0_OUT, SPI0_MOSI, NCO_P0, URT2_RX, TM36_CKO, TM26_OC1H, I2C0_SCL, URT1_TX, URT0_RX, URT7_RX        |                           |
| 14  | PE0  | GPE0, OBM_I0, URT0_TX, DAC_TRG0, SPI0_NSS, TM20_OC00, TM26_OC00, MALE, MAD8, URT4_TX                        |                           |
| 15  | PE1  | GPE1, OBM_I1, URT0_RX, DMA_TRG1, SPI0_MISO, TM20_OC01, TM26_OC01, MOE, MAD9, TM36_OC0H, URT4_RX             |                           |
| 16  | PE2  | GPE2, OBM_P0, I2C1_SCL, URT1_TX, NCO_P0, SPI0_CLK, TM20_OC02, TM26_OC02, MWE, MAD10, TM36_OC1H, URT5_TX     |                           |
| 17  | PE3  | GPE3, OBM_P1, I2C1_SDA, URT1_RX, NCO_CK0, SPI0_MOSI, TM20_OC0N, TM26_OC0N, MCE, MALE2, URT5_RX              |                           |
| 18  | PB4  | GPB4, TM01_CKO, SPI0_D3, TM26_TRGO, URT2_CLK, TM20_IC0, TM36_IC0, MALE, MAD8                                |                           |
| 19  | PB5  | GPB5, TM16_CKO, SPI0_D2, TM26_ETR, URT2_NSS, TM20_IC1, TM36_IC1, MOE, MAD9                                  |                           |
| 20  | PB6  | GPB6, CPU_RXEV, SPI0_NSSI, URT0_BRO, URT2_CTS, TM20_ETR, TM36_IC2, MWE, MAD10, URT2_TX                      |                           |
| 21  | PB7  | GPB7, CPU_TXEV, URT0_TMO, URT2_RTS, TM20_TRGO, TM36_IC3, MCE, MALE2, URT2_RX                                |                           |
| 22  | PB8  | GPB8, CMP0_P0, RTC_OUT, URT0_TX, URT2_BRO, TM20_OC01, TM36_OC01, SPI0_D3, MAD0, SDT_P0, OBM_P0, URT4_TX     |                           |
| 23  | PB9  | GPB9, CMP1_P0, RTC_TS, URT0_RX, URT2_TMO, TM20_OC02, TM36_OC02, SPI0_D2, MAD1, MAD8, OBM_P1, URT4_RX        |                           |
| 24  | PB10 | GPB10, I2C0_SCL, URT0_NSS, URT2_DE, TM20_OC11, TM36_OC11, URT1_TX, MAD2, MAD1, SPI0_NSSI                    |                           |
| 25  | PB11 | GPB11, I2C0_SDA, URT0_DE, IR_OUT, TM20_OC12, TM36_OC12, URT1_RX, MAD3, MAD9, DMA_TRG0, URT0_CLK             |                           |
| 26  | PB12 | GPB12, DMA_TRG0, NCO_P0, URT1_CLK, MAD4, MAD2, URT5_TX                                                      |                           |
| 27  | VDD2 |                                                                                                             |                           |
| 28  | PB13 | GPB13, DAC_TRG0, TM00_ETR, URT0_CTS, TM20_ETR, TM36_ETR, URT0_CLK, MAD5, MAD10, CCL_P0, URT4_RX             |                           |
| 29  | PB14 | GPB14, DMA_TRG0, TM00_TRGO, URT0_RTS, TM20_TRGO, TM36_BK0, URT0_NSS, MAD6, MAD3, CCL_P1, URT4_TX            |                           |
| 30  | VSS2 |                                                                                                             |                           |
| 31  | PB15 | GPB15, IR_OUT, NCO_CK0, URT1_NSS, MAD7, MAD11, URT5_RX                                                      |                           |
| 32  | PE8  | GPE8, CPU_TXEV, OBM_I0, URT2_TX, SDT_I0, TM36_CKO, TM20_CKO, TM26_CKO, MAD11, URT4_TX                       |                           |
| 33  | PE9  | GPE9, CPU_RXEV, OBM_I1, URT2_RX, SDT_I1, TM36_TRGO, TM20_TRGO, TM26_TRGO, MOE, URT4_RX                      |                           |
| 34  | PC0  | GPC0, ICK0, TM00_CKO, URT0_CLK, URT2_CLK, TM20_OC00, TM36_OC00, I2C0_SCL, MCLK, MWE, URT0_TX, URT5_TX       |                           |
| 35  | PC1  | GPC1, ADC0_TRG, TM01_CKO, TM36_IC0, URT1_CLK, TM20_OC0N, TM36_OC0N, I2C0_SDA, MAD8, MAD4, URT0_RX, URT5_RX  |                           |
| 36  | PC2  | GPC2, ADC0_OUT, TM10_CKO, OBM_P0, URT2_CLK, TM20_OC10, TM36_OC10, SDT_I0, MAD9, MAD12                       |                           |
| 37  | PC3  | GPC3, OBM_P1, TM16_CKO, URT0_CLK, URT1_CLK, TM20_OC1N, TM36_OC1N, SDT_I1, MAD10, MAD5                       |                           |
| 38  | PC4  | GPC4, SWCLK, I2C0_SCL, URT0_RX, URT1_RX, TM36_OC2, SDT_I0, URT6_RX                                          |                           |
| 39  | PC5  | GPC5, SWDIO, I2C0_SDA, URT0_TX, URT1_TX, TM36_OC3, SDT_I1, URT6_TX                                          |                           |
| 40  | PC6  | GPC6, RSTN, RTC_TS, URT0_NSS, URT1_NSS, TM20_ETR, TM26_ETR, MBW1, MALE                                      |                           |
| 41  | PC7  | GPC7, ADC0_TRG, RTC_OUT, URT0_DE, URT1_NSS, TM36_TRGO, MBW0, MCE                                            |                           |
| 42  | PC8  | GPC8, ADC0_OUT, I2C0_SCL, URT0_BRO, URT1_TX, TM20_OC0H, TM36_OC0H, TM36_OC0N, MAD11, MAD13, CCL_P0, URT6_TX |                           |
| 43  | PC9  | GPC9, CMP0_P0, I2C0_SDA, URT0_TMO, URT1_RX, TM20_OC1H, TM36_OC1H, TM36_OC1N,                                |                           |

## MG32F02A128/A064

|    |       |                                                                                                       |        |
|----|-------|-------------------------------------------------------------------------------------------------------|--------|
|    |       | MAD12, MAD6, CCL_P1, URT6_RX                                                                          |        |
| 44 | PC10  | GPC10, CMP1_P0, I2C1_SCL, URT0_TX, URT2_TX, URT1_TX, TM36_OC2H, TM36_OC2N, MAD13, MAD14, URT7_TX      |        |
| 45 | PC11  | GPC11, I2C1_SDA, URT0_RX, URT2_RX, URT1_RX, TM36_OC3H, TM26_OC01, MAD14, MAD7, URT7_RX                |        |
| 46 | PC12  | GPC12, IR_OUT, DAC_TRG0, URT1_DE, TM10_TRGO, TM36_OC3, TM26_OC02, MAD15, SDT_P0                       |        |
| 47 | PC13  | GPC13, XIN, URT1_NSS, URT0_CTS, URT2_RX, TM10_ETR, TM26_ETR, TM36_OC00, TM20_IC0, SDT_I0, URT6_RX     |        |
| 48 | PC14  | GPC14, XOUT, URT1_TMO, URT0_RTS, URT2_TX, TM10_CKO, TM26_TRGO, TM36_OC10, TM20_IC1, SDT_I1, URT6_TX   |        |
| 49 | VSS1  |                                                                                                       |        |
| 50 | PE12  | GPE12, ADC0_TRG, TM01_CKO, TM16_CKO, TM20_OC10, TM26_OC10, MBW0, URT6_TX                              |        |
| 51 | PE13  | GPE13, ADC0_OUT, TM01_TRGO, TM16_TRGO, TM20_OC11, TM26_OC11, MBW1, TM36_OC2H, URT6_RX                 |        |
| 52 | PE14  | GPE14, RTC_OUT, I2C1_SCL, TM01_ETR, TM16_ETR, TM20_OC12, TM26_OC12, MALE2, CCL_P0, TM36_OC3H, URT7_TX |        |
| 53 | PE15  | GPE15, RTC_TS, I2C1_SDA, TM36_BK0, TM36_ETR, TM20_OC1N, TM26_OC1N, MALE, CCL_P1, URT7_RX              |        |
| 54 | PD0   | GPD0, OBM_I0, TM10_CKO, URT0_CLK, TM26_OC1N, TM20_CKO, TM36_OC2, SPI0_NSS, MA0, MCLK, URT2_NSS        |        |
| 55 | PD1   | GPD1, OBM_I1, TM16_CKO, URT0_CLK, NCO_CK0, TM26_CKO, TM36_OC2N, SPI0_CLK, MA1, URT2_CLK               |        |
| 56 | PD2   | GPD2, TM00_CKO, URT1_CLK, TM26_OC00, TM20_CKO, TM36_CKO, SPI0_MOSI, MA2, MAD4, URT2_TX                |        |
| 57 | PD3   | GPD3, TM01_CKO, URT1_CLK, SPI0_MISO, TM26_CKO, SPI0_D3, MA3, MAD7, TM36_TRGO, URT2_RX                 |        |
| 58 | PD4   | GPD4, TM00_TRGO, TM01_TRGO, URT1_TX, TM26_OC00, SPI0_D2, MA4, MAD6, URT2_TX                           |        |
| 59 | PD5   | GPD5, TM00_ETR, I2C0_SCL, URT1_RX, TM26_OC01, SPI0_MISO, MA5, MAD5, URT2_RX                           |        |
| 60 | PD6   | GPD6, CPU_NMI, I2C0_SDA, URT1_NSS, SPI0_NSSI, TM26_OC02, SPI0_NSS, MA6, SDT_P0, URT2_NSS              |        |
| 61 | PD7   | GPD7, TM00_CKO, TM01_ETR, URT1_DE, SPI0_MISO, TM26_OC0N, SPI0_D4, MA7, MAD0, TM36_IC0                 |        |
| 62 | PD8   | GPD8, CPU_TXEV, TM01_TRGO, URT1_RTS, SPI0_D2, TM26_OC10, SPI0_D7, MA8, MAD3, TM36_IC1, SPI0_CLK       |        |
| 63 | PD9   | GPD9, CPU_RXEV, TM00_TRGO, URT1_CTS, SPI0_NSSI, TM26_OC11, SPI0_D6, MA9, MAD2, TM36_IC2, SPI0_NSS     |        |
| 64 | PD10  | GPD10, CPU_NMI, TM00_ETR, URT1_BRO, RTC_OUT, TM26_OC12, SPI0_D5, MA10, MAD1, TM36_IC3, SPI0_MOSI      |        |
| 65 | PD11  | GPD11, CPU_NMI, DMA_TRG1, URT1_TMO, SPI0_D3, TM26_OC1N, SPI0_NSS, MA11, MWE                           |        |
| 66 | PD12  | GPD12, CMP0_P0, TM10_CKO, OBM_P0, TM00_CKO, SPI0_CLK, TM20_OC0H, TM26_OC0H, MA12, MALE2               |        |
| 67 | PD13  | GPD13, CMP1_P0, TM10_TRGO, OBM_P1, TM00_TRGO, NCO_CK0, TM20_OC1H, TM26_OC1H, MA13, MCE                |        |
| 68 | PD14  | GPD14, TM10_ETR, DAC_TRG0, TM00_ETR, TM20_IC0, TM26_IC0, MA14, MOE, CCL_P0, URT5_TX                   |        |
| 69 | PD15  | GPD15, NCO_P0, IR_OUT, DMA_TRG0, TM20_IC1, TM26_IC1, MA15, CCL_P1, URT5_RX                            |        |
| 70 | VSS   |                                                                                                       |        |
| 71 | VR0   |                                                                                                       |        |
| 72 | VDD   |                                                                                                       |        |
| 73 | VREF+ |                                                                                                       |        |
| 74 | PA0   | GPA0, SDT_P0, CCL_P0, MA0, MAD0, TM36_OC00, URT4_TX                                                   | ADC_I0 |
| 75 | PA1   | GPA1, CCL_P1, MA1, MAD1, TM36_OC10, URT4_RX                                                           | ADC_I1 |
| 76 | PA2   | GPA2, SDT_I0, MA2, MAD2, TM36_OC2, URT5_TX                                                            | ADC_I2 |
| 77 | PA3   | GPA3, SDT_I1, MA3, MAD3, TM36_OC2N, URT5_RX                                                           | ADC_I3 |
| 78 | PA4   | GPA4, MA4, MAD4, TM20_OC00, URT0_TX                                                                   | ADC_I4 |
| 79 | PA5   | GPA5, MA5, MAD5, TM20_OC10, URT0_RX                                                                   | ADC_I5 |
| 80 | PA6   | GPA6, SPI0_D3, MA6, MAD6, TM20_OC0H, URT0_CLK                                                         | ADC_I6 |

### 4.1.2. LQFP64 Package Pinout

Figure 4-2. LQFP64 Package Pinout



2020\_0515

**Table 4-2. LQFP64 Pin AFS List**

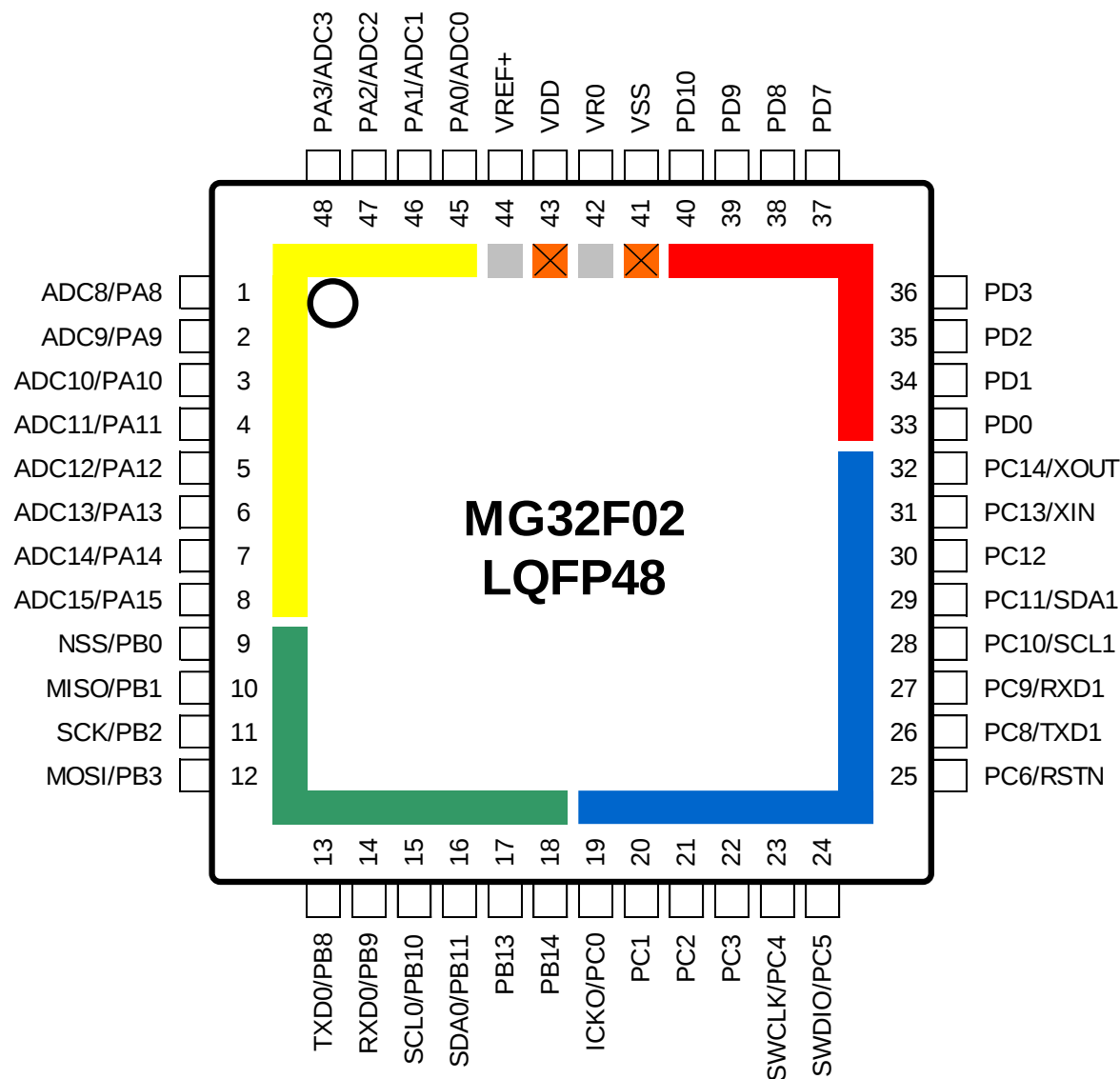
| Pin | Name | Pin AFS List                                                                                                | Analog Function           |
|-----|------|-------------------------------------------------------------------------------------------------------------|---------------------------|
| 1   | PA7  | GPA7, SPI0_D2, MA7, MAD7, TM20_OC1H, URT0_NSS                                                               | ADC_I7                    |
| 2   | PA8  | GPA8, DMA_TRG0, I2C0_SCL, URT2_BRO, SDT_I0, TM20_IC0, SPI0_NSS, MA8, MAD0, TM36_OC0H, URT4_TX               | ADC_I8, CMP0_I0, VBG_OUT  |
| 3   | PA9  | GPA9, DMA_TRG1, I2C1_SCL, URT2_TMO, TM20_IC1, SPI0_MISO, MA9, MAD1, TM36_OC1H, URT5_TX                      | ADC_I9, CMP0_I1           |
| 4   | PA10 | GPA10, TM36_BK0, SPI0_D2, I2C0_SDA, URT2_CTS, SDT_I1, TM26_IC0, SPI0_CLK, MA10, MAD2, TM36_OC2H, URT4_RX    | ADC_I10, CMP1_I0, ADC_PGA |
| 5   | PA11 | GPA11, DAC_TRG0, SPI0_D3, I2C1_SDA, URT2_RTS, TM26_IC1, SPI0_MOSI, MA11, MAD3, TM36_OC3H, URT5_RX           | ADC_I11, CMP1_I1          |
| 6   | PA12 | GPA12, URT1_BRO, TM10_ETR, TM36_IC0, SPI0_D5, MA12, MAD4, TM26_OC00, URT6_TX                                | ADC_I12                   |
| 7   | PA13 | GPA13, CPU_TXEV, URT0_BRO, URT1_TMO, TM10_TRGO, TM36_IC1, SPI0_D6, MA13, MAD5, TM26_OC10, URT6_RX           | ADC_I13                   |
| 8   | PA14 | GPA14, CPU_RXEV, OBM_I0, URT0_TMO, URT1_CTS, TM16_ETR, TM36_IC2, SPI0_D7, MA14, MAD6, TM26_OC0H, URT7_TX    | ADC_I14                   |
| 9   | PA15 | GPA15, CPU_NMI, OBM_I1, URT0_DE, URT1_RTS, TM16_TRGO, TM36_IC3, SPI0_D4, MA15, MAD7, TM26_OC1H, URT7_RX     | ADC_I15                   |
| 10  | PB0  | GPB0, I2C1_SCL, SPI0_NSS, TM01_ETR, TM00_CKO, TM16_ETR, TM26_IC0, TM36_ETR, MA15, URT1_NSS, URT6_TX         | CMP_C0                    |
| 11  | PB1  | GPB1, I2C1_SDA, SPI0_MISO, TM01_TRGO, TM10_CKO, TM16_TRGO, TM26_IC1, TM36_TRGO, URT1_RX, URT6_RX            | CMP_C1                    |
| 12  | PB2  | GPB2, ADC0_TRG, SPI0_CLK, TM01_CKO, URT2_TX, TM16_CKO, TM26_OC0H, I2C0_SDA, URT1_CLK, URT0_TX, URT7_TX      | DAC_P0                    |
| 13  | PB3  | GPB3, ADC0_OUT, SPI0_MOSI, NCO_P0, URT2_RX, TM36_CKO, TM26_OC1H, I2C0_SCL, URT1_TX, URT0_RX, URT7_RX        |                           |
| 14  | PB4  | GPB4, TM01_CKO, SPI0_D3, TM26_TRGO, URT2_CLK, TM20_IC0, TM36_IC0, MALE, MAD8                                |                           |
| 15  | PB5  | GPB5, TM16_CKO, SPI0_D2, TM26_ETR, URT2_NSS, TM20_IC1, TM36_IC1, MOE, MAD9                                  |                           |
| 16  | PB6  | GPB6, CPU_RXEV, SPI0_NSSI, URT0_BRO, URT2_CTS, TM20_ETR, TM36_IC2, MWE, MAD10, URT2_TX                      |                           |
| 17  | PB7  | GPB7, CPU_TXEV, URT0_TMO, URT2_RTS, TM20_TRGO, TM36_IC3, MCE, MALE2, URT2_RX                                |                           |
| 18  | PB8  | GPB8, CMP0_P0, RTC_OUT, URT0_TX, URT2_BRO, TM20_OC01, TM36_OC01, SPI0_D3, MAD0, SDT_P0, OBM_P0, URT4_TX     |                           |
| 19  | PB9  | GPB9, CMP1_P0, RTC_TS, URT0_RX, URT2_TMO, TM20_OC02, TM36_OC02, SPI0_D2, MAD1, MAD8, OBM_P1, URT4_RX        |                           |
| 20  | PB10 | GPB10, I2C0_SCL, URT0_NSS, URT2_DE, TM20_OC11, TM36_OC11, URT1_TX, MAD2, MAD1, SPI0_NSSI                    |                           |
| 21  | PB11 | GPB11, I2C0_SDA, URT0_DE, IR_OUT, TM20_OC12, TM36_OC12, URT1_RX, MAD3, MAD9, DMA_TRG0, URT0_CLK             |                           |
| 22  | PB12 | GPB12, DMA_TRG0, NCO_P0, URT1_CLK, MAD4, MAD2, URT5_TX                                                      |                           |
| 23  | PB13 | GPB13, DAC_TRG0, TM00_ETR, URT0_CTS, TM20_ETR, TM36_ETR, URT0_CLK, MAD5, MAD10, CCL_P0, URT4_RX             |                           |
| 24  | PB14 | GPB14, DMA_TRG0, TM00_TRGO, URT0_RTS, TM20_TRGO, TM36_BK0, URT0_NSS, MAD6, MAD3, CCL_P1, URT4_TX            |                           |
| 25  | PB15 | GPB15, IR_OUT, NCO_CK0, URT1_NSS, MAD7, MAD11, URT5_RX                                                      |                           |
| 26  | PC0  | GPC0, ICKO, TM00_CKO, URT0_CLK, URT2_CLK, TM20_OC00, TM36_OC00, I2C0_SCL, MCLK, MWE, URT0_TX, URT5_TX       |                           |
| 27  | PC1  | GPC1, ADC0_TRG, TM01_CKO, TM36_IC0, URT1_CLK, TM20_OC0N, TM36_OC0N, I2C0_SDA, MAD8, MAD4, URT0_RX, URT5_RX  |                           |
| 28  | PC2  | GPC2, ADC0_OUT, TM10_CKO, OBM_P0, URT2_CLK, TM20_OC10, TM36_OC10, SDT_I0, MAD9, MAD12                       |                           |
| 29  | PC3  | GPC3, OBM_P1, TM16_CKO, URT0_CLK, URT1_CLK, TM20_OC1N, TM36_OC1N, SDT_I1, MAD10, MAD5                       |                           |
| 30  | PC4  | GPC4, SWCLK, I2C0_SCL, URT0_RX, URT1_RX, TM36_OC2, SDT_I0, URT6_RX                                          |                           |
| 31  | PC5  | GPC5, SWDIO, I2C0_SDA, URT0_TX, URT1_TX, TM36_OC3, SDT_I1, URT6_TX                                          |                           |
| 32  | PC6  | GPC6, RSTN, RTC_TS, URT0_NSS, URT1_NSS, TM20_ETR, TM26_ETR, MBW1, MALE                                      |                           |
| 33  | PC7  | GPC7, ADC0_TRG, RTC_OUT, URT0_DE, URT1_NSS, TM36_TRGO, MBW0, MCE                                            |                           |
| 34  | PC8  | GPC8, ADC0_OUT, I2C0_SCL, URT0_BRO, URT1_TX, TM20_OC0H, TM36_OC0H, TM36_OC0N, MAD11, MAD13, CCL_P0, URT6_TX |                           |
| 35  | PC9  | GPC9, CMP0_P0, I2C0_SDA, URT0_TMO, URT1_RX, TM20_OC1H, TM36_OC1H, TM36_OC1N, MAD12, MAD6, CCL_P1, URT6_RX   |                           |
| 36  | PC10 | GPC10, CMP1_P0, I2C1_SCL, URT0_TX, URT2_TX, URT1_TX, TM36_OC2H, TM36_OC2N, MAD13, MAD14, URT7_TX            |                           |
| 37  | PC11 | GPC11, I2C1_SDA, URT0_RX, URT2_RX, URT1_RX, TM36_OC3H, TM26_OC01, MAD14, MAD7, URT7_RX                      |                           |
| 38  | PC12 | GPC12, IR_OUT, DAC_TRG0, URT1_DE, TM10_TRGO, TM36_OC3, TM26_OC02, MAD15, SDT_P0                             |                           |
| 39  | PC13 | GPC13, XIN, URT1_NSS, URT0_CTS, URT2_RX, TM10_ETR, TM26_ETR, TM36_OC00, TM20_IC0, SDT_I0, URT6_RX           |                           |
| 40  | PC14 | GPC14, XOUT, URT1_TMO, URT0_RTS, URT2_TX, TM10_CKO, TM26_TRGO, TM36_OC10, TM20_IC1, SDT_I1, URT6_TX         |                           |
| 41  | VSS1 |                                                                                                             |                           |
| 42  | PD0  | GPD0, OBM_I0, TM10_CKO, URT0_CLK, TM26_OC1N, TM20_CKO, TM36_OC2, SPI0_NSS, MA0, MCLK, URT2_NSS              |                           |
| 43  | PD1  | GPD1, OBM_I1, TM16_CKO, URT0_CLK, NCO_CK0, TM26_CKO, TM36_OC2N, SPI0_CLK, MA1,                              |                           |

|    |              |                                                                                                   |        |
|----|--------------|---------------------------------------------------------------------------------------------------|--------|
|    |              | URT2_CLK                                                                                          |        |
| 44 | <b>PD2</b>   | GPD2, TM00_CKO, URT1_CLK, TM26_OC00, TM20_CKO, TM36_CKO, SPI0_MOSI, MA2, MAD4, URT2_TX            |        |
| 45 | <b>PD3</b>   | GPD3, TM01_CKO, URT1_CLK, SPI0_MISO, TM26_CKO, SPI0_D3, MA3, MAD7, TM36_TRGO, URT2_RX             |        |
| 46 | <b>PD4</b>   | GPD4, TM00_TRGO, TM01_TRGO, URT1_TX, TM26_OC00, SPI0_D2, MA4, MAD6, URT2_TX                       |        |
| 47 | <b>PD5</b>   | GPD5, TM00_ETR, I2C0_SCL, URT1_RX, TM26_OC01, SPI0_MISO, MA5, MAD5, URT2_RX                       |        |
| 48 | <b>PD6</b>   | GPD6, CPU_NMI, I2C0_SDA, URT1_NSS, SPI0_NSSI, TM26_OC02, SPI0_NSS, MA6, SDT_P0, URT2_NSS          |        |
| 49 | <b>PD7</b>   | GPD7, TM00_CKO, TM01_ETR, URT1_DE, SPI0_MISO, TM26_OC0N, SPI0_D4, MA7, MAD0, TM36_IC0             |        |
| 50 | <b>PD8</b>   | GPD8, CPU_TXEV, TM01_TRGO, URT1_RTS, SPI0_D2, TM26_OC10, SPI0_D7, MA8, MAD3, TM36_IC1, SPI0_CLK   |        |
| 51 | <b>PD9</b>   | GPD9, CPU_RXEV, TM00_TRGO, URT1_CTS, SPI0_NSSI, TM26_OC11, SPI0_D6, MA9, MAD2, TM36_IC2, SPI0_NSS |        |
| 52 | <b>PD10</b>  | GPD10, CPU_NMI, TM00_ETR, URT1_BRO, RTC_OUT, TM26_OC12, SPI0_D5, MA10, MAD1, TM36_IC3, SPI0_MOSI  |        |
| 53 | <b>PD11</b>  | GPD11, CPU_NMI, DMA_TRG1, URT1_TMO, SPI0_D3, TM26_OC1N, SPI0_NSS, MA11, MWE                       |        |
| 54 | <b>VSS</b>   |                                                                                                   |        |
| 55 | <b>VR0</b>   |                                                                                                   |        |
| 56 | <b>VDD</b>   |                                                                                                   |        |
| 57 | <b>VREF+</b> |                                                                                                   |        |
| 58 | <b>PA0</b>   | GPA0, SDT_P0, CCL_P0, MA0, MAD0, TM36_OC00, URT4_TX                                               | ADC_I0 |
| 59 | <b>PA1</b>   | GPA1, CCL_P1, MA1, MAD1, TM36_OC10, URT4_RX                                                       | ADC_I1 |
| 60 | <b>PA2</b>   | GPA2, SDT_I0, MA2, MAD2, TM36_OC2, URT5_TX                                                        | ADC_I2 |
| 61 | <b>PA3</b>   | GPA3, SDT_I1, MA3, MAD3, TM36_OC2N, URT5_RX                                                       | ADC_I3 |
| 62 | <b>PA4</b>   | GPA4, MA4, MAD4, TM20_OC00, URT0_TX                                                               | ADC_I4 |
| 63 | <b>PA5</b>   | GPA5, MA5, MAD5, TM20_OC10, URT0_RX                                                               | ADC_I5 |
| 64 | <b>PA6</b>   | GPA6, SPI0_D3, MA6, MAD6, TM20_OC0H, URT0_CLK                                                     | ADC_I6 |

MG32F02A128/A064

4.1.3. LQFP48 Package Pinout

Figure 4-3. LQFP48 Package Pinout



2020\_0515

Table 4-3. LQFP48 Pin AFS List

| Pin | Name | Pin AFS List                                                                                             | Analog Function           |
|-----|------|----------------------------------------------------------------------------------------------------------|---------------------------|
| 1   | PA8  | GPA8, DMA_TRG0, I2C0_SCL, URT2_BRO, SDT_I0, TM20_IC0, SPI0_NSS, MA8, MAD0, TM36_OC0H, URT4_TX            | ADC_I8, CMP0_I0, VBG_OUT  |
| 2   | PA9  | GPA9, DMA_TRG1, I2C1_SCL, URT2_TMO, TM20_IC1, SPI0_MISO, MA9, MAD1, TM36_OC1H, URT5_TX                   | ADC_I9, CMP0_I1           |
| 3   | PA10 | GPA10, TM36_BK0, SPI0_D2, I2C0_SDA, URT2_CTS, SDT_I1, TM26_IC0, SPI0_CLK, MA10, MAD2, TM36_OC2H, URT4_RX | ADC_I10, CMP1_I0, ADC_PGA |
| 4   | PA11 | GPA11, DAC_TRG0, SPI0_D3, I2C1_SDA, URT2_RTS, TM26_IC1, SPI0_MOSI, MA11, MAD3, TM36_OC3H, URT5_RX        | ADC_I11, CMP1_I1          |
| 5   | PA12 | GPA12, URT1_BRO, TM10_ETR, TM36_IC0, SPI0_D5, MA12, MAD4, TM26_OC00, URT6_TX                             | ADC_I12                   |

|    |       |                                                                                                             |         |
|----|-------|-------------------------------------------------------------------------------------------------------------|---------|
| 6  | PA13  | GPA13, CPU_TXEV, URT0_BRO, URT1_TMO, TM10_TRGO, TM36_IC1, SPI0_D6, MA13, MAD5, TM26_OC10, URT6_RX           | ADC_I13 |
| 7  | PA14  | GPA14, CPU_RXEV, OBM_I0, URT0_TMO, URT1_CTS, TM16_ETR, TM36_IC2, SPI0_D7, MA14, MAD6, TM26_OC0H, URT7_TX    | ADC_I14 |
| 8  | PA15  | GPA15, CPU_NMI, OBM_I1, URT0_DE, URT1_RTS, TM16_TRGO, TM36_IC3, SPI0_D4, MA15, MAD7, TM26_OC1H, URT7_RX     | ADC_I15 |
| 9  | PB0   | GPB0, I2C1_SCL, SPI0_NSS, TM01_ETR, TM00_CKO, TM16_ETR, TM26_IC0, TM36_ETR, MA15, URT1_NSS, URT6_TX         | CMP_C0  |
| 10 | PB1   | GPB1, I2C1_SDA, SPI0_MISO, TM01_TRGO, TM10_CKO, TM16_TRGO, TM26_IC1, TM36_TRGO, URT1_RX, URT6_RX            | CMP_C1  |
| 11 | PB2   | GPB2, ADC0_TRG, SPI0_CLK, TM01_CKO, URT2_TX, TM16_CKO, TM26_OC0H, I2C0_SDA, URT1_CLK, URT0_TX, URT7_TX      | DAC_P0  |
| 12 | PB3   | GPB3, ADC0_OUT, SPI0_MOSI, NCO_P0, URT2_RX, TM36_CKO, TM26_OC1H, I2C0_SCL, URT1_TX, URT0_RX, URT7_RX        |         |
| 13 | PB8   | GPB8, CMP0_P0, RTC_OUT, URT0_TX, URT2_BRO, TM20_OC01, TM36_OC01, SPI0_D3, MAD0, SDT_P0, OBM_P0, URT4_TX     |         |
| 14 | PB9   | GPB9, CMP1_P0, RTC_TS, URT0_RX, URT2_TMO, TM20_OC02, TM36_OC02, SPI0_D2, MAD1, MAD8, OBM_P1, URT4_RX        |         |
| 15 | PB10  | GPB10, I2C0_SCL, URT0_NSS, URT2_DE, TM20_OC11, TM36_OC11, URT1_TX, MAD2, MAD1, SPI0_NSSI                    |         |
| 16 | PB11  | GPB11, I2C0_SDA, URT0_DE, IR_OUT, TM20_OC12, TM36_OC12, URT1_RX, MAD3, MAD9, DMA_TRG0, URT0_CLK             |         |
| 17 | PB13  | GPB13, DAC_TRG0, TM00_ETR, URT0_CTS, TM20_ETR, TM36_ETR, URT0_CLK, MAD5, MAD10, CCL_P0, URT4_RX             |         |
| 18 | PB14  | GPB14, DMA_TRG0, TM00_TRGO, URT0_RTS, TM20_TRGO, TM36_BK0, URT0_NSS, MAD6, MAD3, CCL_P1, URT4_TX            |         |
| 19 | PC0   | GPC0, ICKO, TM00_CKO, URT0_CLK, URT2_CLK, TM20_OC00, TM36_OC00, I2C0_SCL, MCLK, MWE, URT0_TX, URT5_TX       |         |
| 20 | PC1   | GPC1, ADC0_TRG, TM01_CKO, TM36_IC0, URT1_CLK, TM20_OC0N, TM36_OC0N, I2C0_SDA, MAD8, MAD4, URT0_RX, URT5_RX  |         |
| 21 | PC2   | GPC2, ADC0_OUT, TM10_CKO, OBM_P0, URT2_CLK, TM20_OC10, TM36_OC10, SDT_I0, MAD9, MAD12                       |         |
| 22 | PC3   | GPC3, OBM_P1, TM16_CKO, URT0_CLK, URT1_CLK, TM20_OC1N, TM36_OC1N, SDT_I1, MAD10, MAD5                       |         |
| 23 | PC4   | GPC4, SWCLK, I2C0_SCL, URT0_RX, URT1_RX, TM36_OC2, SDT_I0, URT6_RX                                          |         |
| 24 | PC5   | GPC5, SWDIO, I2C0_SDA, URT0_TX, URT1_TX, TM36_OC3, SDT_I1, URT6_TX                                          |         |
| 25 | PC6   | GPC6, RSTN, RTC_TS, URT0_NSS, URT1_NSS, TM20_ETR, TM26_ETR, MBW1, MALE                                      |         |
| 26 | PC8   | GPC8, ADC0_OUT, I2C0_SCL, URT0_BRO, URT1_TX, TM20_OC0H, TM36_OC0H, TM36_OC0N, MAD11, MAD13, CCL_P0, URT6_TX |         |
| 27 | PC9   | GPC9, CMP0_P0, I2C0_SDA, URT0_TMO, URT1_RX, TM20_OC1H, TM36_OC1H, TM36_OC1N, MAD12, MAD6, CCL_P1, URT6_RX   |         |
| 28 | PC10  | GPC10, CMP1_P0, I2C1_SCL, URT0_TX, URT2_TX, URT1_TX, TM36_OC2H, TM36_OC2N, MAD13, MAD14, URT7_TX            |         |
| 29 | PC11  | GPC11, I2C1_SDA, URT0_RX, URT2_RX, URT1_RX, TM36_OC3H, TM26_OC01, MAD14, MAD7, URT7_RX                      |         |
| 30 | PC12  | GPC12, IR_OUT, DAC_TRG0, URT1_DE, TM10_TRGO, TM36_OC3, TM26_OC02, MAD15, SDT_P0                             |         |
| 31 | PC13  | GPC13, XIN, URT1_NSS, URT0_CTS, URT2_RX, TM10_ETR, TM26_ETR, TM36_OC00, TM20_IC0, SDT_I0, URT6_RX           |         |
| 32 | PC14  | GPC14, XOUT, URT1_TMO, URT0_RTS, URT2_TX, TM10_CKO, TM26_TRGO, TM36_OC10, TM20_IC1, SDT_I1, URT6_TX         |         |
| 33 | PD0   | GPD0, OBM_I0, TM10_CKO, URT0_CLK, TM26_OC1N, TM20_CKO, TM36_OC2, SPI0_NSS, MA0, MCLK, URT2_NSS              |         |
| 34 | PD1   | GPD1, OBM_I1, TM16_CKO, URT0_CLK, NCO_CKO, TM26_CKO, TM36_OC2N, SPI0_CLK, MA1, URT2_CLK                     |         |
| 35 | PD2   | GPD2, TM00_CKO, URT1_CLK, TM26_OC00, TM20_CKO, TM36_CKO, SPI0_MOSI, MA2, MAD4, URT2_TX                      |         |
| 36 | PD3   | GPD3, TM01_CKO, URT1_CLK, SPI0_MISO, TM26_CKO, SPI0_D3, MA3, MAD7, TM36_TRGO, URT2_RX                       |         |
| 37 | PD7   | GPD7, TM00_CKO, TM01_ETR, URT1_DE, SPI0_MISO, TM26_OC0N, SPI0_D4, MA7, MAD0, TM36_IC0                       |         |
| 38 | PD8   | GPD8, CPU_TXEV, TM01_TRGO, URT1_RTS, SPI0_D2, TM26_OC10, SPI0_D7, MA8, MAD3, TM36_IC1, SPI0_CLK             |         |
| 39 | PD9   | GPD9, CPU_RXEV, TM00_TRGO, URT1_CTS, SPI0_NSSI, TM26_OC11, SPI0_D6, MA9, MAD2, TM36_IC2, SPI0_NSS           |         |
| 40 | PD10  | GPD10, CPU_NMI, TM00_ETR, URT1_BRO, RTC_OUT, TM26_OC12, SPI0_D5, MA10, MAD1, TM36_IC3, SPI0_MOSI            |         |
| 41 | VSS   |                                                                                                             |         |
| 42 | VR0   |                                                                                                             |         |
| 43 | VDD   |                                                                                                             |         |
| 44 | VREF+ |                                                                                                             |         |
| 45 | PA0   | GPA0, SDT_P0, CCL_P0, MA0, MAD0, TM36_OC00, URT4_TX                                                         | ADC_I0  |
| 46 | PA1   | GPA1, CCL_P1, MA1, MAD1, TM36_OC10, URT4_RX                                                                 | ADC_I1  |
| 47 | PA2   | GPA2, SDT_I0, MA2, MAD2, TM36_OC2, URT5_TX                                                                  | ADC_I2  |
| 48 | PA3   | GPA3, SDT_I1, MA3, MAD3, TM36_OC2N, URT5_RX                                                                 | ADC_I3  |

## 4.2. Pin Definition

Table 4-4. Abbreviations for pin definition

| IO Type |                     | IO Structure |                                       |
|---------|---------------------|--------------|---------------------------------------|
| P       | Power/Ground pin    | I            | Digital Input                         |
| B       | Bidirectional       | P            | Output Push-pull capability           |
| I       | Input               | O            | Output Open drain capability          |
| O       | Output              | Q            | Quasi-bidirectional                   |
| A       | Analog I/O          | A            | Analog I/O (Digital I/O disable)      |
| AO      | Analog output only  | U            | Internal pull-up                      |
| AI      | Analog input only   | H            | High Speed                            |
| Q       | Quasi-bidirectional | C2           | Programmable 2-level driving strength |
| -       |                     | C4           | Programmable 4-level driving strength |
| -       |                     | CF           | Fixed driving strength(GPIO mode)     |

Table 4-5. Pin Descriptions

| Pin Name | Pin Number |        |        | IO Type | Default |       | IO Structure   | Alternate Functions | Description                                                                      |
|----------|------------|--------|--------|---------|---------|-------|----------------|---------------------|----------------------------------------------------------------------------------|
|          | LQFP80     | LQFP64 | LQFP48 |         | Type    | Value |                |                     |                                                                                  |
| PA0      | 74         | 58     | 45     | B       | A       |       | A,I,P,O,U,H,C2 | GPA0                | GPIO/Interrupt/KBI Port-A function pin-0                                         |
|          |            |        |        |         |         |       |                | SDT_P0              | SDT output signal-0                                                              |
|          |            |        |        |         |         |       |                | CCL_P0              | CCL output signal-0                                                              |
|          |            |        |        |         |         |       |                | MA0                 | External memory bus address pin 0                                                |
|          |            |        |        |         |         |       |                | MAD0                | External memory bus address/data pin 0                                           |
|          |            |        |        |         |         |       |                | TM36_OC00           | TM36 output compare/PWM channel-00                                               |
|          |            |        |        |         |         |       |                | URT4_TX             | URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting. |
| PA1      | 75         | 59     | 46     | B       | A       |       | A,I,P,O,U,H,C2 | ADC_I0              | ADC analog single-end input channel 0                                            |
|          |            |        |        |         |         |       |                | GPA1                | GPIO/Interrupt/KBI Port-A function pin-1                                         |
|          |            |        |        |         |         |       |                | CCL_P1              | CCL output signal-1                                                              |
|          |            |        |        |         |         |       |                | MA1                 | External memory bus address pin 1                                                |
|          |            |        |        |         |         |       |                | MAD1                | External memory bus address/data pin 1                                           |
|          |            |        |        |         |         |       |                | TM36_OC10           | TM36 output compare/PWM channel-10                                               |
|          |            |        |        |         |         |       |                | URT4_RX             | URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.  |
| PA2      | 76         | 60     | 47     | B       | A       |       | A,I,P,O,U,H,C2 | ADC_I1              | ADC analog single-end input channel 1                                            |
|          |            |        |        |         |         |       |                | GPA2                | GPIO/Interrupt/KBI Port-A function pin-2                                         |
|          |            |        |        |         |         |       |                | SDT_I0              | State detect input signal-0                                                      |
|          |            |        |        |         |         |       |                | MA2                 | External memory bus address pin 2                                                |
|          |            |        |        |         |         |       |                | MAD2                | External memory bus address/data pin 2                                           |
|          |            |        |        |         |         |       |                | TM36_OC2            | TM36 output compare/PWM channel-2                                                |
|          |            |        |        |         |         |       |                | URT5_TX             | URT5 transmit TX signal. URT5_RX and URT5_TX can be swapped by register setting. |
| PA3      | 77         | 61     | 48     | B       | A       |       | A,I,P,O,U,H,C2 | ADC_I2              | ADC analog single-end input channel 2                                            |
|          |            |        |        |         |         |       |                | GPA3                | GPIO/Interrupt/KBI Port-A function pin-3                                         |
|          |            |        |        |         |         |       |                | SDT_I1              | State detect input signal-1                                                      |
|          |            |        |        |         |         |       |                | MA3                 | External memory bus address pin 3                                                |
|          |            |        |        |         |         |       |                | MAD3                | External memory bus address/data pin 3                                           |

|     |    |    |   |   |   |                |           |                                                                                                                       |
|-----|----|----|---|---|---|----------------|-----------|-----------------------------------------------------------------------------------------------------------------------|
|     |    |    |   |   |   |                | TM36_OC2N | TM36 output compare/PWM complement channel-2                                                                          |
|     |    |    |   |   |   |                | URT5_RX   | URT5 receive RX signal. URT5_RX and URT5_TX can be swapped by register setting.                                       |
|     |    |    |   |   |   |                | ADC_I3    | ADC analog single-end input channel 3                                                                                 |
| PA4 | 78 | 62 |   | B | A | A,I,P,O,U,H,C2 | GPA4      | GPIO/Interrupt/KBI Port-A function pin-4                                                                              |
|     |    |    |   |   |   |                | MA4       | External memory bus address pin 4                                                                                     |
|     |    |    |   |   |   |                | MAD4      | External memory bus address/data pin 4                                                                                |
|     |    |    |   |   |   |                | TM20_OC00 | TM20 output compare/PWM channel-00                                                                                    |
|     |    |    |   |   |   |                | URT0_TX   | URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting. |
|     |    |    |   |   |   |                | ADC_I4    | ADC analog single-end input channel 4                                                                                 |
|     |    |    |   |   |   |                |           |                                                                                                                       |
| PA5 | 79 | 63 |   | B | A | A,I,P,O,U,H,C2 | GPA5      | GPIO/Interrupt/KBI Port-A function pin-5                                                                              |
|     |    |    |   |   |   |                | MA5       | External memory bus address pin 5                                                                                     |
|     |    |    |   |   |   |                | MAD5      | External memory bus address/data pin 5                                                                                |
|     |    |    |   |   |   |                | TM20_OC10 | TM20 output compare/PWM channel-10                                                                                    |
|     |    |    |   |   |   |                | URT0_RX   | URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting.   |
|     |    |    |   |   |   |                | ADC_I5    | ADC analog single-end input channel 5                                                                                 |
| PA6 | 80 | 64 |   | B | A | A,I,P,O,U,H,C2 | GPA6      | GPIO/Interrupt/KBI Port-A function pin-6                                                                              |
|     |    |    |   |   |   |                | SPI0_D3   | SPI0 data-3 signal for 4-I/O mode                                                                                     |
|     |    |    |   |   |   |                | MA6       | External memory bus address pin 6                                                                                     |
|     |    |    |   |   |   |                | MAD6      | External memory bus address/data pin 6                                                                                |
|     |    |    |   |   |   |                | TM20_OC0H | TM20 output compare/PWM high channel-0                                                                                |
|     |    |    |   |   |   |                | URT0_CLK  | URT0 clock signal                                                                                                     |
|     |    |    |   |   |   |                | ADC_I6    | ADC analog single-end input channel 6                                                                                 |
| PA7 | 1  | 1  |   | B | A | A,I,P,O,U,H,C2 | GPA7      | GPIO/Interrupt/KBI Port-A function pin-7                                                                              |
|     |    |    |   |   |   |                | SPI0_D2   | SPI0 data-2 signal for 4-I/O mode                                                                                     |
|     |    |    |   |   |   |                | MA7       | External memory bus address pin 7                                                                                     |
|     |    |    |   |   |   |                | MAD7      | External memory bus address/data pin 7                                                                                |
|     |    |    |   |   |   |                | TM20_OC1H | TM20 output compare/PWM high channel-1                                                                                |
|     |    |    |   |   |   |                | URT0_NSS  | URT0 SPI NSS input/output signal                                                                                      |
|     |    |    |   |   |   |                | ADC_I7    | ADC analog single-end input channel 7                                                                                 |
| PA8 | 2  | 2  | 1 | B | A | A,I,P,O,U,H,C2 | GPA8      | GPIO/Interrupt/KBI Port-A function pin-8                                                                              |
|     |    |    |   |   |   |                | DMA_TRG0  | DMA external trigger pin-0 input                                                                                      |
|     |    |    |   |   |   |                | I2C0_SCL  | I2C0 SCL signal                                                                                                       |
|     |    |    |   |   |   |                | URT2_BRO  | URT2 baud-rate timer overflow output signal                                                                           |
|     |    |    |   |   |   |                | SDT_I0    | State detect input signal-0                                                                                           |
|     |    |    |   |   |   |                | TM20_IC0  | TM20 input capture channel-0                                                                                          |
|     |    |    |   |   |   |                | SPI0_NSS  | SPI0 slave select input/output signal                                                                                 |
|     |    |    |   |   |   |                | MA8       | External memory bus address pin 8                                                                                     |
|     |    |    |   |   |   |                | MAD0      | External memory bus address/data pin 0                                                                                |
|     |    |    |   |   |   |                | TM36_OC0H | TM36 output compare/PWM high channel-0                                                                                |
|     |    |    |   |   |   |                | URT4_TX   | URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.                                      |
|     |    |    |   |   |   |                | ADC_I8    | ADC analog single-end input channel 8                                                                                 |

|      |   |   |   |   |   |  |                |           |                                                                                                                                      |
|------|---|---|---|---|---|--|----------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------|
|      |   |   |   |   |   |  |                | CMP0_I0   | Comparator-0 analog input channel 0                                                                                                  |
|      |   |   |   |   |   |  |                | VBG_OUT   | Bandgap voltage output                                                                                                               |
| PA9  | 3 | 3 | 2 | B | A |  | A,I,P,O,U,H,C2 | GPA9      | GPIO/Interrupt/KBI Port-A function pin-9                                                                                             |
|      |   |   |   |   |   |  |                | DMA_TRG1  | DMA external trigger pin-1 input                                                                                                     |
|      |   |   |   |   |   |  |                | I2C1_SCL  | I2C1 SCL signal                                                                                                                      |
|      |   |   |   |   |   |  |                | URT2_TMO  | URT2 timeout timer overflow output signal                                                                                            |
|      |   |   |   |   |   |  |                | TM20_IC1  | TM20 input capture channel-1                                                                                                         |
|      |   |   |   |   |   |  |                | SPI0_MISO | SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting. |
|      |   |   |   |   |   |  |                | MA9       | External memory bus address pin 9                                                                                                    |
|      |   |   |   |   |   |  |                | MAD1      | External memory bus address/data pin 1                                                                                               |
|      |   |   |   |   |   |  |                | TM36_OC1H | TM36 output compare/PWM high channel-1                                                                                               |
|      |   |   |   |   |   |  |                | URT5_TX   | URT5 transmit TX signal. URT5_RX and URT5_TX can be swapped by register setting.                                                     |
|      |   |   |   |   |   |  |                | ADC_I9    | ADC analog single-end input channel 9                                                                                                |
|      |   |   |   |   |   |  |                | CMP0_I1   | Comparator-0 analog input channel 1                                                                                                  |
| PA10 | 4 | 4 | 3 | B | A |  | A,I,P,O,U,H,C2 | GPA10     | GPIO/Interrupt/KBI Port-A function pin-10                                                                                            |
|      |   |   |   |   |   |  |                | TM36_BK0  | TM36 break input signal                                                                                                              |
|      |   |   |   |   |   |  |                | SPI0_D2   | SPI0 data-2 signal for 4-I/O mode                                                                                                    |
|      |   |   |   |   |   |  |                | I2C0_SDA  | I2C0 SDA signal                                                                                                                      |
|      |   |   |   |   |   |  |                | URT2_CTS  | URT2 CTS input control signal                                                                                                        |
|      |   |   |   |   |   |  |                | SDT_I1    | State detect input signal-1                                                                                                          |
|      |   |   |   |   |   |  |                | TM26_IC0  | TM26 input capture channel-0                                                                                                         |
|      |   |   |   |   |   |  |                | SPI0_CLK  | SPI0 clock signal                                                                                                                    |
|      |   |   |   |   |   |  |                | MA10      | External memory bus address pin 10                                                                                                   |
|      |   |   |   |   |   |  |                | MAD2      | External memory bus address/data pin 2                                                                                               |
|      |   |   |   |   |   |  |                | TM36_OC2H | TM36 output compare/PWM high channel-2                                                                                               |
|      |   |   |   |   |   |  |                | URT4_RX   | URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.                                                      |
|      |   |   |   |   |   |  |                | ADC_I10   | ADC analog single-end input channel 10                                                                                               |
|      |   |   |   |   |   |  |                | CMP1_I0   | Comparator-1 analog input channel 0                                                                                                  |
|      |   |   |   |   |   |  |                | ADC_PGA   | ADC PGA voltage output                                                                                                               |
| PA11 | 5 | 5 | 4 | B | A |  | A,I,P,O,U,H,C2 | GPA11     | GPIO/Interrupt/KBI Port-A function pin-11                                                                                            |
|      |   |   |   |   |   |  |                | DAC_TRG0  | DAC trigger start input                                                                                                              |
|      |   |   |   |   |   |  |                | SPI0_D3   | SPI0 data-3 signal for 4-I/O mode                                                                                                    |
|      |   |   |   |   |   |  |                | I2C1_SDA  | I2C1 SDA signal                                                                                                                      |
|      |   |   |   |   |   |  |                | URT2_RTS  | URT2 RTS output control signal                                                                                                       |
|      |   |   |   |   |   |  |                | TM26_IC1  | TM26 input capture channel-1                                                                                                         |
|      |   |   |   |   |   |  |                | SPI0_MOSI | SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting. |
|      |   |   |   |   |   |  |                | MA11      | External memory bus address pin 11                                                                                                   |
|      |   |   |   |   |   |  |                | MAD3      | External memory bus address/data pin 3                                                                                               |
|      |   |   |   |   |   |  |                | TM36_OC3H | TM36 output compare/PWM high channel-3                                                                                               |
|      |   |   |   |   |   |  |                | URT5_RX   | URT5 receive RX signal. URT5_RX and URT5_TX can be swapped by register setting.                                                      |
|      |   |   |   |   |   |  |                | ADC_I11   | ADC analog single-end input channel 11                                                                                               |

|      |   |   |   |   |   |                |           |                                                                                  |
|------|---|---|---|---|---|----------------|-----------|----------------------------------------------------------------------------------|
| PA12 | 6 | 6 | 5 | B | A | A,I,P,O,U,H,C2 | CMP1_I1   | Comparator-1 analog input channel 1                                              |
|      |   |   |   |   |   |                | GPA12     | GPIO/Interrupt/KBI Port-A function pin-12                                        |
|      |   |   |   |   |   |                |           |                                                                                  |
|      |   |   |   |   |   |                | URT1_BRO  | URT1 baud-rate timer overflow output signal                                      |
|      |   |   |   |   |   |                | TM10_ETR  | TM10 external trigger/clock input signal                                         |
|      |   |   |   |   |   |                | TM36_IC0  | TM36 input capture channel-0                                                     |
|      |   |   |   |   |   |                | SPI0_D5   | SPI0 data-1 signal for 2nd SPI device 4-I/O mode                                 |
|      |   |   |   |   |   |                | MA12      | External memory bus address pin 12                                               |
|      |   |   |   |   |   |                | MAD4      | External memory bus address/data pin 4                                           |
|      |   |   |   |   |   |                | TM26_OC00 | TM26 output compare/PWM channel-00                                               |
| PA13 | 7 | 7 | 6 | B | A | A,I,P,O,U,H,C2 | URT6_TX   | URT6 transmit TX signal. URT6_RX and URT6_TX can be swapped by register setting. |
|      |   |   |   |   |   |                | ADC_I12   | ADC analog single-end input channel 12                                           |
|      |   |   |   |   |   |                | GPA13     | GPIO/Interrupt/KBI Port-A function pin-13                                        |
|      |   |   |   |   |   |                | CPU_TXEV  | CPU wakeup event output                                                          |
|      |   |   |   |   |   |                |           |                                                                                  |
|      |   |   |   |   |   |                | URT0_BRO  | URT0 baud-rate timer overflow output signal                                      |
|      |   |   |   |   |   |                | URT1_TMO  | URT1 timeout timer overflow output signal                                        |
|      |   |   |   |   |   |                | TM10_TRGO | TM10 trigger output signal                                                       |
|      |   |   |   |   |   |                | TM36_IC1  | TM36 input capture channel-1                                                     |
|      |   |   |   |   |   |                | SPI0_D6   | SPI0 data-2 signal for 2nd SPI device 4-I/O mode                                 |
| PA14 | 8 | 8 | 7 | B | A | A,I,P,O,U,H,C2 | MA13      | External memory bus address pin 13                                               |
|      |   |   |   |   |   |                | MAD5      | External memory bus address/data pin 5                                           |
|      |   |   |   |   |   |                | TM26_OC10 | TM26 output compare/PWM channel-10                                               |
|      |   |   |   |   |   |                | URT6_RX   | URT6 receive RX signal. URT6_RX and URT6_TX can be swapped by register setting.  |
|      |   |   |   |   |   |                | ADC_I13   | ADC analog single-end input channel 13                                           |
|      |   |   |   |   |   |                | GPA14     | GPIO/Interrupt/KBI Port-A function pin-14                                        |
|      |   |   |   |   |   |                | CPU_RXEV  | CPU wakeup event input                                                           |
|      |   |   |   |   |   |                | OBM_I0    | Output signal break control input signal-0                                       |
|      |   |   |   |   |   |                | URT0_TMO  | URT0 timeout timer overflow output signal                                        |
|      |   |   |   |   |   |                | URT1_CTS  | URT1 CTS input control signal                                                    |
| PA15 | 9 | 9 | 8 | B | A | A,I,P,O,U,H,C2 | TM16_ETR  | TM16 external trigger/clock input signal                                         |
|      |   |   |   |   |   |                | TM36_IC2  | TM36 input capture channel-2                                                     |
|      |   |   |   |   |   |                | SPI0_D7   | SPI0 data-3 signal for 2nd SPI device 4-I/O mode                                 |
|      |   |   |   |   |   |                | MA14      | External memory bus address pin 14                                               |
|      |   |   |   |   |   |                | MAD6      | External memory bus address/data pin 6                                           |
|      |   |   |   |   |   |                | TM26_OC0H | TM26 output compare/PWM high channel-0                                           |
|      |   |   |   |   |   |                | URT7_TX   | URT7 transmit TX signal. URT7_RX and URT7_TX can be swapped by register setting. |
|      |   |   |   |   |   |                | ADC_I14   | ADC analog single-end input channel 14                                           |
|      |   |   |   |   |   |                | GPA15     | GPIO/Interrupt/KBI Port-A function pin-15                                        |
|      |   |   |   |   |   |                | CPU_NMI   | CPU NMI external pin input                                                       |
|      |   |   |   |   |   |                | OBM_I1    | Output signal break control input signal-1                                       |
|      |   |   |   |   |   |                | URT0_DE   | URT0 external drive enable output signal                                         |

|     |    |    |    |   |   |  |                |           |                                                                                                                                      |
|-----|----|----|----|---|---|--|----------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------|
|     |    |    |    |   |   |  |                | URT1_RTS  | URT1 RTS output control signal                                                                                                       |
|     |    |    |    |   |   |  |                | TM16_TRGO | TM16 trigger output signal                                                                                                           |
|     |    |    |    |   |   |  |                | TM36_IC3  | TM36 input capture channel-3                                                                                                         |
|     |    |    |    |   |   |  |                | SPI0_D4   | SPI0 data-0 signal for 2nd SPI device 4-I/O mode                                                                                     |
|     |    |    |    |   |   |  |                | MA15      | External memory bus address pin 15                                                                                                   |
|     |    |    |    |   |   |  |                | MAD7      | External memory bus address/data pin 7                                                                                               |
|     |    |    |    |   |   |  |                | TM26_OC1H | TM26 output compare/PWM high channel-1                                                                                               |
|     |    |    |    |   |   |  |                | URT7_RX   | URT7 receive RX signal. URT7_RX and URT7_TX can be swapped by register setting.                                                      |
|     |    |    |    |   |   |  |                | ADC_I15   | ADC analog single-end input channel 15                                                                                               |
| PB0 | 10 | 10 | 9  | B | A |  | A,I,P,O,U,H,C4 | GPB0      | GPIO/Interrupt/KBI Port-B function pin-0                                                                                             |
|     |    |    |    |   |   |  |                | I2C1_SCL  | I2C1 SCL signal                                                                                                                      |
|     |    |    |    |   |   |  |                | SPI0_NSS  | SPI0 slave select input/output signal                                                                                                |
|     |    |    |    |   |   |  |                | TM01_ETR  | TM01 external trigger/clock input signal                                                                                             |
|     |    |    |    |   |   |  |                | TM00_CKO  | TM00 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | TM16_ETR  | TM16 external trigger/clock input signal                                                                                             |
|     |    |    |    |   |   |  |                | TM26_IC0  | TM26 input capture channel-0                                                                                                         |
|     |    |    |    |   |   |  |                | TM36_ETR  | TM36 external trigger/clock input signal                                                                                             |
|     |    |    |    |   |   |  |                | MA15      | External memory bus address pin 15                                                                                                   |
|     |    |    |    |   |   |  |                | URT1_NSS  | URT1 SPI NSS input/output signal                                                                                                     |
|     |    |    |    |   |   |  |                | URT2_NSS  | URT2 SPI NSS input/output signal                                                                                                     |
|     |    |    |    |   |   |  |                | URT6_TX   | URT6 transmit TX signal. URT6_RX and URT6_TX can be swapped by register setting.                                                     |
|     |    |    |    |   |   |  |                | CMP_C0    | Comparator analog input common channel 0                                                                                             |
| PB1 | 11 | 11 | 10 | B | A |  | A,I,P,O,U,H,C4 | GPB1      | GPIO/Interrupt/KBI Port-B function pin-1                                                                                             |
|     |    |    |    |   |   |  |                | I2C1_SDA  | I2C1 SDA signal                                                                                                                      |
|     |    |    |    |   |   |  |                | SPI0_MISO | SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting. |
|     |    |    |    |   |   |  |                | TM01_TRGO | TM01 trigger output signal                                                                                                           |
|     |    |    |    |   |   |  |                | TM10_CKO  | TM10 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | TM16_TRGO | TM16 trigger output signal                                                                                                           |
|     |    |    |    |   |   |  |                | TM26_IC1  | TM26 input capture channel-1                                                                                                         |
|     |    |    |    |   |   |  |                | TM36_TRGO | TM36 trigger output signal                                                                                                           |
|     |    |    |    |   |   |  |                | URT1_RX   | URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.                  |
|     |    |    |    |   |   |  |                | URT2_CLK  | URT2 clock signal                                                                                                                    |
|     |    |    |    |   |   |  |                | URT6_RX   | URT6 receive RX signal. URT6_RX and URT6_TX can be swapped by register setting.                                                      |
|     |    |    |    |   |   |  |                | CMP_C1    | Comparator analog input common channel 1                                                                                             |
| PB2 | 12 | 12 | 11 | B | A |  | A,I,P,O,U,H,C4 | GPB2      | GPIO/Interrupt/KBI Port-B function pin-2                                                                                             |
|     |    |    |    |   |   |  |                | ADC0_TRG  | ADC trigger start input                                                                                                              |
|     |    |    |    |   |   |  |                | SPI0_CLK  | SPI0 clock signal                                                                                                                    |
|     |    |    |    |   |   |  |                | TM01_CKO  | TM01 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | URT2_TX   | URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be                                             |

|     |    |    |    |   |   |  |                |                                                                                                                       |                                                                                                                                      |
|-----|----|----|----|---|---|--|----------------|-----------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
|     |    |    |    |   |   |  |                |                                                                                                                       | swapped by register setting.                                                                                                         |
|     |    |    |    |   |   |  | TM16_CKO       | TM16 timer overflow output signal                                                                                     |                                                                                                                                      |
|     |    |    |    |   |   |  | TM26_OC0H      | TM26 output compare/PWM high channel-0                                                                                |                                                                                                                                      |
|     |    |    |    |   |   |  | I2C0_SDA       | I2C0 SDA signal                                                                                                       |                                                                                                                                      |
|     |    |    |    |   |   |  | URT1_CLK       | URT1 clock signal                                                                                                     |                                                                                                                                      |
|     |    |    |    |   |   |  | URT0_TX        | URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting. |                                                                                                                                      |
|     |    |    |    |   |   |  | URT7_TX        | URT7 transmit TX signal. URT7_RX and URT7_TX can be swapped by register setting.                                      |                                                                                                                                      |
|     |    |    |    |   |   |  | DAC_P0         | DAC analog output channel 0                                                                                           |                                                                                                                                      |
| PB3 | 13 | 13 | 12 | B | A |  | A,I,P,O,U,H,C4 | GPB3                                                                                                                  | GPIO/Interrupt/KBI Port-B function pin-3                                                                                             |
|     |    |    |    |   |   |  |                | ADC0_OUT                                                                                                              | ADC threshold window compare output                                                                                                  |
|     |    |    |    |   |   |  |                | SPI0_MOSI                                                                                                             | SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting. |
|     |    |    |    |   |   |  |                | NCO_P0                                                                                                                | NCO clock output signal-0                                                                                                            |
|     |    |    |    |   |   |  |                | URT2_RX                                                                                                               | URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.                  |
|     |    |    |    |   |   |  |                | TM36_CKO                                                                                                              | TM36 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | TM26_OC1H                                                                                                             | TM26 output compare/PWM high channel-1                                                                                               |
|     |    |    |    |   |   |  |                | I2C0_SCL                                                                                                              | I2C0 SCL signal                                                                                                                      |
|     |    |    |    |   |   |  |                | URT1_TX                                                                                                               | URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting.                |
|     |    |    |    |   |   |  |                | URT0_RX                                                                                                               | URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting.                  |
|     |    |    |    |   |   |  |                | URT7_RX                                                                                                               | URT7 receive RX signal. URT7_RX and URT7_TX can be swapped by register setting.                                                      |
| PB4 | 18 | 14 |    | B | A |  | A,I,P,O,U,H,C4 | GPB4                                                                                                                  | GPIO/Interrupt/KBI Port-B function pin-4                                                                                             |
|     |    |    |    |   |   |  |                | TM01_CKO                                                                                                              | TM01 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | SPI0_D3                                                                                                               | SPI0 data-3 signal for 4-I/O mode                                                                                                    |
|     |    |    |    |   |   |  |                | TM26_TRGO                                                                                                             | TM26 trigger output signal                                                                                                           |
|     |    |    |    |   |   |  |                | URT2_CLK                                                                                                              | URT2 clock signal                                                                                                                    |
|     |    |    |    |   |   |  |                | TM20_IC0                                                                                                              | TM20 input capture channel-0                                                                                                         |
|     |    |    |    |   |   |  |                | TM36_IC0                                                                                                              | TM36 input capture channel-0                                                                                                         |
|     |    |    |    |   |   |  |                | MALE                                                                                                                  | External memory bus address latch enable(ALE) or data/command select(DC) pin                                                         |
|     |    |    |    |   |   |  |                | MAD8                                                                                                                  | External memory bus address/data pin 8                                                                                               |
| PB5 | 19 | 15 |    | B | A |  | A,I,P,O,U,H,C4 | GPB5                                                                                                                  | GPIO/Interrupt/KBI Port-B function pin-5                                                                                             |
|     |    |    |    |   |   |  |                | TM16_CKO                                                                                                              | TM16 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | SPI0_D2                                                                                                               | SPI0 data-2 signal for 4-I/O mode                                                                                                    |
|     |    |    |    |   |   |  |                | TM26_ETR                                                                                                              | TM26 external trigger/clock input signal                                                                                             |
|     |    |    |    |   |   |  |                | URT2_NSS                                                                                                              | URT2 SPI NSS input/output signal                                                                                                     |
|     |    |    |    |   |   |  |                | TM20_IC1                                                                                                              | TM20 input capture channel-1                                                                                                         |
|     |    |    |    |   |   |  |                | TM36_IC1                                                                                                              | TM36 input capture channel-1                                                                                                         |

|     |    |    |    |   |   |  |                |           |                                                                                                                       |
|-----|----|----|----|---|---|--|----------------|-----------|-----------------------------------------------------------------------------------------------------------------------|
| PB6 | 20 | 16 |    | B | A |  | A,I,P,O,U,H,C2 | MOE       | External memory bus output enable(OE) or read strobe (RD) signal pin                                                  |
|     |    |    |    |   |   |  |                | MAD9      | External memory bus address/data pin 9                                                                                |
|     |    |    |    |   |   |  |                | GPB6      | GPIO/Interrupt/KBI Port-B function pin-6                                                                              |
|     |    |    |    |   |   |  |                | CPU_RXEV  | CPU wakeup event input                                                                                                |
|     |    |    |    |   |   |  |                | SPI0_NSSI | SPI0 slave select input only signal                                                                                   |
|     |    |    |    |   |   |  |                | URT0_BRO  | URT0 baud-rate timer overflow output signal                                                                           |
|     |    |    |    |   |   |  |                | URT2_CTS  | URT2 CTS input control signal                                                                                         |
|     |    |    |    |   |   |  |                | TM20_ETR  | TM20 external trigger/clock input signal                                                                              |
|     |    |    |    |   |   |  |                | TM36_IC2  | TM36 input capture channel-2                                                                                          |
|     |    |    |    |   |   |  |                | MWE       | External memory bus write enable(WE) or write strobe(WR) signal pin                                                   |
|     |    |    |    |   |   |  |                | MAD10     | External memory bus address/data pin 10                                                                               |
|     |    |    |    |   |   |  |                | URT2_TX   | URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting. |
| PB7 | 21 | 17 |    | B | A |  | A,I,P,O,U,H,C2 | GPB7      | GPIO/Interrupt/KBI Port-B function pin-7                                                                              |
|     |    |    |    |   |   |  |                | CPU_TXEV  | CPU wakeup event output                                                                                               |
|     |    |    |    |   |   |  |                | URT0_TMO  | URT0 timeout timer overflow output signal                                                                             |
|     |    |    |    |   |   |  |                | URT2_RTS  | URT2 RTS output control signal                                                                                        |
|     |    |    |    |   |   |  |                | TM20_TRGO | TM20 trigger output signal                                                                                            |
|     |    |    |    |   |   |  |                | TM36_IC3  | TM36 input capture channel-3                                                                                          |
|     |    |    |    |   |   |  |                | MCE       | External memory bus chip enable/select pin                                                                            |
|     |    |    |    |   |   |  |                | MALE2     | External memory bus 2nd address latch enable(ALE2) or command latch enable(CLE) pin                                   |
| PB8 | 22 | 18 | 13 | B | A |  | A,I,P,O,U,H,C4 | URT2_RX   | URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.   |
|     |    |    |    |   |   |  |                | GPB8      | GPIO/Interrupt/KBI Port-B function pin-8                                                                              |
|     |    |    |    |   |   |  |                | CMP0_P0   | Comparator-0 data output                                                                                              |
|     |    |    |    |   |   |  |                | RTC_OUT   | RTC selection output signal                                                                                           |
|     |    |    |    |   |   |  |                | URT0_TX   | URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting. |
|     |    |    |    |   |   |  |                | URT2_BRO  | URT2 baud-rate timer overflow output signal                                                                           |
|     |    |    |    |   |   |  |                | TM20_OC01 | TM20 output compare/PWM channel-01                                                                                    |
|     |    |    |    |   |   |  |                | TM36_OC01 | TM36 output compare/PWM channel-01                                                                                    |
|     |    |    |    |   |   |  |                | SPI0_D3   | SPI0 data-3 signal for 4-I/O mode                                                                                     |
|     |    |    |    |   |   |  |                | MAD0      | External memory bus address/data pin 0                                                                                |
|     |    |    |    |   |   |  |                | SDT_P0    | SDT output signal-0                                                                                                   |
|     |    |    |    |   |   |  |                | OBM_P0    | Output signal break control output signal-0                                                                           |
| PB9 | 23 | 19 | 14 | B | A |  | A,I,P,O,U,H,C4 | URT4_TX   | URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.                                      |
|     |    |    |    |   |   |  |                | GPB9      | GPIO/Interrupt/KBI Port-B function pin-9                                                                              |
|     |    |    |    |   |   |  |                | CMP1_P0   | Comparator-1 data output                                                                                              |
|     |    |    |    |   |   |  |                | RTC_TS    | RTC time stamp input signal                                                                                           |
|     |    |    |    |   |   |  |                | URT0_RX   | URT0 receive RX signal, SPI master/slave data                                                                         |

|      |    |    |    |   |   |  |                |           |                                                                                                                       |
|------|----|----|----|---|---|--|----------------|-----------|-----------------------------------------------------------------------------------------------------------------------|
|      |    |    |    |   |   |  |                |           | input signal. URT0_RX and URT0_TX can be swapped by register setting.                                                 |
|      |    |    |    |   |   |  |                | URT2_TMO  | URT2 timeout timer overflow output signal                                                                             |
|      |    |    |    |   |   |  |                | TM20_OC02 | TM20 output compare/PWM channel-02                                                                                    |
|      |    |    |    |   |   |  |                | TM36_OC02 | TM36 output compare/PWM channel-02                                                                                    |
|      |    |    |    |   |   |  |                | SPI0_D2   | SPI0 data-2 signal for 4-I/O mode                                                                                     |
|      |    |    |    |   |   |  |                | MAD1      | External memory bus address/data pin 1                                                                                |
|      |    |    |    |   |   |  |                | MAD8      | External memory bus address/data pin 8                                                                                |
|      |    |    |    |   |   |  |                | OBM_P1    | Output signal break control output signal-1                                                                           |
|      |    |    |    |   |   |  |                | URT4_RX   | URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.                                       |
| PB10 | 24 | 20 | 15 | B | A |  | A,I,P,O,U,H,C2 | GPB10     | GPIO/Interrupt/KBI Port-B function pin-10                                                                             |
|      |    |    |    |   |   |  |                | I2C0_SCL  | I2C0 SCL signal                                                                                                       |
|      |    |    |    |   |   |  |                | URT0_NSS  | URT0 SPI NSS input/output signal                                                                                      |
|      |    |    |    |   |   |  |                | URT2_DE   | URT2 external drive enable output signal                                                                              |
|      |    |    |    |   |   |  |                | TM20_OC11 | TM20 output compare/PWM channel-11                                                                                    |
|      |    |    |    |   |   |  |                | TM36_OC11 | TM36 output compare/PWM channel-11                                                                                    |
|      |    |    |    |   |   |  |                | URT1_TX   | URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting. |
|      |    |    |    |   |   |  |                | MAD2      | External memory bus address/data pin 2                                                                                |
|      |    |    |    |   |   |  |                | MAD1      | External memory bus address/data pin 1                                                                                |
|      |    |    |    |   |   |  |                | SPI0_NSSI | SPI0 slave select input only signal                                                                                   |
| PB11 | 25 | 21 | 16 | B | A |  | A,I,P,O,U,H,C2 | GPB11     | GPIO/Interrupt/KBI Port-B function pin-11                                                                             |
|      |    |    |    |   |   |  |                | I2C0_SDA  | I2C0 SDA signal                                                                                                       |
|      |    |    |    |   |   |  |                | URT0_DE   | URT0 external drive enable output signal                                                                              |
|      |    |    |    |   |   |  |                | IR_OUT    | IR output signal                                                                                                      |
|      |    |    |    |   |   |  |                | TM20_OC12 | TM20 output compare/PWM channel-12                                                                                    |
|      |    |    |    |   |   |  |                | TM36_OC12 | TM36 output compare/PWM channel-12                                                                                    |
|      |    |    |    |   |   |  |                | URT1_RX   | URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.   |
|      |    |    |    |   |   |  |                | MAD3      | External memory bus address/data pin 3                                                                                |
|      |    |    |    |   |   |  |                | MAD9      | External memory bus address/data pin 9                                                                                |
|      |    |    |    |   |   |  |                | DMA_TRG0  | DMA external trigger pin-0 input                                                                                      |
|      |    |    |    |   |   |  |                | URT0_CLK  | URT0 clock signal                                                                                                     |
| PB12 | 26 | 22 |    | B | A |  | A,I,P,O,U,H,C2 | GPB12     | GPIO/Interrupt/KBI Port-B function pin-12                                                                             |
|      |    |    |    |   |   |  |                | DMA_TRG0  | DMA external trigger pin-0 input                                                                                      |
|      |    |    |    |   |   |  |                | NCO_P0    | NCO clock output signal-0                                                                                             |
|      |    |    |    |   |   |  |                |           |                                                                                                                       |
|      |    |    |    |   |   |  |                | URT1_CLK  | URT1 clock signal                                                                                                     |
|      |    |    |    |   |   |  |                | MAD4      | External memory bus address/data pin 4                                                                                |
|      |    |    |    |   |   |  |                | MAD2      | External memory bus address/data pin 2                                                                                |
|      |    |    |    |   |   |  |                | URT5_TX   | URT5 transmit TX signal. URT5_RX and URT5_TX can be swapped by register setting.                                      |
| PB13 | 28 | 23 | 17 | B | A |  | A,I,P,O,U,H,C2 | GPB13     | GPIO/Interrupt/KBI Port-B function pin-13                                                                             |
|      |    |    |    |   |   |  |                | DAC_TRG0  | DAC trigger start input                                                                                               |
|      |    |    |    |   |   |  |                | TM00_ETR  | TM00 external trigger/clock input signal                                                                              |

|      |    |    |    |   |   |  |                      |           |                                                                                                                       |
|------|----|----|----|---|---|--|----------------------|-----------|-----------------------------------------------------------------------------------------------------------------------|
|      |    |    |    |   |   |  |                      | URT0_CTS  | URT0 CTS input control signal                                                                                         |
|      |    |    |    |   |   |  |                      | TM20_ETR  | TM20 external trigger/clock input signal                                                                              |
|      |    |    |    |   |   |  |                      | TM36_ETR  | TM36 external trigger/clock input signal                                                                              |
|      |    |    |    |   |   |  |                      | URT0_CLK  | URT0 clock signal                                                                                                     |
|      |    |    |    |   |   |  |                      | MAD5      | External memory bus address/data pin 5                                                                                |
|      |    |    |    |   |   |  |                      | MAD10     | External memory bus address/data pin 10                                                                               |
|      |    |    |    |   |   |  |                      | CCL_P0    | CCL output signal-0                                                                                                   |
|      |    |    |    |   |   |  |                      | URT4_RX   | URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.                                       |
| PB14 | 29 | 24 | 18 | B | A |  | A,I,P,O,U,H,C2       | GPB14     | GPIO/Interrupt/KBI Port-B function pin-14                                                                             |
|      |    |    |    |   |   |  |                      | DMA_TRG0  | DMA external trigger pin-0 input                                                                                      |
|      |    |    |    |   |   |  |                      | TM00_TRGO | TM00 trigger output signal                                                                                            |
|      |    |    |    |   |   |  |                      | URT0_RTS  | URT0 RTS output control signal                                                                                        |
|      |    |    |    |   |   |  |                      | TM20_TRGO | TM20 trigger output signal                                                                                            |
|      |    |    |    |   |   |  |                      | TM36_BK0  | TM36 break input signal                                                                                               |
|      |    |    |    |   |   |  |                      | URT0_NSS  | URT0 SPI NSS input/output signal                                                                                      |
|      |    |    |    |   |   |  |                      | MAD6      | External memory bus address/data pin 6                                                                                |
|      |    |    |    |   |   |  |                      | MAD3      | External memory bus address/data pin 3                                                                                |
|      |    |    |    |   |   |  |                      | CCL_P1    | CCL output signal-1                                                                                                   |
|      |    |    |    |   |   |  |                      | URT4_TX   | URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.                                      |
|      |    |    |    |   |   |  |                      |           |                                                                                                                       |
| PB15 | 31 | 25 |    | B | A |  | A,I,P,O,U,H,C2       | GPB15     | GPIO/Interrupt/KBI Port-B function pin-15                                                                             |
|      |    |    |    |   |   |  |                      | IR_OUT    | IR output signal                                                                                                      |
|      |    |    |    |   |   |  |                      | NCO_CK0   | NCO external clock input signal-0                                                                                     |
|      |    |    |    |   |   |  |                      |           |                                                                                                                       |
|      |    |    |    |   |   |  |                      | URT1_NSS  | URT1 SPI NSS input/output signal                                                                                      |
|      |    |    |    |   |   |  |                      | MAD7      | External memory bus address/data pin 7                                                                                |
|      |    |    |    |   |   |  |                      | MAD11     | External memory bus address/data pin 11                                                                               |
|      |    |    |    |   |   |  |                      | URT5_RX   | URT5 receive RX signal. URT5_RX and URT5_TX can be swapped by register setting.                                       |
| PC0  | 34 | 26 | 19 | B | A |  | A,I,P,O,Q,U,H,C<br>2 | GPC0      | GPIO/Interrupt/KBI Port-C function pin-0                                                                              |
|      |    |    |    |   |   |  |                      | ICKO      | Internal clock source clock output                                                                                    |
|      |    |    |    |   |   |  |                      | TM00_CKO  | TM00 timer overflow output signal                                                                                     |
|      |    |    |    |   |   |  |                      | URT0_CLK  | URT0 clock signal                                                                                                     |
|      |    |    |    |   |   |  |                      | URT2_CLK  | URT2 clock signal                                                                                                     |
|      |    |    |    |   |   |  |                      | TM20_OC00 | TM20 output compare/PWM channel-00                                                                                    |
|      |    |    |    |   |   |  |                      | TM36_OC00 | TM36 output compare/PWM channel-00                                                                                    |
|      |    |    |    |   |   |  |                      | I2C0_SCL  | I2C0 SCL signal                                                                                                       |
|      |    |    |    |   |   |  |                      | MCLK      | External memory bus clock pin                                                                                         |
|      |    |    |    |   |   |  |                      | MWE       | External memory bus write enable(WE) or write strobe(WR) signal pin                                                   |
|      |    |    |    |   |   |  |                      | URT0_TX   | URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting. |
|      |    |    |    |   |   |  |                      | URT5_TX   | URT5 transmit TX signal. URT5_RX and URT5_TX can be swapped by register setting.                                      |
| PC1  | 35 | 27 | 20 | B | A |  | A,I,P,O,Q,U,H,C<br>2 | GPC1      | GPIO/Interrupt/KBI Port-C function pin-1                                                                              |
|      |    |    |    |   |   |  |                      | ADC0_TRG  | ADC trigger start input                                                                                               |

|     |    |    |    |   |   |   |                      |           |                                                                                                                     |
|-----|----|----|----|---|---|---|----------------------|-----------|---------------------------------------------------------------------------------------------------------------------|
|     |    |    |    |   |   |   |                      | TM01_CKO  | TM01 timer overflow output signal                                                                                   |
|     |    |    |    |   |   |   |                      | TM36_IC0  | TM36 input capture channel-0                                                                                        |
|     |    |    |    |   |   |   |                      | URT1_CLK  | URT1 clock signal                                                                                                   |
|     |    |    |    |   |   |   |                      | TM20_OC0N | TM20 output compare/PWM complement channel-0                                                                        |
|     |    |    |    |   |   |   |                      | TM36_OC0N | TM36 output compare/PWM complement channel-0                                                                        |
|     |    |    |    |   |   |   |                      | I2C0_SDA  | I2C0 SDA signal                                                                                                     |
|     |    |    |    |   |   |   |                      | MAD8      | External memory bus address/data pin 8                                                                              |
|     |    |    |    |   |   |   |                      | MAD4      | External memory bus address/data pin 4                                                                              |
|     |    |    |    |   |   |   |                      | URT0_RX   | URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting. |
|     |    |    |    |   |   |   |                      | URT5_RX   | URT5 receive RX signal. URT5_RX and URT5_TX can be swapped by register setting.                                     |
| PC2 | 36 | 28 | 21 | B | A |   | A,I,P,O,Q,U,H,C<br>2 | GPC2      | GPIO/Interrupt/KBI Port-C function pin-2                                                                            |
|     |    |    |    |   |   |   |                      | ADC0_OUT  | ADC threshold window compare output                                                                                 |
|     |    |    |    |   |   |   |                      | TM10_CKO  | TM10 timer overflow output signal                                                                                   |
|     |    |    |    |   |   |   |                      | OBM_P0    | Output signal break control output signal-0                                                                         |
|     |    |    |    |   |   |   |                      | URT2_CLK  | URT2 clock signal                                                                                                   |
|     |    |    |    |   |   |   |                      | TM20_OC10 | TM20 output compare/PWM channel-10                                                                                  |
|     |    |    |    |   |   |   |                      | TM36_OC10 | TM36 output compare/PWM channel-10                                                                                  |
|     |    |    |    |   |   |   |                      | SDT_I0    | State detect input signal-0                                                                                         |
|     |    |    |    |   |   |   |                      | MAD9      | External memory bus address/data pin 9                                                                              |
|     |    |    |    |   |   |   |                      | MAD12     | External memory bus address/data pin 12                                                                             |
| PC3 | 37 | 29 | 22 | B | A |   | A,I,P,O,Q,U,H,C<br>2 | GPC3      | GPIO/Interrupt/KBI Port-C function pin-3                                                                            |
|     |    |    |    |   |   |   |                      | OBM_P1    | Output signal break control output signal-1                                                                         |
|     |    |    |    |   |   |   |                      | TM16_CKO  | TM16 timer overflow output signal                                                                                   |
|     |    |    |    |   |   |   |                      | URT0_CLK  | URT0 clock signal                                                                                                   |
|     |    |    |    |   |   |   |                      | URT1_CLK  | URT1 clock signal                                                                                                   |
|     |    |    |    |   |   |   |                      | TM20_OC1N | TM20 output compare/PWM complement channel-1                                                                        |
|     |    |    |    |   |   |   |                      | TM36_OC1N | TM36 output compare/PWM complement channel-1                                                                        |
|     |    |    |    |   |   |   |                      | SDT_I1    | State detect input signal-1                                                                                         |
|     |    |    |    |   |   |   |                      | MAD10     | External memory bus address/data pin 10                                                                             |
|     |    |    |    |   |   |   |                      | MAD5      | External memory bus address/data pin 5                                                                              |
| PC4 | 38 | 30 | 23 | B | Q | H | A,I,P,O,Q,U,H,C<br>2 | GPC4      | GPIO/Interrupt/KBI Port-C function pin-4                                                                            |
|     |    |    |    |   |   |   |                      | SWCLK     | Serial wire debug clock signal                                                                                      |
|     |    |    |    |   |   |   |                      | I2C0_SCL  | I2C0 SCL signal                                                                                                     |
|     |    |    |    |   |   |   |                      | URT0_RX   | URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting. |
|     |    |    |    |   |   |   |                      | URT1_RX   | URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting. |
|     |    |    |    |   |   |   |                      | TM36_OC2  | TM36 output compare/PWM channel-2                                                                                   |
|     |    |    |    |   |   |   |                      | SDT_I0    | State detect input signal-0                                                                                         |

|     |    |    |    |   |   |   |                      |           |                                                                                                                       |
|-----|----|----|----|---|---|---|----------------------|-----------|-----------------------------------------------------------------------------------------------------------------------|
|     |    |    |    |   |   |   |                      | URT6_RX   | URT6 receive RX signal. URT6_RX and URT6_TX can be swapped by register setting.                                       |
| PC5 | 39 | 31 | 24 | B | Q | H | A,I,P,O,Q,U,H,C<br>2 | GPC5      | GPIO/Interrupt/KBI Port-C function pin-5                                                                              |
|     |    |    |    |   |   |   |                      | SWDIO     | Serial wire debug data signal                                                                                         |
|     |    |    |    |   |   |   |                      | I2C0_SDA  | I2C0 SDA signal                                                                                                       |
|     |    |    |    |   |   |   |                      | URT0_TX   | URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting. |
|     |    |    |    |   |   |   |                      | URT1_TX   | URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting. |
|     |    |    |    |   |   |   |                      | TM36_OC3  | TM36 output compare/PWM channel-3                                                                                     |
|     |    |    |    |   |   |   |                      | SDT_I1    | State detect input signal-1                                                                                           |
|     |    |    |    |   |   |   |                      | URT6_TX   | URT6 transmit TX signal. URT6_RX and URT6_TX can be swapped by register setting.                                      |
| PC6 | 40 | 32 | 25 | B | Q | H | A,I,P,O,Q,U,H,C<br>F | GPC6      | GPIO/Interrupt/KBI Port-C function pin-6                                                                              |
|     |    |    |    |   |   |   |                      | RSTN      | External hardware reset input                                                                                         |
|     |    |    |    |   |   |   |                      | RTC_TS    | RTC time stamp input signal                                                                                           |
|     |    |    |    |   |   |   |                      | URT0_NSS  | URT0 SPI NSS input/output signal                                                                                      |
|     |    |    |    |   |   |   |                      | URT1_NSS  | URT1 SPI NSS input/output signal                                                                                      |
|     |    |    |    |   |   |   |                      | TM20_ETR  | TM20 external trigger/clock input signal                                                                              |
|     |    |    |    |   |   |   |                      | TM26_ETR  | TM26 external trigger/clock input signal                                                                              |
|     |    |    |    |   |   |   |                      | MBW1      | External memory bus byte write enable 1 pin                                                                           |
| PC7 | 41 | 33 |    | B | A |   | A,I,P,O,Q,U,H,C<br>2 | MALE      | External memory bus address latch enable(ALE) or data/command select(DC) pin                                          |
|     |    |    |    |   |   |   |                      | GPC7      | GPIO/Interrupt/KBI Port-C function pin-7                                                                              |
|     |    |    |    |   |   |   |                      | ADC0_TRG  | ADC trigger start input                                                                                               |
|     |    |    |    |   |   |   |                      | RTC_OUT   | RTC selection output signal                                                                                           |
|     |    |    |    |   |   |   |                      | URT0_DE   | URT0 external drive enable output signal                                                                              |
|     |    |    |    |   |   |   |                      | URT1_NSS  | URT1 SPI NSS input/output signal                                                                                      |
|     |    |    |    |   |   |   |                      | TM36_TRGO | TM36 trigger output signal                                                                                            |
|     |    |    |    |   |   |   |                      | MBW0      | External memory bus byte write enable 0 pin                                                                           |
| PC8 | 42 | 34 | 26 | B | A |   | A,I,P,O,Q,U,H,C<br>2 | MCE       | External memory bus chip enable/select pin                                                                            |
|     |    |    |    |   |   |   |                      | GPC8      | GPIO/Interrupt/KBI Port-C function pin-8                                                                              |
|     |    |    |    |   |   |   |                      | ADC0_OUT  | ADC threshold window compare output                                                                                   |
|     |    |    |    |   |   |   |                      | I2C0_SCL  | I2C0 SCL signal                                                                                                       |
|     |    |    |    |   |   |   |                      | URT0_BRO  | URT0 baud-rate timer overflow output signal                                                                           |
|     |    |    |    |   |   |   |                      | URT1_TX   | URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting. |
|     |    |    |    |   |   |   |                      | TM20_OC0H | TM20 output compare/PWM high channel-0                                                                                |
|     |    |    |    |   |   |   |                      | TM36_OC0H | TM36 output compare/PWM high channel-0                                                                                |
|     |    |    |    |   |   |   |                      | TM36_OC0N | TM36 output compare/PWM complement channel-0                                                                          |
|     |    |    |    |   |   |   |                      | MAD11     | External memory bus address/data pin 11                                                                               |
|     |    |    |    |   |   |   |                      | MAD13     | External memory bus address/data pin 13                                                                               |
|     |    |    |    |   |   |   |                      | CCL_P0    | CCL output signal-0                                                                                                   |
|     |    |    |    |   |   |   |                      | URT6_TX   | URT6 transmit TX signal. URT6_RX and                                                                                  |

|      |    |    |    |   |   |                      |           |                                                                                                                       |
|------|----|----|----|---|---|----------------------|-----------|-----------------------------------------------------------------------------------------------------------------------|
| PC9  | 43 | 35 | 27 | B | A | A,I,P,O,Q,U,H,C<br>2 |           | URT6_TX can be swapped by register setting.                                                                           |
|      |    |    |    |   |   |                      | GPC9      | GPIO/Interrupt/KBI Port-C function pin-9                                                                              |
|      |    |    |    |   |   |                      | CMP0_P0   | Comparator-0 data output                                                                                              |
|      |    |    |    |   |   |                      | I2C0_SDA  | I2C0 SDA signal                                                                                                       |
|      |    |    |    |   |   |                      | URT0_TMO  | URT0 timeout timer overflow output signal                                                                             |
|      |    |    |    |   |   |                      | URT1_RX   | URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.   |
|      |    |    |    |   |   |                      | TM20_OC1H | TM20 output compare/PWM high channel-1                                                                                |
|      |    |    |    |   |   |                      | TM36_OC1H | TM36 output compare/PWM high channel-1                                                                                |
|      |    |    |    |   |   |                      | TM36_OC1N | TM36 output compare/PWM complement channel-1                                                                          |
|      |    |    |    |   |   |                      | MAD12     | External memory bus address/data pin 12                                                                               |
|      |    |    |    |   |   |                      | MAD6      | External memory bus address/data pin 6                                                                                |
|      |    |    |    |   |   |                      | CCL_P1    | CCL output signal-1                                                                                                   |
| PC10 | 44 | 36 | 28 | B | A | A,I,P,O,Q,U,H,C<br>2 | URT6_RX   | URT6 receive RX signal. URT6_RX and URT6_TX can be swapped by register setting.                                       |
|      |    |    |    |   |   |                      | GPC10     | GPIO/Interrupt/KBI Port-C function pin-10                                                                             |
|      |    |    |    |   |   |                      | CMP1_P0   | Comparator-1 data output                                                                                              |
|      |    |    |    |   |   |                      | I2C1_SCL  | I2C1 SCL signal                                                                                                       |
|      |    |    |    |   |   |                      | URT0_TX   | URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting. |
|      |    |    |    |   |   |                      | URT2_TX   | URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting. |
|      |    |    |    |   |   |                      | URT1_TX   | URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting. |
|      |    |    |    |   |   |                      | TM36_OC2H | TM36 output compare/PWM high channel-2                                                                                |
|      |    |    |    |   |   |                      | TM36_OC2N | TM36 output compare/PWM complement channel-2                                                                          |
|      |    |    |    |   |   |                      | MAD13     | External memory bus address/data pin 13                                                                               |
| PC11 | 45 | 37 | 29 | B | A | A,I,P,O,Q,U,H,C<br>2 | MAD14     | External memory bus address/data pin 14                                                                               |
|      |    |    |    |   |   |                      | URT7_TX   | URT7 transmit TX signal. URT7_RX and URT7_TX can be swapped by register setting.                                      |
|      |    |    |    |   |   |                      | GPC11     | GPIO/Interrupt/KBI Port-C function pin-11                                                                             |
|      |    |    |    |   |   |                      | I2C1_SDA  | I2C1 SDA signal                                                                                                       |
|      |    |    |    |   |   |                      | URT0_RX   | URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting.   |
|      |    |    |    |   |   |                      | URT2_RX   | URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.   |
|      |    |    |    |   |   |                      | URT1_RX   | URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.   |
|      |    |    |    |   |   |                      | TM36_OC3H | TM36 output compare/PWM high channel-3                                                                                |

|      |    |    |    |   |   |  |                      |           |                                                                                                                       |
|------|----|----|----|---|---|--|----------------------|-----------|-----------------------------------------------------------------------------------------------------------------------|
|      |    |    |    |   |   |  |                      | TM26_OC01 | TM26 output compare/PWM channel-01                                                                                    |
|      |    |    |    |   |   |  |                      | MAD14     | External memory bus address/data pin 14                                                                               |
|      |    |    |    |   |   |  |                      | MAD7      | External memory bus address/data pin 7                                                                                |
|      |    |    |    |   |   |  |                      | URT7_RX   | URT7 receive RX signal. URT7_RX and URT7_TX can be swapped by register setting.                                       |
| PC12 | 46 | 38 | 30 | B | A |  | A,I,P,O,Q,U,H,C<br>2 | GPC12     | GPIO/Interrupt/KBI Port-C function pin-12                                                                             |
|      |    |    |    |   |   |  |                      | IR_OUT    | IR output signal                                                                                                      |
|      |    |    |    |   |   |  |                      | DAC_TRG0  | DAC trigger start input                                                                                               |
|      |    |    |    |   |   |  |                      | URT1_DE   | URT1 external drive enable output signal                                                                              |
|      |    |    |    |   |   |  |                      | TM10_TRG0 | TM10 trigger output signal                                                                                            |
|      |    |    |    |   |   |  |                      | TM36_OC3  | TM36 output compare/PWM channel-3                                                                                     |
|      |    |    |    |   |   |  |                      | TM26_OC02 | TM26 output compare/PWM channel-02                                                                                    |
|      |    |    |    |   |   |  |                      | MAD15     | External memory bus address/data pin 15                                                                               |
|      |    |    |    |   |   |  |                      | SDT_P0    | SDT output signal-0                                                                                                   |
|      |    |    |    |   |   |  |                      | URT1_CLK  | URT1 clock signal                                                                                                     |
|      |    |    |    |   |   |  |                      | MAM1      | The least significant bit of the EMB address                                                                          |
| PC13 | 47 | 39 | 31 | B | A |  | A,I,P,O,Q,U,CF       | GPC13     | GPIO/Interrupt/KBI Port-C function pin-13                                                                             |
|      |    |    |    |   |   |  |                      | XIN       | External Xtal/OSC input                                                                                               |
|      |    |    |    |   |   |  |                      | URT1_NSS  | URT1 SPI NSS input/output signal                                                                                      |
|      |    |    |    |   |   |  |                      | URT0_CTS  | URT0 CTS input control signal                                                                                         |
|      |    |    |    |   |   |  |                      | URT2_RX   | URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.   |
|      |    |    |    |   |   |  |                      | TM10_ETR  | TM10 external trigger/clock input signal                                                                              |
|      |    |    |    |   |   |  |                      | TM26_ETR  | TM26 external trigger/clock input signal                                                                              |
|      |    |    |    |   |   |  |                      | TM36_OC00 | TM36 output compare/PWM channel-00                                                                                    |
|      |    |    |    |   |   |  |                      | TM20_IC0  | TM20 input capture channel-0                                                                                          |
|      |    |    |    |   |   |  |                      | SDT_I0    | State detect input signal-0                                                                                           |
|      |    |    |    |   |   |  |                      | URT6_RX   | URT6 receive RX signal. URT6_RX and URT6_TX can be swapped by register setting.                                       |
| PC14 | 48 | 40 | 32 | B | A |  | A,I,P,O,Q,U,H,C<br>F | GPC14     | GPIO/Interrupt/KBI Port-C function pin-14                                                                             |
|      |    |    |    |   |   |  |                      | XOUT      | External Xtal output                                                                                                  |
|      |    |    |    |   |   |  |                      | URT1_TMO  | URT1 timeout timer overflow output signal                                                                             |
|      |    |    |    |   |   |  |                      | URT0_RTS  | URT0 RTS output control signal                                                                                        |
|      |    |    |    |   |   |  |                      | URT2_TX   | URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting. |
|      |    |    |    |   |   |  |                      | TM10_CKO  | TM10 timer overflow output signal                                                                                     |
|      |    |    |    |   |   |  |                      | TM26_TRG0 | TM26 trigger output signal                                                                                            |
|      |    |    |    |   |   |  |                      | TM36_OC10 | TM36 output compare/PWM channel-10                                                                                    |
|      |    |    |    |   |   |  |                      | TM20_IC1  | TM20 input capture channel-1                                                                                          |
|      |    |    |    |   |   |  |                      | SDT_I1    | State detect input signal-1                                                                                           |
|      |    |    |    |   |   |  |                      | URT6_TX   | URT6 transmit TX signal. URT6_RX and URT6_TX can be swapped by register setting.                                      |
| PD0  | 54 | 42 | 33 | B | A |  | A,I,P,O,U,H,C4       | GPD0      | GPIO/Interrupt/KBI Port-D function pin-0                                                                              |
|      |    |    |    |   |   |  |                      | OBM_I0    | Output signal break control input signal-0                                                                            |
|      |    |    |    |   |   |  |                      | TM10_CKO  | TM10 timer overflow output signal                                                                                     |
|      |    |    |    |   |   |  |                      | URT0_CLK  | URT0 clock signal                                                                                                     |

|     |    |    |    |   |   |  |                |           |                                                                                                                                      |
|-----|----|----|----|---|---|--|----------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------|
|     |    |    |    |   |   |  |                | TM26_OC1N | TM26 output compare/PWM complement channel-1                                                                                         |
|     |    |    |    |   |   |  |                | TM20_CKO  | TM20 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | TM36_OC2  | TM36 output compare/PWM channel-2                                                                                                    |
|     |    |    |    |   |   |  |                | SPI0_NSS  | SPI0 slave select input/output signal                                                                                                |
|     |    |    |    |   |   |  |                | MA0       | External memory bus address pin 0                                                                                                    |
|     |    |    |    |   |   |  |                | MCLK      | External memory bus clock pin                                                                                                        |
|     |    |    |    |   |   |  |                | URT2_NSS  | URT2 SPI NSS input/output signal                                                                                                     |
| PD1 | 55 | 43 | 34 | B | A |  | A,I,P,O,U,H,C4 | GPD1      | GPIO/Interrupt/KBI Port-D function pin-1                                                                                             |
|     |    |    |    |   |   |  |                | OBM_I1    | Output signal break control input signal-1                                                                                           |
|     |    |    |    |   |   |  |                | TM16_CKO  | TM16 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | URT0_CLK  | URT0 clock signal                                                                                                                    |
|     |    |    |    |   |   |  |                | NCO_CK0   | NCO external clock input signal-0                                                                                                    |
|     |    |    |    |   |   |  |                | TM26_CKO  | TM26 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | TM36_OC2N | TM36 output compare/PWM complement channel-2                                                                                         |
|     |    |    |    |   |   |  |                | SPI0_CLK  | SPI0 clock signal                                                                                                                    |
|     |    |    |    |   |   |  |                | MA1       | External memory bus address pin 1                                                                                                    |
|     |    |    |    |   |   |  |                | URT2_CLK  | URT2 clock signal                                                                                                                    |
| PD2 | 56 | 44 | 35 | B | A |  | A,I,P,O,U,H,C4 | GPD2      | GPIO/Interrupt/KBI Port-D function pin-2                                                                                             |
|     |    |    |    |   |   |  |                |           |                                                                                                                                      |
|     |    |    |    |   |   |  |                | TM00_CKO  | TM00 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | URT1_CLK  | URT1 clock signal                                                                                                                    |
|     |    |    |    |   |   |  |                | TM26_OC00 | TM26 output compare/PWM channel-00                                                                                                   |
|     |    |    |    |   |   |  |                | TM20_CKO  | TM20 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | TM36_CKO  | TM36 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | SPI0_MOSI | SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting. |
|     |    |    |    |   |   |  |                | MA2       | External memory bus address pin 2                                                                                                    |
|     |    |    |    |   |   |  |                | MAD4      | External memory bus address/data pin 4                                                                                               |
| PD3 | 57 | 45 | 36 | B | A |  | A,I,P,O,U,H,C4 | URT2_TX   | URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting.                |
|     |    |    |    |   |   |  |                | GPD3      | GPIO/Interrupt/KBI Port-D function pin-3                                                                                             |
|     |    |    |    |   |   |  |                |           |                                                                                                                                      |
|     |    |    |    |   |   |  |                | TM01_CKO  | TM01 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | URT1_CLK  | URT1 clock signal                                                                                                                    |
|     |    |    |    |   |   |  |                | SPI0_MISO | SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting. |
|     |    |    |    |   |   |  |                | TM26_CKO  | TM26 timer overflow output signal                                                                                                    |
|     |    |    |    |   |   |  |                | SPI0_D3   | SPI0 data-3 signal for 4-I/O mode                                                                                                    |
|     |    |    |    |   |   |  |                | MA3       | External memory bus address pin 3                                                                                                    |
|     |    |    |    |   |   |  |                | MAD7      | External memory bus address/data pin 7                                                                                               |
|     |    |    |    |   |   |  |                | TM36_TRGO | TM36 trigger output signal                                                                                                           |
|     |    |    |    |   |   |  |                | URT2_RX   | URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be                                               |

|          |                                  |    |    |   |   |  |                |           |                                                                                                                                      |
|----------|----------------------------------|----|----|---|---|--|----------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------|
|          |                                  |    |    |   |   |  |                |           | swapped by register setting.                                                                                                         |
| PD4      | 58                               | 46 |    | B | A |  | A,I,P,O,U,H,C4 | GPD4      | GPIO/Interrupt/KBI Port-D function pin-4                                                                                             |
|          |                                  |    |    |   |   |  |                | TM00_TRGO | TM00 trigger output signal                                                                                                           |
|          |                                  |    |    |   |   |  |                | TM01_TRGO | TM01 trigger output signal                                                                                                           |
|          |                                  |    |    |   |   |  |                | URT1_TX   | URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting.                |
|          |                                  |    |    |   |   |  |                | TM26_OC00 | TM26 output compare/PWM channel-00                                                                                                   |
|          |                                  |    |    |   |   |  |                | SPI0_D2   | SPI0 data-2 signal for 4-I/O mode                                                                                                    |
|          |                                  |    |    |   |   |  |                | MA4       | External memory bus address pin 4                                                                                                    |
|          |                                  |    |    |   |   |  |                | MAD6      | External memory bus address/data pin 6                                                                                               |
|          |                                  |    |    |   |   |  |                | URT2_TX   | URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting.                |
|          |                                  |    |    |   |   |  |                |           |                                                                                                                                      |
| PD5      | 59                               | 47 |    | B | A |  | A,I,P,O,U,H,C4 | GPD5      | GPIO/Interrupt/KBI Port-D function pin-5                                                                                             |
|          |                                  |    |    |   |   |  |                | TM00_ETR  | TM00 external trigger/clock input signal                                                                                             |
|          |                                  |    |    |   |   |  |                | I2C0_SCL  | I2C0 SCL signal                                                                                                                      |
|          |                                  |    |    |   |   |  |                | URT1_RX   | URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.                  |
|          |                                  |    |    |   |   |  |                | TM26_OC01 | TM26 output compare/PWM channel-01                                                                                                   |
|          |                                  |    |    |   |   |  |                | SPI0_MISO | SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting. |
|          |                                  |    |    |   |   |  |                | MA5       | External memory bus address pin 5                                                                                                    |
|          |                                  |    |    |   |   |  |                | MAD5      | External memory bus address/data pin 5                                                                                               |
|          |                                  |    |    |   |   |  |                | URT2_RX   | URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.                  |
|          |                                  |    |    |   |   |  |                |           |                                                                                                                                      |
| PD6      | 60                               | 48 |    | B | A |  | A,I,P,O,U,H,C2 | GPD6      | GPIO/Interrupt/KBI Port-D function pin-6                                                                                             |
|          |                                  |    |    |   |   |  |                | CPU_NMI   | CPU NMI external pin input                                                                                                           |
|          |                                  |    |    |   |   |  |                | I2C0_SDA  | I2C0 SDA signal                                                                                                                      |
|          |                                  |    |    |   |   |  |                | URT1_NSS  | URT1 SPI NSS input/output signal                                                                                                     |
|          |                                  |    |    |   |   |  |                | SPI0_NSSI | SPI0 slave select input only signal                                                                                                  |
|          |                                  |    |    |   |   |  |                | TM26_OC02 | TM26 output compare/PWM channel-02                                                                                                   |
|          |                                  |    |    |   |   |  |                | SPI0_NSS  | SPI0 slave select input/output signal                                                                                                |
|          |                                  |    |    |   |   |  |                | MA6       | External memory bus address pin 6                                                                                                    |
|          |                                  |    |    |   |   |  |                | SDT_P0    | SDT output signal-0                                                                                                                  |
| URT2_NSS | URT2 SPI NSS input/output signal |    |    |   |   |  |                |           |                                                                                                                                      |
|          |                                  |    |    |   |   |  |                |           |                                                                                                                                      |
| PD7      | 61                               | 49 | 37 | B | A |  | A,I,P,O,U,H,C4 | GPD7      | GPIO/Interrupt/KBI Port-D function pin-7                                                                                             |
|          |                                  |    |    |   |   |  |                | TM00_CKO  | TM00 timer overflow output signal                                                                                                    |
|          |                                  |    |    |   |   |  |                | TM01_ETR  | TM01 external trigger/clock input signal                                                                                             |
|          |                                  |    |    |   |   |  |                | URT1_DE   | URT1 external drive enable output signal                                                                                             |
|          |                                  |    |    |   |   |  |                | SPI0_MISO | SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and                                               |

|      |    |    |    |   |   |  |                |           |                                                                                                                                      |
|------|----|----|----|---|---|--|----------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------|
|      |    |    |    |   |   |  |                |           | SPI0_MISO can be swapped by register setting.                                                                                        |
|      |    |    |    |   |   |  |                | TM26_OC0N | TM26 output compare/PWM complement channel-0                                                                                         |
|      |    |    |    |   |   |  |                | SPI0_D4   | SPI0 data-0 signal for 2nd SPI device 4-I/O mode                                                                                     |
|      |    |    |    |   |   |  |                | MA7       | External memory bus address pin 7                                                                                                    |
|      |    |    |    |   |   |  |                | MAD0      | External memory bus address/data pin 0                                                                                               |
|      |    |    |    |   |   |  |                | TM36_IC0  | TM36 input capture channel-0                                                                                                         |
| PD8  | 62 | 50 | 38 | B | A |  | A,I,P,O,U,H,C4 | GPD8      | GPIO/Interrupt/KBI Port-D function pin-8                                                                                             |
|      |    |    |    |   |   |  |                | CPU_TXEV  | CPU wakeup event output                                                                                                              |
|      |    |    |    |   |   |  |                | TM01_TRGO | TM01 trigger output signal                                                                                                           |
|      |    |    |    |   |   |  |                | URT1_RTS  | URT1 RTS output control signal                                                                                                       |
|      |    |    |    |   |   |  |                | SPI0_D2   | SPI0 data-2 signal for 4-I/O mode                                                                                                    |
|      |    |    |    |   |   |  |                | TM26_OC10 | TM26 output compare/PWM channel-10                                                                                                   |
|      |    |    |    |   |   |  |                | SPI0_D7   | SPI0 data-3 signal for 2nd SPI device 4-I/O mode                                                                                     |
|      |    |    |    |   |   |  |                | MA8       | External memory bus address pin 8                                                                                                    |
|      |    |    |    |   |   |  |                | MAD3      | External memory bus address/data pin 3                                                                                               |
|      |    |    |    |   |   |  |                | TM36_IC1  | TM36 input capture channel-1                                                                                                         |
|      |    |    |    |   |   |  |                | SPI0_CLK  | SPI0 clock signal                                                                                                                    |
|      |    |    |    |   |   |  |                |           |                                                                                                                                      |
| PD9  | 63 | 51 | 39 | B | A |  | A,I,P,O,U,H,C2 | GPD9      | GPIO/Interrupt/KBI Port-D function pin-9                                                                                             |
|      |    |    |    |   |   |  |                | CPU_RXEV  | CPU wakeup event input                                                                                                               |
|      |    |    |    |   |   |  |                | TM00_TRGO | TM00 trigger output signal                                                                                                           |
|      |    |    |    |   |   |  |                | URT1_CTS  | URT1 CTS input control signal                                                                                                        |
|      |    |    |    |   |   |  |                | SPI0_NSSI | SPI0 slave select input only signal                                                                                                  |
|      |    |    |    |   |   |  |                | TM26_OC11 | TM26 output compare/PWM channel-11                                                                                                   |
|      |    |    |    |   |   |  |                | SPI0_D6   | SPI0 data-2 signal for 2nd SPI device 4-I/O mode                                                                                     |
|      |    |    |    |   |   |  |                | MA9       | External memory bus address pin 9                                                                                                    |
|      |    |    |    |   |   |  |                | MAD2      | External memory bus address/data pin 2                                                                                               |
|      |    |    |    |   |   |  |                | TM36_IC2  | TM36 input capture channel-2                                                                                                         |
| PD10 | 64 | 52 | 40 | B | A |  | A,I,P,O,U,H,C2 | SPI0_NSS  | SPI0 slave select input/output signal                                                                                                |
|      |    |    |    |   |   |  |                | GPD10     | GPIO/Interrupt/KBI Port-D function pin-10                                                                                            |
|      |    |    |    |   |   |  |                | CPU_NMI   | CPU NMI external pin input                                                                                                           |
|      |    |    |    |   |   |  |                | TM00_ETR  | TM00 external trigger/clock input signal                                                                                             |
|      |    |    |    |   |   |  |                | URT1_BRO  | URT1 baud-rate timer overflow output signal                                                                                          |
|      |    |    |    |   |   |  |                | RTC_OUT   | RTC selection output signal                                                                                                          |
|      |    |    |    |   |   |  |                | TM26_OC12 | TM26 output compare/PWM channel-12                                                                                                   |
|      |    |    |    |   |   |  |                | SPI0_D5   | SPI0 data-1 signal for 2nd SPI device 4-I/O mode                                                                                     |
|      |    |    |    |   |   |  |                | MA10      | External memory bus address pin 10                                                                                                   |
|      |    |    |    |   |   |  |                | MAD1      | External memory bus address/data pin 1                                                                                               |
| PD11 | 65 | 53 |    | B | A |  | A,I,P,O,U,H,C2 | TM36_IC3  | TM36 input capture channel-3                                                                                                         |
|      |    |    |    |   |   |  |                | SPI0_MOSI | SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting. |
|      |    |    |    |   |   |  |                | GPD11     | GPIO/Interrupt/KBI Port-D function pin-11                                                                                            |
|      |    |    |    |   |   |  |                | CPU_NMI   | CPU NMI external pin input                                                                                                           |

|      |    |  |  |   |   |                |           |                                                                                     |
|------|----|--|--|---|---|----------------|-----------|-------------------------------------------------------------------------------------|
|      |    |  |  |   |   |                | DMA_TRG1  | DMA external trigger pin-1 input                                                    |
|      |    |  |  |   |   |                | URT1_TMO  | URT1 timeout timer overflow output signal                                           |
|      |    |  |  |   |   |                | SPI0_D3   | SPI0 data-3 signal for 4-I/O mode                                                   |
|      |    |  |  |   |   |                | TM26_OC1N | TM26 output compare/PWM complement channel-1                                        |
|      |    |  |  |   |   |                | SPI0_NSS  | SPI0 slave select input/output signal                                               |
|      |    |  |  |   |   |                | MA11      | External memory bus address pin 11                                                  |
|      |    |  |  |   |   |                | MWE       | External memory bus write enable(WE) or write strobe(WR) signal pin                 |
| PD12 | 66 |  |  | B | A | A,I,P,O,U,H,C2 | GPD12     | GPIO/Interrupt/KBI Port-D function pin-12                                           |
|      |    |  |  |   |   |                | CMP0_P0   | Comparator-0 data output                                                            |
|      |    |  |  |   |   |                | TM10_CKO  | TM10 timer overflow output signal                                                   |
|      |    |  |  |   |   |                | OBM_P0    | Output signal break control output signal-0                                         |
|      |    |  |  |   |   |                | TM00_CKO  | TM00 timer overflow output signal                                                   |
|      |    |  |  |   |   |                | SPI0_CLK  | SPI0 clock signal                                                                   |
|      |    |  |  |   |   |                | TM20_OC0H | TM20 output compare/PWM high channel-0                                              |
|      |    |  |  |   |   |                | TM26_OC0H | TM26 output compare/PWM high channel-0                                              |
|      |    |  |  |   |   |                | MA12      | External memory bus address pin 12                                                  |
|      |    |  |  |   |   |                | MALE2     | External memory bus 2nd address latch enable(ALE2) or command latch enable(CLE) pin |
| PD13 | 67 |  |  | B | A | A,I,P,O,U,H,C2 | GPD13     | GPIO/Interrupt/KBI Port-D function pin-13                                           |
|      |    |  |  |   |   |                | CMP1_P0   | Comparator-1 data output                                                            |
|      |    |  |  |   |   |                | TM10_TRGO | TM10 trigger output signal                                                          |
|      |    |  |  |   |   |                | OBM_P1    | Output signal break control output signal-1                                         |
|      |    |  |  |   |   |                | TM00_TRGO | TM00 trigger output signal                                                          |
|      |    |  |  |   |   |                | NCO_CK0   | NCO external clock input signal-0                                                   |
|      |    |  |  |   |   |                | TM20_OC1H | TM20 output compare/PWM high channel-1                                              |
|      |    |  |  |   |   |                | TM26_OC1H | TM26 output compare/PWM high channel-1                                              |
|      |    |  |  |   |   |                | MA13      | External memory bus address pin 13                                                  |
|      |    |  |  |   |   |                | MCE       | External memory bus chip enable/select pin                                          |
| PD14 | 68 |  |  | B | A | A,I,P,O,U,H,C2 | GPD14     | GPIO/Interrupt/KBI Port-D function pin-14                                           |
|      |    |  |  |   |   |                | TM10_ETR  | TM10 external trigger/clock input signal                                            |
|      |    |  |  |   |   |                | DAC_TRG0  | DAC trigger start input                                                             |
|      |    |  |  |   |   |                | TM00_ETR  | TM00 external trigger/clock input signal                                            |
|      |    |  |  |   |   |                | TM20_IC0  | TM20 input capture channel-0                                                        |
|      |    |  |  |   |   |                | TM26_IC0  | TM26 input capture channel-0                                                        |
|      |    |  |  |   |   |                | MA14      | External memory bus address pin 14                                                  |
|      |    |  |  |   |   |                | MOE       | External memory bus output enable(OE) or read strobe (RD) signal pin                |
|      |    |  |  |   |   |                | CCL_P0    | CCL output signal-0                                                                 |
|      |    |  |  |   |   |                | URT5_TX   | URT5 transmit TX signal. URT5_RX and URT5_TX can be swapped by register setting.    |
| PD15 | 69 |  |  | B | A | A,I,P,O,U,H,C2 | GPD15     | GPIO/Interrupt/KBI Port-D function pin-15                                           |
|      |    |  |  |   |   |                | NCO_P0    | NCO clock output signal-0                                                           |
|      |    |  |  |   |   |                | IR_OUT    | IR output signal                                                                    |
|      |    |  |  |   |   |                | DMA_TRG0  | DMA external trigger pin-0 input                                                    |
|      |    |  |  |   |   |                | TM20_IC1  | TM20 input capture channel-1                                                        |

|     |    |  |  |   |   |                |           |                                                                                                                                      |
|-----|----|--|--|---|---|----------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------|
|     |    |  |  |   |   |                | TM26_IC1  | TM26 input capture channel-1                                                                                                         |
|     |    |  |  |   |   |                | MA15      | External memory bus address pin 15                                                                                                   |
|     |    |  |  |   |   |                | CCL_P1    | CCL output signal-1                                                                                                                  |
|     |    |  |  |   |   |                | URT5_RX   | URT5 receive RX signal. URT5_RX and URT5_TX can be swapped by register setting.                                                      |
| PE0 | 14 |  |  | B | A | A,I,P,O,U,H,C4 | GPE0      | GPIO/Interrupt/KBI Port-E function pin-0                                                                                             |
|     |    |  |  |   |   |                | OBM_I0    | Output signal break control input signal-0                                                                                           |
|     |    |  |  |   |   |                | URT0_TX   | URT0 transmit TX signal, SPI master/slave data output signal. URT0_RX and URT0_TX can be swapped by register setting.                |
|     |    |  |  |   |   |                | DAC_TRG0  | DAC trigger start input                                                                                                              |
|     |    |  |  |   |   |                | SPI0_NSS  | SPI0 slave select input/output signal                                                                                                |
|     |    |  |  |   |   |                | TM20_OC00 | TM20 output compare/PWM channel-00                                                                                                   |
|     |    |  |  |   |   |                | TM26_OC00 | TM26 output compare/PWM channel-00                                                                                                   |
|     |    |  |  |   |   |                | MALE      | External memory bus address latch enable(ALE) or data/command select(DC) pin                                                         |
|     |    |  |  |   |   |                | MAD8      | External memory bus address/data pin 8                                                                                               |
|     |    |  |  |   |   |                | URT4_TX   | URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.                                                     |
| PE1 | 15 |  |  | B | A | A,I,P,O,U,H,C4 | GPE1      | GPIO/Interrupt/KBI Port-E function pin-1                                                                                             |
|     |    |  |  |   |   |                | OBM_I1    | Output signal break control input signal-1                                                                                           |
|     |    |  |  |   |   |                | URT0_RX   | URT0 receive RX signal, SPI master/slave data input signal. URT0_RX and URT0_TX can be swapped by register setting.                  |
|     |    |  |  |   |   |                | DMA_TRG1  | DMA external trigger pin-1 input                                                                                                     |
|     |    |  |  |   |   |                | SPI0_MISO | SPI0 master input / slave output signal or data-1 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting. |
|     |    |  |  |   |   |                | TM20_OC01 | TM20 output compare/PWM channel-01                                                                                                   |
|     |    |  |  |   |   |                | TM26_OC01 | TM26 output compare/PWM channel-01                                                                                                   |
|     |    |  |  |   |   |                | MOE       | External memory bus output enable(OE) or read strobe (RD) signal pin                                                                 |
|     |    |  |  |   |   |                | MAD9      | External memory bus address/data pin 9                                                                                               |
|     |    |  |  |   |   |                | TM36_OC0H | TM36 output compare/PWM high channel-0                                                                                               |
|     |    |  |  |   |   |                | URT4_RX   | URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting.                                                      |
| PE2 | 16 |  |  | B | A | A,I,P,O,U,H,C4 | GPE2      | GPIO/Interrupt/KBI Port-E function pin-2                                                                                             |
|     |    |  |  |   |   |                | OBM_P0    | Output signal break control output signal-0                                                                                          |
|     |    |  |  |   |   |                | I2C1_SCL  | I2C1 SCL signal                                                                                                                      |
|     |    |  |  |   |   |                | URT1_TX   | URT1 transmit TX signal, SPI master/slave data output signal. URT1_RX and URT1_TX can be swapped by register setting.                |
|     |    |  |  |   |   |                | NCO_P0    | NCO clock output signal-0                                                                                                            |
|     |    |  |  |   |   |                | SPI0_CLK  | SPI0 clock signal                                                                                                                    |
|     |    |  |  |   |   |                | TM20_OC02 | TM20 output compare/PWM channel-02                                                                                                   |
|     |    |  |  |   |   |                | TM26_OC02 | TM26 output compare/PWM channel-02                                                                                                   |
|     |    |  |  |   |   |                | MWE       | External memory bus write enable(WE) or write strobe(WR) signal pin                                                                  |

|     |    |  |  |   |   |                |           |                                                                                                                                      |
|-----|----|--|--|---|---|----------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------|
|     |    |  |  |   |   |                | MAD10     | External memory bus address/data pin 10                                                                                              |
|     |    |  |  |   |   |                | TM36_OC1H | TM36 output compare/PWM high channel-1                                                                                               |
|     |    |  |  |   |   |                | URT5_TX   | URT5 transmit TX signal. URT5_RX and URT5_TX can be swapped by register setting.                                                     |
| PE3 | 17 |  |  | B | A | A,I,P,O,U,H,C4 | GPE3      | GPIO/Interrupt/KBI Port-E function pin-3                                                                                             |
|     |    |  |  |   |   |                | OBM_P1    | Output signal break control output signal-1                                                                                          |
|     |    |  |  |   |   |                | I2C1_SDA  | I2C1 SDA signal                                                                                                                      |
|     |    |  |  |   |   |                | URT1_RX   | URT1 receive RX signal, SPI master/slave data input signal. URT1_RX and URT1_TX can be swapped by register setting.                  |
|     |    |  |  |   |   |                | NCO_CK0   | NCO external clock input signal-0                                                                                                    |
|     |    |  |  |   |   |                | SPI0_MOSI | SPI0 master output / slave input signal or data-0 signal for 4-I/O mode. SPI0_MOSI and SPI0_MISO can be swapped by register setting. |
|     |    |  |  |   |   |                | TM20_OC0N | TM20 output compare/PWM complement channel-0                                                                                         |
|     |    |  |  |   |   |                | TM26_OC0N | TM26 output compare/PWM complement channel-0                                                                                         |
|     |    |  |  |   |   |                | MCE       | External memory bus chip enable/select pin                                                                                           |
|     |    |  |  |   |   |                | MALE2     | External memory bus 2nd address latch enable(ALE2) or command latch enable(CLE) pin                                                  |
|     |    |  |  |   |   |                | URT5_RX   | URT5 receive RX signal. URT5_RX and URT5_TX can be swapped by register setting.                                                      |
| PE8 | 32 |  |  | B | A | A,I,P,O,U,H,C2 | GPE8      | GPIO/Interrupt/KBI Port-E function pin-8                                                                                             |
|     |    |  |  |   |   |                | CPU_TXEV  | CPU wakeup event output                                                                                                              |
|     |    |  |  |   |   |                | OBM_I0    | Output signal break control input signal-0                                                                                           |
|     |    |  |  |   |   |                | URT2_TX   | URT2 transmit TX signal, SPI master/slave data output signal. URT2_RX and URT2_TX can be swapped by register setting.                |
|     |    |  |  |   |   |                | SDT_I0    | State detect input signal-0                                                                                                          |
|     |    |  |  |   |   |                | TM36_CKO  | TM36 timer overflow output signal                                                                                                    |
|     |    |  |  |   |   |                | TM20_CKO  | TM20 timer overflow output signal                                                                                                    |
|     |    |  |  |   |   |                | TM26_CKO  | TM26 timer overflow output signal                                                                                                    |
|     |    |  |  |   |   |                | MAD11     | External memory bus address/data pin 11                                                                                              |
|     |    |  |  |   |   |                | URT4_TX   | URT4 transmit TX signal. URT4_RX and URT4_TX can be swapped by register setting.                                                     |
| PE9 | 33 |  |  | B | A | A,I,P,O,U,H,C2 | GPE9      | GPIO/Interrupt/KBI Port-E function pin-9                                                                                             |
|     |    |  |  |   |   |                | CPU_RXEV  | CPU wakeup event input                                                                                                               |
|     |    |  |  |   |   |                | OBM_I1    | Output signal break control input signal-1                                                                                           |
|     |    |  |  |   |   |                | URT2_RX   | URT2 receive RX signal, SPI master/slave data input signal. URT2_RX and URT2_TX can be swapped by register setting.                  |
|     |    |  |  |   |   |                | SDT_I1    | State detect input signal-1                                                                                                          |
|     |    |  |  |   |   |                | TM36_TRGO | TM36 trigger output signal                                                                                                           |
|     |    |  |  |   |   |                | TM20_TRGO | TM20 trigger output signal                                                                                                           |
|     |    |  |  |   |   |                | TM26_TRGO | TM26 trigger output signal                                                                                                           |
|     |    |  |  |   |   |                | MOE       | External memory bus output enable(OE) or read                                                                                        |

|      |    |  |  |   |   |         |                                                                                  |                                                                                 |                                                                                     |
|------|----|--|--|---|---|---------|----------------------------------------------------------------------------------|---------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
|      |    |  |  |   |   |         |                                                                                  | strobe (RD) signal pin                                                          |                                                                                     |
|      |    |  |  |   |   |         | URT4_RX                                                                          | URT4 receive RX signal. URT4_RX and URT4_TX can be swapped by register setting. |                                                                                     |
| PE12 | 50 |  |  | B | A |         | A,I,P,O,U,H,C2                                                                   | GPE12                                                                           | GPIO/Interrupt/KBI Port-E function pin-12                                           |
|      |    |  |  |   |   |         |                                                                                  | ADC0_TRG                                                                        | ADC trigger start input                                                             |
|      |    |  |  |   |   |         |                                                                                  |                                                                                 |                                                                                     |
|      |    |  |  |   |   |         |                                                                                  | TM01_CKO                                                                        | TM01 timer overflow output signal                                                   |
|      |    |  |  |   |   |         |                                                                                  | TM16_CKO                                                                        | TM16 timer overflow output signal                                                   |
|      |    |  |  |   |   |         |                                                                                  | TM20_OC10                                                                       | TM20 output compare/PWM channel-10                                                  |
|      |    |  |  |   |   |         |                                                                                  | TM26_OC10                                                                       | TM26 output compare/PWM channel-10                                                  |
|      |    |  |  |   |   |         |                                                                                  | MBW0                                                                            | External memory bus byte write enable 0 pin                                         |
|      |    |  |  |   |   | URT6_TX | URT6 transmit TX signal. URT6_RX and URT6_TX can be swapped by register setting. |                                                                                 |                                                                                     |
| PE13 | 51 |  |  | B | A |         | A,I,P,O,U,H,C2                                                                   | GPE13                                                                           | GPIO/Interrupt/KBI Port-E function pin-13                                           |
|      |    |  |  |   |   |         |                                                                                  | ADC0_OUT                                                                        | ADC threshold window compare output                                                 |
|      |    |  |  |   |   |         |                                                                                  |                                                                                 |                                                                                     |
|      |    |  |  |   |   |         |                                                                                  | TM01_TRGO                                                                       | TM01 trigger output signal                                                          |
|      |    |  |  |   |   |         |                                                                                  | TM16_TRGO                                                                       | TM16 trigger output signal                                                          |
|      |    |  |  |   |   |         |                                                                                  | TM20_OC11                                                                       | TM20 output compare/PWM channel-11                                                  |
|      |    |  |  |   |   |         |                                                                                  | TM26_OC11                                                                       | TM26 output compare/PWM channel-11                                                  |
|      |    |  |  |   |   |         |                                                                                  | MBW1                                                                            | External memory bus byte write enable 1 pin                                         |
|      |    |  |  |   |   |         |                                                                                  | TM36_OC2H                                                                       | TM36 output compare/PWM high channel-2                                              |
|      |    |  |  |   |   | URT6_RX | URT6 receive RX signal. URT6_RX and URT6_TX can be swapped by register setting.  |                                                                                 |                                                                                     |
| PE14 | 52 |  |  | B | A |         | A,I,P,O,U,H,C2                                                                   | GPE14                                                                           | GPIO/Interrupt/KBI Port-E function pin-14                                           |
|      |    |  |  |   |   |         |                                                                                  | RTC_OUT                                                                         | RTC selection output signal                                                         |
|      |    |  |  |   |   |         |                                                                                  | I2C1_SCL                                                                        | I2C1 SCL signal                                                                     |
|      |    |  |  |   |   |         |                                                                                  | TM01_ETR                                                                        | TM01 external trigger/clock input signal                                            |
|      |    |  |  |   |   |         |                                                                                  | TM16_ETR                                                                        | TM16 external trigger/clock input signal                                            |
|      |    |  |  |   |   |         |                                                                                  | TM20_OC12                                                                       | TM20 output compare/PWM channel-12                                                  |
|      |    |  |  |   |   |         |                                                                                  | TM26_OC12                                                                       | TM26 output compare/PWM channel-12                                                  |
|      |    |  |  |   |   |         |                                                                                  | MALE2                                                                           | External memory bus 2nd address latch enable(ALE2) or command latch enable(CLE) pin |
|      |    |  |  |   |   |         |                                                                                  | CCL_P0                                                                          | CCL output signal-0                                                                 |
|      |    |  |  |   |   |         |                                                                                  | TM36_OC3H                                                                       | TM36 output compare/PWM high channel-3                                              |
|      |    |  |  |   |   | URT7_TX | URT7 transmit TX signal. URT7_RX and URT7_TX can be swapped by register setting. |                                                                                 |                                                                                     |
| PE15 | 53 |  |  | B | A |         | A,I,P,O,U,H,C2                                                                   | GPE15                                                                           | GPIO/Interrupt/KBI Port-E function pin-15                                           |
|      |    |  |  |   |   |         |                                                                                  | RTC_TS                                                                          | RTC time stamp input signal                                                         |
|      |    |  |  |   |   |         |                                                                                  | I2C1_SDA                                                                        | I2C1 SDA signal                                                                     |
|      |    |  |  |   |   |         |                                                                                  | TM36_BK0                                                                        | TM36 break input signal                                                             |
|      |    |  |  |   |   |         |                                                                                  | TM36_ETR                                                                        | TM36 external trigger/clock input signal                                            |
|      |    |  |  |   |   |         |                                                                                  | TM20_OC1N                                                                       | TM20 output compare/PWM complement channel-1                                        |
|      |    |  |  |   |   |         |                                                                                  | TM26_OC1N                                                                       | TM26 output compare/PWM complement channel-1                                        |
|      |    |  |  |   |   | MALE    | External memory bus address latch                                                |                                                                                 |                                                                                     |

## MG32F02A128/A064

|       |    |    |    |    |    |  |  |         |                                                                                 |
|-------|----|----|----|----|----|--|--|---------|---------------------------------------------------------------------------------|
|       |    |    |    |    |    |  |  |         | enable(ALE) or data/command select(DC) pin                                      |
|       |    |    |    |    |    |  |  | CCL_P1  | CCL output signal-1                                                             |
|       |    |    |    |    |    |  |  | URT7_RX | URT7 receive RX signal. URT7_RX and URT7_TX can be swapped by register setting. |
| VSS   | 70 | 54 | 41 | P  |    |  |  |         | IO/Core/ADC ground                                                              |
| VSS2  | 30 |    |    | P  |    |  |  |         | IO ground                                                                       |
| VSS1  | 49 | 41 |    | P  |    |  |  |         | IO ground                                                                       |
| VR0   | 71 | 55 | 42 | AO | AO |  |  |         | Core power supply/LDO output (place 0.1uF+4.7uF capacitors and close pin)       |
| VDD   | 72 | 56 | 43 | P  |    |  |  |         | IO power supply/LDO input (place 0.1uF+10uF capacitors and close pin)           |
| VDD2  | 27 |    |    | P  |    |  |  |         | IO power supply (place 0.1uF+10uF capacitors and close pin)                     |
| VREF+ | 73 | 57 | 44 | AI | AI |  |  |         | ADC voltage reference (place 0.1uF+4.7uF capacitors and close pin)              |

### 4.3. Pin AFS Summary Table

The following table is the AFS signal list of the related IO pin for all pins' summary. (AFS=n, n: I/O pin AFS setting value)

Table 4-6. Pin AFS Summary Table

| Pin  | AFS=0 | AFS=1    | AFS=2     | AFS=3     | AFS=4    | AFS=5     | AFS=6     | AFS=7     | AFS=8 | AFS=9    | AFS=10    | AFS=11   |
|------|-------|----------|-----------|-----------|----------|-----------|-----------|-----------|-------|----------|-----------|----------|
| PA0  | GPA0  |          |           |           |          |           | SDT_P0    | CCL_P0    | MA0   | MAD0     | TM36_OC00 | URT4_TX  |
| PA1  | GPA1  |          |           |           |          |           |           | CCL_P1    | MA1   | MAD1     | TM36_OC10 | URT4_RX  |
| PA2  | GPA2  |          |           |           |          |           | SDT_I0    |           | MA2   | MAD2     | TM36_OC2  | URT5_TX  |
| PA3  | GPA3  |          |           |           |          |           | SDT_I1    |           | MA3   | MAD3     | TM36_OC2N | URT5_RX  |
| PA4  | GPA4  |          |           |           |          |           |           |           | MA4   | MAD4     | TM20_OC00 | URT0_TX  |
| PA5  | GPA5  |          |           |           |          |           |           |           | MA5   | MAD5     | TM20_OC10 | URT0_RX  |
| PA6  | GPA6  |          |           |           |          |           |           | SPI0_D3   | MA6   | MAD6     | TM20_OC0H | URT0_CLK |
| PA7  | GPA7  |          |           |           |          |           |           | SPI0_D2   | MA7   | MAD7     | TM20_OC1H | URT0_NSS |
| PA8  | GPA8  | DMA_TRG0 |           | I2C0_SCL  | URT2_BRO | SDT_I0    | TM20_IC0  | SPI0_NSS  | MA8   | MAD0     | TM36_OC0H | URT4_TX  |
| PA9  | GPA9  | DMA_TRG1 |           | I2C1_SCL  | URT2_TMO |           | TM20_IC1  | SPI0_MISO | MA9   | MAD1     | TM36_OC1H | URT5_TX  |
| PA10 | GPA10 | TM36_BK0 | SPI0_D2   | I2C0_SDA  | URT2_CTS | SDT_I1    | TM26_IC0  | SPI0_CLK  | MA10  | MAD2     | TM36_OC2H | URT4_RX  |
| PA11 | GPA11 | DAC_TRG0 | SPI0_D3   | I2C1_SDA  | URT2_RTS |           | TM26_IC1  | SPI0_MOSI | MA11  | MAD3     | TM36_OC3H | URT5_RX  |
| PA12 | GPA12 |          |           |           | URT1_BRO | TM10_ETR  | TM36_IC0  | SPI0_D5   | MA12  | MAD4     | TM26_OC00 | URT6_TX  |
| PA13 | GPA13 | CPU_TXEV |           | URT0_BRO  | URT1_TMO | TM10_TRGO | TM36_IC1  | SPI0_D6   | MA13  | MAD5     | TM26_OC10 | URT6_RX  |
| PA14 | GPA14 | CPU_RXEV | OBM_I0    | URT0_TMO  | URT1_CTS | TM16_ETR  | TM36_IC2  | SPI0_D7   | MA14  | MAD6     | TM26_OC0H | URT7_TX  |
| PA15 | GPA15 | CPU_NMI  | OBM_I1    | URT0_DE   | URT1_RTS | TM16_TRGO | TM36_IC3  | SPI0_D4   | MA15  | MAD7     | TM26_OC1H | URT7_RX  |
| PB0  | GPB0  | I2C1_SCL | SPI0_NSS  | TM01_ETR  | TM00_CKO | TM16_ETR  | TM26_IC0  | TM36_ETR  | MA15  | URT1_NSS |           | URT6_TX  |
| PB1  | GPB1  | I2C1_SDA | SPI0_MISO | TM01_TRGO | TM10_CKO | TM16_TRGO | TM26_IC1  | TM36_TRGO |       | URT1_RX  |           | URT6_RX  |
| PB2  | GPB2  | ADC0_TRG | SPI0_CLK  | TM01_CKO  | URT2_TX  | TM16_CKO  | TM26_OC0H | I2C0_SDA  |       | URT1_CLK | URT0_TX   | URT7_TX  |
| PB3  | GPB3  | ADC0_OUT | SPI0_MOSI | NCO_P0    | URT2_RX  | TM36_CKO  | TM26_OC1H | I2C0_SCL  |       | URT1_TX  | URT0_RX   | URT7_RX  |
| PB4  | GPB4  | TM01_CKO | SPI0_D3   | TM26_TRGO | URT2_CLK | TM20_IC0  | TM36_IC0  |           | MALE  | MAD8     |           |          |
| PB5  | GPB5  | TM16_CKO | SPI0_D2   | TM26_ETR  | URT2_NSS | TM20_IC1  | TM36_IC1  |           | MOE   | MAD9     |           |          |
| PB6  | GPB6  | CPU_RXEV | SPI0_NSSI | URT0_BRO  | URT2_CTS | TM20_ETR  | TM36_IC2  |           | MWE   | MAD10    |           | URT2_TX  |
| PB7  | GPB7  | CPU_TXEV |           | URT0_TMO  | URT2_RTS | TM20_TRGO | TM36_IC3  |           | MCE   | MALE2    |           | URT2_RX  |
| PB8  | GPB8  | CMP0_P0  | RTC_OUT   | URT0_TX   | URT2_BRO | TM20_OC01 | TM36_OC01 | SPI0_D3   | MAD0  | SDT_P0   | OBM_P0    | URT4_TX  |
| PB9  | GPB9  | CMP1_P0  | RTC_TS    | URT0_RX   | URT2_TMO | TM20_OC02 | TM36_OC02 | SPI0_D2   | MAD1  | MAD8     | OBM_P1    | URT4_RX  |
| PB10 | GPB10 |          | I2C0_SCL  | URT0_NSS  | URT2_DE  | TM20_OC11 | TM36_OC11 | URT1_TX   | MAD2  | MAD1     | SPI0_NSSI |          |
| PB11 | GPB11 |          | I2C0_SDA  | URT0_DE   | IR_OUT   | TM20_OC12 | TM36_OC12 | URT1_RX   | MAD3  | MAD9     | DMA_TRG0  | URT0_CLK |
| PB12 | GPB12 | DMA_TRG0 | NCO_P0    |           |          |           |           | URT1_CLK  | MAD4  | MAD2     |           | URT5_TX  |
| PB13 | GPB13 | DAC_TRG0 | TM00_ETR  | URT0_CTS  |          | TM20_ETR  | TM36_ETR  | URT0_CLK  | MAD5  | MAD10    | CCL_P0    | URT4_RX  |
| PB14 | GPB14 | DMA_TRG0 | TM00_TRGO | URT0_RTS  |          | TM20_TRGO | TM36_BK0  | URT0_NSS  | MAD6  | MAD3     | CCL_P1    | URT4_TX  |
| PB15 | GPB15 | IR_OUT   | NCO_CK0   |           |          |           |           | URT1_NSS  | MAD7  | MAD11    |           | URT5_RX  |
| PC0  | GPC0  | ICKO     | TM00_CKO  | URT0_CLK  | URT2_CLK | TM20_OC00 | TM36_OC00 | I2C0_SCL  | MCLK  | MWE      | URT0_TX   | URT5_TX  |
| PC1  | GPC1  | ADC0_TRG | TM01_CKO  | TM36_IC0  | URT1_CLK | TM20_OC0N | TM36_OC0N | I2C0_SDA  | MAD8  | MAD4     | URT0_RX   | URT5_RX  |
| PC2  | GPC2  | ADC0_OUT | TM10_CKO  | OBM_P0    | URT2_CLK | TM20_OC10 | TM36_OC10 | SDT_I0    | MAD9  | MAD12    |           |          |
| PC3  | GPC3  | OBM_P1   | TM16_CKO  | URT0_CLK  | URT1_CLK | TM20_OC1N | TM36_OC1N | SDT_I1    | MAD10 | MAD5     |           |          |
| PC4  | GPC4  | SWCLK    | I2C0_SCL  | URT0_RX   | URT1_RX  |           | TM36_OC2  | SDT_I0    |       |          |           | URT6_RX  |
| PC5  | GPC5  | SWDIO    | I2C0_SDA  | URT0_TX   | URT1_TX  |           | TM36_OC3  | SDT_I1    |       |          |           | URT6_TX  |
| PC6  | GPC6  | RSTN     | RTC_TS    | URT0_NSS  | URT1_NSS | TM20_ETR  | TM26_ETR  |           | MBW1  | MALE     |           |          |
| PC7  | GPC7  | ADC0_TRG | RTC_OUT   | URT0_DE   | URT1_NSS |           | TM36_TRGO |           | MBW0  | MCE      |           |          |
| PC8  | GPC8  | ADC0_OUT | I2C0_SCL  | URT0_BRO  | URT1_TX  | TM20_OC0H | TM36_OC0H | TM36_OC0N | MAD11 | MAD13    | CCL_P0    | URT6_TX  |
| PC9  | GPC9  | CMP0_P0  | I2C0_SDA  | URT0_TMO  | URT1_RX  | TM20_OC1H | TM36_OC1H | TM36_OC1N | MAD12 | MAD6     | CCL_P1    | URT6_RX  |

# MG32F02A128/A064

|      |       |           |           |          |           |           |           |           |          |        |           |           |
|------|-------|-----------|-----------|----------|-----------|-----------|-----------|-----------|----------|--------|-----------|-----------|
| PC10 | GPC10 | CMP1_P0   | I2C1_SCL  | URT0_TX  | URT2_TX   | URT1_TX   | TM36_OC2H | TM36_OC2N | MAD13    | MAD14  |           | URT7_TX   |
| PC11 | GPC11 |           | I2C1_SDA  | URT0_RX  | URT2_RX   | URT1_RX   | TM36_OC3H | TM26_OC01 | MAD14    | MAD7   |           | URT7_RX   |
| PC12 | GPC12 |           | IR_OUT    | DAC_TRG0 | URT1_DE   | TM10_TRGO | TM36_OC3  | TM26_OC02 | MAD15    | SDT_P0 |           |           |
| PC13 | GPC13 | XIN       | URT1_NSS  | URT0_CTS | URT2_RX   | TM10_ETR  | TM26_ETR  | TM36_OC00 | TM20_IC0 | SDT_I0 |           | URT6_RX   |
| PC14 | GPC14 | XOUT      | URT1_TMO  | URT0_RTS | URT2_TX   | TM10_CKO  | TM26_TRGO | TM36_OC10 | TM20_IC1 | SDT_I1 |           | URT6_TX   |
| PD0  | GPD0  | OBM_I0    | TM10_CKO  | URT0_CLK | TM26_OC1N | TM20_CKO  | TM36_OC2  | SPI0_NSS  | MA0      | MCLK   |           | URT2_NSS  |
| PD1  | GPD1  | OBM_I1    | TM16_CKO  | URT0_CLK | NCO_CK0   | TM26_CKO  | TM36_OC2N | SPI0_CLK  | MA1      |        |           | URT2_CLK  |
| PD2  | GPD2  |           | TM00_CKO  | URT1_CLK | TM26_OC00 | TM20_CKO  | TM36_CKO  | SPI0_MOSI | MA2      | MAD4   |           | URT2_TX   |
| PD3  | GPD3  |           | TM01_CKO  | URT1_CLK |           | SPI0_MISO | TM26_CKO  | SPI0_D3   | MA3      | MAD7   | TM36_TRGO | URT2_RX   |
| PD4  | GPD4  | TM00_TRGO | TM01_TRGO | URT1_TX  |           |           | TM26_OC00 | SPI0_D2   | MA4      | MAD6   |           | URT2_TX   |
| PD5  | GPD5  | TM00_ETR  | I2C0_SCL  | URT1_RX  |           |           | TM26_OC01 | SPI0_MISO | MA5      | MAD5   |           | URT2_RX   |
| PD6  | GPD6  | CPU_NMI   | I2C0_SDA  | URT1_NSS |           | SPI0_NSSI | TM26_OC02 | SPI0_NSS  | MA6      | SDT_P0 |           | URT2_NSS  |
| PD7  | GPD7  | TM00_CKO  | TM01_ETR  | URT1_DE  |           | SPI0_MISO | TM26_OC0N | SPI0_D4   | MA7      | MAD0   | TM36_IC0  |           |
| PD8  | GPD8  | CPU_TXEV  | TM01_TRGO | URT1_RTS |           | SPI0_D2   | TM26_OC10 | SPI0_D7   | MA8      | MAD3   | TM36_IC1  | SPI0_CLK  |
| PD9  | GPD9  | CPU_RXEV  | TM00_TRGO | URT1_CTS |           | SPI0_NSSI | TM26_OC11 | SPI0_D6   | MA9      | MAD2   | TM36_IC2  | SPI0_NSS  |
| PD10 | GPD10 | CPU_NMI   | TM00_ETR  | URT1_BRO |           | RTC_OUT   | TM26_OC12 | SPI0_D5   | MA10     | MAD1   | TM36_IC3  | SPI0_MOSI |
| PD11 | GPD11 | CPU_NMI   | DMA_TRG1  | URT1_TMO |           | SPI0_D3   | TM26_OC1N | SPI0_NSS  | MA11     | MWE    |           |           |
| PD12 | GPD12 | CMP0_P0   | TM10_CKO  | OBM_P0   | TM00_CKO  | SPI0_CLK  | TM20_OC0H | TM26_OC0H | MA12     | MALE2  |           |           |
| PD13 | GPD13 | CMP1_P0   | TM10_TRGO | OBM_P1   | TM00_TRGO | NCO_CK0   | TM20_OC1H | TM26_OC1H | MA13     | MCE    |           |           |
| PD14 | GPD14 |           | TM10_ETR  | DAC_TRG0 | TM00_ETR  |           | TM20_IC0  | TM26_IC0  | MA14     | MOE    | CCL_P0    | URT5_TX   |
| PD15 | GPD15 |           | NCO_P0    | IR_OUT   | DMA_TRG0  |           | TM20_IC1  | TM26_IC1  | MA15     |        | CCL_P1    | URT5_RX   |
| PE0  | GPE0  | OBM_I0    |           | URT0_TX  | DAC_TRG0  | SPI0_NSS  | TM20_OC00 | TM26_OC00 | MALE     | MAD8   |           | URT4_TX   |
| PE1  | GPE1  | OBM_I1    |           | URT0_RX  | DMA_TRG1  | SPI0_MISO | TM20_OC01 | TM26_OC01 | MOE      | MAD9   | TM36_OC0H | URT4_RX   |
| PE2  | GPE2  | OBM_P0    | I2C1_SCL  | URT1_TX  | NCO_P0    | SPI0_CLK  | TM20_OC02 | TM26_OC02 | MWE      | MAD10  | TM36_OC1H | URT5_TX   |
| PE3  | GPE3  | OBM_P1    | I2C1_SDA  | URT1_RX  | NCO_CK0   | SPI0_MOSI | TM20_OC0N | TM26_OC0N | MCE      | MALE2  |           | URT5_RX   |
| PE8  | GPE8  | CPU_TXEV  | OBM_I0    | URT2_TX  | SDT_I0    | TM36_CKO  | TM20_CKO  | TM26_CKO  |          | MAD11  |           | URT4_TX   |
| PE9  | GPE9  | CPU_RXEV  | OBM_I1    | URT2_RX  | SDT_I1    | TM36_TRGO | TM20_TRGO | TM26_TRGO |          | MOE    |           | URT4_RX   |
| PE10 | GPE10 | I2C0_SCL  | I2C1_SCL  | URT0_TX  | URT4_TX   |           |           |           |          | SDT_I0 |           |           |
| PE11 | GPE11 | I2C0_SDA  | I2C1_SDA  | URT0_RX  | URT4_RX   |           |           |           |          | SDT_I1 |           |           |
| PE12 | GPE12 | ADC0_TRG  |           |          | TM01_CKO  | TM16_CKO  | TM20_OC10 | TM26_OC10 | MBW0     |        |           | URT6_TX   |
| PE13 | GPE13 | ADC0_OUT  |           |          | TM01_TRGO | TM16_TRGO | TM20_OC11 | TM26_OC11 | MBW1     |        | TM36_OC2H | URT6_RX   |
| PE14 | GPE14 | RTC_OUT   | I2C1_SCL  |          | TM01_ETR  | TM16_ETR  | TM20_OC12 | TM26_OC12 | MALE2    | CCL_P0 | TM36_OC3H | URT7_TX   |
| PE15 | GPE15 | RTC_TS    | I2C1_SDA  |          | TM36_BK0  | TM36_ETR  | TM20_OC1N | TM26_OC1N | MALE     | CCL_P1 |           | URT7_RX   |
| Pin  | AFS=0 | AFS=1     | AFS=2     | AFS=3    | AFS=4     | AFS=5     | AFS=6     | AFS=7     | AFS=8    | AFS=9  | AFS=10    | AFS=11    |

[Package Pin Group Indication by  
Background Color]

|  |                                                     |
|--|-----------------------------------------------------|
|  | Light Blue Color : Not supported High Speed<br>Pins |
|  | Light Cyan Color : Supported ODC 4-Level<br>Pins    |

## 4.1. Analog Function Pin Table

The following table is the analog signal pin list for all the analog function.

**Table 4-7. Analog Function Pin Table**

| Pin Name | ADC     | CMP     | Others  |
|----------|---------|---------|---------|
| PA0      | ADC_I0  |         |         |
| PA1      | ADC_I1  |         |         |
| PA2      | ADC_I2  |         |         |
| PA3      | ADC_I3  |         |         |
| PA4      | ADC_I4  |         |         |
| PA5      | ADC_I5  |         |         |
| PA6      | ADC_I6  |         |         |
| PA7      | ADC_I7  |         |         |
| PA8      | ADC_I8  | CMP0_I0 | VBG_OUT |
| PA9      | ADC_I9  | CMP0_I1 |         |
| PA10     | ADC_I10 | CMP1_I0 | ADC_PGA |
| PA11     | ADC_I11 | CMP1_I1 |         |
| PA12     | ADC_I12 |         |         |
| PA13     | ADC_I13 |         |         |
| PA14     | ADC_I14 |         |         |
| PA15     | ADC_I15 |         |         |
| PB0      |         | CMP_C0  |         |
| PB1      |         | CMP_C1  |         |
| PB2      |         |         | DAC_P0  |

## 4.2. Alternate Functions Pin List

The following table is the pin list of the related AFS IO signal for all AFS signals' summary.

**Table 4-8. Alternate Functions Pin List**

| No. | AFS List |          | Pin List for the AFS IO ([ ] : AFS setting value) |               |               |               |               |               |               |               |
|-----|----------|----------|---------------------------------------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
|     | Group    | AFS Name | Pin-1<br>Name                                     | Pin-2<br>Name | Pin-3<br>Name | Pin-4<br>Name | Pin-5<br>Name | Pin-6<br>Name | Pin-7<br>Name | Pin-8<br>Name |
| 1   | GPA      | GPA0     | PA0 [0]                                           |               |               |               |               |               |               |               |
| 2   |          | GPA1     | PA1 [0]                                           |               |               |               |               |               |               |               |
| 3   |          | GPA2     | PA2 [0]                                           |               |               |               |               |               |               |               |
| 4   |          | GPA3     | PA3 [0]                                           |               |               |               |               |               |               |               |
| 5   |          | GPA4     | PA4 [0]                                           |               |               |               |               |               |               |               |
| 6   |          | GPA5     | PA5 [0]                                           |               |               |               |               |               |               |               |
| 7   |          | GPA6     | PA6 [0]                                           |               |               |               |               |               |               |               |
| 8   |          | GPA7     | PA7 [0]                                           |               |               |               |               |               |               |               |
| 9   |          | GPA8     | PA8 [0]                                           |               |               |               |               |               |               |               |
| 10  |          | GPA9     | PA9 [0]                                           |               |               |               |               |               |               |               |
| 11  |          | GPA10    | PA10 [0]                                          |               |               |               |               |               |               |               |
| 12  |          | GPA11    | PA11 [0]                                          |               |               |               |               |               |               |               |
| 13  |          | GPA12    | PA12 [0]                                          |               |               |               |               |               |               |               |
| 14  |          | GPA13    | PA13 [0]                                          |               |               |               |               |               |               |               |
| 15  |          | GPA14    | PA14 [0]                                          |               |               |               |               |               |               |               |
| 16  |          | GPA15    | PA15 [0]                                          |               |               |               |               |               |               |               |
| 17  | GPB      | GPB0     | PB0 [0]                                           |               |               |               |               |               |               |               |
| 18  |          | GPB1     | PB1 [0]                                           |               |               |               |               |               |               |               |
| 19  |          | GPB2     | PB2 [0]                                           |               |               |               |               |               |               |               |
| 20  |          | GPB3     | PB3 [0]                                           |               |               |               |               |               |               |               |
| 21  |          | GPB4     | PB4 [0]                                           |               |               |               |               |               |               |               |
| 22  |          | GPB5     | PB5 [0]                                           |               |               |               |               |               |               |               |
| 23  |          | GPB6     | PB6 [0]                                           |               |               |               |               |               |               |               |
| 24  |          | GPB7     | PB7 [0]                                           |               |               |               |               |               |               |               |
| 25  |          | GPB8     | PB8 [0]                                           |               |               |               |               |               |               |               |
| 26  |          | GPB9     | PB9 [0]                                           |               |               |               |               |               |               |               |
| 27  |          | GPB10    | PB10 [0]                                          |               |               |               |               |               |               |               |
| 28  |          | GPB11    | PB11 [0]                                          |               |               |               |               |               |               |               |
| 29  |          | GPB12    | PB12 [0]                                          |               |               |               |               |               |               |               |
| 30  |          | GPB13    | PB13 [0]                                          |               |               |               |               |               |               |               |
| 31  |          | GPB14    | PB14 [0]                                          |               |               |               |               |               |               |               |
| 32  |          | GPB15    | PB15 [0]                                          |               |               |               |               |               |               |               |
| 33  | GPC      | GPC0     | PC0 [0]                                           |               |               |               |               |               |               |               |
| 34  |          | GPC1     | PC1 [0]                                           |               |               |               |               |               |               |               |
| 35  |          | GPC2     | PC2 [0]                                           |               |               |               |               |               |               |               |
| 36  |          | GPC3     | PC3 [0]                                           |               |               |               |               |               |               |               |
| 37  |          | GPC4     | PC4 [0]                                           |               |               |               |               |               |               |               |
| 38  |          | GPC5     | PC5 [0]                                           |               |               |               |               |               |               |               |
| 39  |          | GPC6     | PC6 [0]                                           |               |               |               |               |               |               |               |
| 40  |          | GPC7     | PC7 [0]                                           |               |               |               |               |               |               |               |
| 41  |          | GPC8     | PC8 [0]                                           |               |               |               |               |               |               |               |

|    |       |          |          |          |          |          |          |          |         |          |
|----|-------|----------|----------|----------|----------|----------|----------|----------|---------|----------|
| 42 |       | GPC9     | PC9 [0]  |          |          |          |          |          |         |          |
| 43 |       | GPC10    | PC10 [0] |          |          |          |          |          |         |          |
| 44 |       | GPC11    | PC11 [0] |          |          |          |          |          |         |          |
| 45 |       | GPC12    | PC12 [0] |          |          |          |          |          |         |          |
| 46 |       | GPC13    | PC13 [0] |          |          |          |          |          |         |          |
| 47 |       | GPC14    | PC14 [0] |          |          |          |          |          |         |          |
| 48 | GPD   | GPD0     | PD0 [0]  |          |          |          |          |          |         |          |
| 49 |       | GPD1     | PD1 [0]  |          |          |          |          |          |         |          |
| 50 |       | GPD2     | PD2 [0]  |          |          |          |          |          |         |          |
| 51 |       | GPD3     | PD3 [0]  |          |          |          |          |          |         |          |
| 52 |       | GPD4     | PD4 [0]  |          |          |          |          |          |         |          |
| 53 |       | GPD5     | PD5 [0]  |          |          |          |          |          |         |          |
| 54 |       | GPD6     | PD6 [0]  |          |          |          |          |          |         |          |
| 55 |       | GPD7     | PD7 [0]  |          |          |          |          |          |         |          |
| 56 |       | GPD8     | PD8 [0]  |          |          |          |          |          |         |          |
| 57 |       | GPD9     | PD9 [0]  |          |          |          |          |          |         |          |
| 58 |       | GPD10    | PD10 [0] |          |          |          |          |          |         |          |
| 59 |       | GPD11    | PD11 [0] |          |          |          |          |          |         |          |
| 60 |       | GPD12    | PD12 [0] |          |          |          |          |          |         |          |
| 61 |       | GPD13    | PD13 [0] |          |          |          |          |          |         |          |
| 62 |       | GPD14    | PD14 [0] |          |          |          |          |          |         |          |
| 63 |       | GPD15    | PD15 [0] |          |          |          |          |          |         |          |
| 64 | GPE   | GPE0     | PE0 [0]  |          |          |          |          |          |         |          |
| 65 |       | GPE1     | PE1 [0]  |          |          |          |          |          |         |          |
| 66 |       | GPE2     | PE2 [0]  |          |          |          |          |          |         |          |
| 67 |       | GPE3     | PE3 [0]  |          |          |          |          |          |         |          |
| 68 |       | GPE8     | PE8 [0]  |          |          |          |          |          |         |          |
| 69 |       | GPE9     | PE9 [0]  |          |          |          |          |          |         |          |
| 70 |       | GPE10    | PE10 [0] |          |          |          |          |          |         |          |
| 71 |       | GPE11    | PE11 [0] |          |          |          |          |          |         |          |
| 72 |       | GPE12    | PE12 [0] |          |          |          |          |          |         |          |
| 73 |       | GPE13    | PE13 [0] |          |          |          |          |          |         |          |
| 74 |       | GPE14    | PE14 [0] |          |          |          |          |          |         |          |
| 75 |       | GPE15    | PE15 [0] |          |          |          |          |          |         |          |
| 76 | Chip  | SWCLK    | PC4 [1]  |          |          |          |          |          |         |          |
| 77 |       | SWDIO    | PC5 [1]  |          |          |          |          |          |         |          |
| 78 |       | RSTN     | PC6 [1]  |          |          |          |          |          |         |          |
| 79 |       | ICKO     | PC0 [1]  |          |          |          |          |          |         |          |
| 80 |       | XIN      | PC13 [1] |          |          |          |          |          |         |          |
| 81 |       | XOUT     | PC14 [1] |          |          |          |          |          |         |          |
| 82 | ANAI0 | ADC0_TRG | PB2 [1]  | PC1 [1]  | PC7 [1]  | PE12 [1] |          |          |         |          |
| 83 |       | ADC0_OUT | PB3 [1]  | PC2 [1]  | PC8 [1]  | PE13 [1] |          |          |         |          |
| 84 |       | CMP0_P0  | PB8 [1]  | PC9 [1]  | PD12 [1] |          |          |          |         |          |
| 85 |       | CMP1_P0  | PB9 [1]  | PC10 [1] | PD13 [1] |          |          |          |         |          |
| 86 |       | DAC_TRG0 | PA11 [1] | PB13 [1] | PC12 [3] | PD14 [3] | PE0 [4]  |          |         |          |
| 87 | I2C0  | I2C0_SCL | PA8 [3]  | PB3 [7]  | PB10 [2] | PC0 [7]  | PC4 [2]  | PC8 [2]  | PD5 [2] | PE10 [1] |
| 88 |       | I2C0_SDA | PA10 [3] | PB2 [7]  | PB11 [2] | PC1 [7]  | PC5 [2]  | PC9 [2]  | PD6 [2] | PE11 [1] |
| 89 | I2C1  | I2C1_SCL | PA9 [3]  | PB0 [1]  | PC10 [2] | PE2 [2]  | PE10 [2] | PE14 [2] |         |          |

## MG32F02A128/A064

|     |         |           |           |           |           |           |           |           |          |          |
|-----|---------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|
| 90  |         | I2C1_SDA  | PA11 [3]  | PB1 [1]   | PC11 [2]  | PE3 [2]   | PE11 [2]  | PE15 [2]  |          |          |
| 91  | URT0    | URT0_TX   | PA4 [11]  | PB2 [10]  | PB8 [3]   | PC5 [3]   | PC10 [3]  | PE0 [3]   | PE10 [3] | PC0 [10] |
| 92  |         | URT0_RX   | PA5 [11]  | PB3 [10]  | PB9 [3]   | PC4 [3]   | PC11 [3]  | PE1 [3]   | PE11 [3] | PC1 [10] |
| 93  |         | URT0_CLK  | PA6 [11]  | PC0 [3]   | PC3 [3]   | PD0 [3]   | PD1 [3]   | PB11 [11] | PB13 [7] |          |
| 94  |         | URT0_NSS  | PA7 [11]  | PB10 [3]  | PC6 [3]   | PB14 [7]  |           |           |          |          |
| 95  |         | URT0_BRO  | PA13 [3]  | PB6 [3]   | PC8 [3]   |           |           |           |          |          |
| 96  |         | URT0_TMO  | PA14 [3]  | PB7 [3]   | PC9 [3]   |           |           |           |          |          |
| 97  |         | URT0_DE   | PA15 [3]  | PB11 [3]  | PC7 [3]   |           |           |           |          |          |
| 98  |         | URT0_CTS  | PB13 [3]  | PC13 [3]  |           |           |           |           |          |          |
| 99  |         | URT0_RTS  | PB14 [3]  | PC14 [3]  |           |           |           |           |          |          |
| 100 | URT1    | URT1_TX   | PB3 [9]   | PB10 [7]  | PC5 [4]   | PC8 [4]   | PC10 [5]  | PD4 [3]   | PE2 [3]  |          |
| 101 |         | URT1_RX   | PB1 [9]   | PB11 [7]  | PC4 [4]   | PC9 [4]   | PC11 [5]  | PD5 [3]   | PE3 [3]  |          |
| 102 |         | URT1_CLK  | PB2 [9]   | PB12 [7]  | PC1 [4]   | PC3 [4]   | PD2 [3]   | PD3 [3]   |          |          |
| 103 |         | URT1_NSS  | PB0 [9]   | PB15 [7]  | PC6 [4]   | PC7 [4]   | PC13 [2]  | PD6 [3]   |          |          |
| 104 |         | URT1_BRO  | PA12 [4]  | PD10 [3]  |           |           |           |           |          |          |
| 105 |         | URT1_TMO  | PA13 [4]  | PC14 [2]  | PD11 [3]  |           |           |           |          |          |
| 106 |         | URT1_DE   | PC12 [4]  | PD7 [3]   |           |           |           |           |          |          |
| 107 |         | URT1_CTS  | PA14 [4]  | PD9 [3]   |           |           |           |           |          |          |
| 108 |         | URT1_RTS  | PA15 [4]  | PD8 [3]   |           |           |           |           |          |          |
| 109 | URT2    | URT2_TX   | PB2 [4]   | PC10 [4]  | PC14 [4]  | PD2 [11]  | PD4 [11]  | PE8 [3]   | PB6 [11] |          |
| 110 |         | URT2_RX   | PB3 [4]   | PC11 [4]  | PC13 [4]  | PD3 [11]  | PD5 [11]  | PE9 [3]   | PB7 [11] |          |
| 111 |         | URT2_CLK  | PB4 [4]   | PC0 [4]   | PC2 [4]   | PD1 [11]  |           |           |          |          |
| 112 |         | URT2_NSS  | PB5 [4]   | PD0 [11]  | PD6 [11]  |           |           |           |          |          |
| 113 |         | URT2_BRO  | PA8 [4]   | PB8 [4]   |           |           |           |           |          |          |
| 114 |         | URT2_TMO  | PA9 [4]   | PB9 [4]   |           |           |           |           |          |          |
| 115 |         | URT2_DE   | PB10 [4]  |           |           |           |           |           |          |          |
| 116 |         | URT2_CTS  | PA10 [4]  | PB6 [4]   |           |           |           |           |          |          |
| 117 |         | URT2_RTS  | PA11 [4]  | PB7 [4]   |           |           |           |           |          |          |
| 118 | URT4567 | URT4_TX   | PA0 [11]  | PA8 [11]  | PB8 [11]  | PB14 [11] | PE0 [11]  | PE8 [11]  | PE10 [4] |          |
| 119 |         | URT4_RX   | PA1 [11]  | PA10 [11] | PB9 [11]  | PB13 [11] | PE1 [11]  | PE9 [11]  | PE11 [4] |          |
| 120 |         | URT5_TX   | PA2 [11]  | PA9 [11]  | PB12 [11] | PC0 [11]  | PD14 [11] | PE2 [11]  |          |          |
| 121 |         | URT5_RX   | PA3 [11]  | PA11 [11] | PB15 [11] | PC1 [11]  | PD15 [11] | PE3 [11]  |          |          |
| 122 |         | URT6_TX   | PA12 [11] | PB0 [11]  | PC5 [11]  | PC8 [11]  | PC14 [11] | PE12 [11] |          |          |
| 123 |         | URT6_RX   | PA13 [11] | PB1 [11]  | PC4 [11]  | PC9 [11]  | PC13 [11] | PE13 [11] |          |          |
| 124 |         | URT7_TX   | PA14 [11] | PB2 [11]  | PC10 [11] | PE14 [11] |           |           |          |          |
| 125 |         | URT7_RX   | PA15 [11] | PB3 [11]  | PC11 [11] | PE15 [11] |           |           |          |          |
| 126 | SPI0    | SPI0_CLK  | PB2 [2]   | PD12 [5]  | PE2 [5]   | PA10 [7]  | PD1 [7]   | PD8 [11]  |          |          |
| 127 |         | SPI0_MOSI | PB3 [2]   | PE3 [5]   | PA11 [7]  | PD2 [7]   | PD10 [11] |           |          |          |
| 128 |         | SPI0_MISO | PB1 [2]   | PD3 [5]   | PD7 [5]   | PE1 [5]   | PA9 [7]   | PD5 [7]   |          |          |
| 129 |         | SPI0_NSS  | PB0 [2]   | PD0 [7]   | PE0 [5]   | PA8 [7]   | PD6 [7]   | PD11 [7]  | PD9 [11] |          |
| 130 |         | SPI0_D2   | PA10 [2]  | PB5 [2]   | PB9 [7]   | PD8 [5]   | PA7 [7]   | PD4 [7]   |          |          |
| 131 |         | SPI0_D3   | PA11 [2]  | PB4 [2]   | PB8 [7]   | PD11 [5]  | PA6 [7]   | PD3 [7]   |          |          |
| 132 |         | SPI0_NSSI | PB6 [2]   | PB10 [10] | PD6 [5]   | PD9 [5]   |           |           |          |          |
| 133 |         | SPI0_D4   | PA15 [7]  | PD7 [7]   |           |           |           |           |          |          |
| 134 |         | SPI0_D5   | PA12 [7]  | PD10 [7]  |           |           |           |           |          |          |
| 135 |         | SPI0_D6   | PA13 [7]  | PD9 [7]   |           |           |           |           |          |          |
| 136 |         | SPI0_D7   | PA14 [7]  | PD8 [7]   |           |           |           |           |          |          |
| 137 | TM00    | TM00_CKO  | PB0 [4]   | PC0 [2]   | PD2 [2]   | PD7 [1]   | PD12 [4]  |           |          |          |

|     |      |           |           |          |           |          |          |  |  |  |
|-----|------|-----------|-----------|----------|-----------|----------|----------|--|--|--|
| 138 |      | TM00_TRGO | PB14 [2]  | PD4 [1]  | PD9 [2]   | PD13 [4] |          |  |  |  |
| 139 |      | TM00_ETR  | PB13 [2]  | PD5 [1]  | PD10 [2]  | PD14 [4] |          |  |  |  |
| 140 | TM01 | TM01_CKO  | PB2 [3]   | PB4 [1]  | PC1 [2]   | PD3 [2]  | PE12 [4] |  |  |  |
| 141 |      | TM01_TRGO | PB1 [3]   | PD4 [2]  | PD8 [2]   | PE13 [4] |          |  |  |  |
| 142 |      | TM01_ETR  | PB0 [3]   | PD7 [2]  | PE14 [4]  |          |          |  |  |  |
| 143 | TM10 | TM10_CKO  | PB1 [4]   | PC2 [2]  | PC14 [5]  | PD0 [2]  | PD12 [2] |  |  |  |
| 144 |      | TM10_TRGO | PA13 [5]  | PC12 [5] | PD13 [2]  |          |          |  |  |  |
| 145 |      | TM10_ETR  | PA12 [5]  | PC13 [5] | PD14 [2]  |          |          |  |  |  |
| 146 | TM16 | TM16_CKO  | PB2 [5]   | PB5 [1]  | PC3 [2]   | PD1 [2]  | PE12 [5] |  |  |  |
| 147 |      | TM16_TRGO | PA15 [5]  | PB1 [5]  | PE13 [5]  |          |          |  |  |  |
| 148 |      | TM16_ETR  | PA14 [5]  | PB0 [5]  | PE14 [5]  |          |          |  |  |  |
| 149 | TM20 | TM20_CKO  | PD0 [5]   | PD2 [5]  | PE8 [6]   |          |          |  |  |  |
| 150 |      | TM20_TRGO | PB7 [5]   | PB14 [5] | PE9 [6]   |          |          |  |  |  |
| 151 |      | TM20_ETR  | PB6 [5]   | PB13 [5] | PC6 [5]   |          |          |  |  |  |
| 152 |      | TM20_IC0  | PA8 [6]   | PB4 [5]  | PC13 [8]  | PD14 [6] |          |  |  |  |
| 153 |      | TM20_IC1  | PA9 [6]   | PB5 [5]  | PC14 [8]  | PD15 [6] |          |  |  |  |
| 154 |      | TM20_OC00 | PA4 [10]  | PC0 [5]  | PE0 [6]   |          |          |  |  |  |
| 155 |      | TM20_OC01 | PB8 [5]   | PE1 [6]  |           |          |          |  |  |  |
| 156 |      | TM20_OC02 | PB9 [5]   | PE2 [6]  |           |          |          |  |  |  |
| 157 |      | TM20_OC0N | PC1 [5]   | PE3 [6]  |           |          |          |  |  |  |
| 158 |      | TM20_OC10 | PA5 [10]  | PC2 [5]  | PE12 [6]  |          |          |  |  |  |
| 159 |      | TM20_OC11 | PB10 [5]  | PE13 [6] |           |          |          |  |  |  |
| 160 |      | TM20_OC12 | PB11 [5]  | PE14 [6] |           |          |          |  |  |  |
| 161 |      | TM20_OC1N | PC3 [5]   | PE15 [6] |           |          |          |  |  |  |
| 162 |      | TM20_OC0H | PA6 [10]  | PC8 [5]  | PD12 [6]  |          |          |  |  |  |
| 163 |      | TM20_OC1H | PA7 [10]  | PC9 [5]  | PD13 [6]  |          |          |  |  |  |
| 164 | TM26 | TM26_CKO  | PD1 [5]   | PD3 [6]  | PE8 [7]   |          |          |  |  |  |
| 165 |      | TM26_TRGO | PB4 [3]   | PC14 [6] | PE9 [7]   |          |          |  |  |  |
| 166 |      | TM26_ETR  | PB5 [3]   | PC6 [6]  | PC13 [6]  |          |          |  |  |  |
| 167 |      | TM26_IC0  | PA10 [6]  | PB0 [6]  | PD14 [7]  |          |          |  |  |  |
| 168 |      | TM26_IC1  | PA11 [6]  | PB1 [6]  | PD15 [7]  |          |          |  |  |  |
| 169 |      | TM26_OC00 | PA12 [10] | PD2 [4]  | PD4 [6]   | PE0 [7]  |          |  |  |  |
| 170 |      | TM26_OC01 | PC11 [7]  | PD5 [6]  | PE1 [7]   |          |          |  |  |  |
| 171 |      | TM26_OC02 | PC12 [7]  | PD6 [6]  | PE2 [7]   |          |          |  |  |  |
| 172 |      | TM26_OC0N | PD7 [6]   | PE3 [7]  |           |          |          |  |  |  |
| 173 |      | TM26_OC10 | PA13 [10] | PD8 [6]  | PE12 [7]  |          |          |  |  |  |
| 174 |      | TM26_OC11 | PD9 [6]   | PE13 [7] |           |          |          |  |  |  |
| 175 |      | TM26_OC12 | PD10 [6]  | PE14 [7] |           |          |          |  |  |  |
| 176 |      | TM26_OC1N | PD0 [4]   | PD11 [6] | PE15 [7]  |          |          |  |  |  |
| 177 |      | TM26_OC0H | PA14 [10] | PB2 [6]  | PD12 [7]  |          |          |  |  |  |
| 178 |      | TM26_OC1H | PA15 [10] | PB3 [6]  | PD13 [7]  |          |          |  |  |  |
| 179 | TM36 | TM36_CKO  | PB3 [5]   | PD2 [6]  | PE8 [5]   |          |          |  |  |  |
| 180 |      | TM36_TRGO | PB1 [7]   | PC7 [6]  | PD3 [10]  | PE9 [5]  |          |  |  |  |
| 181 |      | TM36_ETR  | PB0 [7]   | PB13 [6] | PE15 [5]  |          |          |  |  |  |
| 182 |      | TM36_IC0  | PA12 [6]  | PB4 [6]  | PD7 [10]  | PC1 [3]  |          |  |  |  |
| 183 |      | TM36_IC1  | PA13 [6]  | PB5 [6]  | PD8 [10]  |          |          |  |  |  |
| 184 |      | TM36_IC2  | PA14 [6]  | PB6 [6]  | PD9 [10]  |          |          |  |  |  |
| 185 |      | TM36_IC3  | PA15 [6]  | PB7 [6]  | PD10 [10] |          |          |  |  |  |

## MG32F02A128/A064

|     |     |           |           |          |           |          |          |  |  |  |
|-----|-----|-----------|-----------|----------|-----------|----------|----------|--|--|--|
| 186 |     | TM36_OC00 | PA0 [10]  | PC0 [6]  | PC13 [7]  |          |          |  |  |  |
| 187 |     | TM36_OC01 | PB8 [6]   |          |           |          |          |  |  |  |
| 188 |     | TM36_OC02 | PB9 [6]   |          |           |          |          |  |  |  |
| 189 |     | TM36_OC0N | PC1 [6]   | PC8 [7]  |           |          |          |  |  |  |
| 190 |     | TM36_OC10 | PA1 [10]  | PC2 [6]  | PC14 [7]  |          |          |  |  |  |
| 191 |     | TM36_OC11 | PB10 [6]  |          |           |          |          |  |  |  |
| 192 |     | TM36_OC12 | PB11 [6]  |          |           |          |          |  |  |  |
| 193 |     | TM36_OC1N | PC3 [6]   | PC9 [7]  |           |          |          |  |  |  |
| 194 |     | TM36_OC2  | PA2 [10]  | PC4 [6]  | PD0 [6]   |          |          |  |  |  |
| 195 |     | TM36_OC2N | PA3 [10]  | PD1 [6]  | PC10 [7]  |          |          |  |  |  |
| 196 |     | TM36_OC3  | PC5 [6]   | PC12 [6] |           |          |          |  |  |  |
| 197 |     | TM36_OC0H | PA8 [10]  | PC8 [6]  | PE1 [10]  |          |          |  |  |  |
| 198 |     | TM36_OC1H | PA9 [10]  | PC9 [6]  | PE2 [10]  |          |          |  |  |  |
| 199 |     | TM36_OC2H | PA10 [10] | PC10 [6] | PE13 [10] |          |          |  |  |  |
| 200 |     | TM36_OC3H | PA11 [10] | PC11 [6] | PE14 [10] |          |          |  |  |  |
| 201 |     | TM36_BK0  | PB14 [6]  | PA10 [1] | PE15 [4]  |          |          |  |  |  |
| 202 | RTC | RTC_OUT   | PB8 [2]   | PC7 [2]  | PD10 [5]  | PE14 [1] |          |  |  |  |
| 203 |     | RTC_TS    | PB9 [2]   | PC6 [2]  | PE15 [1]  |          |          |  |  |  |
| 204 | EMB | MAD0      | PB8 [8]   | PA0 [9]  | PA8 [9]   | PD7 [9]  |          |  |  |  |
| 205 |     | MAD1      | PB9 [8]   | PA1 [9]  | PA9 [9]   | PB10 [9] | PD10 [9] |  |  |  |
| 206 |     | MAD2      | PB10 [8]  | PA2 [9]  | PA10 [9]  | PB12 [9] | PD9 [9]  |  |  |  |
| 207 |     | MAD3      | PB11 [8]  | PA3 [9]  | PA11 [9]  | PB14 [9] | PD8 [9]  |  |  |  |
| 208 |     | MAD4      | PB12 [8]  | PA4 [9]  | PA12 [9]  | PC1 [9]  | PD2 [9]  |  |  |  |
| 209 |     | MAD5      | PB13 [8]  | PA5 [9]  | PA13 [9]  | PC3 [9]  | PD5 [9]  |  |  |  |
| 210 |     | MAD6      | PB14 [8]  | PA6 [9]  | PA14 [9]  | PC9 [9]  | PD4 [9]  |  |  |  |
| 211 |     | MAD7      | PB15 [8]  | PA7 [9]  | PA15 [9]  | PC11 [9] | PD3 [9]  |  |  |  |
| 212 |     | MAD8      | PC1 [8]   | PB4 [9]  | PB9 [9]   | PE0 [9]  |          |  |  |  |
| 213 |     | MAD9      | PC2 [8]   | PB5 [9]  | PB11 [9]  | PE1 [9]  |          |  |  |  |
| 214 |     | MAD10     | PC3 [8]   | PB6 [9]  | PB13 [9]  | PE2 [9]  |          |  |  |  |
| 215 |     | MAD11     | PC8 [8]   | PB15 [9] | PE8 [9]   |          |          |  |  |  |
| 216 |     | MAD12     | PC9 [8]   | PC2 [9]  |           |          |          |  |  |  |
| 217 |     | MAD13     | PC10 [8]  | PC8 [9]  |           |          |          |  |  |  |
| 218 |     | MAD14     | PC11 [8]  | PC10 [9] |           |          |          |  |  |  |
| 219 |     | MAD15     | PC12 [8]  |          |           |          |          |  |  |  |
| 220 |     | MWE       | PB6 [8]   | PE2 [8]  | PC0 [9]   | PD11 [9] |          |  |  |  |
| 221 |     | MOE       | PB5 [8]   | PE1 [8]  | PD14 [9]  | PE9 [9]  |          |  |  |  |
| 222 |     | MALE      | PB4 [8]   | PE0 [8]  | PE15 [8]  | PC6 [9]  |          |  |  |  |
| 223 |     | MCE       | PB7 [8]   | PE3 [8]  | PC7 [9]   | PD13 [9] |          |  |  |  |
| 224 |     | MCLK      | PC0 [8]   | PD0 [9]  |           |          |          |  |  |  |
| 225 |     | MBW0      | PC7 [8]   | PE12 [8] |           |          |          |  |  |  |
| 226 |     | MBW1      | PC6 [8]   | PE13 [8] |           |          |          |  |  |  |
| 227 |     | MALE2     | PE14 [8]  | PB7 [9]  | PD12 [9]  | PE3 [9]  |          |  |  |  |
| 228 |     | MA0       | PA0 [8]   | PD0 [8]  |           |          |          |  |  |  |
| 229 |     | MA1       | PA1 [8]   | PD1 [8]  |           |          |          |  |  |  |
| 230 |     | MA2       | PA2 [8]   | PD2 [8]  |           |          |          |  |  |  |
| 231 |     | MA3       | PA3 [8]   | PD3 [8]  |           |          |          |  |  |  |
| 232 |     | MA4       | PA4 [8]   | PD4 [8]  |           |          |          |  |  |  |
| 233 |     | MA5       | PA5 [8]   | PD5 [8]  |           |          |          |  |  |  |

|     |       |          |           |           |          |           |          |          |          |  |
|-----|-------|----------|-----------|-----------|----------|-----------|----------|----------|----------|--|
| 234 |       | MA6      | PA6 [8]   | PD6 [8]   |          |           |          |          |          |  |
| 235 |       | MA7      | PA7 [8]   | PD7 [8]   |          |           |          |          |          |  |
| 236 |       | MA8      | PA8 [8]   | PD8 [8]   |          |           |          |          |          |  |
| 237 |       | MA9      | PA9 [8]   | PD9 [8]   |          |           |          |          |          |  |
| 238 |       | MA10     | PA10 [8]  | PD10 [8]  |          |           |          |          |          |  |
| 239 |       | MA11     | PA11 [8]  | PD11 [8]  |          |           |          |          |          |  |
| 240 |       | MA12     | PA12 [8]  | PD12 [8]  |          |           |          |          |          |  |
| 241 |       | MA13     | PA13 [8]  | PD13 [8]  |          |           |          |          |          |  |
| 242 |       | MA14     | PA14 [8]  | PD14 [8]  |          |           |          |          |          |  |
| 243 |       | MA15     | PA15 [8]  | PB0 [8]   | PD15 [8] |           |          |          |          |  |
| 244 | Other | CPU_TXEV | PA13 [1]  | PB7 [1]   | PD8 [1]  | PE8 [1]   |          |          |          |  |
| 245 |       | CPU_RXEV | PA14 [1]  | PB6 [1]   | PD9 [1]  | PE9 [1]   |          |          |          |  |
| 246 |       | CPU_NMI  | PA15 [1]  | PD6 [1]   | PD10 [1] | PD11 [1]  |          |          |          |  |
| 247 |       | IR_OUT   | PB11 [4]  | PB15 [1]  | PC12 [2] | PD15 [3]  |          |          |          |  |
| 248 |       | OBM_I0   | PA14 [2]  | PD0 [1]   | PE0 [1]  | PE8 [2]   |          |          |          |  |
| 249 |       | OBM_I1   | PA15 [2]  | PD1 [1]   | PE1 [1]  | PE9 [2]   |          |          |          |  |
| 250 |       | OBM_P0   | PB8 [10]  | PC2 [3]   | PD12 [3] | PE2 [1]   |          |          |          |  |
| 251 |       | OBM_P1   | PB9 [10]  | PC3 [1]   | PD13 [3] | PE3 [1]   |          |          |          |  |
| 252 |       |          |           |           |          |           |          |          |          |  |
| 253 |       |          |           |           |          |           |          |          |          |  |
| 254 |       | CCL_P0   | PA0 [7]   | PB13 [10] | PC8 [10] | PD14 [10] | PE14 [9] |          |          |  |
| 255 |       | CCL_P1   | PA1 [7]   | PB14 [10] | PC9 [10] | PD15 [10] | PE15 [9] |          |          |  |
| 256 |       | DMA_TRG0 | PA8 [1]   | PB11 [10] | PB12 [1] | PB14 [1]  | PD15 [4] |          |          |  |
| 257 |       | DMA_TRG1 | PA9 [1]   | PD11 [2]  | PE1 [4]  |           |          |          |          |  |
| 258 |       | SDT_I0   | PA2 [6]   | PC2 [7]   | PC4 [7]  | PC13 [9]  | PE8 [4]  | PE10 [9] | PA8 [5]  |  |
| 259 |       | SDT_I1   | PA3 [6]   | PC3 [7]   | PC5 [7]  | PC14 [9]  | PE9 [4]  | PE11 [9] | PA10 [5] |  |
| 260 |       | SDT_P0   | PA0 [6]   | PB8 [9]   | PC12 [9] | PD6 [9]   |          |          |          |  |
| 261 |       | NCO_P0   | PB3 [3]   | PB12 [2]  | PD15 [2] | PE2 [4]   |          |          |          |  |
| 262 |       | NCO_CK0  | PB15 [2]  | PD1 [4]   | PD13 [5] | PE3 [4]   |          |          |          |  |
| 263 | AADC  | ADC_I0   | PA0 [17]  |           |          |           |          |          |          |  |
| 264 |       | ADC_I1   | PA1 [17]  |           |          |           |          |          |          |  |
| 265 |       | ADC_I2   | PA2 [17]  |           |          |           |          |          |          |  |
| 266 |       | ADC_I3   | PA3 [17]  |           |          |           |          |          |          |  |
| 267 |       | ADC_I4   | PA4 [17]  |           |          |           |          |          |          |  |
| 268 |       | ADC_I5   | PA5 [17]  |           |          |           |          |          |          |  |
| 269 |       | ADC_I6   | PA6 [17]  |           |          |           |          |          |          |  |
| 270 |       | ADC_I7   | PA7 [17]  |           |          |           |          |          |          |  |
| 271 |       | ADC_I8   | PA8 [17]  |           |          |           |          |          |          |  |
| 272 |       | ADC_I9   | PA9 [17]  |           |          |           |          |          |          |  |
| 273 |       | ADC_I10  | PA10 [17] |           |          |           |          |          |          |  |
| 274 |       | ADC_I11  | PA11 [17] |           |          |           |          |          |          |  |
| 275 |       | ADC_I12  | PA12 [17] |           |          |           |          |          |          |  |
| 276 |       | ADC_I13  | PA13 [17] |           |          |           |          |          |          |  |
| 277 |       | ADC_I14  | PA14 [17] |           |          |           |          |          |          |  |
| 278 |       | ADC_I15  | PA15 [17] |           |          |           |          |          |          |  |
| 279 | ACMP  | CMP_C0   | PB0 [18]  |           |          |           |          |          |          |  |
| 280 |       | CMP_C1   | PB1 [18]  |           |          |           |          |          |          |  |
| 281 |       | CMP0_I0  | PA8 [18]  |           |          |           |          |          |          |  |

## MG32F02A128/A064

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|     |     |         |           |  |  |  |  |  |  |  |
|-----|-----|---------|-----------|--|--|--|--|--|--|--|
| 282 |     | CMP0_I1 | PA9 [18]  |  |  |  |  |  |  |  |
| 283 |     | CMP1_I0 | PA10 [18] |  |  |  |  |  |  |  |
| 284 |     | CMP1_I1 | PA11 [18] |  |  |  |  |  |  |  |
| 285 | ANA | DAC_P0  | PB2 [19]  |  |  |  |  |  |  |  |
| 286 |     | ADC_PGA | PA10 [19] |  |  |  |  |  |  |  |
| 287 |     | VBG_OUT | PA8 [19]  |  |  |  |  |  |  |  |

## 5. Memory Map

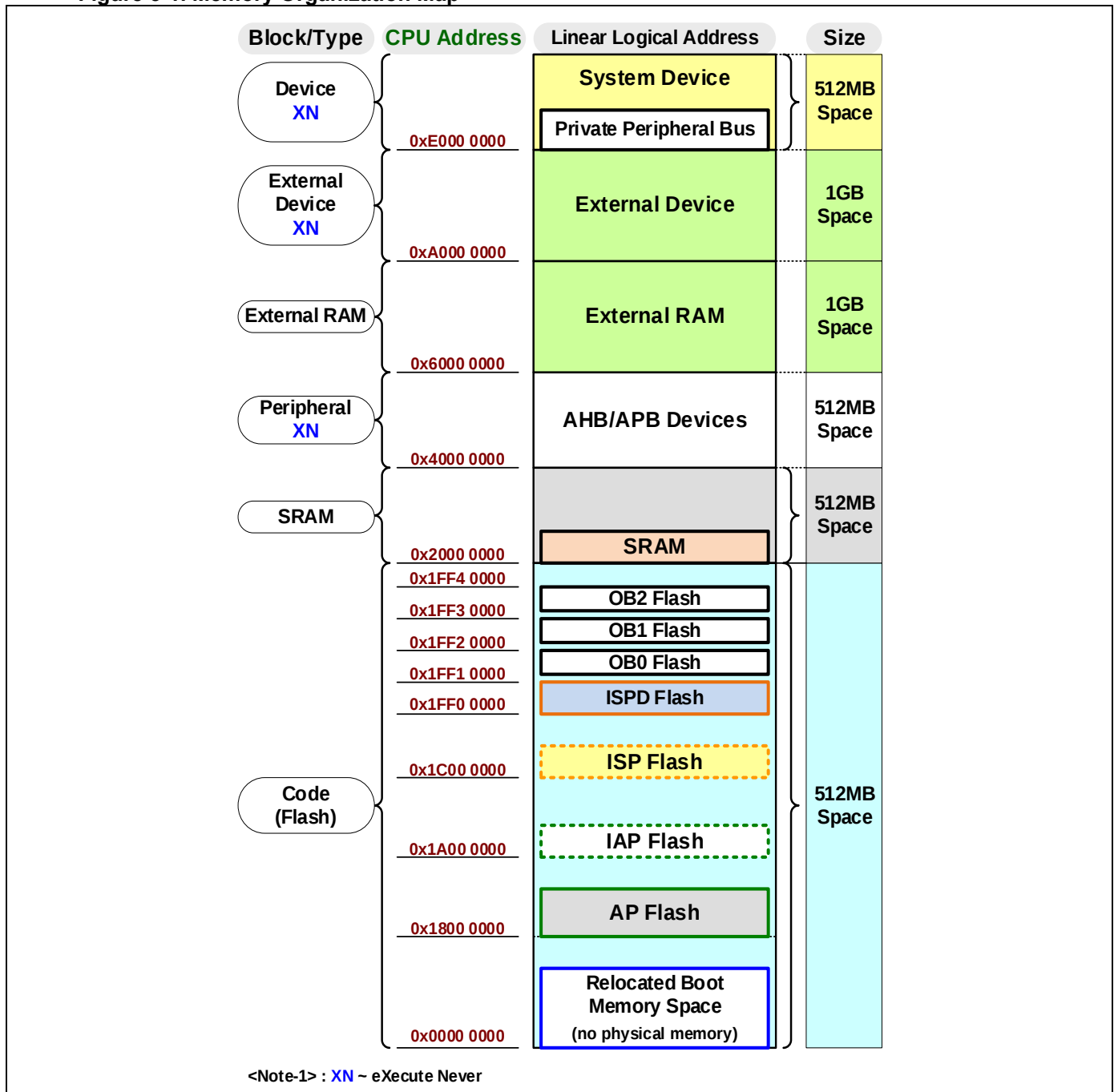
### 5.1. Memory Organization

There are up to **16K** bytes of SRAM built in the chip. The chip has up to **128K** bytes of embedded main flash memory for code and data, programmable memory size of embedded system flash memory for boot load code and 64 bytes of embedded option-byte (**OB**) flash memory for chip configuration. Others, there are many module independent hardware control registers and locate at the memory space of AHB/APB devices.

User can configure the whole flash to store for his Application Program (AP) code, In-System-Program (ISP) code and In-Application-Program (IAP) memory. User can adjust the size for the three flash memories.

The following diagram is showing the memory organization map. There are separated eight memory blocks and the memory size is 512M-byte for each block. The block is signed “XN” which is not able to execute code.

Figure 5-1. Memory Organization Map



## 5.2. CPU Memory Map

The following table is showing the memory address map of CPU. The block is signed “XN” which is not able to execute code.

**Table 5-1. CPU Memory Address Map**

| Block Index | Block Name      | XN | Boundary address |             | Size  | Address Space               | Note                                                        |
|-------------|-----------------|----|------------------|-------------|-------|-----------------------------|-------------------------------------------------------------|
|             |                 |    | Start address    | End address |       |                             |                                                             |
| 7           | System Device   | XN | 0xE010 0000      | 0xFFFF FFFF | 511MB | VENDOR_SYS                  |                                                             |
|             |                 |    | 0xE000 0000      | 0xE00F FFFF | 1MB   | Private Peripheral Bus(PPB) | M0 Reserved Cortex M0 internal peripherals                  |
| 6           | External Device | XN | 0xC000 0000      | 0xDFFF FFFF | 512MB | Reserved                    | External memory (SRAM, Flash)                               |
| 5           | External Device | XN | 0xA000 0000      | 0xBFFF FFFF | 512MB | Reserved                    | External memory (SRAM, Flash)                               |
| 4           | External RAM    |    | 0x8000 0000      | 0x9FFF FFFF | 512MB | Reserved                    | External memory (SRAM, Flash)                               |
| 3           | External RAM    |    | 0x6000 0000      | 0x7FFF FFFF | 512MB | Reserved                    | External memory (SRAM, Flash)                               |
| 2           | Peripheral      | XN | 0x4000 0000      | 0x5FFF FFFF | 512MB | APB/AHB                     | APB/AHB modules                                             |
| 1           | SRAM            |    | 0x3000 0200      | 0x3FFF FFFF | 256MB | Reserved                    |                                                             |
|             |                 |    | 0x3000 0000      | 0x3000 01FF | 512B  | Reserved                    |                                                             |
|             |                 |    | 0x2000 4000      | 0x2FFF FFFF | 256MB | Reserved                    |                                                             |
|             |                 |    | 0x2000 3800      | 0x2000 3FFF | 2KB   | SRAM                        | Upper 2K-byte suggestion for DMA                            |
|             |                 |    | 0x2000 0000      | 0x2000 37FF | 14KB  | SRAM                        | 14/8KB for flash size 128/64KB chip                         |
| 0           | Code            |    | 0x1FF3 0200      | 0x1FFF FFFF | 832KB | Reserved                    |                                                             |
|             |                 |    | 0x1FF3 0040      | 0x1FF3 01FF | 448B  | OB Flash-2                  |                                                             |
|             |                 |    | 0x1FF3 0000      | 0x1FF3 003F | 64B   |                             | Hardware Option byte-2 (64-byte)                            |
|             |                 |    | 0x1FF2 0200      | 0x1FF2 FFFF | 64KB  | Reserved                    |                                                             |
|             |                 |    | 0x1FF2 0050      | 0x1FF2 01FF | 432B  | OB Flash-1                  |                                                             |
|             |                 |    | 0x1FF2 0040      | 0x1FF2 004F | 16B   |                             | Unique ID (16-byte)                                         |
|             |                 |    | 0x1FF2 0000      | 0x1FF2 003F | 64B   |                             | Hardware Option byte-1 (64-byte)                            |
|             |                 |    | 0x1FF1 0200      | 0x1FF1 FFFF | 64KB  | Reserved                    |                                                             |
|             |                 |    | 0x1FF1 0040      | 0x1FF1 01FF | 448B  | OB Flash-0                  |                                                             |
|             |                 |    | 0x1FF1 0000      | 0x1FF1 003F | 64B   |                             | Hardware Option byte-0 (64-byte)                            |
|             |                 |    | 0x1FF0 0200      | 0x1FF0 FFFF | 64KB  | Reserved                    |                                                             |
|             |                 |    | 0x1FF0 0000      | 0x1FF0 01FF | 512B  | ISPD Flash                  | ISP data flash                                              |
|             |                 |    | 0x1C02 0000      | 0x1FEF FFFF | 63MB  | Reserved                    |                                                             |
|             |                 |    | 0x1C00 0000      | 0x1C01 FFFF | 128KB | ISP Flash                   | Boot Flash memory (configurable size)                       |
|             |                 |    | 0x1A02 0000      | 0x1BFF FFFF | 32MB  | Reserved                    |                                                             |
|             |                 |    | 0x1A00 0000      | 0x1A01 FFFF | 128KB | IAP Flash                   | Data Flash memory (configurable size)                       |
|             |                 |    | 0x1802 0000      | 0x19FF FFFF | 32MB  | Reserved                    |                                                             |
|             |                 |    | 0x1800 0000      | 0x1801 FFFF | 128KB | AP Flash                    | Application Flash memory (configurable size by chip option) |
|             |                 |    | 0x0002 0000      | 0x17FF FFFF | 384MB | Reserved                    |                                                             |
|             |                 |    | 0x0000 0000      | 0x0001 FFFF | 128KB | Relocated memory space      | Interrupt Vector<br>0x0000 00C0~0x0000 0000                 |

XN : eXecute Never , 1 Block = 512MB

Relocated memory space : Main flash memory, Boot flash memory or SRAM depending on BOOT configuration

### 5.3. Peripheral Memory Boundary

Table 5-2. Peripheral Memory Boundary Address

| Address Type | Boundary address |             | Size  | Sections / Groups Peripheral | Module      | Note                                |
|--------------|------------------|-------------|-------|------------------------------|-------------|-------------------------------------|
|              | Start address    | End address |       |                              |             |                                     |
| APB          | 0x5F01 0100      | 0x5FFF FFFF | 16MB  | APB                          | Reserved    |                                     |
|              | 0x5F01 0000      | 0x5F01 00FF | 256B  |                              | <b>APX</b>  | APB module extended control         |
|              | 0x5F00 0100      | 0x5F00 FFFF | 64KB  |                              | Reserved    |                                     |
|              | 0x5F00 0000      | 0x5F00 00FF | 256B  |                              | <b>APB</b>  | APB module global control           |
|              | 0x5E00 0000      | 0x5EFF FFFF | 16MB  | Reserved                     | Reserved    |                                     |
|              | 0x5D04 0100      | 0x5DFF FFFF | 16MB  | WDT/RTC                      | Reserved    |                                     |
|              | 0x5D04 0000      | 0x5D04 00FF | 256B  |                              | <b>RTC</b>  | Real Time Clock                     |
|              | 0x5D01 0100      | 0x5D03 FFFF | 192KB |                              | Reserved    |                                     |
|              | 0x5D01 0000      | 0x5D01 00FF | 256B  |                              | <b>WWDT</b> | Window WatchDog Timer               |
|              | 0x5D00 0100      | 0x5D00 FFFF | 64KB  |                              | Reserved    |                                     |
|              | 0x5D00 0000      | 0x5D00 00FF | 256B  |                              | <b>IWDT</b> | Independent WatchDog Timer          |
|              | 0x5C08 0100      | 0x5CFF FFFF | 15MB  | CMP/DAC                      | Reserved    |                                     |
|              | 0x5C08 0000      | 0x5C08 00FF | 256B  |                              | <b>DAC</b>  | Digital-to-Analog controller        |
|              | 0x5C00 0100      | 0x5C07 FFFF | 512KB |                              | Reserved    |                                     |
|              | 0x5C00 0000      | 0x5C00 00FF | 256B  |                              | <b>CMP</b>  | Analog Comparator 0,1               |
|              | 0x5B00 0100      | 0x5BFF FFFF | 16MB  | ADC                          | Reserved    |                                     |
|              | 0x5B00 0000      | 0x5B00 00FF | 256B  |                              | <b>ADC</b>  | Analog-to-Digital controller        |
|              | 0x5700 0000      | 0x5AFF FFFF | 64MB  | Reserved                     | Reserved    |                                     |
|              | 0x5686 0100      | 0x56FF FFFF | 8MB   | TM2x/3x                      | Reserved    |                                     |
|              | 0x5686 0000      | 0x5686 00FF | 256B  |                              | <b>TM36</b> | 32-bit Timer with 4 IC/OC/PWM       |
|              | 0x5606 0100      | 0x5685 FFFF | 8MB   |                              | Reserved    |                                     |
|              | 0x5606 0000      | 0x5606 00FF | 256B  |                              | <b>TM26</b> | 32-bit Timer with 2 IC/OC/PWM       |
|              | 0x5600 0100      | 0x5605 FFFF | 384KB |                              | Reserved    |                                     |
|              | 0x5600 0000      | 0x5600 00FF | 256B  |                              | <b>TM20</b> | 32-bit Timer with 2 IC/OC/PWM       |
|              | 0x5586 0100      | 0x55FF FFFF | 8MB   | TM0x/1x                      | Reserved    |                                     |
|              | 0x5586 0000      | 0x5586 00FF | 256B  |                              | <b>TM16</b> | Basic32-bit Timer/Counter           |
|              | 0x5580 0100      | 0x5585 FFFF | 384KB |                              | Reserved    |                                     |
|              | 0x5580 0000      | 0x5580 00FF | 256B  |                              | <b>TM10</b> | Basic32-bit Timer/Counter           |
|              | 0x5501 0100      | 0x557F FFFF | 8MB   |                              | Reserved    |                                     |
|              | 0x5501 0000      | 0x5501 00FF | 256B  |                              | <b>TM01</b> | Basic 16-bit Timer/Counter          |
|              | 0x5500 0100      | 0x5500 FFFF | 64KB  |                              | Reserved    |                                     |
|              | 0x5500 0000      | 0x5500 00FF | 256B  |                              | <b>TM00</b> | Basic 16-bit Timer/Counter          |
|              | 0x5401 0000      | 0x54FF FFFF | 16MB  | Reserved                     | Reserved    |                                     |
|              | 0x5400 0100      | 0x5400 FFFF | 64KB  | Reserved                     | Reserved    |                                     |
|              | 0x5400 0000      | 0x5400 00FF | 256B  |                              | Reserved    |                                     |
|              | 0x5300 0100      | 0x53FF FFFF | 16MB  | SPI                          | Reserved    |                                     |
|              | 0x5300 0000      | 0x5300 00FF | 256B  |                              | <b>SPI0</b> | SPI bus controller with data buffer |
|              | 0x5207 0100      | 0x52FF FFFF | 16MB  | UART                         | Reserved    |                                     |
|              | 0x5207 0000      | 0x5207 00FF | 256B  |                              | <b>URT7</b> | Basic UART bus controller           |
|              | 0x5206 0100      | 0x5206 FFFF | 64KB  |                              | Reserved    |                                     |
|              | 0x5206 0000      | 0x5206 00FF | 256B  |                              | <b>URT6</b> | Basic UART bus controller           |
|              | 0x5205 0100      | 0x5205 FFFF | 64KB  |                              | Reserved    |                                     |
|              | 0x5205 0000      | 0x5205 00FF | 256B  |                              | <b>URT5</b> | Basic UART bus controller           |
|              | 0x5204 0100      | 0x5204 FFFF | 64KB  |                              | Reserved    |                                     |
|              | 0x5204 0000      | 0x5204 00FF | 256B  |                              | <b>URT4</b> | Basic UART bus controller           |
|              | 0x5202 0100      | 0x5203 FFFF | 128KB |                              | Reserved    |                                     |
|              | 0x5202 0000      | 0x5202 00FF | 256B  |                              | <b>URT2</b> | Advance UART bus controller         |
|              | 0x5201 0100      | 0x5201 FFFF | 64KB  |                              | Reserved    |                                     |
|              | 0x5201 0000      | 0x5201 00FF | 256B  |                              | <b>URT1</b> | Advance UART bus controller         |
|              | 0x5200 0100      | 0x5200 FFFF | 64KB  |                              | Reserved    |                                     |

## MG32F02A128/A064

|     |             |             |        |                 |             |                                |
|-----|-------------|-------------|--------|-----------------|-------------|--------------------------------|
|     | 0x5200 0000 | 0x5200 00FF | 256B   |                 | <b>URT0</b> | Advance UART bus controller    |
|     | 0x5101 0100 | 0x51FF FFFF | 16MB   | I2C             | Reserved    |                                |
|     | 0x5101 0000 | 0x5101 00FF | 256B   |                 | <b>I2C1</b> | I2C bus controller             |
|     | 0x5100 0100 | 0x5100 FFFF | 64KB   |                 | Reserved    |                                |
|     | 0x5100 0000 | 0x5100 00FF | 256B   |                 | <b>I2C0</b> | I2C bus controller             |
|     | 0x5000 0100 | 0x50FF FFFF | 16MB   | EXT Interrupt   | Reserved    |                                |
|     | 0x5000 0000 | 0x5000 00FF | 256B   |                 | <b>EXIC</b> | External Interrupt Controller  |
| AHB | 0x4FF0 0100 | 0x4FFF FFFF | 1024KB | Chip            | Reserved    |                                |
|     | 0x4FF0 0000 | 0x4FF0 00FF | 256B   |                 | <b>CFG</b>  | Hardware option (NVR0/1/2)     |
|     | 0x4F00 0100 | 0x4FEF FFFF | 15MB   |                 | Reserved    |                                |
|     | 0x4F00 0000 | 0x4F00 00FF | 256B   |                 | <b>WRI</b>  | Writer Interface Control       |
|     | 0x4E00 0000 | 0x4EFF FFFF | 16MB   | Reserved        | Reserved    |                                |
|     | 0x4D02 0100 | 0x4DFF FFFF | 16MB   | Memory          | Reserved    |                                |
|     | 0x4D02 0000 | 0x4D02 00FF | 256B   |                 | <b>EMB</b>  | External Memory Bus Controller |
|     | 0x4D00 0100 | 0x4D01 FFFF | 128KB  |                 | Reserved    |                                |
|     | 0x4D00 0000 | 0x4D00 00FF | 256B   |                 | <b>MEM</b>  | Internal Memory Controller     |
|     | 0x4C03 0100 | 0x4CFF FFFF | 16MB   | System          | Reserved    |                                |
|     | 0x4C03 0000 | 0x4C03 00FF | 256B   |                 | <b>SYS</b>  | System and Chip Control        |
|     | 0x4C02 0100 | 0x4C02 FFFF | 64KB   |                 | Reserved    |                                |
|     | 0x4C02 0000 | 0x4C02 00FF | 256B   |                 | <b>PW</b>   | Power Management Controller    |
|     | 0x4C01 0100 | 0x4C01 FFFF | 64KB   |                 | Reserved    |                                |
|     | 0x4C01 0000 | 0x4C01 00FF | 256B   |                 | <b>CSC</b>  | Clock Source Controller        |
|     | 0x4C00 0100 | 0x4C00 FFFF | 64KB   |                 | Reserved    |                                |
|     | 0x4C00 0000 | 0x4C00 00FF | 256B   |                 | <b>RST</b>  | Reset Source Controller        |
|     | 0x4BF0 0100 | 0x4BFF FFFF | 1024KB | General Purpose | Reserved    |                                |
|     | 0x4BF0 0000 | 0x4BF0 00FF | 256B   |                 | <b>DMA</b>  | Direct memory access           |
|     | 0x4B00 0100 | 0x4BEF FFFF | 15MB   |                 | Reserved    |                                |
|     | 0x4B00 0000 | 0x4B00 00FF | 256B   |                 | <b>GPL</b>  | General Purpose Logic          |
|     | 0x4500 0000 | 0x4AFF FFFF | 96MB   | Reserved        | Reserved    | Reserved for future design     |
|     | 0x4404 0100 | 0x44FF FFFF | 16MB   | IO Configure    | Reserved    |                                |
|     | 0x4404 0000 | 0x4404 00FF | 256B   |                 | <b>PE</b>   |                                |
|     | 0x4403 0100 | 0x4403 FFFF | 64KB   |                 | Reserved    |                                |
|     | 0x4403 0000 | 0x4403 00FF | 256B   |                 | <b>PD</b>   |                                |
|     | 0x4402 0100 | 0x4402 FFFF | 64KB   |                 | Reserved    |                                |
|     | 0x4402 0000 | 0x4402 00FF | 256B   |                 | <b>PC</b>   |                                |
|     | 0x4401 0100 | 0x4401 FFFF | 64KB   |                 | Reserved    |                                |
|     | 0x4401 0000 | 0x4401 00FF | 256B   |                 | <b>PB</b>   |                                |
|     | 0x4400 0100 | 0x4400 FFFF | 64KB   |                 | Reserved    |                                |
|     | 0x4400 0000 | 0x4400 00FF | 256B   |                 | <b>PA</b>   |                                |
|     | 0x4100 0200 | 0x43FF FFFF | 48MB   | Reserved        |             | Reserved for future design     |
|     | 0x4100 0000 | 0x4100 01FF | 512B   | GPIO            | <b>IOP</b>  | IO Port Input/Output           |
|     | 0x4000 0000 | 0x40FF FFFF | 16MB   | Reserved        |             | Reserved for future design     |

### 5.4. Boot Modes

During chip startup, the hardware configuration option-byte (**OB**) is used to select one of the three boot options:

- **Boot from User Application Program (AP) Flash**
- **Boot from In-System-Program (ISP)**
- **Boot from embedded SRAM**

## 6. Functional Description

### 6.1. CPU Core

#### 6.1.1. Introduction

The chip is embedded a CPU core of Cortex®-M0 processor. The processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional DAP hardware debug functionality.

The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

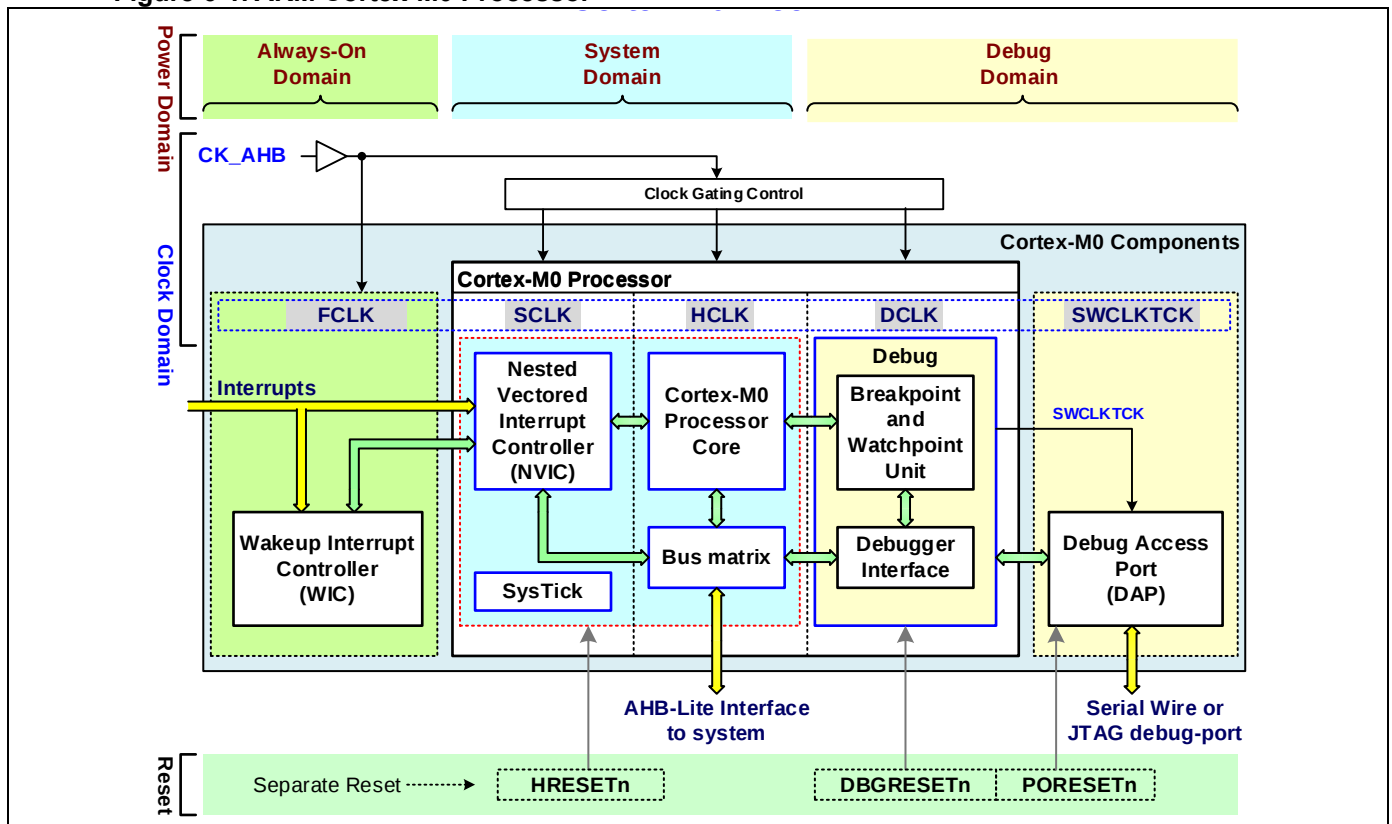
#### 6.1.2. CPU Features

- **ARM® 32-bit Cortex®-M0 CPU**
- **Operation frequency up to 48MHz**
- **Built-in one NVIC for 32 external interrupt inputs with 4-level priority**
- **Built-in one 24-bit system tick timer**
- **Built-in one single-cycle 32-bit multiplier**
- **Built-in one SWD serial wire debugger with 2 watch points and 4 breakpoint**
- **The ARMv6-M Thumb® instruction set**

#### 6.1.3. ARM Cortex-M0 Processor

The following diagram is showing the block of ARM® Cortex®-M0 Processor.

**Figure 6-1. ARM Cortex-M0 Processor**



## 6.2. Power Management

### 6.2.1. Introduction

The chip power is implemented only by single power supply input and embedded one LDO to supply the internal core logic power. The chip supports one power controller (PW) to manage Power-on reset (POR) circuit, Low-voltage reset (LVR) circuit, Brown-Out Detectors (BOD0/1/2), power down control and wakeup control.

It supports power-down modes: **SLEEP** mode and **STOP** modes. The power-down modes reduce chip power and provide the different power-saving scheme for chip application.

### 6.2.2. Chip Power Features

- Built-in one embedded regulator for core logic power
- Built-in brown-out detectors
  - BOD0 detect 1.4V
  - BOD1 detect by selected level 4.2V/3.7V/2.4V/2.0V
  - BOD2 detect 1.7V
- Built-in a power management controller with power-down and wakeup control
- Support three power operation modes
  - ON(Normal) mode and SLEEP , STOP power down modes
- Support wake-up from SLEEP/STOP modes via multiple sources

### 6.2.3. Power Operation Mode

There are three power operation modes of **ON**, **SLEEP**, **STOP** to be supported in the power controller.

- **ON mode**

In **ON** mode, the CPU is able running in full speed. All peripheral modules can use full power to do normally full function operation. These modules can enable or disable independent to save current consumption.

- **SLEEP mode**

In **SLEEP** mode, only the CPU is stopped and entering CPU sleep mode. All peripheral modules can be configurable to continue to operate or sleep.

In this mode, the chip can be waked up by the related interrupt or event occurs.

- **STOP mode**

The **STOP** mode provides the lowest current consumption. The different from SLEEP mode is that CPU is entering CPU deep-sleep mode and all peripheral modules are disabled except some special modules or devices. These modules or devices can be configurable to continue to operate in STOP mode or not. They include of IWDG, RTC, CMP modules and LVR, BOD0, BOD1, BOD2 devices. The internal voltage regulator is also running in low power mode.

In this mode, the chip can be waked up by some of the external input lines (GPIO) and some events detection.

### 6.2.4. Power Supply

The chip power is implemented only by single power supply input for easy application PCB design. It is embedded one internal low dropout linear regulator (LDO) to generate the +1.5 volt voltage power VDDC for core logic power supply.

The **VDD** pin(s) is/are using for IO power supply input and internal LDO input. The **VSS** pin(s) is/are used to connect the external ground for internal reference ground of internal LDO, hard macros and digital logic. The **VR0** pin is the LDO output and it needs to connect bypass capacitors for normal operation. The **+VREFF** pin is the input of ADC reference voltage which can connect to **VDD** pin for general application.

### 6.2.5. CPU Power Down

For chip entering power down mode, the firmware must execute WFI or WFE instruction to force the CPU enters sleep mode or deep sleep mode. Then the chip will enter the power down mode of **SLEEP** or **STOP**. User can configure the CPU sleep mode by setting CPU register of SLEEPDEEP after firmware executes WFI or WFE instruction.

**Table 6-1. Power-Down Mode Selection**

| CPU        | System | CPU Register |
|------------|--------|--------------|
|            |        | SLEEPDEEP    |
| Run        | ON     | x            |
| sleep      | SLEEP  | 0            |
| deep sleep | STOP   | 1            |

## 6.3. System Reset

### 6.3.1. Introduction

During reset, all Registers are set to their initial values, and the program starts execution from the Reset Vector. The chip includes a reset source controller (RST) to manage multiple sources of reset and generates Warm reset and Cold reset signals to chip system and internal modules. This controller also provides the reset event flags for firmware, which are used to recognize the reset occurred source.

### 6.3.2. Chip Reset Features

- **Built-in embedded POR(power-on reset)/LVR(low-voltage reset) circuit**
- **Built-in one reset source controller**
  - Programmable chip cold reset and warm reset for reset source
  - Independent software reset control for internal modules
- **Provide multiple reset sources**
  - POR/LVR/BOD/External reset pin input/Software force reset
  - IWD/WWDT/ADC/Comparator
  - IAR(Illegal address error reset)/Flash access protect error reset
  - Missing clock detect (MCD) reset

### 6.3.3. Chip Reset Levels

The chip provides three reset levels – POR reset, Cold reset and Warm reset. POR reset is the highest priority reset and is generated by chip hardware. Cold reset is the 2<sup>nd</sup> priority and Warm reset is the lowest priority reset.

When POR reset occurred, it will cause to generate Cold reset to chip. Also when Cold reset occurred, it will cause to generate Warm reset to chip.

#### ● **Power-On Reset**

Power-on reset (**POR**) is used to internally reset the chip and also the CPU during power-up. The chip will keep in reset state and will not start to work until the VDD power rises above the voltage of Power-On Reset. And, the reset state is activated again whenever the VDD power falls below the POR threshold voltage. During a power off cycle, VDD must fall below the POR threshold voltage before power is reapplied in order to ensure a power-on reset.

#### ● **Cold Reset**

Cold reset is the 2<sup>nd</sup> priority reset. The Cold reset is also generated and caused by POR reset occurred. It sends to some modules like as IWD/WWDT ... to do deep level module reset. It will cause to reload all hardware configurations **OB** and disable the register lock function for the modules which are support the register lock function.

#### ● **Warm Reset**

Warm reset is the lowest priority reset. The Warm reset is also generated and caused by Cold reset occurred. It sends to all modules to clear flags and hardware circuit. It will cause to reload some hardware configuration **OB** and reset the registers of module to default value if the module is unlocked or not supported lock function. It will clear Warm reset source enable bits in RST controller if the RST controller is unlocked.

### 6.3.4. External Reset

The chip provides an external hardware reset input from **RSTN** pin, which is accomplished by holding low level for the **RSTN** pin. The **RSTN** pin is configured to as external reset pin or others (GPIO ...) by hardware configuration **OB**. To ensure a reliable power-up reset, then the hardware reset from **RSTN** pin is necessary.

### 6.3.5. Module Reset

For each AHB or APB control module, it can receive the system Warm reset signal to reset the module's control flags, registers and logical circuit. For some modules of IWDT, WWDT, RTC, PW, CSC and MEM, they can receive the Cold reset to unlock the register locked function and reset the module.

## 6.4. System Clock

### 6.4.1. Introduction

The chip builds in a clock source controller (CSC) for system clock source management. There are four clock sources for the system application: Internal High-frequency RC Oscillator (**IHRCO**), Internal crystal oscillator (**XOSC**), Internal Low-frequency RC Oscillator (**ILRCO**) and External Clock Input (**EXTCK**).

One **XOSC** oscillator is embedded for external Xtal circuit. One PLL is embedded to multiply the frequency of clock source and output clock for CPU and other peripheral modules. One missing clock detector (**MCD**) is built-in to monitor the clock of external Xtal or external clock source.

### 6.4.2. Chip Clock Features

- Built-in embedded ILRCO (internal low frequency RC oscillator) by 32KHz
- Built-in embedded IHRCO (internal high frequency RC oscillator)
  - Trimmed to 11.059 or 12MHz  $\pm 1\%$  at +25°C
- Built-in embedded PLL clock output for system clock
- Built-in embedded XOSC oscillator with MCD for external 32KHz or 4 to 25MHz Xtal
- Support external clock input up to 36MHz
- Built-in a clock source controller with clock enable control for modules
- Support internal XOSC oscillator and internal ILRCO/IHRCO clock output

### 6.4.3. System Clock Source

There are four clock sources for the system application: Internal High-frequency RC Oscillator (**IHRCO**), Internal crystal oscillator (**XOSC**), Internal Low-frequency RC Oscillator (**ILRCO**) and External Clock Input (**EXTCK**). Software can select the one of the four clock sources by application required and switches them on the fly. But software needs to settle the clock source stably before clock switching.

### 6.4.4. PLL Clock

One PLL is embedded to multiply the frequency of system clock source from **IHRCO**, **ILRCO**, **XOSC** and **EXTCK**. The PLL multiplication value can be from 4 to 32. The PLL input frequency range is about 4~8 MHz and PLL VCO output frequency is up to over 150MHz. Usually, the PLL output frequency should be divided to do as CPU or others clock source. Refer the Electrical Characteristics chapter for detail specification about PLL.

### 6.4.5. Module Process Clock Control

The CSC module is able to do the process clock enable setting and select the process clock source for internal modules. User must select the module process clock and enable the module process clock before configure the module for operation normal.

## 6.5. System Common Control

### 6.5.1. Introduction

The chip embeds one system control (SYS) module for system common control. It is including of one system event interrupt global enable control, chip manufacture identification code.

### 6.5.2. Features

- System interrupt global enable control for system interrupt source
- Chip manufacture identification code - Device ID, Product ID, User ID, Module Options

## 6.6. Memory Access

### 6.6.1. Introduction

The chip has separate address spaces for program and data memory. The logical separation of program and data memory allows the memory to be accessed by 32bit addresses, which can be quickly stored and manipulated by the CPU. The chip supports one memory controller (MEM) to manage the internal flash memory and SRAM access operation.

### 6.6.2. Features

#### ❖ Embedded Memory

- Built-in embedded 128K bytes flash memory for application code
  - Optional 64K/128K bytes flash memory by different product
- Built-in embedded 16K bytes SRAM
  - Support private 2K bytes for DMA and 14K bytes for software to improve access performance

#### ❖ Memory Controller Features

- Support ICP (In-circuit program) for ISP boot code update through SWD interface
- Support ISP (In-system program) for application code update
  - Support programmable ISP flash memory size for ISP boot code
  - Provide fixed 512 bytes ISPD flash memory as ISP private data
- Support IAP (In-application program) for application data update
  - Support programmable IAP flash memory size
- Support flash memory page erase in 512 bytes

### 6.6.3. Memory Controller

A memory controller is supported to access on chip flash memory, SRAM on AHB bus. It includes **ICP** (In-Circuit Programming)/ **ISP** (In-System Programming)/ **IAP** (In-Application Programming) circuits for flash memory accessing, option byte loader for hardware option registers loading and an external memory bus EMB interface with the capability of accessing external program memory.

The chip has up to 128K bytes of embedded main flash memory for code and data, programmable memory size of embedded system flash memory for boot load code and 64 bytes of embedded option-byte flash memory for chip configuration.

The memory controller (MEM) supports to Read/ Program (Write)/ Erase the flash memory. User can directly read the data from flash memory by CPU read instruction commands and do not need through any register. For “Program” mode, MEM provides the 32-bit data write operation into flash memory for new data updated. For “Erase” mode, the Erase address is only valid at low 9-bit CPU address=0 (X...XX0 0000 0000B) and is addressing 512-byte alignment.

### 6.6.4. ICP/ISP/IAP for Flash Memory

There are 3 flash access modes are provided in chip for ICP, ISP and IAP application: program mode and read mode. ICP is allowed to update the entire contents of the flash memory by using the hardware SWD interface and no any firmware request. Others, User can use these two modes of ISP and IAP to update new data into flash storage and get flash content by a firmware flash memory access handler.

### 6.6.5. Hardware Option Byte Flash Memory

There can be up to **64** bytes of on-chip Option Bytes Flash memory. It is used to store the hardware option configuration setting.

The embedded option-byte (**OB**) flash memory will load into the hardware configuration option-byte register (**OR**) after power-on reset. The hardware configuration **OR** are designed to configure the clock source from internal RC oscillator or crystal oscillator; the booted memory selection from AP, ISP flash memory or SRAM; the memory size of IAP flash memory; other chip configurations ... etc.

## 6.7. External Memory Bus

The chip has built in an external memory bus (EMB) controller to access the external device of SRAM, NOR/NAND flash and 8080 interface LCD. The EMB controller supports address bus and data bus multiplex mode. Also, it provides two address latch enable signals to support the multiple control of the address and data cycle.

### 6.7.1. Features

- Support SRAM, NAND/NOR flash, LCD interface
- Support synchronous or asynchronous timing mode control
- Support 8/16-bit data width
- Support multiple types of address and data multiplex mode
- Provide optional 16/24/30-bit address mode
  - Memory space 2G/32M/128K-byte for 16-bit data width
  - Memory space 16M/64K-byte for 8-bit data width
- Received and transmitted data are buffered with DMA capability
- Configurable time cycle for address latch time and data access time
- Allow running CPU code on external SRAM

### 6.7.2. EMB Control Function

EMB supports optional data bus 8/16-bit data width and optional 16/24/30-bit address mode. The maximum memory space size of external device is 2G/32M/128K-byte for 16-bit data width or 16M/64K-byte for 8-bit data width.

EMB supports multiple types of address and data interface modes. They include multiple types of address and data multiplex modes.

EMB provides multiple timing states and programmable timing cycle for external device flexible design.

## 6.8. GPIO

### 6.8.1. Introduction

The chip has following I/O ports: **PA[15:0]**, **PB[15:0]**, **PC[14:0]**, **PD[15:0]**, **PE[15:12][9:8][3:0]**. Support maximum 73 GPIO pins for LQFP80 package. **RSTN** pin is an alternated function pin on **PC6**. If select external crystal oscillator as system clock input, **PC13** and **PC14** are configured to **XIN** and **XOUT**. The exact number of I/O pins available depends upon the package types.

The chip has built in several IO mode control (**PA/PB/PC/PD/PE**) modules for each GPIO port. These modules are used for GPIO pin IO mode control, alternated function selection, driver strength setting, input inverse selection, pull-high enable, deglitch filter setting and high speed enable. Also one IO Port access control (**IOP**) module is built-in to control the input and output state of GPIO mode for all GPIO ports.

### 6.8.2. Features

- Support general purpose IO pins for application
  - Maximum 73 GPIO pins for LQFP80 package
  - Maximum 59 GPIO pins for LQFP64 package
  - Maximum 44 GPIO pins for LQFP48 package
- Provide selectable IO modes by pin independent
  - Push-Pull output
  - Quasi bidirectional
  - Open-drain output
  - Input only with high impedance
  - Analog IO
- Flexible pin alternate function selection
- Support programmable drive strength by pin independent

- Support IO deglitch filter by pin independent
- Support input inverse selection by pin independent
- Support pull-high option by pin independent
- Support high speed option by pin independent except RSTN,XIN
- GPIO pin state and IO mode setting keep optional after reset

### 6.8.3. GPIO Control Block

The GPIO Control block includes IOM (IO pad Mode control), IOP (IO Port access control) and AFS (Alternate Function Select) blocks.

- **IO Operation Mode**

The IO operating modes are supported analog IO, digital input, push-pull output, and open-drain output, quasi-bidirectional. Provide selectable IO modes by pin independent.

The IO mode control block supports programmable IO operation modes, output high speed option, pull-high option, output drive strength, IO deglitch filter and input inverse selection by pin independent.

- **IO Port Access**

When the AFS setting is set GPIO function mode for any IO pin, user can directly set the logical output or get the logical input for the IO pin. There is one independent data out register bit to store the output logic value for each GPIO pin. Also user can directly read the input data register bit to get the GPIO pin logical state for each GPIO pin.

For firmware control, there are one set control bit to set the data out register bit and one clear control bit to clear the data out register bit for each GPIO pin.

The chip provides one set-or-clear register control bit to set, clear the data out register bit or read pin status for each GPIO pin. The register bit is written 1 to set data bit and written 0 to clear data. Read the register bit to get the GPIO pin status. As this register bit is cost eight bit memory space, firmware is easy to control single GPIO pin by CPU byte-access instruction command. It is like the bit access IO control of 8051 MCU.

- **Alternate Function Select Control**

User can configure the alternate function between module function IO and IO pins through the AFS matrix for each GPIO pin independently. Usually the AFS default setting is GPIO function for each GPIO pin except the **XIN/XOUT**, **SWCLK/SWDIO** and **RSTN** function pins. These pins may be changed by hardware configuration **OB**.

## 6.9. Interrupt

### 6.9.1. Introduction

After reset, the CPU begins execution from the location of reset interrupt vector (0x00000004) addressing, where should be the starting of the user's application code. To service the interrupts, the interrupt service locations (called interrupt vectors) should be located in the address 0x000000BF~0x00000000.

The chip is built-in ARM® cortex M0 CPU and is embedded a NVIC (Nested Vectored Interrupt Controller) for 32 external interrupt inputs with 4-level priority. Also builds in an EXIC (External Interrupt Controller) module and connects to NVIC.

### 6.9.2. Interrupt Features

- Built-in one NVIC for 32 external interrupt inputs with 4-level priority
- Built-in one EXIC (external interrupt controller) for NVIC connection
  - Independent high/low level and rising/falling edge trigger selection
- Built-in one WIC (wakeup interrupt controller) for wakeup event control
- All GPIO pins can be configured as interrupt source and key pad input
  - Support port OR logic for interrupt function
  - Support port AND logic for KBI function
- Support external pins for CPU NMI/RXEV/TXEV function
  - Configurable pin for CPU NMI input function
  - Configurable pin for CPU RXEV input function
  - Configurable pin for CPU TXEV output function

## 6.9.3. Interrupt Structure

Each interrupt is assigned a fixed location in the program memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. NMI interrupt, for example, is assigned to location 0x00000008. If NMI is going to be used, its service routine must begin at location 0x00000008.

The interrupt service locations are spaced at an interval of 4 bytes: 0x00000004 for Reset Interrupt, 0x00000008 for **NMI**, 0x0000000C for **Hard-Fault**, 0x0000002C for **SVC**Call, 0x00000038 for **PendSV**, 0x0000003C for **SysTick**, etc.

### ● Exception types

The NVIC has 7 exception types: **Reset**, **NMI**, **HardFault**, **SVC**Call, **PendSV**, **SysTick** and Interrupt (IRQ). The NVIC supports 32 external interrupt input. An interrupt is an exception signaled by a peripheral or generated by a software request. The four priority level interrupt structure allows great flexibility in handling these interrupt sources.

### ● Interrupt Sources

The 'Pending Bits' are the interrupt flags that will generate an interrupt if it is enabled by setting the 'Set Enable Bit'. The 'Pending Bits' can be set or cleared by software, with the same result as though it had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled in software. The 'Priority Bits' determine the priority level for each interrupt. The 'Priority within Level' is the polling sequence used to resolve simultaneous requests of the same priority level. The 'Vector Address' is the entry point of an interrupt service routine in the program memory.

**Table 6-2. Interrupt Source Table**

| NVIC          |         |                |              |              |                    | Comment                         |
|---------------|---------|----------------|--------------|--------------|--------------------|---------------------------------|
| Exception No. | IRQ No. | Interrupt Name | Priority     | Activation   | Exception handlers |                                 |
| 0             | -       | Initial        | -            |              |                    |                                 |
| 1             | -       | Reset          | -3           | Asynchronous |                    | Reset exception                 |
| 2             | -14     | NMI            | -2           | Asynchronous | System handlers    | Non Maskable Interrupt          |
| 3             | -13     | HardFault      | -1           | Synchronous  | Fault handler      | Cortex-M0 Hard Fault Interrupt  |
| 4~10          | -       | Reserved       | -            |              |                    |                                 |
| 11            | -5      | SVC            | Configurable | Synchronous  | System handlers    | Cortex-M0 SV Call Interrupt     |
| 12~13         | -       | Reserved       | -            |              |                    |                                 |
| 14            | -2      | PendSV         | Configurable | Asynchronous | System handlers    | Cortex-M0 Pend SV Interrupt     |
| 15            | -1      | SysTick        | Configurable | Asynchronous | System handlers    | Cortex-M0 System Tick Interrupt |
| 16~47         | 0~31    | -              | Configurable | Asynchronous | ISRs               | Peripheral Interrupts           |

Configurable : Programmable priority level 0~3

### ● Interrupt Priority

The priority scheme for servicing the interrupts has four interrupt levels. The priority bits in CPU registers, IPR0-7, SHPR2 and SHPR3, determine the priority level of each interrupt.

The interrupt priority registers provide an 8-bit priority field for each interrupt and each register holds four priority fields. The processor implements only bits [7:6] of each field, bits [5:0] read as zero and ignore writes.

Higher-priority interrupt will be not interrupted by lower-priority interrupt request. If two interrupt requests of different priority levels are received simultaneously, the request of higher priority is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determine which request is serviced. The table of "interrupt sources" shows the internal polling sequence in the same priority level and the interrupt vector address. The lower exception number gets the higher priority.

## 6.9.4. Nested Vectored Interrupt Controller

The Cortex®-M0 processor integrates a configurable Nested Vectored Interrupt Controller (NVIC) that supports low latency interrupt processing and includes a non-mask interrupt (**NMI**). The NVIC provides a zero-

jitter interrupt option and four interrupt priority levels.

Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with sleep mode. Optionally, sleep mode support can include a deep sleep function that enables the entire device to be rapidly powered down.

### 6.9.5. Wakeup Interrupt Controller

The chip includes a Wakeup Interrupt Controller (WIC) which can detect an interrupt or wakeup event from EXIC and wake the processor from deep sleep mode. The WIC is enabled only when the DEEPSLEEP bit in the CPU register of SCR is set to 1. The WIC is not programmable, and does not have any registers or user interface. It operates entirely from hardware signals.

### 6.9.6. External Interrupt Controller

The External Interrupt Controller (EXIC) includes four external port interrupt blocks (EXINT) to manage the external pin input interrupt events, one wakeup control block for wakeup event control and control the NMI/RXEV events. The EXIC also do as the interface controller between internal modules and NVIC for the interrupt and wakeup events management.

## 6.10. General Purpose Logic

### 6.10.1. Introduction

The chip builds in one general purpose logic (GPL) module. It provides the combined functions of Data Order Change, Parity Check, Data Inverse and CRC.

### 6.10.2. Features

- **Support data inverse, bit order change, byte order change and parity check**
  - Data bit order change for 8/16/32-bit reverse
  - Data byte order change between Little endian and Big endian for 16/32-bit range
  - Parity Check for 8/16/32 bit range
- **Support CRC (Cyclic Redundancy Check) calculation**
  - Programmable CRC initial value
  - CRC output bit order change
- **CRC with fixed common polynomial**
  - CRC8 polynomial 0x07
  - CRC16 polynomial 0x8005
  - CCITT16 polynomial 0x1021
  - CRC32(IEEE 802.3) polynomial 0x4C11DB7
- **Support signed/unsigned 32-bit divider**
  - Operation in 8 clock cycles
- **Input data are buffered with DMA capability**

### 6.10.3. GPL Control Block

- **Byte Order Change**

The GPL can change the byte order of input data for big or little endian format for 32-bit range or 16-bit range.

- **Bit Order Change**

The GPL can change the bit order of input data for 8/16/32-bit reversion. This process is able to select data size of 8-bit, 16-bit and 32-bit.

- **Data Invert**

The GPL can invert the data value from input data.

- **Parity Check**

The GPL can set the parity check polarity by odd or even and calculate parity.

- **CRC Calculation**

The CRC (cyclic redundancy check) block is used to get an 8/16/32-bit CRC data code and calculates the result. The CRC block can process continuously with sequent CRC code and store the last result into data buffer always.

- **Hardware Arithmetic Divider**

The GPL module is including a 32-bit hardware arithmetic divider. The arithmetic divider is general using for firmware development. The hardware divider is supported both unsigned and signed arithmetic calculation by register setting.

## 6.11. APB Common Control

### 6.11.1. Introduction

The chip builds in one APB (APB bus common control) module for the common control of APB devices.

### 6.11.2. Features

- **Timer synchronous enable global control**
- **OBM(Output Signal Break and Modulation) control**
  - Support two sets of OBM for output signal break and modulation control
- **NCO(Numerically Controlled Oscillator) output with FDC and PF modes**
- **Infrared Remote Modulation Output**

### 6.11.3. APB Control Block

- **Timer Common Control**

The TMx modules supports two timer enable control bits of **TMx\_EN** and **TMx\_EN2** to enable the Main timer and 2nd timer separately for each TMx module.

In APB module, there are the same control bits of **APB\_TMx\_EN** and **APB\_TMx\_EN2** as the timer enable bits of **TMx\_EN** and **TMx\_EN2**. These control register bits are built in one 32-bit register and can be enabled or disabled synchronously by setting **APB\_TMx\_EN** or **APB\_TMx\_EN2** registers for firmware easy control. (x = Timer module index).

The ITR6 and the ITR7 are used as the common signals of trigger event or clock signal for all timer modules. User can select the trigger source signal by register setting. The **APB\_ITR6** and **APB\_ITR7** signals can be selected from others TMx timer, URTx, ADC0, RTC modules and EXIC global interrupt events.

- **OBM Control**

The APB module is including of two identical sets of output signal break and modulation (OBM) block. The OBM block is used to break one of the output signals or do signal modulation.

- **IR Control**

The APB module is including of one IR (Infrared Remote) modulation block. This block is used to do signal modulation for the transmission of IR control.

- **NCO Control**

The APB module is including of one Numerically Controlled Oscillator (NCO) block. The NCO block is used to generate a divided frequency with a decimal clock signal from input clock signal. It is useful for the accurate frequency clock requested application.

The NCO block supports two output modes, one is fixed duty cycle mode (FDC) and another is pulse frequency mode (PFM). The NCO output signal can be outputted to external pin or internal other modules. It can send to UART modules to do as clock source input. Also it can output to do as the common trigger event or clock signal ITR7 for Timer modules. There are one output pin **NCO\_P0** to output the NCO output signal and this output signal can be inverted by setting register for application request.

## 6.12. APX

### 6.12.1. Introduction

The chip builds in one APX module for the extended function control of APB devices.

### 6.12.2. Features

- **Support two sets of CCL(Configurable Custom Logic)**

### 6.12.3. APX Control Block

- **CCL Control**

The APX module is including of two sets of Configurable Custom Logic (CCL) block. Each CCL block can be connected to the device pins or other internal peripherals' signal. The CCL can eliminate external extra logic gate devices for simple glue logic functions on user application. It supports the L-to-H signal detected event flag and the interrupt.

## 6.13. Direct Memory Access

### 6.13.1. Introduction

The chip is built-in a direct memory access controller (DMA) which is used to improve the performance of data transfer between peripheral and memory, memory to memory and peripheral to peripheral. Data can be quickly transfer by through DMA without costing any CPU resources.

Notify: The sign of (n= DMA channel index number) is using for Registers, Signals and Pins/Ports in the descriptions of this chapter.

### 6.13.2. Features

- **5 independently configurable channels with dedicated hardware DMA requests**
  - Access to Memory, APB and AHB Peripherals as source and destination
  - Support SRAM/Flash/EMB access memory space as memory source and destination
  - Peripheral is including of ADC0,DAC,I2Cx,URTx,SPIx,TM36
- **DMA transfer management type**
  - memory-to-memory (channel 0,3 only)
  - peripheral-to-memory
  - memory-to-peripheral
  - peripheral-to-peripheral
- **Built-in two type priority control between channel requests**
  - Channel request by Round Robin
  - Software configurable priority level
- **Programmable transfer number of data and up to 131072**
- **Programmable burst length 1,2,4**
- **Support transfer loop mode and start address auto reload control**
- **Provide single/block/demand mode for external pin trigger request**

### 6.13.3. DMA Control

The DMA controller (DMA) is used to transfer data between these sources and destinations of AHB peripheral, APB peripheral, SRAM and external memory. Two external pins of **DMA\_TRG0** and **DMA\_TRG1** are able to input as the trigger signal of DMA data transfer.

Each DMA channel is able to process the transfer types of peripheral-to-memory, memory-to-peripheral and peripheral-to-peripheral. The transfer type of memory-to-memory is only support for channel-0 and channel-3. The transferred memory sources can be embedded SRAM, Flash or external SRAM, Flash, 8080 LCD device by through EMB interface.

### 6.14. ADC

#### 6.14.1. Introduction

The chip builds in one ADC0 module which embeds one 12-bit successive approximation ADC (analog-to-digital converter), one PGA (programmable gain amplifier) with gain 1~4 and digital logic for output code control. It supports the configurable multiplexed channels those include 16 external and 4 internal sources. The analog-to-digital conversion can be performed in one-shot, continuous, one-loop scan or continuous loop scan modes.

The ADC is embedded one temperature sensor to measure the internal thermal of chip for product application.

#### 6.14.2. Features

- **12-bit SAR ADC with 1.5Msps**
  - Configurable resolution : 12/10/8-bit
  - Configurable sampling time
- **Provide external 16 channels and internal 7 channels input**
  - Internal channel source : VBUF, VSSA, LDO VR0, DAC out, 1/2VDD, VPG, TS out
- **Support auto-sampling and trigger by external pin, internal events and software bit**
- **Data alignment for output code left/right justify**
- **Built-in input buffer stage with bypass option**
- **PGA with programmable gain : 1~4**
- **Provide internal voltage source VBUF 1.4V**
- **Optional ADC top voltage reference from external VREF+ or internal IVR24**
- **Interrupt generation at the end of sampling, end of conversion, end of sequence conversion**
- **Support voltage window detect and output code limitation**
  - Two level programmable window threshold
- **Built-in three channel independent hardware accumulator for ADC output code**
- **Support one-shot/channel scan/loop scan**
- **ADC data are buffered with DMA capability**
- **Support wait mode**
  - Prevents ADC overrun in application with low frequency
- **Support auto off mode**
  - ADC auto power off except during the active conversion phase
- **Built-in a temperature sensor**
  - Temperature resolution : +/- 2 °C (Typical)
  - Temperature operation range : -40°C ~ 125°C

#### 6.14.3. ADC Control Block

The ADC control block consists of an analog multiplexer (AMUX) with 16 input channels, a **1.5Msps/12-bit** SAR (successive-approximation-register) ADC, reference voltage circuit, ADC conversion trigger start control block and change scan control block.

- **ADC Input Channels**

The analog multiplexer (AMUX) selects the inputs to the ADC, allowing any of the input pins to be measured in single-ended mode.

The analog input pins used for the A/D converters also have its I/O pins for digital input and output function. In order to give the proper analog performance, a pin that is being used with the ADC should have its digital output as disabled. It is done by putting the port pin into the input-only mode. And when an analog signal is applied to the **ADC\_In** pin and the digital input from this pin is not needed, software could set the corresponding pin to AIO mode to turn off the digital input buffer to reduce current consumption.

- **Single-End Mode**

The ADC supports single-end operation modes. The ADC can convert the ADC output to unsigned code for single-end mode.

- **ADC Sampling Time**

For input signal quality and conversion speed issue, user can adjust the ADC sampling time. Usually increase the ADC sampling time to get more stable voltage and better ADC performance if the conversion rate and signal bandwidth are reasonable and valid for actual application.

- **ADC Conversion Mode**

The ADC is supported three conversion modes of One Shot, Channel Scan and Loop Scan.

- **ADC Output Control**

When an ADC conversion is complete, the ADC raw code is generated and sends to the ADC output control blocks those are including of Digital Offset Adjuster, Signed Code Converter, Digital Resolution Adjuster, Voltage Window Detector, Code Limiter and Data Alignment Adjuster.

The ADC output code will be adjusted by the ADC output control blocks and store the conversion result data to the ADC data register.

- **Voltage Window Detect and Code Limit**

The ADC can compare the input voltage by a threshold window. Also the ADC output code can be compared by a code limit area to skip or clamp the code by the same threshold window.

- **ADC Data Sum Accumulate**

The ADC built-in one hardware accumulator for ADC output code. The accumulator is used to accumulate the sequential ADC data with programmable data number and records the sum to the summary registers. User can set the accumulated ADC data number. The ADC is supported three sum data registers and user can get the accumulated sum from these registers.

- **ADC Wait and Auto-Off**

The ADC supports a wait mode function to prevent ADC overrun in application with low frequency ADC sampling clock. Also ADC supports an auto off mode function to force the ADC auto entering power-off except during the active conversion phase.

## 6.15. Analog Comparator

### 6.15.1. Introduction

The chip builds in one CMP module which embeds two general purpose analog comparators with flexible input multiplexer, two internal voltage references of R-ladder and independent digital synchronized filter for each analog comparator. These analog comparators can be configured to two standalone comparators or a combined window comparator. The module provides the comparator output result status bit and the interrupt flags of rising edge or falling edge change. Also the output result can be output to external pin or internal other modules for trigger event.

### 6.15.2. Features

- Provide 2 fast Rail-to-rail comparators
- Programmable 64-step threshold of internal voltage reference
- Provide external total 6 channels input for all comparators
- Provide flexible 6 channels input for each +/- input path selection
- Programmable response time for optimal current consumption
- Combined window comparator from two comparators
- Selectable compare output polarity
- Support wakeup from SLEEP and STOP modes
- Compare output to I/O , interrupt or as internal module trigger event
  - Timer internal trigger, Capture events, or Break events
- Support analog watch dog as a reset source

### 6.15.3. CMP Control Block

The CMP module includes two general purpose analog comparators CMP0~1 by the same design structure and two internal voltage references *IVREF*/*IVREF2* by R-ladder structure. Each one is with the independent input multiplexer, digital synchronized filter and digital output circuit. The *IVREF* is only using for CMP0 and the *IVREF2* is only using for CMP1.

The analog comparator is built-in two internal voltage references – **IVREF** and **IVREF2** with 64-steps R-ladder structure. They can use as one of the analog comparator input and compare with another input from external source.

Each the analog multiplexer (AMUX) of the positive or negative input of any analog comparator has flexible 6 channels input. These channels are including of two common external channels, two comparator independently external channels and two common internal channels.

The two common external channels are from **CMP\_C0** and **CMP\_C1** pins those can input to all analog comparators. The two independent external channels are from **CMPn\_I0** and **CMPn\_I1** pins those can input to the analog comparator CMP0/1. The two common internal channels are from internal voltage reference of **IVREF** or **IVREF2** and internal DAC output **DAC\_P0** those can input to all analog comparators.

The analog input pins used for the comparators also have its I/O port's digital input and output function. In order to give the proper analog performance, a pin that is being used should have its digital output as disabled. It is done by putting the port pin into the digital input mode. And when an analog signal is applied to the analog input pin and the digital input from this pin is not needed, software could set the corresponding pin to AIO mode to reduce current consumption in the digital input buffer.

## 6.16. DAC

### 6.16.1. Introduction

The chip builds in one DAC module which embeds one 12-bit voltage mode DAC (digital-to-analog converter) and digital logic for input code control. The digital-to-analog conversion can be performed and start trigger by data register written, events (external pin input or internal events). The DAC can output a full-scale voltage from 0.2 volt to VDD-0.2 volt under the conversion rate up to 1MHz when DAC output buffer is on.

### 6.16.2. Features

- One 12-bit voltage DAC
  - Maximum conversion rate is 1MHz
  - Analog output to ADC internal channel
- Conversion start trigger by register written, external pin and internal events
- Build in internal output buffer
- Data alignment for input code left/right justify
  - Configurable code width : 12/10/8-bit
- Output data are buffered with DMA capability

### 6.16.3. DAC Control Block

The DAC control block consists of a 1Msps/12-bit voltage mode DAC, reference voltage circuit, a DAC data code register, a DAC conversion output register (**DAC\_DOR0**) and DAC conversion trigger start control block.

The DAC output is programmable to full-scale output voltage from 0.2 volt to VDD-0.2 volt with DAC output buffer on. The voltage DAC output resistive load is minimum 7.5Kohm with DAC output buffer on.

## 6.17. IWDG

### 6.17.1. Introduction

The chip has one independent Watch-dog timer to use as a recovery method in situations where the CPU may be subjected to software upset. It will trigger system reset when the counter reaches a given timeout value.

### 6.17.2. Features

- 8-bit down counter with 12-bit prescaler and clocked by its own CK\_ILRGO
- Operating capability in SLEEP and STOP modes
- Selectable reset or interrupt when the counter underflow
- Support two early wakeup comparators with interrupt
- Support register key-protected and reset-locked functions

### 6.17.3. IWDG Control

The IWDT watch-dog timer consists of a 12-bit prescaler and an 8-bit timer. When the watch-dog timer is enabled, software should always reset the timer before the timer is timeout. When the watch-dog timer is reset, the timer will be reloaded 0xFF value to restart counting.

If the chip is out of control by any disturbance, the firmware may miss to reset the timer and the timer timeout will be coming. It makes the IWDT generating a reset event and sends it to Reset Source Controller (RST) to do as the warm reset events or cold reset events.

The IWDT is able to record default initialized value in hardware option byte (**OB**) about IWDT on/off, input clock divider value, IWDT registers write protection.

The IWDT is able to operate in **STOP** mode and the APB clock is stopped and the module is asynchronous control for all logic.

The IWDT supports to wakeup chip in **STOP** mode by the events of watch-dog timer underflow and early wakeup-0/1 detection. When the chip is entering **STOP** mode and any of these IWDT wakeup events is happened, the IWDT will send the wakeup event to Power Controller (PW) to do as the system wakeup events.

## 6.18. WWDT

### 6.18.1. Introduction

The system window watchdog is used to detect the occurrence of a software fault which causes the application program abnormal. The watchdog circuit generates a system reset when the counter reaches a given timeout value.

The WWDT has a configurable time-window that can be programmed to detect abnormally late or early application behavior.

### 6.18.2. Features

- 10-bit counter with 1 or 256 divider , 1/2/4~128 divider
- Configurable time-window to detect abnormally late or early application behavior
- Selectable reset or interrupt when the counter is underflow or reloaded outside the window
- Support warning interrupt
- Support register key-protected and reset-locked functions

### 6.18.3. WWDT Control

The WWDT watch-dog timer consists of one /1 or /256 clock prescaler, one 7-bit clock divider and one 10-bit timer. When the watch-dog timer is enabled, software should always reset the timer before the timer is timeout. When the watch-dog timer is reset, the timer will reload the value to restart counting.

When the firmware is out of control, which may miss to reset the timer and the timer timeout will be coming. It makes the WWDT generating a reset event and sends it to Reset Source Controller (RST) to do as the warm reset events or cold reset events. If the firmware reset the timer and the counter value is over the threshold value of window compare threshold in the same time, it also makes the WWDT generating a reset event.

## 6.19. RTC

### 6.19.1. Introduction

The real-time clock is an independent 32-bit timer. The RTC provides a time clock with programmable alarm interrupt. User can use as a calendar with software programmable alarm seconds, minutes, hours, day, and date.

The RTC provides a wakeup flag to perform auto wakeup from power down mode with interrupt.

### 6.19.2. Features

- Built-in 32-bit counter with selectable clock source
- Support alarm function and time-stamp function
  - Support alarm function with 32-bit programmable compare register
- Support wakeup from Stop mode
- Support periodic timer tick interrupt or wakeup
- Support register key-protected and reset-locked functions

### 6.19.3. RTC Control

The RTC supports an alarm function and one register to sets the RTC alarm compare value. When the RTC timer value is matched with RTC alarm compare value, the RTC alarm flag is asserted and generates an interrupt. Also the RTC can capture from the 32-bit timer value or reload value to the 32-bit timer.

The RTC supports a time stamp function by external input. User can select input trigger edge of rising edge, falling edge or dual-edge. When an external input signal is matched, the RTC time stamp flag is asserted and generates an interrupt.

One **RTC\_OUT** output is able to output the RTC internal signals to internal modules or external pin. There are four signals of timer overflow signal toggle output, time stamp trigger event, timer input periodic clock signal and alarm compare output event which can be selected and sent from **RTC\_OUT** output.

The RTC is able to operate in **STOP** mode and the APB clock is stopped and the module is asynchronous control for all logic.

The RTC supports to wakeup chip in **STOP** mode by the events of timer overflow, timer input periodic clock and alarm compare output. When the chip is entering **STOP** mode and any of these RTC wakeup events is happened, the RTC will send the wakeup event to Power Controller (PW) to do as the system wakeup events.

## 6.20. Timer

### 6.20.1. Introduction

The chip has seven Timer/Counter modules: TM00, TM01, TM10, TM16, TM20, TM26 and TM36. All of them can be configured as timers or event counters.

TM0x has an 8-bit timer/counter with 8-bit prescaler. TM1x has a 16-bit timer/counter with 16-bit prescaler. TM2x has a 16-bit timer/counter with 16-bit prescaler and embeds two input capture/output compare channels. TM36 has a 16-bit timer/counter with 16-bit prescaler and embeds four input capture/output compare channels.

### 6.20.2. Features

- **Provide seven timers/counters : TM00, TM01, TM10, TM16, TM20, TM26, TM36**
- **Timer module common functions**
  - Selectable Full-counter , Cascade , Separate modes
  - Multiple internal and external signals as timer clock source or trigger source
  - Internal timer events output to pin or other modules as input trigger event
  - Support timer reset , trigger start and clock gating for trigger source function
  - Timer overflow as clock output to external pin output
  - Programmable counter auto-stop mode
  - Main counter support up/down control (TM16/TM26/TM36 only)
  - 2nd counter support up/down control (Separate mode)
- **Provide TM36 timer module**
  - 32-bit timer/counter
  - 4 CCP (input Capture/output Compare/PWM) channels
  - 3 CCP channels with OCN (complementary output compare)
  - PWM function with center-align, dead time control and break control
  - Support OC comparator split to two separated comparators mode
  - QEI(Quadrature Encoder Interface) support
  - One IC and three OC with DMA capability
  - Extra repetition counter for auto-stop mode
- **Provide TM2x timer modules**
  - 32-bit timer/counter
  - 2 CCP (input Capture/output Compare/PWM) channels
  - 2 CCP channels with OCN (complementary output compare)
  - PWM function with edge-align
  - Support OC comparator split to two separated comparators mode
  - QEI(Quadrature Encoder Interface) support (TM26 only)

- Extra repetition counter for auto-stop mode
- Provide TM1x timer modules (TM10,TM16)
  - 32-bit timer/counter
- Provide TM0x timer modules (TM00,TM01)
  - 16-bit timer/counter

### 6.20.3. Module Functions

The following table is showing the implemented functions of Timer modules.

**Table 6-3. Timer Module Function Table**

| Module Functions         | TM00 | TM01 | TM10 | TM16 | TM20 | TM26 | TM36 |
|--------------------------|------|------|------|------|------|------|------|
| Timer/Counter total bits | 16   | 16   | 32   | 32   | 32   | 32   | 32   |
| Timer Cascade Mode       | yes  | yes  | yes  | yes  | yes  | yes  | yes  |
| Timer Separate Mode      | yes  | yes  | yes  | yes  | yes  | yes  | yes  |
| Timer Full-Counter Mode  | yes  | yes  | yes  | yes  | yes  | yes  | yes  |
| Independent channels     |      |      |      |      | 2    | 2    | 4    |
| Internal TRGI lines      | 8    | 8    | 8    | 8    | 8    | 8    | 8    |
| External TRGI lines      | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| Output TRGO lines        | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| Output CKO lines         | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| Input Capture IC lines   |      |      |      |      | 2    | 2    | 4    |
| Output OC lines          |      |      |      |      | 2    | 2    | 4    |
| Output OCN lines         |      |      |      |      | 2    | 2    | 3    |
| Output OCH lines         |      |      |      |      | 2    | 2    | 4    |
| Input Break lines        |      |      |      |      |      |      | 1    |
| PWM separated two        |      |      |      |      | yes  | yes  | yes  |
| PWM edge-align           |      |      |      |      | yes  | yes  | yes  |
| PWM center-align         |      |      |      |      |      |      | yes  |
| Dead-time generator      |      |      |      |      |      |      | yes  |
| Up/Down of 1st Timer     | U    | U    | U    | U/D  | U    | U/D  | U/D  |
| Up/Down of 2nd Timer     | U/D  | U/D  | U/D  | U/D  | U/D  | U/D  | U/D  |
| Timer auto Stop          | yes  | yes  | yes  | yes  | yes  | yes  | yes  |
| QEI timer U/D control    |      |      |      |      |      | yes  | yes  |
| 3-input XOR to CH-0      |      |      |      |      |      |      | yes  |
| DMA request capability   |      |      |      |      |      |      | yes  |

**<Note>** 1. Timer Cascade Mode ~ 16-bit\_counter+16-bit\_prescaler or 8-bit\_counter+8-bit\_prescaler  
 2. Timer Separate Mode ~ two 16-bit\_counter or 8-bit\_counter  
 3. Timer Full-Counter Mode ~ 32-bit\_counter or 16-bit counter

### 6.20.4. Timer Control Block

The TMx module is including of a Trigger/Clock control block, a Counter Stage, an Capture/Compare control block and Input/Output Stages of channel I/O control (TM2x,TM3x only) and a Break control block (TM36 only). TMx support three timer operation modes: (1) Cascade Mode (2) Separate Mode (3) Full-Counter Mode.

#### ● Trigger Control Block

The Trigger Control block has two functions, one is to control the timer trigger input events and another is to control the timer trigger output events.

The timer trigger input events are including of Reset Timer, Gated Clock and Timer-Start Trigger for Main Timer and 2<sup>nd</sup> Timer. The input source of the timer trigger input events is selected from external trigger signal, internal trigger signals or external channel input signal of **TMx\_IN0/TMx\_IN1**.

The source of the timer trigger output events are able to come from many internal events or signals of this timer module. Also user can use the software register to set the trigger output directly. This source of output event can select and invert the output signal by registers.

- **Timer Input/Output Channels**

The following table is showing the channel input signals for each timer module. TM0x and TM1x modules are no channel input selection function as the input capture/output compare is not support. Each channel has four input lines.

- **Timer Input Capture and Output Compare**

The input capture (IC) and output compare (OC) functions are only supported for TM2x and TM3x modules. TM0x and TM1x modules are no the functions of the input capture/output compare.

User can configure each of the timer IC/OC channel independently as input capture, output compare or PWM mode.

- **PWM Dead-Time Control**

The Dead Time Generator (DTG) is only support for TM36 module. User can use with the DTG function and configure the timer channel as 16bit PWM mode or Two 8bit PWMs mode.

- **Break Control Block**

The break control block is only support for TM36 module. The module can input the break events from internal events, external events or software register to break the timer output signals.

- **QEI Control Block**

The QEI (Quadrature Encoder Interface) control block is only support for TM26 and TM36 modules. The QEI block can input from two external signals to control the Main Timer up or down counting. The QEI block provides five control modes and user can enable QEI control and configure the QEI control mode by register.

When the QEI control block is enabled, the timer will reset during up counting or reload the auto-reload value during down counting if detect the index signal active pulse.

## 6.21. I2C

### 6.21.1. Introduction

The I2C interface is a two-wire, bi-directional serial bus. It is ideally suited for typical microcontroller applications. The I2C protocol allows the systems designer to interconnect up to 128 different devices using only two bi-directional bus lines, one for clock (SCL) and one for data (SDA). The I2C bus provides control of SDA, SCL generation and synchronization, arbitration logic, and START/STOP control and generation. The only external hardware needed to implement this bus is a single pull-up resistor for each of the I2C bus lines. All devices connected to the bus have individual addresses, and mechanisms for resolving bus contention are inherent in the I2C protocol.

The I2C module builds in the shadow buffer and data register to improve transmit and receive communication performance.

### 6.21.2. Features

- Provide two identical I2c modules : I2C0 , I2C1
- Support master and slave mode
- Support programmable clock rate control and clock rate up to 1 MHz
- Support programmable high/low period control for master mode
- Support clock stretching for slave mode
- Support general call function
- Support multi-master processing capability
- Support both Byte mode and Buffer mode flow control
- Support Byte mode bus event code for simplex firmware control
- Support Buffer mode 4-byte data buffer and 32-bit data register for high speed communication
- Received and transmitted data are buffered with DMA capability
- Support slave address hardware detection wakeup from STOP mode
- Support SMBus timeout detection

### 6.21.3. I2C Control

- **I2C Data Byte Mode Control**

The module provides one bus event register to get the I2C Event Code for software byte-mode simplex control. An 8-bit shift buffer and an 8-bit data register are used for the I2C data Byte mode.

- **I2C Data Buffer Mode Control**

The module implements an 8-bit shift buffer, a 32-bit shadow buffer and a 32-bit data register for data flow control of data Buffer mode..

- **I2C Master Timing Control**

Two timing control registers are simply used to configure the I2C timing of high and low cycle time.

- **I2C Timeout Timer Control**

The module provides one 8-bit timeout timer (TMO) for I2C access time-out control.

## 6.22. UART

### 6.22.1. Introduction

There are two types of UART module, one is advanced UART modules and another is basic UART modules. The advanced UART modules are including of URT0 ~ URT2. The basic UART modules are including of URT4 ~ URT7 those are only support asynchronous communication mode through RX and TX two pins.

The advanced UART module support full-duplex transmission, meaning it can transmit and receive simultaneously. The module builds in the shadow buffer and data register by transmit and receive independently to improve transmit and receive communication performance. It can commence reception of a second byte before a previously received byte has been read from the register. However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.

The advanced UART module can operate in multiple modes: asynchronous communication, synchronous communication, SPI master, *SmartCard*, *LIN*, multi-processor mode. The asynchronous communication operates as a full-duplex Universal Asynchronous Receiver and Transmitter (UART), which can transmit and receive simultaneously and at different baud rates.

### 6.22.2. Features

- **Provide seven UART modules : URT0~2, URT4~7**
- **UART module common functions**
  - Provide precise UART baud-rate control by programmable oversampling rate
  - Support baud rate up to 6 Mbit/s
  - Programmable data word length - 7 or 8 bits
  - Hardware parity checking and parity generation
  - Programmable 4~32 oversampling rate
  - Swappable TX/RX pin configuration
  - Separate signal polarity control for transmission and reception
- **Provide URT0/1/2 advanced UART module**
  - Support UART, Synchronous, SPI master/slave, SmartCard, LIN, Multi-processor modes
  - Selectable MSB or LSB first data order
  - Configurable stop bits - 0.5, 1, 1.5 or 2 stop bits
  - Support a timeout timer for Idle/RX/Break/Calibration timeout detection
  - Support 4-byte data buffer and 32-bit data register for high speed communication
  - Support auto baud-rate detection and calibration
  - Support multiprocessor communication for master and slave mode - Idle-Line , Address-Bit
  - Support low speed UART-like frame format IrDA
  - Support transceiver hardware flow control by CTS/RTS signals only
  - Provide driver enable signal to activate the transmission for bidirectional communication
  - Support transmission-error hardware detection and auto resent control for Smart-card application
  - Support receiving parity error hardware detection and auto retry control for Smart-card application

- Received and transmitted data are buffered with DMA capability
- Provide URT4/5/6/7 basic UART modules
  - Support TX/RX independent 8-bit data register for simplex firmware control
  - Configurable stop bits - 1 or 2 stop bits

## 6.22.3. Module Functions

The following table is showing the implemented functions of UART modules.

**Table 6-4. UART Module Function Table**

| Module Functions                  | URT0/1/2       | URT4/5/6/7 | Comment                                                                    |
|-----------------------------------|----------------|------------|----------------------------------------------------------------------------|
| UART - asynchronous               | yes            | yes        |                                                                            |
| Synchronous - SPI Master mode     | yes            |            | Synchronous - Master 2 data lines                                          |
| Synchronous - SPI Slave mode      | yes            |            | Synchronous - Slave 2 data lines                                           |
| SmartCard - ISO7816-3             | yes            |            |                                                                            |
| LIN                               | yes            |            |                                                                            |
| Multiprocessor - Address Bit      | yes            |            |                                                                            |
| Multiprocessor - Idle Line        | yes            |            |                                                                            |
| IrDA - UART Like                  | yes            |            | low speed UART-like frame format IrDA (SIR Normal Mode)                    |
| Hardware flow control             | yes            |            | only support CTS/RTS                                                       |
| External Clock pin                | 1              |            |                                                                            |
| Timer BRO,TMO pins                | 2              |            |                                                                            |
| Shadow Buffer                     | 4-byte         |            |                                                                            |
| Data 7-bit option                 | yes            | yes        |                                                                            |
| TX parity bit generation          | yes            | yes        | hardware auto generate the parity bit from the data byte                   |
| Msb/Lsb transfer option           | yes            |            |                                                                            |
| Configurable stop bits            | 0.5, 1, 1.5, 2 | 1, 2       | programmable Stop bit length                                               |
| Auto Baud-Rate calibration        | yes            |            | auto Baud-Rate detection and calibration                                   |
| Mute mode auto enter/exit         | yes            |            | enter mute mode if address match does not occur                            |
| Break condition detect            | yes            |            |                                                                            |
| Idle line detect                  | yes            |            |                                                                            |
| Programmable over sampling number | 4~32           | 4~32       |                                                                            |
| Programmable clock phase/polarity | yes            |            | for synchronous mode                                                       |
| General timer control             | yes            | yes        | baud-rate timer and timeout timer as general timer                         |
| Drive enable                      | yes            |            | Drive enable signal of the transmission mode for the external transceiver. |
| RX parity error detect            | yes            | yes        | checks parity of received data byte                                        |
| Frame error detect                | yes            | yes        |                                                                            |
| Data overrun detect               | yes            | yes        | receive buffer over threshold level; transmit buffer empty                 |
| TX error detect                   | yes            |            | SmartCard/LIN                                                              |
| Noise character detect            | yes            |            | skip or not for noise character                                            |
| Idle timeout detect               | yes            |            | for SmartCard application                                                  |
| RX timeout detect                 | yes            |            | aging character detection                                                  |
| Break timeout detect              | yes            |            | for LIN application                                                        |
| Calibration timeout detect        | yes            |            | for LIN application                                                        |
| DMA request capability            | yes            |            |                                                                            |

## 6.22.4. UART Control

The UART module is able to configure the control mode from one of UART (asynchronous mode), SYNC (synchronous mode), IDLE (multi-processor idle mode) and ADR (multi-processor address-bit mode).

The UART module implements two operation modes of Idle-Line mode or Address-Bit mode for multi-processor communication.

- **UART Data Buffer**

The UART module implements two 8-bit shift buffers, two 32-bit shadow buffer and two 32-bit data register for data flow control and reduce the CPU overhead.

- **UART Data Character Format Setting**

The UART character is defined as the data unit for UART transaction. Generally, the character is including of one Start bit, 8-bit or 7-bit data bits and one Stop bit. Others, it also can insert one parity bit (PAR) and one address bit (ADR) for multi-processor mode.

- **UART TMO Timeout Control**

The module is provides one 16-bit timeout timer (TMO) for UART access time-out control. It can configure as an UART timeout timer or a general using timer by register. When the TMO timer is configured as a general using timer, there is one reload register for the timer.

The TMO timer can use to detect Idle Line condition, Break Timeout, RX Timeout, Idle Timeout and Baud-Rate Calibration Timeout.

- **UART Baud-Rate Control**

The Baud-Rate timer (BR) can configure as an UART Baud-Rate generator or a general using timer. The Baud-Rate timer generator is able to output the internal clock for UART communication Baud-Rate control.

- **UART Mute Mode Control**

The UART module is support a mute mode to disable receiving data character but the shift buffer is still operation for status detection. When the UART is entering mute mode, the RX shadow buffer is never load into data from shift buffer. The mute mode is useful for multi-processor communication.

The mute mode can be automatic by hardware detection to enter or exit by register configuration. Also it can be directly forced to enter or exit by register setting and user can manual to control the mute mode entering and exiting.

- **UART IrDA Control**

The UART module is built an IrDA encoder and an IrDA decoder in the data interface for IrDA communication.

- **UART DE Control**

The UART module provides one data enable signal of **URTx\_DE**. This signal is used to indicate the data transmitted period and can output to external signal drive device. The external signal drive device can receive the UART TX signal and drive it with a signal enhanced buffer to the target of UART receiver for long distance communication.

- **UART Hardware Flow Control**

The UART supports a hardware flow control function for data transaction and provides two control signals of **URTx\_CTS** (Clear to Send) and **URTx\_RTS** (Request to Send) for the hardware flow control.

## 6.23. SPI

### 6.23.1. Introduction

The chip provides a high-speed serial peripheral interface (SPI). SPI is a full-duplex, high-speed and synchronous communication bus with two operation modes: Master mode and Slave mode. The SPI clock rate can be up to 22 MHz for Master mode and up to 16 MHz for Slave mode under a 48MHz APB clock.

The SPI module builds in the shadow buffer and data register by transmit and receive independently to improve transmit and receive communication performance.

### 6.23.2. Features

- **Support master and slave mode**
  - Support full duplex , half duplex or simplex communication mode
  - Support data communication without NSS(slave select signal)
  - Support master data input sampling delay half of SPI clock
  - Support configurable idle state for SPI master standard mode data output
  - Support asynchronous clock mode for SPI slave standard mode
- **Support programmable clock rate control**
- **Selectable 4~32-bit frame size**

- Support 4-byte data buffer and 32-bit data register for high speed communication
- Received and transmitted data are buffered with DMA capability
- Support multi-master processing capability
- Selectable clock polarity and phase
- Selectable MSB or LSB first data order
- NSS line management by hardware or software for master mode
- Configurable data transfer modes
  - Standard SPI mode (separated transmit and receive line)
  - Single /Dual/Quad/Octal SPI mode with bidirectional data transfer
- Support DTR (Double Transfer Rate) mode
- Data transmit/receive overrun detect
- Support hardware master mode failure detection and auto slave mode change

### 6.23.3. SPI Control

- **SPI Data Buffer Mode Control**

The module implements two 32-bit shift buffers, two 32-bit shadow buffer and two 32-bit data register for data flow control and reduce the CPU overhead.

- **SPI Data Frame**

User can set the data frame bit size from 4-bit to 32-bit by register. Also user can configure the frame data order by Lsb first or Msb first.

- **SPI Data Modes**

The SPI module provides several data modes and can be configured to one of the modes of standard SPI, 1-Line SPI, 2-Line SPI, 4-Line SPI, two duplicated 4-Line SPI or 8-Line SPI for flexible SPI application.

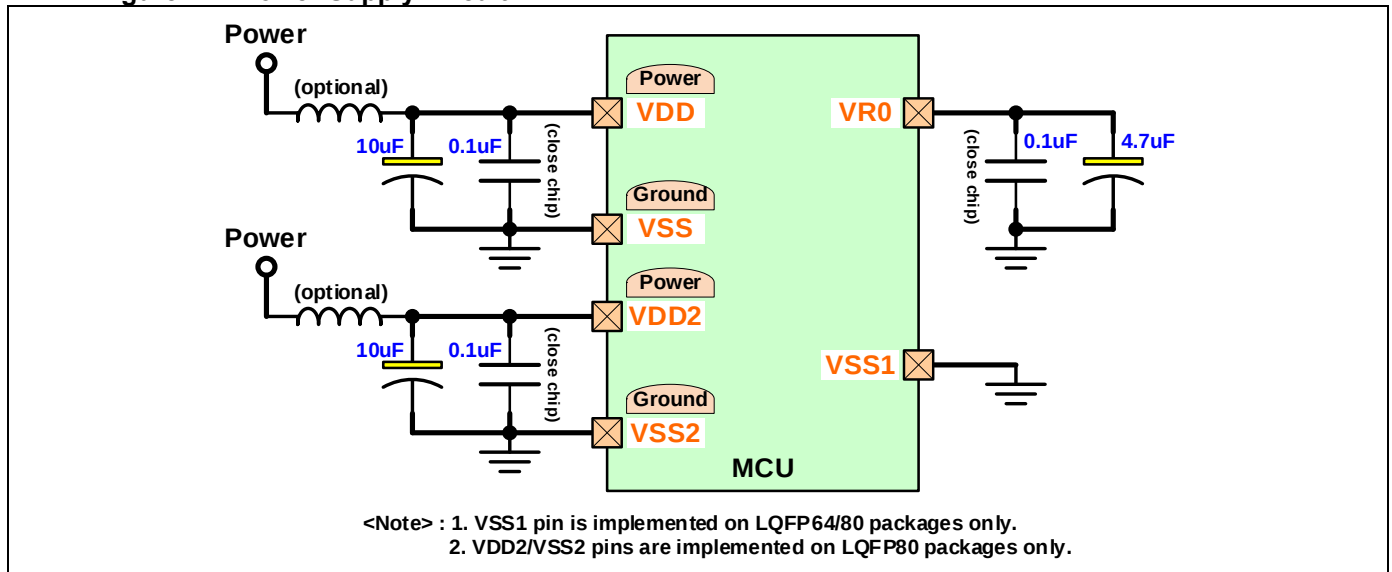
## 7. Application Notes

### 7.1. Power Supply Circuit

To have the chip work with power supply varying from 1.8V to 5.5V, adding some external decoupling and bypass capacitors is necessary on **VDD/VSS** power pins, as shown in following figure. Also the same application suggestion on **VDD2/VSS2** power pins for LQFP80 package. The **VR0** pin is the embedded LDO voltage output as internal core logic power supply. It needs to place one 0.1uF capacitor and one 4.7uF capacitor to be closed the pin.

The following figure is showing the power supply suggestion circuit.

**Figure 7-1. Power Supply Circuit**



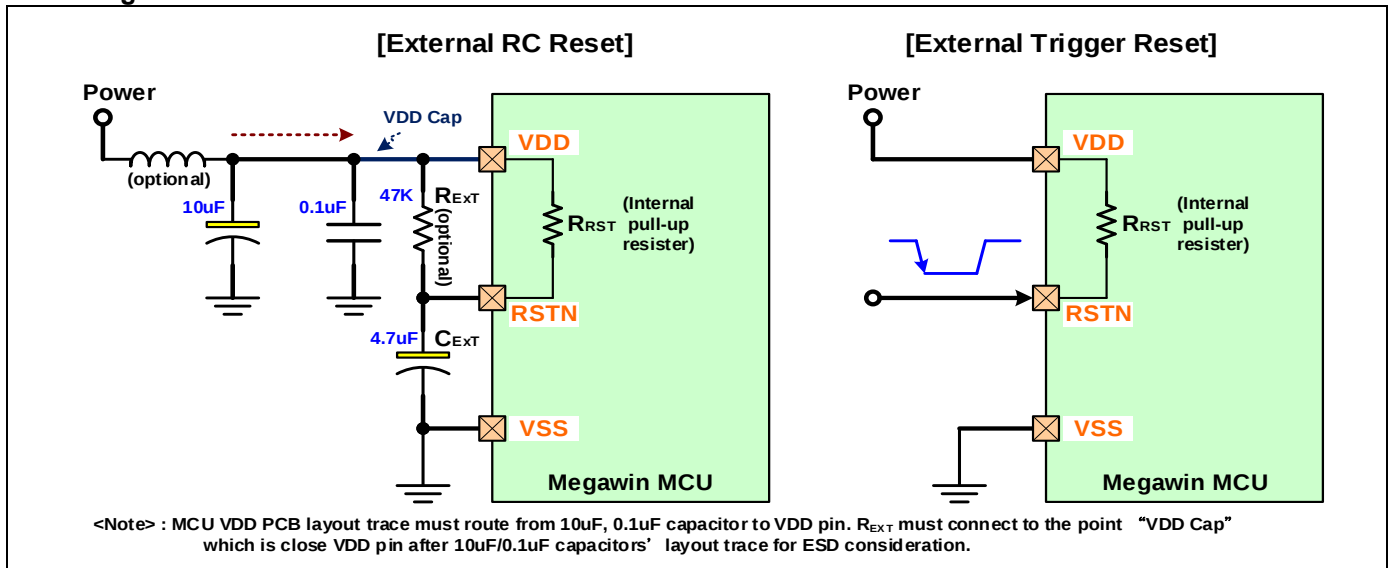
## 7.2. Reset Circuit

Normally, the power-on reset can be successfully generated during power-up. However, to further ensure the MCU a reliable reset during power-up, the external reset is necessary. The following figure shows the external reset circuit, which consists of a capacitor  $C_{EXT}$  connected to  $VSS$  (ground) and a resistor  $R_{EXT}$  connected to  $VDD$  (power supply).

In general,  $R_{EXT}$  is optional because the  $RSTN$  pin has an internal pull-high resistor ( $R_{RST}$ ). This internal diffused resistor to  $VDD$  permits a power-up reset using only an external capacitor  $C_{EXT}$  to  $VSS$ .

Strongly suggestion, the  $RSTN$  pin must set to output mode if it is used to do as both chip reset and GPIO functions in application. In this condition, the pin input low may make chip reset locked error if it set to GPIO input mode.

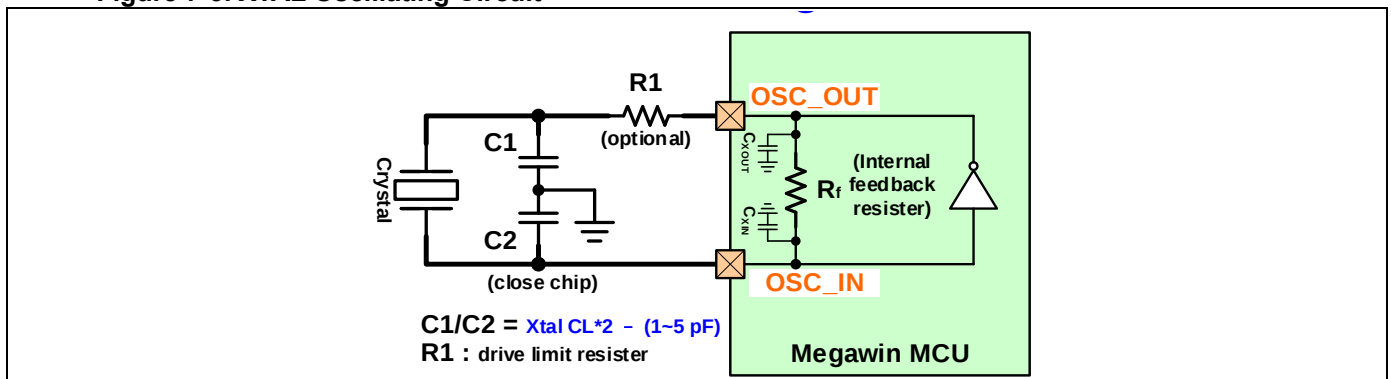
Figure 7-2. Reset Circuit



## 7.3. Xtal Oscillating Circuit

To achieve successful and exact oscillating (up to 25MHz), the capacitors  $C1$  and  $C2$  are necessary, as shown in following figure. Normally,  $C1$  and  $C2$  have the same value. Refer the capacitor load (CL) value in Xtal manufacture specification for the final matching capacitor of  $C1$  &  $C2$ .

Figure 7-3. XTAL Oscillating Circuit



❖ **Xtal Capacitor Selection**

$C_{XIN}$  /  $C_{XOUT}$ : Chip internal total equivalent capacitance of internal oscillator circuit, bounding pad, bounding wire, lead frame.

**Table 7-1. Internal Total Equivalent Capacitance for XOSC circuit**

| Component  | Capacitance Value |
|------------|-------------------|
| $C_{XOUT}$ | 1.5pF (0.9~2.0pF) |
| $C_{XIN}$  | 2.3pF (2.2~2.4pF) |

The XTAL Load Capacitance  $CL = C11 // C22 + Cp$

$C11 = C1 + C_{XOUT}$

$C22 = C2 + C_{XIN}$

$Cp$ : the distribution/stray capacitance that is generated by PCB layout path

= 1.18 pF/in for 2-layer FR4 PCB (Trace width=12mil, PCB height= 1.6mm)

= 3.16 pF/in for 4-layer FR4 PCB (Trace width=10mil, Subtract height=6mil)

The following table lists the suggested **C1** & **C2** value for the different capacitor load (**CL**) crystal application.

**Table 7-2. Reference Capacitance of C1 & C2 for crystal oscillating circuit**

| Crystal C Load | C1, C2 Capacitance |
|----------------|--------------------|
| 12.5pF         | 20pF (18~22pF)     |
| 20pF           | 36pF (33~39pF)     |
| 32pF           | 62pF (56~62pF)     |

❖ **Xtal Capacitor Value Calculation Example**● **C1/C2 Capacitor Selection Example-1**

If  $CL = 12.5$  pF (get from Xtal manufacture specification),

$Cp = 1\sim 2$ pF, then  $C11//C22 = 10.5 \sim 11.5$  pF

$$\frac{C11 * C22}{C11 + C22} = 10.5 \sim 11.5 \text{ pF}$$

$C11$  and  $C22$  are symmetric, we can get  $C11 = C22 = 21 \sim 23$  pF.

Then  $C1 = C11 - C_{XOUT} = 19\text{pF} \sim 22.1\text{pF} \rightarrow 20\text{pF}$

$C2 = C22 - C_{XIN} = 18.6\text{pF} \sim 20.8\text{pF} \rightarrow 20\text{pF}$

● **C1/C2 Capacitor Selection Example-2**

If  $CL = 20$  pF (get from Xtal manufacture specification),

$Cp = 1\sim 2$ pF, then  $C11//C22 = 18 \sim 19$  pF

$$\frac{C11 * C22}{C11 + C22} = 18 \sim 19 \text{ pF}$$

$C11$  and  $C22$  are symmetric, we can get  $C11 = C22 = 36 \sim 38$  pF.

Then  $C1 = C11 - C_{XOUT} = 34\text{pF} \sim 37.1\text{pF} \rightarrow 36\text{pF}$

$C2 = C22 - C_{XIN} = 33.6\text{pF} \sim 35.8\text{pF} \rightarrow 36\text{pF}$

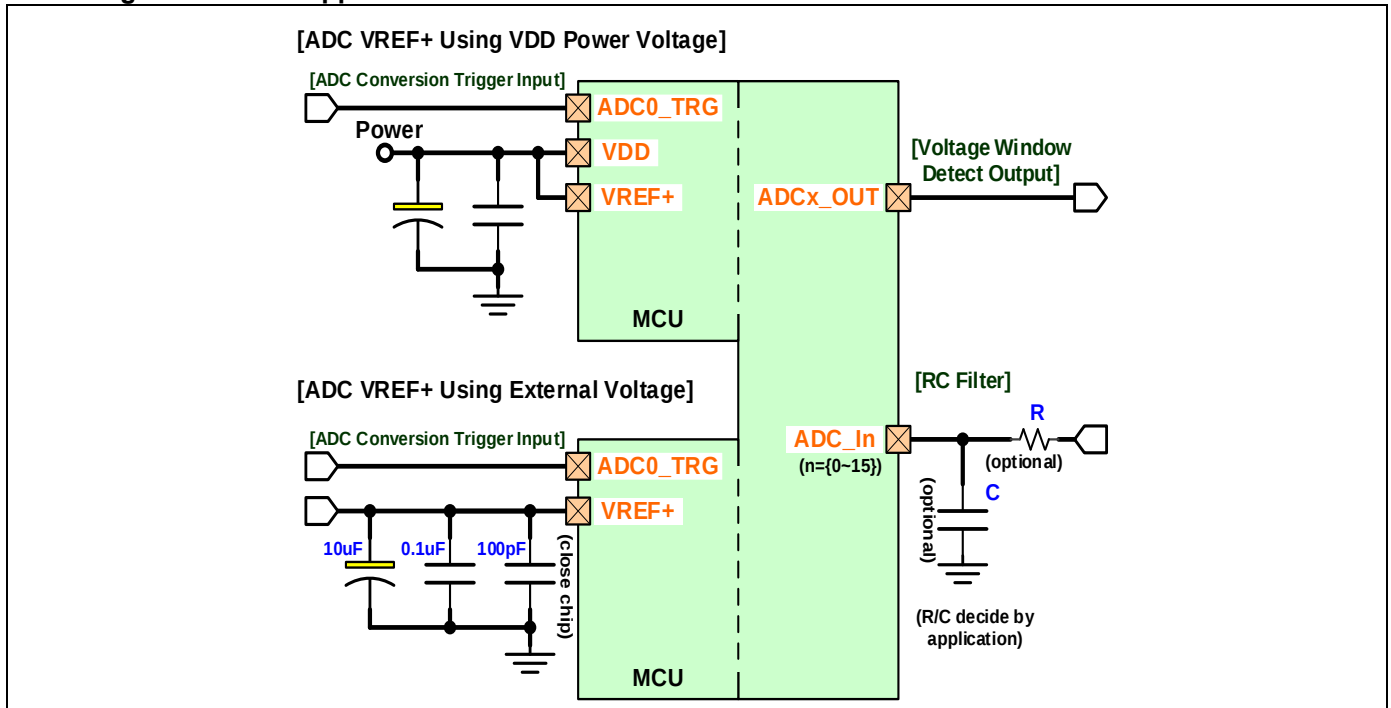
## 7.4. ADC Application Circuit

The ADC reference voltage source can be from (1) VDD power by connecting **+VREF** pin to **VDD** pin directly (2) external quiet reference voltage source.

When uses the VDD power as the ADC reference voltage, it must connect **+VREF** pin trace to the point which is at current flow behind the power capacitor(s). When uses the external reference voltage source as the ADC reference voltage, it must add some decoupling and bypass capacitors, as shown in following figure.

An optional **ADCx\_TRG** pin is able to input the trigger signal for ADC input conversion and an optional **ADCx\_OUT** pin is used to output the internal ADC window detection status.

**Figure 7-4. ADC Application Circuit**

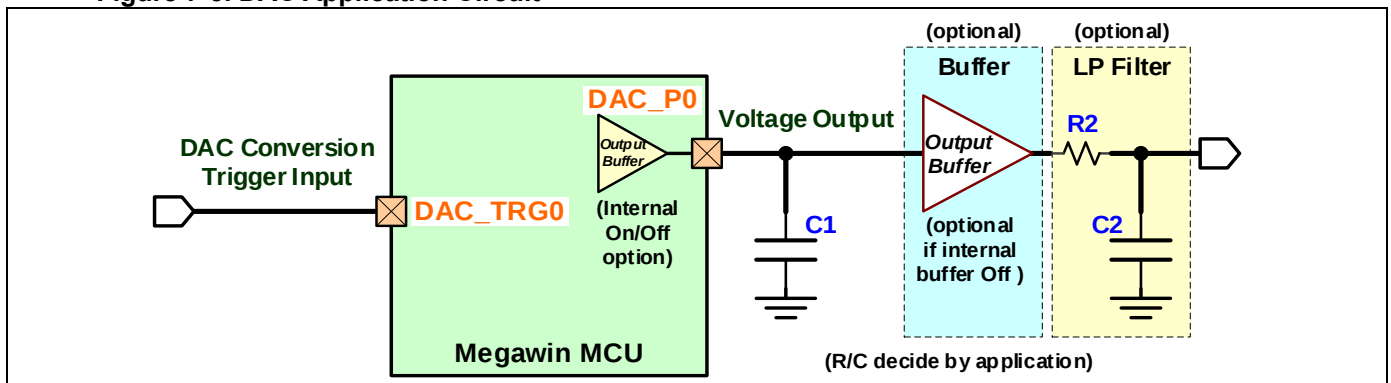


## 7.5. DAC Application Circuit

The DAC is built-in an internal output buffer which output resistive load is minimum 7.5Kohm. A capacitor (**C1**) is suggested and used to keep more stable output voltage. When the internal output buffer is enabled, the DAC output range is 0.2 volt to VDD-0.2 volt.

The external output buffer is suggested necessary if the output resistive load is over the 7.5Kohm. An external low-pass filter (**R2/C2**) is suggestion to be implemented in the application circuit for more better outputting performance. An optional **DAC\_TRG0** pin is able to input the trigger signal for DAC output conversion.

**Figure 7-5. DAC Application Circuit**



## 8. Electrical Characteristics

### 8.1. Parameter Glossary

Table 8-1. Parameter Glossary

| Symbol                                              | Definition                  | Descriptions                                                                                                                                           |
|-----------------------------------------------------|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Abbreviations for electrical characteristics</b> |                             |                                                                                                                                                        |
| <b>Min</b>                                          | Minimum value               | Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value. |
| <b>Max</b>                                          | Maximum value               | Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value. |
| <b>Typ</b>                                          | Typical value               | Unless otherwise specified, the value is based on TA=25 °C, VDD=5V.                                                                                    |
| <b>VDD</b>                                          | Power supply voltage        | The voltage range is specified in characteristics table or conditions column.                                                                          |
| <b>VSS</b>                                          | Power reference voltage     | Unless otherwise specified, all voltages are referred to VSS.                                                                                          |
| <b>TA</b>                                           | Ambient temperature         | The temperature range is specified in characteristics table or conditions column.                                                                      |
| <b>T<sub>PC</sub></b>                               | Peripheral clock cycle time | The peripheral input clock source may select APB, SYS or other clock. This clock frequency needs lower than 1/2 of the module process clock frequency. |

### 8.2. Absolute Maximum Rating

Table 8-2. Absolute Maximum Rating

| Parameter                                              | Rating           | Unit |
|--------------------------------------------------------|------------------|------|
| Ambient temperature under bias                         | -40 ~ +105       | °C   |
| Storage temperature                                    | -65 ~ + 150      | °C   |
| Voltage on any Port I/O Pin or RST with respect to VSS | -0.5 ~ VDD + 0.5 | Volt |
| Voltage on VDD with respect to VSS                     | -0.5 ~ +6.0      | Volt |
| Maximum total current through VDD and VSS              | 200              | mA   |
| Maximum output current sunk by any I/O pin             | 40               | mA   |

Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### 8.3. DC Characteristics

**Table 8-3. DC Characteristics**

VDD=5.0V±10%, VSS=0V, TA = 25 °C and execute NOP for each CPU cycle (unless otherwise specified)

| Symbol              | Parameter                                            | Conditions                                                   | Limits   |      |          | Unit            |
|---------------------|------------------------------------------------------|--------------------------------------------------------------|----------|------|----------|-----------------|
|                     |                                                      |                                                              | Min      | Typ  | Max      |                 |
|                     | Current Consumption                                  |                                                              |          |      |          |                 |
| IOP1                | ON(normal) mode operating current                    | TL1 (APB=AHB=32KHz) dhrystone                                |          | 0.10 |          | mA              |
| IOP2                |                                                      | TL2 (APB=AHB=12MHz) dhrystone                                |          | 3.5  |          | mA              |
| IOP3                |                                                      | TL3 (APB=AHB=24MHz) dhrystone + IP                           |          | 7.9  |          | mA              |
| IOP4                |                                                      | TL4 (APB=AHB=24MHz - XTAL) dhrystone + IP                    |          | 8.7  |          | mA              |
| IOP5                |                                                      | TL5 (APB=AHB=24MHz - EXTCK) dhrystone + IP                   |          | 7.7  |          | mA              |
| IOP6                |                                                      | TL6 (APB=AHB=48MHz) dhrystone + all IP                       |          | 14.0 |          | mA              |
| ISLP0               | SLEEP mode operating current (IWDT Enable)           | SL0 (ILRCO on: IWDT Disable, APB=AHB=32KHz)                  |          | 108  |          | uA              |
| ISLP1               |                                                      | SL1 (IHRCO on: APB=6MHz,AHB=3MHz)                            |          | 872  |          | uA              |
| ISLP2               |                                                      | SL2 (IHRCO on: APB=AHB=12MHz)                                |          | 1198 |          | uA              |
| ISLP3               |                                                      | SL3 (XTAL=12MHz: APB/AHB=6MHz/3MHz)                          |          | 1690 |          | uA              |
| ISLP4               |                                                      | SL4 (ILRCO on: APB=AHB=32KHz) with Low Power SLEEP mode      |          | 39   |          | uA              |
| ISTP0               | STOP mode operating current (LVR/BOD0/BOD1 Disabled) | ST0 (ILRCO off)                                              |          | 1.67 |          | uA              |
| ISTP1               |                                                      | ST1 (IWDT Enable, ILRCO=32KHz)                               |          | 4.10 |          | uA              |
| ISTP2               |                                                      | ST2 (RTC Enable, ILRCO=32KHz)                                |          | 4.00 |          | uA              |
| Wakeup Time         |                                                      |                                                              |          |      |          |                 |
| twk_SLP0            | Wakeup from SLEEP mode (Normal SLEEP mode)           | IHRCO/ILRCO on, wakeup by RTC event (APB Clock= IHRCO clock) |          | 5    | 6        | T <sub>PC</sub> |
| twk_SLP1            | Wakeup from SLEEP mode (Low Power SLEEP mode)        | IHRCO/ILRCO on, wakeup by RTC event (APB Clock= IHRCO clock) | 20       |      |          | us              |
| twk_STP0            | Wakeup from STOP mode                                | ILRCO on, wakeup by RTC event                                | 20       |      |          | us              |
| BOD Characteristics |                                                      |                                                              |          |      |          |                 |
| VLVR                | LVR detection level (VR0)                            | TA = -40℃ to +105℃                                           |          | 1.28 |          | Volt            |
| VBOD0               | BOD0 detection level (VR0)                           | TA = -40℃ to +105℃                                           | 1.40     |      | 1.45     | Volt            |
| IBOD0+LVR           | BOD0 and LVR Current Consumption                     | TA = 25℃                                                     |          |      | 3.5      | uA              |
| VBOD10              | BOD1 detection level for 2.0V                        | TA = -40℃ to +105℃                                           | 1.8(*1)  | 2.0  | 2.2(*1)  | Volt            |
| VBOD11              | BOD1 detection level for 2.4V                        | TA = -40℃ to +105℃                                           | 2.22(*1) | 2.4  | 2.62(*1) | Volt            |
| VBOD12              | BOD1 detection level for 3.7V                        | TA = -40℃ to +105℃                                           | 3.50     | 3.7  | 3.90     | Volt            |
| VBOD13              | BOD1 detection level for 4.2V                        | TA = -40℃ to +105℃                                           | 3.89(*1) | 4.2  | 4.59(*1) | Volt            |
| IBOD1               | BOD1 Current Consumption                             | TA = 25℃                                                     |          |      | 9.0      | uA              |
| VBOD2               | BOD2 detection level for 1.7V                        | TA = -40℃ to +105℃                                           | 1.65     | 1.70 | 1.75     | Volt            |
| IBOD2               | BOD2 Current Consumption                             | TA = 25℃                                                     |          |      | 9.0      | uA              |
| Operating Condition |                                                      |                                                              |          |      |          |                 |
| VPSR                | Power-on Slope Rate                                  | TA = -40℃ to +105℃                                           | 0.05     |      |          | V/ms            |
| VOP1                | CPU Operating Speed 0–48MHz                          | TA = -40℃ to +105℃                                           | 2.7      |      | 5.5      | Volt            |

|                        |                             |                      |            |  |            |             |
|------------------------|-----------------------------|----------------------|------------|--|------------|-------------|
| <b>V<sub>OP2</sub></b> | CPU Operating Speed 0–12MHz | TA = -40°C to +105°C | <b>1.8</b> |  | <b>5.5</b> | <b>Volt</b> |
|------------------------|-----------------------------|----------------------|------------|--|------------|-------------|

(\*1) Data based on characterization results, not tested in production.

T<sub>PC</sub>: APB clock cycle time, IP: internal peripheral modules, **all IP**: all test modules

TL3 ~ TL6: Measure current with IO toggle, **SL4**: Refer the wakeup time t<sub>WK\_SLP1</sub> as the low power SLEEP mode

**Table 8-4. Current Measurement Condition Level Definition Table**

| Chip Power State | ON Mode           |                  |                        |                  |                  |                      | SLEEP Mode        |                   |                   |                   |                   | STOP Mode         |                   |                   |
|------------------|-------------------|------------------|------------------------|------------------|------------------|----------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Test Level       | TL1               | TL2              | TL3                    | TL4              | TL5              | TL6                  | SL0               | SL1               | SL2               | SL3               | SL4               | ST0               | ST1               | ST2               |
| Symbol           | I <sub>OP1</sub>  | I <sub>OP2</sub> | I <sub>OP3</sub>       | I <sub>OP4</sub> | I <sub>OP5</sub> | I <sub>OP6</sub>     | I <sub>SLP0</sub> | I <sub>SLP1</sub> | I <sub>SLP2</sub> | I <sub>SLP3</sub> | I <sub>SLP4</sub> | I <sub>stp0</sub> | I <sub>stp1</sub> | I <sub>stp2</sub> |
| CPU State        | Normal            |                  |                        |                  |                  |                      | Sleep             |                   |                   |                   |                   | Deep Sleep        |                   |                   |
| CPU Code (*1)    | dhystone          | dhystone         | dhystone + normal code |                  |                  | dhystone+ heavy code | -                 | -                 | -                 | -                 | -                 | -                 | -                 | -                 |
| APB Clock        | 32KHz ILRCO       | 12MHz IHRCO      | 24MHz PLL/4            | 24MHz PLL/4      | 24MHz PLL/4      | 48MHz PLL/2          | 32KHz ILRCO       | 6MHz IHRCO/2      | 12MHz IHRCO       | 6MHz XTAL/2       | 32KHz ILRCO       | -                 | 32KHz ILRCO       | 32KHz ILRCO       |
| AHB/CPU Clock    | 32KHz APB         | 12MHz APB        | 24MHz APB              | 24MHz APB        | 24MHz APB        | 48MHz APB            | 32KHz APB         | 3MHz APB/2        | 12MHz APB         | 3MHz APB/2        | 32KHz APB         | -                 | 32KHz APB         | 32KHz APB         |
| ILRCO (32KHz)    | V                 | V                | V                      | V                | V                | V                    | V                 | V                 | V                 | V                 | V                 |                   | V                 | V                 |
| IHRCO (12MHz)    |                   | V                | V                      |                  |                  | V                    |                   | V                 | V                 |                   |                   |                   |                   |                   |
| XTAL (12MHz)     |                   |                  |                        | Medium           |                  |                      |                   |                   |                   | Medium            |                   |                   |                   |                   |
| EXTCK (12MHz)    |                   |                  |                        |                  | V                |                      |                   |                   |                   |                   |                   |                   |                   |                   |
| PLL              |                   |                  | V                      | V                | V                | V                    |                   |                   |                   |                   |                   |                   |                   |                   |
| LDO (*2)         | Normal            |                  |                        |                  |                  |                      | Normal            |                   |                   |                   |                   | Low Power         |                   |                   |
| LVR              | V                 | V                | V                      | V                | V                | V                    | V                 | V                 | V                 | V                 | V                 |                   |                   |                   |
| BOD0             | V                 | V                | V                      | V                | V                | V                    | V                 | V                 | V                 | V                 | V                 |                   |                   |                   |
| BOD1             |                   |                  | V                      | V                | V                | V                    |                   |                   |                   |                   |                   |                   |                   |                   |
| SLEEP Mode (*3)  |                   |                  |                        |                  |                  |                      | Normal            | Normal            | Normal            | Normal            | Low Power         |                   |                   |                   |
| ADC0             |                   |                  | CK_APB                 | CK_APB           | CK_APB           | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| CMP              |                   |                  | CK_APB                 | CK_APB           | CK_APB           | CK_APB               |                   | CK_APB            | CK_APB            | CK_APB            |                   |                   |                   |                   |
| RTC              |                   |                  | CK_UT                  | CK_UT            | CK_UT            | CK_UT                |                   |                   |                   |                   |                   |                   |                   | CK_UT             |
| IWDT             | CK_ILRCO          | CK_ILRCO         | CK_ILRCO               | CK_ILRCO         | CK_ILRCO         | CK_ILRCO             |                   | CK_ILRCO          | CK_ILRCO          | CK_ILRCO          |                   |                   | CK_ILRCO          |                   |
| WWDT             |                   |                  | CK_APB                 | CK_APB           | CK_APB           | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| TM00             | CK_APB            | CK_APB           | CK_APB                 | CK_APB           | CK_APB           | CK_APB               |                   | CK_APB            | CK_APB            | CK_APB            |                   |                   |                   |                   |
| TM01             |                   |                  |                        |                  |                  | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| TM10             |                   |                  | CK_APB                 | CK_APB           | CK_APB           | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| TM16             |                   |                  |                        |                  |                  | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| TM20             |                   |                  |                        |                  |                  | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| TM26             |                   |                  |                        |                  |                  | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| TM36             |                   |                  | CK_APB                 | CK_APB           | CK_APB           | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| I2C0             |                   |                  | CK_APB                 | CK_APB           | CK_APB           | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| I2C1             |                   |                  |                        |                  |                  | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| URT0             |                   |                  | CK_APB                 | CK_APB           | CK_APB           | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| URT1             |                   |                  |                        |                  |                  | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| URT2             |                   |                  |                        |                  |                  | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| SPI0             |                   |                  |                        |                  |                  | CK_APB               |                   |                   |                   |                   |                   |                   |                   |                   |
| IO Pins          | all Push-Pull Low |                  | IO Toggle              |                  |                  |                      | all Push-Pull Low |                   |                   |                   |                   | all Push-Pull Low |                   |                   |

**Note: (\*1)** [CPU Code]  
**dhystone**: CPU runs "Dhystone" benchmarks code.  
**normal code**: Set CK\_APB and CK\_AHB frequency by table. The module clock divider can be /4, /8 or others.  
**heavy code**: 1. Set CK\_APB and CK\_AHB frequency by table. The module clock set the highest frequency (module clock DIV=/2).  
2. Let the module operates as busy as possible and fills full data through the buffer. (EX: transfer 4 bytes for one transaction)  
**(\*2)** Normal: PW\_LDO\_ON=0, Low Power: PW\_LDO\_STP=1  
**(\*3)** Normal: PW\_WKSLP\_MDS=0, Low Power: PW\_WKSLP\_MDS=1

## 8.4. IO Characteristics

**Table 8-5. IO Characteristics**

VSS=0V, TA = 25 °C and execute NOP for each CPU cycle (unless otherwise specified)

| Symbol                     | Parameter                                                                                                  | Conditions                                        | Limits      |              |             | Unit |
|----------------------------|------------------------------------------------------------------------------------------------------------|---------------------------------------------------|-------------|--------------|-------------|------|
|                            |                                                                                                            |                                                   | Min         | Typ          | Max         |      |
| <b>V<sub>IH</sub></b>      | Input High voltage                                                                                         | Except RSTN,XIN/XOUT pins                         | <b>0.6</b>  |              |             | VDD  |
| <b>V<sub>IH_XOSC</sub></b> | Input High voltage (XIN)                                                                                   | XIN pin GPIO mode                                 | <b>0.75</b> |              |             | VDD  |
| <b>V<sub>IH_RST</sub></b>  | Input High voltage (RSTN)                                                                                  | RSTN pin reset/GPIO mode                          | <b>0.75</b> |              |             | VDD  |
| <b>V<sub>IL</sub></b>      | Input Low voltage                                                                                          | Except RSTN,XIN/XOUT pins                         |             |              | <b>0.15</b> | VDD  |
| <b>V<sub>IL_XOSC</sub></b> | Input Low voltage (XIN)                                                                                    | XIN pin GPIO mode                                 |             |              | <b>0.2</b>  | VDD  |
| <b>V<sub>IL_RST</sub></b>  | Input Low voltage (RSTN)                                                                                   | RSTN pin reset/GPIO mode                          |             |              | <b>0.2</b>  | VDD  |
| <b>VDD=5.0V</b>            |                                                                                                            |                                                   |             |              |             |      |
| <b>I<sub>IH</sub></b>      | Input High Leakage current                                                                                 | V <sub>PIN</sub> = VDD                            |             | <b>0.02</b>  | <b>0.1</b>  | uA   |
| <b>I<sub>IL</sub></b>      | Input Low Leakage current                                                                                  | V <sub>PIN</sub> = 0.4V                           |             | <b>0.01</b>  | <b>0.1</b>  | uA   |
| <b>I<sub>H2L</sub></b>     | Logic 1 to 0 input transition current<br>(quasi-bidirectional or input mode with on-chip pull-up resistor) | V <sub>PIN</sub> = 2.2V (V <sub>IH</sub> voltage) |             | <b>250</b>   | <b>500</b>  | uA   |
| <b>I<sub>OH1</sub></b>     | Output High current (push-pull output mode & Full level)                                                   | VDD=5.0V, V <sub>PIN</sub> = 2.4V                 |             | <b>38.5</b>  |             | mA   |
| <b>I<sub>OH2</sub></b>     | Output High current (push-pull output mode & 1/2 level)                                                    | VDD=5.0V, V <sub>PIN</sub> = 2.4V                 |             | <b>19.8</b>  |             | mA   |
| <b>I<sub>OH3</sub></b>     | Output High current (push-pull output mode & 1/4 level)                                                    | VDD=5.0V, V <sub>PIN</sub> = 2.4V                 |             | <b>10.1</b>  |             | mA   |
| <b>I<sub>OH4</sub></b>     | Output High current (push-pull output mode & 1/8 level)                                                    | VDD=5.0V, V <sub>PIN</sub> = 2.4V                 |             | <b>5.2</b>   |             | mA   |
| <b>I<sub>OL1</sub></b>     | Output Low current(Full level)                                                                             | VDD=5.0V, V <sub>PIN</sub> = 0.4V                 |             | <b>30.4</b>  |             | mA   |
| <b>I<sub>OL2</sub></b>     | Output Low current(1/2 level)                                                                              | VDD=5.0V, V <sub>PIN</sub> = 0.4V                 |             | <b>15.7</b>  |             | mA   |
| <b>I<sub>OL3</sub></b>     | Output Low current(1/4 level)                                                                              | VDD=5.0V, V <sub>PIN</sub> = 0.4V                 |             | <b>8.0</b>   |             | mA   |
| <b>I<sub>OL4</sub></b>     | Output Low current(1/8 level)                                                                              | VDD=5.0V, V <sub>PIN</sub> = 0.4V                 |             | <b>4.0</b>   |             | mA   |
| <b>R<sub>VWeak</sub></b>   | IO pin very weak pull-high resistance                                                                      |                                                   |             | <b>250</b>   |             | Kohm |
| <b>R<sub>PU</sub></b>      | IO pin pull-high resistance                                                                                | Except RSTN                                       |             | <b>13.3</b>  |             | Kohm |
| <b>R<sub>RST</sub></b>     | Internal reset pull-high resistance                                                                        | RSTN pin                                          |             | <b>250</b>   |             | Kohm |
| <b>TR1</b>                 | IO rising time (Normal mode and IO output drive strength is Full level)                                    | Except RSTN,XIN/XOUT pins<br>C load=30pF          |             | <b>13.7</b>  |             | ns   |
| <b>TR2</b>                 | IO rising time (Normal mode and IO output drive strength is 1/4 level)                                     | Except RSTN,XIN/XOUT pins<br>C load=30pF          |             | <b>28.9</b>  |             | ns   |
| <b>TR3</b>                 | IO rising time (High speed mode and IO output drive strength is Full level)                                | Except RSTN,XIN/XOUT pins<br>C load=30pF          |             | <b>5.58</b>  |             | ns   |
| <b>TR4</b>                 | IO rising time (High speed mode and IO output drive strength is 1/4 level)                                 | Except RSTN,XIN/XOUT pins<br>C load=30pF          |             | <b>26.8</b>  |             | ns   |
| <b>TR5</b>                 | IO rising time (XOUT GPIO mode)                                                                            | C load=30pF                                       |             | <b>5.60</b>  |             | ns   |
| <b>TR6</b>                 | IO rising time (XIN GPIO mode)                                                                             | C load=30pF                                       |             | <b>5.29</b>  |             | ns   |
| <b>TR7</b>                 | IO rising time (RSTIN GPIO mode)                                                                           | C load=30pF                                       |             | <b>7.36</b>  |             | ns   |
| <b>TF1</b>                 | IO falling time (Normal mode and IO output drive strength is Full level)                                   | Except RSTN,XIN/XOUT pins<br>C load=30pF          |             | <b>13.7</b>  |             | ns   |
| <b>TF2</b>                 | IO falling time (Normal mode and IO output drive strength is 1/4 level)                                    | Except RSTN,XIN/XOUT pins<br>C load=30pF          |             | <b>16.45</b> |             | ns   |
| <b>TF3</b>                 | IO falling time (High speed mode)                                                                          | Except RSTN,XIN/XOUT pins                         |             | <b>3.2</b>   |             | ns   |

|                          |                                                                                                         |                                                   |  |              |            |             |
|--------------------------|---------------------------------------------------------------------------------------------------------|---------------------------------------------------|--|--------------|------------|-------------|
|                          | and IO output drive strength is Full level)                                                             | C load=30pF                                       |  |              |            |             |
| <b>TF4</b>               | IO falling time (High speed mode and IO output drive strength is 1/4 level)                             | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>9.65</b>  |            | <b>ns</b>   |
| <b>TF5</b>               | IO falling time (XOUT GPIO mode)                                                                        | C load=30pF                                       |  | <b>3.1</b>   |            | <b>ns</b>   |
| <b>TF6</b>               | IO falling time (XIN GPIO mode)                                                                         | C load=30pF                                       |  | <b>2.6</b>   |            | <b>ns</b>   |
| <b>TF7</b>               | IO falling time (RSTIN GPIO mode)                                                                       | C load=30pF                                       |  | <b>3.0</b>   |            | <b>ns</b>   |
| <b>VDD=3.3V</b>          |                                                                                                         |                                                   |  |              |            |             |
| <b>I<sub>IH</sub></b>    | Input High Leakage current                                                                              | V <sub>PIN</sub> = VDD                            |  | <b>0.02</b>  | <b>0.1</b> | <b>uA</b>   |
| <b>I<sub>IL</sub></b>    | Input Low Leakage current                                                                               | V <sub>PIN</sub> = 0.4V                           |  | <b>0.01</b>  | <b>0.1</b> | <b>uA</b>   |
| <b>I<sub>H2L</sub></b>   | Logic 1 to 0 input transition current (quasi-bidirectional or input mode with on-chip pull-up resistor) | V <sub>PIN</sub> = 1.6V (V <sub>IH</sub> voltage) |  | <b>115</b>   | <b>150</b> | <b>uA</b>   |
| <b>I<sub>OH1</sub></b>   | Output High current (push-pull output mode & Full level)                                                | VDD=3.3V, V <sub>PIN</sub> = 2.4V                 |  | <b>13</b>    |            | <b>mA</b>   |
| <b>I<sub>OH2</sub></b>   | Output High current (push-pull output mode & 1/2 level)                                                 | VDD=3.3V, V <sub>PIN</sub> = 2.4V                 |  | <b>6.5</b>   |            | <b>mA</b>   |
| <b>I<sub>OH3</sub></b>   | Output High current (push-pull output mode & 1/4 level)                                                 | VDD=3.3V, V <sub>PIN</sub> = 2.4V                 |  | <b>3.5</b>   |            | <b>mA</b>   |
| <b>I<sub>OH4</sub></b>   | Output High current (push-pull output mode & 1/8 level)                                                 | VDD=3.3V, V <sub>PIN</sub> = 2.4V                 |  | <b>1.7</b>   |            | <b>mA</b>   |
| <b>I<sub>OL1</sub></b>   | Output Low current(Full level)                                                                          | VDD=3.3V, V <sub>PIN</sub> = 0.4V                 |  | <b>22</b>    |            | <b>mA</b>   |
| <b>I<sub>OL2</sub></b>   | Output Low current(1/2 level)                                                                           | VDD=3.3V, V <sub>PIN</sub> = 0.4V                 |  | <b>11.3</b>  |            | <b>mA</b>   |
| <b>I<sub>OL3</sub></b>   | Output Low current(1/4 level)                                                                           | VDD=3.3V, V <sub>PIN</sub> = 0.4V                 |  | <b>5.6</b>   |            | <b>mA</b>   |
| <b>I<sub>OL4</sub></b>   | Output Low current(1/8 level)                                                                           | VDD=3.3V, V <sub>PIN</sub> = 0.4V                 |  | <b>2.8</b>   |            | <b>mA</b>   |
| <b>R<sub>VWeak</sub></b> | IO pin very weak pull-high resistance                                                                   |                                                   |  | <b>420</b>   |            | <b>Kohm</b> |
| <b>R<sub>PU</sub></b>    | IO pin pull-high resistance                                                                             | Except RSTN                                       |  | <b>19.5</b>  |            | <b>Kohm</b> |
| <b>R<sub>RST</sub></b>   | Internal reset pull-high resistance                                                                     | RSTN pin                                          |  | <b>426</b>   |            | <b>Kohm</b> |
| <b>TR1</b>               | IO rising time (Normal mode and IO output drive strength is Full level)                                 | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>19.4</b>  |            | <b>ns</b>   |
| <b>TR2</b>               | IO rising time (Normal mode and IO output drive strength is 1/4 level)                                  | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>38.4</b>  |            | <b>ns</b>   |
| <b>TR3</b>               | IO rising time (High speed mode and IO output drive strength is Full level)                             | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>7.7</b>   |            | <b>ns</b>   |
| <b>TR4</b>               | IO rising time (High speed mode and IO output drive strength is 1/4 level)                              | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>35.5</b>  |            | <b>ns</b>   |
| <b>TR5</b>               | IO rising time (XOUT GPIO mode)                                                                         | C load=30pF                                       |  | <b>7.0</b>   |            | <b>ns</b>   |
| <b>TR6</b>               | IO rising time (XIN GPIO mode)                                                                          | C load=30pF                                       |  | <b>7.3</b>   |            | <b>ns</b>   |
| <b>TR7</b>               | IO rising time (RSTIN GPIO mode)                                                                        | C load=30pF                                       |  | <b>11.3</b>  |            | <b>ns</b>   |
| <b>TF1</b>               | IO falling time (Normal mode and IO output drive strength is Full level)                                | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>19.9</b>  |            | <b>ns</b>   |
| <b>TF2</b>               | IO falling time (Normal mode and IO output drive strength is 1/4 level)                                 | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>21.8</b>  |            | <b>ns</b>   |
| <b>TF3</b>               | IO falling time (High speed mode and IO output drive strength is Full level)                            | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>3.66</b>  |            | <b>ns</b>   |
| <b>TF4</b>               | IO falling time (High speed mode and IO output drive strength is 1/4 level)                             | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>12.76</b> |            | <b>ns</b>   |
| <b>TF5</b>               | IO falling time (XOUT GPIO mode)                                                                        | C load=30pF                                       |  | <b>4.2</b>   |            | <b>ns</b>   |
| <b>TF6</b>               | IO falling time (XIN GPIO mode)                                                                         | C load=30pF                                       |  | <b>3.1</b>   |            | <b>ns</b>   |

## MG32F02A128/A064

|                          |                                                                                                         |                                                   |  |              |            |             |
|--------------------------|---------------------------------------------------------------------------------------------------------|---------------------------------------------------|--|--------------|------------|-------------|
| <b>TF7</b>               | IO falling time (RSTIN GPIO mode)                                                                       | C load=30pF                                       |  | <b>3.8</b>   |            | <b>ns</b>   |
| <b>VDD=1.8V</b>          |                                                                                                         |                                                   |  |              |            |             |
| <b>I<sub>IH</sub></b>    | Input High Leakage current                                                                              | V <sub>PIN</sub> = VDD                            |  | <b>0.02</b>  | <b>0.1</b> | <b>uA</b>   |
| <b>I<sub>IL</sub></b>    | Input Low Leakage current                                                                               | V <sub>PIN</sub> = 0.4V                           |  | <b>0.01</b>  | <b>0.1</b> | <b>uA</b>   |
| <b>I<sub>H2L</sub></b>   | Logic 1 to 0 input transition current (quasi-bidirectional or input mode with on-chip pull-up resistor) | V <sub>PIN</sub> = 1.1V (V <sub>IH</sub> voltage) |  | <b>27.1</b>  |            | <b>uA</b>   |
| <b>I<sub>OH1</sub></b>   | Output High current (push-pull output mode & Full level)                                                | VDD=1.8V, V <sub>PIN</sub> = 1.4V                 |  | <b>3.3</b>   |            | <b>mA</b>   |
| <b>I<sub>OH2</sub></b>   | Output High current (push-pull output mode & 1/2 level)                                                 | VDD=1.8V, V <sub>PIN</sub> = 1.4V                 |  | <b>1.7</b>   |            | <b>mA</b>   |
| <b>I<sub>OH3</sub></b>   | Output High current (push-pull output mode & 1/4 level)                                                 | VDD=1.8V, V <sub>PIN</sub> = 1.4V                 |  | <b>0.9</b>   |            | <b>mA</b>   |
| <b>I<sub>OH4</sub></b>   | Output High current (push-pull output mode & 1/8 level)                                                 | VDD=1.8V, V <sub>PIN</sub> = 1.4V                 |  | <b>0.45</b>  |            | <b>mA</b>   |
| <b>I<sub>OL1</sub></b>   | Output Low current(Full level)                                                                          | VDD=1.8V, V <sub>PIN</sub> = 0.4V                 |  | <b>10.7</b>  |            | <b>mA</b>   |
| <b>I<sub>OL2</sub></b>   | Output Low current(1/2 level)                                                                           | VDD=1.8V, V <sub>PIN</sub> = 0.4V                 |  | <b>5.4</b>   |            | <b>mA</b>   |
| <b>I<sub>OL3</sub></b>   | Output Low current(1/4 level)                                                                           | VDD=1.8V, V <sub>PIN</sub> = 0.4V                 |  | <b>2.7</b>   |            | <b>mA</b>   |
| <b>I<sub>OL4</sub></b>   | Output Low current(1/8 level)                                                                           | VDD=1.8V, V <sub>PIN</sub> = 0.4V                 |  | <b>1.3</b>   |            | <b>mA</b>   |
| <b>R<sub>VWeak</sub></b> | IO pin very weak pull-high resistance                                                                   |                                                   |  | <b>1080</b>  |            | <b>Kohm</b> |
| <b>R<sub>PU</sub></b>    | IO pin pull-high resistance                                                                             | Except RSTN                                       |  | <b>45</b>    |            | <b>Kohm</b> |
| <b>R<sub>RST</sub></b>   | Internal reset pull-high resistance                                                                     | RSTN pin                                          |  | <b>1100</b>  |            | <b>Kohm</b> |
| <b>TR1</b>               | IO rising time (Normal mode and IO output drive strength is Full level)                                 | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>38.6</b>  |            | <b>ns</b>   |
| <b>TR2</b>               | IO rising time (Normal mode and IO output drive strength is 1/4 level)                                  | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>68</b>    |            | <b>ns</b>   |
| <b>TR3</b>               | IO rising time (High speed mode and IO output drive strength is Full level)                             | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>15.78</b> |            | <b>ns</b>   |
| <b>TR4</b>               | IO rising time (High speed mode and IO output drive strength is 1/4 level)                              | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>62.4</b>  |            | <b>ns</b>   |
| <b>TR5</b>               | IO rising time (XOUT GPIO mode)                                                                         | C load=30pF                                       |  | <b>15.1</b>  |            | <b>ns</b>   |
| <b>TR6</b>               | IO rising time (XIN GPIO mode)                                                                          | C load=30pF                                       |  | <b>15.9</b>  |            | <b>ns</b>   |
| <b>TR7</b>               | IO rising time (RSTIN GPIO mode)                                                                        | C load=30pF                                       |  | <b>22.7</b>  |            | <b>ns</b>   |
| <b>TF1</b>               | IO falling time (Normal mode and IO output drive strength is Full level)                                | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>40.8</b>  |            | <b>ns</b>   |
| <b>TF2</b>               | IO falling time (Normal mode and IO output drive strength is 1/4 level)                                 | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>42.3</b>  |            | <b>ns</b>   |
| <b>TF3</b>               | IO falling time (High speed mode and IO output drive strength is Full level)                            | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>7.5</b>   |            | <b>ns</b>   |
| <b>TF4</b>               | IO falling time (High speed mode and IO output drive strength is 1/4 level)                             | Except RSTN,XIN/XOUT pins<br>C load=30pF          |  | <b>40.5</b>  |            | <b>ns</b>   |
| <b>TF5</b>               | IO falling time (XOUT GPIO mode)                                                                        | C load=30pF                                       |  | <b>6.1</b>   |            | <b>ns</b>   |
| <b>TF6</b>               | IO falling time (XIN GPIO mode)                                                                         | C load=30pF                                       |  | <b>6.1</b>   |            | <b>ns</b>   |
| <b>TF7</b>               | IO falling time (RSTIN GPIO mode)                                                                       | C load=30pF                                       |  | <b>7.9</b>   |            | <b>ns</b>   |

## 8.5. External Clock Characteristics

**Table 8-6. External Clock Characteristics**

VDD=1.8V ~ 5.5V, VSS=0V, TA = -40°C ~ +105°C (unless otherwise specified)

| Symbol                      | Parameter                                 | Conditions                | Crystal     |             | External Clock |             | Unit              |
|-----------------------------|-------------------------------------------|---------------------------|-------------|-------------|----------------|-------------|-------------------|
|                             |                                           |                           | Min         | Max         | Min            | Max         |                   |
| <b>f<sub>xosc</sub></b>     | Oscillator Frequency                      | VDD = 1.8V ~ 5.5V         | <b>4</b>    | <b>25</b>   |                | <b>36</b>   | MHz               |
| <b>t<sub>xosc</sub></b>     | Clock Period                              |                           | <b>40</b>   |             | <b>27.7</b>    |             | ns                |
| <b>t<sub>H_XOSC</sub></b>   | High Time                                 |                           | <b>0.4T</b> | <b>0.6T</b> | <b>0.4T</b>    | <b>0.6T</b> | t <sub>xosc</sub> |
| <b>t<sub>L_XOSC</sub></b>   | Low Time                                  |                           | <b>0.4T</b> | <b>0.6T</b> | <b>0.4T</b>    | <b>0.6T</b> | t <sub>xosc</sub> |
| <b>t<sub>r_XOSC</sub></b>   | Rise Time                                 |                           |             |             |                | <b>7</b>    | ns                |
| <b>t<sub>f_XOSC</sub></b>   | Fall Time                                 |                           |             |             |                | <b>7</b>    | ns                |
| <b>t<sub>START12M</sub></b> | Start-up Time                             | Xtal = 12MHz, CL = 20pF   |             | <b>2</b>    |                |             | ms                |
| <b>t<sub>START32K</sub></b> | Start-up Time                             | Xtal = 32KHz, CL = 12.5pF |             | <b>0.8</b>  |                |             | s                 |
| <b>R<sub>FB12M</sub></b>    | Feedback resistor value of crystal buffer | Xtal = 12MHz, CL = 20pF   | <b>90</b>   | <b>160</b>  |                |             | KΩ                |

## 8.6. PLL Characteristics

**Table 8-7. PLL Characteristics**

| Parameter                        | Conditions           | Limits          |                  |                 | Unit |
|----------------------------------|----------------------|-----------------|------------------|-----------------|------|
|                                  |                      | Min             | Typ              | Max             |      |
| Supply Voltage                   |                      | <b>1.35</b>     | <b>1.50</b>      | <b>1.65</b>     | Volt |
| Input Clock Frequency Range      | TA = -40°C to +105°C | <b>4.0 (*1)</b> |                  | <b>8.5 (*1)</b> | MHz  |
| Output Clock Frequency Range     | TA = -40°C to +105°C | <b>68</b>       |                  | <b>180</b>      | MHz  |
| PLL Locking Time                 | TA = -40°C to +105°C |                 | <b>14.3 (*2)</b> |                 | us   |
| PLL Current Consumption          | TA = +25°C, VDD=5.0V |                 | <b>0.30</b>      |                 | mA   |
| PLL Period Jitter (Peak-to-Peak) | TA = -40°C to +105°C |                 | <b>720</b>       | <b>1000</b>     | ps   |

(\*1) Data guaranteed by design, not tested in production.

(\*2) Data based on characterization results, not tested in production.

## 8.7. IHRCO Characteristics

**Table 8-8. IHRCO Characteristics**

| Parameter                                       | Conditions           | Limits          |                |                 | Unit |
|-------------------------------------------------|----------------------|-----------------|----------------|-----------------|------|
|                                                 |                      | Min             | Typ            | Max             |      |
| Supply Voltage                                  |                      | <b>1.8</b>      | <b>5.0</b>     | <b>5.5</b>      | Volt |
| IHRCO0 Frequency                                | TA = +25°C           |                 | <b>12</b>      |                 | MHz  |
| IHRCO1 Frequency                                | TA = +25°C           |                 | <b>11.0592</b> |                 | MHz  |
| IHRCO0 Frequency Deviation (factory calibrated) | TA = +25°C           | <b>-1.0</b>     |                | <b>+1.0</b>     | %    |
|                                                 | TA = -40°C to +105°C | <b>-4.0(*1)</b> |                | <b>+3.0(*1)</b> | %    |
| IHRCO1 Frequency Deviation (factory calibrated) | TA = +25°C           | <b>-1.0</b>     |                | <b>+1.0</b>     | %    |
|                                                 | TA = -40°C to +105°C | <b>-4.0(*1)</b> |                | <b>+3.0(*1)</b> | %    |
| IHRCO Start-up Time                             | TA = 25°C            |                 |                | <b>5(*1)</b>    | us   |
| IHRCO Current Consumption                       | TA = +25°C, VDD=5.0V |                 | <b>0.35</b>    |                 | mA   |

(\*1) Data based on characterization results, not tested in production.

## 8.8. ILRCO Characteristics

Table 8-9. ILRCO Characteristics

| Parameter                                         | Conditions           | Limits  |     |         | Unit |
|---------------------------------------------------|----------------------|---------|-----|---------|------|
|                                                   |                      | Min     | Typ | Max     |      |
| Supply Voltage                                    |                      | 1.8     | 5.0 | 5.5     | Volt |
| ILRCO Frequency                                   | TA = +25°C           |         | 32  |         | KHz  |
| ILRCO Frequency Deviation<br>(factory calibrated) | TA = +25°C, VDD=5.0V | -4      |     | +4      | %    |
|                                                   | TA = -40°C to +105°C | -15(*1) |     | +15(*1) | %    |
| ILRCO Current Consumption                         | TA = +25°C, VDD=5.0V |         |     | 2       | uA   |

(1) Data based on characterization results, not tested in production.

## 8.9. LDO Characteristics

Table 8-10. LDO Characteristics

VDD=5.0V±10%, VSS=0V, TA = -40°C ~ +105 °C

| Symbol       | Parameter                    | Conditions                                         | Limits |        |     | Unit |
|--------------|------------------------------|----------------------------------------------------|--------|--------|-----|------|
|              |                              |                                                    | Min    | Typ    | Max |      |
| Supply Range |                              |                                                    |        |        |     |      |
| VDD          | Supply Voltage               | Normal Mode, IOUT=20mA                             | 1.8    | 5.0    | 5.5 | V    |
| General      |                              |                                                    |        |        |     |      |
| VR0          | LDO Output Voltage (VR0 pin) | ON(Normal) mode                                    |        | 1.60   |     | Volt |
|              |                              | Low power mode (VDD=1.8V~5.5V), TA = -40℃ ~ +105 ℃ |        | 1.35   |     | Volt |
| IQ           | Current                      | VDD=1.7V~5.0V, Temp.= 25℃                          |        | 30     |     | uA   |
|              |                              | VDD=1.7V~5.0V, Temp.= -40℃ ~ +105℃                 |        | 50(*1) |     | uA   |
| VDROP        | Dropout Voltage (VDD-VR0)    | IOUT=40mA, VDD=2.0V~5.5V (VR0 =1.60V +/-5%)        | 530    |        |     | mV   |
|              |                              | IOUT=30mA, VDD=1.9V~5.5V (VR0 =1.60V +/-5%)        | 420    |        |     | mV   |
|              |                              | IOUT=20mA, VDD=1.8V~5.5V (VR0 =1.60V +/-5%)        | 310    |        |     | mV   |
| IOUT         | Max output current           | VDD=5.0V                                           | 50     |        |     | mA   |
|              |                              | VDD=3.6V                                           | 50     |        |     | mA   |
|              |                              | VDD=2.0V                                           | 40     |        |     | mA   |
|              |                              | VDD=1.9V                                           | 30     |        |     | mA   |
|              |                              | VDD=1.8V                                           | 20     |        |     | mA   |

(1) Data based on characterization results, not tested in production.

## 8.10. Flash Characteristics

Table 8-11. Flash Characteristics

VDD=5.0V±10%, VSS=0V, TA = -40°C ~ +105 °C

| Parameter                           | Conditions | Limits |     |     | Unit  |
|-------------------------------------|------------|--------|-----|-----|-------|
|                                     |            | Min    | Typ | Max |       |
| Supply Voltage                      |            | 1.8    |     | 5.5 | Volt  |
| Flash Write (Erase/Program) Voltage |            | 1.8    |     | 5.5 | Volt  |
| Flash Erase/Program Cycle           |            | 20000  |     |     | Times |
| Flash Data Retention                | TA = +25°C | 100    |     |     | Year  |

## 8.11. ADC Characteristics

Table 8-12. ADC Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C, C<sub>LOAD</sub>=10pF, Gain=x1 (unless otherwise specified)

| Symbol                | Parameter                       | Conditions                                                                                | Limits |      |     | Unit |
|-----------------------|---------------------------------|-------------------------------------------------------------------------------------------|--------|------|-----|------|
|                       |                                 |                                                                                           | Min    | Typ  | Max |      |
| Supply Range          |                                 |                                                                                           |        |      |     |      |
| VDDA                  | Analog Supply Voltage           |                                                                                           | 2.4    | 5.0  | 5.5 | Volt |
| IADC_ON               | Operation Current - normal      |                                                                                           |        | 1200 |     | uA   |
| IADC_OFF              | Operation Current - power-down  |                                                                                           |        | 0.1  |     | uA   |
| ADC Static Parameters |                                 |                                                                                           |        |      |     |      |
| Bits                  | Resolution                      |                                                                                           |        |      | 12  | bits |
| INL                   | Integral nonlinearity (INL)     | VREF = 5V, VDD = 5V,<br>1.5Msps Conversion Rate<br>(sampling clock = 36 MHz/24<br>clocks) |        | ±7   |     | LSB  |
| INL                   | Integral nonlinearity (INL)     | VREF = 5V, VDD = 5V,<br>1Msps Conversion Rate<br>(sampling clock = 24 MHz/24<br>clocks)   |        | ±6   |     | LSB  |
| INL                   | Integral nonlinearity (INL)     | VREF = 5V, VDD = 5V,<br>1Msps Conversion Rate<br>(sampling clock = 30 MHz/30<br>clocks)   |        | ±6   |     | LSB  |
| DNL                   | Differential nonlinearity (DNL) | VREF = 5V, VDD = 5V,<br>1.5Msps Conversion Rate<br>(sampling clock = 36 MHz/24<br>clocks) | -1     | 2.5  |     | LSB  |
| DNL                   | Differential nonlinearity (DNL) | VREF = 5V, VDD = 5V,<br>1Msps Conversion Rate<br>(sampling clock = 36 MHz/24<br>clocks)   | -1     | 2.5  |     | LSB  |
| DNL                   | Differential nonlinearity (DNL) | VREF = 5V, VDD = 5V,<br>1Msps Conversion Rate<br>(sampling clock = 48 MHz/30<br>clocks)   | -1     | 2.5  |     | LSB  |
| E <sub>OFFSET</sub>   | Offset error                    | VREF = 5V, VDD = 5V,<br>1.5Msps Conversion Rate<br>(sampling clock = 36 MHz/24<br>clocks) |        | ±4   |     | LSB  |
| E <sub>OFFSET</sub>   | Offset error                    | VREF = 5V, VDD = 5V,<br>1Msps Conversion Rate<br>(sampling clock = 24 MHz/24<br>clocks)   |        | ±4   |     | LSB  |
| E <sub>OFFSET</sub>   | Offset error                    | VREF = 5V, VDD = 5V,<br>1Msps Conversion Rate<br>(sampling clock = 30 MHz/30<br>clocks)   |        | ±4   |     | LSB  |

|                                    |                                                                         |                                                                                           |             |             |                        |               |
|------------------------------------|-------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|-------------|-------------|------------------------|---------------|
| <b>E<sub>FS</sub></b>              | Full scale error                                                        | VREF = 5V, VDD = 5V,<br>1.5Msps Conversion Rate<br>(sampling clock = 36 MHz/24<br>clocks) |             | <b>±14</b>  |                        | <b>LSB</b>    |
| <b>E<sub>FS</sub></b>              | Full scale error                                                        | VREF = 5V, VDD = 5V,<br>1Msps Conversion Rate<br>(sampling clock = 24 MHz/24<br>clocks)   |             | <b>±10</b>  |                        | <b>LSB</b>    |
| <b>E<sub>FS</sub></b>              | Full scale error                                                        | VREF = 5V, VDD = 5V,<br>1Msps Conversion Rate<br>(sampling clock = 30 MHz/30<br>clocks)   |             | <b>±10</b>  |                        | <b>LSB</b>    |
| <b>ADC Input and DC Characters</b> |                                                                         |                                                                                           |             |             |                        |               |
| <b>V<sub>AIN</sub></b>             | ADC input voltage range (Single Ended)                                  | gain = 1.0                                                                                | <b>0</b>    |             | <b>V<sub>ref</sub></b> | <b>Volt</b>   |
| <b>C<sub>LOAD</sub></b>            | Input capacitance                                                       |                                                                                           |             | <b>5</b>    |                        | <b>pF</b>     |
| <b>V<sub>XREF</sub></b>            | External ADC reference voltage                                          |                                                                                           | <b>2.4</b>  |             | <b>V<sub>DDA</sub></b> | <b>Volt</b>   |
| <b>V<sub>DDIREF</sub></b>          | Supply Voltage range for V <sub>IREF</sub>                              |                                                                                           | <b>2.7</b>  |             | <b>5.5</b>             | <b>Volt</b>   |
| <b>V<sub>IREF</sub></b>            | Internal ADC reference voltage                                          | -40 °C < < 105 °C                                                                         |             | <b>2.40</b> |                        | <b>Volt</b>   |
|                                    | Internal ADC reference voltage spread over<br>the temperature range     | -40 °C < < 105 °C<br>V <sub>IREF</sub> = 2.40V at 25°C                                    |             | <b>40</b>   |                        | <b>mV</b>     |
| <b>V<sub>BUF</sub></b>             | Internal VBUF reference voltage                                         | -40 °C < < 105 °C                                                                         | <b>1.38</b> | <b>1.40</b> | <b>1.42</b>            | <b>Volt</b>   |
|                                    | Internal VBUF reference voltage spread over<br>the temperature range    | -40 °C < < 105 °C<br>V <sub>BUF</sub> = 1.40V at 25°C                                     |             | <b>30</b>   |                        | <b>mV</b>     |
| <b>T<sub>ADEN</sub></b>            | ADC enable time                                                         |                                                                                           |             | <b>5</b>    |                        | <b>us</b>     |
| <b>ADC Conversion Parameters</b>   |                                                                         |                                                                                           |             |             |                        |               |
| <b>F<sub>s</sub></b>               | Sampling clock                                                          |                                                                                           |             |             | <b>48</b>              | <b>MHz</b>    |
| <b>F<sub>Conv</sub></b>            | Conversion rate                                                         | VDDA = 5.5 ~ 4.0 V                                                                        |             |             | <b>1500</b>            | <b>Ksps</b>   |
|                                    |                                                                         | VDDA = 4.0 ~ 2.4 V                                                                        |             |             | <b>1000</b>            | <b>Ksps</b>   |
| <b>T<sub>Conv</sub></b>            | Conversion time in conversion clock<br>(not including acquisition time) | ADC0_CONV_TIME=0                                                                          |             | <b>24</b>   |                        | <b>clocks</b> |
|                                    |                                                                         | ADC0_CONV_TIME=1                                                                          |             | <b>30</b>   |                        | <b>clocks</b> |

## 8.12. ADC PGA Characteristics

**Table 8-13. ADC PGA Characteristics**

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C (unless otherwise specified)

| Symbol             | Parameter                 | Conditions                                                                                          | Limits |      |            | Unit |
|--------------------|---------------------------|-----------------------------------------------------------------------------------------------------|--------|------|------------|------|
|                    |                           |                                                                                                     | Min    | Typ  | Max        |      |
| Supply Range       |                           |                                                                                                     |        |      |            |      |
| VDDA               | Analog Supply Voltage     |                                                                                                     | 2.4    | 5.0  | 5.5        | Volt |
|                    | DC Characteristics        |                                                                                                     |        |      |            |      |
| V <sub>OS2</sub>   | input offset voltage      | With Calibration<br>Gain=x1                                                                         | -6     |      | 10         | mV   |
| V <sub>CM_IN</sub> | Input Common-mode Voltage | VDDA>3.0V,Gain=x1,as a unit gain buffer                                                             | 0.03   |      | VDDA/2+0.5 | V    |
|                    |                           | VDDA<3.0V,Gain=x1,as a unit gain buffer                                                             | 0.03   |      | VDDA/2     | V    |
| I <sub>Q</sub>     | Ground Current            | VDDA=5.0V, VIN= VDDA/2;<br>VOUT=VDDA/2, Gain=x1<br>(RFB=120KΩ current Not included when<br>Gain=x1) |        | 1150 |            | uA   |
| AC Characteristics |                           |                                                                                                     |        |      |            |      |

|            |                              |                  |  |            |  |      |
|------------|------------------------------|------------------|--|------------|--|------|
| <b>SR</b>  | Slew rate (*1)               | Normal Operation |  | <b>3.5</b> |  | V/us |
| <b>UGF</b> | PGA Bandwidth Frequency (*2) | Normal Operation |  | <b>10</b>  |  | MHz  |

(\*1) Data guaranteed by design, not tested in production.

(\*2) The UGF will be divided by the GAIN setting. (ex: Ideal UGF will be 10MHz/4 when PGA gain=4)

### 8.13. Analog Comparator Characteristics

**Table 8-14. Analog Comparator Characteristics**

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C (unless otherwise specified)

| Symbol       | Parameter                           | Conditions                            | Limits |     |         | Unit |
|--------------|-------------------------------------|---------------------------------------|--------|-----|---------|------|
|              |                                     |                                       | Min    | Typ | Max     |      |
| Supply Range |                                     |                                       |        |     |         |      |
| VDDA         | Analog Supply Voltage               | -40°C ~ +105°C                        | 2.0    | 5.0 | 5.5     | Volt |
| ICOMP0       | Operation Current - CMP0            | High response time without IVREF (*1) |        | 9   |         | uA   |
|              |                                     | High response time with IVREF (*1)    |        | 210 |         | uA   |
|              |                                     | Low response time                     |        | 2   |         | uA   |
| ICOMP1       | Operation Current - CMP1            | High response time without IVREF (*1) |        | 9   |         | uA   |
|              |                                     | High response time with IVREF (*1)    |        | 210 |         | uA   |
|              |                                     | Low response time                     |        | 2   |         | uA   |
|              | Analog Comparator Core              |                                       |        |     |         |      |
| VOS          | Input Offset Voltage                |                                       | -5     | 15  |         | mV   |
| VCM          | Input Common Mode Voltage           |                                       | 50     |     | VDDA-50 | mV   |
| VHYS         | Comparator hysteresis               | Disable Hysteresis                    |        | 0   |         | mV   |
|              | Input voltage range 50mV ~ VDD-50mV | High response time                    |        | 11  |         | mV   |
|              |                                     | Low response time                     |        | 9   |         | mV   |
| TRT          | Response time                       | High response time - Falling          |        | 230 |         | ns   |
|              |                                     | High response time - Rising           |        | 200 |         | ns   |
|              |                                     | Low response time - Falling           |        | 0.7 |         | us   |
|              |                                     | Low response time – Rising            |        | 0.7 |         | us   |
| tPWON        | Power on Time (from power-down)     | High response time                    |        | 550 |         | ns   |
|              |                                     | Low response time                     |        | 15  |         | us   |
| RU           | Unit Resistance                     |                                       |        | 390 |         | ohm  |

(\*1) IVREF : Internal voltage reference circuit

### 8.14. Temperature Sensor Characteristics

**Table 8-15. Temperature Characteristics**

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C (unless otherwise specified)

| Symbol                            | Parameter               | Conditions     | Limits |     |     | Unit  |
|-----------------------------------|-------------------------|----------------|--------|-----|-----|-------|
|                                   |                         |                | Min    | Typ | Max |       |
| Supply Range                      |                         |                |        |     |     |       |
| VDDA                              | Analog Supply Voltage   | calculate VREF | 2.4    | 5.0 | 5.5 | Volt  |
| Temperature Conversion Parameters |                         |                |        |     |     |       |
| TRANG                             | Temperature range       |                | -40    |     | 125 | °C    |
| SlopeAVG                          | Linearity (curve slope) |                | 2.4    |     | 2.7 | mV/°C |

## MG32F02A128/A064

|                            |                      |                   |     |     |     |    |
|----------------------------|----------------------|-------------------|-----|-----|-----|----|
| <b>V<sub>0</sub></b>       | Voltage at 0 °C (*1) | TA = 0°C (± 5 °C) | 710 | 750 | 780 | mv |
|                            | Accuracy             |                   | -3  | ±2  | +4  | °C |
| <b>t<sub>START</sub></b>   | Startup time         |                   | 20  | 25  | 30  | ms |
| <b>I<sub>TEMP_ON</sub></b> | Operation current    |                   |     | 280 |     | uA |

(\*1) Data based on characterization results, not tested in production.

### 8.15. DAC Characteristics

**Table 8-16. DAC Characteristics**

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C, TT case

| Symbol                    | Parameter                                    | Conditions                                                                                                                                                                | Limits |       |         | Unit  |
|---------------------------|----------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------|---------|-------|
|                           |                                              |                                                                                                                                                                           | Min    | Typ   | Max     |       |
| Supply Range              |                                              |                                                                                                                                                                           |        |       |         |       |
| VDDA                      | Analog Supply Voltage (VDDA)                 | VDD = 2.4V~5.5V                                                                                                                                                           | 2.4    |       | 5.5     | Volt  |
| DAC Static Parameters     |                                              |                                                                                                                                                                           |        |       |         |       |
|                           | Resolution                                   |                                                                                                                                                                           |        |       | 12      | bits  |
| DNL                       | Differential nonlinearity (DNL)              | DAC Buffer OFF                                                                                                                                                            |        | ±2.25 |         | LSB   |
| DNL                       | Differential nonlinearity (DNL)              | DAC Buffer ON                                                                                                                                                             |        | ±2    |         | LSB   |
| INL                       | Integral nonlinearity (INL)                  | DAC Buffer OFF                                                                                                                                                            | -7     |       | 2       | LSB   |
| INL                       | Integral nonlinearity (INL)                  | DAC Buffer ON                                                                                                                                                             | -13    |       | 2       | LSB   |
| E <sub>OFFSET</sub>       | Offset error                                 | DAC Buffer OFF                                                                                                                                                            | -1     |       | 6       | LSB   |
| E <sub>OFFSET</sub>       | Offset error                                 | DAC Buffer ON                                                                                                                                                             | -1     |       | 30      | LSB   |
| E <sub>GAIN</sub>         | Gain error (Full scale error - Offset Error) | DAC Buffer OFF                                                                                                                                                            |        | ±2    |         | LSB   |
| E <sub>GAIN</sub>         | Gain error (Full scale error - Offset Error) | DAC Buffer ON                                                                                                                                                             |        | ±2    |         | LSB   |
|                           | DAC DC Characters                            |                                                                                                                                                                           |        |       |         |       |
| FSR                       | Full scale range                             | DAC Buffer ON                                                                                                                                                             | 0.2    |       | VDD-0.2 | Volt  |
| R <sub>LOAD</sub>         | Resistive load with buffer ON                |                                                                                                                                                                           | 7.5    |       |         | Kohm  |
| R <sub>o</sub>            | Resistive load with buffer OFF               | VDD=2.4V                                                                                                                                                                  | 13     |       |         | Kohm  |
|                           |                                              | VDD=3.3V                                                                                                                                                                  | 17     |       |         | Kohm  |
|                           |                                              | VDD=5.5V                                                                                                                                                                  | 20     |       |         | Kohm  |
| C <sub>LOAD</sub>         | Capacitive load                              |                                                                                                                                                                           |        |       | 50      | pF    |
| I <sub>DAC</sub>          | DAC operation current                        | DAC Buffer OFF                                                                                                                                                            | 0.65   | 0.73  | 0.80    | uA    |
|                           |                                              | DAC Buffer ON                                                                                                                                                             | 1.00   | 1.17  | 1.30    | uA    |
| I <sub>OFF</sub>          | DAC power-down current                       |                                                                                                                                                                           |        |       | 1       | uA    |
| DAC Conversion Parameters |                                              |                                                                                                                                                                           |        |       |         |       |
| F <sub>s</sub>            | Sampling Clock                               |                                                                                                                                                                           |        |       | 1       | MHz   |
| F <sub>CONV</sub>         | Conversion Rate                              | C <sub>LOAD</sub> ≤ 50 pF, R <sub>LOAD</sub> ≥ 5 KΩ<br>DAC output change from input code i to i+1 LSB                                                                     |        |       | 1       | Msp/s |
| T <sub>SETTLING</sub>     | Settling Time                                | C <sub>LOAD</sub> ≤ 50 pF, R <sub>LOAD</sub> ≥ 5 KΩ<br>DAC output change from input code i to i+1 LSB                                                                     |        | 540   |         | ns    |
|                           |                                              | C <sub>LOAD</sub> ≤ 50 pF, R <sub>LOAD</sub> ≥ 5 KΩ<br>Input code transition between the lowest and the highest input codes when DAC output reaches final value +/- 1 LSB |        | 2     | 4       | us    |
| T <sub>START</sub>        | Startup time after DAC ON                    |                                                                                                                                                                           |        |       | 10      | us    |

## 8.16. UART Characteristics

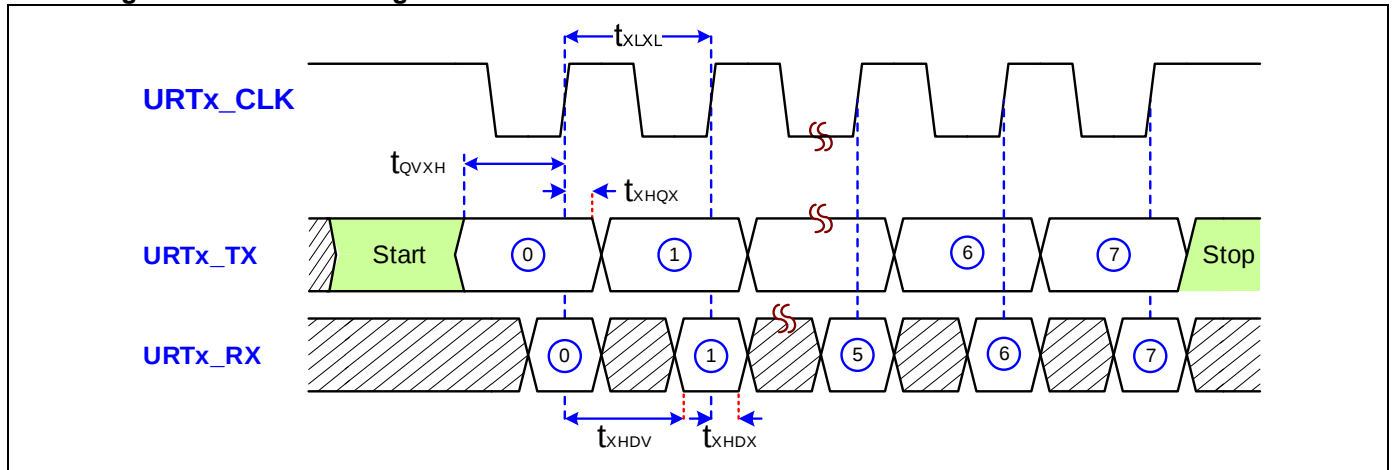
**Table 8-17. UART Characteristics**

VDD=5.0V±10%, VSS=0V, TA = -40°C ~ +105°C (unless otherwise specified)

| Symbol                             | Parameter                                | Conditions      | Limits              |     |                     | Unit            |
|------------------------------------|------------------------------------------|-----------------|---------------------|-----|---------------------|-----------------|
|                                    |                                          |                 | Min                 | Typ | Max                 |                 |
| UART Mode                          |                                          |                 |                     |     |                     |                 |
| f <sub>CK</sub>                    | Serial Port Clock Frequency              |                 |                     |     | 6                   | MHz             |
| t <sub>LXL</sub>                   | Serial Port Clock Cycle Time             |                 | 4                   |     |                     | T <sub>PC</sub> |
| t <sub>QVXH</sub>                  | Output Data Setup to Clock Rising Edge   |                 | T <sub>PC</sub> -20 |     |                     | ns              |
| t <sub>XHQX</sub>                  | Output Data Hold after Clock Rising Edge |                 | T <sub>PC</sub> -10 |     |                     | ns              |
| t <sub>XHDX</sub>                  | Input Data Hold after Clock Rising Edge  |                 | 0                   |     |                     | ns              |
| t <sub>XHDV</sub>                  | Clock Rising Edge to Input Data Valid    |                 |                     |     | T <sub>PC</sub> -20 | ns              |
| SPI Master Mode (Synchronous Mode) |                                          |                 |                     |     |                     |                 |
| f <sub>MCK</sub>                   | SPI Output Clock Frequency               | VDD=3.3V ~ 5.5V |                     |     | 18                  | MHz             |
|                                    |                                          | VDD=1.8V ~ 3.3V |                     |     | 16                  | MHz             |
| t <sub>MCKH</sub>                  | SPI Clock High Time                      |                 | 2                   |     |                     | T <sub>PC</sub> |
| t <sub>MCKL</sub>                  | SPI Clock Low Time                       |                 | 2                   |     |                     | T <sub>PC</sub> |
| SPI Slave Mode (Synchronous Mode)  |                                          |                 |                     |     |                     |                 |
| f <sub>MCK</sub>                   | SPI Input Clock Frequency                | VDD=3.3V ~ 5.5V |                     |     | 12                  | MHz             |
|                                    |                                          | VDD=1.8V ~ 3.3V |                     |     | 12                  | MHz             |
| t <sub>MCKH</sub>                  | SPI Clock High Time                      |                 | 4                   |     |                     | T <sub>PC</sub> |
| t <sub>MCKL</sub>                  | SPI Clock Low Time                       |                 | 4                   |     |                     | T <sub>PC</sub> |

T<sub>PC</sub> : APB clock or SYS clock cycle time

**Figure 8-1. UART Timing Waveform**



## 8.17. SPI Characteristics

**Table 8-18. SPI Characteristics**

VDD=5.0V±10%, VSS=0V, TA = -40°C ~ +105°C (unless otherwise specified)

| Symbol            | Parameter                                                         | Conditions      | Limits                |     |     | Unit            |
|-------------------|-------------------------------------------------------------------|-----------------|-----------------------|-----|-----|-----------------|
|                   |                                                                   |                 | Min                   | Typ | Max |                 |
| Master Mode       |                                                                   |                 |                       |     |     |                 |
| f <sub>MCK</sub>  | SPI Clock Frequency                                               | VDD=3.3V ~ 5.5V |                       |     | 22  | MHz             |
|                   |                                                                   | VDD=1.8V ~ 3.3V |                       |     | 16  | MHz             |
| t <sub>MCKH</sub> | SPI Clock High Time                                               |                 | 2                     |     |     | T <sub>PC</sub> |
| t <sub>MCKL</sub> | SPI Clock Low Time                                                |                 | 2                     |     |     | T <sub>PC</sub> |
| t <sub>MIS</sub>  | D <sub>IN</sub> Valid to SPI Clock Shift Edge                     |                 | 2T <sub>PC</sub> + 20 |     |     | ns              |
| t <sub>MIH</sub>  | SPI Clock Shift Edge to D <sub>IN</sub> Change                    |                 | 0                     |     |     | ns              |
| t <sub>MOH</sub>  | SPI Clock Shift Edge to D <sub>OUT</sub> Change                   |                 |                       |     | 10  | ns              |
| Slave Mode        |                                                                   |                 |                       |     |     |                 |
| f <sub>SCK</sub>  | SPI Clock Frequency                                               | VDD=3.3V ~ 5.5V |                       |     | 16  | MHz             |
|                   |                                                                   | VDD=1.8V ~ 3.3V |                       |     | 12  | MHz             |
| t <sub>SE</sub>   | NSS Falling to First SPI Clock Edge                               |                 | 2                     |     |     | T <sub>PC</sub> |
| t <sub>SD</sub>   | Last SPI Clock Edge to NSS Rising                                 |                 | 2                     |     |     | T <sub>PC</sub> |
| t <sub>SEZ</sub>  | NSS Falling to D <sub>OUT</sub> Valid                             |                 |                       |     | 4   | T <sub>PC</sub> |
| t <sub>SDZ</sub>  | NSS Rising to D <sub>OUT</sub> High-Z                             |                 |                       |     | 4   | T <sub>PC</sub> |
| t <sub>CKH</sub>  | SPI Clock High Time                                               |                 | 3                     |     |     | T <sub>PC</sub> |
| t <sub>CKL</sub>  | SPI Clock Low Time                                                |                 | 3                     |     |     | T <sub>PC</sub> |
| t <sub>sis</sub>  | D <sub>IN</sub> Valid to SPI Clock Sample Edge                    |                 | 2                     |     |     | T <sub>PC</sub> |
| t <sub>sih</sub>  | SPI Clock Sample Edge to D <sub>IN</sub> Change                   |                 | 2                     |     |     | T <sub>PC</sub> |
| t <sub>soh</sub>  | SPI Clock Shift Edge to D <sub>OUT</sub> Change                   |                 |                       |     | 4   | T <sub>PC</sub> |
| t <sub>SLH</sub>  | Last SPI Clock Edge to D <sub>OUT</sub> Change<br>(CPHA = 1 only) |                 | 1                     |     | 2   | T <sub>PC</sub> |

T<sub>PC</sub> : APB clock or SYS clock cycle time

D<sub>IN</sub> : SPI input data signal

D<sub>OUT</sub> : SPI output data signal

Figure 8-2. SPI Master Timing Waveform

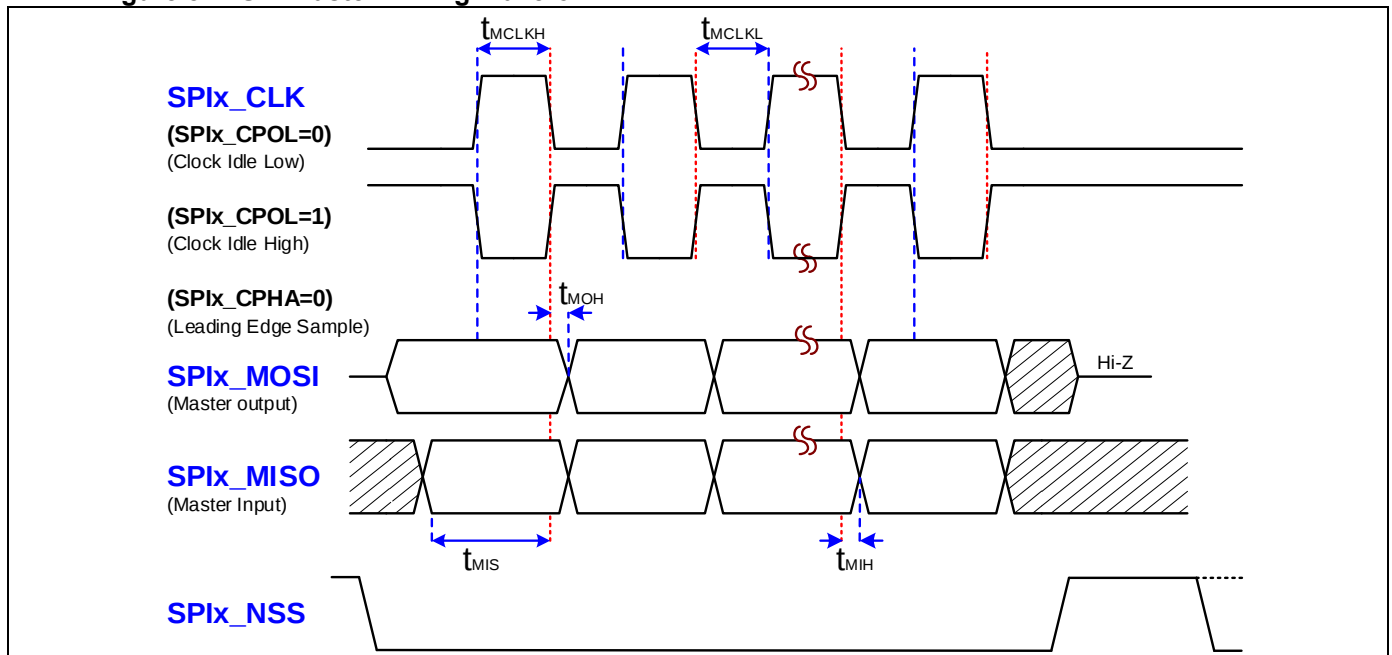
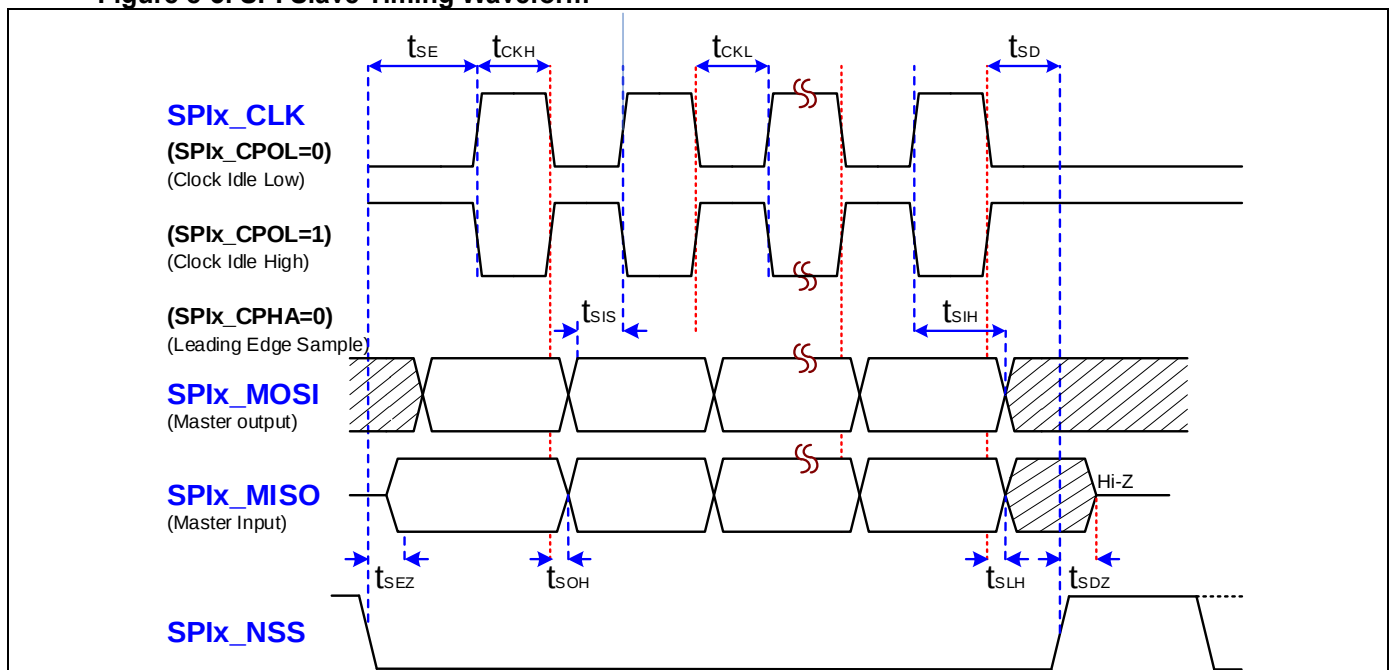


Figure 8-3. SPI Slave Timing Waveform



## 8.18. I2C Characteristics

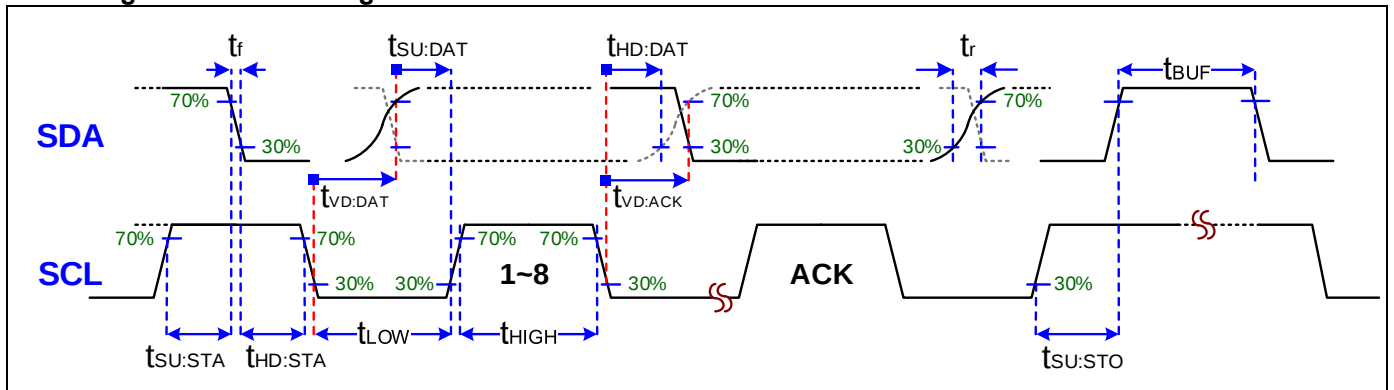
**Table 8-19. I2C Characteristics**

VDD=5.0V±10%, VSS=0V, TA = -40°C ~ +105°C (unless otherwise specified)

| Symbol              | Parameter                                  | Conditions | Standard-mode |      | Fast-mode      |     | Fast-mode Plus |      | Unit            |
|---------------------|--------------------------------------------|------------|---------------|------|----------------|-----|----------------|------|-----------------|
|                     |                                            |            | Min           | Max  | Min            | Max | Min            | Max  |                 |
| f <sub>SCL</sub>    | SCL Clock Frequency                        |            | 0             | 100  | 0              | 400 | 0              | 1000 | KHz             |
| t <sub>Low</sub>    | Low period of the SCL clock                |            | 4.7           |      | 1.3            |     | 0.5            |      | us              |
| t <sub>Low_M</sub>  | Low period of the SCL clock (Master Mode)  |            | 2             |      | 2              |     | 2              |      | T <sub>PC</sub> |
| t <sub>Low_S</sub>  | Low period of the SCL clock (Slave Mode)   |            | 4             |      | 4              |     | 4              |      | T <sub>PC</sub> |
| t <sub>High</sub>   | High period of the SCL clock               |            | 4.0           |      | 0.6            |     | 0.26           |      | us              |
| t <sub>High_M</sub> | High period of the SCL clock (Master Mode) |            | 3             |      | 3              |     | 3              |      | T <sub>PC</sub> |
| t <sub>High_S</sub> | High period of the SCL clock (Slave Mode)  |            | 5             |      | 5              |     | 5              |      | T <sub>PC</sub> |
| t <sub>HD;STA</sub> | Hold time for START condition              |            | 4.0           |      | 0.6            |     | 0.26           |      | us              |
| t <sub>SU;STA</sub> | Setup time for START condition             |            | 4.7           |      | 0.6            |     | 0.26           |      | us              |
| t <sub>HD;DAT</sub> | Data hold time                             |            | 0             |      | 0              |     | 0              |      | us              |
| t <sub>SU;DAT</sub> | Data setup time                            |            | 250           |      | 100            |     | 50             |      | ns              |
| t <sub>SU;STO</sub> | Setup time for STOP condition              |            | 4.0           |      | 0.6            |     | 0.26           |      | us              |
| t <sub>BUF</sub>    | Bus free time between a STOP and START     |            | 4.7           |      | 1.3            |     | 0.5            |      | us              |
| t <sub>VD;DAT</sub> | Data valid time                            |            |               | 3.45 |                | 0.9 |                | 0.45 | us              |
| t <sub>VD;ACK</sub> | Data valid acknowledge time                |            |               | 3.45 |                | 0.9 |                | 0.45 | us              |
| t <sub>r</sub>      | Rise time of both SDA and SCL signals      |            |               | 1000 |                | 300 |                | 120  | ns              |
| t <sub>f</sub>      | Fall time of both SDA and SCL signals      |            |               | 300  | 20x (VDD/5.5V) | 300 | 20x (VDD/5.5V) | 120  | ns              |
| C <sub>i</sub>      | Capacitive load for each IO pin            |            |               | 10   |                | 10  |                | 10   | pF              |

T<sub>PC</sub> : APB clock or SYS clock cycle time

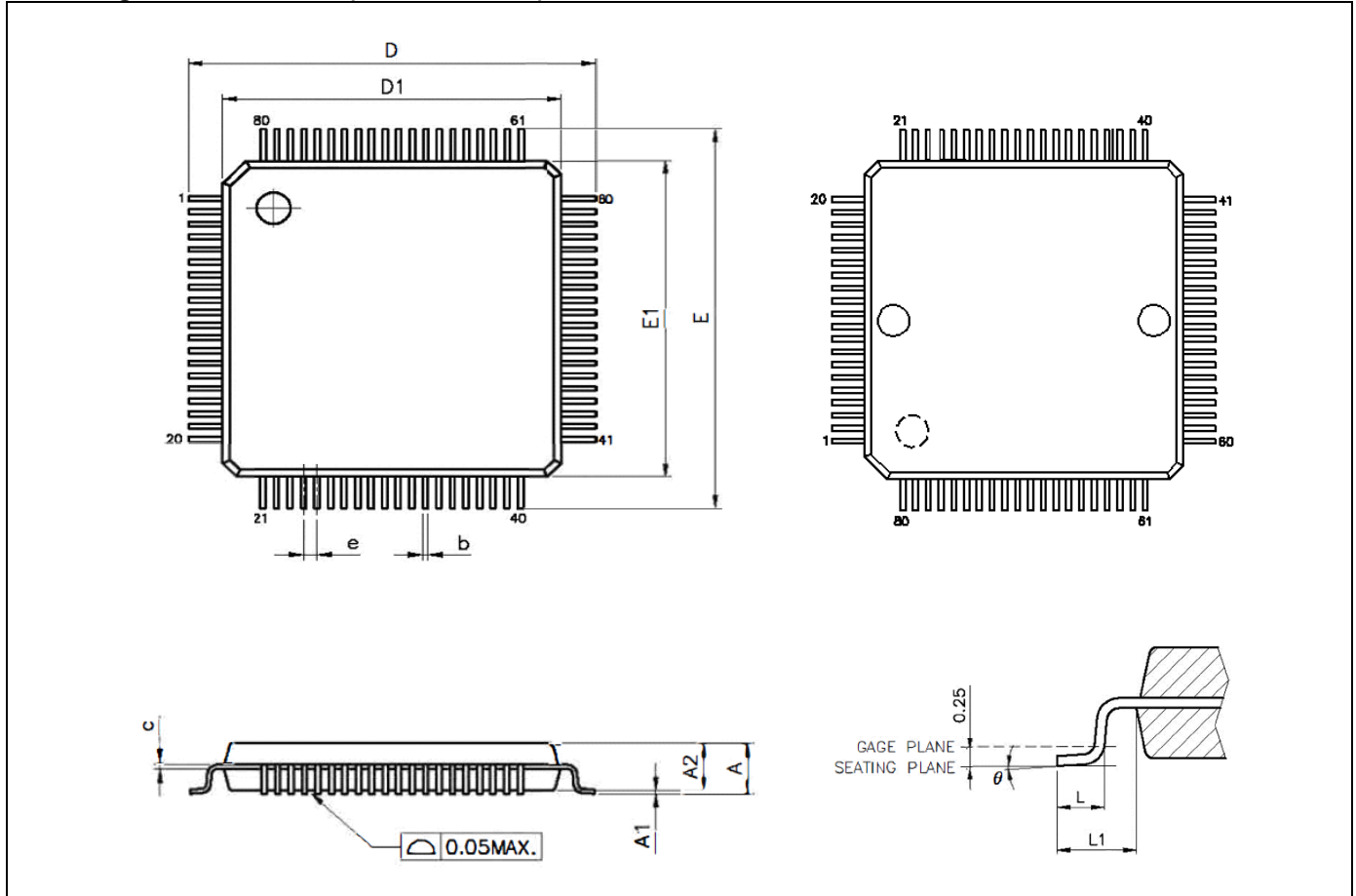
**Figure 8-4. I2C Timing Waveform**



## 9. Package Dimension

### 9.1. LQFP-80

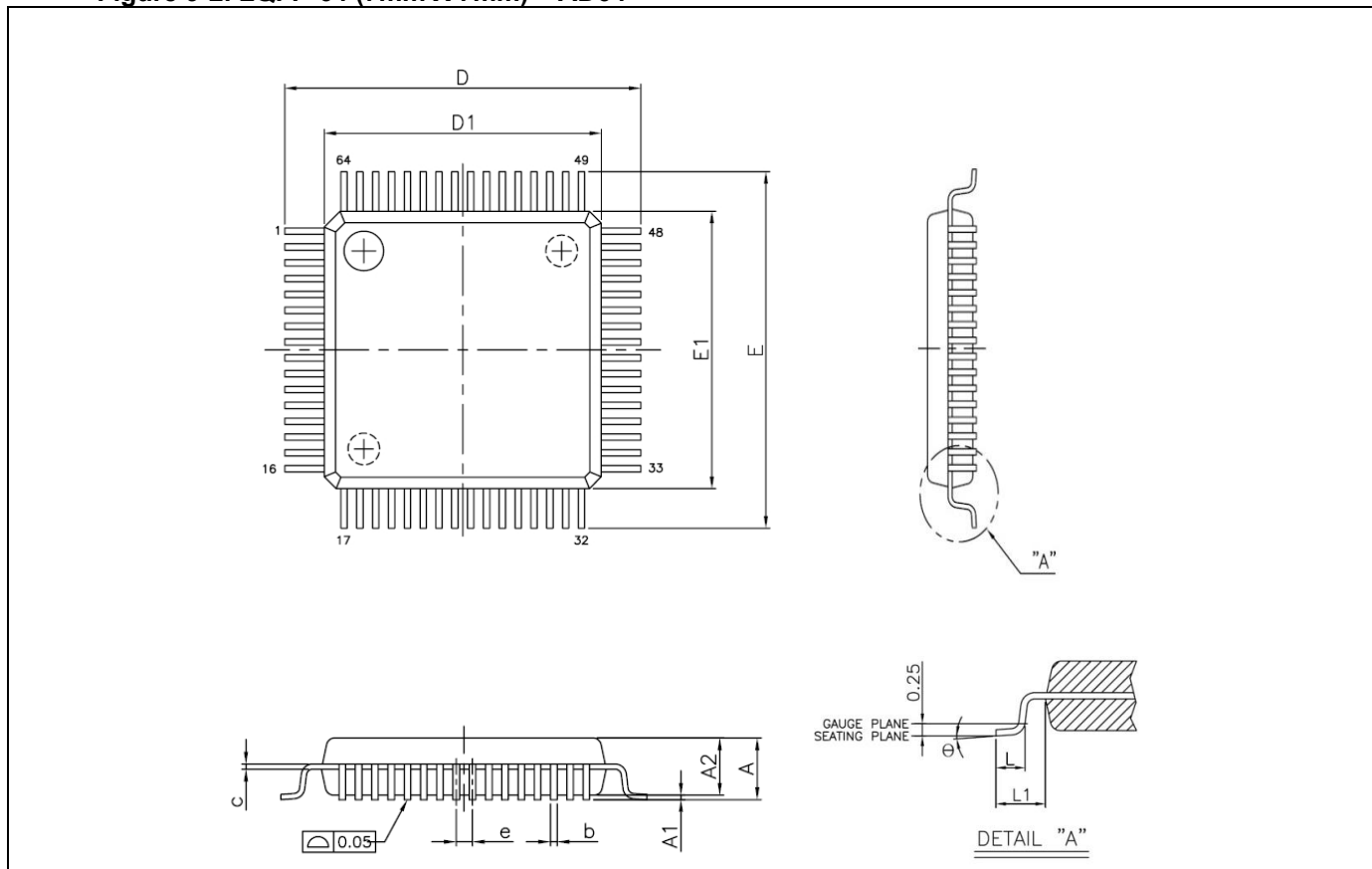
Figure 9-1. LQFP-80 (10mm X 10mm) ~ AD80



| Unit    | mm        |      |      | inch      |       |       |
|---------|-----------|------|------|-----------|-------|-------|
| Symbols | Min.      | Nom. | Max. | Min.      | Nom.  | Max.  |
| A       | ---       | ---  | 1.60 | ---       | ---   | 0.062 |
| A1      | 0.05      | ---  | 0.15 | 0.001     | ---   | 0.005 |
| A2      | 1.35      | 1.40 | 1.45 | 0.053     | 0.055 | 0.057 |
| b       | 0.13      | 0.18 | 0.23 | 0.005     | 0.007 | 0.009 |
| c       | 0.09      | ---  | 0.20 | 0.003     | ---   | 0.007 |
| D       | 12.00 BSC |      |      | 0.472 BSC |       |       |
| D1      | 10.00 BSC |      |      | 0.393 BSC |       |       |
| E       | 12.00 BSC |      |      | 0.472 BSC |       |       |
| E1      | 10.00 BSC |      |      | 0.393 BSC |       |       |
| e       | 0.40 BSC  |      |      | 0.015 BSC |       |       |
| L       | 0.45      | 0.60 | 0.75 | 0.018     | 0.024 | 0.030 |
| L1      | 1.00 REF  |      |      | 0.039 REF |       |       |
| e       | 0°        | 3.5° | 7°   | 0°        | 3.5°  | 7°    |

## 9.2. LQFP-64

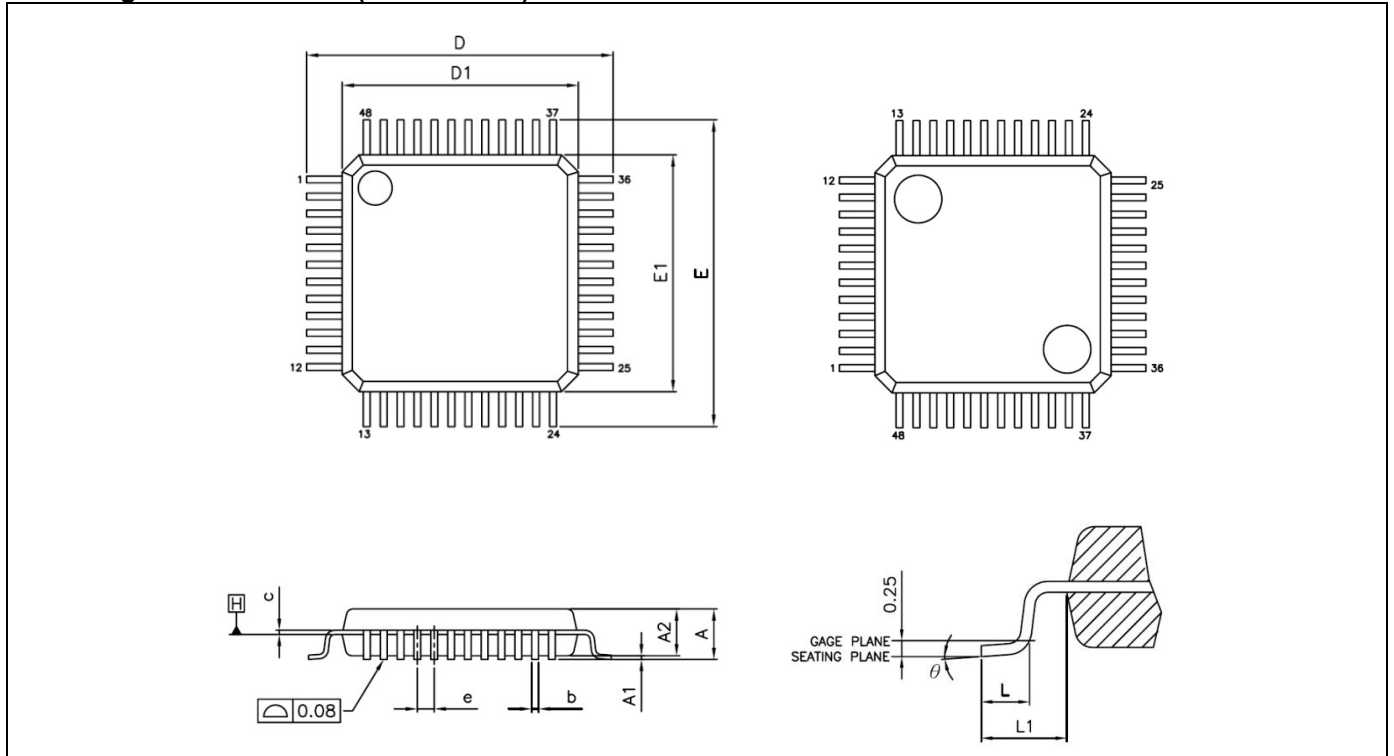
Figure 9-2. LQFP-64 (7mm X 7mm) ~ AD64



| Unit    | mm       |      |      | inch      |       |       |
|---------|----------|------|------|-----------|-------|-------|
| Symbols | Min.     | Nom. | Max. | Min.      | Nom.  | Max.  |
| A       | ---      | ---  | 1.60 | ---       | ---   | 0.062 |
| A1      | 0.05     | ---  | 0.15 | 0.001     | ---   | 0.005 |
| A2      | 1.35     | 1.40 | 1.45 | 0.053     | 0.055 | 0.057 |
| b       | 0.13     | 0.18 | 0.23 | 0.005     | 0.007 | 0.009 |
| c       | 0.09     | ---  | 0.20 | 0.003     | ---   | 0.007 |
| D       | 9.00 BSC |      |      | 0.354 BSC |       |       |
| D1      | 7.00 BSC |      |      | 0.275 BSC |       |       |
| e       | 0.40 BSC |      |      | 0.015 BSC |       |       |
| E       | 9.00 BSC |      |      | 0.354 BSC |       |       |
| E1      | 7.00 BSC |      |      | 0.275 BSC |       |       |
| L       | 0.45     | 0.60 | 0.75 | 0.018     | 0.024 | 0.030 |
| L1      | 1.00 REF |      |      | 0.039 REF |       |       |
| θ       | 0°       | 3.5° | 7°   | 0°        | 3.5°  | 7°    |

## 9.3. LQFP-48

Figure 9-3. LQFP-48 (7mm X 7mm) ~ AD48



| Unit    | mm       |      |      | inch      |       |       |
|---------|----------|------|------|-----------|-------|-------|
| Symbols | Min.     | Nom. | Max. | Min.      | Nom.  | Max.  |
| A       | ---      | ---  | 1.60 | ---       | ---   | 0.062 |
| A1      | 0.05     | ---  | 0.15 | 0.001     | ---   | 0.005 |
| A2      | 1.35     | 1.40 | 1.45 | 0.053     | 0.055 | 0.057 |
| b       | 0.17     | 0.22 | 0.27 | 0.006     | 0.008 | 0.010 |
| c       | 0.09     | ---  | 0.20 | 0.003     | ---   | 0.007 |
| D       | 9.00 BSC |      |      | 0.354 BSC |       |       |
| D1      | 7.00 BSC |      |      | 0.275 BSC |       |       |
| E       | 9.00 BSC |      |      | 0.354 BSC |       |       |
| E1      | 7.00 BSC |      |      | 0.275 BSC |       |       |
| e       | 0.50 BSC |      |      | 0.019 BSC |       |       |
| L       | 0.45     | 0.60 | 0.75 | 0.018     | 0.024 | 0.030 |
| L1      | 1.00 REF |      |      | 0.039 REF |       |       |
| e       | 0°       | 3.5° | 7°   | 0°        | 3.5°  | 7°    |

## 10. Revision History

| Revision V1.31 (2025_0702) |                                                                                                                                                                                                                               | Chapter   |
|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| 1                          | Update I <sub>DAC</sub> parameter in the table of “Table 8-16. DAC Characteristics”.                                                                                                                                          | 8.15      |
| Revision V1.30 (2025_0108) |                                                                                                                                                                                                                               | Chapter   |
| 1                          | Update SRAM size for MG32F02A064 in the table of “Table 2-1. Chip Selection Table”.                                                                                                                                           | 2         |
| 2                          | Add “Q” (Quasi-bidirectional) IO Type definition in the table of “Table 4 4. Abbreviations for pin definition”. Change “Default Type” of PC[0..3][7..14] from “Q” to “A” in the table of “Table 4 5. Pin Descriptions”.       | 4.2       |
| 3                          | Add descriptions of advanced and basic UART module.                                                                                                                                                                           | 6.22.1    |
| 4                          | Add R <sub>VWeak</sub> parameter in the table of “Table 8-5. IO Characteristics”.                                                                                                                                             | 8.4       |
| 5                          | Update the table of “Table 8-6. External Clock Characteristics” about f <sub>xosc</sub> parameter.                                                                                                                            | 8.5       |
| Revision V1.20 (2022_0621) |                                                                                                                                                                                                                               | Chapter   |
| 1                          | Add the figure of “Figure 8-1. UART Timing Waveform” and add “Symbol” column in the table of “Table 8-17. UART Characteristics” in the section of “8.16. UART Characteristics”.                                               | 8.16      |
| 2                          | Add the figures of “Figure 8-2. SPI Master Timing Waveform” and “Figure 8-3. SPI Slave Timing Waveform” in the section of “8.17. SPI Characteristics”. Add “Symbol” column in the table of “Table 8-18. I2C Characteristics”. | 8.17      |
| 3                          | Add the figure of “Figure 8-4. I2C Timing Waveform” in the section of “8.18. I2C Characteristics”.                                                                                                                            | 8.18      |
| Revision V1.10 (2022_0308) |                                                                                                                                                                                                                               | Chapter   |
| 1                          | Remove SDT function in General Description chapter and the section of “6.12. APX”.                                                                                                                                            | 1<br>6.12 |
| 2                          | Add the descriptions of VR0 pin in the section of “7.1. Power Supply Circuit”.                                                                                                                                                | 7.1       |
| Revision V1.00 (2022_0211) |                                                                                                                                                                                                                               | Chapter   |
| 1                          | Correct the “SPI” descriptions from three modules to four modules for SPI communication in Features chapter.                                                                                                                  |           |
| 2                          | Update the “I <sub>OP6</sub> ” parameters in the table of “Table 8-3. DC Characteristic”.                                                                                                                                     | 8.3       |
| 3                          | Add the table of “Table 8-4. Current Measurement Condition Level Definition Table”.                                                                                                                                           | 8.3       |
| 4                          | Update the “TR1~TR7” and “TF1~TF7” parameters in the table of “Table 8-5. IO Characteristics”.                                                                                                                                | 8.4       |
| 5                          | Update the “VR0” and “VDROP” parameters in the table of “Table 8-10. LDO Characteristics”.                                                                                                                                    | 8.9       |
| Revision V0.72 (2021_1215) |                                                                                                                                                                                                                               | Chapter   |
| 1                          | Update the “SPI” descriptions in Features chapter.                                                                                                                                                                            |           |
| 2                          | Update the table of “Table 2-1. Chip Selection Table”.                                                                                                                                                                        | 2         |
| 3                          | Correct the wrong word “Code” to “Cold” in the descriptions of the section “6.3.3. Chip Reset Levels”.                                                                                                                        | 6.3.3     |
| 4                          | Update the descriptions of the section “6.23.1. Introduction”.                                                                                                                                                                | 6.23.1    |
| 5                          | Correct the wrong word “Slop” to “Slope” in the table of “Table 8-3. DC Characteristics”.                                                                                                                                     | 8.3       |
| 6                          | Change “Cycle-to-Cycle Jitter” to “Period Jitter” in the table of “Table 8-6. PLL Characteristics”.                                                                                                                           | 8.6       |

|                                   |                                                                                                                                 |                |
|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------|----------------|
| 7                                 | Update the “SPI Clock Frequency” parameters of slave mode in the table of “Table 8-17. SPI Characteristics”.                    | 8.17           |
| 8                                 | Update the diagram of package dimension for each package in Package Dimension chapter.                                          | 9              |
| <b>Revision V0.71 (2021_0623)</b> |                                                                                                                                 | <b>Chapter</b> |
| 1                                 | Update the table of “Table 2-1. Chip Selection Table”.                                                                          | 2              |
| <b>Revision V0.70 (2021_0609)</b> |                                                                                                                                 | <b>Chapter</b> |
| 1                                 | Support EMB bus 8-bit data width.                                                                                               | 6.7            |
| 2                                 | Update the description of the section of “6.15.3. CMP Control Block”.                                                           | 6.15.3         |
| 3                                 | Update the Conditions description of “Current Consumption” in the table of “Table 8-3. DC Characteristics”.                     | 8.3            |
| 4                                 | Update the $I_{SLP0}/I_{SLP1}/I_{SLP2}$ parameters in the table of “Table 8-3. DC Characteristics”.                             | 8.3            |
| 5                                 | Add the $I_{SLP3}/I_{SLP4}/I_{WK\_SLP1}$ parameters in the table of “Table 8-3. DC Characteristics”.                            | 8.3            |
| 6                                 | Merge the $I_{DAC}/I_{BUF}$ parameters in the table of “Table 8-15. DAC Characteristics”.                                       | 8.15           |
| <b>Revision V0.60 (2021_0426)</b> |                                                                                                                                 | <b>Chapter</b> |
| 1                                 | Update the descriptions of the section of “6.23.1 Introduction”.                                                                | 6.23.1         |
| 2                                 | Update ‘Internal VBUF reference voltage’ parameter in the table “Table 8-11. ADC Characteristics”.                              | 8.11           |
| <b>Revision V0.50 (2021_0322)</b> |                                                                                                                                 | <b>Chapter</b> |
| 1                                 | Add ‘Wakeup Time’ characteristics in the table of “Table 8-3. DC Characteristics”.                                              | 8.3            |
| <b>Revision V0.40 (2021_0129)</b> |                                                                                                                                 | <b>Chapter</b> |
| 1                                 | Separate the series Data Sheet for MG32F02A128/A064 chips.                                                                      |                |
| 2                                 | Update the descriptions of the section of “7.2. Reset Circuit” and “7.5. DAC Application Circuit” in Application Notes chapter. | 7.2<br>7.5     |
| <b>Revision V0.30 (2021_0127)</b> |                                                                                                                                 | <b>Chapter</b> |
| 1                                 | Update the parameters’ value in Electrical Characteristics chapter.                                                             | 8              |
| 2                                 | Add the information of ‘Dimensions in inch’ for each package in Package Dimension chapter.                                      | 9              |
| <b>Revision V0.20 (2020_0928)</b> |                                                                                                                                 | <b>Chapter</b> |
| 1                                 | Add (*1) comment for the section of Operating in Feature chapter.                                                               |                |
| 2                                 | Update the section of Part Number List in Order Information chapter.                                                            | 2              |
| <b>Revision V0.10 (2020_0401)</b> |                                                                                                                                 | <b>Chapter</b> |
| 1                                 | Preliminary version                                                                                                             |                |

### 11. Disclaimers

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