MDSF40

Data Sheet

8-Bit MCU Embedded 40V 3-Phase P/N MOSFET Pre-Driver

Version: A9

Features

Motor Controller (MOC)
- Estimated Angle Phase Lock Loop (PLL)
- Field Oriental Control (FOC)
- Slide Mode Rotor Position Estimated (SMO)
- Space Vector PWM (SVPWM)
- Supports Digital OCP and Analog OCP (Over Current Protection)
- Supports Initial Angle Estimated (IAE)
- Programmable Dead-band
- Independent General Low Pass Filter
- Independent General PWM
- External Capture
- Internal Capture

Gate Driver
- Integrated 40V 3-phase P/N MOSFET Pre-driver
- Shoot-through protection
- Built-in 5V LDO

Embedded MCU
- MCS®-51 Compatible
- 1T 8052 Central Processing Unit
- 4.5V to 5.5V Operation Range
- 4 Level Priority Interrupt
- 13 Interrupt Sources
    - Two External Interrupts (INT0N, INT1N)
    - Two External OCP Interrupts (AOCP, OCP)
- Memory Size:
    - 16K Byte Flash Program Memory
    - 256 Byte EEPROM
    - 256 Byte IRAM
    - 512 Byte XRAM
- Up to 25 General-Purpose Input / Output (GPIO) Pins
- Three 16-bit Timer/Counters
- Watchdog Timer (WDT)

- 8 Cannels 10-bit Analog-to-Digital Converter (ADC)
- Full Duplex UART Serial Channel
- IIC Interface (Master/Slave Mode)
- One Wire RF/IR Receiver Output Signal Decode

CRC Function

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1. General Description

The MDSF40 is a highly integrated motor drive controller. The MDSF40 is composed of FOC sensor-less MCU and 40V 3-phase P/N MOSFET pre-driver that suit for under DC 30V and medium motor system, for example household fan、water pump、server fan…etc.

2. Block Diagram

Figure 1 Block Diagram
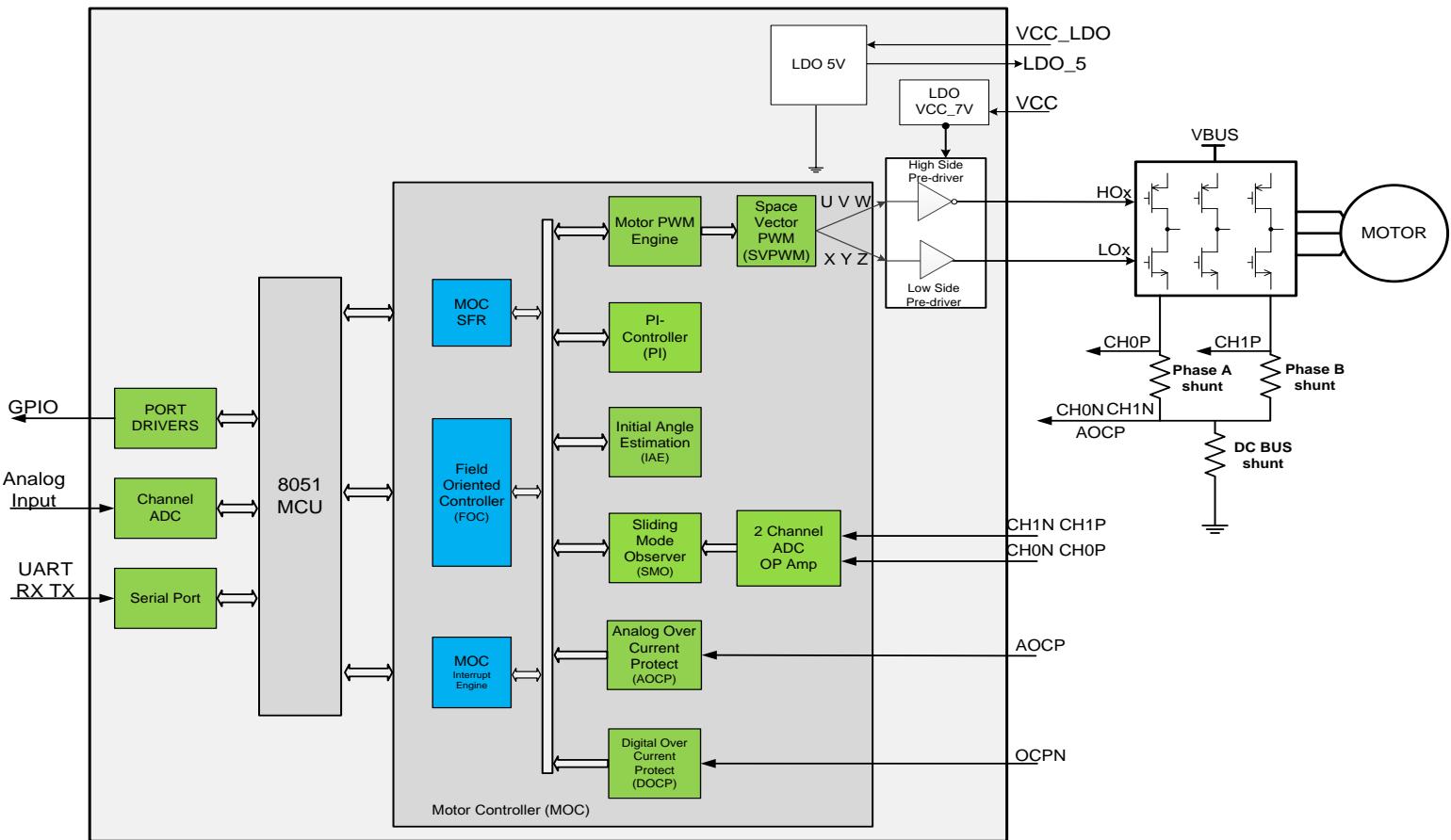
3. Pin Assignments

Figure 2 LQFP48 7x7-48(AA2)

Pin assignments for MDSF40AD48 (LQFP48-7x7):

Top pins (left to right, 48–37):
- 48 VCC_7
- 47 N.C.
- 46 PGND
- 45 LDO_5
- 44 VCC_LDO
- 43 P1.7 / DOCPN
- 42 P1.6 / AOCP
- 41 OP_VINP
- 40 OP_VINN
- 39 OP_VOUT
- 38 (unlabeled)
- 37 P0.1 / OP0N

Left pins (top to bottom, 1–12):
- 1 VCC
- 2 UH
- 3 UL
- 4 VH
- 5 VL
- 6 WH
- 7 WL
- 8 N.C.
- 9 O2
- 10 I2
- 11 O1
- 12 I1

Right pins (top to bottom, 36–25):
- 36 P0.2 / OP1P / CH1
- 35 P0.3 / OP1N
- 34 P0.4 / CH2
- 33 P0.5 / IR1 / CH3
- 32 P0.6 / CAP1 / CH4
- 31 P0.7 / CAP2 / CH5
- 30 P3.2 / INT0N / CH6
- 29 P3.3 / INT1N / IR2 / CH7
- 28 V18
- 27 VSS
- 26 VDD_5V
- 25 XTALO / T0 / P3.4

Bottom pins (left to right, 13–24):
- 13 N.C.
- 14 IPWM / P2.6
- 15 IIC_SCL / P2.5
- 16 IIC_SDA / P2.4
- 17 N.C.
- 18 FG / P2.7
- 19 TX / P3.1
- 20 RX / P3.0
- 21 SCL_ICE
- 22 SDA_ICE
- 23 RSTN
- 24 XTALI / T1 / P3.5

4. Pin Definitions

Table 1 Pin Definitions

Pin #	Name	Type	Description
1	VCC	Power	Supply voltage input.
2	UH	O	High side phase-U PMOS driver.
3	UL	O	Low side phase-U NMOS driver.
4	VH	O	High side phase-V PMOS driver.
5	VL	O	Low side phase-V NMOS driver.
6	WH	O	High side phase-W PMOS driver.
7	WL	O	Low side phase-W NMOS driver.
8	NC		
9	O2	O	Open-drain_2 output.
10	I2	I	Open-drain_2 input.
11	O1	O	Open-drain_1 output.
12	I1	I	Open-drain_1 input.
13	NC		
14	P2.6	I/O	Bit6 of Port 2.
	IPWM	O	Independent User PWM Output
15	P2.5	I/O	Bit5 of Port 2.
	IIC_SCL	O	IIC clock
16	P2.4	I/O	Bit4 of Port 2.
	IIC_SDA	O	IIC data
17	NC		
18	P2.7	I/O	Bit7 of Port 2.
	FG	O	Function Generate Output
19	P3.1	I/O	Bit1 of Port 3.
	TX	O	Serial Data Receive (UART)
20	P3.0	I/O	Bit0 of Port 3.
	RX	I	Serial Data Transmit (UART)
21	SCL$_{ICE}$		For ICE.
22	SDA$_{ICE}$		For ICE.
23	RSTN	I	System Reset.
24	P3.5	I/O	Bit 5 of Port 3
	XTALI	I	Crystal input pin. **Connect the crystal 12MHz between this pin and XTALO and a 22pF capacitor to VSS**

	T1	I	TIMER1 External Input
25	P3.4	I/O	Bit 4 of Port 3
	XTALO	O	Crystal output pin. **Connect the crystal 12MHz between this pin and XTALI and a 22pF capacitor to VSS**
	T0	I	TIMER0 External Input
26	VDD5	Power	5.0V Voltage Input. A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS.
27	VSS	Ground	Power Ground.
28	V18	O	1.8V Voltage Output. A 0.1uF and 1uF (minimum) capacitor should be connected between this pin and VSS.
29	P3.3	I/O	Bit 3 of Port 3
	CH7	I	Analog Input Ch7
	INT1N	I	External Interrupt 1. Low level trigger or falling edge trigger
	IR2	I	IR receiver signal input 2
30	P3.2	I/O	Bit2 of Port 3
	CH6	I	Analog Input Ch6
	INT0N	I	External Interrupt 0. Low level trigger or falling edge trigger
31	P0.7	I/O	Bit7 of Port 0
	CH5	I	Analog Input Ch5
	CAP2	I	Capture Input 2
32	P0.6	I/O	Bit6 of Port 0
	CH4	I	Analog Input Ch4
	CAP1	I	Capture Input 1
33	P0.5	I/O	Bit5 of Port 0
	CH3	I	Analog Input Ch3
	IR1	I	IR receiver signal input 1
34	P0.4	I/O	Bit4 of Port 0.
	CH2	I	Analog Input Ch2.
35	P0.3	I/O	Bit3 of Port 0.
	OP1N	0	OP1-Amp N- Input
36	P0.2	I/O	Bit2 of Port 0.
	CH1	I	Analog Input Ch1. (Current feedback)
	OP1P	I	OP1-Amp P-Input.
37	P0.1	I/O	Bit1 of Port 0.
	OP0N	I	OP0-Amp N-Input.
38	P0.0	I/O	Bit0 of Port 0.

	CH0	I	Analog Input Ch0. (Current feedback)
	OP0P	I	OP0-Amp P- Input.
39	OP_VOUT	O	OPA output
40	OP_VINN	I	OPA N-Input
41	OP_VINP	I	OPA P-Input
42	P1.6	I/O	Bit6 of Port 1.
	AOCP	I	Analog OCP Control.
43	P1.7	I/O	Bit7 of Port 1.
	DOCPN	I	Digital OCP Control.
44	VCC_LDO	Power	LDO 5V power supply.
45	LDO_5	Power output	5V output of LDO.
46	PGND	Ground	Power ground.
47	NC		
48	VCC_7	O	LDO VCC_7 output

5. Absolute Maximum Ratings

VDD5 Supply Voltage.......................................V_{SS}-0.3V to V_{SS}+6.0V

VCC Supply Voltage..-0.3V to 40V

Storage Temperature...-50℃ to 150℃

Operating Temperature with LDO_5V 30mA..........................-40℃ to 85℃

Operating Temperature w/o LDO_5V   ....-40℃ to 105℃

GPIO I_{OH}...-6mA

GPIO I_{OL}...6mA

Gate Driver Source peak current 80mA

Gate Driver Sink peak current 50mA

ΘJC Thermal Resistance, Junction-to-case (LQFP7x7-48).......17℃/W

ΘJA Thermal Resistance, Junction-to-ambient (LQFP7x7-48)......60℃/W

Total Power Dissipation...1500mW

Electrostatic Discharge Capability – Human Body Mode.............2000V

Electrostatic Discharge Capability – Machine Mode..................200V

6. D.C. Characteristics

Table 2 D.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V	Conditions				
MCU							
V_{DD5}	Operating Voltage	—	fsys=48MHz	4.5	5	5.5	V
V_{18}	V_{18} Output Range	—	Load Current <30mA	1.71	1.8	1.81	V
I_{DD}	Operating Current	5V	No load, fsys=48Mhz,ADC off, MOC off	—	9	12	mA
V_{IL}	Input Low Voltage for I/O Ports.	—	—	0	—	0.3 V_{DD5}	V
V_{IH}	Input High Voltage for I/O Ports.	—	—	0.75 V_{DD5}	—	V_{DD5}	V
V_{LVD}	LVD Voltage Level	—	—				
V_{OL}	Output Low Voltage for I/O Ports.	VDD5	I_{OL}=20mA	—	—	0.5	V
V_{OH}	Output High Voltage for I/O Ports.	VDD5	I_{OH}=-7.4mA	4.5	—	—	V
R_{PU}	Pull-up Resistance for I/O Ports	VDD5	—	10	30	50	KΩ
R_{PD}	Pull-down Resistance for I/O Ports	VDD5	—	10	30	50	KΩ
Gate Driver, V_{CC} = 24 V, T_A = 25 ºC, unless otherwise specified.							
VCC	DC Voltage Input			10	–	40	V
$V_{IH\_U/V/WH}$	Logic "1" Input Voltage	Vcc = 10V to 40V		2.4	–	–	
$V_{IL\_U/W/WH}$	Logic "0" Input Voltage	Vcc = 10V to 40V		–	–	0.8	V
O1,O2(open drain)	Low level output voltage	Io = 5mA		–	0.2	–	
$I_{O+\_U/V/WH}$	Source Peak Current	CL = 1nF			80		mA

$I_{O-\_U/V/WH}$	Sink Peak Current	CL = 1nF		50		mA
I_{QCC}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V			800	μA
R_{IN}	HI_U/V/W, LI_U/V/W Pin Pull Low Resistor			100		KΩ
Rh_{OUT}	HO_U/V/W Pin Pull High Resistor			100		KΩ
Rl_{OUT}	LO_U/V/W Pin Pull Low Resistor			100		KΩ
VCC_7 LDO Characteristics						
VCC_7	VCC_7 Regulator Output Voltage	VCC = 24V, Io = 6mA		17		V
5V LDO Characteristics						
V_{LDO}	Regulator Output Voltage	VCC = 24V, Io = 30mA		5.0		V

7. A.C. Characteristics

Ta=25℃

Table 3 A.C. Characteristics

MCU							
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD5	Conditions				
f_{SYS}	System Frequency	4.5V~5.5V	Ta=-40℃ to 125℃	TBD	48	TBD	MHz
			Ta=-20℃ to 85℃	TBD	48	TBD	MHz
			Ta=25℃	-1%	48	1%	MHz
f_{TIMER}	Timer Input Pin Frequency	–	–	–	–	4	fsys
t_{INT}	Interrupt Pulse Width	–	–	1	5	10	tsys
t_{LVD}	Low Voltage Width to interrupt	–		120	240	480	us
t_{V18}	V_{18} Stable Time	–	–	60	120	240	us
t_{RSDT}	System Reset Delay Time(Power On Reset)	–	–	25	50	100	ms

Gate Driver , VCC=24V, VSS=0V, CL=1nF, TA=25℃						
Symbol	Definition	Test Condition	Min.	Typ.	Max.	Unit
t_{on}	(HI_U/V/W) Turn-on Propagation Delay			260		ns
t_{off}	(HI_U/V/W) Turn-off Propagation Delay			220		
t_R	Turn on rise time			75		
t_F	Turn off fall time			72		

On-chip Oscillator Frequency Accuracy over Device V_{DD} and Temperature

8. OPA Characteristics

Table 4 OPA Characteristic

Ta=25℃, V_{DD}= 5V, V_{SS}=GND

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CRM}	Common Mode Input Range		V_{SS}-0.3	—	V_{DD}+0.3	V
V_{OS}	Input Offset Voltage	V_{CM}=V_{SS}	-4.5		4.5	mV
A_{OL}	DC Open-Loop Gain	V_{OUT}=0.3V~V_{DD}-0.3V V_{CM}=V_{SS}	88	112		dB
GBWP	Gain Bandwidth Product	R_L=10KΩ C_L=60 pF		1		MHz
SR	Slew Rate	C_L=60 pF		0.6		V/us

9. A/D Converter Characteristics

Figure 3 A/D Converter Characteristics
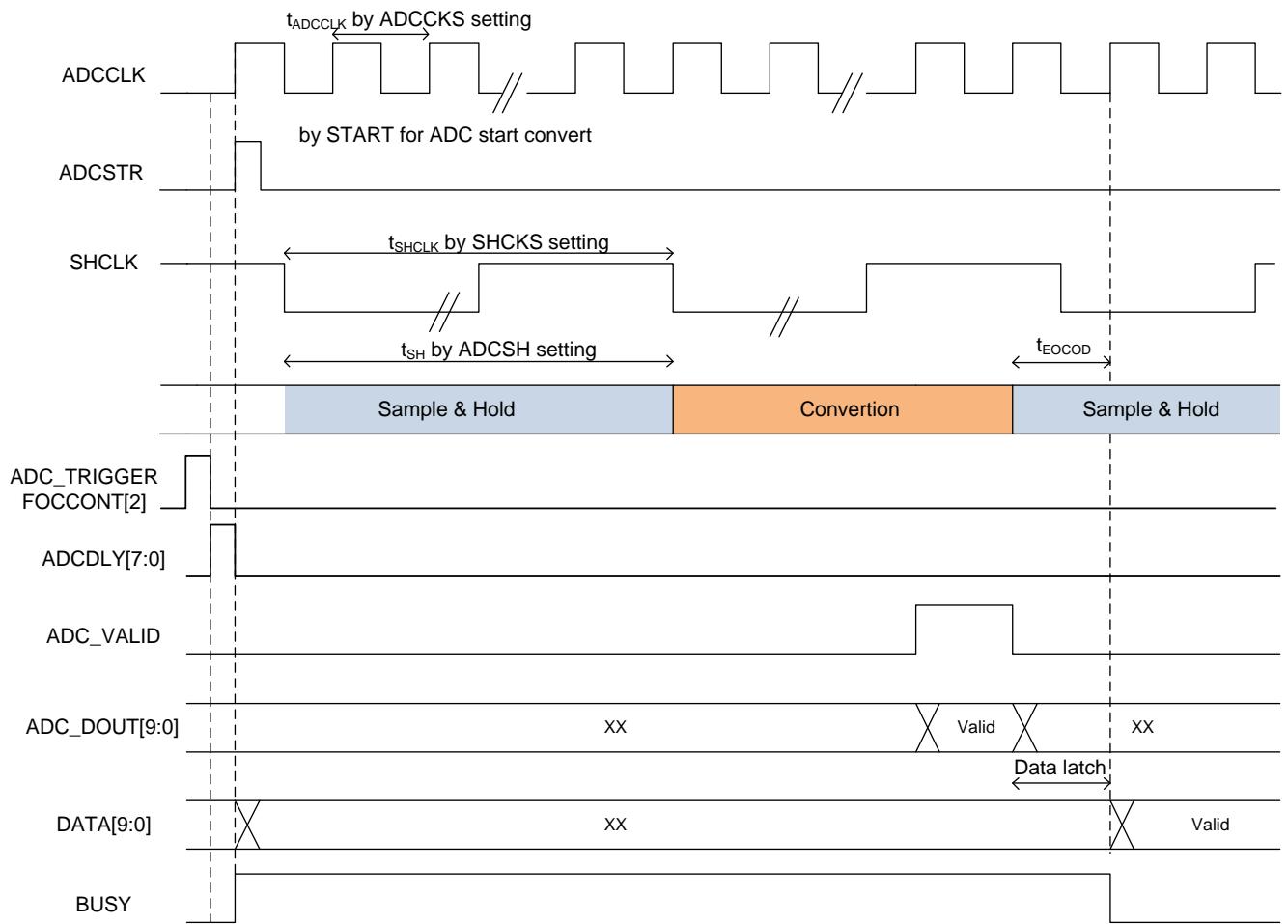
Table 5 ADC Characteristics

Ta=25℃

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
R_I	Input Impedance	—	—	—		—	MΩ
I_{AD}	Additional Power Consumption if A/D Converter is Used	5V	—	—	5	—	mA
I_{ADSTB}	A/D Converter Standby Current	—	Load Current < 10mA	—	—	4	uA
t_{ADCCLK}	A/D Converter Clock Time	—	4MHz	—	0.25	—	us
		—	2MHz	—	0.5	—	us
t_{CONV}	A/D Conversion Time	—	4MHz	—	2.5	—	us
		—	2MHz	—	5	—	us
t_{SHCLK}	A/D Sample and Hold Clock Time	—	1MHz	—	1	—	us
		—	500KHz	—	2	—	us
		—	400KHz	—	2.5	—	us
		—	333KHz	—	3	—	us
t_{SH}	A/D Sample and Hold Time	—	1MHz	1	—	4	us
		—	500KHz	2	—	8	us
		—	400KHz	2.5	—	10	us
		—	333KHz	3	—	12	us
DNL	Differential Non-linearity	4.5V	No load, t_{CONV}=2.5us	-1	—	+3	LSB
		5.5V		-1	—	+3	LSB
		4.5V	No load, t_{CONV}=5us	-1	—	+3	LSB
		5.5V		-1	—	+3	LSB
INL	Integral Non-linearity	4.5V	No load, t_{CONV}=2.5us	-4	—	+4	LSB
		5.5V		-4	—	+4	LSB
		4.5V	No load, t_{CONV}=5us	-4	—	+4	LSB
		5.5V		-4	—	+4	LSB
G_{ERR}	Gain Error	—	—	-10	—	+10	LSB
t_{EOCOD}	End of Conversion Output Delay	5V	—	—		—	ns

10. Memory

The **MDSF40** memory structure follows the general 8052 structure.

There are three memory areas: Program Memory (Flash), External Data Memory (XRAM) and Internal Data Memory (IRAM). In addition, **MDSF40** integrates 16K bytes Flash, 256 bytes IRAM and 512 bytes XRAM.

Figure 4-10 Memory architecture in MDSF40
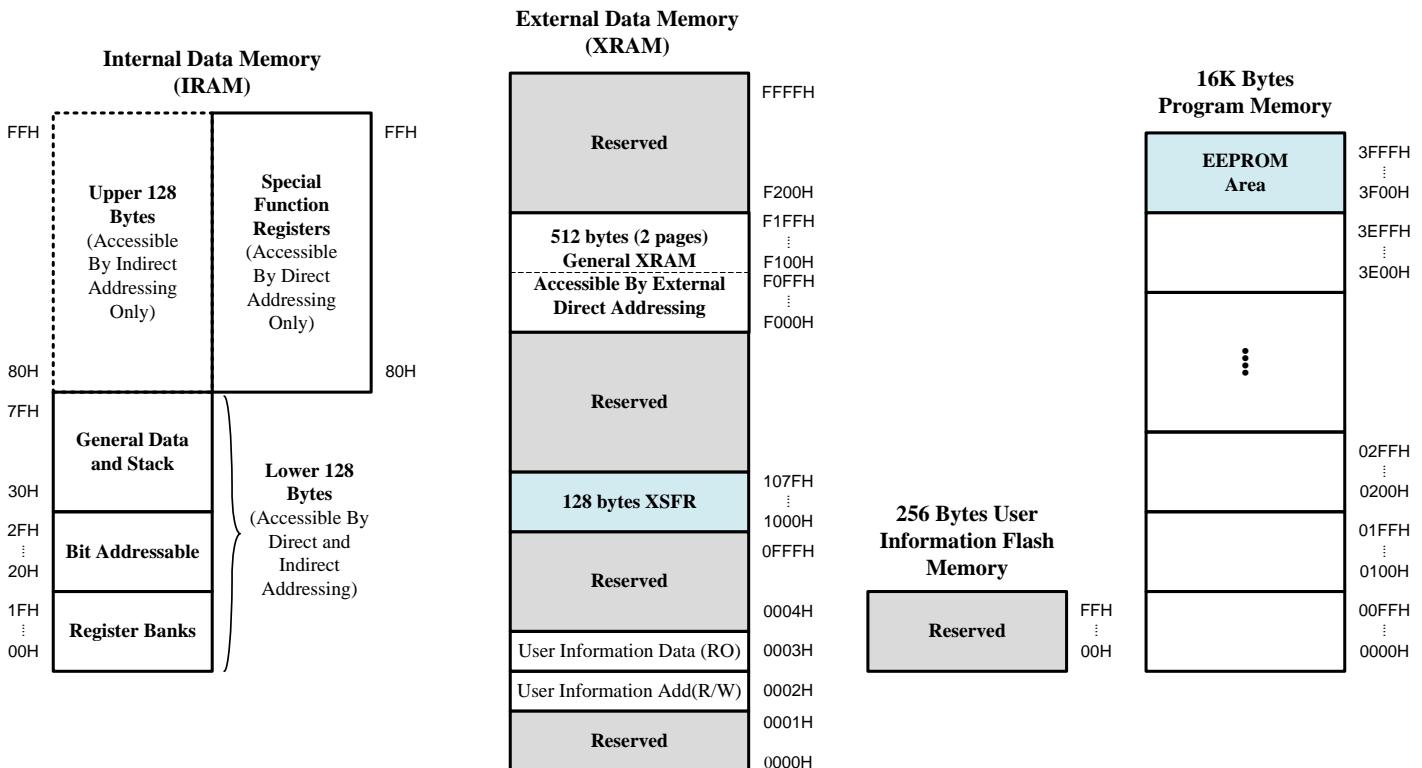
Memory architecture in MDSF40

10.1. Program Memory

The **MDSF40** contains 16K bytes of on-chip Flash memory for program storage. It contain 256 bytes information flash for store the user information. There are 128 bytes in the last page of program memory can be access by user for store any parameter. It's similar to EEPROM function and will be described in the EEPROM chapter.

Figure 5 Program Memory

16K Bytes Program Memory

EEPROM Area	3FFFH ⋮ 3F00H — Page 63
	3EFFH ⋮ 3E00H — Page 62
⋮	
	02FFH ⋮ 0200H — Page 2
	01FFH ⋮ 0100H — Page 1
	00FFH ⋮ 0000H — Page 0

64 page

256 Bytes User Information Flash Memory

Reserved	FFH ⋮ 00H

The architecture of flash memory
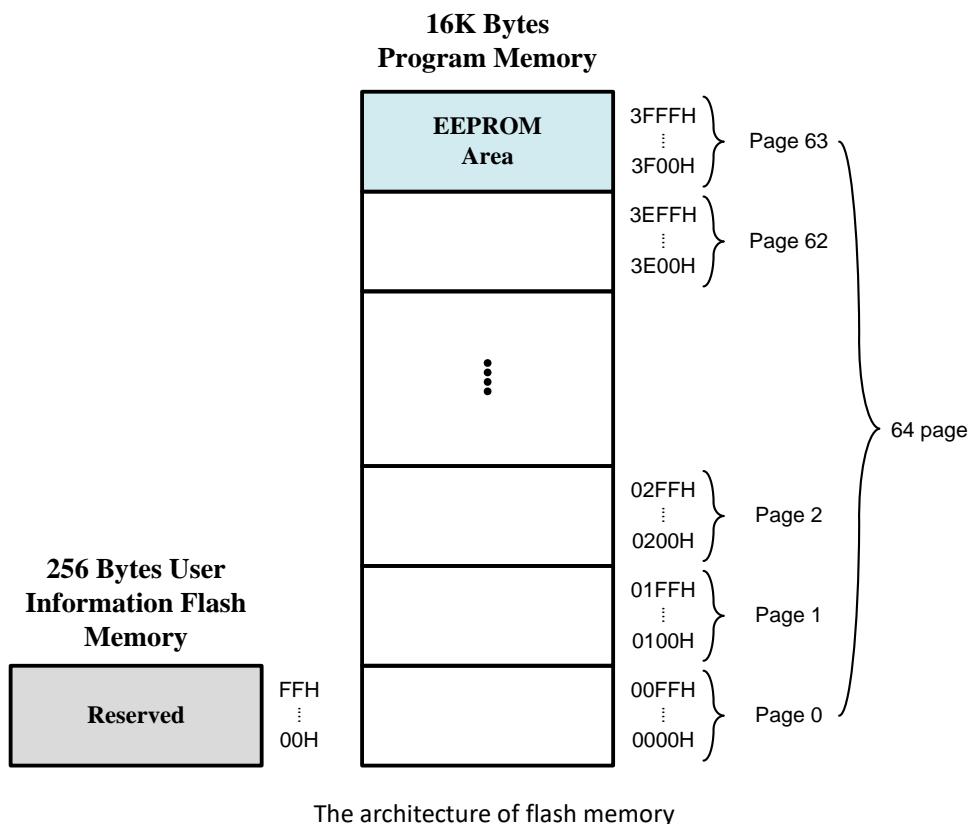
10.2. Data Memory

The **MDSF40** contains 256 bytes of general internal data memory (IRAM) and 512 bytes of external data memory (XRAM).

10.2.1 Internal Data Memory (IRAM)(00H~FFH)

The lower 128 bytes of IRAM may be accessed through both direct and indirect addressing. The upper 128 bytes of IRAM and the 128 bytes of SFR registers share the same address space. The upper 128 bytes of data memory may only be accessed using indirect addressing. The SFR registers can only be accessed through direct addressing. The lowest 32 bytes (00H -1FH) of data memory are grouped into 4 banks of 8 registers each. The **RS0** and **RS1** bits (**PSW**.3 and **PSW**.4) select which register bank is in use. Instructions using register addressing will only access the currently specified bank.

Figure 6 Internal Data Memory

Internal Data Memory
(IRAM)

FFH

Upper 128 Bytes
(Accessible By Indirect Addressing Only)

Special Function Registers
(Accessible By Direct Addressing Only)

FFH

80H

80H

7FH

General Data and Stack

30H

Lower 128 Bytes
(Accessible By Direct and Indirect Addressing)

2FH

Bit Addressable

20H

1FH

Register Banks

00H

The IRAM architecture
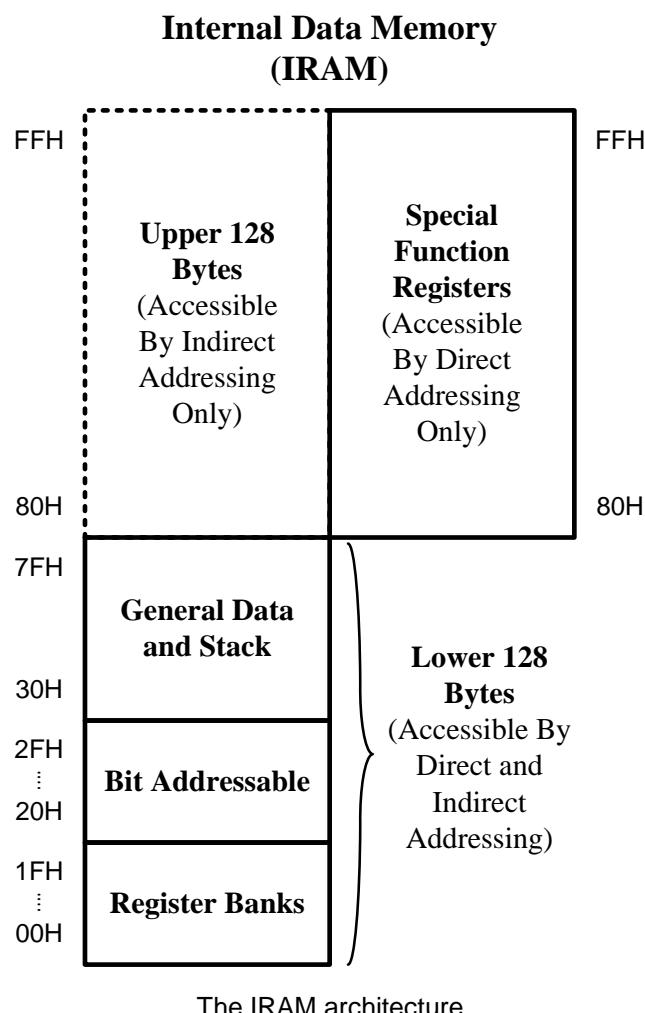
10.2.2 External Data Memory (XRAM)(F000H~F1FFH)

External addresses F000H to F1FFH contain the on-chip expanded SRAM. This 512 bytes external data memory can be accessed via external direct addressing mode (with **MOVX** instructions). The address space of instruction **MOVX** @Ri,A (i=0,1) is determined by **RCON**[7:0] of SFR 86H **RCON**(internal RAM control register). The **RCON**[7:0] can only be set the value of F0H (page0) or F1H (page1), and the default is F0H (page0). One page of XRAM is 256 bytes.

There are 128 bytes expend SFR (XSFR) in the expended region of the external data memory. The mapping address is form 1000H to 107FH and it provide more function for more application. The content of information flash can be read by assign the information address in the address 0002H of XRAM and the read out data is store in the space of address 0003H of XRAM.

Figure 7 External Data Memory
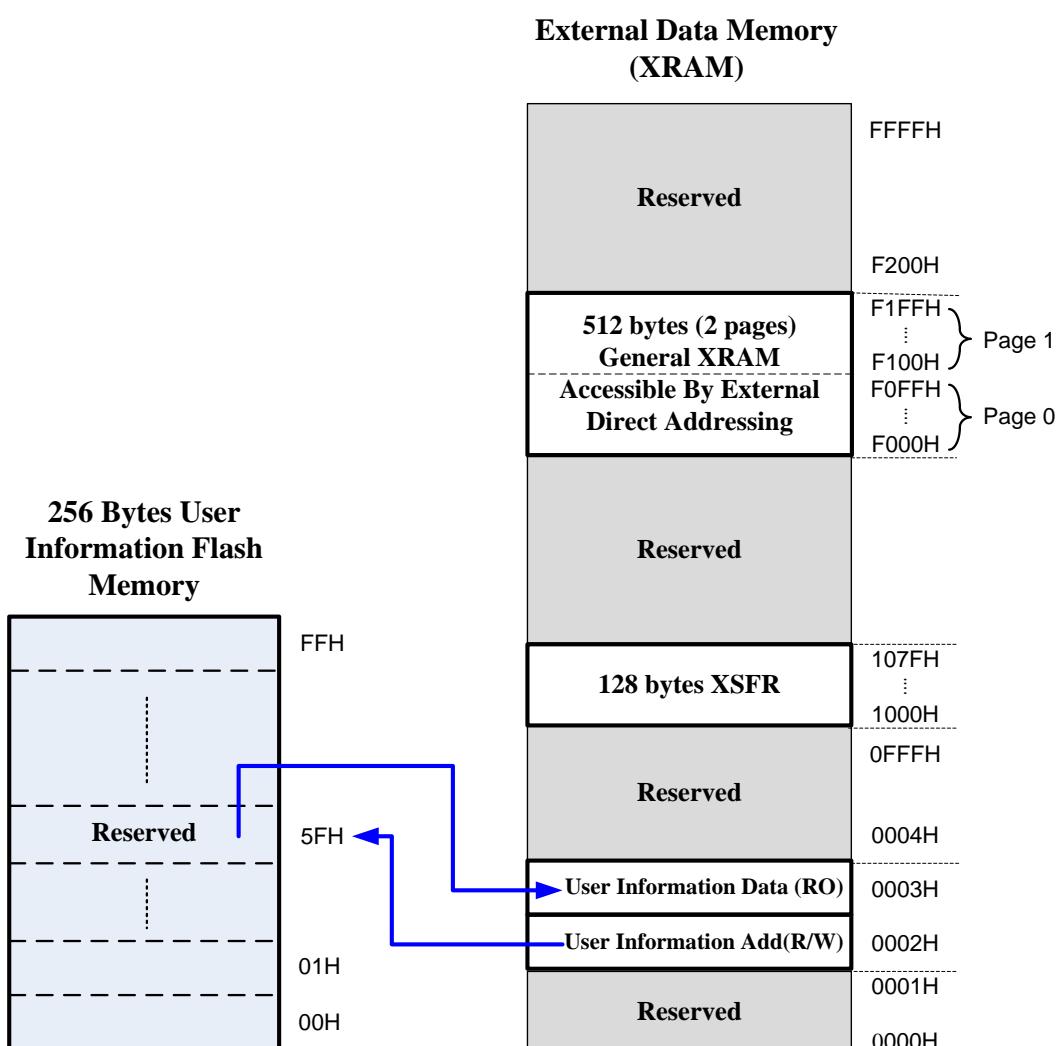
The XRAM architecture and an expression of read information content

11. Special Function Registers (SFR)

11.1 SFR Memory Map

Table 6 11.1 SFR Memory Map

	8	9	A	B	C	D	E	F	
F8	PINCONG1	PINCONG2	PINCONG3	PINCONG4	PINCONG5	PINCONG6	RSTS	TAKEY	FF
F0	B	PINSET1	PINSET2	PINSET3	PINSET4	PINSET5	PINSET6	PINSET7	F7
E8	IICS	IICCTL	IICA1	IICA2	SFR_PAGE	SP_CYC	AOCPCONT	OCPNCONT	EF
E0	ACC	MPWMDATL	MPWMDATH	MPWMCONT1	MPWMINV	MPWMDB	PI_GAIN	MPWMCONT2	E7
D8	VDCCONT	CAPT_L	CAPT_H	CAPH_L	CAPH_H	CAPCONT	PI_KT_L	PI_KT_H	DF
D0	PSW	PFCON	FOC_D1_L	FOC_D1_H	FOC_D2_L	FOC_D2_H	FOCCONT	PI_TMSR	D7
C8	T2CON	ADCOFST_L	ADCOFST_H	ADCAUTO_L	ADCAUTO_H				CF
C0	IRCON1	ADCSTR	ADCCONT	ADCD1	ADCD2	ADCDLY	ADCAUTO	PINCONG7	C7
B8	IEN1	IP1	IICRWD	SMO_D1_L	SMO_D1_H	SMO_D2_L	SMO_D2_H	MPWMCPSF	BF
B0	P3	SD_MODE	PI_MIN_LMT_L	PI_MIN_LMT_H	TL2	TH2	WDTC	WDTK	B7
A8	IEN0	IP0	PI_TR_L	PI_TR_H	PI_OUT_L	PI_OUT_H	PI_FB_L	PI_FB_H	AF
A0	P2	USER_LPF_L	USER_LPF_H	EEPROM	INI_ANG_DAT	INI_ANG_CTRL	PI_CMD_L	PI_CMD_H	A7
98	SCON	SBUF	SRELL	SRELH	IICEBT	PI_UI_L	PI_UI_H	MOTOR_CONT2	9F
90	P1	PI_KI_L	PI_KI_H	PI_KP_L	PI_KP_H	PI_MAX_LMT_L	PI_MAX_LMT_H	MOTOR_CONT1	97
88	TCON	TMOD	TL0	TL1	TH0	TH1	AUX	SYNC	8F
80	P0	SP	DP0L	DP0H	DP1L	DP1H	RCON	PCON	87
	0	1	2	3	4	5	6	7	

Table 7 SFR Descriptions

SYMBOL	DIRECT ADDRESS [L,H]		SFR_PAGE						
			0	1	2	3	4	5	6
MPWM									
MPWMDATA [L,H]	E1H	E2H	CYCLE	DUTY_U	DUTY_V	DUTY_W			
PI-Controller									
PI_KI[L,H]	91H	92H	IQ_KI	ID_KI	Spd_KI	PLL_KI	User_KI		
PI_KP [L,H]	93H	94H	IQ_KP	ID_KP	Spd_KP	PLL_KP	User_KP		
PI_KT [L,H]	DEH	DFH	IQ_KT	ID_KT	Spd_KT	PLL_KT	User_KT		
PI_TR [L,H]	AAH	ABH	IQ_TR	ID_TR	Spd_TR	PLL_TR			
PI_MAX_LMT [L,H]	95H	96H	IQ_MAX	ID_MAX	Spd_MAX	PLL_MAX	User_MAX		
PI_MIN_LMT [L,H]	B2H	B3H	IQ_MIN	ID_MIN	Spd_MIN	PLL_MIN	User_MIN		
PI_CMD[L,H]	A6H	A7H	IQ_CMD	ID_CMD	Spd_CMD	PLL_CMD	User_CMD		
PI_UI [L,H]	9DH	9EH	IQ_UI	ID_UI	Spd-UI	PLL-UI	User_UI		
PI_OUT [L,H]	ACH	ADH	IQ_OUT	ID_OUT	Spd-OUT	PLL-OUT	User_OUT		
PI_FB [L,H]	AEH	AFH	IQ_FB	ID_FB	Spd-FB	PLL-FB	User_FB		
Slide Mode Controller									
SMO_D1 [L,H]	BBH	BCH	GS	SMO-gain	angle base	Z-correct	SMO-angle	BanBan-gain	
SMO_D2 [L,H]	BDH	BEH	FS	SMO-filter	angle shift	MAXSMC_Err	SPEED		
ADC Offset Value									
ADCOSFST [L,H]	C9H	CAH	ADC1OS	ADC2OS					
ADCAUTO [L,H]	CBH	CCH		CH2(R)	CH3(R)				
Field Oriented Controller									
FOC_D1 [L,H]	D2H	D3H	V_{DC_NOW}	V_{DC_Normal}	$V_{DC\_Correct}$				
FOC_D2[L,H]	D4H	D5H	Q-axis V	D-axis V		AS	CPU_ANG	FOC-angle	SVPWM_amp
Independent General Low Pass Filter									
GEN_LPF[L,H]	A1H	A2H	GEN_gain	LPF_In	LPF_Out	Last_Out			
Initial Angle Estimated Controller									
INI_ANG_CTRL	A4H		Pattern 10	Pattern 32	Pattern 54				
EEPROM									
EEPROM	A3H		EE_ADDR	EE_DATA	EE_ACT				
CAPTURE									
CAPCONT	DDH		E_CAPCONT	I_CAPCONT					
CAPT [L,H]	D9H	DAH	EXT_CAPT	INT_CAPT					
CAPH[L,H]	DBH	DCH	EXT_CAPH	INT_CAPH					

11.2 SFR Reset Value

Table 8 SFR Reset Value

SYMBOL	DESCRIPTION	DIRECT ADDRESS	RESET VALUE
ACC	Accumulator	E0H	00H
ADCSTR	ADC Start Convert and Setting Register	C1H	00H
ADCCONT	ADC Control Register	C2H	83H
ADCD1	ADC Data Register 1	C3H	00H
ADCD2	ADC Data Register 2	C4H	00H
ADCDLY	ADC Sample Delay	C5H	33H
ADCOFST_L	ADC Data Offset Low byte	C9H	00H
ADCOFST_H	ADC Data Offset High byte	CAH	02H
ADCAUTO_L	ADC Auto Sample Data Low byte	CBH	00H
ADCAUTO_H	ADC Auto Sample Data High byte	CCH	00H
AUX	Auxiliary	8EH	11H
AOCPCONT	Analog OCP Control Register	EEH	C7H
B	B Register	F0H	00H
CAPCONT	Capture Control Register	DDH	03H
CAPT_L	Capture Total Count Low	D9H	00H
CAPT_H	Capture Total Count High	DAH	00H
CAPH_L	Capture High-level Count Low	DBH	00H
CAPH_H	Capture High-level Count High	DCH	00H
DPTR0:	Data Pointer 0 (2 bytes)		
DP0L	Data Pointer 0 Low	82H	00H
DP0H	Data Pointer 0 High	83H	00H
DPTR1:	Data Pointer 1 (2 bytes)		
DP1L	Data Pointer 1 Low	84H	00H
DP1H	Data Pointer 1 High	85H	00H
EEPROM	D&Q -Axis Voltage Offset Low byte	A3H	00H
FOCCONT	Field Oriented Control Register	D6H	00H
FOC_D1_L	Field Oriented Control Data1 Low byte	D2H	00H
FOC_D1_H	Field Oriented Control Data1 High byte	D3H	00H
FOC_D2_L	Field Oriented Control Data2 Low byte	D4H	00H
FOC_D2_H	Field Oriented Control Data2 High byte	D5H	00H
IEN0	Interrupt Enable Register 0	A8H	00H
IEN1	Interrupt Enable Register 1	B8H	00H

IP0	Interrupt Priority Register 0	A9H	00H
IP1	Interrupt Priority Register 1	B9H	00H
IRCON1	Interrupt Request Register 1	C0H	00H
IICS	IIC Status Register	E8H	00H
IICCTRL	IIC Control Register	E9H	04H
IICA1	IIC Address 1 Register	EAH	A0H
IICA2	IIC Address 2 Register	EBH	60H
IICRWD	IIC Read Write Register	BAH	00H
IICEBT	IIC Enable Bus Transaction Register	9CH	00H
INI_ANG_DAT	Initial Angle Estimated Data Register	A4H	EBH
INI_ANG_CTRL	Initial Angle Estimated Control Register	A5H	18H
MOTOR_CONT1	Motor Control Register 1	97H	00H
MOTOR_CONT2	Motor Control Register 2	9FH	A4H
MOTOR_CONT3	Motor Control Register 3	C6H	00H
MPWMCONT1	MPWM Control Register 1	E3H	00H
MPWMDATL	MPWM Data Low	E1H	00H
MPWMDATH	MPWM Data High	E2H	00H
MPWMDB	Motor PWM Dead-band Register	E5H	78H
MPWMINV	MPWM Inverse Selection Register	E4H	00H
MPWMCONT2	MPWM Control Register 2	E7H	00H
MPWMCPSF	Motor PWM Compensation Factor Register	BFH	00H
OCPNCONT	OCP Control Register	EFH	85H
P0	Port 0	80H	FFH
P1	Port 1	90H	FFH
P2	Port 2	A0H	FFH
P3	Port 3	B0H	FFH
PCON	Power Control Register	87H	00H
PSW	Program Status Word Register	D0H	00H
PFCON	Peripheral Frequency Control Register	D1H	00H
PINCONG1	Pin Configure Register 1	F8H	AAH
PINCONG2	Pin Configure Register 2	F9H	AAH
PINCONG3	Pin Configure Register 3	FAH	A0H
PINCONG4	Pin Configure Register 4	FBH	AAH
PINCONG5	Pin Configure Register 5	FCH	AAH
PINCONG6	Pin Configure Register 6	FDH	A0H
PINCONG7	Pin Configure Register 7	C7H	0AH
PINSET1	Pin I/O Setting Register 1	F1H	AAH

PINSET2	Pin I/O Setting Register 2	F2H	AAH
PINSET3	Pin I/O Setting Register 3	F3H	0AH
PINSET4	Pin I/O Setting Register 4	F4H	00H
PINSET5	Pin I/O Setting Register 5	F5H	80H
PINSET6	Pin I/O Setting Register 6	F6H	0AH
PINSET7	Pin I/O Setting Register 7	F7H	B0H
PI_GAIN	PI-Control Error x16	E6H	F7H
PI_KT_L	PI-control KT Data Low byte	DEH	00H
PI_KT_H	PI-control KT Data High byte	DFH	00H
PI_TMSR	PI-control Tracking Mode Select Register	D7H	00H
PI_MIN_LMT_L	PI-control Minimal Limit Data Low byte	B2H	01H
PI_MIN_LMT_H	PI-control Minimal Limit Data High byte	B3H	80H
PI_TR_L	PI-control TR Data Low byte	AAH	00H
PI_TR_H	PI-control TR Data High byte	ABH	00H
PI_OUT_L	PI-control Output Data Low byte	ACH	00H
PI_OUT_H	PI-control Output Data High byte	ADH	00H
PI_FB_L	PI-control Feedback Data Low byte	AEH	00H
PI_FB_H	PI-control Feedback Data High byte	AFH	00H
PI_CMD_L	PI-control Command Data Low byte	A6H	00H
PI_CMD_H	PI-control Command Data High byte	A7H	00H
PI-UI_L	PI-control Integral Data Low byte	9DH	00H
PI-UI_H	PI-control Integral Data High byte	9EH	00H
PI_KI_L	PI-control KI Data Low byte	91H	00H
PI_KI_H	PI-control KI Data High byte	92H	00H
PI_KP_L	PI-control KP Data Low byte	93H	00H
PI_KP_H	PI-control KP Data High byte	94H	00H
PI_MAX_LMT_L	PI-control Minimal Limit Data Low byte	95H	FFH
PI_MAX_LMT_H	PI-control Minimal Limit Data High byte	96H	7FH
RCON	Internal RAM Control Register	86H	F0H
RSTS	Reset Source Register	FEH	0AH
SFR_PAGE	Special Function Registers Page	ECH	00H
SP_CYC	Speed Control Loop Cycle	EDH	26H
SCON	Serial Port Control Register	98H	00H
SBUF	Serial Port Data Buffer	99H	00H
SRELL	Serial Port Reload Register High	9AH	00H
SRELH	Serial Port Reload Register High	9BH	00H
SP	Stack Pointer	81H	07H

SMO_D1_L	Sliding Mode Observer Data1 Low Byte	BBH	----
SMO_D1_H	Sliding Mode Observer Data1 High Byte	BCH	----
SMO_D2_L	Sliding Mode Observer Data2 Low Byte	BDH	00H
SMO_D2_H	Sliding Mode Observer Data2 High Byte	BEH	00H
SYNC	MOC Sync Register	8FH	00H
T2CON	Timer 2 Control Register	C8H	00H
TAKEY	Time Access Key Register	FFH	00H
TCON	Timer 0/1 Control Register	88H	00H
TH0	Timer 0 High byte	8CH	00H
TH1	Timer 1 High byte	8DH	00H
TH2	Timer 2 High byte	B5H	00H
TL0	Timer 0 Low byte	8AH	00H
TL1	Timer 1 Low byte	8BH	00H
TL2	Timer 2 Low byte	B4H	00H
TMOD	Timer 0/1 Mode Register	89H	00H
GEN_LPF_L	User Low Pass Filter Data Low byte	A1H	00H
GEN_LPF _H	User Low Pass Filter Data High byte	A2H	00H
WDTC	Watchdog Timer Control Register	B6H	04H
WDTK	Watchdog Timer Refresh Key	B7H	00H

11.3 XSFR Memory Map

Table 9 XSFR Memory Map

	8	9	A	B	C	D	E	F	
1078									107F
1070	Z-alpha_L	Z-alpha_H	ES_I-alpha_L	ES_I-alpha_H	ES_E-alpha_L	ES_E-alpha_H			1077
1068	Z-beta_L	Z-beta_H	ES_I-beta_L	ES_I-beta_H	ES_E-beta_L	ES_E-beta_H			106F
1060	Ia_L	Ia_H	I-alpha_L	I-alpha_H	V-alpha_L	V-alpha_H	Va_L	Va_H	1067
1058	Ib_L	Ib_H	I-beta_L	I-beta_H	V-beta_L	V-beta_H	Vb_L	Vb_H	105F
1050									1057
1048									104F
1040	IR_DOUT0	IR_DOUT1	IR_DOUT2	IR_DOUT3	IR_DOUT4	IR_DOUT5			1047
1038	IR_DEC_SET	IR_DEC_CTRL	IR_HEADER_Z1_L	IR_HEADER_Z1_H	IR_HEADER_Z2_L	IR_HEADER_Z2_H	IR_STOP_Z_L	IR_STOP_Z_H	103F
1030	MD_MODE	MD_CONT	MD0	MD1	MD2	MD3	MD4	MD5	1037
1028	SOFT_RST_KEY	SOFT_RST_EN							102F
1020	IPWM_MAX_L	IPWM_MAX_H	IPWM_DUTY_L	IPWM_DUTY_H	IPWM_CTRL			FGCTRL	1027
1018	CRC_CTRL	CRC_DIN	CRC_DOUT_L	CRC_DOUT_H	CRC_STR_BANK	CRC_END_BANK			101F
1010									1017
1008									100F
1000									1007
	0	1	2	3	4	5	6	7	

11.4 XSFR Reset Value

Table 10 XSFR Reset Value

SYMBOL	DESCRIPTION	DIRECT ADDRESS	RESET VALUE
CRC_CTRL	CRC Control Register	1018H	00H
CRC_DIN	CRC Input Data Register	1019H	00H
CRC_DOUT_L	CRC Output Remainder Low Byte Data Register	101AH	00H
CRC_DOUT_H	CRC Output Remainder High Byte Data Register	101BH	00H
CRC_STR_BANK	Start Bank Index for Flash Bank CRC Computation	101CH	00H
CRC_END_BANK	End Bank Index for Flash Bank CRC Computation	101DH	00H
FGCTRL	Function Generator Control Register	1027H	00H
IR_DOUT0	IR Decode Output Data Byte0	1040H	00H
IR_DOUT1	IR Decode Output Data Byte1	1041H	00H
IR_DOUT2	IR Decode Output Data Byte2	1042H	00H
IR_DOUT3	IR Decode Output Data Byte3	1043H	00H
IR_DOUT4	IR Decode Output Data Byte4	1044H	00H
IR_DOUT5	IR Decode Output Data Byte5	1045H	00H
IR_DEC_SET	IR Data Decode Setting Register	1038H	00H
IR_DEC_CTRL	IR Data Decode Control Register	1039H	00H
IR_HEADER_Z1_L	IR Data HEADER Zone1 Low Byte Cycles Number	103AH	80H
IR_HEADER_Z1_H	IR Data HEADER Zone1 High Byte Cycles Number	103BH	BBH
IR_HEADER_Z2_L	IR Data HEADER Zone2 Low Byte Cycles Number	103CH	00H
IR_HEADER_Z2_H	IR Data HEADER Zone2 High Byte Cycles Number	103DH	7DH
IR_STOP_Z_L	IR Data STOP Zone Low Byte Cycles Number	103EH	80H
IR_STOP_Z_H	IR Data STOP Zone High Byte Cycles Number	103FH	BBH
IPWM_MAX_L	Independent General PWM Max. Low Byte	1020H	02H
IPWM_ MAX _H	Independent General PWM Max. High Byte	1021H	00H
IPWM_DUTY_L	Independent General PWM Duty Low Byte	1022H	FFH
IPWM_ DUTY _H	Independent General PWM Duty High Byte	1023H	FFH
IPWM_CTRL	Independent General PWM Control Register	1024H	00H
MD_MODE	MDU Mode Control Register	1030H	10H
MD_CTRL	MDU Control Register	1031H	00H
MD0	Multiplication Division Register 0	1032H	00H
MD1	Multiplication Division Register 1	1033H	00H
MD2	Multiplication Division Register 2	1034H	00H
MD3	Multiplication Division Register 3	1035H	00H
MD4	Multiplication Division Register 4	1036H	00H

MD5	Multiplication Division Register 5	1037H	00H
SOFT_RST_KEY	Software Reset Key Register	1028H	00H
SOFT_RST_EN	Software Reset Enable Register	1029H	00H
ES_I-alpha_L	Estimate Current Iα Low Byte Data Register	1072H	00H
ES_I-alpha_H	Estimate Current Iα High Byte Data Register	1073H	00H
ES_E-alpha_L	Estimate EEMF Eα Low Byte Data Register	1074H	00H
ES_E-alpha_H	Estimate EEMF Eα High Byte Data Register	1075H	00H
ES_I-beta_L	Estimate Current Iβ Low Byte Data Register	106AH	00H
ES_I- beta _H	Estimate Current Iβ High Byte Data Register	106BH	00H
ES_E- beta _L	Estimate EEMF Eβ Low Byte Data Register	106CH	00H
ES_E- beta _H	Estimate EEMF Eβ High Byte Data Register	106DH	00H
Ia_L	Phase A Current Low Byte Data Register	1060H	00H
Ia_H	Phase A Current High Byte Data Register	1061H	00H
I-alpha_L	α-axis Stator Current Low Byte Data Register	1062H	00H
I-alpha_H	α-axis Stator Current High Byte Data Register	1063H	00H
Ib_L	Phase B Current Low Byte Data Register	1058H	00H
Ib_H	Phase B Current High Byte Data Register	1059H	00H
I-beta_L	β-axis Stator Current Low Byte Data Register	105AH	00H
I-beta_H	β-axis Stator Current High Byte Data Register	105BH	00H
V-alpha_L	α-axis Stator Voltage Low Byte Data Register	1060H	00H
V-alpha_H	α-axis Stator Voltage High Byte Data Register	1061H	00H
Va_L	Phase A Drive Voltage Low Byte Data Register	1062H	00H
Va_H	Phase A Drive Voltage High Byte Data Register	1063H	00H
V-beta_L	β-axis Stator Voltage Low Byte Data Register	105CH	00H
V-beta_H	β-axis Stator Voltage High Byte Data Register	105DH	00H
Vb_L	Phase B Drive Voltage Low Byte Data Register	105EH	00H
Vb_H	Phase B Drive Voltage High Byte Data Register	105FH	00H
Z-alpha_L	The Z gain of EEMF Eα Low Byte Data Register	1070H	00H
Z-alpha_H	The Z gain of EEMF Eα High Byte Data Register	1071H	00H
Z-beta_L	The Z gain of EEMF Eβ Low Byte Data Register	1068H	00H
Z-beta_H	The Z gain of EEMF Eβ High Byte Data Register	1069H	00H

12. Instruction Set

Table 11 12 The **MDSF40** is fully binary compatible with the MCS-51 instruction set.

Arithmetic operations	Description	Bytes	Cycles	Hex Code
ADD A,Rn	Add register to accumulator	1	1	0x28-0x2F
ADD A,direct	Add directly addressed data to accumulator	2	2	0x25
ADD A,@Ri	Add indirectly addressed data to accumulator	1	2	0x26-0x27
ADD A,#data	Add immediate data to accumulator	2	2	0x24
ADDC A,Rn	Add register to accumulator with carry	1	1	0x38-0x3F
ADDC A,direct	Add directly addressed data to accumulator with carry	2	2	0x35
ADDC A,@Ri	Add indirectly addressed data to accumulator with carry	1	2	0x36-0x37
ADDC A,#data	Add immediate data to accumulator with carry	2	2	0x34
SUBB A,Rn	Subtract register from accumulator with borrow	1	1	0x98-0x9F
SUBB A,direct	Subtract directly addressed data from accumulator with borrow	2	2	0x95
SUBB A,@Ri	Subtract indirectly addressed data from accumulator with borrow	1	2	0x96-0x97
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2	0x94
INC A	Increment accumulator	1	1	0x04
INC Rn	Increment register	1	2	0x08-0x0F
INC direct	Increment directly addressed location	2	3	0x05
INC @Ri	Increment indirectly addressed location	1	3	0x06-0x07
INC DPTR	Increment data pointer	1	1	0xA3
DEC A	Decrement accumulator	1	1	0x14
DEC Rn	Decrement register	1	2	0x18-0x1F
DEC direct	Decrement directly addressed location	2	3	0x15
DEC @Ri	Decrement indirectly addressed location	1	3	0x16-0x17
MUL AB	Multiply A and B	1	5	0xA4
DIV	Divide A by B	1	5	0x84
DA A	Decimally adjust accumulator	1	1	0xD4

Logic operations	Description	Bytes	Cycles	Hex Code
ANL A,Rn	AND register to accumulator	1	1	0x58-0x5F
ANL A,direct	AND directly addressed data to accumulator	2	2	0x55
ANL A,@Ri	AND indirectly addressed data to accumulator	1	2	0x56-0x57
ANL A,#data	AND immediate data to accumulator	2	2	0x54
ANL direct,A	AND accumulator to directly addressed location	2	3	0x52
ANL direct,#data	AND immediate data to directly addressed location	3	4	0x53
ORL A,Rn	OR register to accumulator	1	1	0x48-0x4F
ORL A,direct	OR directly addressed data to accumulator	2	2	0x45
ORL A,@Ri	OR indirectly addressed data to accumulator	1	2	0x46-0x47
ORL A,#data	OR immediate data to accumulator	2	2	0x44
ORL direct,A	OR accumulator to directly addressed location	2	3	0x42
ORL direct,#data	OR immediate data to directly addressed location	3	4	0x43
XRL A,Rn	Exclusive OR register to accumulator	1	1	0x68-0x6F
XRL A,direct	Exclusive OR directly addressed data to accumulator	2	2	0x65
XRL A,@Ri	Exclusive OR indirectly addressed data to accumulator	1	2	0x66-0x67
XRL A,#data	Exclusive OR immediate data to accumulator	2	2	0x64
XRL direct,A	Exclusive OR accumulator to directly addressed location	2	3	0x62
XRL direct,#data	Exclusive OR immediate data to directly addressed location	3	4	0x63
CLR A	Clear accumulator	1	1	0xE4
CPL A	Complement accumulator	1	1	0xF4
RL A	Rotate accumulator left	1	1	0x23
RLC A	Rotate accumulator left through carry	1	1	0x33
RR A	Rotate accumulator right	1	1	0x03
RRC A	Rotate accumulator right through carry	1	1	0x13
SWAP A	Swap nibbles within the accumulator	1	1	0xC4

Data transfer operations	Description	Bytes	Cycles	Hex Code
MOV A,Rn	Move register to accumulator	1	1	0xE8-0xEF
MOV A,direct	Move directly addressed data to accumulator	2	2	0xE5
MOV A,@Ri	Move indirectly addressed data to accumulator	1	2	0xE6-0xE7
MOV A,#data	Move immediate data to accumulator	2	2	0x74
MOV Rn,A	Move accumulator to register	1	2	0xF8-0xFF
MOV Rn,direct	Move directly addressed data to register	2	4	0xA8-0xAF
MOV Rn,#data	Move immediate data to register	2	2	0x78-0x7F
MOV direct,A	Move accumulator to direct	2	3	0xF5
MOV direct,Rn	Move register to direct	2	3	0x88-0x8F
MOV direct1,direct2	Move directly addressed data to directly addressed location	3	4	0x85
MOV direct,@Ri	Move indirectly addressed data to directly addressed location	2	4	0x86-0x87
MOV direct,#data	Move immediate data to directly addressed location	3	3	0x75
MOV @Ri,A	Move accumulator to indirectly addressed location	1	3	0xF6-0xF7
MOV @Ri,direct	Move directly addressed data to indirectly addressed location	2	5	0xA6-0xA7
MOV @Ri,#data	Move immediate data to in directly addressed location	2	3	0x76-0x77
MOV DPTR,#data16	Load data pointer with a 16-bit immediate	3	3	0x90
MOVC A,@A+DPTR	Load accumulator with a code byte relative to DPTR	1	3	0x93
MOVC A,@A+PC	Load accumulator with a code byte relative to PC	1	3	0x83
MOVX A,@Ri	Move external RAM (8-bit address) to accumulator	1	3	0xE2-0xE3
MOVX A,@DPTR	Move external RAM (16-bit address) to accumulator	1	3	0xE0
MOVX @Ri,A	Move accumulator to external RAM (8-bit address)	1	4	0xF2-0xF3
MOVX @DPTR,A	Move accumulator to external RAM (16-bit address)	1	4	0xF0
PUSH direct	Push directly addressed data onto stack	2	4	0xC0

POP direct	Pop directly addressed location from stack	2	3	0xD0
XCH A,Rn	Exchange register with accumulator	1	2	0xC8-0xCF
XCH A,direct	Exchange directly addressed location with accumulator	2	3	0xC5
XCH A,@Ri	Exchange indirect RAM with accumulator	1	3	0xC6-0xC7
XCHD A,@Ri	Exchange low-order nibbles of indirect and accumulator	1	3	0xD6-0xD7

Program branches	Description	Bytes	Cycles	Hex Code
ACALL addr11	Absolute subroutine call	2	6	xxx10001b
LCALL addr16	Long subroutine call	3	6	0x12
RET	Return from subroutine	1	4	0x22
RETI	Return from interrupt	1	4	0x32
AJMP addr11	Absolute jump	2	3	xxx00001b
LJMP addr16	Long jump	3	4	0x02
SJMP rel	Short jump (relative address)	2	3	0x80
JMP @A+DPTR	Jump indirect relative to the DPTR	1	2	0x73
JZ rel	Jump if accumulator is zero	2	3	0x60
JNZ rel	Jump if accumulator is not zero	2	3	0x70
JC rel	Jump if carry flag is set	2	3	0x40
JNC	Jump if carry flag is not set	2	3	0x50
JB bit,rel	Jump if directly addressed bit is set	3	4	0x20
JNB bit,rel	Jump if directly addressed bit is not set	3	4	0x30
JBC bit,rel	Jump if directly addressed bit is set and clear bit	3	4	0x10
CJNE A,direct,rel	Compare directly addressed data to accumulator and jump if not equal	3	4	0xB5
CJNE A,#data,rel	Compare immediate data to accumulator and jump if not equal	3	4	0xB4
CJNE Rn,#data,rel	Compare immediate data to register and jump if not equal	3	4	0xB8-0xBF
CJNE @Ri,#data,rel	Compare immediate to indirect RAM and jump if not equal	3	4	0xB6-0xB7
DJNZ Rn,rel	Decrement register and jump if not zero	2	3	0xD8-0xDF
DJNZ direct,rel	Decrement directly addressed location and jump if not zero	3	4	0xD5
NOP	No operation	1	1	0

Boolean manipulation	Description	Bytes	Cycles	Hex Code
CLR C	Clear carry flag	1	1	0xC3
CLR bit	Clear directly addressed bit	2	3	0xC2
SETB C	Set carry flag	1	1	0xD3
SETB bit	Set directly addressed bit	2	3	0xD2
CPL C	Complement carry flag	1	1	0xB3
CPL bit	Complement directly addressed bit	2	3	0xB2
ANL C,bit	AND directly addressed bit to carry flag	2	2	0x82
ANL C,/bit	AND complement of directly addressed bit to carry	2	2	0xB0
ORL C,bit	OR directly addressed bit to carry flag	2	2	0x72
ORL C,/bit	OR complement of directly addressed bit to carry	2	2	0xA0
MOV C,bit	Move directly addressed bit to carry flag	2	2	0xA2
MOV bit,C	Move carry flag to directly addressed bit	2	3	0x92

13. MCU

Table 12 8051 Engine

SFR	Description	address	Reset value
ACC	Accumulator	E0H	00H
B	B Register	F0H	00H
PSW	Program Status Word Register	D0H	00H
SP	Stack Pointer	81H	07H
DP0H	Data Pointer 0 High	83H	00H
DP0L	Data Pointer 0 Low	82H	00H
DP1H	Data Pointer 1 High	85H	00H
DP1L	Data Pointer 1 Low	84H	00H
AUX	Auxiliary	8EH	11H
RCON	Internal RAM Control Register	86H	F0H

13.1.1 Accumulator (ACC)

The most important of all special function registers, that's the first comment about **Accumulator** which is also known as **ACC** or **A.** The **Accumulator** (sometimes referred to as Register A also) holds the result of most of arithmetic and logic operations.

Table 13 Accumulator (ACC) SFR

ACC			Address = E0H				Reset Value = 0x00H	
Accumulator								
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.1.2 B Register (B)

The **B** register is used during multiplying and division instructions. It can also be used as a scratch-pad register to hold temporary data.

Table 14 B Register (B)

B			Address = F0H				Reset Value = 0x00H	
B Register								
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.1.3 Program Status Word Register (PSW)

The **PSW** register contains status bits that reflect the current state of the CPU. Note that the Parity bit can only be modified by hardware upon the state of **ACC** register.

Table 15 Program Status Word Register (PSW)

PSW			Address = D0H				Reset Value = 0x00H	
Program Status Word Register								
	CY	AC	F0	RS1	RS0	OV	F1	P
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

CY	Carry flag :
	Carry bit in arithmetic operations and accumulator for Boolean operations.
AC	Auxiliary Carry flag :
	Set if there is a carry-out from third bit of Accumulator in BCD Operations.
F0	General purpose Flag0 :
	General purpose flag available for user.
RS1	Register bank select control bit 1, used to select working register bank.
RS0	Register bank select control bit 0, used to select working register bank.
OV	Overflow flag :
	Set in case of overflow in Accumulator during arithmetic operations.
F1	General purpose Flag 1 :
	General purpose flag available for user.
P	Parity flag :
	Reflects the number of '1's in the Accumulator.
	P = '1' if Accumulator contains an odd number of '1's
	P = '0' if Accumulator contains an even number of '1's

The state of **RS1** and **RS0** bits selects the working register bank as follows:

Table 16 **RS1** and **RS0**

RS1	RS0	Selected Register Bank	Location
0	0	Bank 0	00H – 07H
0	1	Bank 1	08H – 0FH
1	0	Bank 2	10H – 17H
1	1	Bank 3	18H – 1FH

13.1.4 Stack Pointer (SP)

This register points to the top of stack in internal data memory space. It is used to store the return address of program before executing interrupt routine or subprograms. The **SP** is incremented before executing **PUSH** or **CALL** instruction and it is decremented after executing **POP** or **RET(I)** instruction (it always points the top of stack). A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08.

Table 17 Stack Pointer (SP)

SP		Address = 81H				Reset Value = 0x07H		
Stack Pointer								
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.1.5 Data Pointer 0 (DP0)

These registers are intended to hold 16-bit address in the indirect addressing mode used by **MOVX** (move external memory), **MOVC** (move program memory) or **JMP** (computed branch) instructions. They may be manipulated as 16-bit register or as two separate 8-bit registers. **DP0H** holds higher byte and **DP0L** holds lower byte of indirect address.

It is generally used to access external code or data space, e.g.:

■ **MOVCA**,@**A+DPTR** (code space)

■ **MOVA**,@**DPTR** (data space)

Table 18 Data Pointer 0 (DP0)

DP0L		Address = 82H				Reset Value = 0x00H		
Data Pointer 0 Low Byte								
	DP0L[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DP0H		Address = 83H				Reset Value = 0x00H		
Data Pointer 0 High Byte								
	DP0H[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.1.6 Data Pointer 1 (DP1)

The dual data pointer accelerates the movement of block data. The standard **DPTR** is a 16-bit register that is used to address external memory, or peripherals. The standard data pointer is called **DPTR0** and the second data pointer is called **DPTR1**. The data pointer select bit chooses the active pointer. The data pointer select bit (**DPS**) is located in the LSB of **AUX** register (AUX.1).

The user switches between **DPTR0** and **DPTR1** by toggling the **DPS** bit. All DPTR-related instructions use the currently selected **DPTR** for any activity.

Table 19 Data Pointer 1 (DP1)

DP1L			Address = 84H			Reset Value = 0x00H	
Data Pointer 1Low Byte							
	DP1L[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DP1H			Address = 85H			Reset Value = 0x00H	
Data Pointer 1 High Byte							
	DP1H[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.1.7 Auxiliary Register (AUX)

Table 20 Auxiliary Register (AUX)

AUX			Address = 8EH			Reset Value = 0x11H	
Auxiliary Register							
	LVD_EN	LVD	-----	ITS	SMOD	BRS	DPS	CP
Bit	7	6	5	4	3	2	1	0
Type	R/W	R	X	R/W	R/W	R/W	R/W	R
LVD_EN	Low voltage detect enable :						
	1: Enable						
LVD	Low voltage detect status. :						
	1:Low voltage occur						
ITS	MCU instruction timing select. :						
	0:1T						
	1:2T						
SMOD	Serial Port (UART) baud rate select.						
BRS	Serial Port (UART) baud rate generator select.						
DPS	Data pointer register select :						
	0 : Select DPTR Register DP0H, DP0L						
	1 : Select DPTR Register DP1H, DP1L						
CP	Code protect :						
	0 : Non-protect						
	1: Protect						

13.1.8 Internal RAM Control Register (RCON)

512 bytes of on-chip expanded RAM are provided and can be accessed by external memory addressing method only (instruction **MOVX**). The address space of instruction **MOVX** @Ri,**A** (i= 0,1) is determined by **RCON**[7:0] of **RCON**. The **RCON**[7:0] can only be set the value of F0H (page0) or F1H (page1), and the default is F0H (page0). One page of XRAM is 256 bytes.

Table 21 Internal RAM Control Register (RCON)

RCON			Address = 86H			Reset Value = 0xF0H	
Internal RAM Control Register							
	RCON[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.2 GPIO

Four I/O ports are available: **Port0**, **Port1**, **Port2**, and **Port3**.

All 32port pins on **MDSF40** can configure to one of four modes : quasi-bidirectional (standard 8051 port outputs),push-pull output, open drain output, or input-only. All port pins default to input-only mode after reset.

Two configuration registers (**PINSETx**, **PINCONGx**) for each port select the output mode for each port pin.

Table 22 GPIO

SFR	Description	address	Reset value
P0	Port 0	80H	FFH
P1	Port 1	90H	FFH
P2	Port 2	A0H	FFH
P3	Port 3	B0H	FFH
PINCONG1	Pin Configure Register 1	F8H	AAH
PINCONG2	Pin Configure Register 2	F9H	AAH
PINCONG3	Pin Configure Register 3	FAH	A0H
PINCONG4	Pin Configure Register 4	FBH	AAH
PINCONG5	Pin Configure Register 5	FCH	AAH
PINCONG6	Pin Configure Register 6	FDH	A0H
PINCONG7	Pin Configure Register 7	C7H	0AH
PINSET1	Pin I/O Setting Register 1	F1H	AAH
PINSET2	Pin I/O Setting Register 2	F2H	AAH
PINSET3	Pin I/O Setting Register 3	F3H	0AH
PINSET4	Pin I/O Setting Register 4	F4H	00H
PINSET5	Pin I/O Setting Register 5	F5H	80H
PINSET6	Pin I/O Setting Register 6	F6H	0AH
PINSET7	Pin I/O Setting Register 7	F7H	B0H

13.2.1 Port

Table 23 Port

P0		Address = 80H					Reset Value = 0XFFH	
Port 0								
	-----	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W
P1		Address = 90H					Reset Value = 0XFFH	
Port 1								
	-----	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W
P2		Address = A0H					Reset Value = 0XFFH	
Port 2								
	P2.7	P2.6	P2.5	P2.4	P2.3	-----	-----	-----
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	X	X	X
P3		Address = B0H					Reset Value = 0XFFH	
Port 3								
	-----	-----	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

13.2.2 Pin Configure Register (PINCONG)

Table 24 13.2.2 Pin Configure Register (PINCONG)

PINCONG1		Address = F8H				Reset Value = 0xAAH	
Pin Configure Register 1							
	CH4CONG[1:0]		CH5CONG[1:0]		CH6CONG[1:0]		CH7CONG[1:0]
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
00 :	Quasi-bidirectional(standard 8051 port outputs)							
01 :	Push-pull output							
10 :	Input-only (High impedance)							
11 :	Open drain output							

PINCONG2		Address = F9H				Reset Value = 0xAAH	
Pin Configure Register 2							
	CH0CONG[1:0]		CH1CONG[1:0]		CH2CONG[1:0]		CH3CONG[1:0]
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
00 :	Quasi-bidirectional(standard 8051 port outputs)							
01 :	Push-pull output							
10 :	Input-only (High impedance)							
11 :	Open drain output							

PINCONG3		Address = FAH				Reset Value = 0xA0H	
Pin Configure Register 3							
	XCONG[1:0]		UCONG[1:0]		XTAL**O**CONG[1:0]		XTAL**I**CONG[1:0]
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
00 :	Quasi-bidirectional(standard 8051 port outputs)							
01 :	Push-pull output							
10 :	Input-only (High impedance)							
11 :	Open drain output							

PINCONG4		Address = FBH				Reset Value = 0xAAH	
Pin Configure Register 4							
	ZCONG[1:0]		WCONG[1:0]		YCONG[1:0]		VCONG[1:0]
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
00 :	Quasi-bidirectional(standard 8051 port outputs)							

01 :	Push-pull output
10 :	Input-only (High impedance)
11 :	Open drain output

PINCONG5			Address = FCH				Reset Value = 0xAAH	

Pin Configure Register 5

	OCPNCONG[1:0]		CH1NCONG[1:0]		CH0NCONG [1:0]		AOCPCONG [1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 :	Quasi-bidirectional(standard 8051 port outputs)
01 :	Push-pull output
10 :	Input-only (High impedance)
11 :	Open drain output

PINCONG6			Address = FDH				Reset Value = 0xA0H	

Pin Configure Register 6

	IIC_SCLCONG [1:0]		IIC_SDACONG [1:0]		RXCONG[1:0]		TXCONG[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 :	Quasi-bidirectional(standard 8051 port outputs)
01 :	Push-pull output
10 :	Input-only (High impedance)
11 :	Open drain output

PINCONG7			Address = C7H				Reset Value = 0x0AH	

Pin Configure Register 7

	-----		-----		FGCONG [1:0]		IPWMCONG [1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

00 :	Quasi-bidirectional(standard 8051 port outputs)
01 :	Push-pull output
10 :	Input-only (High impedance)
11 :	Open drain output

13.2.3 Pin I/O Setting Register (PINSET)

Table 25 13.2.3 Pin I/O Setting Register (PINSET)

PINSET1			Address = F1H				Reset Value = 0xAAH	

Pin I/O Setting Register 1

	CH4SET[1:0]		CH5SET[1:0]		CH6SET[1:0]		CH7SET[1:0]	
Bit	7	6	5	4	3	2	1	0

Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 :	No pull							
01 :	Pull down							
10 :	Pull up							
11 :	No pull							

PINSET2			Address = F2H				Reset Value = 0xAAH	
Pin I/O Setting Register 2								
	CH0SET[1:0]		CH1SET[1:0]		CH2SET[1:0]		CH3SET[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 :	No pull							
01 :	Pull down							
10 :	Pull up							
11 :	No pull							

PINSET3			Address = F3H				Reset Value = 0x0AH	
Pin I/O Setting Register 3								
	XSET[1:0]		USET[1:0]		XTAL**O**SET[1:0]		XTAL**I**SET[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 :	No pull							
01 :	Pull down							
10 :	Pull up							
11 :	No pull							

PINSET4			Address = F4H				Reset Value = 0x00H	
Pin I/O Setting Register 4								
	ZSET[1:0]		WSET[1:0]		YSET[1:0]		VSET[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 :	No pull							
01 :	Pull down							
10 :	Pull up							
11 :	No pull							

PINSET5			Address = F5H				Reset Value = 0x80H	
Pin I/O Setting Register 5								
	OCPNSET[1:0]		CH1NSET[1:0]		CH0NSET [1:0]		AOCPSET[1:0]	

	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
00 :	No pull							
01 :	Pull down							
10 :	Pull up							
11 :	No pull							

PINSET6			Address = F6H			Reset Value = 0x0AH		
Pin I/O Setting Register 6								
	IIC_SCLSET[1:0]		IIC_SDASET[1:0]		RXSET[1:0]		TXSET [1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
00 :	No pull							
01 :	Pull down							
10 :	Pull up							
11 :	No pull							

PINSET7			Address = F7H			Reset Value = 0xB0H		
Pin I/O Setting Register 7								
	MOCS	----	OCPNDBT[1:0]		FGSET[1:0]		IPWMSET[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MOCS								
0 : U、V、W、X、Y、Z is GPIO Mode.								
1: U、V、W、X、Y、Z is SVPWM Mode.(ADC CH0& CH1 Auto Converter)								
MOCS=1, Pin set must to Push-pull output mode. **(PINSET3 [7:4] and PINSET4 [7:0])**								
OCPNDBT (De-bounce time for digital OCPN)								
00 :	0nS							
01 :	250nS							
10 :	500nS							
11 :	1000nS							
FGSET[1:0], IPWMSET[1:0]								
00 :	No pull							
01 :	Pull down							
10 :	Pull up							
11 :	No pull							

13.3 Clock Structure

The clock source of the device may be either external, or internal. The external crystal (12MHz) is connect to pins **XTALI** and **XTALO** and the internal clock source (on-chip oscillator) is run at 2MHz. The choice of internal or external clock source is setting by **Writer** before program the code.

Figure 8 Clock architecture of MDSF40
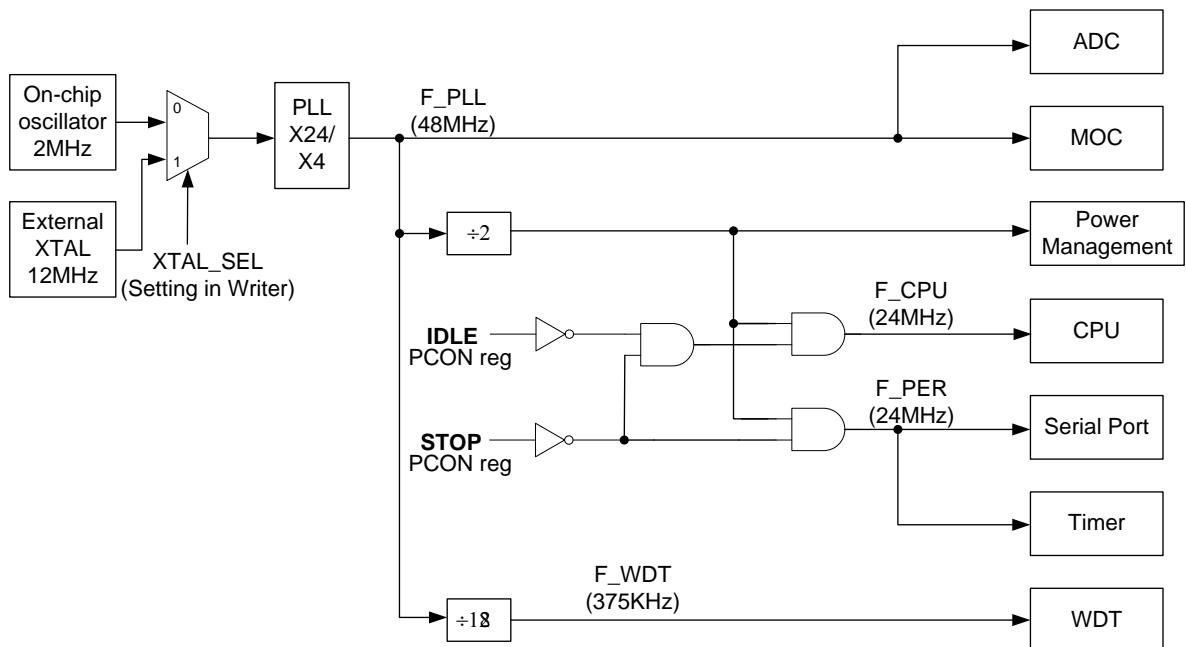
Clock architecture of MDSF40

13.4 Timer

The **MDSF40** have three 16-bit timer/counter registers: **Timer0**, **Timer1** and **Timer2**. All can be configured for counter or timer operations.

In addition to the "timer" or "counter" selection, **Timer0** and **Timer1** have four operating modes from which to select which are selected by bit-pairs (**M1**, **M0**) in **TMOD**. Modes 0, 1,and 2 are the same for both timer/counters. Mode 3 is different.

Table 26 Timer

	Timer0	**Timer1**	**Timer2**
Mode 0	13-bit timer/counter	13-bit timer/counter	13-bit timer/counter
Mode 1	16-bit timer/counter	16-bit timer/counter	16-bit timer/counter
Mode 2	8-bit auto-reload timer/counter	8-bit auto-reload timer/counter	8-bit auto-reload timer/counter
Mode 3	two independent 8-bit timers/counters	stop	8-bit timers/counters

Two Special Function registers (**TMOD** and **TCON**) are used to select the appropriate mode.

Table 27 Timer SFR

SFR	**Description**	**address**	**Reset value**
PFCON	Peripheral Frequency Control Register	D1H	00H
TMOD	Timer0/1 Mode Register	89H	00H
TCON	Timer0/1 Control Register	88H	00H
T2CON	Timer2 Control Register	C8H	00H
TH0	Timer0 High byte	8CH	00H
TL0	Timer0 Low byte	8AH	00H
TH1	Timer1 High byte	8DH	00H
TL1	Timer1 Low byte	8BH	00H
TH2	Timer2 High byte	B5H	00H
TL2	Timer2 Low byte	B4H	00H

13.4.1 Peripheral Frequency Control Register (PFCON)

Table 28 13.4.1 Peripheral Frequency Control Register (PFCON)

13.4.2 Timer 0/1 Mode Register (TMOD)

Table 29 **TMOD** register is used in configuration of MCU**Timer0** and **Timer1**.

TMOD				Address = 89H			Reset Value = 0x00H	
Timer 0/1 Mode Register								
	GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

GATE1	Timer1 gate control :		
[7]	If set, enables external gate control (pin **INT1N**) for Counter1. When **INT1N** is high, and TR1 bit is set, the Counter1 is incremented every falling edge on **INT1N** input pin		
C/T1	Timer1 counter/timer select :		
[6]	0 : Timer		
	1 : Counter		
GATE0	Timer 0 gate control :		
[5]	If set, enables external gate control (pin **INT0N**) for Counter0. When **INT0N** is high, and TR0 bit is set, the Counter0 is incremented every falling edge on**INT0N** input pin		
C/T0	Timer0 counter/timer select :		
[4]	0 : Timer		
	1 : Counter		
T1M1 /T0M1	T1M0 /T0M0	Mode	Function
0	0	Mode0	13-bit Counter/Timer, with 5 lower bits in TL0 (TL1) register and 8 bits in TH0 (TH1) register (for Timer0 or Timer1, respectively). The 3 high-order bits of TL0 (TL1) are zeroed whenever Mode 0 is enabled. (Not auto-reload)
0	1	Mode1	16-bit Counter/Timer. (Not auto-reload)
1	0	Mode2	8 -bit auto-reload Counter/Timer. The reload value is kept in TH0 (TH1), while TL0 (TL1) is incremented every clock cycle. Reloaded from TH0 (TH1) at overflow.
1	1	Mode3	For Timer1: Timer1 is stopped. For Timer0: Timer0 acts as two independent 8 bit Timers / Counters – TL0, TH0. (Not auto-reload)

13.4.3 Timer 0/1Control Register (TCON)

TCON register is used to control operation of these modules.**MDSF40** includes two external digital interrupt sources **INT0N** and **INT1N**), with dedicated interrupt sources. **INT0N** and **INT1N** are configurable as falling edge or low level. The **IT0** and **IT1** bits in **TCON** select level- or edge-sensitive.**IE0** and **IE1** in the **TCON** register serve as the interrupt-pending flags for the **INT0N** and **INT1N** external interrupts, respectively.

Table 30 Timer 0/1Control Register (TCON)

TCON			Address = 88H			Reset Value = 0x00H		
Timer 0/1 Control Register								
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TF1	Timer1 overflow flag :
	Bit set by hardware when Timer1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR1	Timer1 run control :
	0 : Stop
	1 : Run
TF0	Timer0 overflow flag :
	Bit set by hardware when Timer1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR0	Timer0run control :
	0 : Stop
	1 : Run
IE1	External interrupt 1 flag :
	Set by hardware, when External interrupt (**INT1N**) is observed. Cleared by hardware when interrupt is processed.
IT1	External interrupt 1 type control :
	0 : External interrupt 1 is activated at low level on input pin
	1 : External interrupt 1 is activated at falling edge on input pin
IE0	External interrupt 0 flag :
	Set by hardware, when External interrupt (**INT0N**) is observed. Cleared by hardware when interrupt is processed.
IT0	External interrupt 0 type control :
	0 : External interrupt 0 is activated at low level on input pin
	1 : External interrupt 0 is activated at falling edge on input pin

The **TF0**, **TF1** (**Timer0** and **Timer1** overflow flags), **IE0** and **IE1** (External interrupt 0 and 1 flags) will be automatically cleared by hardware when the corresponding service routine is called.

13.4.4 Timer2 Control Register (T2CON)

T2CON is used to control **Timer2**run/stop, mode, prescaler.

Table 31 Timer2 Control Register (T2CON)

T2CON			Address = C8H				Reset Value = 0x00H	
Timer2 Control Register								
	-----	-----	TF2	TR2	T2M1	T2M0	T2PS1	T2PS0
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W
TF2	Timer2 overflow flag :							
	Bit set by hardware when Timer2 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.							
TR2	Timer2run control :							
	0 : Stop							
	1 : Run							
T2PS[1:0]	Timer2(T2) Prescaler select :							
	00 :F_PER/12							
	01 : F_PER							
	10 : F_PER/96							
	11 :-----							
T2M1	T2M0	Mode	Function					
0	0	Mode0	13-bit Timer, with 5 lower bits in TL2 register and 8 bits in TH2 register.(Not auto-reload)					
0	1	Mode1	16-bit Timer. (Not auto-reload)					
1	0	Mode2	8 -bit auto-reload Timer. The reload value is kept in TH2, while TL2 is incremented every clock cycle. Reloaded from TH2 at overflow.					
1	1	Mode3	8 bit Timers. (Not auto-reload)					

13.4.5 Timer0 Mode 0

Figure 9 Timer0 Mode 0
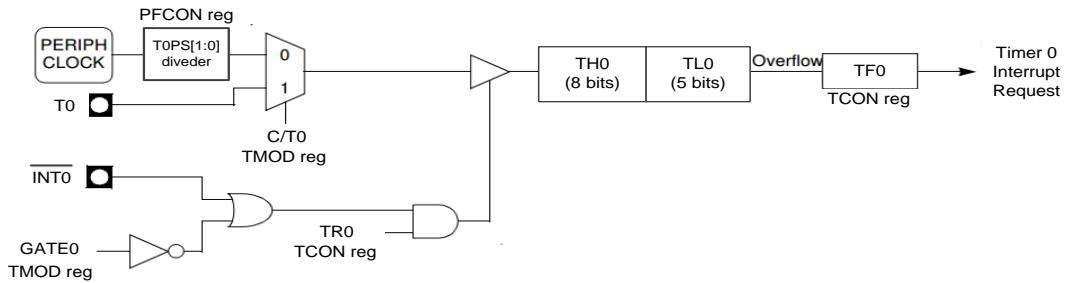
13.4.6 Timer0 Mode 1

Figure 10 Timer0 Mode 1
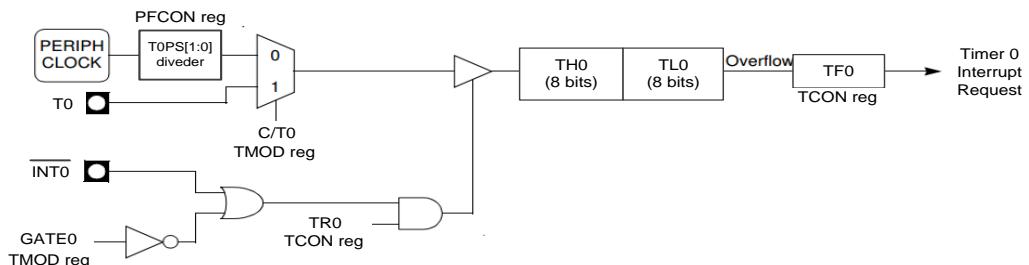
13.4.7 Timer0 Mode 2

Figure 11 Timer0 Mode 2
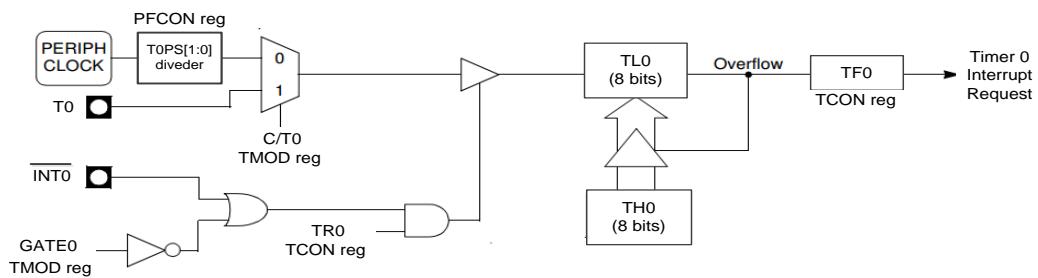
13.4.8 Timer0 Mode 3

Figure 12 Timer0 Mode 3
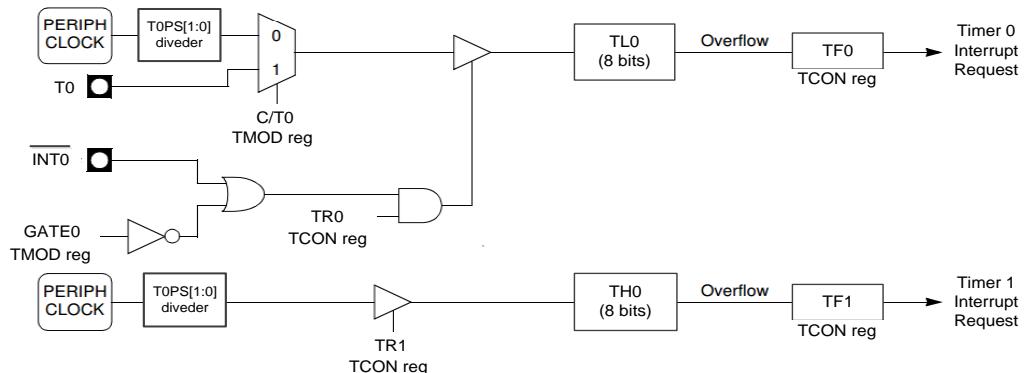
13.4.9 Timer1 Mode 0

Figure 13 Timer1 Mode 0
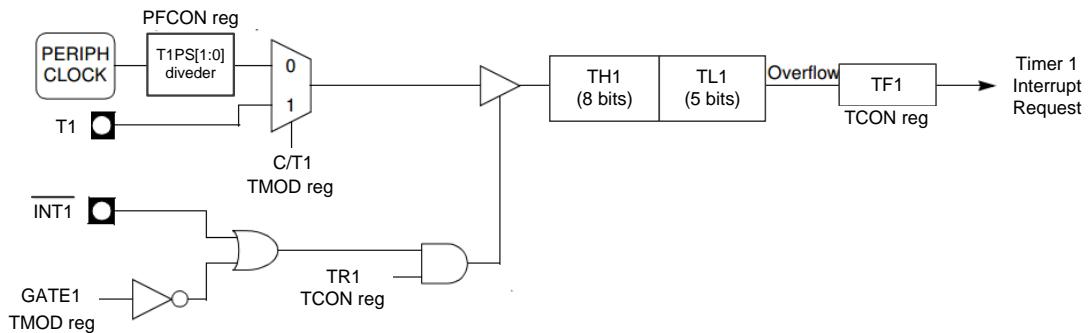
13.4.10 Timer1 Mode 1

Figure 14 Timer1 Mode 1
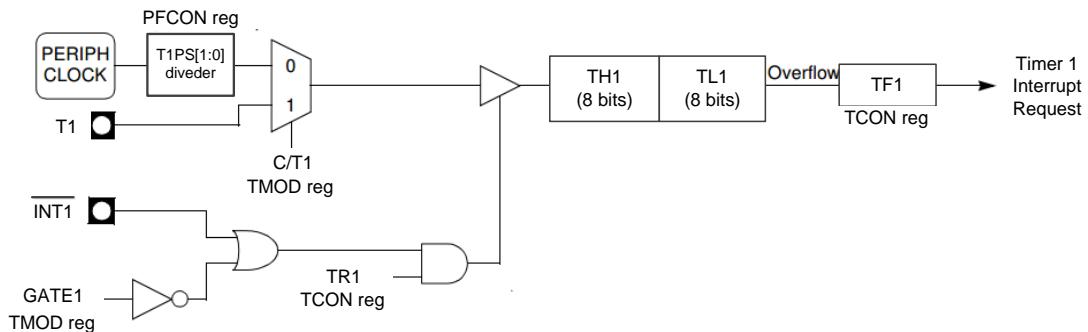
13.4.11 Timer1 Mode 2

Figure 15 Timer1 Mode 2
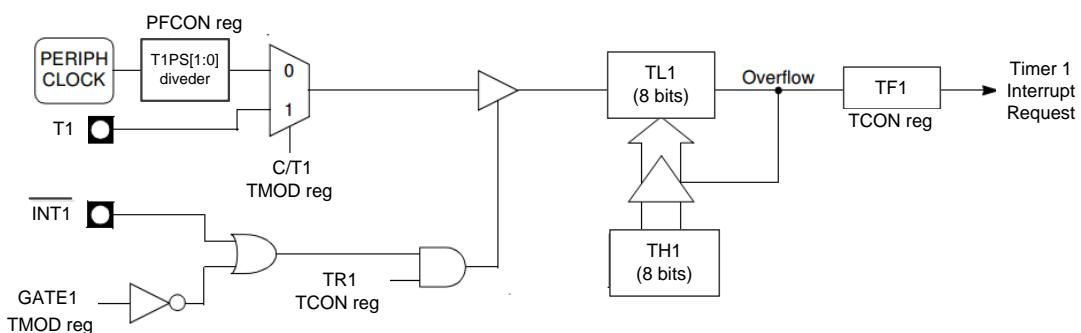
13.4.12 Timer2 Mode 0

Figure 16 Timer2 Mode 0
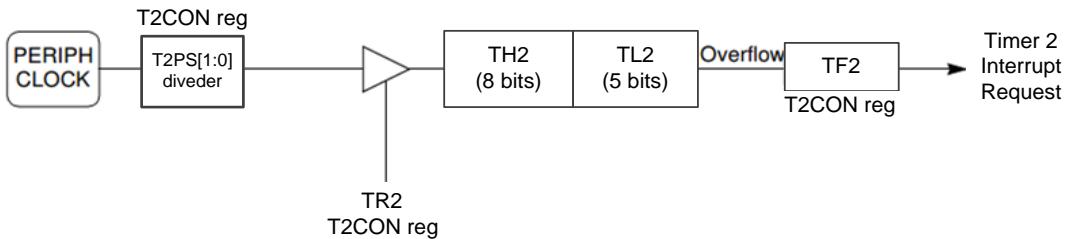
13.4.13 Timer2 Mode 1

Figure 17 Timer2 Mode 1
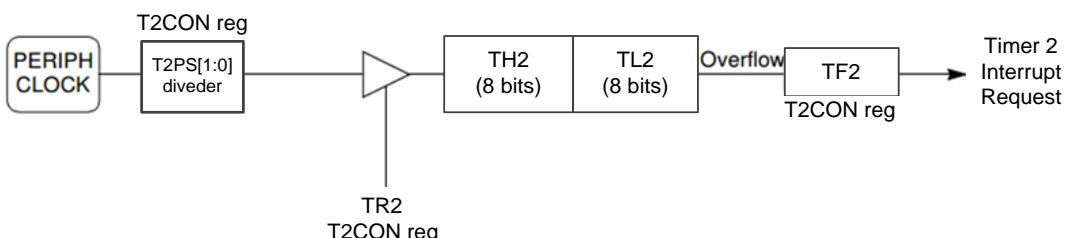
13.4.14 Timer2 Mode 2

Figure 18 Timer2 Mode 2
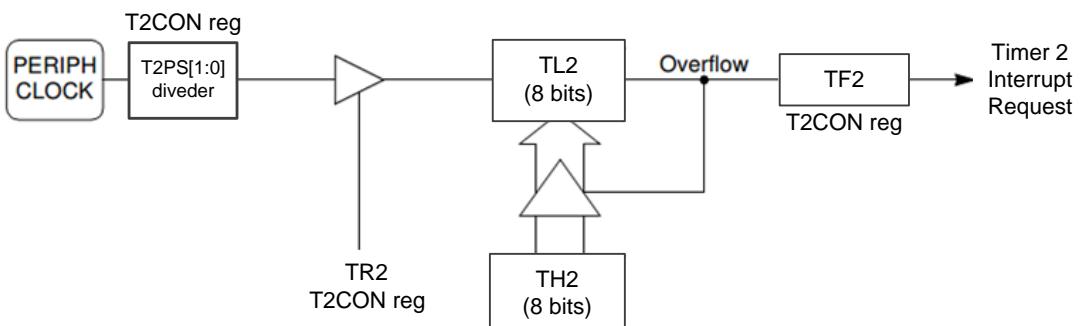
13.4.15 Timer2 Mode 3

Figure 19 Timer2 Mode 3
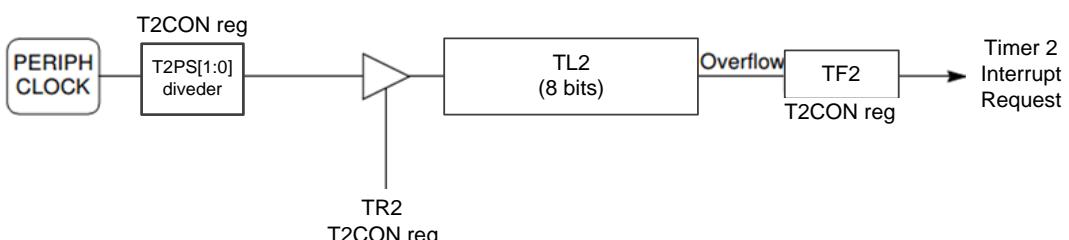
13.5 Watchdog Timer

The Watchdog Timer (**WDT**) is a8-bit free-running counter that generates a reset signal or interrupt (**WDTC**.6) if it overflows. It can help the application software to recover from an abnormal condition. The **WDT** is independent from **Timer0**, **Timer1**, or **Timer2**. The **F_WDT** is 375KHz, it is from on-chip RC oscillator.

$$WDTCLK = F\_WDT \times \frac{1}{2^{WDTM}}$$

WDT (8-bit counter) overflow time $= \frac{256}{WDTCLK}$

Figure 20 13.5 SDT Block
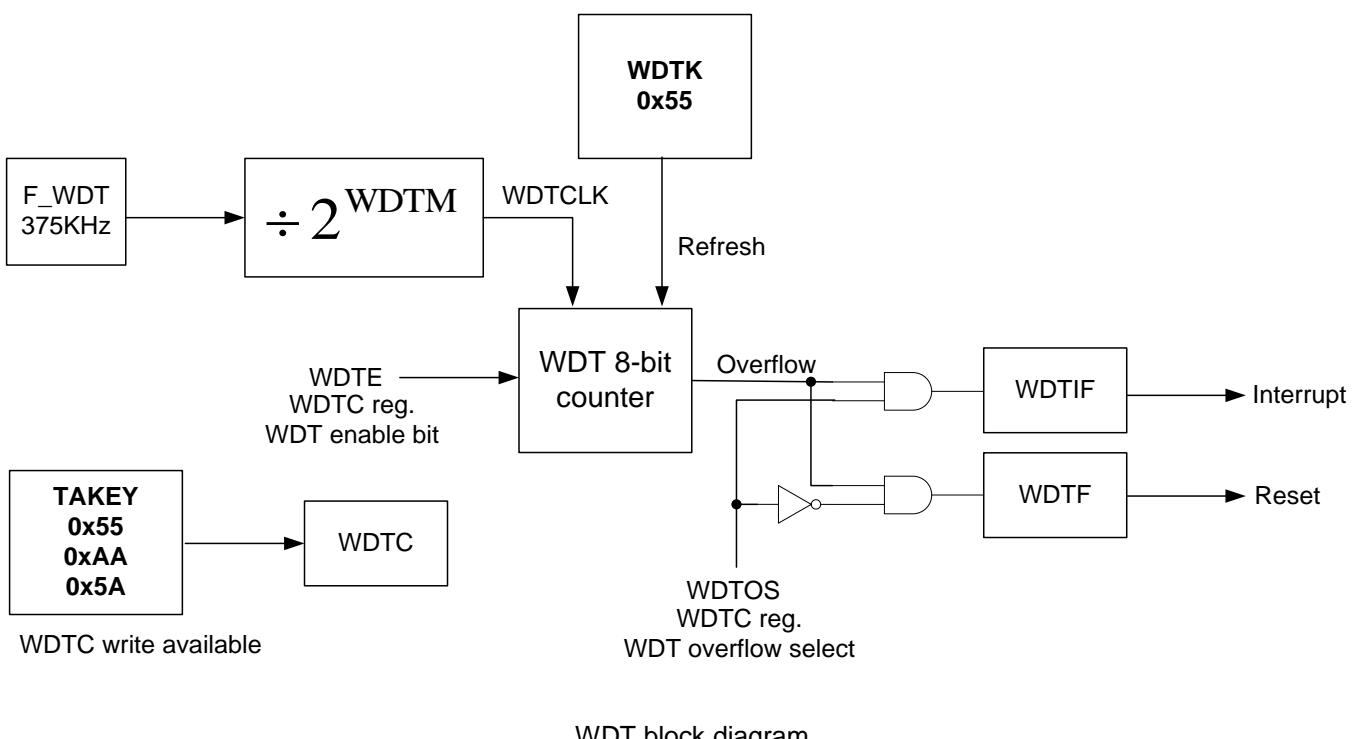
WDT block diagram

Table 32 WDT SFR

SFR	Description	address	Reset value
RSTS	Reset Source Register	FEH	0AH
TAKEY	Time Access Key Register	FFH	00H
WDTC	Watchdog Timer Control Register	B6H	04H
WDTK	Watchdog Timer Refresh Key	B7H	00H

RSTS				Address = FEH			Reset Value = 0x0AH	
Reset Source Register								
	-----	-----	-----	WDTRF	PINRF[1:0]		PORF[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R/W	R/W	R/W	R/W	R/W
WDTRF	Watchdog timer reset flag.							
	This flag is set to 1 if the Watchdog Timer Reset caused the reset.							
PINRF[1:0]	$\overline{RST}$ pin reset flag.							
	This flag is set to 10b if the $\overline{RST}$ pin caused the reset.							
	Clear by firmware.							
PORF[1:0]	POR reset flag.							
	This flag is set to 10b if the POR caused the reset.							
	Clear by firmware.							

13.5.1 Watchdog Timer Control Register (WDTC)

Table 33 13.5.1 Watchdog Timer Control Register (WDTC)

WDTC			Address = B6H			Reset Value = 0x04H		
Watchdog Timer Control Register								
	-----	WDTOS	WDTE	-----	WDTM[3:0]			
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	X	R/W	R/W	R/W	R/W
WDTOS	Watchdog timer overflow select :							
	0 : When WDT overflow, enable WDT reset.							
	1 : When WDT overflow, enable WDT interrupt.							
WDTE	Watchdog timer enable :							
	0 : Disable WDT.							
	1 : Enable WDT.							
WDTM[3:0]	WDT clock divider :							
	$WDTCLK = 375KHz \times \frac{1}{2^{WDTM}}$ (default is 375K / 16)							

13.5.2 Time Access Key Register (TAKEY)

Table 34 13.5.2 Time Access Key Register (TAKEY)

TAKEY			Address = FFH			Reset Value = 0x00H		
Time Access Key Register								
	TAKEY[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
WDTC default is read only, must write three specific values 55H, AAH and 5AH to the TAKEY enable the WDTC write available.								
The sequence is:								
MOV TAKEY, #55h								
MOV TAKEY, #AAh								
MOV TAKEY, #5Ah								

13.5.3 Watchdog Timer Refresh Key (WDTK)

Table 35 13.5.3 Watchdog Timer Refresh Key (WDTK)

WDTK				Address = B7H			Reset Value = 0x00H	
Watchdog Timer Refresh Key								
	WDTK[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
The application must write 0x55 into the WDTK register, for the Watchdog timer to be cleared.								

13.6 Serial Port (UART)

The Serial Port provides a flexible full-duplex synchronous/asynchronous receiver/transmitter, called **UART**. The communication rate can be set by configuring the baud rate in **SFRs**. The two serial buffers consist of two separate registers, a transmit buffer and a receive buffer. Writing data to the SFR **SBUF**, transfers the data to the serial output buffer and starts the transmission. Reading from the **SBUF**, reads data from the serial receive buffer. The serial port can simultaneously transmit and receive data. It can also buffer 1 byte at receive, which prevents the receive data from being lost if the CPU reads the second byte before the transmission of the first byte is completed.

Table 36 Serial Port (UART)

SFR	Description	address	Reset value
AUX	Auxiliary	8EH	11H
PFCON	Peripheral Frequency Control Register	D1H	00H
SCON	Serial Port Control Register	98H	00H
SBUF	Serial Port Data Buffer	99H	00H
SRELH	Serial Port Reload Register High	9BH	00H
SRELL	Serial Port Reload Register Low	9AH	00H

Table 37 Serial Port (UART) SFR

AUX				Address = 8EH			Reset Value = 0x11H	
Auxiliary Register								
	LVD_EN	LVD	-----	ITS	SMOD	BRS	DPS	CP
Bit	7	6	5	4	3	2	1	0
Type	R/W	R	X	R/W	R/W	R/W	R/W	R
LVD_EN	Low voltage detect enable :							
	1: Enable							
LVD	Low voltage detect status. :							
	1: Low voltage occur							
ITS	MCU instruction timing select. :							
	0:1T							
	1:2T							
SMOD	Serial Port (UART) baud rate select.							
BRS	Serial Port (UART) baud rate generator select.							
DPS	Data pointer register select :							
	0 : Select DPTR Register DP0H, DP0L							
	1 : Select DPTR Register DP1H, DP1L							
CP	Code protect :							
	0 : Non-protect							
	1: Protect							

Table 38 Serial Port (UART) SFR

PFCON				Address = D1H			Reset Value = 0x00H	
Peripheral Frequency Control Register								
	-----	-----	SRELPS[1:0]		T1PS[1:0]		T0PS[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W
SRELPS[1:0]	Serial port (UART) Prescaler select :							
	00 :F_PER/64							
	01 :F_PER/32							
	10 :F_PER/16							
	11 :F_PER/8							
T1PS[1:0]	Timer1 (T1) Prescaler select :							
	00 :F_PER/12							
	01 :F_PER							
	10 :F_PER/96							
	11 :-----							
T0PS[1:0]	Timer0(T0) Prescaler select :							
	00 : F_PER/12							
	01 : F_PER							
	10 : F_PER/96							
	11 :-----							

13.6.1 Serial Port Control Register (SCON)

Table 39 13.6.1 The **SCON** register controls the function of Serial Port (**UART**).

SCON				Address = 98H			Reset Value = 0x00H	
Serial Port Control Register								
	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SM0	SM1	Mode	Description	Baud Rate	
0	0	Mode 0	Shift register	F_PER/12	
0	1	Mode 1	8bit UART	Variable	
1	0	Mode 2	9bit UART	Depends on SMOD (AUX.3)	
				SMOD	Baud Rate
				0	F_PER/64
				1	F_PER/32
1	1	Mode 3	9bit UART	Variable	

SM2	Multiprocessor communication enable
REN	Serial reception enable :
	0 : Serial reception at Serial Port is disabled.
	1 :Serial reception at Serial Port is enabled.
TB8	Transmitter bit 8 :
	This bit is used while transmitting data through Serial Port in Modes 2 and 3. The state of this bit corresponds with the state of the 9th transmitted bit (e.g. parity check or multiprocessor communication). It is controlled by software.
RB8	Received bit 8 :
	This bit is used while receiving data through Serial Port 0 in Modes 2 and 3. It reflects the state of the 9th received bit.
	In Mode 1, if multiprocessor communication is enabled (sm2 = 0), this bit is the stop bit that was received.
	In Mode 0 this bit is not used.
TI	Transmit interrupt flag : (completion of a serial transmission)
	It is set by hardware at the end of bit 8 in mode 0 or at the beginning of a stop bit in other modes. It must be cleared by software.
RI	Receive interrupt flag : (It must be cleared by software.)
	It is set by hardware after completion of a serial reception at Serial Port 0.
	It is set by hardware at the end of bit 8 in mode 0 or in the middle of a stop bit in other modes.

Serial Port working in modes 1 or mode 3:

When BRS = 0 (AUX.2)

TIPS[1:0] = 00b

$$\text{Baud rate} = \frac{2^{\text{SMOD}}}{32\times(256\text{-TH1})} \times \frac{\text{F\_PER}}{12}$$

TIPS[1:0] = 01b

$$\text{baud rate} = \frac{2^{\text{SMOD}}}{32\times(256\text{-TH1})} \times \text{F\_PER}$$

TIPS[1:0] = 10b

$$\text{baud rate} = \frac{2^{\text{SMOD}}}{32\times(256\text{-TH1})} \times \frac{\text{F\_PER}}{96}$$

When BRS = 1 (AUX.2)

SRELPS[1:0] = 00b

$$\text{baud rate} = \frac{2^{\text{SMOD}}}{2^{10}-\text{SREL[H,L]}} \times \frac{\text{F\_PER}}{64}$$

SRELPS [1:0] = 01b

$$\text{baud rate} = \frac{2^{\text{SMOD}}}{2^{10}-\text{SREL[H,L]}} \times \frac{\text{F\_PER}}{32}$$

SRELPS [1:0] = 10b

$$\text{baud rate} = \frac{2^{\text{SMOD}}}{2^{10}-\text{SREL[H,L]}} \times \frac{\text{F\_PER}}{16}$$

SRELPS [1:0] = 11b

$$\text{baud rate} = \frac{2^{\text{SMOD}}}{2^{10}-\text{SREL[H,L]}} \times \frac{\text{F\_PER}}{8}$$

13.6.2 Serial Port Data Buffer (SBUF)

Writing data to this register sets data in serial output buffer and starts the transmission through Serial Port. Reading from the **SBUF**, reads data from the serial receive buffer.

Table 40 13.6.2 Serial Port Data Buffer (SBUF)

SBUF			Address = 99H			Reset Value = 0x00H	
Serial Port Data Buffer							
	SBUF[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.6.3 Serial Port Reload Register (SREL)

Serial Port Reload Register is used for Serial Port baud rate generation. Only 10 bits are used, where 8 bits from the **SRELL** as lower bits and 2 bits from the **SRELH** (SRELH.1, SRELH.0) as higher bits.

Table 41 13.6.3 Serial Port Reload Register (SREL)

SRELL			Address = 9AH			Reset Value = 0x00H	
Serial Port Reload Register Low							
	SREL[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SRELH			Address = 9BH			Reset Value = 0x00H	
Serial Port Reload Register High							
	-----	-----	-----	-----	-----	-----	SREL.9	SREL.8
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	X	R/W	R/W

13.7 Power Management

The Power Control Register (**PCON**) is used to control the **MDSF40 STOP** and **IDLE** power management modes.

Table 42 13.7 Power Management

PCON				Address = 87H			Reset Value = 0x00H	
Power Control Register								
	-----	-----	-----	-----	-----	-----	STOP	IDLE
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	X	R/W	R/W
STOP	Stop mode bit.							
[1]	Setting this bit activates STOP operation. (read as 0)							
IDLE	Idle mode bit.							
[0]	Setting this bit activates IDLE mode operation. (read as 0)							

13.7.1 STOP MODE

Setting the **STOP** Mode Select bit (**PCON**.1) causes the controller core to enter **STOP** mode as soon as the instruction that sets the bit completes execution. **In STOP mode the CPU, GPIO, UART, Timers, and MOC are stopped, but the WDT is still work.**

STOP mode can terminate by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

The assertion of an enabled interrupt will cause the **STOP** Mode Selection bit (**PCON**.1) to be cleared and the CPU to resume operation.

13.7.2 IDLE MODE

Setting the **IDLE** Mode Select bit (**PCON**.0) causes the hardware to halt the CPU and enter **IDLE** mode as soon as the instruction that sets the bit completes execution.

In IDLE mode only the CPU and MOC is stop. All internal registers and memory maintain their original data.

IDLE mode can terminate by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

The assertion of an enabled interrupt will cause the **IDLE** Mode Selection bit (**PCON**.0) to be cleared and the CPU to resume operation.

13.8 Reset

The reset logic is used to place the device into a known state.

MDSF40 provides Power-on Reset flag, External Reset **RSTN** flag and Watchdog timer Reset flag to monitor reset status. The source of the reset can be monitor.

13.8.1 Reset Source Register (RSTS)

Table 43 13.8.1 Reset Source Register (RSTS)

13.9 Interrupt Controller

The **ISR** - Interrupt Service Routine unit, is a subcomponent responsible for interrupt handling. It receives up to **14** interrupt requests. Each interrupt source has its own request flag that is located in devices which is a source of interrupt. No interrupt request flags are located directly in **ISR**. All interrupts are requested by high level on correspondent inputs to **ISR**. Each of the interrupt sources can be individually enabled or disabled by corresponding enable flag in **IEN0**, **IEN1** SFR registers..Additionally all interrupts can be globally enabled or disabled by the —**EA** flag in the **IEN0** SFR. All interrupt sources are divided into 6 interrupts groups. Each of the interrupt groups can have one of four interrupt priority levels assigned. The interrupt priority level is defined by flags located in the **IP0** and **IP1** SFR registers.

Table 44 13.9 Interrupt Controller

Interrupt vectors

Interrupt Number (use Keil C Tool)	Interrupt Vector Address	Interrupt Request Flags
0	0003H	IE0 – External interrupt 0
1	000BH	TF0 – Timer0 interrupt
2	0013H	IE1 – External interrupt 1
3	001BH	TF1 – Timer1 interrupt
4	0023H	SPIF(TI, RI)– Serial port interrupt
5	002BH	TF2 – Timer2 interrupt
6	0033H	-----
7	003BH	-----
8	0043H	OCPSIF – OCP Short interrupt
9	004BH	ADCIF –ADC interrupt
10	0053H	MPWMMINIF–MPWM MIN interrupt
11	005BH	MPWMMAXIF–MPWM MAX interrupt
12	0063H	IICIF – IIC interrupt
13	006BH	LVDIF – Low voltage detect interrupt
14	0073H	WDTIF – Watchdog timer interrupt
15	007BH	CAPTUREIF –CAPTURE interrupt

Table 45 Interrupt Priority Groups

Interrupt Priority Groups

Group priority	Interrupt Group	Highest priority in group		Lowest priority in group
Highest	Group0	LVDIF	IE0	-----
	Group1	WDTIF	TF0	-----
	Group2	OCPSIF	ADCIF	IE1
	Group3	MPWMMINIF	MPWMMAXIF	TF1
	Group4	IICIF	SPIF(TI, RI)	-----
Lowest	Group5	CAPIF	TF2	-----

SFR	Description	address	Reset value
IEN0	Interrupt Enable Register 0	A8H	00H
IEN1	Interrupt Enable Register 1	B8H	00H
IRCON1	Interrupt Request Register 1	C0H	00H
IP0	Interrupt Priority Register 0	A9H	00H
IP1	Interrupt Priority Register 1	B9H	00H

MDSF40

13.9.1 Interrupt Enable Register 0 (IEN0)

Table 46 13.9.1 Interrupt Enable Register 0 (IEN0)

IEN0			Address = A8H			Reset Value = 0x00H		
Interrupt Enable Register 0								
	EA	-----	ET2	ESP	ET1	EX1	ET0	EX0
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	R/W	R/W	R/W	R/W	R/W	R/W

EA	Interrupts enable :
[7]	0 : Disable All interrupts.
	1 : Enable interrupt.
ET2	Timer2 interrupt enable:
[5]	0 : Disable Timer2 overflow interrupt.
	1 : When EA = 1, enable Timer2 overflow interrupt.
ESP	Serial port interrupt enable:
[4]	0 : Disable Serial port interrupt.
	1 : When EA = 1, enable Serial port interrupt.
ET1	Timer1 interrupt enable:
[3]	0 : Disable Timer1 overflow interrupt.
	1 : When EA = 1, enable Timer1 overflow interrupt.
EX1	External interrupt 1 enable:
[2]	0 : Disable External interrupt 1.
	1 : When EA = 1, enable External interrupt 1.
ET0	Timer0 interrupt enable:
[1]	0 : Disable Timer0 overflow interrupt.
	1 : When EA = 1, enable Timer0 overflow interrupt.
EX0	External interrupt 0 enable:
[0]	0 : Disable External interrupt 0.
	1 : When EA = 1, enable External interrupt 0.

13.9.2 Interrupt Enable Register 1 (IEN1)

Table 47 13.9.2 Interrupt Enable Register 1 (IEN1)

IEN1				Address = B8H			Reset Value = 0x00H	
Interrupt Enable Register 1								
	CAPIE	WDTIE	LVDIE	IICIE	MPWMM	MPWMM	ADCIE	OCPSIE
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CAPIE	Capture interrupt enable:
[7]	0 : Disable CAPTURE interrupt.
	1 : When EA = 1, enable CAPTURE interrupt.
WDTIE	Watchdog timer interrupts enable :
[6]	0 : Disable WDT interrupt.
	1 : When EA = 1 and WDTOS = 1, enable WDT overflow interrupt.
LVDIE	LVD (Low voltage detect) interrupt enable:
[5]	0 : Disable LVD interrupt.
	1 : When EA = 1, enable LVD interrupt.
IICIE	IIC interrupt enable:
[4]	0 : Disable IIC interrupt.
	1 : When EA = 1, enable IIC interrupt.
MPWMMAXIE	MPWM maximum interrupt enable:
[3]	0 : Disable MPWM maximum interrupt.
	1 : When EA = 1, enable MPWM maximum interrupt.
MPWMMINIE	MPWM minimum interrupt enable:
[2]	0 : Disable MPWM minimum interrupt .
	1 : When EA = 1, enable MPWM minimum interrupt.
ADCIE	ADC interrupt enable:
[1]	0 : Disable ADC interrupt.
	1 : When EA = 1, enable ADC interrupt.
OCPSIE	OCP (Over current protect) Short interrupt enable:
[0]	0 : Disable OCP Short interrupt .
	1 : When EA = 1, enable OCP Short interrupt.

13.9.3 Interrupt Request Register 1 (IRCON1)

Table 48 13.9.3 Interrupt Request Register 1 (IRCON1)

IRCON1		Address = C0H				Reset Value = 0x00H		
Interrupt Request Register 1								
Bit	CAPTUREIF	WDTIF	LVDIF	IICIF	MPWMMAXIF	MPWMMINIF	ADCIF	OCPSIF
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CAPTIF[7]	Capture interrupt flag.
WDTIF[6]	Watchdog timer interrupts flag.
LVDIF[5]	LVD (Low voltage detect) interrupt flag.
IICIF[4]	IIC interrupt flag
MPWMMAXIF[3]	MPWM maximum interrupt flag.
MPWMMINIF[2]	MPWM minimum interrupt flag.
ADCIF[1]	ADC interrupt flag.
OCPSIF[0]	OCP Short interrupt flag.

13.9.4 Interrupt Priority Register (IP0, IP1)

The 14 interrupt sources are grouped into 6 priority groups. For each of the groups, one of four priority levels can be selected. It is achieved by setting appropriate values in **IP0** and **IP1** registers. The contents of the Interrupt Priority Registers define the priority levels for each interrupt source according to the tables below.

Table 49 13.9.4 Interrupt Priority Register (IP0, IP1)

IP0		Address = A9H				Reset Value = 0x10H		
Interrupt Priority Register 0								
	-----	-----	G5IP0	G4IP0	G3IP0	G2IP0	G1IP0	G0IP0
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

G5IP0[5]	Group5 interrupt priority bit 0
G4IP0[4]	Group4 interrupt priority bit 0
G3IP0[3]	Group3 interrupt priority bit 0
G2IP0[2]	Group2 interrupt priority bit 0
G1IP0[1]	Group1 interrupt priority bit 0
G0IP0[0]	Group0 interrupt priority bit 0

IP1				Address = B9H			Reset Value = 0x00H	
Interrupt Priority Register 1								
	-----	-----	G5IP1	G4IP1	G3IP1	G2IP1	G1IP1	G0IP1
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W
G5IP1[5]	Group5 interrupt priority bit 1							
G4IP1[4]	Group4 interrupt priority bit 1							
G3IP1[3]	Group3 interrupt priority bit 1							
G2IP1[2]	Group2 interrupt priority bit 1							
G1IP1[1]	Group1 interrupt priority bit 1							
G0IP1[0]	Group0 interrupt priority bit 1							

		Group x	
Level	**Priority**	IP1[GxIP1]	IP0 [GxIP0]
Level 0	Lowest	0	0
Level 1		0	1
Level 2		1	0
Level 3	Highest	1	1
x : 0~5			

14. 10-bit Analog-to-Digital Converter (ADC)

The **MDSF40** provides eight channels 10-bit ADC. The result of the conversion is provided at **ADCD** [9:0].\

Table 50 14. 10-bit Analog-to-Digital Converter (ADC)

SFR	Description	address	Reset value
ADCSTR	ADC Start Convert and Setting Register	C1H	00H
ADCCONT	ADC Control Register	C2H	83H
ADCD1	ADC Data Register 1	C3H	00H
ADCD2	ADC Data Register 2	C4H	00H
ADCDLY	ADC Sample Delay (For CH0&CH1)	C5H	33H
ADCOFST_L	ADC Offset Value Register Low Byte	C9H	00H
ADCOFST_H	ADC Offset Value Register High Byte	CAH	02H
ADCAUTO_L	ADC Auto Sample Data Register Low Byte	CBH	00H
ADCAUTO_H	ADC Auto Sample Data Register High Byte	CCH	00H

Figure 21 ADC conversion timing

ADC conversion timing
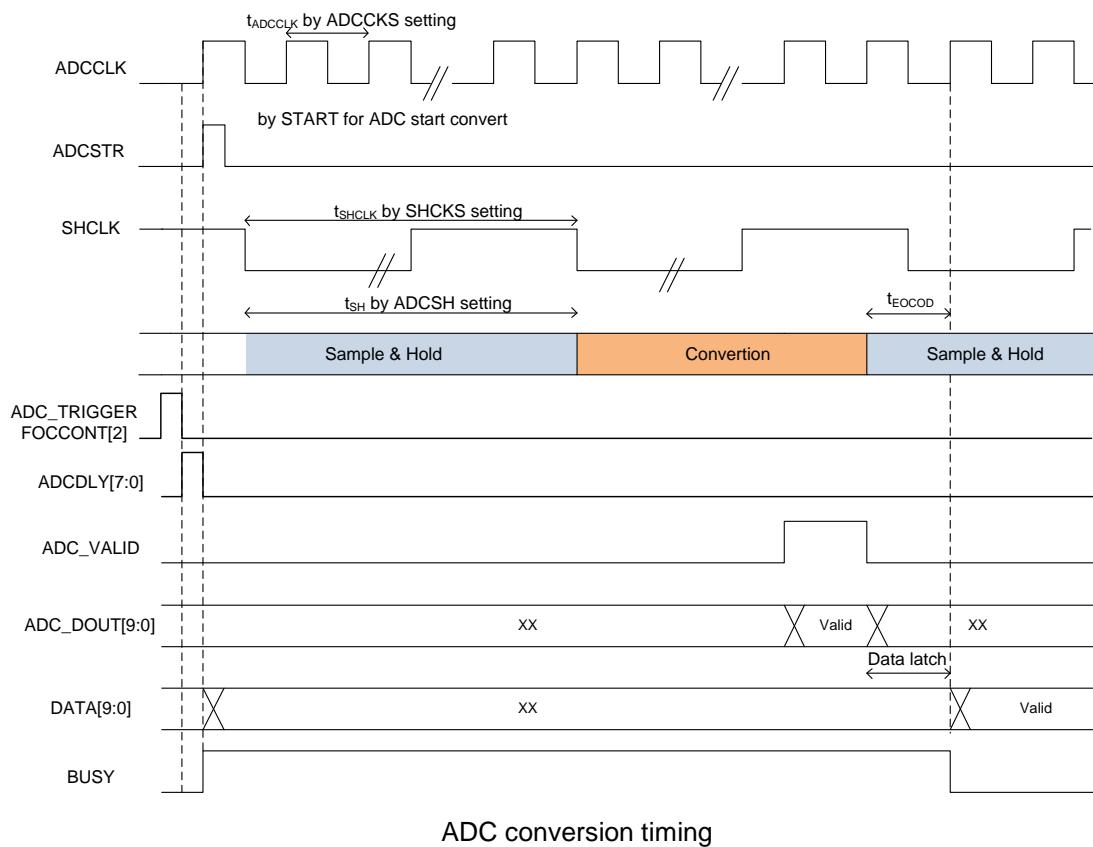
Figure 22 ADC CH0 and CH1 conversion

ADC CH0 and CH1 conversion
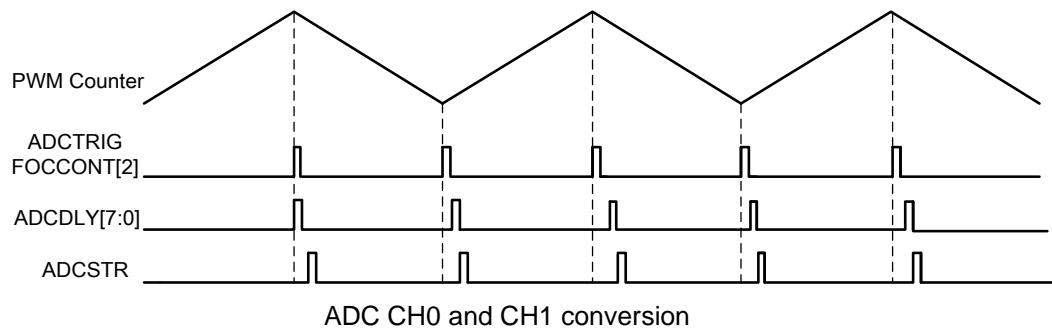
14.1 ADC Control Register (ADCCONT)

Table 51 14.1 ADC Control Register (ADCCONT)

ADCCONT			Address = C2H		Reset Value = 0x83H		
ADC Control Register							
	ADCPD	ADCSH[1:0]		ADCDS	ADCCKS	ADDCH[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADCPD	ADC power down control register :							
[7]	0 : Normal							
	1 : Power down							
ADCSH	ADC sample and hold time : (base on SHCLK)							
[5:6]	00 : 1 clock							
	01 : 2 clock							
	10 : 3 clock							
	11 : 4 clock							
ADCDS	ADC data select :							
[4]		MSB		10 bit result			LSB	
	0 :		ADCD2[7:0]			ADCD1.1		ADCD1.0
	1 :	ADCD1.1		ADCD1.0		ADCD2[7:0]		
ADCCKS	ADC conversion clock select : (ADCCLK)							
[3]	0 : 24MHz							
	1 : 12MHz							
ADCCH	ADC conversion channel select :							
[2:0]	000 :CH0				100 :CH4			
	001 :CH1				101 :CH5			
	010 :CH2				110 :CH6			
	011 : CH3				111 : CH7			

14.2 ADC Start Convert and Setting Register (ADCSTR)

Table 52   14.2 ADC Start Convert and Setting Register (ADCSTR)

ADCSTR			Address = C1H			Reset Value = 0x00H	
ADC Start Convert and Setting Register							
	SHCKS[1:0]		ADCGAIN		BUSY	ADC_SH_MD		START
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	X	R	X	X	X	W

SHCKS	ADC sample and hold clock select : (SHCLK)	
[7:6]	00 : 1MHz	10 : 400KHz
	01 : 500KHz	11 : 333KHz
OPAGAIN	OPA Gain	
[5:4]	00 : 1	10 : 5
	01 : 2.5	11 : 10
BUSY	ADC conversion busy flag :	
[3]	0 : ADC conversion finish	
	1 : ADC conversion busy	
ADC_SH_MD	ADC sample and hold mode	
[2:1]	00 : CPU self to decide	10 : 2 channel input
	01 : CPU self to decide	11 : only 1 channel input
START	ADC start conversion register : (write 1 only)	
[0]	1 : ADC start conversion	

14.3 ADC Sample Delay Register (ADCDLY)

Table 53 14.3 ADC Sample Delay Register (ADCDLY)

ADCDLY			Address = C5H			Reset Value = 0x33H	
ADC Sample Delay Register							
	ADCDLY [1:0]						
Bit	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

14.4 ADC Data Register (ADCD1, ADCD2)

Table 54 14.4 ADC Data Register (ADCD1, ADCD2)

ADCD1			Address = C3H			Reset Value = 0x00H	
ADC Data Register1							
	ADCD1 [1:0]						
Bit	---	---	---	---	---	---	1	0
Type	R	R	R	R	R	R	R	R

14.5 ADC Offset Value Register (ADCOS)

Table 55 14.5 ADC Offset Value Register (ADCOS)

SFR	Description						
ADCOS_L	ADC Offset Value Register Low Byte						
ADCOS_H	ADC Offset Value Register High Byte						
	Parameters		**Description**			**Reset Value**	
SFR_PAGE = 0	ADCOS1		ADC1 Offset Value			0x0200H	
SFR_PAGE = 1	ADCOS2		ADC2 Offset Value			0x0200H	
ADCOS_L	Address = C9H		Reset Value = 0x00H				
ADC Offset Value Low Byte							
	ADCOS_L [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADCOS_H	Address =CAH		Reset Value = 0x20H				
ADC Offset Value High Byte							
	ADCOS_H [15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

14.6 ADC Auto Sample Date Register (ADCAUTO)

Table 56 14.6 ADC Auto Sample Date Register (ADCAUTO)

SFR	Description						
ADCAUTO_L	ADC Auto Sample Data Register Low Byte						
ADCAUTO_H	ADC Auto Sample Data Register High Byte						
	Parameters			**Description**			**Reset Value**
SFR_PAGE = 0	ADCDATA_CH2			ADC Channel 2 Data			0x0000H
SFR_PAGE = 1	ADCDATA_CH3			ADC Channel 3 Data			0x0000H
ADCAUTO_L	Address = CBH			Reset Value = 0x00H			
ADC Auto Sample Data Register Low Byte							
	ADCAUTO_L [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R
ADCAUTO_H	Address =CCH			Reset Value = 0x00H			
ADC Auto Sample Data Register High Byte							
	ADCAUTO _H [15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

15. EEPROM

The **MDSF40** provides internal flash control signals which can do byte read/write in total 256-byte and page erase in last page of flash. The read/write address, data, and command are control by EE_ADDR, EE_DATA, and EE_CMD register respectively which in the page of EEPROM SFR.

Table 57 15. EEPROM

SYMBOL	DIRECT ADDRESS	SFR_PAGE						
	[L,H]	0	1	2	3	4	5	6
EEPROM								
EEPROM	A3H	EE_ADDR	EE_DATA	EE_CMD				

MDSF40

SFR	Description		
EEPROM	EEPROM Function in FLASH		
SFR_PAGE	**Parameters**	**Description**	**Reset Value**
SFR_PAGE = 0	EE_ADDR	EEPROM read/write address	0x00H
SFR_PAGE = 1	EE_DATA	EEPROM read/write data	0x00H
SFR_PAGE = 2	EE_CMD	EEPROM command	0x00H

Figure 23 EEPROM control flow

Erase EEPROM Flow : Erase Command Erase Flag = 1 : is erasing / Erase Flag = 0 : erase down

Read EEPROM Flow : Read Address → Read Command Read Flag = 1 : is reading / Read Flag = 0 : read down

Write EEPROM Flow : Write Address → Write Data / Write Data → Write Address → Write Command Write Flag = 1 : is writing / Write Flag = 0 : read down
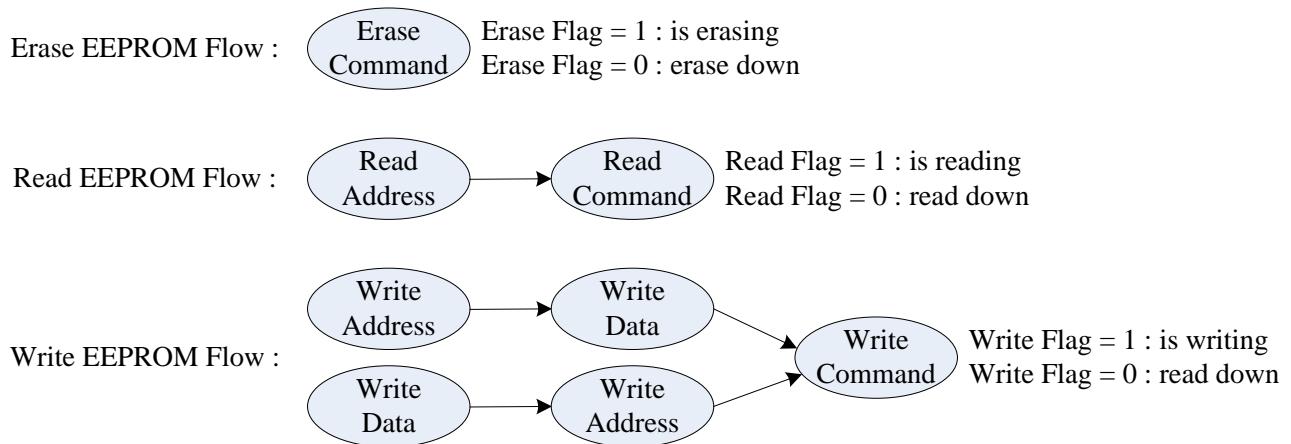
EEPROM control flow

15.1 EEPROM Read/Write Address Register (EE_ADDR)

Table 58 15.1 EEPROM Read/Write Address Register (EE_ADDR)

EE_ADDR	Address = A3H (SFR_PAGE = 0)				Reset Value = 0x00H		
EEPROM read/write address							
	EE_ADDR [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.2 EEPROM Read/Write Data Register (EE_Data)

Table 59 15.2 EEPROM Read/Write Data Register (EE_Data)

EE_DATA	Address = A3H (SFR_PAGE = 1)				Reset Value = 0x00H		
EEPROM read/write data							
	EE_DATA [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.3 EEPROM Command Register (EE_CMD)

Table 60 15.3 EEPROM Command Register (EE_CMD)

EE_CMD	Address = A3H (SFR_PAGE = 2)				Reset Value = 0x00H		
EEPROM command							
	EE_CMD [7:0]						
	ERS_FLAG	---	WR_FLAG	RD_FLAG	ERASE	---	WR_CMD	RD_CMD
Bit	7	6	5	4	3	2	1	0
Type	R/W	---	R/W	R/W	R/W	---	R/W	R/W
ERS_FLAG	EEPROM ERASE Flag:						
[7]	1 : EEPROM Erase progressing						
WR_FLAG	EEPROM WRITE Flag:						
[5]	1 : EEPROM Write progressing						
RD_FLAG	EEPROM READ Flag:						
[4]	1 : EEPROM Read progressing						
ERASE	EERPOM ERASE:						
[3]	1 : ERASE command						
WR_CMD	EERPOM WRITE command:						
[1]	1 : WRITE command						
RD_CMD	EERPOM READ command:						
[0]	1 : READ command						

16. IIC Emulation

The IIC module uses the SCL (clock) and the SDA (data) line to communicate with external IIC interface. Its speed can be selected to 400Kbps (maximum) by software setting the IICBR [2:0] control bit. The IIC module provided 2 interrupts (RXIF, TXIF). It will generate START, repeated START and STOP signals automatically in master mode and can detects START, repeated START and STOP signals in slave mode. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400pF.

Table 61 The interrupt vector is 63h.

SFR	Description	address	Reset value
IICS	IIC Status Register	E8H	00H
IICCTRL	IIC Control Register	E9H	04H
IICA1	IIC Address 1 Register	EAH	A0H
IICA2	IIC Address 2 Register	EBH	60H
IICRWD	IIC Read Write Register	BAH	00H
IICEBT	IIC Enable Bus Transaction Register	9CH	00H

16.1 IIC Control Register (IICCTL)

Table 62 16.1 IIC Control Register (IICCTL)

IICCTL			Address = E9H			Reset Value = 0x04H	
IIC Control Register							
	IICEN	MSS	MAS	AB_EN	BF_EN	IICBR[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IICEN	Enable IIC module
[7]	0 : Disable
	1 : Enable
MSS	Master or slave mode select
[6]	0 : slave mode
	1 : master mode *The software must set this bit before setting others register.
MAS	Master address select (master mode only)
[5]	0 : Master address is to use IICA1
	1 : Master address is to use IICA2
AB_EN	Arbitration lost enable bit. (Master mode only)
[4]	If set AB_EN bit, the hardware will check arbitration lost. Once arbitration lost occurred, hardware will return to IDLE state. If this bit is cleared, hardware will not care arbitration lost condition. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.
BF_EN	Bus busy enable bit. (Master mode only)
[3]	If set BF_EN bit, hardware will not generate a start condition to bus until BF=0. Clear this bit will always generate a start condition to bus when MStart is set. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.
IICBR	Baud rate selection (master mode only) , where Fosc is 12MHz

IICBR		
[2:0]	000 : Fosc/32	100 : Fosc/512
	001 : Fosc/64	101 : Fosc/1024
	010 : Fosc/128	110 : Fosc/2048
	011 : Fosc/256	111 : Fosc/4096

16.2 IIC Status Register (IICS)

Table 63 16.2 IIC Status Register (IICS)

IICS			Address = E8H			Reset Value = 0x00H		
IIC Status Register								
	---	MPIF	LAIF	RXIF	TXIF	RXAK	TXAK	RW or BB
Bit	7	6	5	4	3	2	1	0
Type	---	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MPIF	The Stop condition Interrupt Flag
[6]	The stop condition occurred and this bit will be set. Software need to clear this bit.
LAIF	Arbitration lost bit. (Master mode only)
[5]	The Arbitration Interrupt Flag, the bus arbitration lost occurred and this bit will be set. Software need to clear this bit.
RXIF	The data Receive Interrupt Flag
[4]	RXIF is set after the IICRWD (IIC Read Write Data Buffer) is loaded with a newly receive data.
TXIF	The data Transmit Interrupt Flag
[3]	TXIF is set when the data of the IICRWD (IIC Read Write Data Buffer) is downloaded to the shift register.
RXAK	The Acknowledge Status indicate bit
[2]	When clear, it means an acknowledge signal has been received after the complete 8 bits data transmit on the bus.
TXAK	The Acknowledge status transmit bit
[1]	When received complete 8 bits data, this bit will set (NoAck) or clear (Ack) and transmit to master to indicate the receive status.
RW or BB	Bus busy or slave mode read/write on the IIC bus
[0]	**Master Mode:** BB : Bus busy bit If detect scl=0 or sda=0 or bus start, this bit will be set. If detect stop,this bit will be cleared. This bit can be cleared by software to return ready state. **Slave Mode:** RW : The slave mode read (received) or wrote (transmit) on the IIC bus. When this bit is clear, the slave module received data on the IIC bus (SDA).(Slave mode only).

16.3 IIC Address1 Register (IICA1)

Table 64 16.3 IIC Address1 Register (IICA1)

IICA1			Address = EAH				Reset Value = 0xA0H
IIC Address1 Register							
	IICA1						Match1 or RW1
Bit	7	6	5	4	3	2	1	0
Type	R/W							R or R/W
Slave mode								
IICA1	IIC Address1 registers							
[7:1]	This is the first 7-bit address for this slave module. It will be checked when an address (from master) is received.							
Match1	IICA1 match bit (Read only)							
[0]	When IICA1 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets first data, this bit will clear.							
Master mode								
IICA1	IIC Address1 registers							
[7:1]	This 7-bit address indicates the slave with which it wants to communicate.							
RW1	Master read/write mode indicate							
[0]	This bit will be sent out as RW of the slave side if the module has set the MStart or RStart bit. It appears at the 8th bit after the IIC address as below figure. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master transmit mode. The Fig. as shown as follow. RW1=1, master receive mode RW1=0, master transmit mode							

16.4 IIC Address2 Register (IICA2)

Table 65 16.4 IIC Address2 Register (IICA2)

IICA2			Address = EBH				Reset Value = 0x60H
IIC Address 2 Register							
	IICA2						Match2 or RW2
Bit	7	6	5	4	3	2	1	0
Type	R/W							R or R/W
Slave mode								
IICA2	IIC Address2 registers							
[7:1]	This is the second 7-bit address for this slave module. It will be checked when an address (from master) is received.							

Match2	IICA2 match bit (Read only)
[0]	When IICA2 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets first data, this bit will clear.
Master mode	
IICA2	IIC Address registers
[7:1]	This 7-bit address indicates the slave with which it wants to communicate.
RW2	Master read/write mode indicate
[0]	This bit will be sent out as RW of the slave side if the module has set the MStart or RStart bit. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master transmit mode. RW2=1, master receive mode RW2=0, master transmit mode

16.5 IIC Read Write Register (IICRWD)

Table 66 16.5 IIC Read Write Register (IICRWD)

IICRWD				Address = BAH			Reset Value = 0x00H	
IIC Read Write Register								
	IICRWD							
Bit	7	6	5	4	3	2	1	0
Type	R/W							
IICRWD	IIC read write data buffer							
[7:0]	In receiving (read) mode, the received byte is stored here.							
	In transmitting mode, the byte to be shifted out through SDA stays here.							

16.6 IIC Enable Transaction Register (IICEBT)

Table 67 16.6 IIC Enable Transaction Register (IICEBT)

IICEBT			Address = 9CH				Reset Value = 0x00H	
IIC Enable Transaction Register								
	FU_EN		---	---	---	---	---	---
Bit	7	6	5	4	3	2	1	0
Type	R/W		---	---	---	---	---	---
Master mode								
[7:6]	Function Enable							
	00 :	reserved						
	01 :	IIC bus module will enable read/write data transfer on SDA and SCL						
	10 :	IIC bus module generate a start condition on the SDA/SCL, then send out address which is stored in the IICA1/IICA2(selected by MAS control bit)						

	11 :	IIC bus module generates a stop condition on the SDA/SCL.
Notice :	\multicolumn{2}{l}{1. FU_EN[7:6] will be auto-clear by hardware, so setting FU_EN[7:6] repeatedly is necessary.}

Slave mode		
[7:6]	\multicolumn{2}{l}{Function Enable}
	01 :	FU_EN[7:6] should be set as 01 only. The other value is inhibited.
Notice :	\multicolumn{2}{l}{1. FU_EN[7:6] should be set as 01 before read/write data transfer for bus release; otherwise, SCL will be locked(pull low). 2. FU_EN[7:6] should be set as 01 after read/write data transfer for receiving a stop condition from bus master. 3. In transmit data mode(slave mode), the output data should be filled into IICRWD before setting FU_EN[7:6] as 01. 4. FU_EN[7:6] will be auto-clear by hardware, so setting FU_EN[7:6] repeatedly is necessary.}

17. Capture

The **MDSF40** provides external and internal signal capture function that can count the high level length and the period length of the external and internal signal. The interrupt will issue after a rising edge of the external or internal capture signal, and it is combine external signal capture and internal signal capture interrupt. User must to monitor the external capture OK (E_CAP_OK) and internal capture OK (I_CAP_OK) in the capture interrupt routine to distinguish which counter can access, and it is cleared by user when set the clear capture OK flag (EOK_CLR or UOK_CLR) bit "1". The external and internal capture function are share same SFR but separate in different page.

Table 68 17. Capture

SYMBOL	DIRECT ADDRESS		SFR_PAGE						
	[L,H]		0	1	2	3	4	5	6
CAPTURE									
CAPCONT	DDH		E_CAPCONT	I_CAPCONT					
CAPT [L,H]	D9H	DAH	EXT_CAPT	INT_CAPT					
CAPH[L,H]	DBH	DCH	EXT_CAPH	INT_CAPH					

17.1 External Capture

Figure 24 External Capture control waveform of external capture
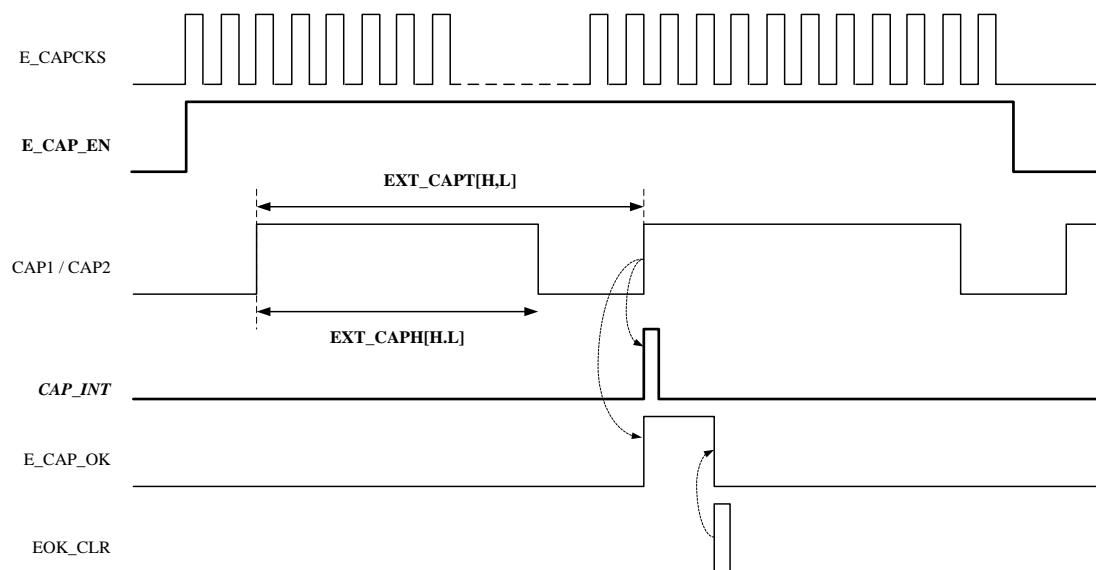
The control waveform of external capture

17.1.1 External Signal Capture Control Register (E_CAPCONT)

Table 69 17.1.1 External Signal Capture Control Register (E_CAPCONT)

E_CAPCONT	Address = DDH **(SFR_PAGE = 0)**			Reset Value = 0x03H			
External Signal Capture Control							
	E_CAPCONT [7:0]						
	E_CAP_EN	E_CAP_OK	---	CAPPINSEL	EOK_CLR	E_CAPCKS[2:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	---	R/W	W	R/W	R/W	R/W

E_CAP_EN	External Capture Enable
[7]	0: External Capture Disable
	1: External Capture Enable
E_CAP_OK	External Capture OK :
[6]	1 : External signal capture down, clear by user.
CAPPINSEL	External Capture input pin select :
[4]	0 : CAP2(P0.7)
	1 : CAP1(P0.6)
EOK_CLR	External Capture OK Clear :
[3]	1 : clear the **E_CAP_OK** bit.
E_CAPCKS	External Capture clock select :
[2:0]	000 : 48MHz/4	100 : 48MHz/64
	001 : 48MHz/8	101 : 48MHz/128
	010 : 48MHz/16	110 : 48MHz/256
	011 : 48MHz/32	111 : 48MHz/512

17.1.2 External Signal Capture Total Count Register (EXT_CAPT)

Table 70 17.1.2 External Signal Capture Total Count Register (EXT_CAPT)

EXT_CAPT_L	Address = D9H **(SFR_PAGE = 0)**			Reset Value = 0x00H			
External Signal Capture Total Count Low Byte							
	EXT_CAPT[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

EXT_CAPT_H	Address = DAH **(SFR_PAGE = 0)**			Reset Value = 0x00H			
External Signal Capture Total Count High Byte							
	EXT_CAPT[15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.1.3 External Signal Capture High-Level Count Register (EXT_CAPH)

Table 71 17.1.3 External Signal Capture High-Level Count Register (EXT_CAPH)

EXT_CAPH_L		Address = DBH **(SFR_PAGE = 0)**				Reset Value = 0x00H	
External Signal Capture High-level Count Low Byte							
	EXT_CAPH[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

EXT_CAPH_H		Address = DCH **(SFR_PAGE = 0)**				Reset Value = 0x00H	
External Signal Capture High-level Count High Byte							
	EXT_CAPH[15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.2 Internal Capture

Figure 25 Internal Capture control waveform
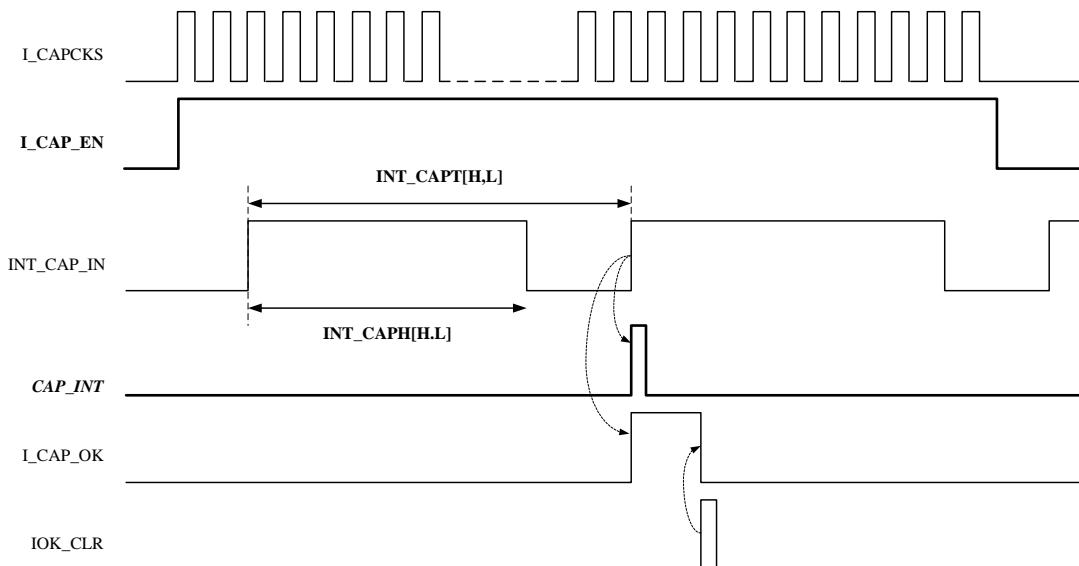
The control waveform of internal capture

17.2.1 Internal Signal Capture Control Register (I_CAPCONT)

Table 72 17.2.1 Internal Signal Capture Control Register (I_CAPCONT)

I_CAPCONT		Address = DDH **(SFR_PAGE = 1)**			Reset Value = 0x03H		
External Signal Capture Control							
				I_CAPCONT [7:0]			
	I_CAP_EN	I_CAP_OK	---	INT_CAP_IN	IOK_CLR	I_CAPCKS[2:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	---	R/W	W	R/W	R/W	R/W

I_CAP_EN	Internal Capture Enable
[7]	0: Internal Capture Disable
	1: Internal Capture Enable
I_CAP_OK	Internal Capture OK :
[6]	1 : Internal signal capture down, clear by user.
INT_CAP_IN	Internal Capture Input Data:
[4]	0 : Data 0 input
	1 : Data 1 input
IOK_CLR	Internal Capture OK Clear :
[3]	1 : clear the **I_CAP_OK** bit.
I_CAPCKS	Internal Capture clock select :
[2:0]	000 : 48MHz/4	100 : 48MHz/64
	001 : 48MHz/8	101 : 48MHz/128
	010 : 48MHz/16	110 : 48MHz/256
	011 : 48MHz/32	111 : 48MHz/512

17.2.2 Internal Signal Capture Total Count Register (INT_CAPT)

Table 73 17.2.2 Internal Signal Capture Total Count Register (INT_CAPT)

INT_CAPT_L		Address = D9H **(SFR_PAGE = 1)**			Reset Value = 0x00H		
Internal Signal Capture Total Count Low Byte							
				INT_CAPT[7:0]			
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

INT_CAPT_H		Address = DAH **(SFR_PAGE = 1)**			Reset Value = 0x00H		
Internal Signal Capture Total Count High Byte							
				INT_CAPT[15:8]			
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.2.3 Internal Signal Capture High-Level Count Register (INT_CAPH)

Table 74 17.2.3 Internal Signal Capture High-Level Count Register (INT_CAPH)

INT_CAPH_L	Address = DBH **(SFR_PAGE = 1)**			Reset Value = 0x00H			
Internal Signal Capture High-level Count Low Byte							
	INT_CAPH[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

INT_CAPH_H	Address = DCH **(SFR_PAGE = 1)**			Reset Value = 0x00H			
Internal Signal Capture High-level Count High Byte							
	INT_CAPH[15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

18. Multiplication and Division Unit (MDU)

The **MDU** is an on-chip arithmetic co-processor which enables the **MDSF40** to perform additional extended arithmetic operations. All operations are singed/unsigned integer operations. Operands and results are stored in **MD0**–**MD5** registers. The module is controlled by the **MD_MODE** and **MD_CTRL** register. Any calculation of the **MDU** overwrites its operands. The **MDU** support five operations: Division 32-bit/16-bit, Division 16-bit/16-bit, Multiplication, Shift and Normalize.

Table 75 18. Multiplication and Division Unit (MDU)

XSFR	Description	address	Reset value
MD_MODE	MDU Mode Control Register	1030H	10H
MD_CTRL	MDU Control Register	1031H	00H
MD0	Multiplication Division Register 0	1032H	00H
MD1	Multiplication Division Register 1	1033H	00H
MD2	Multiplication Division Register 2	1034H	00H
MD3	Multiplication Division Register 3	1035H	00H
MD4	Multiplication Division Register 4	1036H	00H
MD5	Multiplication Division Register 5	1037H	00H

18.1 MDU Mode Control Register (MD_MODE)

Table 76 18.1 MDU Mode Control Register (MD_MODE)

MD_MODE			Address = 1030H			Reset Value = 0x10H	
MDU Mode Control Register							
	-----	-----	-----	MDUF	-----	-----	MDUS	----
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R	X	X	R/W	X

MDUF	MDU finish flag :
[4]	0 : MDU busy.
	1 : MDU calculation finished.
MDUS	MDU Signed select :
[1]	0 :Signed calculation.
	1 :Unsigned calculation.

18.2 MDU Control Register (MD_CTRL)

Table 77 18.2 MDU Control Register (MD_CTRL)

MD_CTRL			Address = 1031H			Reset Value = 0x10H	
MDU Control Register							
	MDEF	MDOV	SLR	SC[4:0]				
Bit	7	6	5	4	3	2	1	0
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W

MDEF	MDU Error flag :
[7]	Indicates an improperly performed operation (when one of the arithmetic operations has been restarted or interrupted by a new operation).
MDOV	MDU Overflow flag :
[6]	Overflow occurrence in the MDU operation.
SLR	Shift direction :
[5]	0 : shift left operation
	1 : shift right operation
SC	Shift counter :
[4:0]	When set to all '0's, normalize operation is selected. After normalization, the SC[4:0] contain the number of normalizing shifts performed.
	When at least one of these bit is set high shift operation is selected. The number of shifts performed is determined by the number written to SC[4:0], where SC.4 is the MSB.

18.3 MD0 – MD5 (Multiplication Division Register)

Table 78 18.3 MD0 – MD5 (Multiplication Division Register)

MD0		Address = 1032H				Reset Value = 0x00H		
Multiplication Division Register 0								
	MD0[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD1		Address = 1033H				Reset Value = 0x00H		
Multiplication Division Register 1								
	MD1[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD2		Address = 1034H				Reset Value = 0x00H		
Multiplication Division Register 2								
	MD2[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD3		Address = 1035H				Reset Value = 0x00H		
Multiplication Division Register 3								
	MD3[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

18.4 MDU Operation Description

The operation of the **MDU** consists of three phases:

18.4.1 Loading the MDx registers

The type of calculation the **MDU** has to perform is selected by the order in which the MDx registers are written to. A write to **MD0** is the first transfer to be done in any case. Next writes must be done as shown in the table below to determine the **MDU** operation. The last write will start the selected operation.

Table 79 18.4 MDU Operation Description

Operation	32-bit/16-bit	16-bit/-16bit	16-bit x 16-bit	Shift/ normalizing
First write	MD0 Dividend Low	MD0 Dividend Low	MD0 Multiplicand Low	MD0 LSB
	MD1 Dividend	MD1 Dividend High	MD4 Multiplicator Low	MD1
	MD2 Dividend		MD1 Multiplicand High	MD2
	MD3 Dividend High			MD3 MSB
	MD4 Divisor Low	MD4 Divisor Low		
Last write	MD5 Divisor High	MD5 Divisor High	MD5 Multiplicator High	MD_CONT start conversion

MDSF40

18.4.2 Executing calculation

During the calculation period, the **MDU** works in parallel to the CPU. When the calculation is complete, the hardware will set the **MDUF** bit to one (**MDUF** = '1'). The flag will be cleared at the next calculation.

Table 80 The following table provides the execution time for each mathematical operation.

Operation	Number of clock cycles	
Division 32-bit/16-bit	17 clock cycles	
Division 16-bit/16-bit	9 clock cycles	
Multiplication	11 clock cycles	
Shift	Min 3 clock cycles (SC = 01H)	Max 18 clock cycles (SC = 1FH)
Normalize	Min 4 clock cycles (SC <= 01H)	Max 19 clock cycles (SC = 1FH)

18.4.3 Reading the result from the MDx registers

The Read-out sequence of the first "MDx" registers is not critical but the last read determines the end of a whole calculation.

Table 81 18.4.3 Reading the result from the MDx registers

Operation	32-bit/16-bit	16-bit/16-bit	16-bit x 16-bit	Shift/ normalizing
First read	MD0 Quotient Low	MD0 Quotient Low	MD0 Product Low	MD0 LSB
	MD1 Quotient	MD1 Quotient High	MD1 Product	MD1
	MD2 Quotient		MD2 Product	MD2
	MD3 Quotient High			
	MD4 Remainder Low	MD4 Remainder Low		
Last read	MD5 Remainder High	MD5 Remainder High	MD3 Product High	MD3 MSB

18.4.4 Shifting

In shift operation, 32-bit integer variable stored in **MD0** to **MD3** registers (the latter contains the most significant byte) is shifted left or right by a specified number of bits. The **SLR** bit (**MD_CONT**.5) defines the shift direction, and bits **SC**[4:0] (**MD_CONT**.4 –**MD_CONT**.0) specifies the shift count (which must not be 0). During shift operation, zeroes come into the left end of **MD3** for shifting right or right end of the **MD0** for shifting left.

18.4.5 Normalizing

All leading zeroes of 32-bit integer variable stored in **MD0** to **MD3** registers, the latter contains the most significant byte are removed by shift left operations. The whole operation is completed when the MSB (most significant bit) of **MD3** register contains a '1'. After normalizing, bits **SC**[4:0] (**MD_CONT**.4 – **MD_CONT**.0) contain the number of shift left operations, which were done.

19. Cyclic Redundant Check (CRC)

This CRC check function is based on CRC16-CCITT polynomial $X^{16} + X^{12} + X^5 + 1$. The general architecture of CRC computation is using LSFR and XOR by serial. The architecture is modified by parallel computation for speed up the compute time in the MDSF40.

Figure 26 The general LSFR architecture of CRC16-CCITT
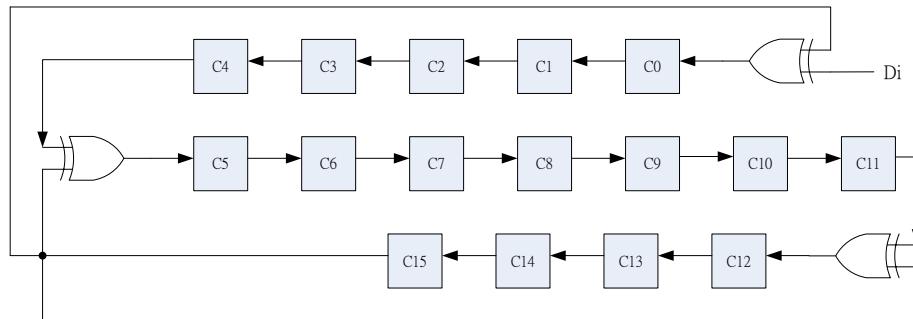
The general LSFR architecture of CRC16-CCITT

The CRC function can support byte data and flash bank CRC computation. The data selection and the control are setting by the CRC XSFRs.

Table 82 CRC SFR Table

XSFR	Description	address	Reset value
CRC_CTRL	CRC Control Register	1018H	00H
CRC_DIN	CRC Input Data Register	1019H	00H
CRC_DOUT_L	CRC Output Remainder Low Byte Data Register	101AH	00H
CRC_DOUT_H	CRC Output Remainder High Byte Data Register	101BH	00H
CRC_STR_BANK	Start Bank Index for Flash Bank CRC Computation	101CH	00H
CRC_END_BANK	End Bank Index for Flash Bank CRC Computation	101DH	00H

Figure 27 The byte and flash bank CRC computation architecture
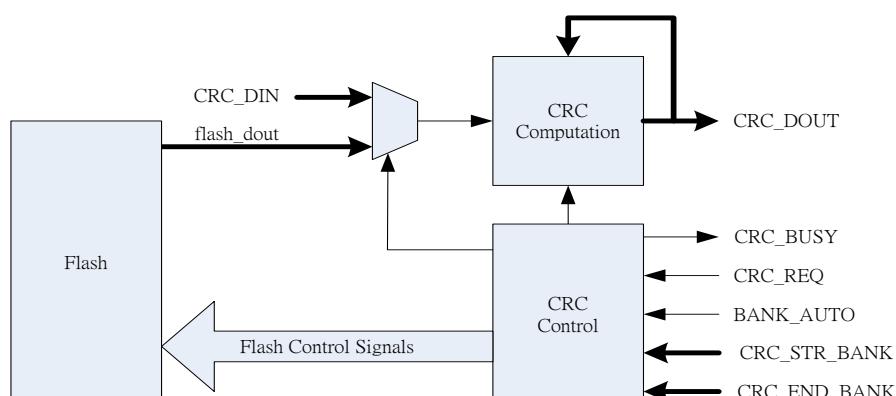
The byte and flash bank CRC computation architecture

19.1 CRC Control Register (CRC_CTRL)

Table 83 19.1 CRC Control Register (CRC_CTRL)

CRC_CTRL		Address = 1018H						Reset Value = 0x00H
CRC Control Register								
	CRC_REQ	CRC_BUSY	---	---	---	---	---	BANK_AUTO
Bit	7	6	5	4	3	2	1	0
Type	W	W	----	---	---	---	---	R/W

CRC_REQ	CRC Computation Request:
[7]	1 : CRC Computation Request
CRC_BUSY	CRC Computation Busy:
[6]	0 : CRC Computation Down
	1 : CRC Computation Busy
BANK_AUTO	Enable Bank CRC Computation:
[0]	0 : Disable (CRC_DIN 1-byte CRC Computation).
	1 : Enable (Bank multi-byte CRC Computation)

19.2 CRC Input Data Register (CRC_DIN)

Table 84 19.2 CRC Input Data Register (CRC_DIN)

CRC_DIN		Address = 1019H						Reset Value = 0x00H
CRC Input Data Register								
	CRC_DIN [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

19.3 CRC Output Remainder Data Register (CRC_DOUT_H, CRC_DOUT_L)

Table 85 19.3 CRC Output Remainder Data Register (CRC_DOUT_H, CRC_DOUT_L)

CRC_DOUT_L		Address = 101AH						Reset Value = 0x00H
CRC Output Remainder Low Byte Data Register								
	CRC_DOUT [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

CRC_DOUT_H			Address = 101BH			Reset Value = 0x00H	
CRC Output Remainder High Byte Data Register							
	CRC_DOUT [15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

19.4 Start Bank Index for Bank CRC Computation (CRC_STR_BANK)

Table 86 19.4 Start Bank Index for Bank CRC Computation (CRC_STR_BANK)

CRC_STR_BANK			Address = 101CH			Reset Value = 0x00H	
Start Bank Index for Flash Bank CRC Computation							
	CRC_STR_BANK						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CRC_STR_BANK	Start Bank Index for Flash Bank CRC Computation:
[7:0]	0~127

19.5 End Bank Index for Bank CRC Computation (CRC_END_BANK)

Table 87 19.5 End Bank Index for Bank CRC Computation (CRC_END_BANK)

CRC_END_BANK				Address = 101DH			Reset Value = 0x00H	
End Bank Index for Flash Bank CRC Computation								
	CRC_END_BANK							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CRC_END _BANK [7:0]	End Bank Index for Flash Bank CRC Computation: 0~127							

16K Bytes Flash ROM
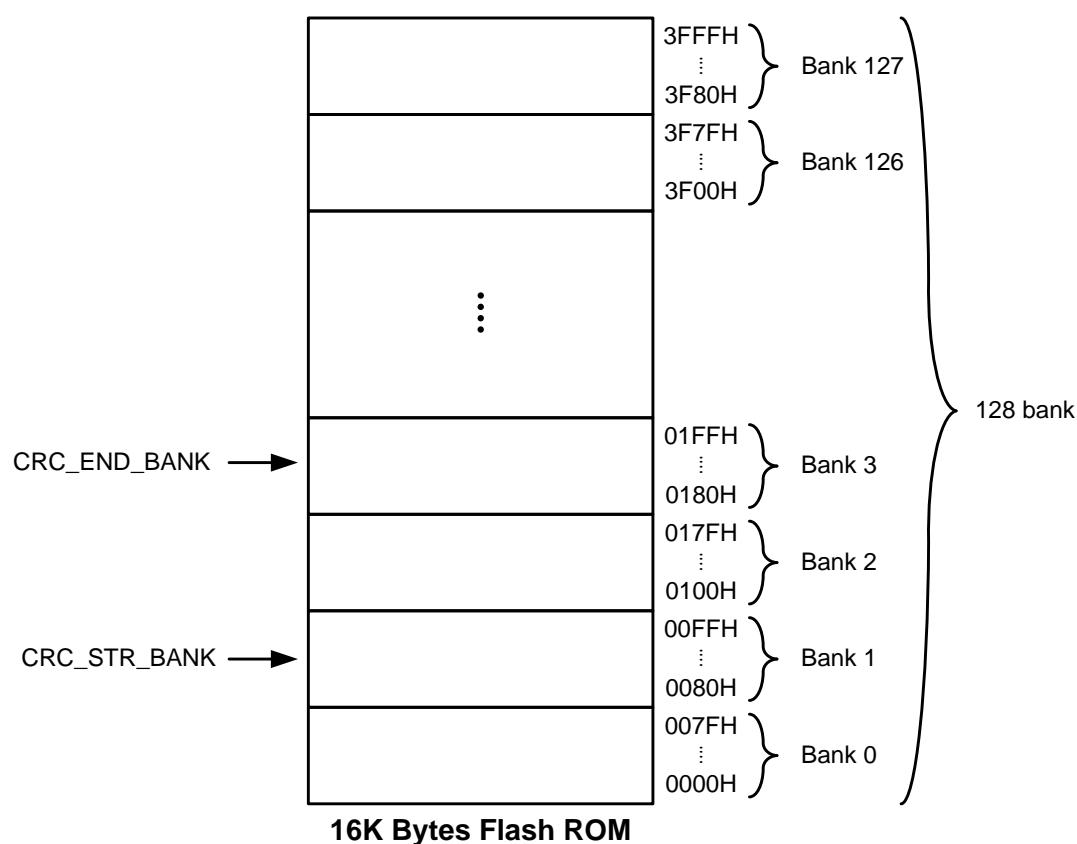
EX:
CRC_STR_BANK = 0x01
CRC_END_BANK = 0x03
The bank range for CRC computation : (0x01 ~ 0x03) bank

The example of bank assign for bank CRC computation

20. Independent General PWM

MDSF40 support one16-bit independent general PWM output for other duty control application.

Table 88 20. Independent General PWM

XSFR	Description	address	Reset value
IPWM_MAX_L	Independent General PWM Max Low Byte	1020H	02H
IPWM_MAX _H	Independent General PWM Max High Byte	1021H	00H
IPWM_DUTY_L	Independent General PWM Duty Low Byte	1022H	FFH
IPWM_DUTY_H	Independent General PWM Duty High Byte	1023H	FFH
IPWM_CTRL	Independent General PWM Control Register	1024H	00H

Figure 28 Independent general PWM generator
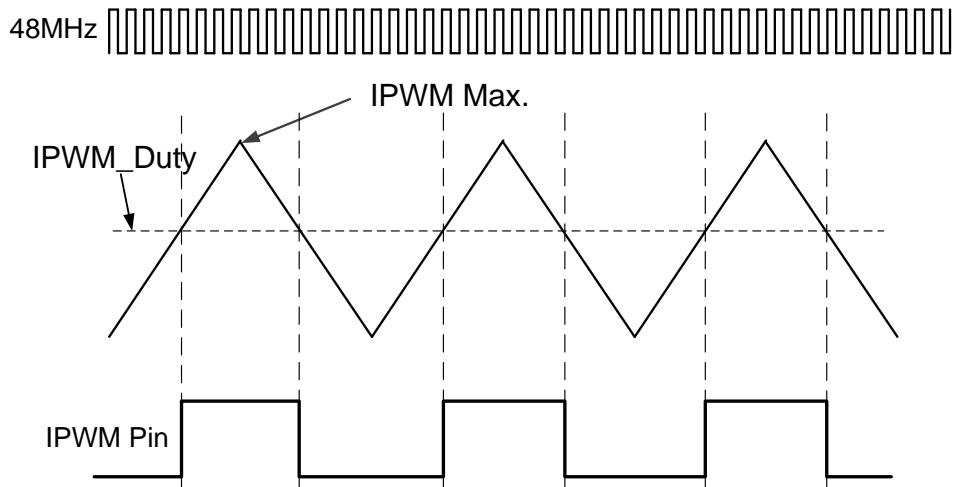
Independent general PWM generator

20.1 Independent General PWM Control Register (IPWM_CTRL)

Table 89 20.1 Independent General PWM Control Register (IPWM_CTRL)

IPWM_CTRL				Address = 1024H			Reset Value = 0x00H	
Independent General PWM Control Register								
	----	----	----	----	----	IPWM_MODE		IPWM_EN
Bit	7	6	5	4	3	2	1	0
Type	----	----	----	----	----	R/W		R/W

IPWM_MODE	Independent General PWM mode select:
[2:1]	00 : Force Low
	01 : Force High
	10 : Active High
	11 : Active Low
IPWM_EN	Independent General PWM enable:
[0]	0 : Disable
	1 : Enable.

20.2 Independent General PWM Max Register (IPWM_MAX)

Table 90 20.2 Independent General PWM Max Register (IPWM_MAX)

IPWM_MAX_L				Address = 1020H			Reset Value = 0x02H	
Independent General PWM Max. Low Byte								
	IPWM_ MAX _L [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IPWM_MAX_H				Address = 1021H			Reset Value = 0x00H	
Independent General PWM Max. High Byte								
	IPWM_ MAX _H [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

20.3 Independent General PWM Duty Register (IPWM_DUTY)

Table 91 20.3 Independent General PWM Duty Register (IPWM_DUTY)

IPWM_DUTY_L			Address = 1022H			Reset Value = 0xFFH	
Independent General PWM Duty Low Byte							
	IPWM_DUTY_L [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IPWM_DUTY_H			Address = 1023H			Reset Value = 0xFFH	
Independent General PWM Duty High Byte							
	IPWM_DUTY_H [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

21. One Wire RF/IR Signal Decode

The one wire RF/IR signal decode function can decode one wire data automatically by hardware that after setting the data format and type by IR decode XSFR. The maximum decode data is 48 bits. It can decode the output data of RF receiver module or control board.

Figure 29 Block of one wire signal decode by MDSF40
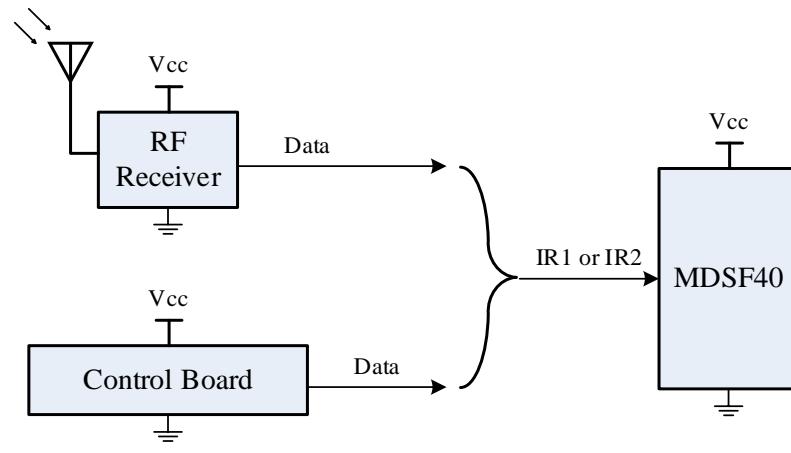
One wire signal decode by MDSF40

Table 92 One wire signal SFR

XSFR	Description	address	Reset value
IR_DEC_SET	IR Data Decode Setting Register	1038H	00H
IR_DEC_CTRL	IR Data Decode Control Register	1039H	00H
IR_HEADER_Z1_L	IR Data HEADER Zone1 Low Byte Cycles Register	103AH	80H
IR_HEADER_Z1_H	IR Data HEADER Zone1 High Byte Cycles Register	103BH	BBH
IR_HEADER_Z2_L	IR Data HEADER Zone2 Low Byte Cycles Register	103CH	00H
IR_HEADER_Z2_H	IR Data HEADER Zone2 High Byte Cycles Register	103DH	7DH
IR_STOP_Z_L	IR Data STOP Zone Low Byte Cycles Register	103EH	80H
IR_STOP_Z_H	IR Data STOP Zone High Byte Cycles Register	103FH	BBH
IR_DOUT0	IR Decode Output Data Byte0	1040H	00H
IR_DOUT1	IR Decode Output Data Byte1	1041H	00H
IR_DOUT2	IR Decode Output Data Byte2	1042H	00H
IR_DOUT3	IR Decode Output Data Byte3	1043H	00H
IR_DOUT4	IR Decode Output Data Byte4	1044H	00H
IR_DOUT5	IR Decode Output Data Byte5	1045H	00H

21.1 IR Data Decoder Setting Register (IR_DEC_SET)

Table 93 21.1 IR Data Decoder Setting Register (IR_DEC_SET)

IR_DEC_SET		Address = 1038H			Reset Value = 0x00H		
IR Data Decoder Setting Register							
	HEADER_EN	DOUT_REV	DIN_TYP	DIN_DB		CLK_DIV_SEL	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W		R/W		

HEADER_EN	Input Data with HEADER:
[7]	0 : No HEADER
	1 : With HEADER
DOUT_REV	IR Decode Output Data Reverse:
[6]	0 : First input data is LSB
	1 : First input data is MSB
DIN_TYP	Input Data Type:
[5]	0 : Data Type1: Falling to Rising edge: Duty > 50% -> Din = 0; Duty < 50% -> Din = 1
	1 : Data Type2: Falling to Rising edge: Duty > 50% -> Din = 1; Duty < 50% -> Din = 0
DIN_DB_SEL	Input Data De-bounce Time Select:
[4:3]	00 : 0 ns
	01 : 250 ns
	10 : 500 ns
	11 : 1000 ns
CLK_DIV_SEL	Data Decode Clock Frequency Select (**clk_ir_dec**):
[2:0]	000 : 24 MHz
	001 : 16 MHz
	010 : 8 MHz
	011 : 6 MHz
	100 : 3 MHz
	101: 2 MHz

Figure 30 IR Data Type 1

$$\text{IR\_DEC\_SET[5] (DIN\_TYP)} = 0 : \text{Data Type 1}$$
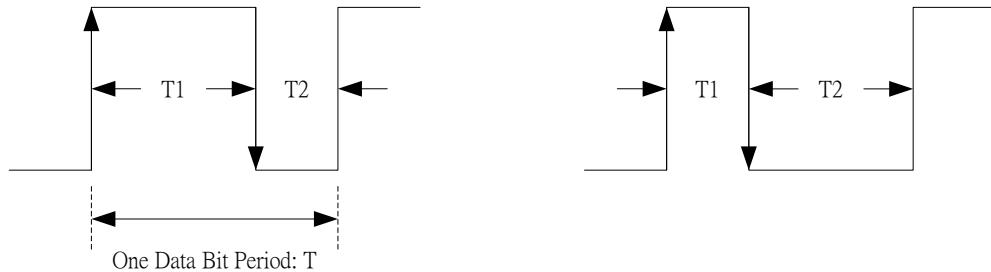
$$T1 > T/2 : \text{Data} = 1 \qquad\qquad T1 < T/2 : \text{Data} = 0$$

Figure 31 IR Data Type 2

$$\text{IR\_DEC\_SET[5] (DIN\_TYP)} = 1 : \text{Data Type 2}$$
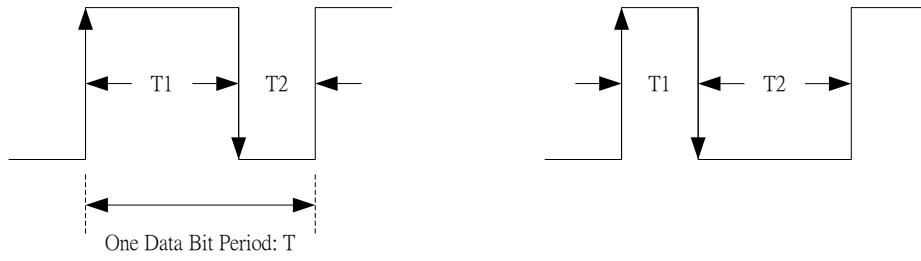
$$T1 > T/2 : \text{Data} = 0 \qquad\qquad T1 < T/2 : \text{Data} = 1$$

The input data type select

Figure 32 IR output data reverse select

$$\text{IR\_DEC\_SET[6] (DOUT\_REV)} = 0 : \text{first input data is LSB}$$
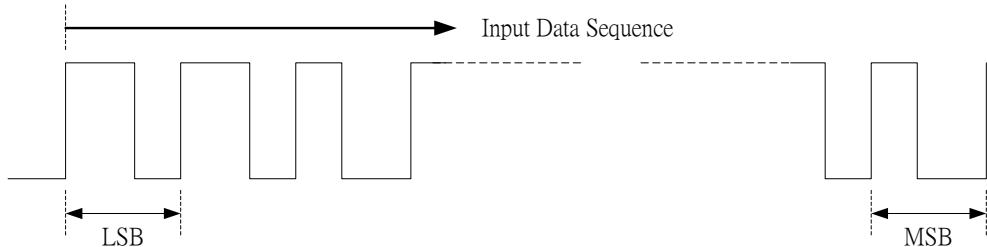
$$\text{IR\_DEC\_SET[6] (DOUT\_REV)} = 1 : \text{first input data is MSB}$$
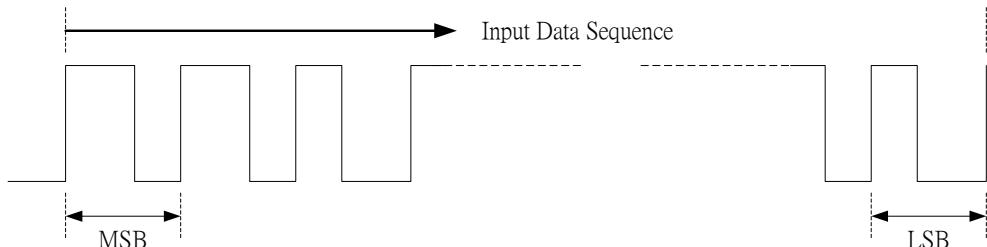
The output data reverse select

21.2 IR Data Decoder Control Register (IR_DEC_CTRL)

Table 94 21.2 IR Data Decoder Control Register (IR_DEC_CTRL)

IR_DEC_CTRL			Address = 1039H				Reset Value = 0x00H	
IR Data Decoder Control Register								
	IR_DEC_EN	IRIN_SEL	---	IR_DEC_OK	---	---	---	IR_DEC_OK_CLR
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	---	R/W	---	---	---	W
IR_DEC_EN	IR Decode Enable:							
[7]	1 : Enable IR Decode.							
IRIN_SEL	IR Decode Data Input Select:							
[6]	0 : IR decode data input from PIN CH3							
	1 : IR decode data input from PIN CH7							
IR_DEC_OK	IR Input Decode OK Flag:							
[4]	1 : IR Input Decode Finish. ***Clear by User***.							
IR_DEC_OK_CLR	Clear IR Decode OK Flag:							
[0]	1 : Clear IR Decode OK Flag (IR_DEC_OK).							

Note:

User must periodicity to monitor the IR_DEC_CTRL[4] (IR_DEC_OK) bit to determine the decoder is completion or not. The decode data can be received when the IR_DEC_OK = 1. And user must to clear the ID_DEC_OK bit by set IR_DEC_CTRL[0] (IR_DEC_OK_CLR) after receive the data for prepare decode next input data.

21.3 IR Data Header Zone1 Cycle Low & High Byte Register (IR_HEADER_Z1_L, IR_HEADER_Z1_H)

Table 95 IR Data Header Zone1 Cycle Low and High Byte Register

IR_HEADER_Z1_L				Address = 103AH			Reset Value = 0x80H	
IR Data HEADER Zone1 Low Byte Cycles Number								
	IR_HEADER_Z1_L							
Bit	7	6	5	4	3	2	1	0
Type	R/W							
IR_HEADER_Z1_L	IR Data Header Zone1 Time Cycles: HEADER_Z1[7:0]							

IR_HEADER_Z1_H				Address = 103BH			Reset Value = 0xBBH	
IR Data HEADER Zone1 High Byte Cycles Number								
	IR_HEADER_Z1_H							
Bit	7	6	5	4	3	2	1	0
Type	R/W							
IR_HEADER_Z1_H	IR Data Header Zone1 Time Cycles: HEADER_Z1[15:8]							

21.4 IR Data Header Zone2 Cycle Low & High Byte Register (IR_HEADER_Z2_L, IR_HEADER_Z2_H)

Table 96 IR Data Header Zone2 Cycle Low and High Byte Register

IR_HEADER_Z2_L				Address = 103CH			Reset Value = 0x00H	
IR Data HEADER Zone2 Low Byte Cycles Number								
	IR_HEADER_Z2_L							
Bit	7	6	5	4	3	2	1	0
Type	R/W							
IR_HEADER_Z2_L	IR Data Header Zone2 Time Cycles: HEADER_Z2[7:0]							

IR_HEADER_Z2_H				Address = 103DH			Reset Value = 0x7DH	
IR Data HEADER Zone2 High Byte Cycles Number								
	IR_HEADER_Z2_H							
Bit	7	6	5	4	3	2	1	0
Type	R/W							
HEADER_Z2_H	IR Data Header Zone2 Time Cycles:HEADER_Z2[15:8]							

21.5 IR Data Stop Zone Cycle Low & High Byte Register (IR_STOP_Z_L, IR_STOP_Z_H)

Table 97 IR Data Stop Zone Cycle Low and High Byte Register

IR_STOP_Z_L				Address = 103EH			Reset Value = 0x80H	
IR Data STOP Zone Low Byte Cycles Number								
	IR_STOP_Z_L							
Bit	7	6	5	4	3	2	1	0
Type	R/W							
IR_STOP_Z_L	IR Data Stop Time Cycles: STOP_Z[7:0]							
IR_STOP_Z_H				Address = 103FH			Reset Value = 0xBBH	
IR Data STOP Zone High Byte Cycles Number								
	IR_STOP_Z_H							
Bit	7	6	5	4	3	2	1	0
Type	R/W							
IR_STOP_Z_H	IR Data Stop Time Cycles: STOP_Z[15:8]							

Note:

1. Data is without header when IR_DEC_SET[7] (HEADER_EN) = 0.

2. IR_HEADER_Z1, IR_HEADER_Z2, and IR_STOP_Z cycles are based on *clk_ir_dec* clock.

Figure 33 IR header and stop signal express
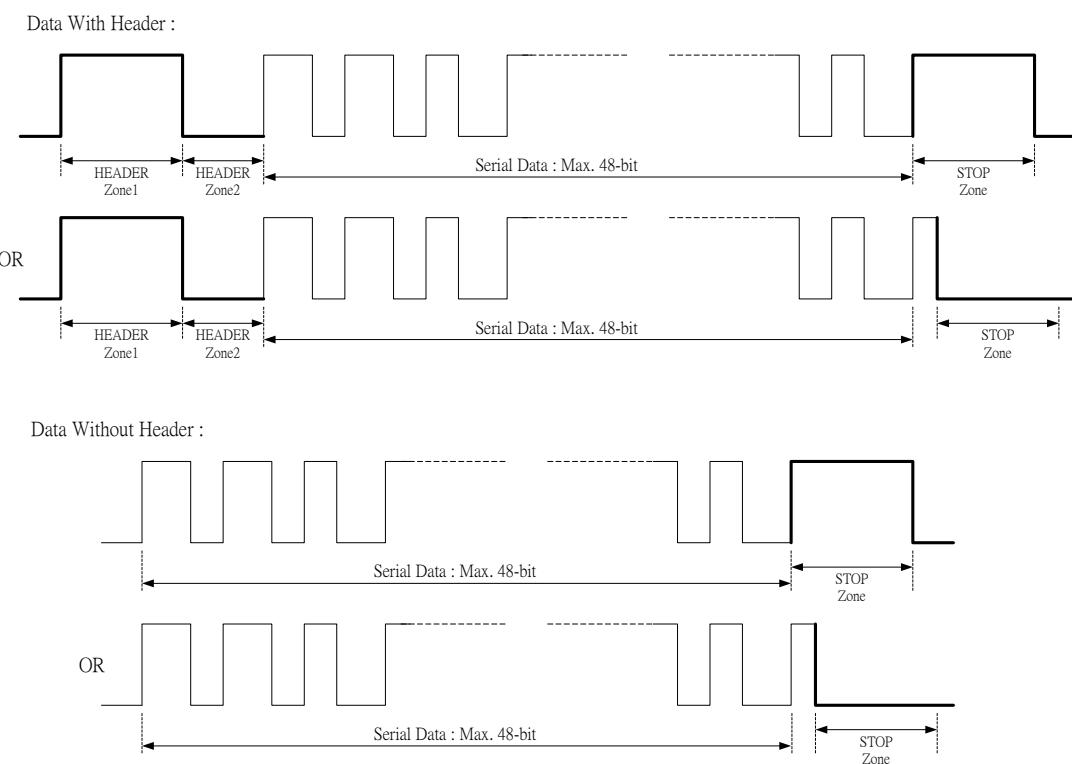
The header and stop signal express

21.6 IR Decode Output Register Byte0 ~ Byte5 (IR_DOUT0 ~ IR_DOUT5)

Table 98 21.6 IR Decode Output Register Byte0 ~ Byte5 (IR_DOUT0 ~ IR_DOUT5)

IR_DOUT0			Address = 1040H			Reset Value = 0x00H		
IR Decode Output Data Byte0								
	IR_DOUT [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

IR_DOUT1			Address = 1041H			Reset Value = 0x00H		
IR Decode Output Data Byte1								
	IR_DOUT [15:8]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

IR_DOUT2			Address = 1042H			Reset Value = 0x00H		
IR Decode Output Data Byte2								
	IR_DOUT [23:16]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

IR_DOUT3			Address = 1043H			Reset Value = 0x00H		
IR Decode Output Data Byte3								
	IR_DOUT [31:24]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

IR_DOUT4			Address = 1044H			Reset Value = 0x00H		
IR Decode Output Data Byte4								
	IR_DOUT [23:16]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

IR_DOUT5			Address = 1045H			Reset Value = 0x00H		
IR Decode Output Data Byte5								
	IR_DOUT [31:24]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

22. Software Reset

MDSF40 support software reset function for reset system by user. It is must release the software reset key before software reset enable.

Table 99 Software Reset

XSFR	Description	address	Reset value
SOFT_RST_KEY	Software Reset Key Register	1028H	00H
SOFT_RST_EN	Software Reset Enable Register	1029H	00H

22.1 Software Reset Key Register (SOFT_RST_KEY)

Table 100 Software Reset Key Register (SOFT_RST_KEY)

SOFT_RST_KEY		Address = 1028H				Reset Value = 0x00H		
Software Reset Key Register								
	SOFT_RST_KEY [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Software reset control key, must write three specific values AAH, 55H and A5H to the SOFT_RST_KEY for enable the SOFT_RST_EN write available. The sequence is: **MOV SOFT_RST_KEY, #AAh** **MOV SOFT_RST_KEY, #55h** **MOV SOFT_RST_KEY, #A5h**								

22.2 Software Reset Enable Register (SOFT_RST_EN)

Table 101 Software Reset Enable Register (SOFT_RST_EN)

SOFT_RST_EN		Address = 1029H				Reset Value = 0x00H		
Software Reset Enable Register								
	SRST_EN	-----	-----	-----	-----	-----	-----	-----
Bit	7	6	5	4	3	2	1	0
Type	W	X	X	X	X	X	X	X
SRST_EN	Software reset enable :							
	0 : Disable Software Reset.							
	1 : Enable Software Reset.							

23. Motor Controller(MOC)

Figure 34 Motor Controller(MOC) Block
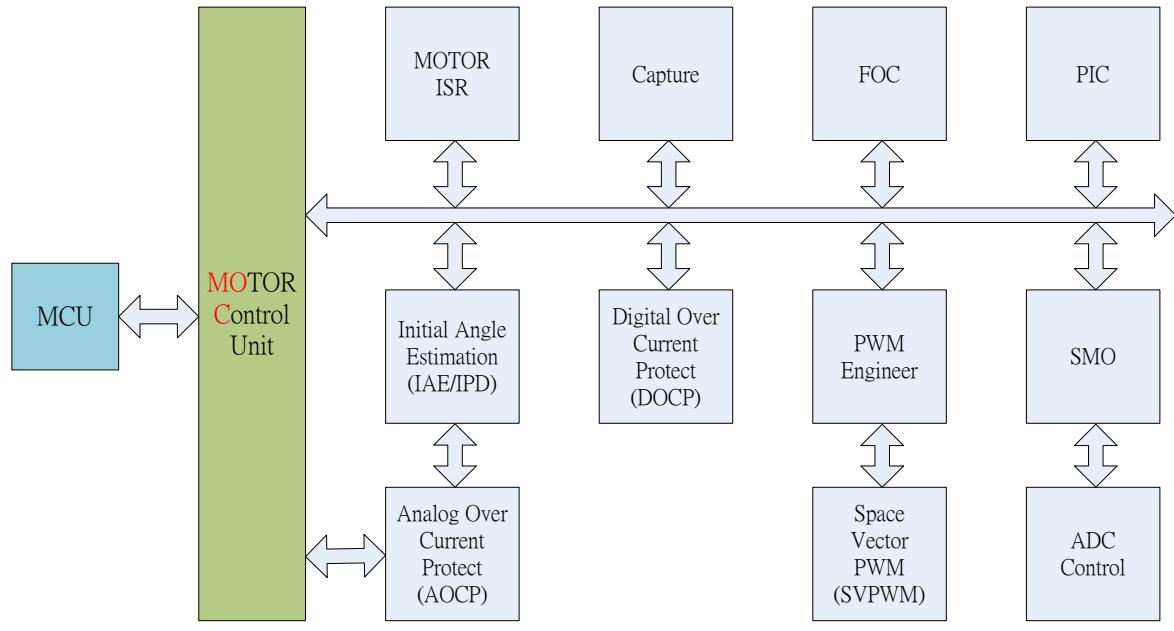
The architecture of Motor Controller Unit

Figure 35 Architecture of Field Oriented Controller Unit
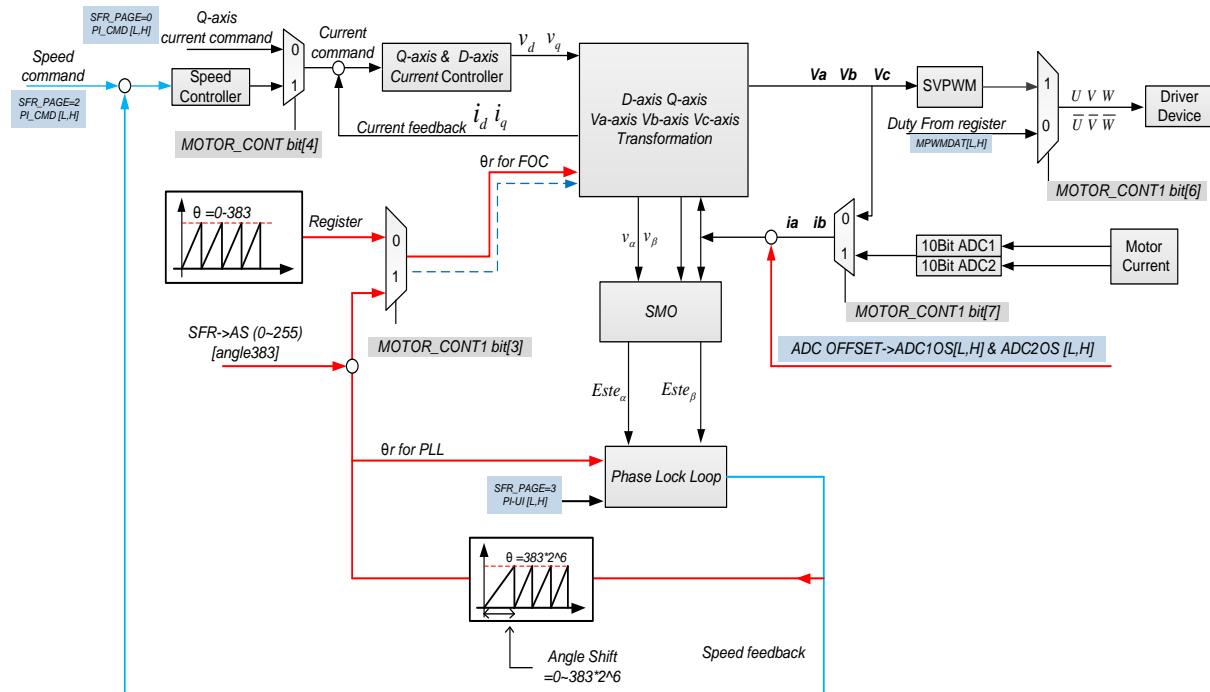
The architecture of Field Oriented Controller Unit

23.1 MOC Engine

Table 102 23.1 MOC Engine

SFR	Type	Description	address	Reset value
MOTOR_CONT1	R/W	Motor Control Register 1	97H	00H
MOTOR_CONT2	R/W	Motor Control Register 2	9FH	A4H
MOTOR_CONT3	R/W	Motor Control Register 3	C6H	00H
FOCCONT	R/W	FOC Control Register	D6H	00H
SP_CYC	W	SPEED Loop Control Cycle	EDH	26H
PI-GAIN	W	PI-Control Gain Register	E6H	F7H
PI-Control Data Register:				
PI_KI_L	R/W	PI-Control KI Data Low byte	91H	00H
PI_KI_H	R/W	PI-Control KI Data High byte	92H	00H
PI_KP_L	R/W	PI-Control KP Data Low byte	93H	00H
PI_KP_H	R/W	PI-Control KP Data High byte	94H	00H
PI_KT_L	W	PI-control KT Data Low byte	DEH	00H
PI_KT_H	W	PI-control KT Data High byte	DFH	00H
PI_TR_L	R/W	PI-control TR Data Low byte	AAH	00H
PI_TR_H	R/W	PI-control TR Data High byte	ABH	00H
PI_MAX_LMT_L	W	PI-Control Maximum Limit Data Low byte	95H	FFH
PI_MAX_LMT_H	W	PI-Control Maximum Limit Data High byte	96H	7FH
PI_MIN_LMT_L	W	PI-Control Minimum Limit Data Low byte	B2H	01H
PI_MIN_LMT_H	W	PI-Control Minimum Limit Data High byte	B3H	80H
PI_CMD_L	R/W	PI- Control Command Data Low byte	A6H	00H
PI_CMD_H	R/W	PI- Control Command Data High byte	A7H	00H
PI_OUT_L	R/W	PI- Control Output Data Low byte	ACH	00H
PI_OUT_H	R/W	PI- Control Output Data High byte	ADH	00H
PI-FB_L	R/W	PI- Control Feedback Data Low byte	AEH	00H
PI-FB_H	R/W	PI- Control Feedback Data High byte	AFH	00H
PI-UI_L	R/W	PI- Control Integral Data Low byte	9DH	00H
PI-UI_H	R/W	PI- Control Integral Data High byte	9EH	00H
PI_TMSR	R/W	PI-control Tracking Mode Select Register	D7H	00H
SMO Control Data Register:				
SMO_D1_L	R/W	SMO Data1 Low byte	BBH	00H
SMO_D1_H	R/W	SMO Data1 High byte	BCH	00H
SMO_D2_L	R/W	SMO Data2 Low byte	BDH	00H
SMO_D2_H	R/W	SMO Data2 High byte	BEH	00H

FOC Control Data Register:					
FOC_D1_L	R/W	FOC Data1 Low byte		D2H	00H
FOC_D1_H	R/W	FOC Data1 High byte		D3H	00H
FOC_D2_L	R/W	FOC Data2 Low byte		D4H	00H
FOC_D2_H	R/W	FOC Data2 High byte		D5H	00H
DC Bus Voltage Correction Control Register:					
VDCCONT	R/W	SMO Data1 Low byte		D8H	00H
General Low Pass Filter Register:					
GEN_LPF_L	R/W	General Low Pass Filter Data Low Byte		A1H	00H
GEN_LPF_H	R/W	General Low Pass Filter Data High Byte		A2H	00H
FG Control Register:					
FGCTRL	R/W	Function Generation Control		1027H	00H

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23.1.1 Motor Control Register (MOTOR_CONT1)

Table 103 23.1.1 Motor Control Register (MOTOR_CONT1)

MOTOR_CONT1			Address = 97H			Reset Value = 0x00H		
Motor Control Register 1								
Bit	SD MODE	MPWM SEL	MPWM EN	IQINS EL	FOC ANGSEL	USER_ PI ACT	GEN_LP F_ACT	SPFB FILTE
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SD_MODE	Clarke input select :	
[7]	0 : From ADC register.	
	1 : From Clarke Transformation output	
MPWMSEL	MPWM duty select :	
[6]	0 : From register	
	1 : From SVPWM register	
MPWMEN	MPWM timer run control enable:	
[5]	0 : Disable	
	1 : Enable	
	MPWMEN =1, ADC CH1 & CH2 Auto Converter:	
IQINSEL	IQ-Control input select:	
[4]	0 : From register	
	1 : From speed PI- control output	
FOCANGSEL	FOC input angle select:	
[3]	0 : From CPU_ANG (Write value of CPU_ANG_H & CPU_ANG_L)	
	1 : From SMO_ANG (Estimated angle)	
	Inverse park transformation input select of angle	
USER_PI_ACT	User PI active	
[2]	0 : disable user PI	
	1 : active user PI	
GEN_LPF_ACT	General Low Pass Filter active	
[1]	1 : LPF Active, Clear by Hardware	
SPFB_FILETER	Speed PI Feedback Filter enable:	
[0]	0 : Disable Filter	
	1 : Enable Filter	

23.1.2 Motor Control Register2 (MOTOR_CONT2)

Table 104 23.1.2 Motor Control Register2 (MOTOR_CONT2)

MOTOR_CONT2			Address = 9FH			Reset Value = 0x00H	
Motor Control Register 2							
	MPWM CPSEN	MPWMCPSTP		SVPWM MODE	SVPWM PS	CPS_LIMI T_EN	IAE SOFEN	CPS_OP SEL
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MPWMCPSEN	Motor PWM Dead Time Compensate Enable:
[7]	0 : Disable -- default
	1 : Enable
MPWMCPSTP	Motor PWM Dead Time Compensate Type: (when SVPWMCPSEN = 1)
[6:5]	00 : Dead time compensate
	01 : Dead time compensate in low amplitude (Default)
	11 : Lowest duty limit is 2xDeadband
SVPWMMODE	SVPWM mode select:
[4]	0 : Continuous (SVPWM) -- default
	1 : Discontinuous (DPWM)
SVPWMPS	SVPWM output phase sequence:
[3]	0 : Positive sequence (A、B、C)
	1 : Negative sequence (B、A、C)
CPS_LIMIT_EN	Dead Time Compensation with Lowest duty limit Enable:
[2]	0 : Dead time compensation without Lowest duty limit
	1 : Dead time compensation + Lowest duty limit (Default)
IAESOFEN	Initial Angle estimation soft start enable:
[1]	0 : Disable
	1 : Enable
CPS_OP_SEL	Dead Time Compensation Signal Operation Select:
[0]	0 : $V\alpha$ and $V\beta$ addition with Compensation factor (Default)
	1 : $V\alpha$ and $V\beta$ subtraction with Compensation factor

23.1.3 Motor Control Register3 (MOTOR_CONT3)

Table 105 23.1.3 Motor Control Register3 (MOTOR_CONT3)

MOTOR_CONT3		Address = C6H					Reset Value = 0x00H
Motor Control Register 3							
	SMO_BIT_ RANGE	SMO_CMP _VALUE	IDQ_FB _SEL		CH3 EN	CH2 EN	---	CPS_LMT_SEL
Bit	7	6	5	4	3	2	1	0
Type			W		W	W		

SMO_BIT_RANGE	SMO bang bang control $Z\alpha$ and $Z\beta$ bit range select:
[7]	0: [29:14]
	1: [30:15]
SMO_CMP_VALUE	SMO bang bang control $I\alpha$ and $I\beta$ compare value select:
[6]	0: compare with MAX_SMC_ERR
	1: compare with 0
IDQ_FB_SEL	Iq, Id feedback value select:
[5:4]	00: Iq/Id direct feedback
	01: two Iq/Id value average
	10: four Iq/Id value average
CH3 EN	CH3 Auto Sample enable:
[3]	0: Disable
	1: Enable
CH2 EN	CH2 Auto Sample enable:
[2]	0: Disable
	1: Enable
CPS_LMT_SEL	Dead time Compensation min duty select:
[0]	0: dead time compensation min duty limit is 2xdeadband
	1: dead time compensation min duty limit is deadband

23.1.4 Field Oriented Control Register (FOCCONT)

Table 106 23.1.4 Field Oriented Control Register (FOCCONT)

FOCCONT		Address = D6H				Reset Value = 0x00H	
Field Oriented Control Register							
Bit	PI CLEAR	ESTCR			INV ADCD	ADC TRIG	PLL EN	SPEED EN
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PICLEAR	Clear register value of PI-Control:
[7]	0: Disable
	1: Enable
ESTCR	Estimation current ration:
[6:4]	000 : Current ValueX1	100 : Current Value/2
	001 : Current ValueX2	101 : Current Value/4
	010 : Current ValueX4	110 : Current Value/8
	011 : Current ValueX8	111 : Current Value/16
INVADCD	Inverse ADC register data:	
[3]	0: Disable	
	1: Enable	
ADCTRIG	ADC Trigger (Phase A and Phase B):	
[2]	0 : PWM counter max	
	1 : PWM counter min	
PLLEN	PLL-Control enable:	
[1]	0: Disable	
	1: Enable	
SPEEDEN	SPEED-Control enable:	
[0]	0: Disable	
	1: Enable	

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23.1.5 PI- Controller GAIN Register (PI_GAIN)

Table 107 23.1.5 PI- Controller GAIN Register (PI_GAIN)

PI_GAIN		Address = E6H				Reset Value = 0xF7H	
PI-Control x16 Gain							
	IQKPG EN	IQKIG EN	IDKPG EN	IDKIG EN	SPKPG EN	SPKIG EN	PLLKP EN	PLLKIG EN
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IQKPGEN	IQ-KP-Gain enable:
[7]	0: Disable
	1: Enable
IQKIGEN	IQ-KI- Gain enable:
[6]	0: Disable
	1: Enable
IDKPGEN	ID-KP- Gain enable:
[5]	0: Disable
	1: Enable
IDKIGEN	ID-KI- Gain enable:
[4]	0: Disable
	1: Enable
SPKPGEN	SPEED-KP- Gain enable:
[3]	0: Disable
	1: Enable
SPKIGEN	SPEED-KI- Gain enable:
[2]	0: Disable
	1: Enable
PLLKPGEN	PLL-KP- Gain enable:
[1]	0: Disable
	1: Enable
PLLKIGEN	PLL-KP- Gain enable:
[0]	0: Disable
	1: Enable

23.1.6 SPEED Loop Control Cycle Register (SP_CYC)

Table 108 23.1.6 SPEED Loop Control Cycle Register (SP_CYC)

SP_CYC			Address = EDH			Reset Value = 0x26H		
SPEED Loop control cycle								
	SP-CYC[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

$$\text{SP-CYC} = \frac{\text{PWM Frequency}}{\text{SPEED Loop Frequency}}$$

23.1.7 PI-Control Data Register

Table 109 23.1.7 PI-Control Data Register

SFR	Description	address	Reset value
PI_TMSR	PI-control Tracking Mode Select Register	D7H	00H
PI_KT_L	PI-control KT Data Low byte	DEH	00H
PI_KT_H	PI-control KT Data High byte	DFH	00H
PI_TMSR	PI-control Tracking Mode Select Register	D7H	00H
PI_MIN_LMT_L	PI-control Minimal Limit Data Low byte	B2H	01H
PI_MIN_LMT_H	PI-control Minimal Limit Data High byte	B3H	80H
PI_TR_L	PI-control TR Data Low byte	AAH	00H
PI_TR_H	PI-control TR Data High byte	ABH	00H
PI_OUT_L	PI-control Output Data Low byte	ACH	00H
PI_OUT_H	PI-control Output Data High byte	ADH	00H
PI_FB_L	PI-control Feedback Data Low byte	AEH	00H
PI_FB_H	PI-control Feedback Data High byte	AFH	00H
PI_CMD_L	PI-control Command Data Low byte	A6H	00H
PI_CMD_H	PI-control Command Data High byte	A7H	00H
PI-UI_L	PI-control Integral Data Low byte	9DH	00H
PI-UI_H	PI-control Integral Data High byte	9EH	00H
PI_KI_L	PI-control KI Data Low byte	91H	00H
PI_KI_H	PI-control KI Data High byte	92H	00H
PI_KP_L	PI-control KP Data Low byte	93H	00H
PI_KP_H	PI-control KP Data High byte	94H	00H
PI_MAX_LMT_L	PI-control Minimal Limit Data Low byte	95H	FFH
PI_MAX_LMT_H	PI-control Minimal Limit Data High byte	96H	7FH

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23.1.7.1 PI-Control KI Data Register

Table 110 23.1.7.1 PI-Control KI Data Register

SFR	Description						
PI_KI_L	PI-Control KI Data Low byte						
PI_KI_H	PI-Control KI Data High byte						

SFR_PAGE	Parameter	Description	Reset Value
SFR_PAGE = 0	IQ_KI	Parameters KI for IQ PI Control	0x0000H
SFR_PAGE = 1	ID_KI	Parameters KI for ID PI Control	0x0000H
SFR_PAGE = 2	SPEED_KI	Parameters KI for SPEED PI Control	0x0000H
SFR_PAGE = 3	PLL_KI	Parameters KI for PLL PI Control	0x09C4H
SFR_PAGE = 4	USER_KI	Parameters KI for USER PI Control	0x0000H

PI_KI_L	Address = 91H	Reset Value = 0x00H					
PI-Control KI Data Low byte							
	PI_KI_L [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI_KI_H	Address = 92H	Reset Value = 0x00H					
PI-Control KI Data High byte							
	PI_KI_H [15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

23.1.7.2 PI-Control KP Data Register

Table 111 **23.1.7.2 PI-Control KP Data Register**

SFR	Description		
PI_KP_L	PI-Control KP Data Low byte		
PI_KP_H	PI-Control KP Data High byte		
SFR_PAGE	**Parameter**	**Description**	**Reset Value**
SFR_PAGE = 0	IQ_KP	Parameters KP for IQ PI Control	0x0000H
SFR_PAGE = 1	ID_KP	Parameters KP for ID PI Control	0x0000H
SFR_PAGE = 2	SPEED_KP	Parameters KP for SPEED PI Control	0x0000H
SFR_PAGE = 3	PLL_KP	Parameters KP for PLL PI Control	0x36B0H
SFR_PAGE = 4	USER_KP	Parameters KP for USER PI Control	0x0000H

PI_KP_L	Address = 93H	Reset Value = 0x00H
PI-Control KP Data Low byte		

	PI_KP_L [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI_KP_H	Address = 94H	Reset Value = 0x00H
PI-Control KP Data High byte		

	PI_KP_H [15:8]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

23.1.7.3 PI-Control KT Data Register

Table 112 **23.1.7.3 PI-Control KT Data Register**

SFR	Description							
PI_KT_L	PI-Control KT Data Low byte							
PI_KT_H	PI-Control KT Data High byte							

SFR_PAGE	Parameter	Description	Reset Value
SFR_PAGE = 0	IQ_KT	Parameters KT for IQ PI Control	0x0000H
SFR_PAGE = 1	ID_KT	Parameters KT for ID PI Control	0x0000H
SFR_PAGE = 2	SPEED_KT	Parameters KT for SPEED PI Control	0x0000H
SFR_PAGE = 3	PLL_KT	Parameters KT for PLL PI Control	0x0000H
SFR_PAGE = 4	USER_KT	Parameters KT for USER PI Control	0x0000H

PI_KT_L	Address = DEH	Reset Value = 0x00H
PI-Control KT Data Low byte		

	PI_KT_L [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI_KT_H	Address = DFH	Reset Value = 0x00H
PI-Control KT Data High byte		

	PI_KT_H [15:8]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

23.1.7.4 PI-Control TR Data Register

Table 113 **23.1.7.4 PI-Control TR Data Register**

SFR	Description						
PI_TR_L	PI-Control TR Data Low byte						
PI_ TR _H	PI-Control TR Data High byte						

SFR_PAGE	Parameter	Description	Reset Value
SFR_PAGE = 0	IQ_TR	Parameters TR for IQ PI Control	0x0000H
SFR_PAGE = 1	ID_ TR	Parameters TR for ID PI Control	0x0000H
SFR_PAGE = 2	SPEED_ TR	Parameters TR for SPEED PI Control	0x0000H
SFR_PAGE = 3	PLL_ TR	Parameters TR for PLL PI Control	0x0000H

PI_ TR _L	Address = AAH	Reset Value = 0x00H					
PI-Control TR Data Low byte							
	PI_ TR _L [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI_ TR _H	Address = ABH	Reset Value = 0x00H					
PI-Control TR Data High byte							
	PI_ TR _H [15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

23.1.7.5 PI-Control Maximum Limit Data Register

Table 114 **23.1.7.5 PI-Control Maximum Limit Data Register**

SFR	Description		
PI_MAX_LMT_L	PI-Control Maximum Limit Data Low byte		
PI_ MAX_LMT _H	PI-Control Maximum Limit Data High byte		
SFR_PAGE	**Parameter**	**Description**	**Reset Value**
SFR_PAGE = 0	IQ_MAX	Maximum Value of IQ PI Control	0x7FFFH
SFR_PAGE = 1	ID_ MAX	Maximum Value of ID PI Control	0x7FFFH
SFR_PAGE = 2	SPEED_MAX	Maximum Value of SPEED PI Control	0x7FFFH
SFR_PAGE = 3	PLL_ MAX	Maximum Value of PLL PI Control	0x7FFFH
SFR_PAGE = 4	USER_ MAX	Maximum Value of USER PI Control	0x0000H

PI_MAX_LMT_L	Address = 95H	Reset Value = 0x00H
PI-Control Maximum Limit Data Low byte		

PI_MAX_LMT_L [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

PI_ MAX_LMT _H	Address = 96H	Reset Value = 0x00H
PI-Control Maximum Limit Data High byte		

PI_ MAX_LMT _H [15:8]							
Bit	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

23.1.7.6 PI-Control Minimum Limit Data Register

Table 115 **23.1.7.6 PI-Control Minimum Limit Data Register**

SFR	Description		
PI_MIN_LMT_L	PI-Control Minimum Limit Data Low byte		
PI_ MIN _LMT _H	PI-Control Minimum Limit Data High byte		
SFR_PAGE	**Parameter**	**Description**	**Reset Value**
SFR_PAGE = 0	IQ_MIN	Minimum Value of IQ PI Control	0x8001H
SFR_PAGE = 1	ID_ MIN	Minimum Value of ID PI Control	0x8001H
SFR_PAGE = 2	SPEED_ MIN	Minimum Value of SPEED PI Control	0x8001H
SFR_PAGE = 3	PLL_ MIN	Minimum Value of PLL PI Control	0x8001H
SFR_PAGE = 4	USER_ MIN	Minimum Value of USER PI Control	0x0000H

PI_MIN_LMT_L		Address = B2H		Reset Value = 0x00H			
PI-Control Minimum Limit Data Low byte							
	PI_MIN_LMT_L [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

PI_ MIN_LMT _H		Address = B3H		Reset Value = 0x00H			
PI-Control Minimum Limit Data High byte							
	PI_ MIN_LMT _H [15:8]						
Bit	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

23.1.7.7 PI-Control Command Data Register

Table 116 **23.1.7.7 PI-Control Command Data Register**

SFR	Description		
PI_CMD_L	PI-Control Command Data Low byte		
PI_CMD_H	PI-Control Command Data High byte		

SFR_PAGE	Parameter	Description	Reset Value
SFR_PAGE = 0	IQ_CMD	Command Value of IQ PI Control	0x0000H
SFR_PAGE = 1	ID_CMD	Command Value of ID PI Control	0x0000H
SFR_PAGE = 2	SPEED_CMD	Command Value of SPEED PI Control	0x0000H
SFR_PAGE = 3	PLL_CMD	Command Value of PLL PI Control	0x0000H
SFR_PAGE = 4	USER_CMD	Command Value of USER PI Control	0x0000H

PI_CMD_L		Address = A6H		Reset Value = 0x00H			
PI-Control Command Data Low byte							
	PI_CMD_L [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI_ CMD _H		Address = A7H		Reset Value = 0x00H			
PI-Control Command Data High byte							
	PI_CMD_H [15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

23.1.7.8   PI-Control Integral Data Register

Table 117 **23.1.7.8   PI-Control Integral Data Register**

SFR	Description						
PI_UI_L	PI-Control Integral Data Low byte						
PI_UI_H	PI-Control Integral Data High byte						

SFR_PAGE	Parameter	Description				Reset Value	
SFR_PAGE = 0	IQ_UI	Integral Data of IQ PI Control				0x0000H	
SFR_PAGE = 1	ID_UI	Integral Data of ID PI Control				0x0000H	
SFR_PAGE = 2	SPEED_UI	Integral Data of SPEED PI Control				0x0000H	
SFR_PAGE = 3	PLL_UI	Integral Data of PLL PI Control				0x0000H	
SFR_PAGE = 4	USER_UI	Integral Data of USER PI Control				0x0000H	

PI_UI_L	Address = 9DH	Reset Value = 0x00H					
PI-Control Integral Data Low byte							

	PI_UI_L [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI_UI_H	Address = 9EH	Reset Value = 0x00H					
PI-Control Integral Data High byte							

	PI_UI_H [15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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23.1.7.9 PI-Control Output Data Register

Table 118 **23.1.7.9 PI-Control Output Data Register**

SFR	Description						
PI_OUT_L	PI-Control Output Data Low byte						
PI_ OUT_H	PI-Control Output Data High byte						

SFR_PAGE	Parameter	Description				Reset Value	
SFR_PAGE = 0	IQ_OUT	Output Data of IQ PI Control				0x0000H	
SFR_PAGE = 1	ID_OUT	Output Data of ID PI Control				0x0000H	
SFR_PAGE = 2	SPEED_OUT	Output Data of SPEED PI Control				0x0000H	
SFR_PAGE = 3	PLL_OUT	Output Data of PLL PI Control				0x0000H	
SFR_PAGE = 4	USER_OUT	Output Data of USER PI Control				0x0000H	

PI_OUT_L	Address = ACH	Reset Value = 0x00H					
PI-Control Output Data Low byte							
	PI_OUT_L [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI_OUT_H	Address = ADH	Reset Value = 0x00H					
PI-Control Output Data High byte							
	PI_OUT_H [15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

23.1.7.10 PI-Control Feedback Data Register

Table 119 **23.1.7.10 PI-Control Feedback Data Register**

SFR	Description						
PI_FB_L	PI-Control Feedback Data Low byte						
PI_ FB_H	PI-Control Feedback Data High byte						

SFR_PAGE	Parameter	Description				Reset Value	
SFR_PAGE = 0	IQ_FB	Feedback Data of IQ PI Control				0x0000H	
SFR_PAGE = 1	ID_FB	Feedback Data of ID PI Control				0x0000H	
SFR_PAGE = 2	SPEED_FB	Feedback Data of SPEED PI Control				0x0000H	
SFR_PAGE = 3	PLL_FB	Feedback Data of PLL PI Control				0x0000H	
SFR_PAGE = 4	USER_FB	Feedback Data of USER PI Control				0x0000H	

PI_FB_L		Address = AEH		Reset Value = 0x00H			
PI-Control Feedback Data Low byte							
	PI_FB_L [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI_FB_H		Address = AFH		Reset Value = 0x00H			
PI-Control Feedback Data High byte							
	PI_FB_H [15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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23.1.7.11 PI Tracking Mode Select Register (PI_TMSR)

Table 120 23.1.7.11 PI Tracking Mode Select Register (PI_TMSR)

PI_TMSR			Address = D7H			Reset Value = 0x00H		
PI Tracking Register								
	IQTM SEL	IQTM EN	IDTM SEL	IDTM EN	SPTM SEL	SPTM EN	PLLTM SEL	PLLTM EN
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IQ TMSEL	IQ-Tracking Mode Select:
[7]	0: Auto Mode
	1: Manual Mode
IQ TMEN	IQ-Tracking Mode Enable:
[6]	0: Disable
	1: Enable
ID TMSEL	ID-Tracking Mode Select:
[5]	0: Auto Mode
	1: Manual Mode
ID TMEN	ID-Tracking Mode Enable:
[4]	0: Disable
	1: Enable
SPEED TMSEL	SPEED-Tracking Mode Select:
[3]	0: Auto Mode
	1: Manual Mode
SPEED TMEN	SPEED -Tracking Mode Enable:
[2]	0: Disable
	1: Enable
PLL TMSEL	PLL-Tracking Mode Select:
[1]	0: Auto Mode
	1: Manual Mode
PLL TMEN	PLL-Tracking Mode Enable:
[0]	0: Disable
	1: Enable

23.1.8 Sliding Mode Observer Data Register

Table 121 23.1.8 Sliding Mode Observer Data Register

SFR	Description		
SMO_D1_L	Sliding Mode Observer Data1 Low byte		
SMO_D1_H	Sliding Mode Observer Data1 High byte		
SFR_PAGE	**Parameters**	**Description**	**Reset Value**
SFR_PAGE = 0	GS	Parameters GS for angle estimation	0x7FFFH
SFR_PAGE = 1	SMO_Gain	Parameters SMO_Gain for angle estimation	0x3E80H
SFR_PAGE = 2	Angle_Base	Parameters Angle_Base for angle estimation	0x0B2FH
SFR_PAGE = 3	Z-Correction	SMO Zgain correction: $Z_{gain} = \frac{Z_{gain} \times Z\text{-Correction}}{32767}$	0x7FFFH
SFR_PAGE = 4	SMO-Angle	Estimated value of SMO angle **(Read Only)**	0x0000H
SFR_PAGE = 5	BanBan-gain	Another Zgain for bang-bang control in SMO	0x7FFFH

SMO_D1_L	Address = BBH	Reset Value = 0x00H

SMO Data1Low Byte

	SMO_D1_L [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SMO_D1_L	Address = BCH	Reset Value = 0x00H

SMO Data1 High Byte

	SMO_D1_H [15:8]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDSF40

SFR	Description							
SMO_D2_L	Sliding Mode Observer Data2Low byte							
SMO_D2_H	Sliding Mode Observer Data2High byte							

SFR_PAGE	Parameters	Description	Reset Value
SFR_PAGE = 0	FS	Parameters FS for angle estimation	0x7FFFH
SFR_PAGE = 1	SMO_Filter	Parameters SMO_Filter for angle estimation	0x0064H
SFR_PAGE = 2	Angle_Shift	Parameters Angle_Shift for angle estimation	0x0000H
SFR_PAGE = 3	MAXSMC_Err	MAXSMC Error Value in Bang Bang Control	0x7FFFH
SFR_PAGE = 4	SPEED	Speed Register **(Read Only)**	0x0000H

SMO_D2_L	Address = BDH	Reset Value = 0x00H
SMO Data2Low Byte		

	SMO_D2_L [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SMO_D2_H	Address = BEH	Reset Value = 0x00H
SMO Data2High Byte		

	SMO_D2_H [15:8]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Kslide_A1 = SMO-gain(Kslide in the page1 of SMO_D1) x MAXSMC_Err(the page3 of SMO_D2)

2. Kslide_A2 = BanBan-gain(the page5 of SMO_D1)

23.1.9 Field Oriented Controller Data Register

Table 122 23.1.9 Field Oriented Controller Data Register

SFR	Description						
FOC_D1_L	Field Oriented Control Data1 Low byte						
FOC_D1_H	Field Oriented Control Data1 High byte						

SFR_PAGE	Parameters	Description				Reset Value	
SFR_PAGE = 0	VDC_Now	The Voltage of DC Bus				0x0000H	
SFR_PAGE = 1	VDC_Normal	The Normalization Voltage of DC Bus				0x0000H	
SFR_PAGE = 2	VDC_Correct	The Correction Voltage of DC Bus **(Read Only)**				0x0000H	

FOC_D1_L	Address = D2H		Reset Value = 0x00H				
FOC Data1Low Byte							

	FOC_D1_L [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FOC_D1_H	Address = D3H		Reset Value = 0x00H				
FOC Data1High Byte							

	FOC_D1_H [15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDSF40

SFR	Description
FOC_D2_L	Field Oriented Control Data2 Low byte
FOC_D2_H	Field Oriented Control Data2 High byte

SFR_PAGE	Parameters	Description	Reset Value
SFR_PAGE = 0	Q-Axis Voltage	Q-Axis Voltage Offset	0x0000H
SFR_PAGE = 1	D-Axis Voltage	D-Axis Voltage Offset	0x0000H
SFR_PAGE = 3	AS	Angle Supplement Data	0x0000H
SFR_PAGE = 4	CPU_ANG	CPU Angle Data Register	0x0000H
SFR_PAGE = 5	FOC-Angle	Park and Inverse Park transformation angle input ※ **Read: Theta for FOC angle.** **Write: Theta offset.**	0x0000H
SFR_PAGE = 6	SVPWM-Amp	Amplitude value of SVPWM transformation	0x4000H

FOC_D2_L	Address = D4H	Reset Value = 0x00H

FOC Data2Low Byte

	FOC_D2_L [7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FOC_D2_H	Address = D5H	Reset Value = 0x00H

FOC Data2High Byte

|	FOC_D2_H [15:8]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 36 Angle Supplement
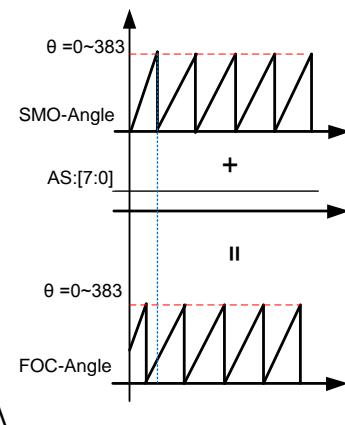
23.1.10 DC BUS Voltage Correction Control Register

Table 123 23.1.10 DC BUS Voltage Correction Control Register

VDCCONT				Address =D8H			Reset Value = 0x00H
VDC Correction control							
		Target_SEL		Type		---	VDC_EN
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	R/W	R/W	R/W	R/W	R/W	R/W
Target_SEL	VDC Target selection (Target_VDC):						
[5:6]	00 : 8191						
	01 : 16383						
	11 : 24574						
Type	VDC Correction Type selection :						
[4]	0 : Vq 、 Vd voltage						
	1 : SVPWM Amplitude						
VDC_EN	VDC Correction enable :						
[0]	0 : Disable.						
	1 : Enable						

Figure 37 DC BUS voltage correction

$$VDC\_Correct = 1 - ADC\ data\ (VDC\_Now)\ X\ \frac{VDC\_Normal}{Target\_VDC}$$
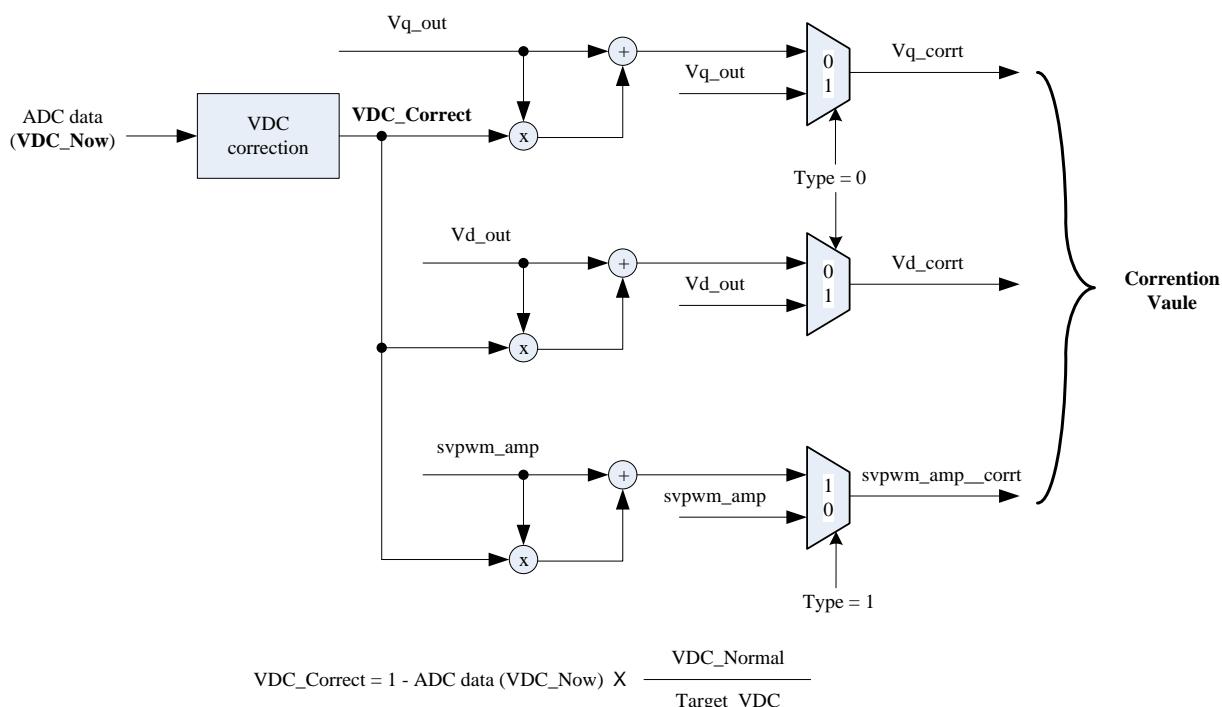
(The VDC_Now and VDC_Normal is accessed from FOC_D1 register)

DC BUS voltage correction

23.2 Motor PWM Engine

Table 124 23.2 MPWM is count up and down timer. (fixed)

SFR	Description	address	Reset value
MPWMCONT1	MPWM Control Register 1.	E3H	00H
MPWMCONT2	MPWM Control Register 2.	E7H	00H
MPWMDB	Motor PWM Dead band Register.	E5H	78H
MPWMINV	MPWM Inverse Selection Register.	E4H	00H
MPWMDATAL	MPWM Data Register Low.	E1H	02H
MPWMDATAH	MPWM Data Register High.	E2H	00H
MPWMCPSF	MPWM Compensate Factor	BFH	00H

23.2.1 MPWM Control Register 1 (MPWMCONT1)

Table 125 Motor PWM output mode select :

MPWMCONT1**(SYNC)**				Address = E3H		Reset Value = 0x00H	
MPWM Control Register							
	-----	HALF SWAP	ALL SWAP	UWXZ SWAP	PWMX_MOD		PWMU_MOD	
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWMU_MOD	Phase U High-side (U) output mode select :
[1:0]	00: Force Low
	01: Force High
	10: Active High
	11: Active Low
PWMX_MOD	Phase U Low-side (X) output mode select :
[3:2]	00: Force Low
	01: Force High
	10: Active High
	11: Active Low
UWXZSWAP	U、W pin swap and X、Z pin swap
[4]	0: Normal
	1: Swap
ALLSWAP	ALL pin swap
[5]	0: Normal
	1: Inverse
HALFSWAP	Half pin swap
[6]	0: Normal
	1: Half change

Figure 38 PWM Pin swap output
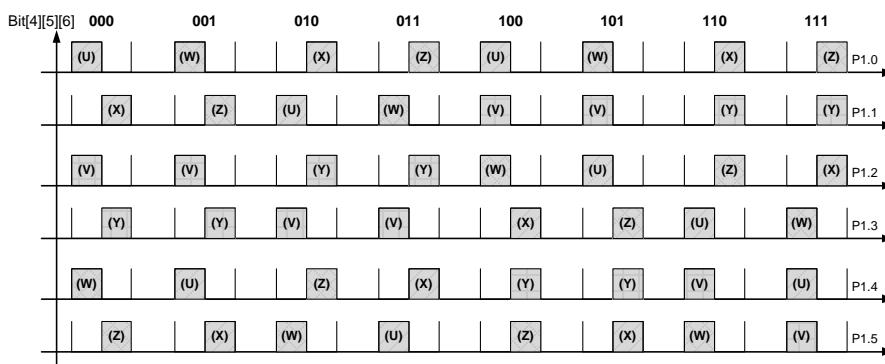
PWM Pin swap output

23.2.2 MPWM Control Register 2 (MPWMCONT2)

Table 126 Motor PWM output mode select

| MPWMCONT2**(SYNC)**			Address = E7H			Reset Value = 0x00H	
MPWM Control Register							
	PWMZ_MOD		PWMW_MOD		PWMY_MOD		PWMV_MOD	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PWMV_MOD	Phase V High-side (V) output mode select :						
[1:0]	00: Force Low						
	01: Force High						
	10: Active High						
	11: Active Low						
PWMY_MOD	Phase V Low-side (Y) output mode select :						
[3:2]	00: Force Low						
	01: Force High						
	10: Active High						
	11: Active Low						
PWMW_MOD	Phase W High-side (W) output mode select :						
[5:4]	00: Force Low						
	01: Force High						
	10: Active High						
	11: Active Low						
PWMZ_MOD	Phase W Low-side (Z) output mode select :						
[7:6]	00: Force Low						
	01: Force High						
	10: Active High						
	11: Active Low						

23.2.3 Motor PWM Dead-band Register (MPWMDB)

Compensation PWM output with Dead-band is use to prevent short-though between high-side and low-side power device.

The frequency of **MPWMDB** is 48MHz. (fixed)

Table 127 Motor PWM Dead-band Register

MPWMDB (SYNC)		Address = E5H			Reset Value = 0x78H		
Motor PWM Dead-band Register							
	MPWMDB[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 39 PWM Output with Dead band

PWM Output with Dead band
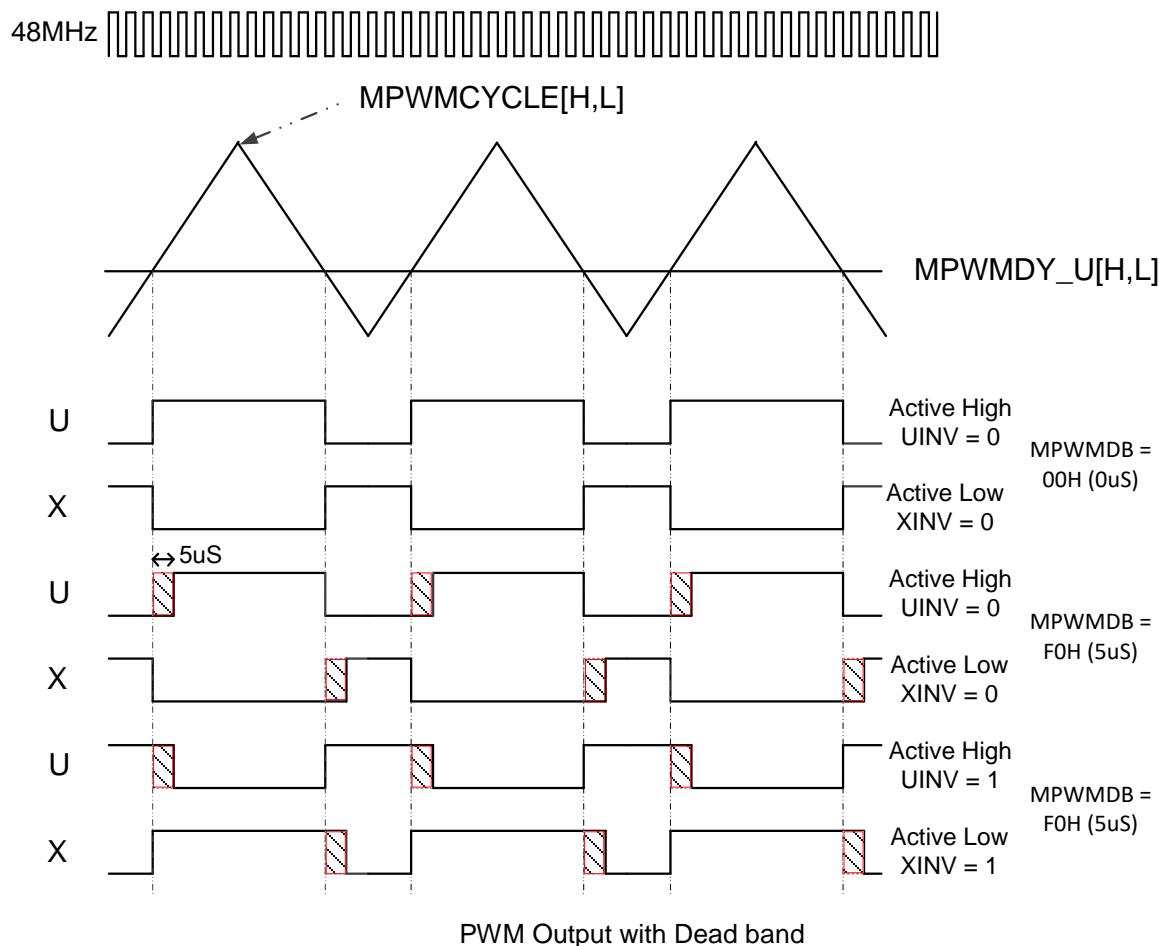
23.2.4 MPWM Inverse Selection Register (MPWMINV)

Motor U,V,W X,Y,Z PWM output Inverse select :

Table 128 Motor U,V,W X,Y,Z PWM output Inverse selection

| MPWMINV (SYNC)				Address = E4H			Reset Value = 0x00H	
MPWM Inverse Selection Register								
	-----	-----	ZINV	WINV	YINV	VINV	XINV	UINV
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W
ZINV	Low-side PWM Z output inverse select :							
[5]	0 : Non-inverse							
	1 : Inverse							
WINV	High-side PWM W output inverse select :							
[4]	0 : Non-inverse							
	1 : Inverse							
YINV	Low-side PWM Y output inverse select :							
[3]	0 : Non-inverse							
	1 : Inverse							
VINV	High-side PWM V output inverse select :							
[2]	0 : Non-inverse							
	1 : Inverse							
XINV	Low-side PWM X output inverse select :							
[1]	0 : Non-inverse							
	1 : Inverse							
UINV	High-side PWM U output inverse select :							
[0]	0 : Non-inverse							
	1 : Inverse							

23.2.5 Motor PWM Data Register (MPWMDATA)

MPWM Cycle :MPWM is 16-bit timer. The frequency of MPWM timer is 48MHz. (fixed)MPWM is count up and down timer. (fixed)

Table 129 Motor PWM Data Register

SFR	Description						
MPWMDATL	MPWM Data Low Byte**(SYNC)**						
MPWMDATH	MPWM Data High Byte**(SYNC)**						
	Parameters		**Description**			**Reset Value**	
SFR_PAGE = 0	MPWM Cycle		Motor PWM cycle value			0x04B0H	
SFR_PAGE = 1	Phase A		Motor PWM Duty value for Phase A			0x0258H	
SFR_PAGE = 2	Phase B		Motor PWM Duty value for Phase B			0x0258H	
SFR_PAGE = 3	Phase C		Motor PWM Duty value for Phase C			0x0258H	
MPWMDATL	Address = E2H		Reset Value = 0x00H				
Motor PWM Data Low Byte							
	MPWMDATL [7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MPWMDATH	Address =E1H		Reset Value = 0x00H				
Motor PWM Data High Byte							
	MPWMDATH [15:8]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 40 PWM counter

PWM counter

MDSF40
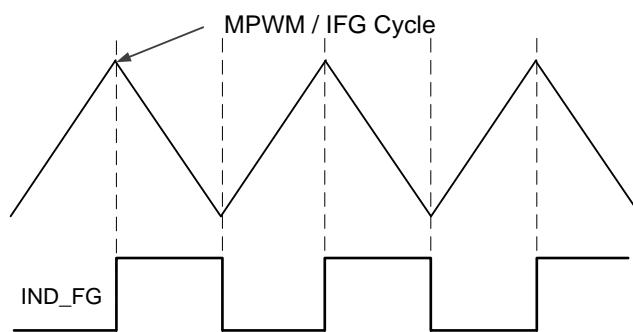
23.2.6 Motor PWM Compensate Factor Register (MPWMCPSF)

Compensation PWM output with Dead-band and PWM frequency ratio that is use to prevent line current distortion when output PWM in very low or high duty.

MPWMCPSFACT is a binary fraction.

Table 130 Motor PWM Compensate Factor Register

MPWMCPSF (SYNC)		Address = BFH			Reset Value = 0x00H		
Motor PWM Compensate Factor Register							
	MPWMCPSFACT[7:0]						
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 41 Motor PWM Compensate Factor Formular

$$MPWMCPSF = \left(\frac{MPWMDB[7:0]}{MPWMCYCLE[15:0]} \times \frac{1}{2}\right)_2$$

ex:

MPWMDB[7:0] = 0x20 = 32

MPWMCYCLE[15:0] = 0x00F0 = 240

MPWMCPSF = 32/480 = 0.06666666...　$\approx$ 0.06640625 = $(.00010001)_2$ = 0x11

23.3 Over Current Protect (OCP)

Table 131 Over Current Protect (OCP) Table

| SFR	Description	address	Reset value
AOCPCONT	Analog Over Current Protect Control Register	EEH	C7H
OCPNCONT	Digital Over Current Protect Control Register	EFH	85H

23.3.1 Analog OCP Control Register (AOCPCONT)

Table 132 Analog OCP Control Register (AOCPCONT)

AOCPCONT		Address = EEH				Reset Value = 0xE7H	
Analog OCP Control Register							
	DOCPNEN	AOCPEN	OPAPD	IPD	----	I_SHORT[3:0]	
Bit	7	6	5	4	3	2	1	0
Type	R	R	----	----	----	R/	R/W	R/W

OCPNEN	Digital OCPN enable:
[7]	0 : Disable
	1 : Enable
AOCPEN	Analog OCP enable:
[6]	0 : Disable
	1 : Enable
OPAPD	OPA Power Down
[5]	0 : Normal
	1 : OPA Power Down
IPD	IPD (Initial Position Detect) Path Select
[4]	0 : IPD Current Compare from AOCP Path
	1 : IPD Current Compare from OPA Path
I_ SHORT	Analog OCP SHORT level select : (OCP interrupt :OCPIF)
[2:0]	000 : 0.15V
	001 : 0.2V
	010 : 0.25V
	011 : 0.3V
	100 : 0.35V
	101 : 0.4V
	110 : 0.45V
	111 : 0.5V(default)

MDSF40

AOCPCONT[4](IPD) signal in MDSF40 for IPD current detect path is come from OP or AOCP: (note: IPD_B = ~IPD)
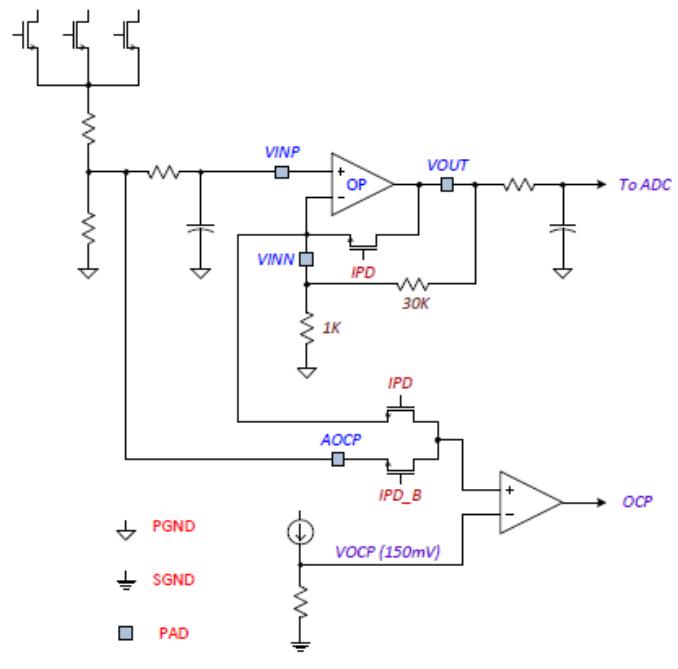
Analog OCP input path select

23.3.2 DOCPN Control Register (DOCPCONT)

Table 133 23.3.2 DOCPN Control Register

OCPNCONT		Address = EFH				Reset Value = 0x85H	
OCPN Control Register							
	OCPST	OCPDBT[4:0]				OCPC	OCPMS
Bit	7	6	5	4	3	2	1	0
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OCPST	OCP Short status :
[7]	0 : No Over current Short
	1 : Over current Short occur. (hardware set OCPC = '0') Six PWM output is high-impedance.
OCPDBT	PIN OCP input de-bounce time (default 41.67nS)
[6:2]	0~31 = 0~1.291uS (48MHz/2 fixed)
OCPC	OCP status clear bit :
[1]	When OCP is occur, hard ware will set OCPC = '0'. In User mode, user can write '1' to clear OCP status, the PWM will output at next PWM cycle.
OCPMS	OCP mode select :
[0]	0 : Auto mode
	1: User mode

Figure 42 Analog OCP and Digital OCP block
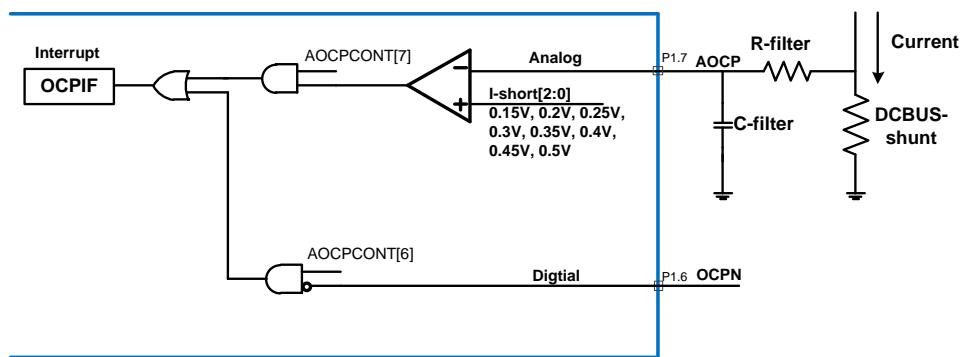
Analog OCP and Digital OCP block

Figure 43 OCP Short occur and PWM out

OCP Short occur and PWM out
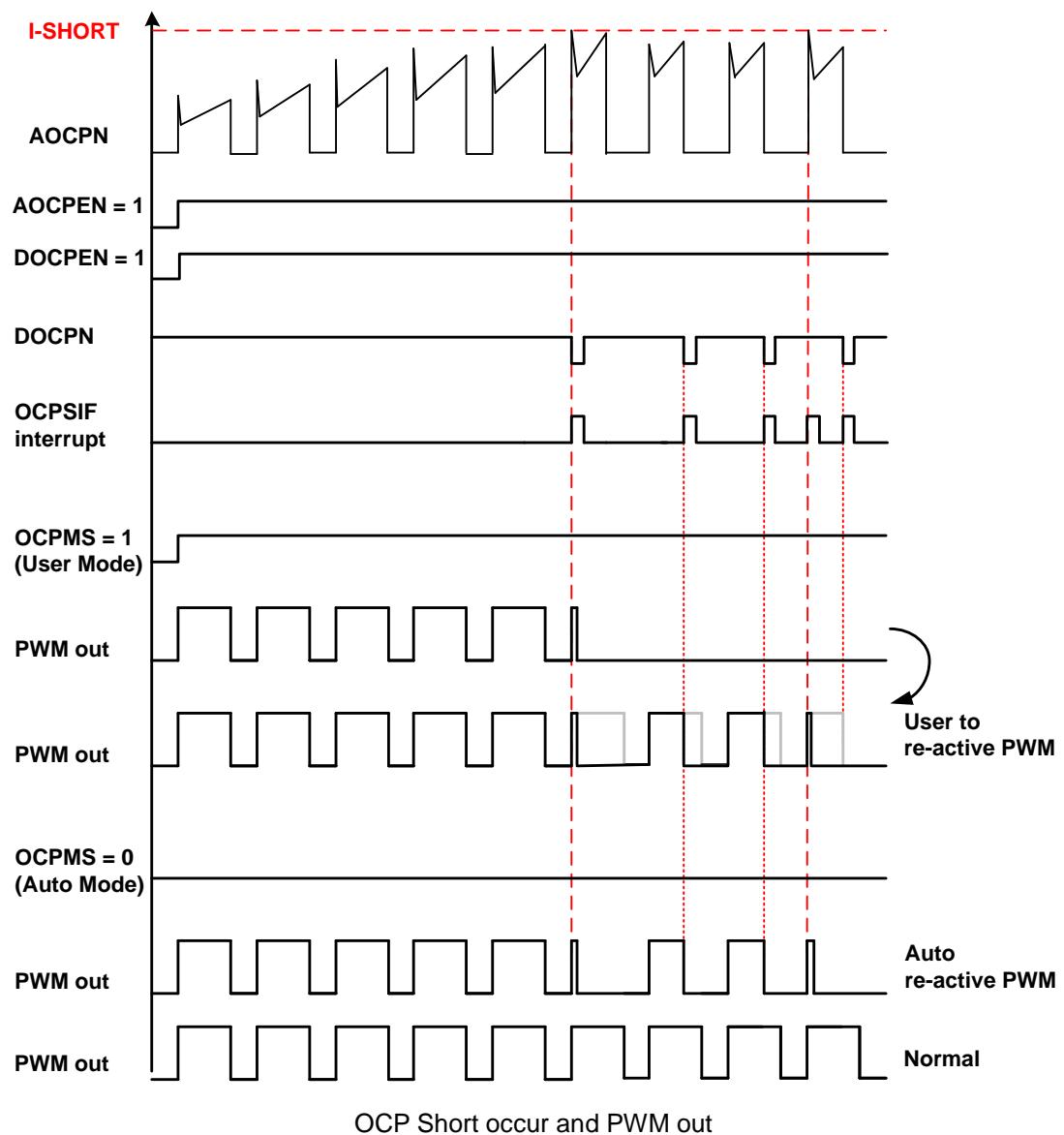
23.4 Initial Angle Estimated Register (IAE)

Table 134 23.4 Initial Angle Estimated Register (IAE)

SFR	Description	address	Reset value
INI_ANG_CTRL	Initial Angle Estimation Control Register	A5H	10H
INI_ANG_DAT	Initial Angle Estimated Data	A4H	EBH

23.4.1 IAE Control Register (INI_ANG_CTRL)

Table 135 23.4.1 IAE Control Register (INI_ANG_CTRL)

INI_ANG_CTRL		Address = A5H			Reset Value = 0x18H		
Initial Angle Control Register							
	IAES	IAEPS			IAEPNS	IAECYC		IAEEN
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R/W	R/W	R/W	R/W

IAES	IAE State:		
[7]	0:Normal		
	1:Busy		
IAEPS	IAE Pattern State:		
[6:4]	001: Pattern1	010: Pattern2	
	011: Pattern3	100: Pattern4	
	101: Pattern5	110: Pattern6	
IAEPNS	IAE Pattern number slate:		
[3]	0: 4 pattern		
	1: 6 pattern		
IAECYC	IAE cycle :		
[2:1]	00: 48MHz	01: 24MHz	
	10: 12MHz	11: 6MHz	
IAEEN	IAE enable:		
[0]	0: Disable		
	1: Enable		

23.4.2 IAE Data Register (INI_ANG_DAT)

Table 136 23.4.2 IAE Data Register (INI_ANG_DAT)

SFR	Description						
INI_ANG_DAT	Initial Angle Estimated Data						
	Parameters		**Description**			**Reset Value**	
SFR_PAGE = 0	Pattern 10		IAE Pattern 1、0			0xEBH	
SFR_PAGE = 1	Pattern 32		IAE Pattern 3、2			0x96H	
SFR_PAGE = 2	Pattern 54		IAE Pattern 5、4			0x7DH	
INI_ANG_DAT	Address = A4H		Reset Value = 0x00H				
	INI_ANG_DAT [7:0]						
	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W
SFR_PAGE = 0	Pattern 1				Pattern 0			
SFR_PAGE = 1	Pattern 3				Pattern 2			
SFR_PAGE = 2	Pattern 5				Pattern 4			
	U、V、W		X、Y、Z		U、V、W		X、Y、Z	
	00 : --		00 : --		00 : --		00 : --	
	01 : U		01 : X		01 : U		01 : X	
	10 : V		10 : Y		10 : V		10 : Y	
	11 : W		11 : Z		11 : W		11 : Z	

Figure 44 IAE states

IAE states
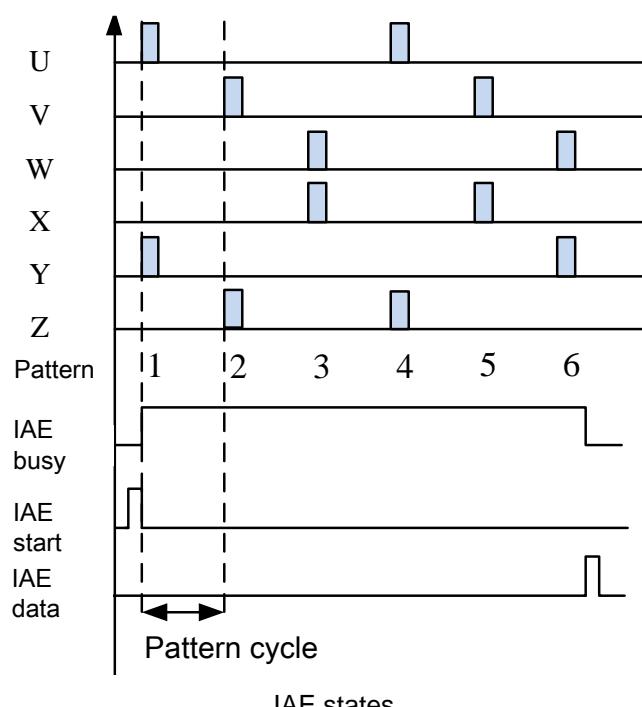
23.5 General Low Pass Filter Register (GEN_LPF)

Table 137 23.5 General Low Pass Filter Register (GEN_LPF)

SFR	Description		
GEN_LPF_L	General Low Pass Filter Data Low Byte		
GEN _LPF_H	General Low Pass Filter Data High Byte		
	Parameters	**Description**	**Reset Value**
SFR_PAGE = 0	GEN_Gain	General LPF Gain (Kslf) parameter	0x0000H
SFR_PAGE = 1	LPF_In	General LPF input data	0x0000H
SFR_PAGE = 2	LPF_Out	General LPF output data	0x0000H
SFR_PAGE = 3	Last_Out	General LPF last output data	0x0000H

GEN_LPF_L	Address = A1H	Reset Value = 0x00H
General Low Pass Filter Data Low Byte		

	GEN_LPF[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

GEN_LPF_H	Address = A2H	Reset Value = 0x00H
General Low Pass Filter Data High Byte		

	GEN_LPF[15:8]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note:

GEN_LPF expression:

*LPF_Out = Last_Out + GEN_Gain x (LPF_In - Last_Out)*

GEN_LPF compute one time when GEN_LPF_ACT = 1 **(MOTOR_CONT1[1])**

23.6 Function Generation Control Register (FGCTRL)

Table 138 23.6 Function Generation Control Register (FGCTRL)

XSFR		Description			address		Reset value
FGCTRL		Function Generation Control			1027H		00H
FGCTRL		Address = 1027H			Reset Value = 0x00H		
FG Control Register							
Bit	FG_EN	---	---	---	---	FGPULSE_SEL		
	7	6	5	4	3	2	1	0
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W
FG_EN	FG output enable:						
[7]	0 : Disable						
	1 : Enable						
FGPULSE_SEL	FG pulse number selection:						
[2:0]	000 : 1 pulses/cycle						
	001 : 2 pulses/cycle						
	010 : 4 pulses/cycle						
	011 : 8 pulses/cycle						
	100 : 12 pulses/cycle						

Figure 45 Pin FG output
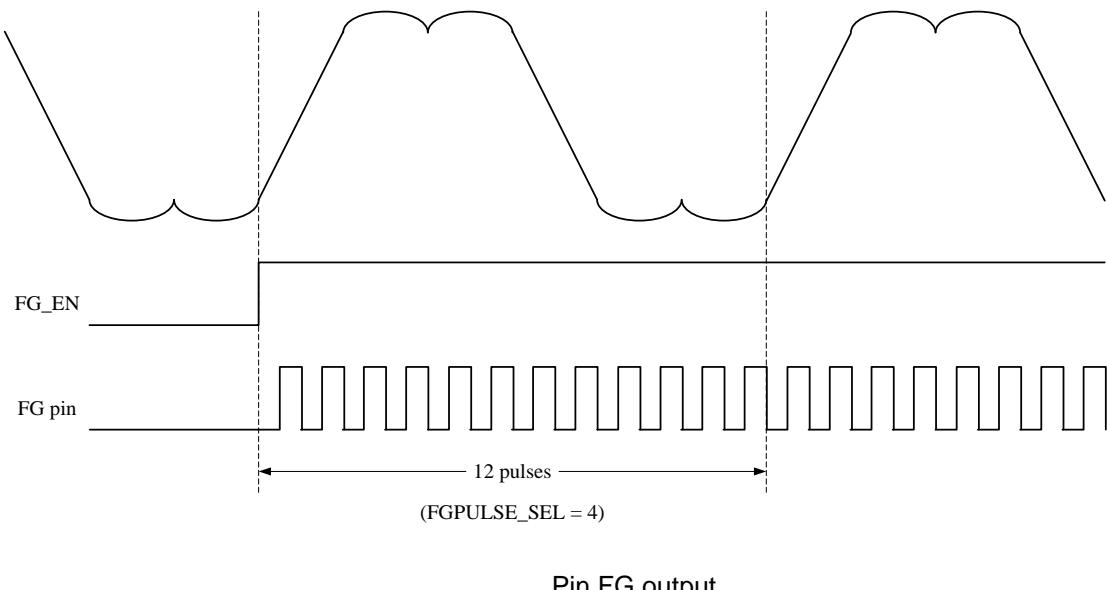
Pin FG output

24. SYNC

MOC behavior is synchronized with **MPWM**, many **MOC** SFRs have **shadow register** that is used to update these SFRs at the same time with **SYNC** register. Write **SYNC** any value will synchronization update these SFRs at the same time.

Table 139 MOC Sync Register

SYNC				Address = 8FH		Reset Value = 00000000B		
MOC Sync Register								
	SYNC[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

Write only.

Table 140 **Shadow register**: (need **SYNC**)

1. MPWMCONT
2. MPWMDB
3. MPWMINV
4. MPWMDATAL
5. MPWMDATAH
6. CPU_ANG_L
7. CPU_ANG_H
8. VDQ_OFST_L
9. VDQ_OFST_H
10. SVPWMAMP

25. Typical Application Circuit

Figure 46 Typical Application Circuit
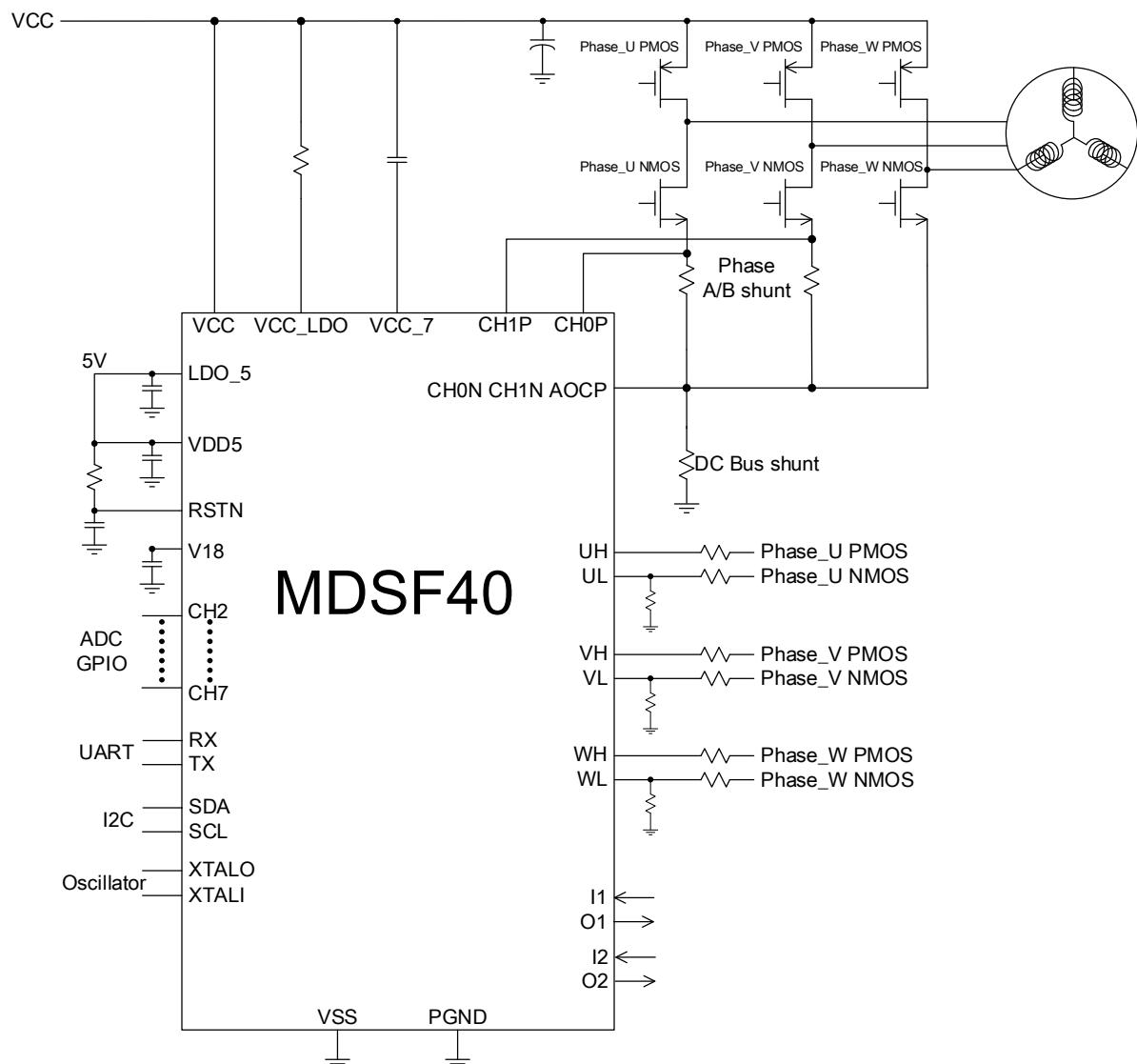
26. Package Information

26.1 LQFP48 7x7mm(AA2) Outline Dimensions

Figure 47 LQFP48 7x7mm
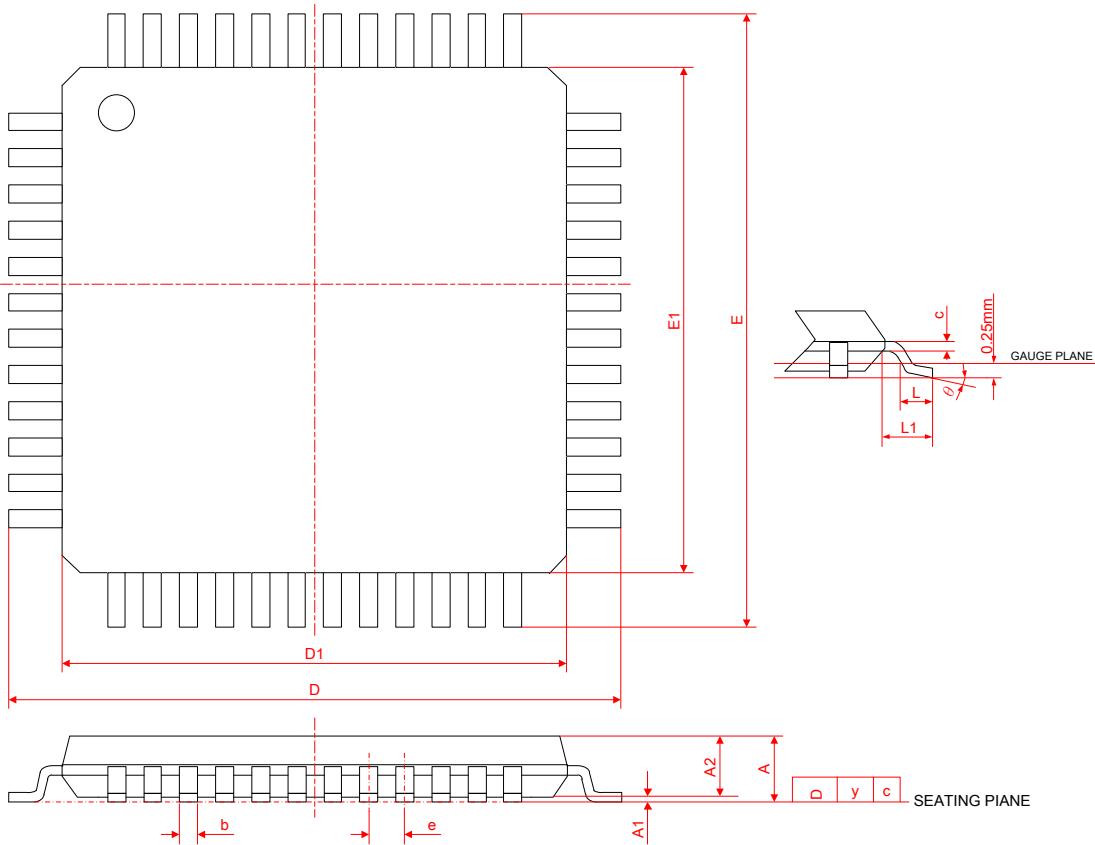
Symbol	Dimension (mm)			Dimension (mil)		
	Min.	**Nor.**	**Max.**	**Min.**	**Nor.**	**Max.**
A	—	—	1.60	—	—	63.0
A1	0.05	—	0.15	2.0	—	6.0
A2	1.35	1.40	1.45	53.0	55.0	57.0
b	0.17	0.22	0.27	6.7	8.7	10.6
c	0.178 TYP			7.0 TYP		
e	0.50 BSC			19.7 BSC		
D	8.90	9.00	9.10	350.0	354.0	358.0
D1	6.90	7.00	7.10	272.0	276.0	280.0
E	8.90	9.00	9.10	350.0	354.0	358.0
E1	6.90	7.00	7.10	272.0	276.0	280.0
L	0.50	0.60	0.70	20.0	24.0	28.0
L1	1.00 REF			1.00 REF		
y	—	—	0.10	—	—	3.9
θ	0°	3.5°	7.0°	0°	3.5°	7.0°

27. Revision History

Table 141 Revision History

Update Date	Version	Modify content
2022/08/23	V0.2	1. MDSF40 Initial 2. Modify Standard Product Name.