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MDRHA0

8Bit Single-Chip Microcontroller

Embedded 100V 3-Phase Gate-Driver

Data sheet

V0.1 2020-11

Microcontrollers

Description

MDRHA0 is a highly integrated motor drive controller. It is composed of BLDC motor MCU and 100V 3-phase gate-driver that suit for under DC 80V motor system, for example household fan water pump、telecom fan…etc.

1. Features

Motor Controller (MOC)

- Space Vector PWM (SVPWM)
- Supports Sin-Wave and Square-Wave Solutions
- Supports Hall Latch Input
- Supports Digital OCP and Analog OCP (Over Current Protection)
- Programmable Dead Band
- Programmable Angle Shift Control (-58° to 58° in 64steps)

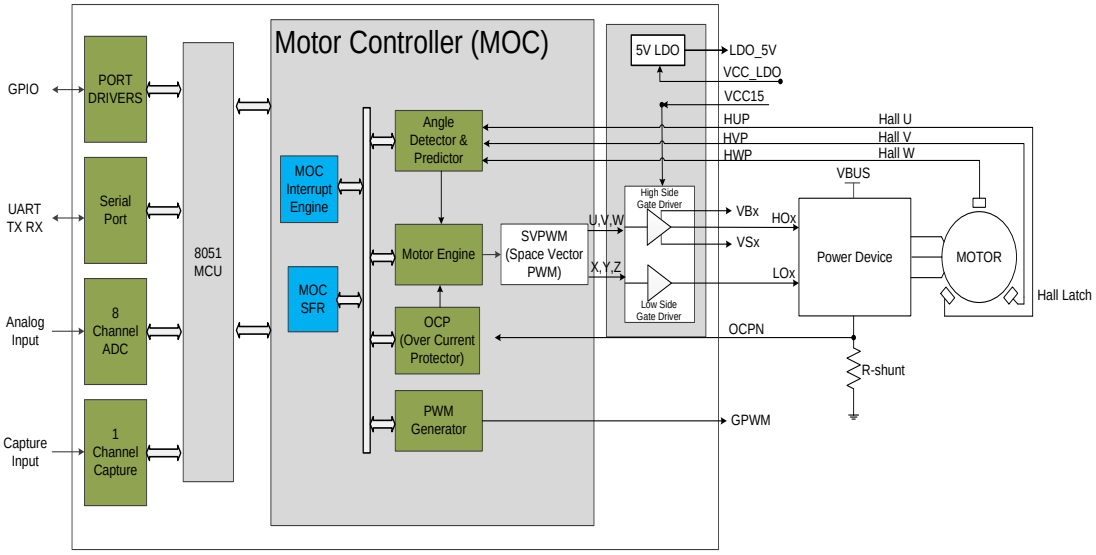
Gate Driver

- Integrated 100V 3-phase Gate-driver
- Built-in 15V/5V 30mA LDO
- Shoot-through protection
- Under voltage lockout for VCC15 and VBS

Embedded MCU

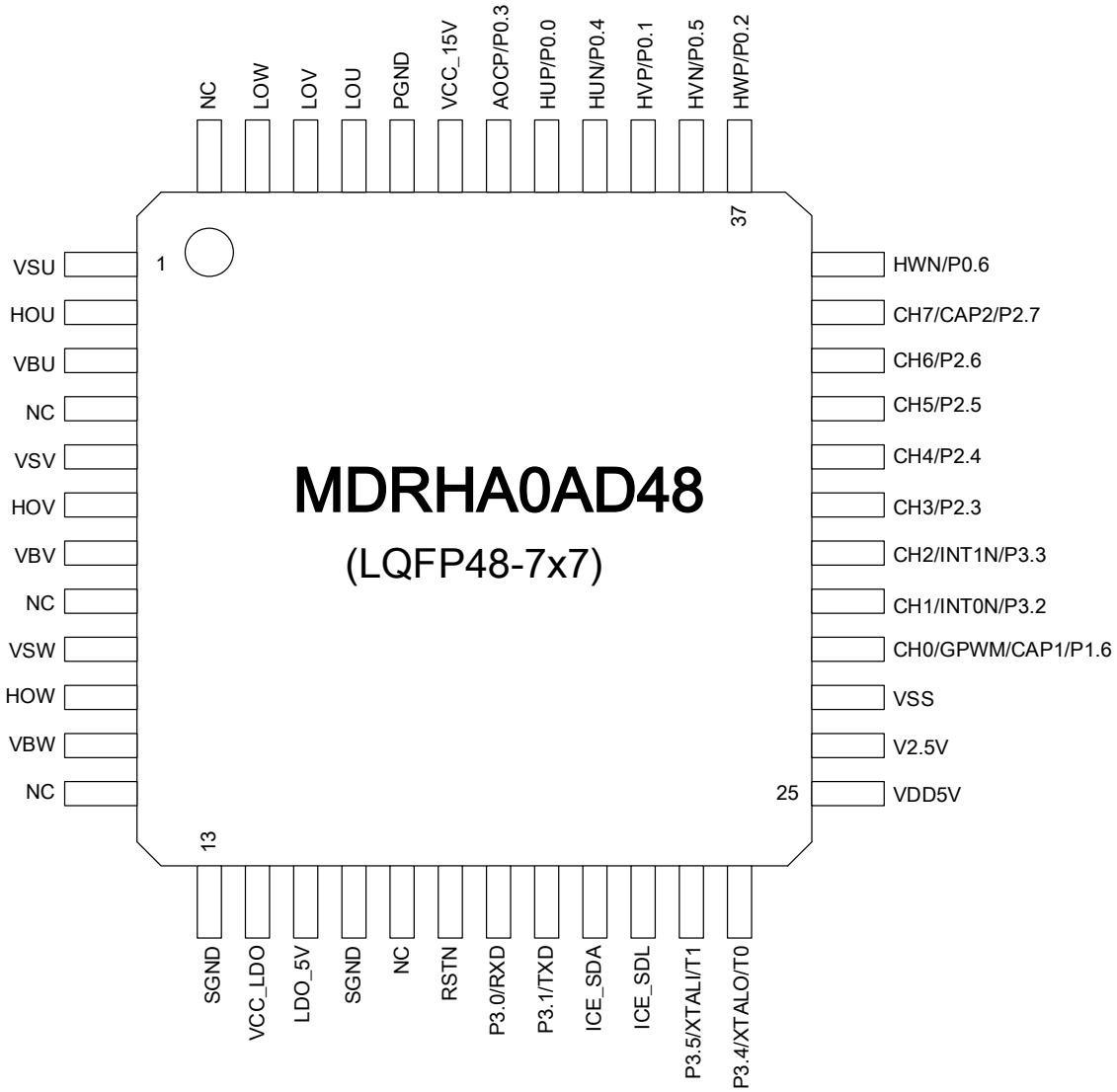
- MCS®-51 Compatible
- 1T 8052 Central Processing Unit
- 4.5V to 5.5V Operation Range
- 4 Level Priority Interrupt
- 13 Interrupt Sources
- 1 External Interrupts (INT1N)
- Memory Size:
- 8KB Flash Program Memory
- 256 x 8-bit IRAM
- 256 x 8-bit XRAM
- Up to 12 General-Purpose Input / Output (GPIO) Pins
- Three 16-bit Timer/Counters
- Watchdog (WD) Timer
- 1-Channel 16-bit Capture
- 8-Channel 10-bit Analog-to-Digital Converter (ADC)
- Full Duplex UART Serial Channel
- Fast Multiplication-Division Unit (MDU): 16*16,32/16, 16/16, 32-bit L/R shifting and 32-bit normalization

2. Block Diagram



3. Pin Assignments

LQFP48 7x7(AA2)



4. Pin Definitions

Pin # LQFP7x7-48	Name	Type	Description
1	VSU		High-side driver U-phase floating supply offset voltage
2	HOU	HVO	High-side driver U-phase gate driver output
3	VBU		High-side driver U-phase floating supply
5	VSV		High-side driver V-phase floating supply offset voltage
6	HOV	HVO	High-side driver V-phase gate driver output
7	VBV		High-side driver V-phase floating supply
9	VSW		High-side driver W-phase floating supply offset voltage
10	HOW	HVO	High-side driver W-phase gate driver output
11	VBW		High-side driver W-phase floating supply
13	SGND	Ground	Logic ground.
14	VCC_LDO	Power	15V to 5V LDO power supply voltage
15	LDO_5V	Power	15V to 5V LDO power output，Max Current Output 30mA
16	SGND	Ground	Gate drivers Signal ground
18	RSTN	I	System Reset.
19	RX	I	Serial Data Transmit (UART)
	P3.0	I/O	Bit 0 of Port 3.
20	TX	O	Serial Data Receive (UART)
	P3.1	I/O	Bit 1 of Port 3.
21	SDA_{ICE}		For ICE(In Circuit Emulator).
22	SCL_{ICE}		For ICE(In Circuit Emulator).
23	XTALI	I	Crystal input pin. **Connect the crystal 12MHz between this pin and XTALO and a 22pF capacitor to VSS.**
	T1	I	TIMER1 External Input.
	P3.5	I/O	Bit 5 of Port 3.
24	XTALO	O	Crystal output pin. **Connect the crystal 12MHz between this pin and XTALI and a 22pF capacitor to VSS.**
	T0	I	TIMER0 External Input.
	P3.4	I/O	Bit 4 of Port 3.

25	VDD5	Power	5.0V Voltage Input. **A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS.**
26	V25	O	2.5V Voltage Output. A 0.1uF and 1uF (minimum) capacitor should be connected between this pin and VSS.
27	VSS	Ground	Logic ground.
28	CH0	I	Analog Input Ch0.
	CAP1	I	Capture Input 1
	GPWM	O	General PWM output.
	P1.6	I/O	Bit 6 of Port 1.
29	CH1	I	Analog Input Ch1.
	INT0N	I	External Interrupt 0. Low level trigger or falling edge trigger.
	P3.2	I/O	Bit 2 of Port 3.
30	CH2	I	Analog Input Ch2.
	INT1N	I	External Interrupt 1. Low level trigger or falling edge trigger.
	P3.3	I/O	Bit 3 of Port 3.
31	CH3	I	Analog Input Ch3.
	P2.3	I/O	Bit 3 of Port 2.
32	CH4	I	Analog Input Ch4.
	P2.4	I/O	Bit 4 of Port 2.
33	CH5	I	Analog Input Ch5.
	P2.5	I/O	Bit 5 of Port 2.
34	CH6	I	Analog Input Ch6.
	P2.6	I/O	Bit 6 of Port 2.
35	CH7	I	Analog Input Ch7.
	CAP2	I	Capture Input 2
	P2.7	I/O	Bit 7 of Port 2.
36	HWN	I	Hall Element negative input. (HALL W)
	P0.6	I/O	Bit 6 of Port 0.
37	HWP	I	Hall Latch input or HALL Element positive input. (HALL W)
	P0.2	I/O	Bit 2 of Port 0.

38	HVN	I	Hall Element negative input. (HALL V)
	P0.5	I/O	Bit 5 of Port 0.
39	HVP	I	Hall Latch input or HALL Element positive input. (HALL V)
	P0.1	I/O	Bit 1 of Port 0.
40	HUN	I	Hall Element negative input. (HALL U)
	P0.4	I/O	Bit 4 of Port 0.
41	HUP	I	Hall Latch input or HALL Element positive input.(HALL U)
	P0.0	I/O	Bit 0 of Port 0.
42	OCPN	I	Over current protection. Active-low.
	P0.3	I/O	Bit 3 of Port 0.
43	VCC15	Power	Logic and low-side gate drivers power supply voltage
44	PGND	Ground	Low-side gate drivers ground
45	LOU	O	Low-side gate driver U-phase output
46	LOV	O	Low-side gate driver V-phase output
47	LOW	O	Low-side gate driver W-phase output
4,8,12,17,48	NC		No connect.

5. Absolute Maximum Ratings

VDD5 Supply Voltage……V_{SS}-0.3V to V_{SS}+6.0V
VDD5 Input Voltage……...V_{SS}-0.3V to V_{DD5}+0.3V
VCC15 Supply Voltage……-0.3V to 118V
V_B High Side floating supply Voltage…….. -0.3V to 100V
V_S High Side offset Voltage…….. -3V to V_B+0.3V
V_{HO} High Side gate-driver output Voltage…….. Vs-3V to V_B+0.3V
V_{LO} Low Side gate-driver output Voltage……PGND-0.3V to VB+0.3V
Storage Temperature……-50℃ to 150℃
Operating Temperature……-40℃ to 125℃
I_{OH} Total……-80mA
I_{OL} Total……80mA
Total Power Dissipation……500mW
Electrostatic Discharge Capability – Human Body Mode……2000V
Electrostatic Discharge Capability – Machine Mode……200V

6. D.C. Characteristics

Ta=25℃

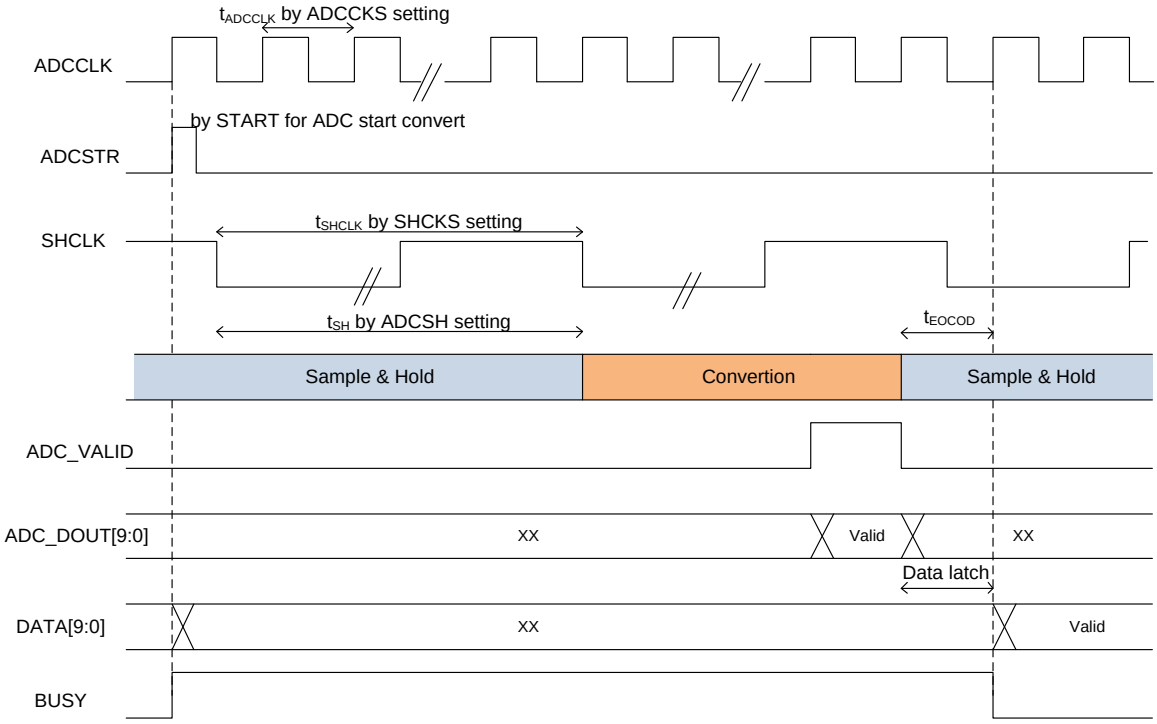
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V	Conditions				
VCC15	Low side supply voltage	—	—	5.5	—	18	V
$V_{B.U.V.W}$	High side floating supply voltage	—	—	V_S+5.5	—	V_S+18	V
$V_{S.U.V.W}$	High side offset voltage	—	—	-1	—	100	V
$V_{HO.U.V.W}$	High side gate driver output voltage			V_S		V_B	V
$V_{LO.U.V.W}$	Low side gate driver output voltage			PGND		VCC	V
V_{25}	V_{25} Output Range	—	Load Current < 10mA	2.35	2.50	2.65	V
I_{VCC}	Operating Current	Vcc	No load, fsys=48Mhz,ADC off, MOC off	—	8	10	mA
V_{IL}	Input Low Voltage for I/O Ports.	—	—	0	—	1	V
V_{IH}	Input High Voltage for I/O Ports.	—	—	2	—	VDD5	V
V_{OL}	Output Low Voltage for I/O Ports.	VDD5	I_{OL}=5mA	—	—	0.5	V
V_{OH}	Output High Voltage for I/O Ports.	VDD5	I_{OH}=-3.8mA	4.5	—	—	V
R_{PU}	Pull-up Resistance for I/O Ports	VDD5	—	10	35	50	KΩ
R_{PD}	Pull-down Resistance for I/O Ports	VDD5	—	10	35	50	KΩ

7. A.C. Characteristics

Ta=25℃

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD5	Conditions				
f_{SYS}	System Frequency	4.5V~5.5V	Ta=-40℃ to 125℃	TBD	48.0	TBD	MHz
			Ta=-20℃ to 85℃	TBD	48.0	TBD	MHz
			Ta=25℃	-1%	48.0	+1%	MHz
f_{TIMER}	Timer Input Pin Frequency	—	—	—	—	4	fsys
t_{INT}	Interrupt Pulse Width	—	—	1	5	10	tsys
t_{LVD}	Low Voltage Width to interrupt	—	—	120	240	480	us
t_{V25}	V_{25} Stable Time	—	—	60	120	240	us
t_{RSDT}	System Reset Delay Time(Power On Reset)	—	—	25	50	100	ms

8. A/D Converter Characteristics



Ta=25℃

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD5	Conditions				
I_{AD}	Additional Power Consumption if A/D Converter is Used	5V	—	—	4.5	—	mA
I_{ADSTB}	A/D Converter Standby Current	—	Load Current < 10mA	—	—	4	uA
t_{ADCCLK}	A/D Converter Clock Time	—	4MHz	—	0.25	—	us
		—	2MHz	—	0.5	—	us
t_{CONV}	A/D Conversion Time	—	4MHz	—	3.25	—	us
		—	2MHz	—	6.5	—	us
t_{SHCLK}	A/D Sample and Hold Clock Time	—	1MHz	—	1	—	us
		—	500KHz	—	2	—	us
		—	400KHz	—	2.5	—	us
		—	333KHz	—	3	—	us
t_{SH}	A/D Sample and Hold Time	—	1MHz	1	—	2	us
		—	500KHz	2	—	4	us
		—	400KHz	2.5	—	5	us
		—	333KHz	3	—	6	us

DNL	Differential Non-linearity	4.5V	No load, t_{CONV}=2.5us	-1	—	+3	LSB
		5.5V		-1	—	+3	LSB
		4.5V	No load, t_{CONV}=5us	-1	—	+3	LSB
		5.5V		-1	—	+3	LSB
INL	Integral Non-linearity	4.5V	No load, t_{CONV}=2.5us	-4	—	+4	LSB
		5.5V		-4	—	+4	LSB
		4.5V	No load, t_{CONV}=5us	-4	—	+4	LSB
		5.5V		-4	—	+4	LSB
G_{ERR}	Gain Error	—	—	-10	—	+10	LSB

9. Special Function Registers (SFR)

9.1 SFRs Memory Map

	8	9	A	B	C	D	E	F	
F8	PINCONG1	PINCONG2	PINCONG3	PINCONG4	PINCONG5	PINCONG6	RSTS	TAKEY	FF
F0	B	PINSET1	PINSET2	PINSET3	PINSET4	PINSET5	PINSET6	PINSET7	F7
E8	ASUD1_1	ASUD1_2	ASUD1_3	ASUD1_4	ASUD2_1	ASUD2_2	ASUD2_3	ASUD2_4	EF
E0	ACC	AS_MD_CONT	MD0	MD1	MD2	MD3	MD4	MD5	E7
D8	CAPCONT	VRHALL	SVPWMAMPFT	MD_CONT	ASUR1	ASUR2	ASUR3	ASUR4	DF
D0	PSW	PFCON	ADCCONT	ADCSTR	-----	ADCD1	ADCD2	SYNC	D7
C8	T2CON	CAPT_H	CAPT_L	CAPH_H	CAPH_L	-----	-----	-----	CF
C0	IRCON1	SVPWMANG	-----	SVPWMAMPL	SVPWMAMPH	-----	-----	-----	C7
B8	IEN1	IP1	GPWMCONT	GPWMMAXL	GPWMMAXH	GPWMDYL	GPWMDYH	-----	BF
B0	P3	MPWMCONT1	MPWMCONT2	MPWMINV	TL2	TH2	WDTC	WDTK	B7
A8	IEN0	IP0	MPWMDYVL	MPWMDYVH	-----	MPWMDYWL	MPWMDYWH	-----	AF
A0	P2	OCPCONT	MCONT2	MPWMMAXL	MPWMMAXH	MPWMDYUL	MPWMDYUH	MPWMDB	A7
98	SCON	SBUF	SRELL	SRELH	HALLDBT	MCONT1	AOCPCONT	-----	9F
90	P1	HALLSET1	HALLSET2	HALLSET3	HALLST	-----	ROTORSPEEDL	ROTORSPEEDH	97
88	TCON	TMOD	TL0	TL1	TH0	TH1	AUX	AS	8F
80	P0	SP	DP0L	DP0H	DP1L	DP1H	RCON	PCON	87
	0	1	2	3	4	5	6	7	

9.2 MDRHA0 SFRs and Reset Value

SYMBOL	DESCRIPTION	DIRECT ADDRESS	RESET VALUE
ACC	Accumulator	E0H	00H
ADCCONT	ADC Control Register	D2H	80H
ADCD1	ADC Data Register 1	D5H	00H
ADCD2	ADC Data Register 2	D6H	00H
ADCSTR	ADC Start Convert and Setting Register	D3H	00H
AOCPCONT	Analog OCP Control Register	9EH	0FH
AS	Angle Shift Control Register	8FH	00H
AS_MD_CONT	ASU and MDU Control Register	E1H	10H
ASUD1_1	ASU Data 1 byte 1	E8H	00H
ASUD1_2	ASU Data 1 byte 2	E9H	00H
ASUD1_3	ASU Data 1 byte 3	EAH	00H
ASUD1_4	ASU Data 1 byte 4	EBH	00H
ASUD2_1	ASU Data 2 byte 1	ECH	00H
ASUD2_2	ASU Data 2 byte 2	EDH	00H
ASUD2_3	ASU Data 2 byte 3	EEH	00H
ASUD2_4	ASU Data 2 byte 4	EFH	00H
ASUR1	ASU Result Register 1	DCH	00H
ASUR2	ASU Result Register 2	DDH	00H
ASUR3	ASU Result Register 3	DEH	00H
ASUR4	ASU Result Register 4	DFH	00H
AUX	Auxiliary	8EH	11H
B	B Register	F0H	00H
CAPCONT	Capture Control Register	D8H	03H
CAPH_H	Capture High-level Count High	CBH	00H
CAPH_L	Capture High-level Count Low	CCH	00H
CAPT_H	Capture Total Count High	C9H	00H
CAPT_L	Capture Total Count Low	CAH	00H
DPTR0:	Data Pointer (2 bytes)		
DP0H	Data Pointer 0 High	83H	00H
DP0L	Data Pointer 0 Low	82H	00H
DPTR1:	Data Pointer 1 (2 bytes)		
DP1H	Data Pointer 1 High	85H	00H
DP1L	Data Pointer 1 Low	84H	00H
GPWMCONT	General PWM Control Register	BAH	00H

GPWMDYH	General PWM Duty Register High	BEH	FFH
GPWMDYL	General PWM Duty Register Low	BDH	FFH
GPWMMAXH	General PWM Max Register High	BCH	00H
GPWMMAXL	General PWM Max Register Low	BBH	02H
HALLDBT	Hall De-bounce Time Register	9CH	0EH
HALLSET1	Hall Setting Register 1	91H	45H
HALLSET2	Hall Setting Register 2	92H	26H
HALLSET3	Hall Setting Register 3	93H	13H
HALLST	Hall Status Register	94H	XXH
IEN0	Interrupt Enable Register 0	A8H	00H
IEN1	Interrupt Enable Register 1	B8H	00H
IP0	Interrupt Priority Register 0	A9H	00H
IP1	Interrupt Priority Register 1	B9H	00H
IRCON1	Interrupt Request Register 1	C0H	00H
MCONT1	Motor Control Register 1	9DH	X011 0000B
MCONT2	Motor Control Register 2	A2H	00H
MD_CONT	MDU Control Register	DBH	00H
MD0	Multiplication Division Register 0	E2H	00H
MD1	Multiplication Division Register 1	E3H	00H
MD2	Multiplication Division Register 2	E4H	00H
MD3	Multiplication Division Register 3	E5H	00H
MD4	Multiplication Division Register 4	E6H	00H
MD5	Multiplication Division Register 5	E7H	00H
MPWMCONT1	MPWM Control Register 1	B1H	00H
MPWMCONT2	MPWM Control Register 2	B2H	00H
MPWMDB	Motor PWM Deadband Register	A7H	00H
MPWMDYUH	Motor PWM Duty Register U High (Phase U)	A6H	07H
MPWMDYUL	Motor PWM Duty Register U Low (Phase U)	A5H	FFH
MPWMDYVH	Motor PWM Duty Register V High (Phase V)	ABH	07H
MPWMDYVL	Motor PWM Duty Register V Low (Phase V)	AAH	FFH
MPWMDYWH	Motor PWM Duty Register W High (Phase W)	AEH	07H
MPWMDYWL	Motor PWM Duty Register W Low (Phase W)	ADH	FFH
MPWMINV	MPWM Inverse Selection Register	B3H	00H
MPWMMAXH	Motor PWM Max Register High	A4H	00H
MPWMMAXL	Motor PWM Max Register Low	A3H	02H
OCPCONT	OCP Control Register	A1H	04H

P0	Port 0	80H	FFH
P1	Port 1	90H	FFH
P2	Port 2	A0H	FFH
P3	Port 3	B0H	FFH
PCON	Power Control Register	87H	00H
PFCON	Peripheral Frequency Control Register	D1H	00H
PINCONG1	Pin Configure Register 1	F8H	AAH
PINCONG2	Pin Configure Register 2	F9H	AAH
PINCONG3	Pin Configure Register 3	FAH	A0H
PINCONG4	Pin Configure Register 4	FBH	AAH
PINCONG5	Pin Configure Register 5	FCH	AAH
PINCONG6	Pin Configure Register 6	FDH	A0H
PINSET1	Pin I/O Setting Register 1	F1H	AAH
PINSET2	Pin I/O Setting Register 2	F2H	AAH
PINSET3	Pin I/O Setting Register 3	F3H	0AH
PINSET4	Pin I/O Setting Register 4	F4H	00H
PINSET5	Pin I/O Setting Register 5	F5H	80H
PINSET6	Pin I/O Setting Register 6	F6H	2AH
PINSET7	Pin I/O Setting Register 7	F7H	FFH
PSW	Program Status Word Register	D0H	00H
RCON	Internal RAM Control Register	86H	F0H
ROTORSPEEDH	Rotor Speed Count Register High	97H	FFH
ROTORSPEEDL	Rotor Speed Count Register Low	96H	FFH
RSTS	Reset Source Register	FEH	0AH
SBUF	Serial Port Data Buffer	99H	00H
SCON	Serial Port Control Register	98H	00H
SP	Stack Pointer	81H	07H
SRELH	Serial Port Reload Register High	9BH	00H
SRELL	Serial Port Reload Register Low	9AH	00H
SVPWMAMPFT	SVPWM Amplitude Fine-Tune Register	DAH	00H
SVPWMAMPH	SVPWM Amplitude Register High	C4H	00H
SVPWMAMPL	SVPWM Amplitude Register Low	C3H	00H
SVPWMANG	SVPWM Angle Register	C1H	00H
SYNC	MOC Sync Register	D7H	00H
T2CON	Timer2 Control Register	C8H	00H
TAKEY	Time Access Key Register	FFH	00H
TCON	Timer 0/1 Control Register	88H	00H

TH0	Timer0 High byte	8CH	00H
TH1	Timer1 High byte	8DH	00H
TH2	Timer2 High byte	B5H	00H
TL0	Timer0 Low byte	8AH	00H
TL1	Timer1 Low byte	8BH	00H
TL2	Timer2 Low byte	B4H	00H
TMOD	Timer 0/1 Mode Register	89H	00H
VRHALL	Virtual Hall Register	D9H	05H
WDTC	Watchdog Timer Control Register	B6H	04H
WDTK	Watchdog Timer Refresh Key	B7H	00H

10. Memory

MDRHA0 memory structure follows the general 8052 structures.

There are three memory areas: Program Memory (Flash), External Data Memory (XRAM) and Internal Data Memory (IRAM). In addition, **MDRHA0** integrates 8Kbytes Flash, 256bytes IRAM and 256bytes XRAM.

10.1. Program Memory

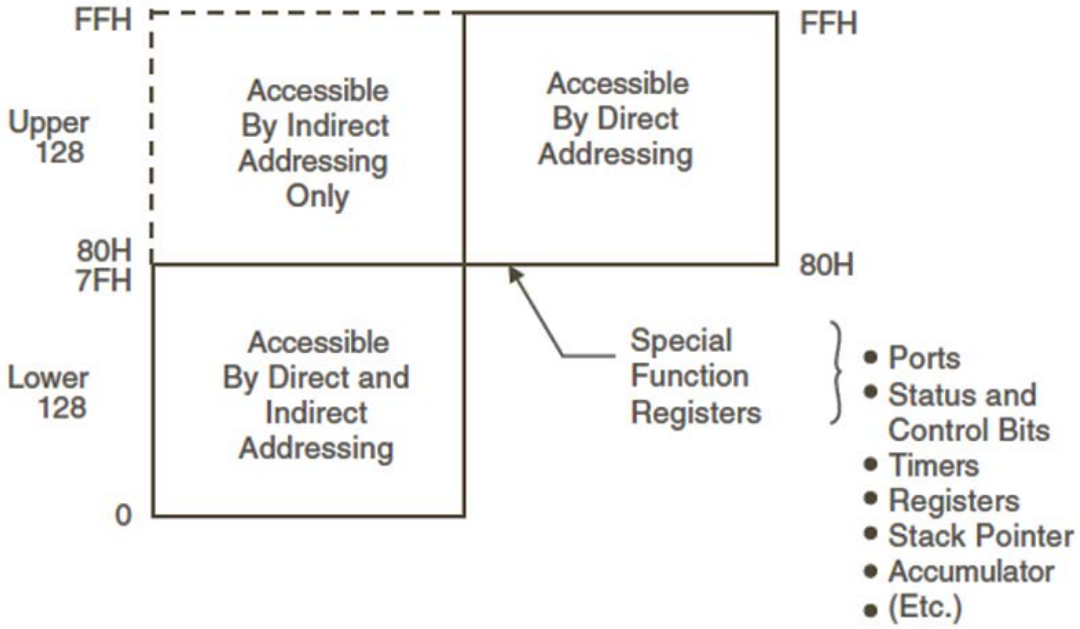
MDRHA0 contains 8Kbytes of on-chip Flash memory for program storage.

10.2. Data Memory

MDRHA0 contains 256bytes of general internal data memory (IRAM) and 256 bytes of external data memory (XRAM).

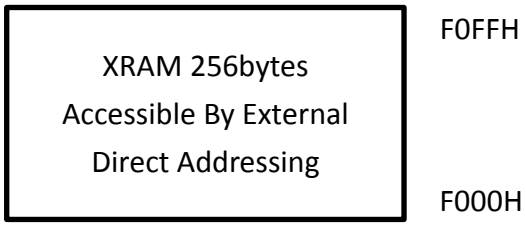
10.2.1 Data Memory (IRAM)(00H~FFH)

The lower 128 bytes of IRAM may be accessed through both direct and indirect addressing. The upper 128 bytes of IRAM and the 128 bytes of SFR registers share the same address space. The upper 128 bytes of data memory may only be accessed using indirect addressing. The SFR registers can only be accessed through direct addressing. The lowest 32 bytes (00H -1FH) of data memory are grouped into 4 banks of 8 registers each. The **RS0** and **RS1** bits (**PSW**.3 and**PSW**.4) select which register bank is in use. Instructions using register addressing will only access the currently specified bank.



10.2.2Data Memory (XRAM)(F000H~F0FFH)

External addresses F000H to F0FFh contain the on-chip expanded SRAM. This memory can be accessed via external direct addressing mode (with **MOVX** instructions). The address space of instruction **MOVX** @Ri, A (i=0,1) is determined by **RCON** [7:0] of SFR 86H**RCON**(internal RAM control register). The default setting of **RCON** [7:0] is F0h (page0). One page of XRAM is 256 bytes.



11. Instruction Set

MDRHA0 is fully binary compatible with the MCS-51 instruction set.

Arithmetic operations	Description	Bytes	Cycles	Hex Code
ADD A,Rn	Add register to accumulator	1	1	0x28-0x2F
ADD A,direct	Add directly addressed data to accumulator	2	2	0x25
ADD A,@Ri	Add indirectly addressed data to accumulator	1	2	0x26-0x27
ADD A,#data	Add immediate data to accumulator	2	2	0x24
ADDC A,Rn	Add register to accumulator with carry	1	1	0x38-0x3F
ADDC A,direct	Add directly addressed data to accumulator with carry	2	2	0x35
ADDC A,@Ri	Add indirectly addressed data to accumulator with carry	1	2	0x36-0x37
ADDC A,#data	Add immediate data to accumulator with carry	2	2	0x34
SUBB A,Rn	Subtract register from accumulator with borrow	1	1	0x98-0x9F
SUBB A,direct	Subtract directly addressed data from accumulator with borrow	2	2	0x95
SUBB A,@Ri	Subtract indirectly addressed data from accumulator with borrow	1	2	0x96-0x97
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2	0x94
INC A	Increment accumulator	1	1	0x04
INC Rn	Increment register	1	2	0x08-0x0F
INC direct	Increment directly addressed location	2	3	0x05
INC @Ri	Increment indirectly addressed location	1	3	0x06-0x07
INC DPTR	Increment data pointer	1	1	0xA3
DEC A	Decrement accumulator	1	1	0x14
DEC Rn	Decrement register	1	2	0x18-0x1F
DEC direct	Decrement directly addressed location	2	3	0x15
DEC @Ri	Decrement indirectly addressed location	1	3	0x16-0x17
MUL AB	Multiply A and B	1	5	0xA4
DIV	Divide A by B	1	5	0x84
DA A	Decimally adjust accumulator	1	1	0xD4

Logic operations	Description	Bytes	Cycles	Hex Code
ANL A,Rn	AND register to accumulator	1	1	0x58-0x5F
ANL A,direct	AND directly addressed data to accumulator	2	2	0x55
ANL A,@Ri	AND indirectly addressed data to accumulator	1	2	0x56-0x57
ANL A,#data	AND immediate data to accumulator	2	2	0x54
ANL direct,A	AND accumulator to directly addressed location	2	3	0x52
ANL direct,#data	AND immediate data to directly addressed location	3	4	0x53
ORL A,Rn	OR register to accumulator	1	1	0x48-0x4F
ORL A,direct	OR directly addressed data to accumulator	2	2	0x45
ORL A,@Ri	OR indirectly addressed data to accumulator	1	2	0x46-0x47
ORL A,#data	OR immediate data to accumulator	2	2	0x44
ORL direct,A	OR accumulator to directly addressed location	2	3	0x42
ORL direct,#data	OR immediate data to directly addressed location	3	4	0x43
XRL A,Rn	Exclusive OR register to accumulator	1	1	0x68-0x6F
XRL A,direct	Exclusive OR directly addressed data to accumulator	2	2	0x65
XRL A,@Ri	Exclusive OR indirectly addressed data to accumulator	1	2	0x66-0x67
XRL A,#data	Exclusive OR immediate data to accumulator	2	2	0x64
XRL direct,A	Exclusive OR accumulator to directly addressed location	2	3	0x62
XRL direct,#data	Exclusive OR immediate data to directly addressed location	3	4	0x63
CLR A	Clear accumulator	1	1	0xE4
CPL A	Complement accumulator	1	1	0xF4
RL A	Rotate accumulator left	1	1	0x23
RLC A	Rotate accumulator left through carry	1	1	0x33
RR A	Rotate accumulator right	1	1	0x03
RRC A	Rotate accumulator right through carry	1	1	0x13
SWAP A	Swap nibbles within the accumulator	1	1	0xC4

Data transfer operations	Description	Bytes	Cycles	Hex Code
MOV A,Rn	Move register to accumulator	1	1	0xE8-0xEF
MOV A,direct	Move directly addressed data to accumulator	2	2	0xE5
MOV A,@Ri	Move indirectly addressed data to accumulator	1	2	0xE6-0xE7
MOV A,#data	Move immediate data to accumulator	2	2	0x74
MOV Rn,A	Move accumulator to register	1	2	0xF8-0xFF
MOV Rn,direct	Move directly addressed data to register	2	4	0xA8-0xAF
MOV Rn,#data	Move immediate data to register	2	2	0x78-0x7F
MOV direct,A	Move accumulator to direct	2	3	0xF5
MOV direct,Rn	Move register to direct	2	3	0x88-0x8F
MOV direct1,direct2	Move directly addressed data to directly addressed location	3	4	0x85
MOV direct,@Ri	Move indirectly addressed data to directly addressed location	2	4	0x86-0x87
MOV direct,#data	Move immediate data to directly addressed location	3	3	0x75
MOV @Ri,A	Move accumulator to indirectly addressed location	1	3	0xF6-0xF7
MOV @Ri,direct	Move directly addressed data to indirectly addressed location	2	5	0xA6-0xA7
MOV @Ri,#data	Move immediate data to in directly addressed location	2	3	0x76-0x77
MOV DPTR,#data16	Load data pointer with a 16-bit immediate	3	3	0x90
MOVC A,@A+DPTR	Load accumulator with a code byte relative to DPTR	1	3	0x93
MOVC A,@A+PC	Load accumulator with a code byte relative to PC	1	3	0x83
MOVX A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	3	0xE2-0xE3
MOVX A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	3	0xE0
MOVX @Ri,A	Move accumulator to external RAM (8-bit addr.)	1	4	0xF2-0xF3
MOVX @DPTR,A	Move accumulator to external RAM (16-bit addr.)	1	4	0xF0

PUSH direct	Push directly addressed data onto stack	2	4	0xC0
POP direct	Pop directly addressed location from stack	2	3	0xD0
XCH A,Rn	Exchange register with accumulator	1	2	0xC8-0xCF
XCH A,direct	Exchange directly addressed location with accumulator	2	3	0xC5
XCH A,@Ri	Exchange indirect RAM with accumulator	1	3	0xC6-0xC7
XCHD A,@Ri	Exchange low-order nibbles of indirect and accumulator	1	3	0xD6-0xD7

Program branches	**Description**	**Bytes**	**Cycles**	**Hex Code**
ACALL addr11	Absolute subroutine call	2	6	xxx10001b
LCALL addr16	Long subroutine call	3	6	0x12
RET	Return from subroutine	1	4	0x22
RETI	Return from interrupt	1	4	0x32
AJMP addr11	Absolute jump	2	3	xxx00001b
LJMP addr16	Long jump	3	4	0x02
SJMP rel	Short jump (relative address)	2	3	0x80
JMP @A+DPTR	Jump indirect relative to the DPTR	1	2	0x73
JZ rel	Jump if accumulator is zero	2	3	0x60
JNZ rel	Jump if accumulator is not zero	2	3	0x70
JC rel	Jump if carry flag is set	2	3	0x40
JNC	Jump if carry flag is not set	2	3	0x50
JB bit,rel	Jump if directly addressed bit is set	3	4	0x20
JNB bit,rel	Jump if directly addressed bit is not set	3	4	0x30
JBC bit,rel	Jump if directly addressed bit is set and clear bit	3	4	0x10
CJNE A,direct,rel	Compare directly addressed data to accumulator and jump if not equal	3	4	0xB5
CJNE A,#data,rel	Compare immediate data to accumulator and jump if not equal	3	4	0xB4
CJNE Rn,#data,rel	Compare immediate data to register and jump if not equal	3	4	0xB8-0xBF
CJNE @Ri,#data,rel	Compare immed. to ind. and jump if not equal	3	4	0xB6-0xB7
DJNZ Rn,rel	Decrement register and jump if not zero	2	3	0xD8-0xDF
DJNZ direct,rel	Decrement directly addressed location and jump if not zero	3	4	0xD5

NOP	No operation	1	1	0

Boolean manipulation	Description	Bytes	Cycles	Hex Code
CLR C	Clear carry flag	1	1	0xC3
CLR bit	Clear directly addressed bit	2	3	0xC2
SETB C	Set carry flag	1	1	0xD3
SETB bit	Set directly addressed bit	2	3	0xD2
CPL C	Complement carry flag	1	1	0xB3
CPL bit	Complement directly addressed bit	2	3	0xB2
ANL C,bit	AND directly addressed bit to carry flag	2	2	0x82
ANL C,/bit	AND complement of directly addressed bit to carry	2	2	0xB0
ORL C,bit	OR directly addressed bit to carry flag	2	2	0x72
ORL C,/bit	OR complement of directly addressed bit to carry	2	2	0xA0
MOV C,bit	Move directly addressed bit to carry flag	2	2	0xA2
MOV bit,C	Move carry flag to directly addressed bit	2	3	0x92

12. MCU

12.1 8051 Engine

SFR	Description	address	Reset value
ACC	Accumulator	E0H	00H
B	B Register	F0H	00H
PSW	Program Status Word Register	D0H	00H
SP	Stack Pointer	81H	07H
DP0H	Data Pointer 0 High	83H	00H
DP0L	Data Pointer 0 Low	82H	00H
DP1H	Data Pointer 1 High	85H	00H
DP1L	Data Pointer 1 Low	84H	00H
AUX	Auxiliary	8EH	11H
RCON	Internal RAM Control Register	86H	F0H

12.1.1 ACC (Accumulator)

The most important of all special function registers, that's the first comment about **Accumulator** which is also known as **ACC** or **A.** The **Accumulator** (sometimes referred to as Register A also) holds the result of most of arithmetic and logic operations.

ACC Address = E0H Reset Value = 00000000B

Accumulator

	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.1.2B (B Register)

The **B** register is used during multiplying and division instructions. It can also be used as a scratch-pad register to hold temporary data.

B Address = F0H Reset Value = 00000000B

B Register

	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.1.3 PSW (Program Status Word Register)

The **PSW** register contains status bits that reflect the current state of the CPU. Note that the Parity bit can only be modified by hardware upon the state of **ACC** register.

PSW Address = D0H Reset Value = 00000000B

Program Status Word Register

	CY	AC	F0	RS1	RS0	OV	F1	P
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

CY	Carry flag : Carry bit in arithmetic operations and accumulator for Boolean operations.
AC	Auxiliary Carry flag : Set if there is a carry-out from third bit of Accumulator in BCD Operations.
F0	General purpose Flag0 : General purpose flag available for user.
RS1	Register bank select control bit 1, used to select working register bank.
RS0	Register bank select control bit 0, used to select working register bank.
OV	Overflow flag : Set in case of overflow in Accumulator during arithmetic operations.
F1	General purpose Flag 1 : General purpose flag available for user.
P	Parity flag : Reflects the number of ‘1’s in the Accumulator. P = ‘1’ if Accumulator contains an odd number of ‘1’s P = ‘0’ if Accumulator contains an even number of ‘1’s

The state of **RS1** and **RS0** bits selects the working register bank as follows:

RS1	RS0	Selected Register Bank	Location
0	0	Bank 0	00H – 07H
0	1	Bank 1	08H – 0FH
1	0	Bank 2	10H – 17H
1	1	Bank 3	18H – 1FH

12.1.4 SP (Stack Pointer)

This register points to the top of stack in internal data memory space. It is used to store the return address of program before executing interrupt routine or subprograms. The **SP** is incremented before executing **PUSH** or **CALL** instruction and it is decremented after executing **POP** or **RET(I)** instruction (it always points the top of stack). A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08.

SP Address = 81H Reset Value = 00000111B

Stack Pointer

	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.1.5 DP0 (Data Pointer 0)

These registers are intended to hold 16-bit address in the indirect addressing mode used by **MOVX** (move external memory), **MOVC** (move program memory) or **JMP** (computed branch) instructions. They may be manipulated as 16-bit register or as two separate 8-bit registers. **DP0H** holds higher byte and **DP0L** holds lower byte of indirect address.

It is generally used to access external code or data space, e.g.:

- **MOVCA**,@**A**+**DPTR** (code space)
- **MOVA**,@**DPTR** (data space)

DP0H Address = 83H Reset Value = 00000000B

Data Pointer 0 High

	DP0H[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DP0L Address = 82H Reset Value = 00000000B

Data Pointer 0 Low

	DP0L[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.1.6 DP1 (Data Pointer 1)

The dual data pointer accelerates the movement of block data. The standard **DPTR** is a 16-bit register that is used to address external memory, or peripherals. The standard data pointer is called **DPTR0** and the second data pointer is called **DPTR1**. The data pointer select bit chooses the active pointer. The data pointer select bit (**DPS**) is located in the LSB of **AUX** register (AUX.1).

The user switches between **DPTR0** and **DPTR1** by toggling the **DPS** bit. All DPTR-related instructions use the currently selected **DPTR** for any activity.

DP1H Address = 85H Reset Value = 00000000B

Data Pointer 1 High

	DP1H[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DP1L Address = 84H Reset Value = 00000000B

Data Pointer 1Low

	DP1L[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.1.7 AUX(Auxiliary Register)

AUX Address = 8EH Reset Value = 00010001B

Auxiliary Register

	LVD_EN	LVD	-----	ITS	SMOD	BRS	DPS	CP
Bit	7	6	5	4	3	2	1	0
Type	R/W	R	X	R/W	R/W	R/W	R/W	R

LVD_EN	Low voltage detect enable : 1: Enable
LVD	Low voltage detect status. : 1:Low voltage occur
ITS	MCU instruction timing select. : 0:1T 1:2T
SMOD	Serial Port (UART) baud rate select.
BRS	Serial Port (UART) baud rate generator select.
DPS	Data pointer register select : 0 : Select DPTR Register DP0H, DP0L

	1 : Select DPTR Register DP1H, DP1L
CP	Code protect : 0 : Non-protect 1: Protect

12.1.8 RCON (Internal RAM Control Register)

256 bytes of on-chip expanded RAM are provided and can be accessed by external memory addressing method only (instruction **MOVX**). The address space of instruction **MOVX** @Ri, **A** (i= 0,1) is determined by **RCON** [7:0] of **RCON**. The default setting of **RCON** [7:0] is F0H.

RCON Address = 86H Reset Value = 11110000B

Internal RAM Control Register

	RCON[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.2GPIO

Four I/O ports are available: **Port0**, **Port1**, **Port2**, and **Port3**.

All 25port pins on **MDRHA0** can configure to one of four modes :quasi-bidirectional (standard 8051 port outputs),push-pull output, open drain output, or input-only. All port pins default to input-only mode after reset.

Two configuration registers (**PINSETx**, **PINCONFGx**) for each port select the output mode for each port pin.

SFR	Description	address	Reset value
P0	Port 0	80H	FFH
P1	Port 1	90H	FFH
P2	Port 2	A0H	FFH
P3	Port 3	B0H	FFH
PINCONG1	Pin Configure Register 1	F8H	AAH
PINCONG2	Pin Configure Register 2	F9H	AAH
PINCONG3	Pin Configure Register 3	FAH	A0H
PINCONG4	Pin Configure Register 4	FBH	AAH
PINCONG5	Pin Configure Register 5	FCH	AAH
PINCONG6	Pin Configure Register 6	FDH	A0H
PINSET1	Pin I/O Setting Register 1	F1H	AAH
PINSET2	Pin I/O Setting Register 2	F2H	AAH
PINSET3	Pin I/O Setting Register 3	F3H	0AH
PINSET4	Pin I/O Setting Register 4	F4H	00H
PINSET5	Pin I/O Setting Register 5	F5H	80H
PINSET6	Pin I/O Setting Register 6	F6H	2AH
PINSET7	Pin I/O Setting Register 7	F7H	FFH

12.2.1 Port

P0 Address = 80H Reset Value = 11111111B

Port 0

	-----	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P1 Address = 90H Reset Value = 11111111B

Port 1

	-----	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P2 Address = A0H Reset Value = 11111111B

Port 2

	P2.7	P2.6	P2.5	P2.4	P2.3	-----	-----	-----
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	X	X	X

P3 Address = B0H Reset Value = 11111111B

Port 3

	-----	-----	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

12.2.2 PINCONG (Pin Configure Register)

PINCONG1 Address = F8H Reset Value = 10101010B

Pin Configure Register 1

	CH4CONG[1:0]		---		CH6CONG[1:0]		---	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	X	X	R/W	R/W	X	X

00 : Quasi-bidirectional(standard 8051 port outputs)

01 : Push-pull output

10 : Input-only (High impedance)

11 : Open drain output

PINCONG2 Address = F9H Reset Value = 10101010B

Pin Configure Register 2

	CH0CONG[1:0]		---		CH2CONG[1:0]		---	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	X	X	R/W	R/W	X	X

00 : Quasi-bidirectional(standard 8051 port outputs)
01 : Push-pull output
10 : Input-only (High impedance)
11 : Open drain output

PINCONG3 Address = FAH Reset Value = 10100000B

Pin Configure Register 3

	XCONG[1:0]		UCONG[1:0]		XTALOCONG[1:0		XTALICONG[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)
01 : Push-pull output
10 : Input-only (High impedance)
11 : Open drain output

PINCONG4 Address = FBH Reset Value = 10101010B

Pin Configure Register 4

	ZCONG[1:0]		WCONG[1:0]		YCONG[1:0]		VCONG[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)
01 : Push-pull output
10 : Input-only (High impedance)
11 : Open drain output

PINCONG5 Address = FCH Reset Value = 10101010B

Pin Configure Register 5

	OCPNCONG[1:0]		HWPCONG[1:0]		HVPCONG[1:0]		HUPCONG[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)
01 : Push-pull output
10 : Input-only (High impedance)
11 : Open drain output

PINCONG6 Address = FDH Reset Value = 10100000B

Pin Configure Register 6

	---		---		RXCONG[1:0]		TXCONG[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)
01 : Push-pull output
10 : Input-only (High impedance)
11 : Open drain output

12.2.3 PINSET (Pin I/O Setting Register)

PINSET1 Address = F1H Reset Value = 10101010B

Pin I/O Setting Register 1

	CH4SET[1:0]		-----		CH6SET[1:0]		-----	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	X	X	R/W	R/W	X	X

00 : No pull
01 : Pull down
10 : Pull up
11 : No pull

PINSET2 Address = F2H Reset Value = 10101010B

Pin I/O Setting Register 2

	CH0SET[1:0]		-----		CH2SET[1:0]		-----	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	X	X	R/W	R/W	X	X

00 :	No pull
01 :	Pull down
10 :	Pull up
11 :	No pull

PINSET3 Address = F3H Reset Value = 00001010B

Pin I/O Setting Register 3

	XSET[1:0]		USET[1:0]		XTALOSET[1:0]		XTALISET[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 :	No pull
01 :	Pull down
10 :	Pull up
11 :	No pull

PINSET4 Address = F4H Reset Value = 00000000B

Pin I/O Setting Register 4

	ZSET[1:0]		WSET[1:0]		YSET[1:0]		VSET[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : No pull
01 : Pull down
10 : Pull up
11 : No pull

PINSET5 Address = F5H Reset Value = 10000000B

Pin I/O Setting Register 5

	OCPNSET[1:0]		HWPSET[1:0]		HVPSET[1:0]		HUPSET[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : No pull
01 : Pull down
10 : Pull up
11 : No pull

PINSET6 Address = F6H Reset Value = 00101010B

Pin I/O Setting Register 6

	-----		MOCS	GPWMS	RXSET[1:0]		TXSET [1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

TXSET[1:0], RXSET[1:0], HUNSET[1:0]

00 : No pull
01 : Pull down
10 : Pull up
11 : No pull

MOCS

0 : U、V、W、X、Y、Z、HUP、HUN、HVP、HVN、HWP、HWN、OCPN is GPIO

1 : U、V、W、X、Y、Z、HUP、HVP、HWP、OCPN is MOC interface. If MOCS = ‘1’ and**MCONT2**.0 = ‘1’, HUN、HVN、HWN is MOC interface.

GPWMS

0 : CH0 is GPIO or AD

1 : CH0 is GPWM

PINSET7 Address = F7H Reset Value = 11111111B

Pin I/O Setting Register 7

	OCPNDBT[1:0]		HWPDBT[1:0]		HVPDBT[1:0]		HUPDBT[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PIN De-bounce time

00 : 0nS

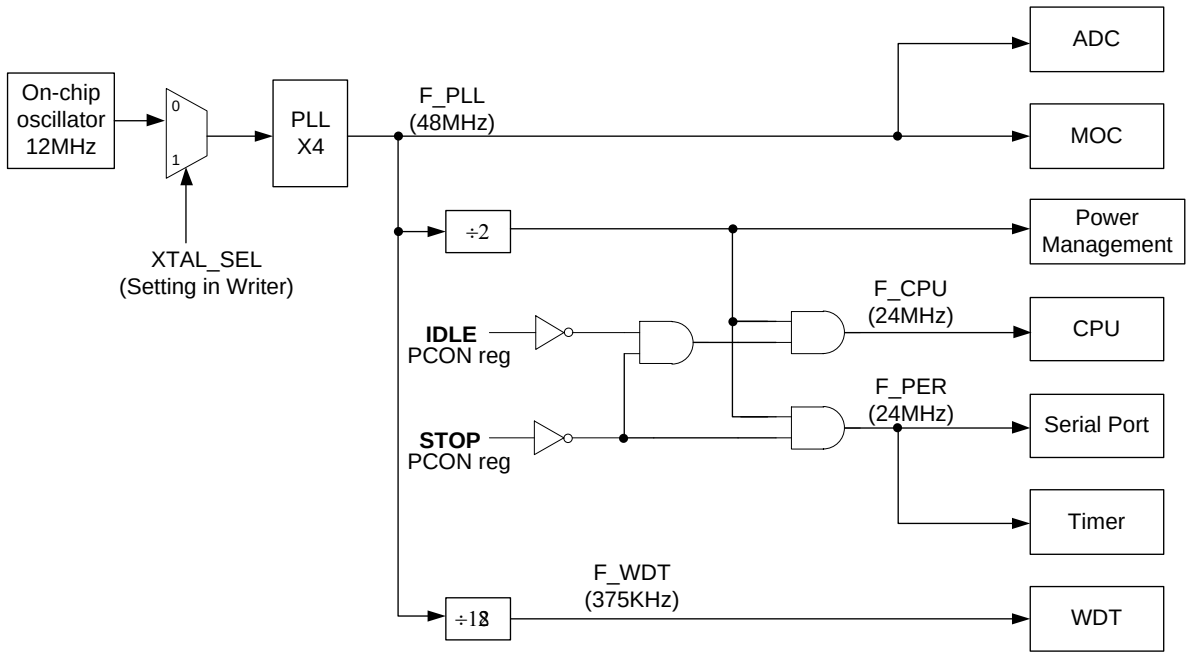
01 : 250nS

10 : 500nS

11 : 1000nS

12.3 Clock Structure

The clock source of MDRHA0 uses an internal oscillator. The internal clock source (on-chip oscillator) is run at 12MHz. The choice of internal, clock source is setting by **Writer**.



12.4Timer

The **MDRHA0** has three 16-bit timer/counter registers: **Timer0**, **Timer1** and **Timer2**. All can be configured for counter, or timer, operations.

In addition to the “timer” or “counter” selection, **Timer0** and **Timer1** have four operating modes from which to select which are selected by bit-pairs (**M1**, **M0**) in **TMOD**. Modes 0, 1,and 2 are the same for both timer/counters. Mode 3 is different.

	Timer0	Timer1	Timer2
Mode 0	13-bit timer/counter	13-bit timer/counter	13-bit timer/counter
Mode 1	16-bit timer/counter	16-bit timer/counter	16-bit timer/counter
Mode 2	8-bit auto-reload timer/counter	8-bit auto-reload timer/counter	8-bit auto-reload timer/counter
Mode 3	two independent 8-bit timers/counters	stop	8-bit timers/counters

Two Special Function registers (**TMOD** and **TCON**) are used to select the appropriate mode.

SFR	Description	address	Reset value
PFCON	Peripheral Frequency Control Register	D1H	00H
TMOD	Timer 0/1 Mode Register	89H	00H
TCON	Timer 0/1 Control Register	88H	00H
T2CON	Timer2 Control Register	C8H	00H
TH0	Timer0 High byte	8CH	00H
TL0	Timer0 Low byte	8AH	00H
TH1	Timer1 High byte	8DH	00H
TL1	Timer1 Low byte	8BH	00H
TH2	Timer2 High byte	B5H	00H
TL2	Timer2 Low byte	B4H	00H

12.4.1 PFCON (Peripheral Frequency Control Register)

PFCON Address = D1H Reset Value = 00000000B

Peripheral Frequency Control Register

	-----	-----	SRELPS[1:0]		T1PS[1:0]		T0PS[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

SRELPS[1:0]	Serial port (UART) Prescaler select : 00 :F_PER/64 01 :F_PER/32 10 :F_PER/16 11 :F_PER/8
T1PS[1:0]	Timer1(T1) Prescaler select : 00 :F_PER/12 01 :F_PER 10 :F_PER/96 11 :-----
T0PS[1:0]	Timer0(T0) Prescaler select : 00 :F_PER/12 01 :F_PER 10 :F_PER/96 11 :-----

12.4.2 TMOD (Timer 0/1 Mode Register)

TMOD register is used in configuration of MCU**Timer0** and **Timer1**.

TMOD Address = 89H Reset Value = 00000000B

Timer 0/1 Mode Register

	GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

GATE1	Timer1 gate control : If set, enables external gate control (pin **INT1N**) for Counter1. When **INT1N** is high, and TR1 bit is set, the Counter1 is incremented every falling edge on **INT1N** input pin
C/T1	Timer1 counter/timer select : 0 : Timer 1 : Counter
GATE0	Timer 0 gate control : If set, enables external gate control (pin **INT0N**) for Counter0. When **INT0N** is high, and TR0 bit is set, the Counter0 is incremented every falling edge on**INT0N** input pin
C/T0	Timer0 counter/timer select : 0 : Timer 1 : Counter

T1M1 /T0M1	T1M0 /T0M0	Mode	Function
0	0	Mode0	13-bit Counter/Timer, with 5 lower bits in TL0 (TL1) register and 8 bits in TH0 (TH1) register (for Timer0 or Timer1, respectively). The 3 high-order bits of TL0 (TL1) are zeroed whenever Mode 0 is enabled. (Not auto-reload)
0	1	Mode1	16-bit Counter/Timer. (Not auto-reload)
1	0	Mode2	8 -bit auto-reload Counter/Timer. The reload value is kept in TH0 (TH1), while TL0 (TL1) is incremented every clock cycle. Reloaded from TH0 (TH1) at overflow.
1	1	Mode3	For Timer1: Timer1 is stopped. For Timer0: Timer0 acts as two independent 8 bit Timers / Counters – TL0, TH0. (Not auto-reload)

12.4.3 TCON (Timer 0/1Control Register)

TCON register is used to control operation of these modules.**MDRHA0** includes two external digital interrupt sources **INT0N** and **INT1N**), with dedicated interrupt sources. **INT0N** and **INT1N** are configurable as falling edge or low level. The **IT0** and **IT1** bits in **TCON** select level- or edge-sensitive.**IE0** and **IE1** in the **TCON** register serve as the interrupt-pending flags for the **INT0N**and **INT1N** external interrupts, respectively.

TCON Address = 88H Reset Value = 00000000B

Timer 0/1 Control Register

	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TF1	Timer1 overflow flag : Bit set by hardware when Timer1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR1	Timer1 run control : 0 : Stop 1 : Run
TF0	Timer0 overflow flag : Bit set by hardware when Timer1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR0	Timer0run control : 0 : Stop 1 : Run
IE1	External interrupt 1 flag : Set by hardware, when External interrupt (**INT1N**) is observed. Cleared by hardware when interrupt is processed.
IT1	External interrupt 1 type control : 0 : External interrupt 1 is activated at low level on input pin 1 : External interrupt 1 is activated at falling edge on input pin
IE0	External interrupt 0 flag : Set by hardware, when External interrupt (**INT0N**) is observed. Cleared by hardware when interrupt is processed.
IT0	External interrupt 0 type control : 0 : External interrupt 0 is activated at low level on input pin 1 : External interrupt 0 is activated at falling edge on input pin

The **TF0**, **TF1** (**Timer0** and**Timer1** overflow flags), **IE0** and **IE1** (External interrupt 0 and 1 flags) will be automatically cleared by hardware when the corresponding service routine is called.

12.4.4 T2CON (Timer2 Control Register)

T2CON is used to control **Timer2**run/stop, mode, prescaler.

T2CON Address = C8H Reset Value = 00000000B

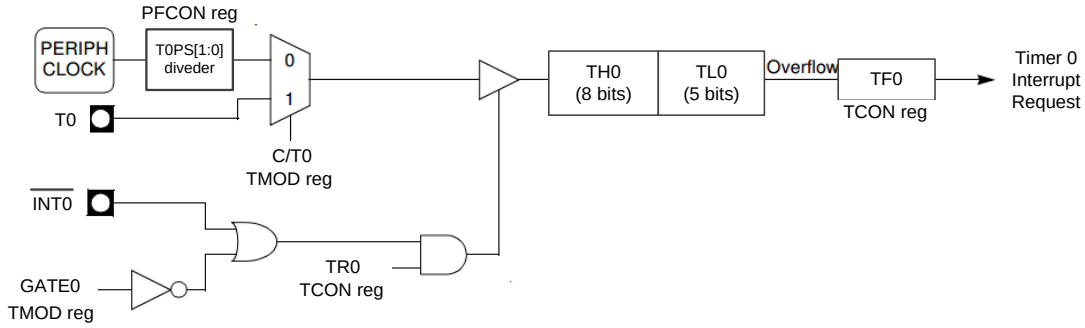
Timer2 Control Register

	-----	-----	TF2	TR2	T2M1	T2M0	T2PS1	T2PS0
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

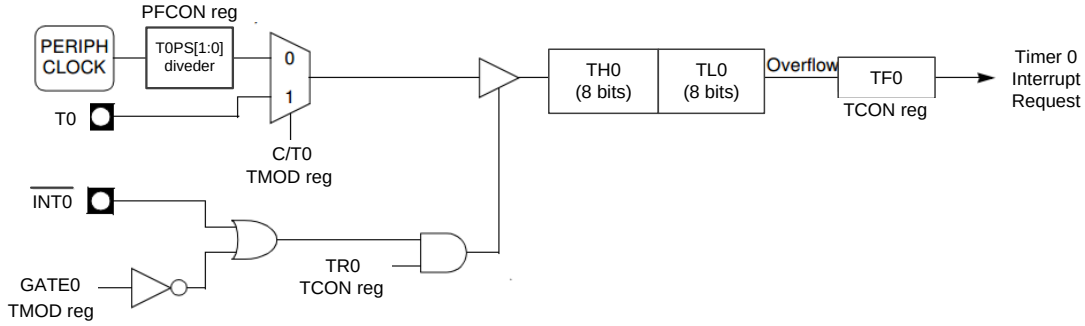
TF2	Timer2 overflow flag : Bit set by hardware when Timer2 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR2	Timer2run control : 0 : Stop 1 : Run
T2PS[1:0]	Timer2(T2) Prescaler select : 00 :F_PER/12 01 : F_PER 10 : F_PER/96 11 :-----

T2M1	T2M0	Mode	Function
0	0	Mode0	13-bit Timer, with 5 lower bits in TL2 register and 8 bits in TH2 register.(Not auto-reload)
0	1	Mode1	16-bit Timer. (Not auto-reload)
1	0	Mode2	8 -bit auto-reload Timer. The reload value is kept in TH2, while TL2 is incremented every clock cycle. Reloaded from TH2 at overflow.
1	1	Mode3	8 bit Timers. (Not auto-reload)

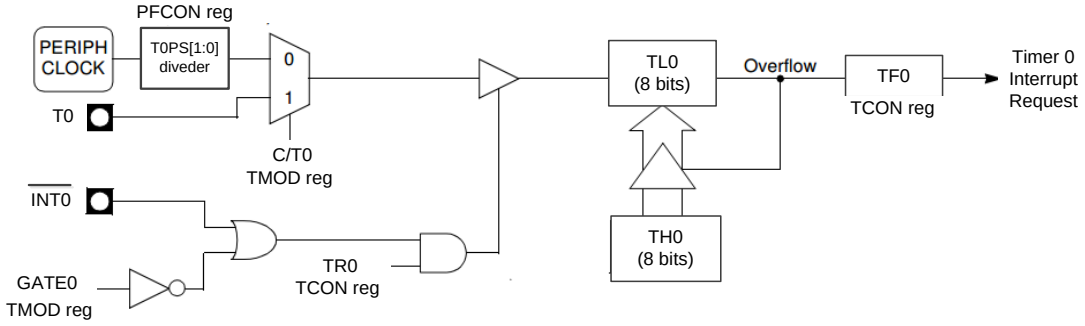
12.4.5 Timer0 Mode 0



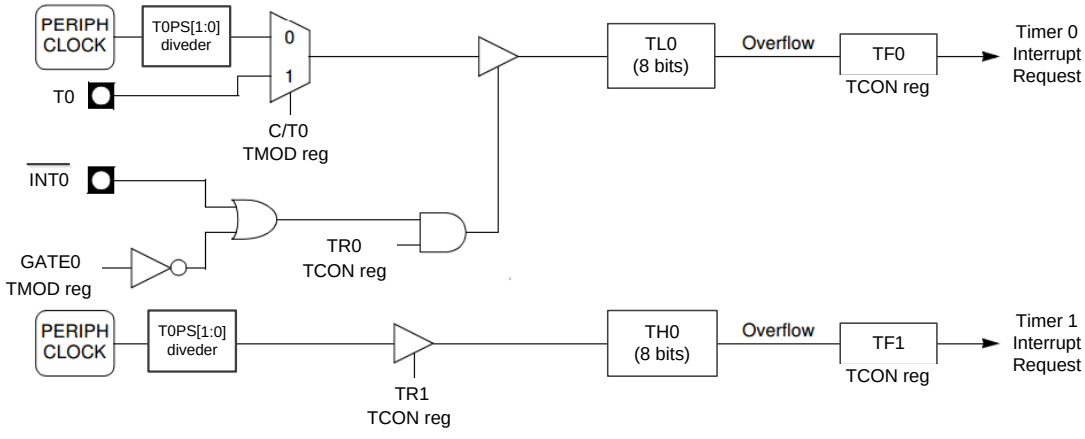
12.4.6 Timer0 Mode 1



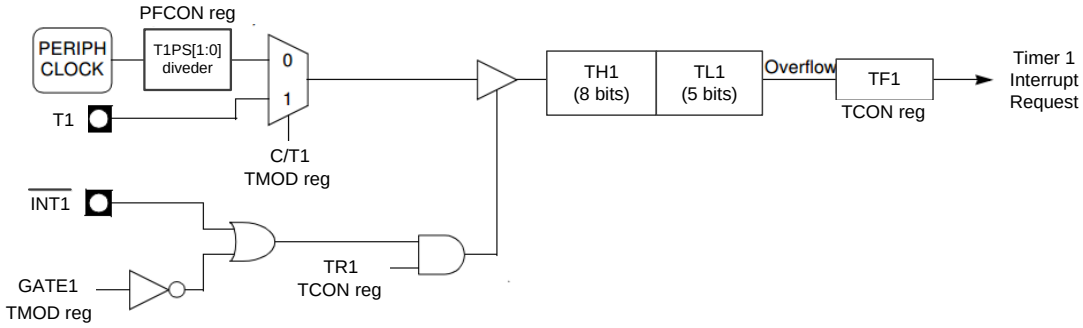
12.4.7 Timer0 Mode 2



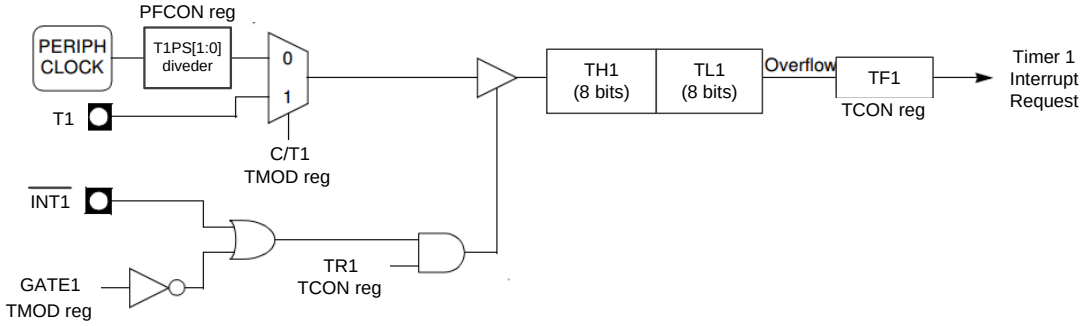
12.4.8 Timer0 Mode 3



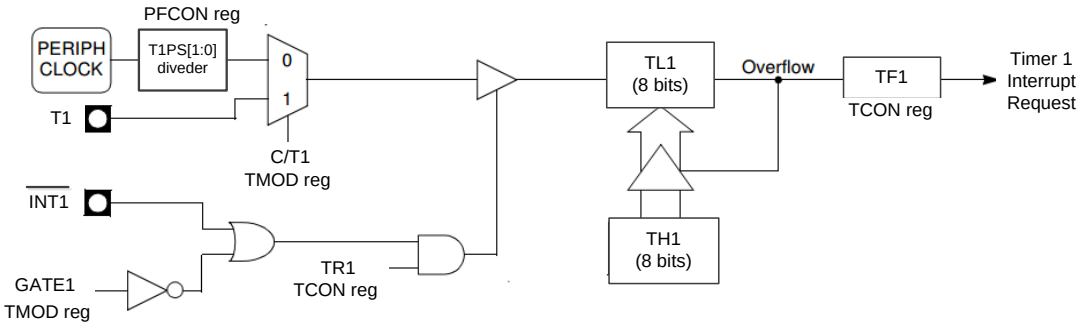
12.4.9 Timer1 Mode 0



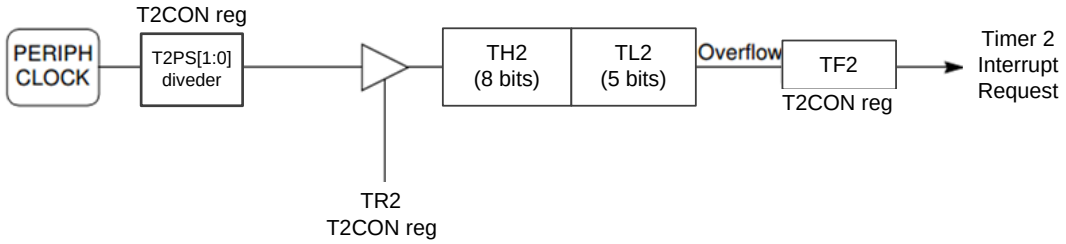
12.4.10 Timer1 Mode 1



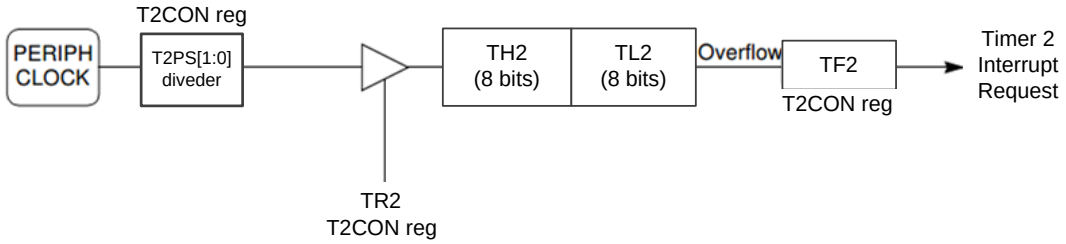
12.4.11 Timer1 Mode 2



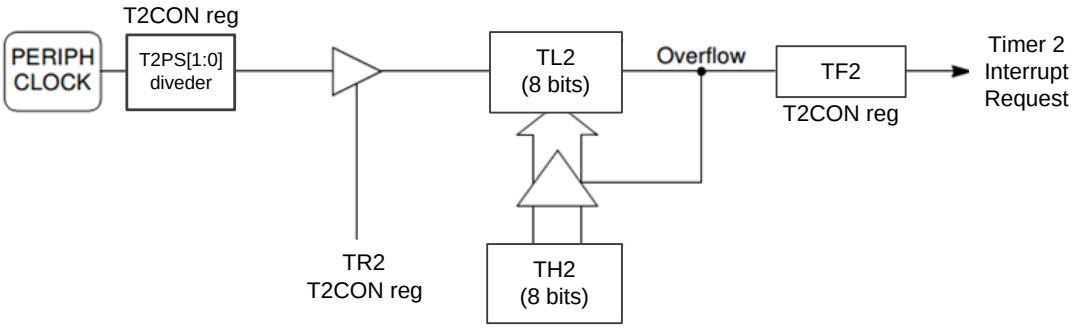
12.4.12 Timer2 Mode 0



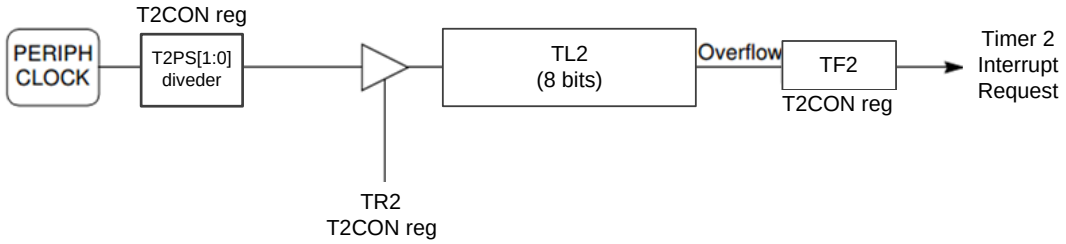
12.4.13 Timer2 Mode 1



12.4.14 Timer2 Mode 2



12.4.15 Timer2 Mode 3



12.5 Watchdog Timer

The Watchdog Timer (**WDT**) is a8-bit free-running counter that generates a reset signal or interrupt (**WDTC**.6) if it over flows. It can help the application software to recover from an abnormal condition. The **WDT** is independent from **Timer0**, **Timer1**, or **Timer2**. The **F_WDT** is 375KHz, it is from on-chip RC oscillator.

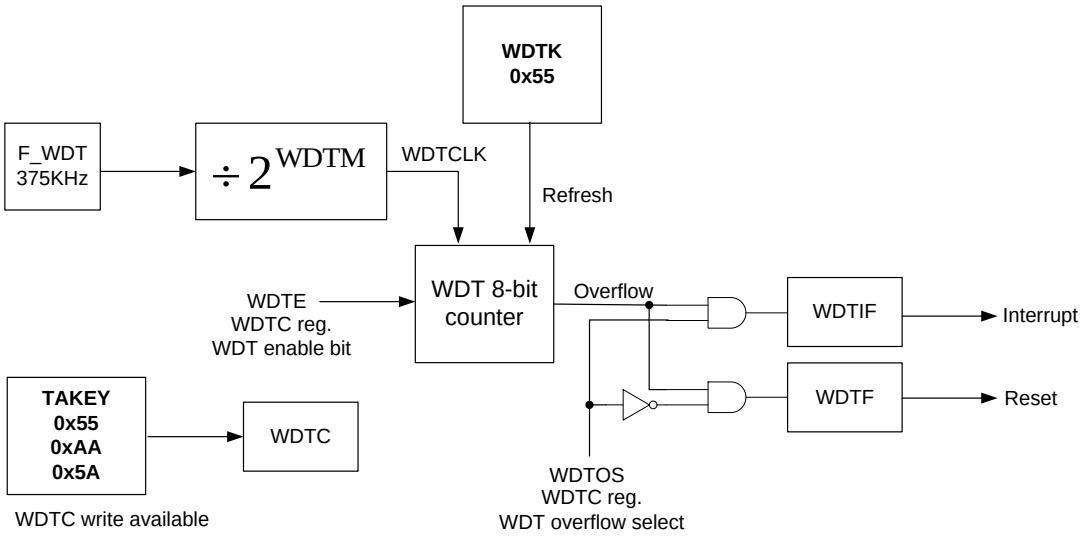


Figure 12.5.1 WDT block diagram

$$WDTCLK = F\_WDT \times \frac{1}{2^{WDTM}}$$

$$\text{WDT (8-bit counter) overflow time} = \frac{256}{WDTCLK}$$

SFR	Description	address	Reset value
RSTS	Reset Source Register	FEH	0AH
TAKEY	Time Access Key Register	FFH	00H
WDTC	Watchdog Timer Control Register	B6H	04H
WDTK	Watchdog Timer Refresh Key	B7H	00H

RSTS Address = FEH Reset Value = 00001010B

Reset Source Register

	-----	-----	-----	WDTRF	PINRF[1:0]		PORF[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R/W	R/W	R/W	R/W	R/W

WDTRF	Watchdog timer reset flag. This flag is set to 1 if the Watchdog Timer Reset caused the reset.
PINRF[1:0]	$\overline{RST}$pin reset flag. This flag is set to 10b if the $\overline{RST}$ pin caused the reset. Clear by firmware.
PORF[1:0]	POR reset flag. This flag is set to 10b if the POR caused the reset. Clear by firmware.

12.5.1 WDTC (Watchdog Timer Control Register)

WDTC Address = B6H Reset Value = 00000100B

Watchdog Timer Control Register

	-----	WDTOS	WDTE	-----	WDTM[3:0]			
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	X	R/W	R/W	R/W	R/W

WDTOS	Watchdog timer overflow select : 0 : When WDT overflow, enable WDT reset. 1 : When WDT overflow, enable WDT interrupt.
WDTE	Watchdog timer enable : 0 : Disable WDT. 1 : Enable WDT.
WDTM[3:0]	WDT clock divider : WDTCLK = $375KHz \times \frac{1}{2^{WDTM}}$ (default is 375KHz / 16)

12.5.2 TAKEY (Time Access Key Register)

TAKEY Address = FFH Reset Value = 00000000B

Time Access Key Register

	TAKEY[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WDTC default is read only, must write three specific values 55H, AAH and 5AH to the TAKEY enable the WDTC write available.

The sequence is:

MOV TAKEY, #55h

MOV TAKEY, #AAh

MOV TAKEY, #5Ah

12.5.3 WDTK (Watchdog Timer Refresh Key)

WDTK Address = B7H Reset Value = 00000000B

Watchdog Timer Refresh Key

	WDTK[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The application must write 0x55 into the WDTK register, for the Watchdog timer to be cleared.

For example, enable the watchdog with a time-out reset period of 5.461ms.

Following write sequence:

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah ; WDTC write is available.
MOV WDTC, #23h ; WDTM [3:0] = 0011b. WDTE =1 to enable the WDT.
MOV WDTK, #55h ;Refresh WDT.
```

12.6Serial Port (UART)

The Serial Port provides a flexible full-duplex synchronous/asynchronous receiver/transmitter, called **UART**. The communication rate can be set by configuring the baud rate in **SFRs**. The two serial buffers consist of two separate registers, a transmit buffer and a receive buffer. Writing data to the SFR **SBUF**, transfers the data to the serial output buffer and starts the transmission. Reading from the **SBUF**, reads data from the serial receive buffer. The serial port can simultaneously transmit and receive data. It can also buffer 1 byte at receive, which prevents the receive data from being lost if the CPU reads the second byte before the transmission of the first byte is completed.

SFR	Description	address	Reset value
AUX	Auxiliary	8EH	11H
PFCON	Peripheral Frequency Control Register	D1H	00H
SCON	Serial Port Control Register	98H	00H
SBUF	Serial Port Data Buffer	99H	00H
SRELH	Serial Port Reload Register High	9BH	00H
SRELL	Serial Port Reload Register Low	9AH	00H

AUX Address = 8EH Reset Value = 00010001B

Auxiliary Register

	LVD_EN	LVD	-----	ITS	SMOD	BRS	DPS	CP
Bit	7	6	5	4	3	2	1	0
Type	R/W	R	X	R/W	R/W	R/W	R/W	R

LVD_EN	Low voltage detect enable : 1: Enable
LVD	Low voltage detect status. : 1: Low voltage occur
ITS	MCU instruction timing select. : 0:1T 1:2T
SMOD	Serial Port (UART) baud rate select.
BRS	Serial Port (UART) baud rate generator select.
DPS	Data pointer register select : 0 : Select DPTR Register DP0H, DP0L 1 : Select DPTR Register DP1H, DP1L

CP	Code protect : 0 : Non-protect 1: Protect

PFCON Address = D1H Reset Value = 00000000B

Peripheral Frequency Control Register

	-----	-----	SRELPS[1:0]		T1PS[1:0]		T0PS[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

SRELPS[1:0]	Serial port (UART) Prescaler select : 00 :F_PER/64 01 :F_PER/32 10 :F_PER/16 11 :F_PER/8
T1PS[1:0]	Timer1(T1) Prescaler select : 00 :F_PER/12 01 :F_PER 10 :F_PER/96 11 :-----
T0PS[1:0]	Timer0(T0) Prescaler select : 00 : F_PER/12 01 : F_PER 10 : F_PER/96 11 :-----

12.6.1 SCON (Serial Port Control Register)

The **SCON** register controls the function of Serial Port (**UART**).

SCON Address = 98H Reset Value = 00000000B

Serial Port Control Register

	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SM0	SM1	Mode	Description	Baud Rate	
0	0	Mode 0	Shift register	F_PER/12	
0	1	Mode 1	8bit UART	Variable	
1	0	Mode 2	9bit UART	Depends on SMOD (AUX.3)	
				SMOD	Baud Rate
				0	F_PER/64
				1	F_PER/32
1	1	Mode 3	9bit UART	Variable	

SM2	Multiprocessor communication enable
REN	Serial reception enable : 0 : Serial reception at Serial Port is disabled. 1 :Serial reception at Serial Port is enabled.
TB8	Transmitter bit 8 : This bit is used while transmitting data through Serial Port in Modes 2 and 3. The state of this bit corresponds with the state of the 9th transmitted bit (e.g. parity check or multiprocessor communication). It is controlled by software.
RB8	Received bit 8 : This bit is used while receiving data through Serial Port 0 in Modes 2 and 3. It reflects the state of the 9th received bit. In Mode 1, if multiprocessor communication is enabled (sm2 = 0), this bit is the stop bit that was received. In Mode 0 this bit is not used.
TI	Transmit interrupt flag : (completion of a serial transmission) It is set by hardware at the end of bit 8 in mode 0 or at the beginning of a stop bit in other modes. It must be cleared by software.
RI	Receive interrupt flag : (It must be cleared by software.) It is set by hardware after completion of a serial reception at Serial Port 0. It is set by hardware at the end of bit 8 in mode 0 or in the middle of a stop bit in other modes.

Serial Port working in modes 1 or mode 3:

When BRS = 0 (AUX.2)

TIPS[1:0] = 00b

$$\text{baud rate} = \frac{2^{SMOD}}{32\times(256\text{-}TH1)} \times \frac{F\_PER}{12}$$

TIPS[1:0] = 01b

$$\text{baud rate} = \frac{2^{SMOD}}{32\times(256\text{-}TH1)} \times F\_PER$$

TIPS[1:0] = 10b

$$\text{baud rate} = \frac{2^{SMOD}}{32\times(256\text{-}TH1)} \times \frac{F\_PER}{96}$$

When BRS = 1 (AUX.2)

SRELPS[1:0] = 00b

$$\text{baud rate} = \frac{2^{SMOD}}{2^{10}-SREL[H,L]} \times \frac{F\_PER}{64}$$

SRELPS [1:0] = 01b

$$\text{baud rate} = \frac{2^{SMOD}}{2^{10}-SREL[H,L]} \times \frac{F\_PER}{32}$$

SRELPS [1:0] = 10b

$$\text{baud rate} = \frac{2^{SMOD}}{2^{10}-SREL[H,L]} \times \frac{F\_PER}{16}$$

SRELPS [1:0] = 11b

$$\text{baud rate} = \frac{2^{SMOD}}{2^{10}-SREL[H,L]} \times \frac{F\_PER}{8}$$

12.6.2 SBUF (Serial Port Data Buffer)

Writing data to this register sets data in serial output buffer and starts the transmission through Serial Port. Reading from the **SBUF**, reads data from the serial receive buffer.

SBUF Address = 99H Reset Value = 00000000B

Serial Port Data Buffer

	SBUF[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.6.3 SREL (Serial Port Reload Register)

Serial Port Reload Register is used for Serial Port baud rate generation. Only 10 bits are used, where 8 bits from the **SRELL** as lower bits and 2 bits from the **SRELH** (SRELH.1, SRELH.0) as higher bits.

SRELH Address = 9BH Reset Value = 00000000B

Serial Port Reload Register High

	-----	-----	-----	-----	-----	-----	SREL.9	SREL.8
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	X	R/W	R/W

SRELL Address = 9AH Reset Value = 00000000B

Serial Port Reload Register Low

	SREL[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.7 Power Management

The Power Control Register (**PCON**) is used to control the **MDRHA0STOP** and **IDLE** power management modes.

PCON Address = 87H Reset Value = 00000000B

Power Control Register

	-----	-----	-----	-----	-----	-----	STOP	IDLE
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	X	R/W	R/W

STOP	Stop mode bit. Setting this bit activates STOP operation. (read as 0)

IDLE	Idle mode bit. Setting this bit activates IDLE mode operation. (read as 0)

12.7.1 STOP MODE

Setting the **STOP** Mode Select bit (**PCON**.1) causes the controller core to enter **STOP** mode as soon as the instruction that sets the bit completes execution. In **STOP** mode the CPU, GPIO, UART, and Timers are stopped, but the ADC, MOC, and WDT is still work.

STOP mode can terminate by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

The assertion of an enabled interrupt will cause the **STOP** Mode Selection bit (**PCON**.1) to be cleared and the CPU to resume operation.

12.7.2 IDLE MODE

Setting the **IDLE** Mode Select bit (**PCON**.0) causes the hardware to halt the CPU and enter **IDLE** mode as soon as the instruction that sets the bit completes execution.

In **IDLE** mode only the CPU is stop. All internal registers and memory maintain their original data.

IDLE mode can terminate by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

The assertion of an enabled interrupt will cause the **IDLE** Mode Selection bit (**PCON**.0) to be cleared and the CPU to resume operation.

12.8 Reset

The reset logic is used to place the device into a known state.

MDRHA0 provides Power-on Reset flag, External Reset **RSTN** flag and Watchdog timer Reset flag to monitor reset status. The source of the reset can be monitor.

12.8.1 RSTS (Reset Source Register)

RSTS Address = FEH Reset Value = 00001010B

Reset Source Register

	-----	-----	-----	WDTRF	PINRF[1:0]		PORF[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R/W	R/W	R/W	R/W	R/W

WDTRF	Watchdog timer reset flag. This flag is set to 1 if the Watchdog Timer Reset caused the reset.
PINRF[1:0]	**RSTN** pin reset flag. This flag is set to 10b if the **RSTN** pin caused the reset. Clear by firmware.
PORF[1:0]	POR reset flag. This flag is set to 10b if the POR caused the reset. Clear by firmware.

12.9Interrupt Controller

The **ISR** - Interrupt Service Routine unit, is a subcomponent responsible for interrupt handling. It receives up to **14**interrupt requests. Each interrupt source has its own request flag that is located in devices which is a source of interrupt. No interrupt request flags are located directly in **ISR**. All interrupts are requested by high level on correspondent inputs to **ISR**. Each of the interrupt sources can be individually enabled or disabled by corresponding enable flag in **IEN0**, **IEN1**SFR registers. Additionally all interrupts can be globally enabled or disabled by the —**EA** flag in the **IEN0** SFR. All interrupt sources are divided into 6 interrupts groups. Each of the interrupt groups can have one of four interrupt priority levels assigned. The interrupt priority level is defined by flags located in the **IP0** and **IP1** SFR registers.

Interrupt Number (use Keil C Tool)	Interrupt Vector Address	Interrupt Request Flags
0	0003H	-----
1	000BH	TF0 – Timer0 interrupt
2	0013H	IE1 – External interrupt 1
3	001BH	TF1 – Timer1 interrupt
4	0023H	SPIF(TI, RI)– Serial port interrupt
5	002BH	TF2 – Timer2 interrupt
6	0033H	-----
7	003BH	-----
8	0043H	OCPSIF – OCP Short interrupt
9	004BH	HALLIF – HALL interrupt
10	0053H	MPWMMINIF–MPWM MIN interrupt
11	005BH	MPWMMAXIF–MPWM MAX interrupt
12	0063H	GPWMMAXIF – GPWM MAX interrupt
13	006BH	LVDIF – Low voltage detect interrupt
14	0073H	WDTIF – Watchdog timer interrupt
15	007BH	OCPLIF – OCP Limit interrupt

Table12.9.1 Interrupt vectors

Group priority	Interrupt Group	Highest priority in group		Lowest priority in group
Highest	Group0	LVDIF	IE0	-----
	Group1	WDTIF	TF0	-----
	Group2	OCPSIF	HALLIF	IE1
	Group3	MPWMMINIF	MPWMMAXIF	TF1
	Group4	GPWMMAXIF	SPIF(TI, RI)	-----
Lowest	Group5	OCPLIF	TF2	-----

Table12.9.2 Interrupt Priority Groups

SFR	Description	address	Reset value
IEN0	Interrupt Enable Register 0	A8H	00H
IEN1	Interrupt Enable Register 1	B8H	00H
IRCON1	Interrupt Request Register 1	C0H	00H
IP0	Interrupt Priority Register 0	A9H	00H
IP1	Interrupt Priority Register 1	B9H	00H

12.9.1IEN0 (Interrupt Enable Register 0)

IEN0 Address = A8H Reset Value = 00000000B

Interrupt Enable Register 0

	EA	-----	ET2	ESP	ET1	EX1	ET0	EX0
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	R/W	R/W	R/W	R/W	R/W	R/W

EA	Interrupts enable : 0 :DisableAll interrupts. 1 :Enable interrupt.
ET2	Timer2 interrupt enable: 0 :Disable Timer2 overflow interrupt. 1 :When EA = 1, enable Timer2 overflow interrupt.
ESP	Serial port interrupt enable: 0 :Disable Serial port interrupt. 1 :When EA = 1, enable Serial port interrupt.
ET1	Timer1 interrupt enable: 0 :Disable Timer1 overflow interrupt. 1 :When EA = 1, enable Timer1 overflow interrupt.
EX1	External interrupt 1 enable: 0 :Disable External interrupt 1. 1 :When EA = 1, enable External interrupt 1.
ET0	Timer0 interrupt enable: 0 :Disable Timer0 overflow interrupt. 1 :When EA = 1, enable Timer0 overflow interrupt.
EX0	External interrupt 0 enable: 0 :Disable External interrupt 0. 1 :When EA = 1, enable External interrupt 0.

12.9.2 IEN1 (Interrupt Enable Register 1)

IEN1 Address = B8H Reset Value = 00000000B

Interrupt Enable Register 1

	OCPLIE	WDTIE	LVDIE	GPWMIE	MPWMMAXIE	MPWMMINIE	HALLIE	OCPSIE
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OCPLIE	OCP (Over current protect) Limit interrupt enable: 0 :Disable OCP Limit interrupt . 1 :When EA = 1, enable OCP Limit interrupt.
WDTIE	Watchdog timer interrupts enable : 0 :Disable WDT interrupt. 1 :When EA = 1 and WDTOS = 1, enable WDT overflow interrupt.
LVDIE	LVD (Low voltage detect) interrupt enable: 0 :Disable LVD interrupt. 1 :When EA = 1, enable LVD interrupt.
GPWMIE	GPWM interrupt enable: 0 :Disable GPWM interrupt. 1 :When EA = 1, enable GPWM interrupt.
MPWMMAXIE	MPWM maximum interrupt enable: 0 :Disable MPWM maximum interrupt. 1 :When EA = 1, enable MPWM maximum interrupt.
MPWMMINIE	MPWM minimum interrupt enable: 0 :Disable MPWM minimum interrupt . 1 :When EA = 1, enable MPWM minimum interrupt.
HALLIE	HALL interrupt enable: 0 :Disable HALL interrupt. 1 :When EA = 1, enable HALL interrupt.
OCPSIE	OCP (Over current protect) Short interrupt enable: 0 :Disable OCP Short interrupt . 1 :When EA = 1, enable OCP Short interrupt.

12.9.3 IRCON1 (Interrupt Request Register 1)

IRCON1 Address = C0H Reset Value = 00000000B

Interrupt Request Register 1

	OCPLIF	WDTIF	LVDIF	GPWMIF	MPWMMAXIF	MPWMMINIF	HALLIF	OCPSIF
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OCPLIF	OCP Limit interrupt flag.
WDTIF	Watchdog timer interrupts flag.
LVDIF	LVD (Low voltage detect) interrupt flag.
GPWMIF	GPWM interrupt flag.
MPWMMAXIF	MPWM maximum interrupt flag.
MPWMMINIF	MPWM minimum interrupt flag.
HALLIF	HALL interrupt flag.
OCPSIF	OCP Short interrupt flag.

12.9.4 IP (Interrupt Priority Register)

The 14interrupt sources are grouped into 6 priority groups. For each of the groups, one of four priority levels can be selected. It is achieved by setting appropriate values in **IP0** and **IP1** registers. The contents of the Interrupt Priority Registers define the priority levels for each interrupt source according to the tables below.

IP0 Address = A9H Reset Value = 00000000B

Interrupt Priority Register 0

	-----	-----	G5IP0	G4IP0	G3IP0	G2IP0	G1IP0	G0IP0
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

G5IP0	Group5 interrupt priority bit 0
G4IP0	Group4 interrupt priority bit 0
G3IP0	Group3 interrupt priority bit 0
G2IP0	Group2 interrupt priority bit 0
G1IP0	Group1 interrupt priority bit 0
G0IP0	Group0 interrupt priority bit 0

IP1 Address = B9H Reset Value = 00000000B

Interrupt Priority Register 1

	-----	-----	G5IP1	G4IP1	G3IP1	G2IP1	G1IP1	G0IP1
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

G5IP1	Group5 interrupt priority bit 1
G4IP1	Group4 interrupt priority bit 1
G3IP1	Group3 interrupt priority bit 1
G2IP1	Group2 interrupt priority bit 1
G1IP1	Group1 interrupt priority bit 1
G0IP1	Group0 interrupt priority bit 1

Level	Priority	GxIP1	GxIP0
Level 0	Lowest	0	0
Level 1		0	1
Level 2		1	0
Level 3	Highest	1	1

13. 10-bit Analog-to-Digital Converter (ADC)

The **MDRHA0** provides eight channels 10-bit ADC. The result of the conversion is provided at **ADCD** [9:0].

SFR	Description	address	Reset value
ADCCONT	ADC Control Register	D2H	80H
ADCSTR	ADC Start Convert and Setting Register	D3H	00H
ADCD1	ADC Data Register 1	D5H	00H
ADCD2	ADC Data Register 2	D6H	00H

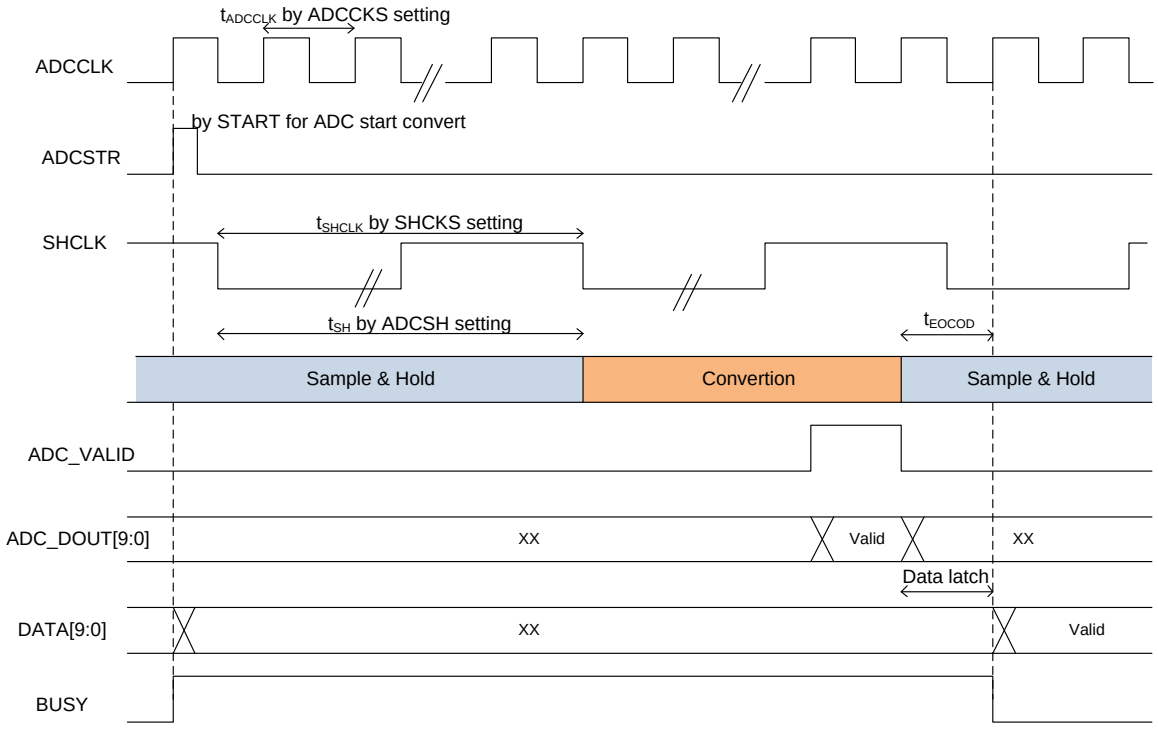


Figure13.1 ADC conversion timing

13.1 ADCCONT (ADC Control Register)

ADCCONT Address = D2H Reset Value = 1000000B

ADC Control Register

	ADCPD	ADCSH[1:0]		ADCDS	ADCCKS	ADDCH[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ADCPD ADC power down control register :

0 : Normal

1 : Power down

ADCSH[1:0] ADC sample and hold time : (base on SHCLK)

00 : 1 clock

01 : 2 clock

10 : 3 clock

11 : 4 clock

ADCDS ADC data select :

	MSB	10 bit result		LSB
0 :	ADCD2[7:0]		ADCD1.1	ADCD1.0
1 :	ADCD1.1	ADCD1.0	ADCD2[7:0]	

ADCCKS ADC conversion clock select : (ADCCLK)

0 : 4MHz

1 : 2MHz

ADCCH[2:0] ADC conversion channel select :

000:CH0	100:CH4
001: Reserve	101: Reserve
010:CH2	110:CH6
011 : Reserve	111 :Reserve

13.2 ADCSTR (ADC Start Convert and Setting Register)

ADCSTR Address = D3H Reset Value = 0000000B

ADC Start Convert and Setting Register

	SHCKS[1:0]		-----	BUSY	-----	-----	-----	START
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	X	R	X	X	X	W

SHCKS[1:0]	ADC sample and hold clock select : (SHCLK) 00 : 1MHz 01 : 500KHz 10 : 400KHz 11 : 333KHz
BUSY	ADC conversion busy flag : 0 : ADC conversion finish 1 : ADC conversion busy
START	ADC start conversion register : (write 1 only) 1 : ADC start conversion

13.3 ADCD1 (ADC Data Register 1)

ADCD1 Address = D5H Reset Value = 00000000B

ADC Data Register 1

	-----	-----	-----	-----	-----	-----	ADCD1.1	ADCD1.0
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

13.4 ADCD2 (ADC Data Register 2)

ADCD2 Address = D6H Reset Value = 00000000B

ADC Data Register 2

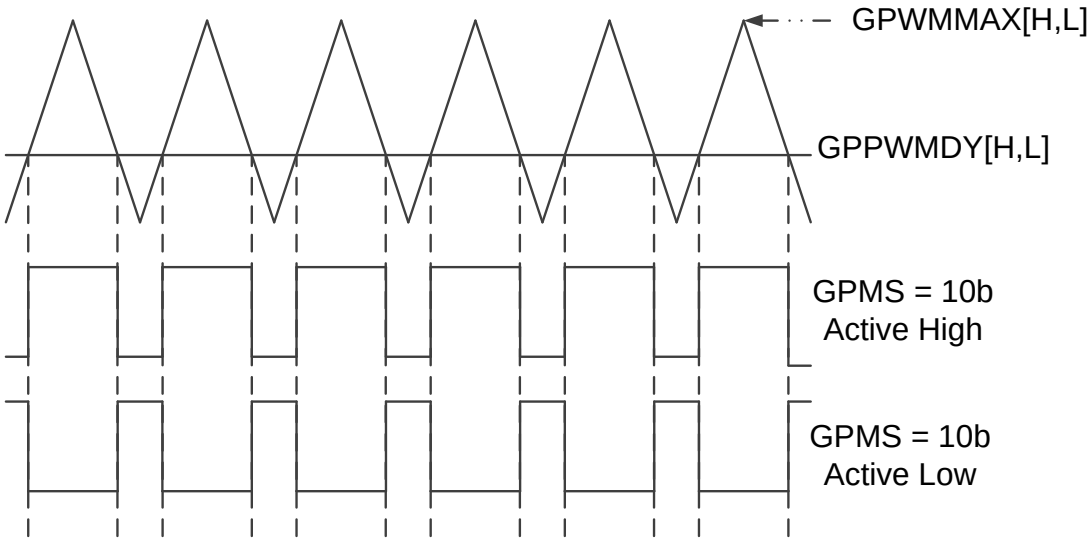
	ADCD2[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

14. General PWM (GPWM)

MDRHA0 have one16-bit general PWM output (**PINSET6**.4 = ‘1’) and six 11-bit PWM (compensation with Deadband) for Motor Controller.

GPWM is count up and down timer.(fixed)

SFR	Description	address	Reset value
GPWMCONT	General PWM Control Register	BAH	00H
GPWMMAXH	General PWM Max Register High	BCH	00H
GPWMMAXL	General PWM Max Register Low	BBH	02H
GPWMDYH	General PWM Duty Register High	BEH	FFH
GPWMDYL	General PWM Duty Register Low	BDH	FFH



14.1 GPWMCONT (General PWM Control Register)

GPWMCONT Address = BAH Reset Value = 00000000B

General PWM Control Register

	GPWMTR	GPMS[1:0]		-----	-----	-----	GPCKS[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	X	X	X	R/W	R/W

GPWMTR	GPWM timer run control : 0 : Stop 1: Run
GPMS[1:0] (SYNC)	GPWM output mode select 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low
GPCKS[1:0] (SYNC)	GPWM clock select : 00 : 48MHz 01 : 48MHz/2 10 : 48MHz/4 11 : 48MHz/8

14.2 GPWMMAX (General PWM Max Register)

GPWMMAXH (SYNC) Address = BCH Reset Value = 00000000B

General PWM Max Register High

	GPWMMAXH[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

GPWMMAXL (SYNC) Address = BBH Reset Value = 00000010B

General PWM Max Register Low

	GPWMMAXL[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

14.3 GPWMDY (General PWM Duty Register)

GPWMDYH (SYNC) Address = BEH Reset Value = 11111111B

General PWM Duty Register High

	GPWMDYH[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

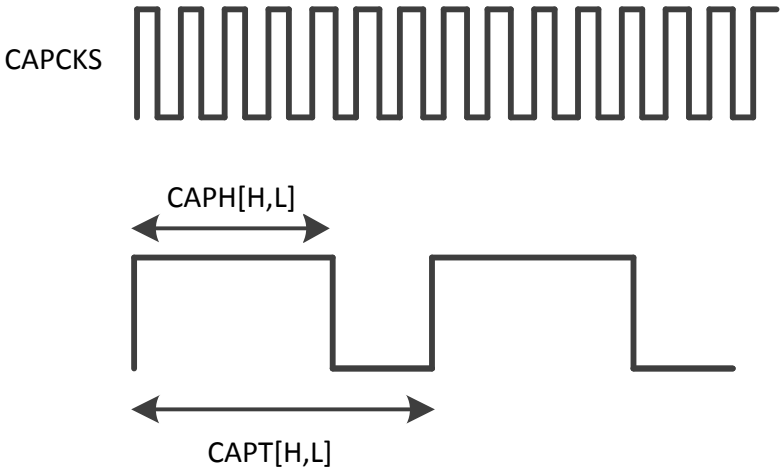
GPWMDYL (SYNC) Address = BDH Reset Value = 11111111B

General PWM Duty Register Low

	GPWMDYL[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15. Capture

SFR	Description	address	Reset value
CAPCONT	Capture Control Register	D8H	03H
CAPH_H	Capture High-level Count High	CBH	00H
CAPH_L	Capture High-level Count Low	CCH	00H
CAPT_H	Capture Total Count High	C9H	00H
CAPT_L	Capture Total Count Low	CAH	00H



15.1 CAPCONT (Capture Control Register)

CAPCONT Address = D8H Reset Value = 00000011B

Capture Control Register

	-----	-----	-----	CAPPINSEL	-----	CAPCKS[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R/W	X	R/W	R/W	R/W

CAPPINSEL Capture input pin select :

0 : disable //CAP2(PIN **CH7**)

1: CAP1(PIN**CH0**)

CAPCKS[2:0] Capture clock select :

000 : 48MHz/4	100 : 48MHz/64
001 : 48MHz/8	101 : 48MHz/128
010 : 48MHz/16	110 : 48MHz/256
011 : 48MHz/32	111 : 48MHz/512

15.2 CAPT (Capture Total Count)

CAPT_H Address = C9H Reset Value = 00000000B

Capture Total Count High

	CAPT[15:8]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

CAPT_L Address = CAH Reset Value = 00000000B

Capture Total Count Low

	CAPT[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

15.3 CAPH (Capture High-level Count)

CAPH_H Address = CBH Reset Value = 00000000B

Capture High-level Count High

	CAPH[15:8]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

CAPH_L Address = CCH Reset Value = 00000000B

Capture High-level Count Low

	CAPH[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

16. Addition and Subtraction Unit (ASU)

ASU provides 32-bit Addition and Subtraction calculation.

SFR	Description	address	Reset value
AS_MD_CONT	ASU and MDU Control Register	E1H	10H
ASUD1_1	ASU Data 1 byte 1	E8H	00H
ASUD1_2	ASU Data 1 byte 2	E9H	00H
ASUD1_3	ASU Data 1 byte 3	EAH	00H
ASUD1_4	ASU Data 1 byte 4	EBH	00H
ASUD2_1	ASU Data 2 byte 1	ECH	00H
ASUD2_2	ASU Data 2 byte 2	EDH	00H
ASUD2_3	ASU Data 2 byte 3	EEH	00H
ASUD2_4	ASU Data 2 byte 4	EFH	00H
ASUR1	ASU Result Register 1	DCH	00H
ASUR2	ASU Result Register 2	DDH	00H
ASUR3	ASU Result Register 3	DEH	00H
ASUR4	ASU Result Register 4	DFH	00H

	MSB			LSB
ASUD1	ASUD1_4	ASUD1_3	ASUD1_2	ASUD1_1
ASUD2	ASUD2_4	ASUD2_3	ASUD2_2	ASUD2_1
ASUR	ASUR4	ASUR3	ASUR2	ASUR1

Addition Calculation (AS_MD_CONT.0 = 0)	ASUR = ASUD1 + ASUD2	ASUR4 limit at 0x7F
Subtraction Calculation (AS_MD_CONT.0 = 1)	ASUR = ASUD1 – ASUD2	ASUR4 limit at 0x81

16.1 AS_MD_CONT (ASU and MDU Control Register)

AS_MD_CONT Address = E1H Reset Value = 00010000B

ASU and MDU Control Register

	-----	-----	-----	MDUF	-----	-----	MDUS	ASUS
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R	X	X	R/W	R/W

MDUF MDU finish flag :

0 : MDU busy.

1 : MDU calculation finished.

MDUS MDU Signed select :

0 :Signed calculation.

1 :Unsigned calculation.

ASUS ASU Subtraction select :

0 : Addition calculation.

1: Subtraction calculation.

16.2 ASUD1 (ASU Data 1)

ASUD1_1 Address = E8H Reset Value = 00000000B

	ASUD1_1[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUD1_2 Address = E9H Reset Value = 00000000B

	ASUD1_2[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUD1_3 Address = EAH Reset Value = 00000000B

	ASUD1_3[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUD1_4 Address = EBH Reset Value = 00000000B

	ASUD1_4[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.3 ASUD2 (ASU Data 2)

ASUD2_1 Address = ECH Reset Value = 00000000B

	ASUD2_1[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUD2_2 Address = EDH Reset Value = 00000000B

	ASUD2_2[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUD2_3 Address = EEH Reset Value = 00000000B

	ASUD2_3[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUD2_4 Address = EFH Reset Value = 00000000B

	ASUD2_4[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.4 ASUR (ASU Result Register)

ASUR1 Address = ECH Reset Value = 00000000B

	ASUR1[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUR2 Address = EDH Reset Value = 00000000B

	ASUR2[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUR3 Address = EEH Reset Value = 00000000B

	ASUR3[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASUR4 Address = EFH Reset Value = 00000000B

	ASUR4[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17. Multiplication and Division Unit (MDU)

The **MDU** is an on-chip arithmetic co-processor which enables the **MDRHA0** to perform additional extended arithmetic operations. All operations are singed/unsigned integer operations. Operands and results are stored in **MD0**–**MD5** registers. The module is controlled by the **AS_MD_CONT** and **MD_CONT** register. Any calculation of the **MDU** overwrites its operands. The **MDU** support five operations: Division 32-bit/16-bit, Division 16-bit/16-bit, Multiplication, Shift and Normalize.

SFR	Description	address	Reset value
AS_MD_CONT	ASU and MDU Control Register	E1H	10H
MD_CONT	MDU Control Register	DBH	00H
MD0	Multiplication Division Register 0	E2H	00H
MD1	Multiplication Division Register 1	E3H	00H
MD2	Multiplication Division Register 2	E4H	00H
MD3	Multiplication Division Register 3	E5H	00H
MD4	Multiplication Division Register 4	E6H	00H
MD5	Multiplication Division Register 5	E7H	00H

17.1 AS_MD_CONT (ASU and MDU Control Register)

AS_MD_CONT Address = E1H Reset Value = 00010000B

ASU and MDU Control Register

	-----	-----	-----	MDUF	-----	-----	MDUS	ASUS
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R	X	X	R/W	R/W

MDUF MDU finish flag :

0 : MDU busy.

1 : MDU calculation finished.

MDUS MDU Signed select :

0 :Signed calculation.

1 :Unsigned calculation.

ASUS ASU Subtraction select :

0 : Addition calculation.

1: Subtraction calculation.

17.2 MD_CONT (MDU Control Register)

MD_CONT Address = DBH Reset Value = 00010000B

MDU Control Register

	MDEF	MDOV	SLR	SC[4:0]				
Bit	7	6	5	4	3	2	1	0
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W

MDEF	MDU Error flag : Indicates an improperly performed operation (when one of the arithmetic operations has been restarted or interrupted by a new operation).
MDOV	MDU Overflow flag : Overflow occurrence in the MDU operation.
SLR	Shift direction : 0 : shift left operation 1 : shift right operation
SC[4:0]	Shift counter : When set to all ‘0‘s, normalize operation is selected. After normalization, the SC[4:0] contain the number of normalizing shifts performed. When at least one of these bit is set high shift operation is selected. The number of shifts performed is determined by the number written to SC[4:0], where SC.4 is the MSB.

17.2.1 MDEF

The **MDEF** error flag indicates an improperly performed operation (when one of the arithmetic operations has been restarted or interrupted by a new operation). The error flag mechanism is automatically enabled with the first write operation to **MD0**and disabled with the final read instruction from **MD3**(multiplication or shift/norm) or **MD5** (division) in phase three.

The error flag is set when:

There is a write access to MDx registers (any of **MD0**-**MD5** and **MD_CONT**) during phase two of **MDU** operation (restart or calculations interrupting) There is a read access to one of MDx registers during phase two of **MDU** operation when the error flag mechanism is enabled. In such condition error flag is set but the calculation is not interrupted. The error flag is reset only after read access to **MD_CONT** register. The error flag is read only.

17.2.2 MDOV

The **MDOV** overflow flag is set when one of the following conditions occurs: Division by zero

Multiplication with a result greater than FFFFH

Start of normalizing if the (‘**MD3**.7’ =‘1’)most significant bit of **MD3** is set

Any operation of the **MDU** that does not match the above conditions clears the overflow flag. Note that the overflow flag is exclusively controlled by hardware. It cannot be written.

17.3 MD0 – MD5 (Multiplication Division Register)

MD0 Address = E2H Reset Value = 00000000B

Multiplication Division Register 0

	MD0[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD1 Address = E3H Reset Value = 00000000B

Multiplication Division Register 1

	MD1[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD2 Address = E4H Reset Value = 00000000B

Multiplication Division Register 2

	MD2[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD3 Address = E5H Reset Value = 00000000B

Multiplication Division Register 3

	MD3[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD4	Address = E6H					Reset Value = 00000000B	
Multiplication Division Register 4							
MD4[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD5	Address = E7H					Reset Value = 00000000B	
Multiplication Division Register 5							
MD5[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.4 MDU Operation Description

The operation of the **MDU** consists of three phases:

17.4.1 Loading the MDx registers

The type of calculation the **MDU** has to perform is selected by the order in which the MDx registers are written to. A write to **MD0** is the first transfer to be done in any case. Next writes must be done as shown in the table below to determine the **MDU** operation. The last write will start the selected operation.

Operation	32-bit/16-bit	16-bit/-16bit	16-bit x 16-bit	Shift/ normalizing
First write	MD0 Dividend Low	MD0 Dividend Low	MD0 Multiplicand Low	MD0 LSB
	MD1 Dividend	MD1 Dividend High	MD4 Multiplicator Low	MD1
	MD2 Dividend		MD1 Multiplicand High	MD2
	MD3 Dividend High			MD3 MSB
	MD4 Divisor Low	MD4 Divisor Low		
Last write	MD5 Divisor High	MD5 Divisor High	MD5 Multiplicator High	MD_CONT start conversion

17.4.2 Executing calculation

During the calculation period, the **MDU** works in parallel to the CPU. When the calculation is complete, the hardware will set the **MDUF** bit to one (**MDUF** = '1'). The flag will be cleared at the next calculation.

The following table provides the execution time for each mathematical operation.

Operation	Number of clock cycles	
Division 32-bit/16-bit	17 clock cycles	
Division 16-bit/16-bit	9 clock cycles	
Multiplication	11 clock cycles	
Shift	Min 3 clock cycles (SC = 01H)	Max 18 clock cycles (SC = 1FH)
Normalize	Min 4 clock cycles (SC <= 01H)	Max 19 clock cycles (SC = 1FH)

17.4.3 Reading the result from the MDx registers

The Read-out sequence of the first "MDx" registers is not critical but the last read determines the end of a whole calculation.

Operation	32-bit/16-bit	16-bit/16-bit	16-bit x 16-bit	Shift/ normalizing
First read	MD0 Quotient Low	MD0 Quotient Low	MD0 Product Low	MD0 LSB
	MD1 Quotient	MD1 Quotient High	MD1 Product	MD1
	MD2 Quotient		MD2 Product	MD2
	MD3 Quotient High			
	MD4 Remainder Low	MD4 Remainder Low		
Last read	MD5 Remainder High	MD5 Remainder High	MD3 Product High	MD3 MSB

17.4.4 Shifting

In shift operation, 32-bit integer variable stored in **MD0** to **MD3**registers (the latter contains the most significant byte) is shifted left or right by a specified number of bits. The **SLR** bit (**MD_CONT**.5) defines the shift direction, and bits **SC**[4:0] (**MD_CONT**.4 – **MD_CONT**.0) specifies the shift count (which must not be 0). During shift operation, zeroes come into the left end of **MD3** for shifting right or right end of the **MD0** for shifting left.

17.4.5 Normalizing

All leading zeroes of 32-bit integer variable stored in **MD0** to **MD3** registers, the latter contains the most significant byte are removed by shift left operations. The whole operation is completed when the MSB (most significant bit) of **MD3** register contains a '1'. After normalizing, bits **SC**[4:0] (**MD_CONT**.4 –**MD_CONT**.0) contain the number of shift left operations, which were done.

18. Motor Controller(MOC)

18.1 HALL Interface

SFR	Description	address	Reset value
HALLDBT	Hall De-bounce Time Register	9CH	0EH
HALLSET1	Hall Setting Register 1	91H	45H
HALLSET2	Hall Setting Register 2	92H	26H
HALLSET3	Hall Setting Register 3	93H	13H
HALLST	Hall Status Register	94H	XXH
ROTORSPEEDH	Rotor Speed Count Register High	97H	FFH
ROTORSPEEDL	Rotor Speed Count Register Low	96H	FFH
VRHALL	Virtual Hall Register	D9H	05H

MCONT1 Address = 9DH Reset Value = X0110000B

Motor Control Register 1

	-----	HCKS[2:0]			HALLALS	DMS	MPWMA	AMDS
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

HCKS[2:0] Hall clock select :

000 : 48MHz/4

001 : 48MHz/8

010 : 48MHz/16

011 : 48MHz/32

100 : 48MHz/64

101 : 48MHz/128

110 : 48MHz/256

111 : 48MHz/512

HALLALS Hall alignment select :

0 : Line voltage (Line to Line)

1 : Phase voltage

DMS Driving mode select :

0 : 120° Square-Wave

1 : Sin-Wave

MPWMA MPWM auto mode :

0 : Disable. (control by firmware)

1 : Enable. (control by MOC)

AMDS Auto mode direction select :

0 : When MPWMA = '1', driving direction is forward.

1 : When MPWMA = '1', driving direction is reverse.

MCONT2 Address = A2H Reset Value = 00000000B

Motor Control Register 2

	MPWMTR	-----			-----	VRHS	AOCPS	-----
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	X	X	X	R/W	R/W	X

MPWMTR	MPWM timer run control : 0 : Stop 1 : Run
VRHS	Virtual Hall select : 0 : Real Hall. (HALL U, HALL V, HALL W) 1 : Virtual Hall.
AOCPS	Analog OCP select : 0 : Digital OCP 1 : Analog OCP

18.1.1 HALLDBT (Hall De-bounce Time Register)

HALLDBT Address = 9CH Reset Value = 00001110B

Hall De-bounce Time Register

	-----	-----	HALLDBT[5:0]					
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

HALLDBT is use to filter the HALL signal.

De-bounce time = $\frac{1}{\frac{48MHz}{16}} \times \mathrm{HALLDBT}[5:0]$

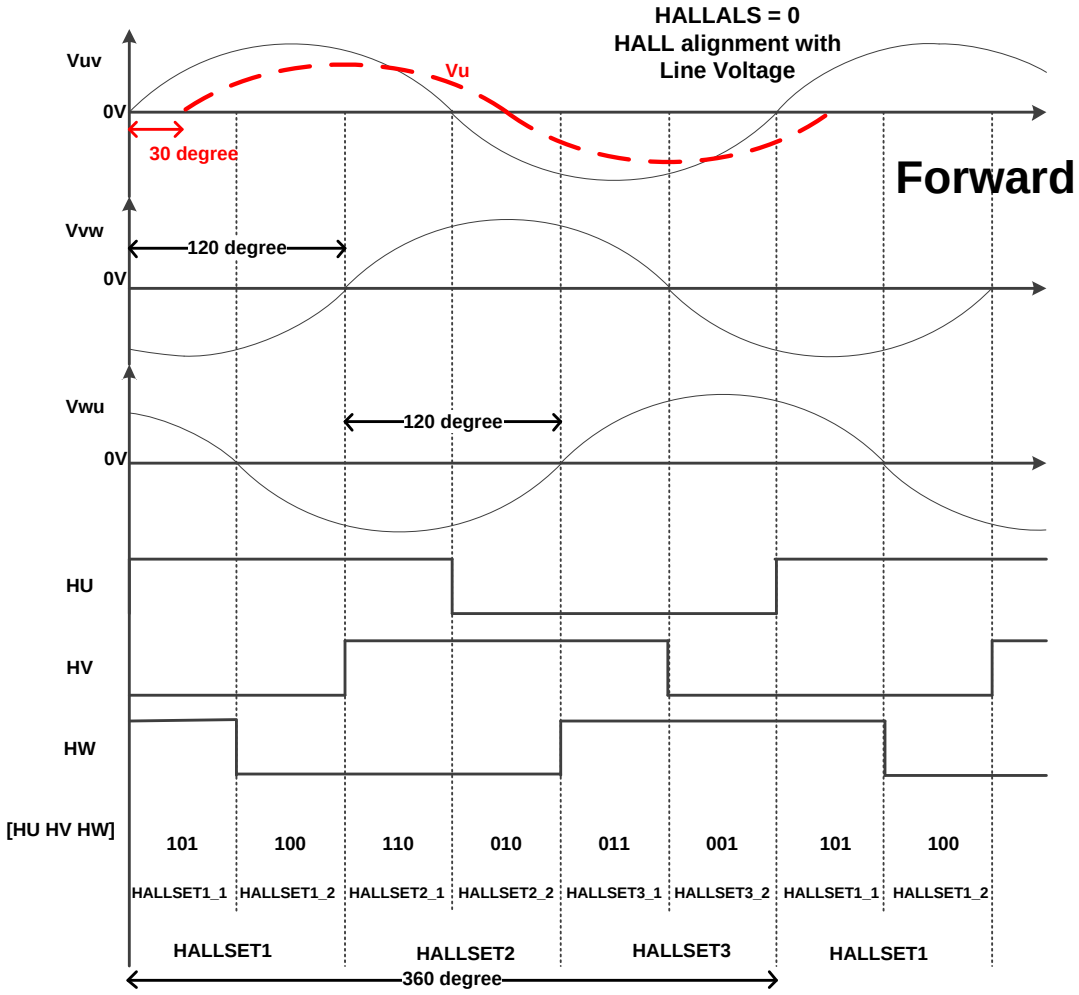
18.1.2 HALLSET (Hall Setting Register 1, 2, 3)

HALLSET define forward direction HALL sequence.

♤Hall alignment select HALLALS = 0 (MCONT1)

Line Voltage(Line to Line) sequence is *Vuv leads* Vvw by *120 degrees* and Vvw *leads Vwu* by *120 degrees.(Forward direction define in MDRHA0)*

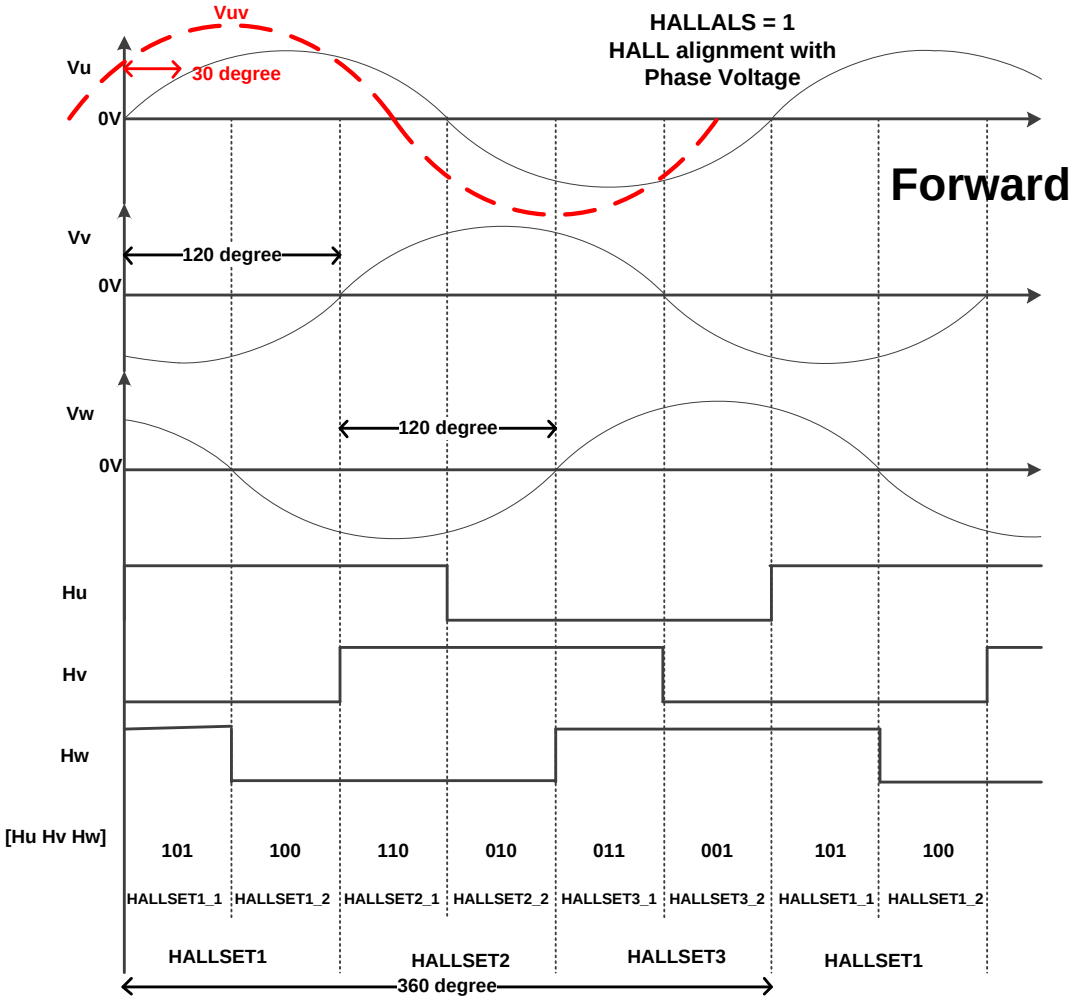
Hall signal is alignment with Line Voltage.



⎚ Hall alignment select HALLALS = 1 (MCONT1)

Phase Voltage sequence is *Vu leads Vv* by *120 degrees* and Vv *leads Vw* by *120 degrees. (Forward direction define in MDRHA0)*

Hall signal is alignment with Phase *Voltage.*



HALLSET1 (SYNC) Address = 91H Reset Value = 01000101B

Hall Setting Register 1

	-----	HALLSET1_2[2:0]			-----	HALLSET1_1[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	X	R/W	R/W	R/W

[2] : HALL U status. [1] : HALL V status. [0] : HALL W status.

HALLSET2 (SYNC) Address = 92H Reset Value = 00100110B

Hall Setting Register 2

	-----	HALLSET2_2 [2:0]			-----	HALLSET2_1[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	X	R/W	R/W	R/W

[2] : HALL U status. [1] : HALL V status. [0] : HALL W status.

HALLSET3 (SYNC) Address = 93H Reset Value = 00010011B

Hall Setting Register 3

	-----	HALLSET3_2[2:0]			-----	HALLSET3_1[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	X	R/W	R/W	R/W

[2] : HALL U status. [1] : HALL V status. [0] : HALL W status.

18.1.3 HALLST (Hall Status Register)

HALLST Address = 94H Reset Value = xxxxxxxxB

Hall Status Register

	-----	H_OLD[2:0]			-----	H_NEW[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	R	R	R	X	R	R	R

H_OLD[2:0]	Hall old status : [2] : HALL U status. [1] : HALL V status. [0] : HALL W status.
H_NEW[2:0]	Hall new status : [2] : HALL U status. [1] : HALL V status. [0] : HALL W status.

18.1.4 ROTORSPEED (Rotor Speed Count Register)

ROTORSPEED is a 16-bit counter (counter is limit at FFFFH). Clock source is depends on **HCKS**(**MCONT1** reg.). The counter input is HALLU.

ROTORSPEEDH Address = 97H Reset Value = 11111111B

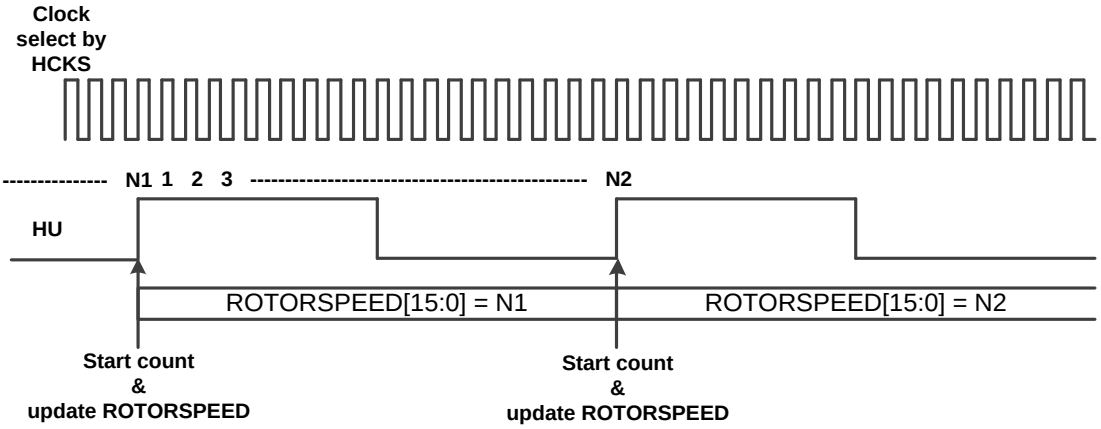
Rotor Speed Count Register High

	ROTORSPEED[15:8]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

ROTORSPEEDL Address = 96H Reset Value = 11111111B

Rotor Speed Count Register Low

	ROTORSPEED[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R



18.1.5 VRHALL (Virtual Hall Register)

VRHALL Address = D9H Reset Value = 00000101B

Virtual Hall Register

	-----	-----	-----	-----	-----	VRH[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

VRH[2:0] Virtual Hall value.

VRH.2 is Virtual HALL U.

VRH.1 is Virtual HALL V.

VRH.0 is Virtual HALL W.

18.2 Motor PWM Engine

MPWM is count up and down timer. (fixed)

SFR	Description	address	Reset value
MCONT1	Motor Control Register 1	9DH	X011 0000B
MCONT2	Motor Control Register 2	A2H	00H
MPWMMAXH	Motor PWM Max Register High	A4H	00H
MPWMMAXL	Motor PWM Max Register Low	A3H	02H
MPWMDYUH	Motor PWM Duty Register U High (Phase U)	A6H	07H
MPWMDYUL	Motor PWM Duty Register U Low (Phase U)	A5H	FFH
MPWMDYVH	Motor PWM Duty Register V High (Phase V)	ABH	07H
MPWMDYVL	Motor PWM Duty Register V Low (Phase V)	AAH	FFH
MPWMDYWH	Motor PWM Duty Register W High (Phase W)	AEH	07H
MPWMDYWL	Motor PWM Duty Register W Low (Phase W)	ADH	FFH
MPWMDB	Motor PWM Deadband Register	A7H	00H
MPWMCONT1	MPWM Control Register 1	B1H	00H
MPWMCONT2	MPWM Control Register 2	B2H	00H
MPWMINV	MPWM Inverse Selection Register	B3H	00H

18.2.1 MCONT1 (Motor Control Register 1)

MCONT1 Address = 9DH Reset Value = X0110000B

Motor Control Register 1

	-----	HCKS[2:0]			HALLALS	DMS	MPWMA	AMDS
Bit	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

HCKS[2:0]	Hall clock select : 000 : 48MHz/4 001 : 48MHz/8 010 : 48MHz/16 011 : 48MHz/32 100 : 48MHz/64 101 : 48MHz/128 110 : 48MHz/256 111 : 48MHz/512
HALLALS	Hall alignment select : 0 : Line voltage (Line to Line) 1 : Phase voltage
DMS	Driving mode select : 0 : 120° Square-Wave 1 : Sin-Wave
MPWMA	MPWM auto mode : 0 : Disable. (control by firmware) 1 : Enable. (control by MOC)
AMDS	Auto mode direction select : 0 : When MPWMA = ‘1’, driving direction is forward. 1 : When MPWMA = ‘1’, driving direction is reverse.

18.2.2 MCONT2 (Motor Control Register 2)

MCONT2 Address = A2H Reset Value = 00000000B

Motor Control Register 2

	MPWMTR	-----			-----	VRHS	AOCPS	-----
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	X	X	X	R/W	R/W	X

MPWMTR	MPWM timer run control : 0 : Stop 1 : Run
VRHS	Virtual Hall select : 0 : Real Hall. (HALL U, HALL V, HALL W) 1 : Virtual Hall.
AOCPS	Analog OCP select : 0 : Digital OCP 1 : Analog OCP

18.2.3MPWMMAX (Motor PWM Max Register)

MPWM is 11-bit timer. The frequency of MPWM timer is 48MHz. (fixed)

MPWM is count up and down timer. (fixed)

MPWMMAXH (SYNC) Address = A4H Reset Value = 00000000B

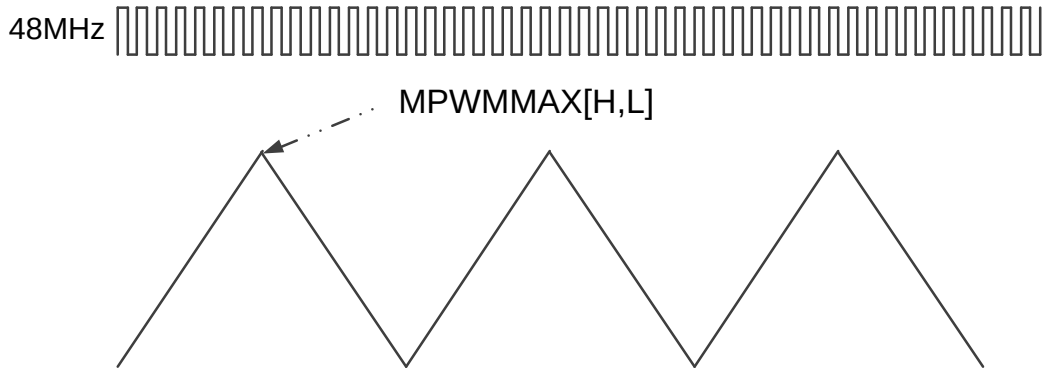
Motor PWM Max Register High

	-----	-----	-----	-----	-----	MPWMMAX[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

MPWMMAXL (SYNC) Address = A3H Reset Value = 00000010B

Motor PWM Max Register Low

	MPWMMAX[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W



18.2.4MPWMDY (Motor PWM Duty Register)

MPWM is 11-bit timer.

MPWMDYU is phase U PWM duty. MPWMDYV is phase V PWM duty. MPWMDYW is phase W PWM duty.

MPWMDYUH (SYNC) Address = A6H Reset Value = 00000111B

Motor PWM Duty Register U High (Phase U)

	-----	-----	-----	-----	-----	MPWMDYU[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

MPWMDYUL (SYNC) Address = A5H Reset Value = 11111111B

Motor PWM Duty Register U Low (Phase U)

	MPWMDYU[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MPWMDYVH (SYNC) Address = ABH Reset Value = 00000111B

Motor PWM Duty Register V High (Phase V)

	-----	-----	-----	-----	-----	MPWMDYV[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

MPWMDYVL (SYNC) Address = AAH Reset Value = 11111111B

Motor PWM Duty Register V Low (Phase V)

	MPWMDYV[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MPWMDYWH (SYNC) Address = AEH Reset Value = 00000111B

Motor PWM Duty Register W High (Phase W)

	-----	-----	-----	-----	-----	MPWMDYW[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

MPWMDYWL (SYNC) Address = ADH Reset Value = 11111111B

Motor PWM Duty Register W Low (Phase W)

	MPWMDYW[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

18.2.5MPWMDB (Motor PWM Deadband Register)

Compensation PWM output with Deadband is use to prevent short-though between high-side and low-side power device.

The frequency of **MPWMDB** is 48MHz. (fixed)

MPWMDB (SYNC) Address = A7H Reset Value = 00000000B

Motor PWM Deadband Register

	MPWMDB[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

18.2.6 MPWMCONT1 (MPWM Control Register 1)

Motor High-side PWM output mode select:

MPWMCONT1 (SYNC) Address = B1H Reset Value = 00000000B

MPWM Control Register 1

	-----	-----	PWMW[1:0]		PWMV[1:0]		PWMU[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

PWMW	Phase W High-side (W) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low
PWMV	Phase V High-side (V) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low
PWMU	Phase U High-side (U) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low

18.2.7 MPWMCONT2 (MPWM Control Register 2)

Motor Low-side PWM output mode select:

MPWMCONT2 (SYNC) Address = B2H Reset Value = 00000000B

MPWM Control Register 2

	-----	-----	PWMZ[1:0]		PWMY[1:0]		PWMX[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

PWMZ	Phase W Low-side (Z) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low
PWMY	Phase V Low-side (Y) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low
PWMX	Phase U Low-side (X) output mode select : 00 : Force Low 01 : Force High 10 : Active High 11 : Active Low

18.2.8 MPWMINV (MPWM Inverse Selection Register)

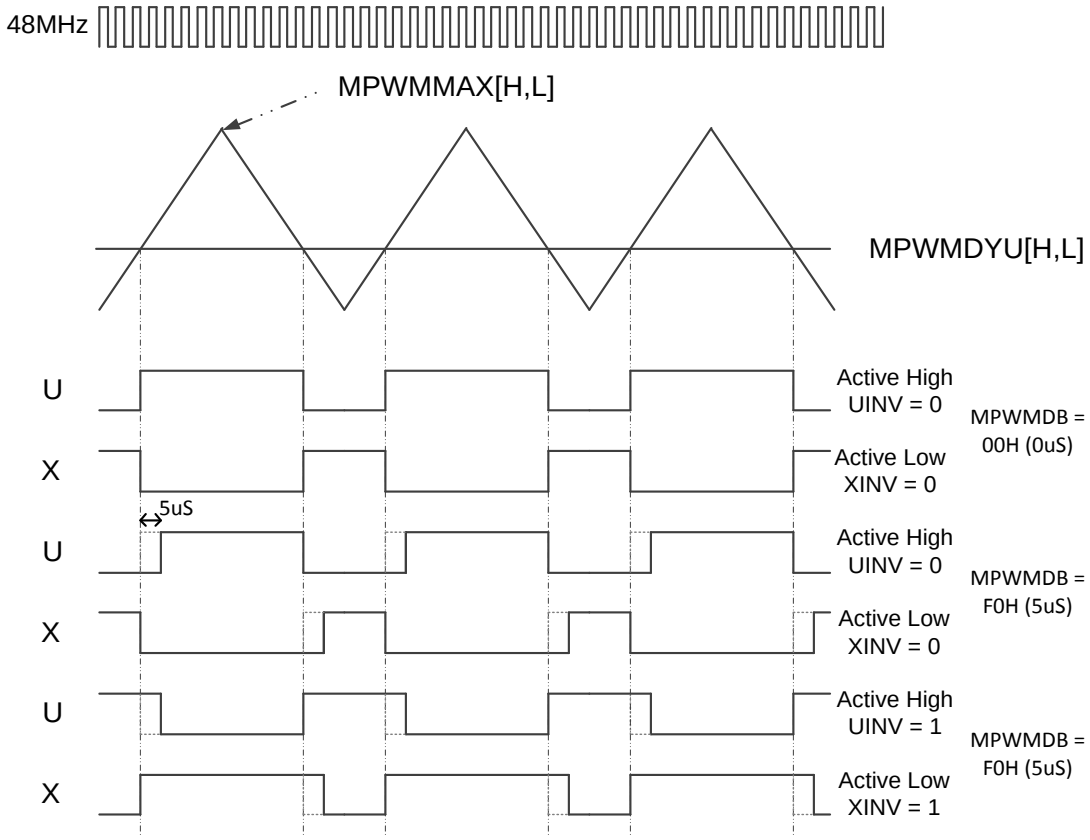
Motor six PWM output Inverse select:

MPWMINV(SYNC) Address = B3H Reset Value = 00000000B

MPWM Inverse Selection Register

	-----	-----	ZINV	WINV	YINV	VINV	XINV	UINV
Bit	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

ZINV	Low-side PWM Z output inverse select : 0 : Non-inverse 1 : Inverse
WINV	High-side PWM W output inverse select : 0 : Non-inverse 1 : Inverse
YINV	Low-side PWM Y output inverse select : 0 : Non-inverse 1 : Inverse
VINV	High-side PWM V output inverse select : 0 : Non-inverse 1 : Inverse
XINV	Low-side PWM X output inverse select : 0 : Non-inverse 1 : Inverse
UINV	High-side PWM U output inverse select : 0 : Non-inverse 1 : Inverse


48MHz
MPWMMAX[H,L]
MPWMDYU[H,L]
U
X
U
X
U
X
5uS
Active High
UINV = 0
Active Low
XINV = 0
Active High
UINV = 0
Active Low
XINV = 0
Active High
UINV = 1
Active Low
XINV = 1
MPWMDB =
00H (0uS)
MPWMDB =
F0H (5uS)
MPWMDB =
F0H (5uS)

18.3 Space Vector PWM (SVPWM)

SFR	Description	address	Reset value
SVPWMAMPH	SVPWM Amplitude Register High	C4H	00H
SVPWMAMPL	SVPWM Amplitude Register Low	C3H	00H
SVPWMAMPFT	SVPWM Amplitude Fine-Tune Register	DAH	00H
SVPWMANG	SVPWM Angle Register	C1H	00H
AS	Angle Shift Control Register	8FH	00H

18.3.1 SVPWMAMP (SVPWM Amplitude Register)

SVPWMAMP is control by user.

SVPWMAMPH(SYNC) Address = C4H Reset Value = 00000000B

SVPWM Amplitude Register High

	-----	-----	-----	-----	-----	SVPWMAMP[10:8]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

SVPWMAMPL(SYNC) Address = C3H Reset Value = 00000000B

SVPWM Amplitude Register Low

	SVPWMAMP[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

18.3.2 SVPWMAMPFT (SVPWM Amplitude Fine-Tune Register)

SVPWMAMPFT Address = DAH Reset Value = 00000000B

SVPWM Amplitude Fine-Tune Register

	-----	-----	-----	-----	-----	SVPWMAMPFT[2:0]		
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	R/W	R/W	R/W

18.3.3 SVPWMANG (SVPWM Angle Register)

1.875∘/bit

0∘~ 358.125∘= 0~191(**SVPWMANG**)

When **MWPMA** = '1' (auto mode), **SVPWMANG** is control by **MOC**.

When **MWPMA** = '0', **SVPWMANG** is control by user.

SVPWMANG Address = C1H Reset Value = 00000000B

SVPWM Angle Register

	SVPWMANG[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

18.3.4 AS (Angle Shift Control Register)

AS is used to compensate phase lag between current and voltage

1.875∘/bit

When **MWPMA** = '1' (auto mode), **AS** is active. Control by user.

AS (SYNC) Address = 8FH Reset Value = 00000000B

Angle Shift Control Register

	AS_LS	-----	-----	AS_VALUE[4:0]				
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	X	R/W	R/W	R/W	R/W	R/W

AS_LS	Angle Shift Lag select: 0 : 0° ~58.125° = 0~ 31(AS_VALUE) 1 : 0° ~-58.125° = 0~ 31(AS_VALUE)

18.4 Over Current Protect (OCP)

MCONT2 Address = A2H Reset Value = 00000000B

Motor Control Register 2

	MPWMTR	-----			-----	VRHS	AOCPS	-----
Bit	7	6	5	4	3	2	1	0
Type	R/W	X	X	X	X	R/W	R/W	X

MPWMTR	MPWM timer run control : 0 : Stop 1 : Run
VRHS	Virtual Hall select : 0 : Real Hall. (HALL A, HALL B, HALL C) 1 : Virtual Hall.
AOCPS	Analog OCP select : 0 : Digital OCP 1 : Analog OCP

OCPCONT Address = A1H Reset Value = 00000100B

OCP Control Register

	OCPST	OCPDBT[4:0]					OCPC	OCPMS
Bit	7	6	5	4	3	2	1	0
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OCPST	OCP Short status: 0 : No Over current Short 1 : Over current Short occur. (hardware set OCPC = '0') Six PWM output is high-impedance.
OCPDBT[4:0]	PIN OCP input de-bounce time (default 41.67nS) 0~31 = 0~1.291uS (48MHz/2 fixed)
OCPC	OCP status clear bit : When OCP is occur, hard ware will set OCPC = '0'. In User mode, user can write '1' to clear OCP status, the PWM will output at next PWM cycle.
OCPMS	OCP mode select : 0 : Auto mode 1: User mode

AOCPCONT Address = 9EH Reset Value = 00001111B

Analog OCP Control Register

	OCPLT	-----	-----	I_LIMIT[2:0]			I_SHORT[1:0]	
Bit	7	6	5	4	3	2	1	0
Type	R	X	X	R/W	R/W	R/W	R/W	R/W

OCPLT	OCP Limit status 0 : No Over current Limit. 1 : Over current Limit occur.
I_LIMIT[2:0]	OCP LIMIT level select : (OCPLIF) 000 : 0.15V 001 : 0.2V 010 : 0.25V 011 : 0.3V (default) 100 : 0.35V 101 : 0.4V 110 : 0.45V 111 : 0.5V
I_SHORT[1:0]	OCP SHORT level select : (OCPSIF) 00 : 0.2V 01 : 0.3V 10 : 0.4V 11 : 0.5V (default)

18.5 SYNC

MOC behavior is synchronized with **MPWM**, many **MOC** SFRs have **shadow register** that is used to update these SFRs at the same time with **SYNC** register. Write **SYNC** any value will synchronization update these SFRs at the same time.

SYNC Address = D7H Reset Value = 00000000B

MOC Sync Register

	SYNC[7:0]							
Bit	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

Write only.

Shadow register: (need **SYNC**)

HALLSET1
HALLSET2
HALLSET3
AS
MPWMMAXH, MPWMMAXL
MPWMDYUH, MPWMDYUL
MPWMDYVH, MPWMDYVL
MPWMDYWH, MPWMDYWL
MPWMDB
MPWMINV
MPWMCONT1
MPWMCONT2
GPWMMAX
GPWMDY
GPWMOCNT.GPMS, GPWMOCNT.GPCT, GPWMOCNT.GPCKS
SVPWMAMP

19. HV Gate-Driver Function Description

19.1 Low Side Power Supply (VCC15, SGND, PGND)

VCC15 is the low side supply and it provides power to both input logic and low side output power stage.

The built-in under-voltage lockout circuit enables the device to operate at sufficient power on when a typical VCC15 supply voltage higher than VCCUV+ =4.2 is present, shown as Figure 19.1.1. The IC shuts down all the gate drivers outputs, when the VCC15 supply voltage is below VCCUV- =3.8 V, shown as Figure 19.1.1. This prevents the external power devices from extremely low gate voltage levels during on-state and therefore from excessive power dissipation.

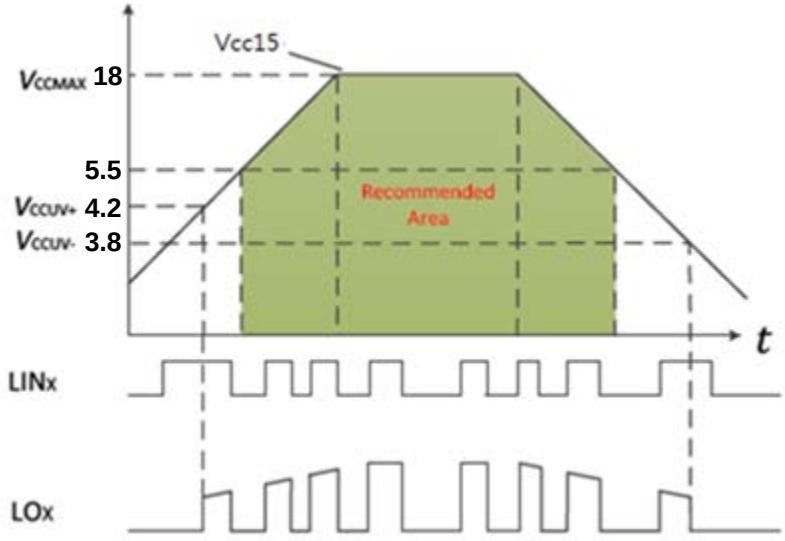


Figure 19.1.1 VCC15 supply UVLO operating area

19.2High Side Power Supply (VBU-VSU, VBU-VSU, VBU-VSU)

VB to VS is the high side supply voltage. The totally high side circuitry can float with respect to PGND following the external high side power device emitter/source voltage. Due to the internally low power consumption, the whole high side circuitry can be supplied by bootstrap topology connected to VCC15, and it can be powered with small bootstrap capacitors.

The device operating area as a function of the supply voltage is given in Figure 19.2.1.

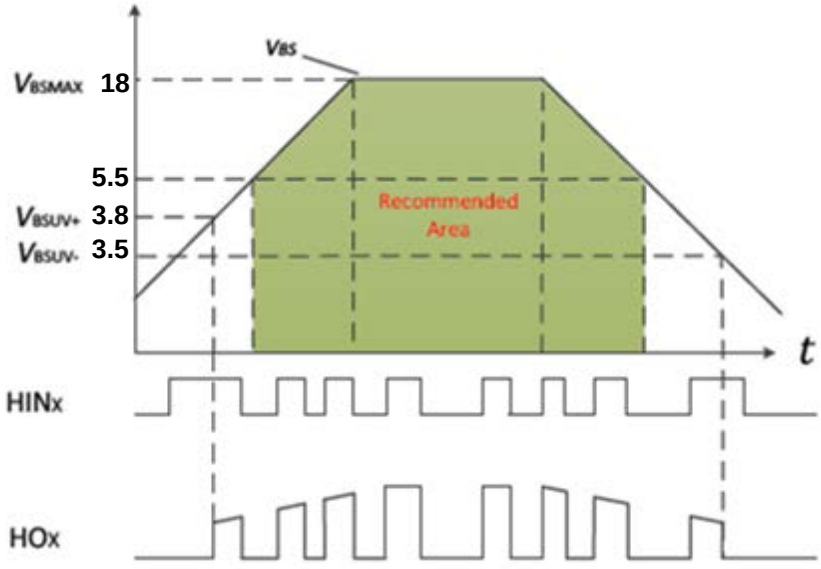


Figure 19.2.1 VBS supply UVLO operating area

19.3 Low Side and High Control Input Logic (HU,V,W / LU,V,W)

The Schmitt trigger threshold of each input is designed enough low such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Input Schmitt trigger and advanced noise filter provide beneficial noise rejection to short input pulses. An internal pull-down resistor of about 100k (positive logic) pre-biases each input during VCC15 supply start-up state. It is anyway recommended for proper work of the driver not to provide input pulse-width lower than 300ns.

19.4 Shoot-Through Prevention

The IC is equipped with shoot-through prevention circuitry (also known as cross conduction prevention circuitry). Figure 19.4.1 shows how this prevention circuitry prevents both the high-side and low-side switches from conducting at the same time. During the inputs controlling high side driver and low side driver are both “high”, the both driver outputs are pulled down “low” to shutdown two power devices in the same bridge.

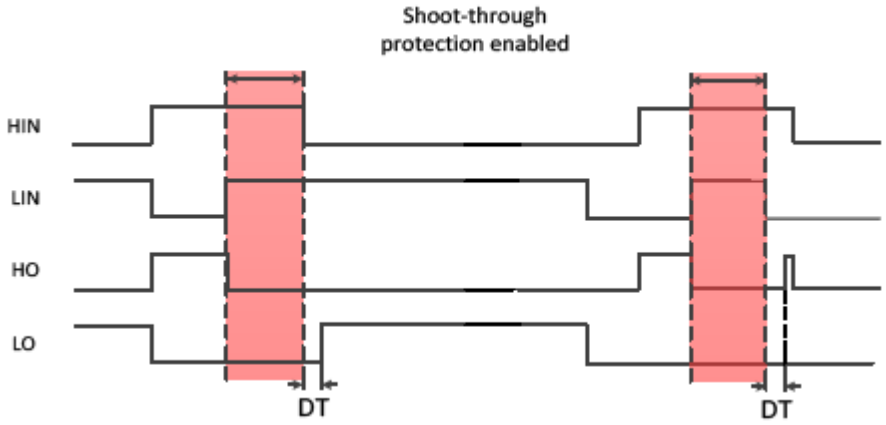


Figure 19.4.1 Shoot-through prevention

19.5 Dead-Time

The IC features integrated a fixed dead-time protection circuitry. The dead time feature inserts a time period (a minimum dead time) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum dead time is automatically inserted whenever the external dead time is shorter than DT; external dead times larger than DT are not modified by the gate driver. Figure 19.5.1 illustrates the dead time period and the relationship between the output gate signals.

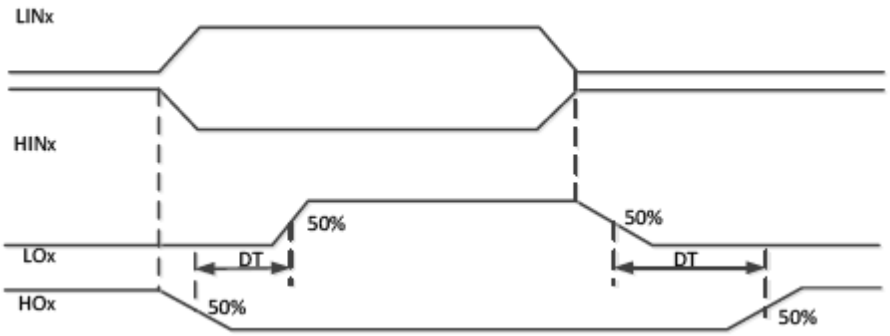


Figure 19.5.1 Dead Time

19.6 Gate Driver (HOU,V,W, LOU,V,W)

Low side and high side driver outputs are specifically designed for pulse operation and dedicated to drive the power devices such as IGBT and MOSFET. Low side outputs (i.e. LOU, V, W) are state triggered by the respective inputs, while high side outputs (i.e. HOU, V, W) are only changed at the edge of the respective inputs. In particular, after releasing from an under voltage condition of the V_{BS} supply, a new turn-on signal (edge) is necessary to activate the respective high side output, while after releasing from a under voltage condition of the VCC15 supply, the low side outputs can directly switch to the state of their respective inputs and don't suffer from the trouble as high side driver.

19.7 Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device or make the function abnormal. All the voltage parameters are absolute voltages referenced to IC PGND unless otherwise stated in the table.

Parameter	Symbol	Min.	Max.	Units
High-side floating supply voltage	$V_{B.U.V.W}$	-3	118	V
High-side offset voltage	$V_{S.U.V.W}$	-3	100	
High-side gate driver output voltage	$V_{HO.U.V.W}$	$V_{S.U.V.W}$ -0.3	$V_{B.U.V.W}$ +0.3	
Low-side gate driver output voltage	$V_{LO.U.V.W}$	PGND-0.3	VCC15+0.3	
Low-side supply voltage	VCC15	5.5	18	
Allowable Offset Voltage Slew Rate	dV/dt		50	V/ns

19.8 Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
High-side floating supply voltage	$V_{B.U.V.W}$	$V_{S.U.V.W}$ +5.5	$V_{S.U.V.W}$ -+18	V
High-side offset voltage	$V_{S.U.V.W}$	-1	100	
High-side gate driver output voltage	$V_{HO.U.V.W}$	$V_{S.U.V.W}$	$V_{B.U.V.W}$	
Low-side gate driver output voltage	$V_{LO.U.V.W}$	PGND	VCC15	
Low-side supply voltage	VCC15	5.5	18	
Allowable Offset Voltage Slew Rate	dV/dt		50	V/ns

Note1: For VBS=15V, normal Logic operation for VS of –6 V to 100 V. The parameter is only guaranteed by design.

19.9 Static Electrical Characteristics

（VCC15-SGND）=(V_B-V_S)=15V. TAMB=25℃unless otherwise specified. The VIN, VTH and IIN Parameters are reference to PGND and are applicable to all six channels. The V_O and I_O parameters are referenced to respective VS and PGND and are applicable to the respective output leads. The V_{CCUV} parameters are referenced to PGND. The V_{BSUV} parameters are referenced to V_S.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Low Side Power Supply Characteristics						
VCC15 quiescent current	I_{QVCC}	$V_{H.U.V.W}$ =$V_{L.U.V.W}$=0 or 5V	-	400	600	μA
VCC15 operating VCC15 supply current	I_{VCCOP}	$f_{L.U.V.W}$=20k, $f_{H.U.V.W}$=20k,	-	1500	-	
VCC15 supply under-voltage positive going threshold	V_{CCUV+}		-	4.2	-	V
VCC15 supply under-voltage negative going threshold	V_{CCUV-}		-	3.8	-	
VCC15supply under-voltage lockout hysteresis	V_{CCHYS}		-	0.4	-	
High Side Floating Power Supply Characteristics						
High side VBS supply under-voltage positive going threshold	V_{BSUV+}		-	3.8	-	V
High side VBS supply under-voltage negative going threshold	V_{BSUV-}		-	3.5	-	
High side VBS supply under-voltage lockout hysteresis	$V_{BSUVHYS}$		-	0.3	-	
High side VBS quiescent current	I_{QBS}	V_{BS}=15V	-	45	200	μA
Offset supply leakage current	I_{LK}	V_B=V_S=100V VCC15=0V	-	-	10	
Gate Driver Output Section						
High Side Output High Short-Circuit Pulse Current	I_{HO+}		-	1.2	-	A
High Side Output Low Short-Circuit Pulse Current	I_{HO-}		-	2.0	-	
Low Side Output High Short-Circuit Pulse Current	I_{LO+}		-	1.2	-	
Low Side Output Low Short-Circuit Pulse Current	I_{LO-}		-	2.0	-	

19.10 Dynamic Electrical Characteristics

（ VCC15-SGND ）=(V_B-V_S)=15 ,Vs.u.v.w=SGND=PGND, and C_{load}=1nF unless otherwise specified, T_{AMB}=25℃.

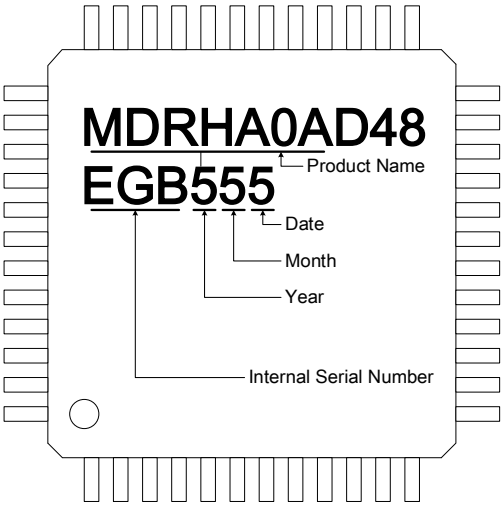
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn-On propagation delay	t_{ON}	$V_{H.U.V.W}$ or $V_{L.U.V.W}$=5V, $V_{S.U.V.W}$=0	-	120	200	ns
Turn-Off Propagation delay	t_{OFF}	$V_{H.U.V.W}$ or $V_{L.U.V.W}$=0, $V_{S.U.V.W}$=0	-	120	200	
Turn-On Rise time	t_R	$V_{H.U.V.W}$ or $V_{L.U.V.W}$=5V, $V_{S.U.V.W}$=0	-	20	-	
Turn-Off Fall time	t_F	$V_{H.U.V.W}$ or $V_{L.U.V.W}$=0, $V_{S.U.V.W}$=0	-	10	-	
Dead Time	DT		-	500	700	
Dead-Time Matching(All Six Channels)	MDT		-	-	50	
Delay Matching(All Six Channels)	MT		-	-	50	

20. Package Information

LQFP48 7x7mm(AA2) Outline Dimensions

21. Marking Distinguish

21.1 Standard Ink (w/o code)



21.2 Customization Ink (with customization code)

21.3 Production Date Code Rule

Year									
2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
5	6	7	8	9	0	1	2	3	4

Month										
Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
1	2	3	4	5	6	7	8	9	A	B	C

Date									
1	2	3	4	5	6	7	8	9	10
1	2	3	4	5	6	7	8	9	A
11	12	13	14	15	16	17	18	19	20
B	C	D	E	F	G	H	J	K	L
21	22	23	24	25	26	27	28	29	30
M	N	P	R	S	T	U	V	W	X
31									
Y									

22. Ordering Information

22.1 Standard Product Name

M	DRH	05	AD48
megawin	*Product Name*	*Voltage*	*Package LQFP-48*

22.2 Customization Product Name

- With customization code, produce by order.

M	DRH	05	AD48	–	XXXXX
megawin	*Product Name*	*Voltage*	*Package LQFP-48*		*Customization Code NO.*

23. Revision History

Update Date	Version	Modify content
2020.11	V0.1	Initial issue.