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8051-Based MCU

MDRFD0
Data Sheet

8Bit Single-Chip Microcontroller
Embedded 600V 3-Phase Gate-Driver

Version: V1.6

Features

Motor Controller (MOC)

- Estimated Angle Phase Lock Loop (PLL)
- Field Oriental Control (FOC) Square-Wave Solutions
- Slide Mode Rotor Position Estimated (SMO)
- Space Vector PWM (SVPWM)
- Supports Digital OCP and Analog OCP (Over Current Protection)
- Supports Initial Angle Estimated (IAE)
- Programmable Dead-band

Gate Driver

- Integrated 600V 3-phase gate-driver
- Shoot-through protection
- Under voltage lockout for VCC15 and VBS
- Built-in 15V/5V LDO

Embedded MCU

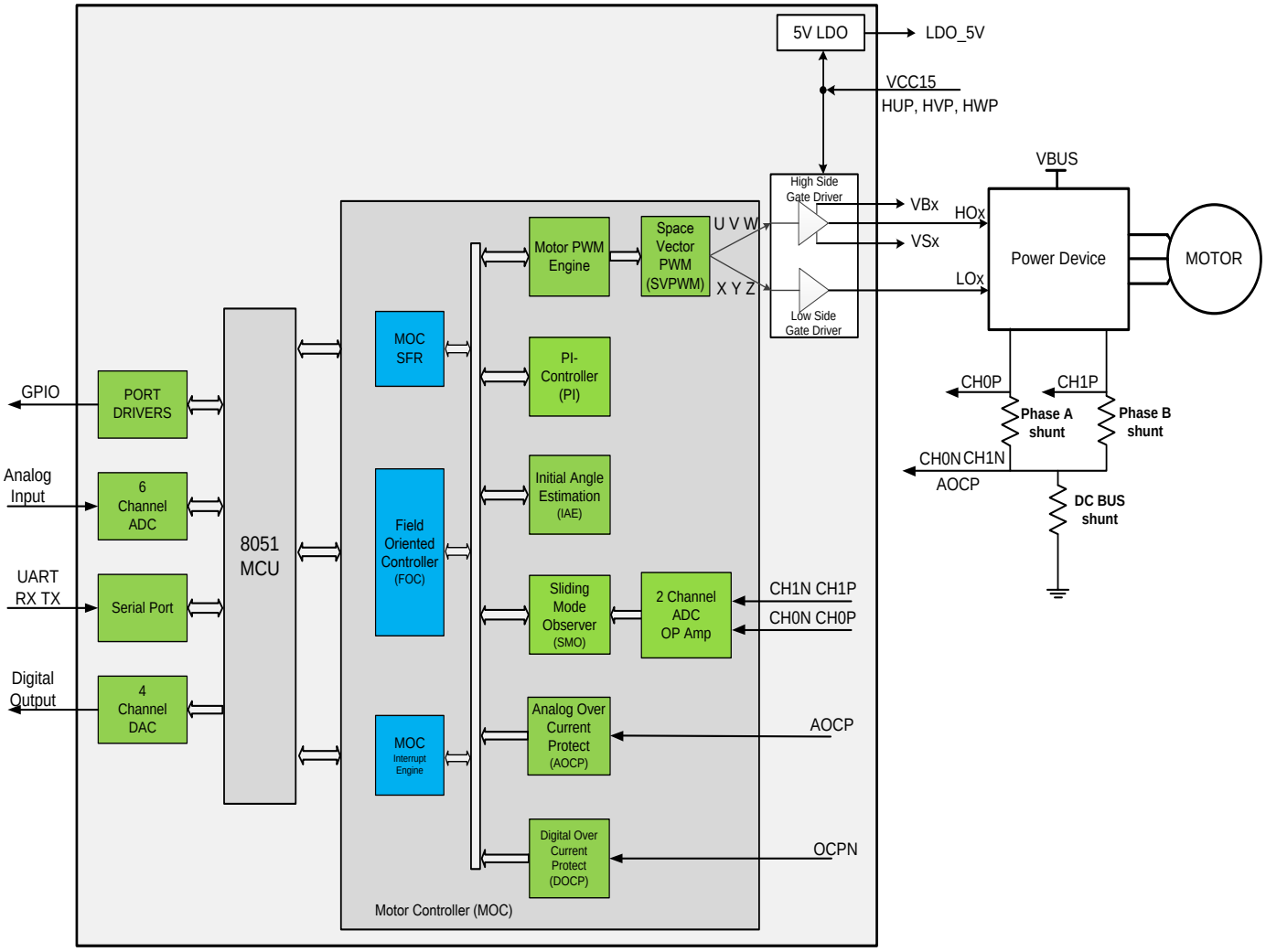
- MCS®-51 Compatible
- 1T 8052 Central Processing Unit
- 4.5V to 5.5V Operation Range
- 4 Level Priority Interrupt
- 13 Interrupt Sources
- 1 External Interrupts (INT1N)
    - 2 External Interrupts (INT0N, INT1N)
    - 2 External OCP Interrupts (AOCP, OCP)
- Memory Size:
- 8KB Flash Program Memory
- 256 x 8-bit IRAM
- 512 x 8-bit XRAM
- Up to 25 General-Purpose Input / Output (GPIO) Pins
- Three 16-bit Timer/Counters
- Watchdog (WD) Timer
  8CH 10-bit ADC & 1CH 10-bit DAC / MDRFD0AD48 / LQFP-48
- Full Duplex UART Serial Channel
- Fast Multiplication-Division Unit (MDU): 16*16,32/16, 16/16, 32-bit L/R shifting and 32-bitnormalization

List of Contents

1. General Description

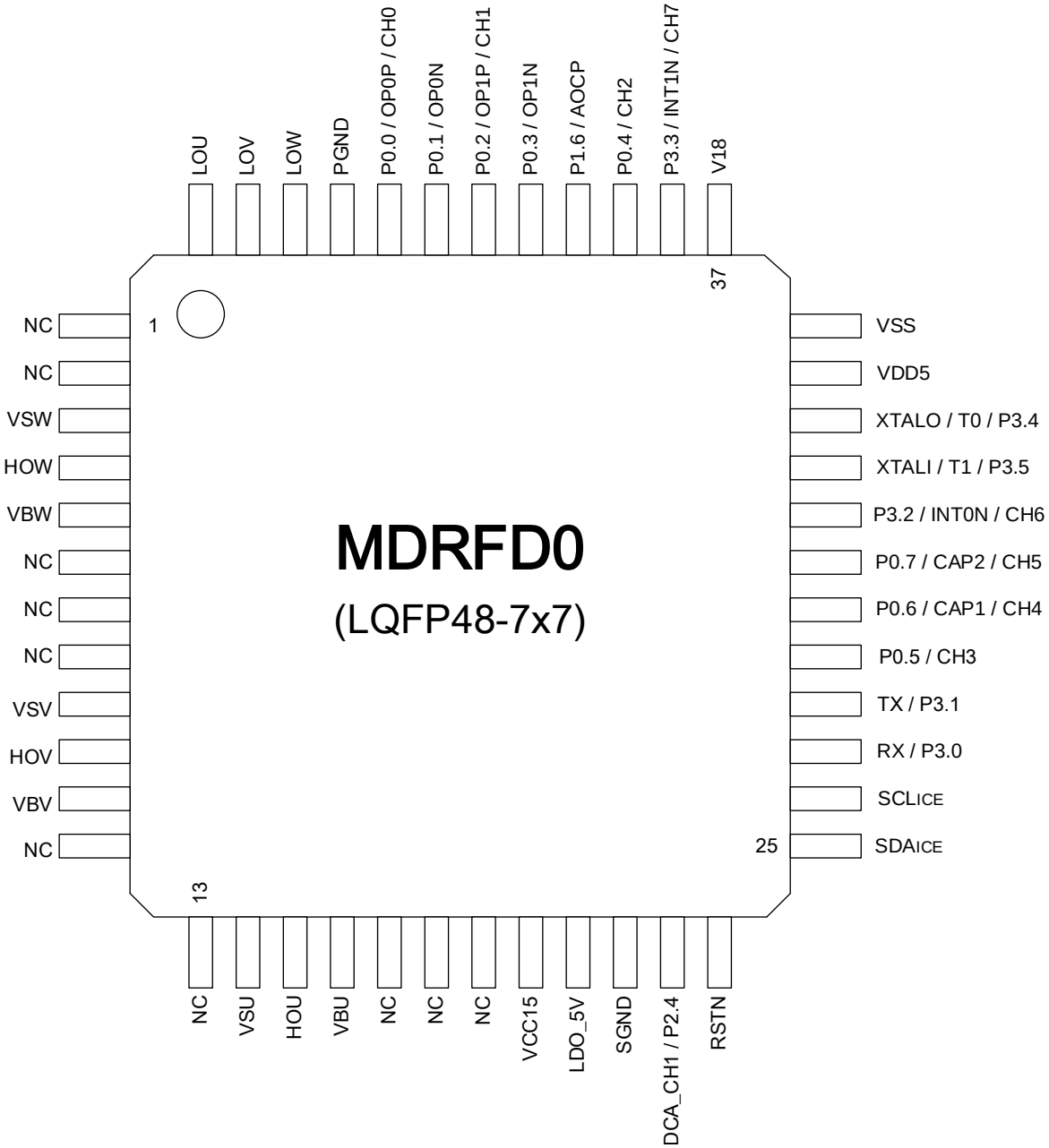
The **MDRFD0** is a highly integrated motor drive controller. The **MDRFD0** is composed of FOC sensor-less MCU and 600V 3-phase Gate-Driver that suit for under DC 400V and medium motor system, for example household fan、water pump、industry fan…etc.

2. Block Diagram



3. Pin Configurations

3.1. Package Instruction LQFP7x7- 48



3.2. Pin Description

Table 3–1.Pin Description

Pin # MDRFD0 LQFP-48	Name	Type	Description
14	VSU		High-side driver U-phase floating supply offset voltage
15	HOU	HV O	High-side driver U-phase gate driver output
16	VBU		High-side driver U-phase floating supply
9	VSV		High-side driver V-phase floating supply offset voltage
10	HOV	HV O	High-side driver V-phase gate driver output
11	VBV		High-side driver V-phase floating supply
3	VSW		High-side driver W-phase floating supply offset voltage
4	HOW	HV O	High-side driver W-phase gate driver output
6	VBW		High-side driver W-phase floating supply
20	VCC15	Power	Logic and low-side gate drivers power supply voltage
21	LDO_5V	Power	5V LDO output
22	SGND	Ground	Logic ground
27	P3.0	I/O	Bit 0 of Port 3.
	RX	I	Serial Data Transmit (UART)
28	P3.1	I/O	Bit 1 of Port 3.
	TX	O	Serial Data Receive (UART)
32	P3.2	I/O	Bit 2 of Port 3.
	CH6	I	Analog Input Ch6.
	INT0N	I	External Interrupt 0. Low level trigger or falling edge trigger.
38	P3.3	I/O	Bit 3 of Port 3.
	CH7	I	Analog Input Ch7.
	INT1N	I	External Interrupt 1. Low level trigger or falling edge trigger.

33	P3.5	I/O	Bit 5 of Port 3.
	XTALI	I	Crystal input pin. **Connect the crystal 12MHz between this pin and XTALO and a 22pF capacitor to VSS.**
	T1	I	TIMER1 External Input.
34	P3.4	I/O	Bit 4 of Port 3.
	XTALO	O	Crystal output pin. **Connect the crystal 12MHz between this pin and XTALI and a 22pF capacitor to VSS.**
	T0	I	TIMER0 External Input.
35	VDD5	Power	5.0V Voltage Input. **A 0.1uF and 10uF (minimum) capacitor should be connected between this pin and VSS.**
36	VSS	Ground	Power Ground.
37	V18	O	1.8V Voltage Output. **A 0.1uF and 1uF (minimum) capacitor should be connected between this pin and VSS.**
31	P0.7	I/O	Bit 7 of Port 0.
	CH5	I	Analog Input Ch5.
	CAP2	I	Capture Input 2.
32	P0.6	I/O	Bit 6 of Port 0.
	CH4	I	Analog Input Ch4.
	CAP1	I	Capture Input 1
29	P0.5	I/O	Bit 5 of Port 0.
	CH3	I	Analog Input Ch3.
39	P0.4	I/O	Bit 2 of Port 0.
	CH2	I	Analog Input Ch2.
41	P0.3	I/O	Bit 2 of Port 0.
	OP1N	I	OP 1-Amp N-Input.
42	P0.2	I/O	Bit 3 of Port 0.
	CH1	I	Analog Input Ch1. (Current feedback)
	OP1P	0	OP 1-Amp P- Input
43	P0.1	I/O	Bit 0 of Port 0.
	OP0N	I	OP 0-Amp N- Input.
44	P0.0	I/O	Bit 1 of Port 0.
	CH0	I	Analog Input Ch0. (Current feedback)
	OP0P	I	OP 0-Amp P-Input.
40	P1.6	I/O	Bit 6 of Port 1.

	AOCP	I	Analog OCP Control.
None	P1.7	I/O	Bit 7 of Port 1.
	DOCPN	I	Digital OCP Control.
None	P2.7	I/O	Bit 7 of Port 2.
	DAC_CH4	O	Digital to Analog Converter Output 4
None	P2.6	I/O	Bit 6 of Port 2.
	DAC_CH3	O	Digital to Analog Converter Output 3
None	P2.5	I/O	Bit 5 of Port 2.
	DAC_CH2	O	Digital to Analog Converter Output 2
23	P2.4	I/O	Bit 4 of Port 2.
	DAC_CH1	O	Digital to Analog Converter Output 1
24	RSTN	I	System Reset.
25	SDA_{ICE}		For ICE.
26	SCL_{ICE}		For ICE.
45	PGND	Ground	Low-side gate drivers ground
48	LOU	O	Low-side gate driver U-phase output
47	LOV	O	Low-side gate driver V-phase output
46	LOW	O	Low-side gate driver W-phase output

4. Absolute Maximum Ratings

VDD5 Supply Voltage……V_{SS}-0.3V to V_{SS}+6.0V
VDD5 Input Voltage……V_{SS}-0.3V to V_{DD}+0.3V
VCC15 Supply Voltage……-0.3V to 20V
V_B High Side floating supply Voltage…… -0.3V to 600V
V_S High Side offset Voltage…… V_B-18V to V_B+0.3V
V_{HO} High Side gate-driver output Voltage…… V_S-0.3V to V_S+0.3V
V_{LO} Low Side gate-driver output Voltage…… PGND-0.3V to V_{CC15}+0.3V
Storage Temperature……-50℃ to 150℃
Operating Temperature……-40℃ to 125℃
I_{OH} Total……-80mA
I_{OL} Total……80mA
Total Power Dissipation……500mW
Electrostatic Discharge Capability – Human Body Mode……TBD KV
Electrostatic Discharge Capability – Machine Mode……TBDV

5. D.C. Characteristics

Ta=25℃

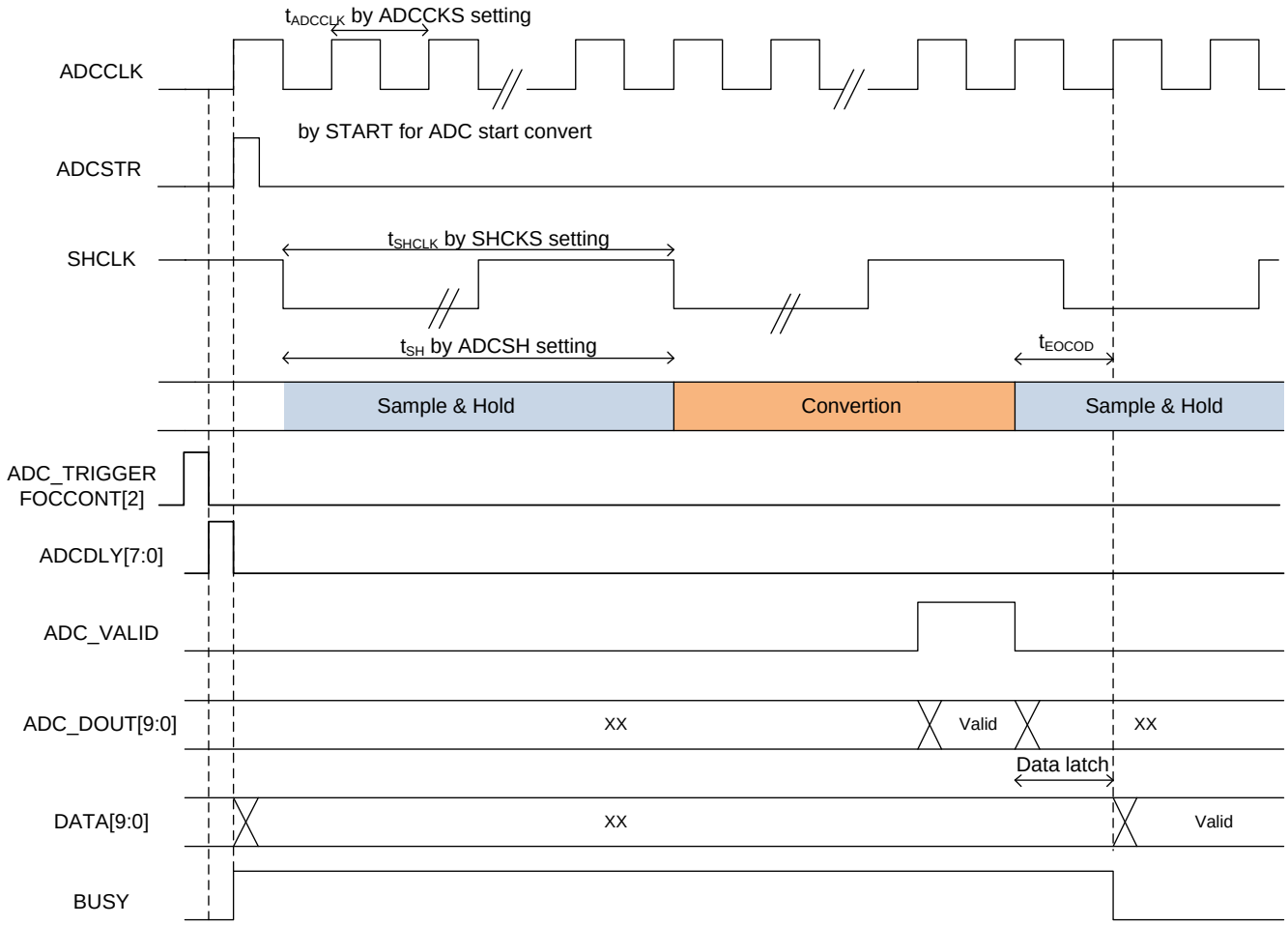
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Vcc15	Low side supply voltage	—	—	11	—	18	
LDO-5V Voltage	LDO-5V Output Range	—	VCC = 12V	4.5	5	5.5	V
LDO-5V Current	LDO-5V Current Range	—	VCC = 12V	—	20	30	mA
VB.U.V.W	High side floating supply voltage	—	—	-8	—	600	V
VS.U.V.W	High side offset voltage	—	—	VB-18	—	VB-11	V
VHO.U.V.W	High side gate driver output voltage			VS		VB	V
VLO.U.V.W	Low side gate driver output voltage			PGND		VCC	V
V_{DD5}	Operating Voltage	—	fsys=48MHz	4.5	5.0	5.5	V
V_{18}	V_{18} Output Range	—	Load Current <30mA	1.71	1.8	1.89	V
I_{DD}	Operating Current	VDD5	No load, fsys=48Mhz,ADC off, MOC off	—	9	12	mA
V_{IL}	Input Low Voltage for I/O Ports.	—	—	0	—	0.3 V_{DD5}	V
V_{IH}	Input High Voltage for I/O Ports.	—	—	0.75 V_{DD5}	—	V_{DD5}	V
V_{LVD}	LVD Voltage Level	—	—				
V_{OL}	Output Low Voltage for I/O Ports.	VDD5	I_{OL}=20mA	—	—	0.5	V
V_{OH}	Output High Voltage for I/O Ports.	VDD5	I_{OH}=-7.4mA	4.5	—	—	V
R_{PU}	Pull-up Resistance for I/O Ports	VDD5	—	10	30	50	KΩ
R_{PD}	Pull-down Resistance for I/O Ports	VDD5	—	10	30	50	KΩ

6. A.C. Characteristics

Ta=25℃

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD5	Conditions				
fsys	System Frequency	4.5V~5.5V	Ta=-40℃ to 125℃	TBD	48.0	TBD	MHz
			Ta=-20℃ to 85℃	TBD	48.0	TBD	MHz
			Ta=25℃	-1%	48.0	+1%	MHz
fTIMER	Timer Input Pin Frequency	—	—	—	—	4	fsys
tINT	Interrupt Pulse Width	—	—	1	5	10	tsys
tLVD	Low Voltage Width to interrupt	—	—	120	240	480	us
tV18	V18 Stable Time	—	—	60	120	240	us
tRSDT	System Reset Delay Time(Power On Reset)	—	—	25	50	100	ms

7. A/D Converter Characteristics



Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD5	Conditions				
RI	Input Impedance	—	—	—		—	MΩ
IAD	Additional Power Consumption if A/D Converter is Used	5V	—	—	6	—	mA
IADSTB	A/D Converter Standby Current	—	Load Current < 10mA	—	—	4	uA
tADCCLK	A/D Converter Clock Time	—	24MHz	—	41.7	—	ns
		—	12MHz	—	83.3	—	ns
tCONV	A/D Conversion Time	—	24MHz	—	0.875	—	us
		—	12MHz	—	1.7	—	us
tSH	A/D Sample and Hold Time	—	6MHz	0.17	—	0.68	us
		—	3MHz	0.34	—	1.36	us
		—	2.4MHz	0.42	—	1.68	us
		—	2MHz	0.5	—	2	us
DNL	Differential Non-linearity	4.5V	No load, tCONV=2.5us	-1	—	+3	LSB
		5.5V		-1	—	+3	LSB
		4.5V	No load, tCONV=5us	-1	—	+3	LSB
		5.5V		-1	—	+3	LSB
INL	Integral Non-linearity	4.5V	No load, tCONV=2.5us	-4	—	+4	LSB
		5.5V		-4	—	+4	LSB
		4.5V	No load, tCONV=5us	-4	—	+4	LSB
		5.5V		-4	—	+4	LSB
GERR	Gain Error	—	—	-10	—	+10	LSB
tEOCOD	End of Conversion Output Delay	5V	—	—		—	ns

8. Special Function Registers (SFR)

SFRs Memory Map

	8	9	A	B	C	D	E	F	
F8	PINCONG1	PINCONG2	PINCONG3	PINCONG4	PINCONG5	PINCONG6	RSTS	TAKEY	FF
F0	B	PINSET1	PINSET2	PINSET3	PINSET4	PINSET5	PINSET6	PINSET7	F7
E8	DAC_CH1	DAC_CH2	DAC_CH3	DAC_CH4	SFR_PAGE	SP_CYC	AOCPCONT	OCPNCONT	EF
E0	ACC	MPWMDATL	MPWMDATH	MPWMCONT	MPWMINV	MPWMDB	PI_GAIN	DAC_CTRL	E7
D8	SPEED_H	CAPT_L	CAPT_H	CAPH_L	CAPH_H	CAPCONT	CPU_ANG_L	CPU_ANG_H	DF
D0	PSW	PFCON	FOC_D1_L	FOC_D1_H	FOC_D2_L	FOC_D2_H	FOCCONT	SPEED_L	D7
C8	T2CON	ADC1OS_L	ADC1OS_H	ADC2OS_L	ADC2OS_H	-----	-----	-----	CF
C0	IRCON1	ADCSTR	ADCCONT	ADCD1	ADCD2	ADCDLY	AS	PINCONG7	C7
B8	IEN1	IP1	MD5	SMO_D1_L	SMO_D1_H	SMO_D2_L	SMO_D2_H	-----	BF
B0	P3	MD2	MD3	MD4	TL2	TH2	WDTC	WDTK	B7
A8	IEN0	IP0	-----	-----	MD_MODE	MD_CONT	MD0	MD1	AF
A0	P2	VDQ_OFST_L	VDQ_OFST_H	-----	INI_ANG_DAT	INI_ANG_CTRL	PI_CMD_L	PI_CMD_H	A7
98	SCON	SBUF	SRELL	SRELH	-----	PI_UI_L	PI_UI_LH	MOTOR_CONT2	9F
90	P1	PI_KI_L	PI_KI_H	PI_KP_L	PI_KP_H	PI_LMT_L	PI_LMT_H	MOTOR_CONT1	97
88	TCON	TMOD	TL0	TL1	TH0	TH1	AUX	SYNC	8F
80	P0	SP	DP0L	DP0H	DP1L	DP1H	RCON	PCON	87
	0	1	2	3	4	5	6	7	

SYMBOL	DIRECT ADDRESS		SFR_PAGE						
	[L,H]		0	1	2	3	4	5	6
MPWM									
MPWMDATA [L,H]	E1H	E2H	CYCLE	DUTY_U	DUTY_V	DUTY_W			
PI-Controller									
PI_KI[L,H]	91H	92H	IQ	ID	Speed	PLL			
PI_KP [L,H]	93H	94H	IQ	ID	Speed	PLL			
PI_LMT [L,H]	95H	96H	IQ	ID	Speed	PLL			
PI_CMD[L,H]	A6H	A7H	IQ	ID	Speed	PLL			
PI_UI [L,H]	9DH	9EH	-------	-------	Speed-UI	PLL-UI			
Slide Mode Controller									
SMO_D1 [L,H]	BBH	BCH	GS	SMO-gain	Angle base	ES_Z-alpha	ES_I-alpha	ES_E-alpha	SMO-angle
SMO_D2 [L,H]	BDH	BEH	FS	SMO-filter	Angle shift	ES_Z-beta	ES_I-beta	ES_E-beta	PLL PI-OUT
Field Oriented Controller									
FOC_D1 [L,H]	D2H	D3H	IQ_FB	ID_FB	Ia	Va	I-alpha	V-alpha	FOC-angle
FOC_D2[L,H]	D4H	D5H	IQ_PI_OUT	ID_PI_OUT	Ib	Vb	I-beta	V-beta	SVPWM-amp
VDQ_OFST[L,H]	A1H	A2H	Q-axis Voltage	D-axis Voltage					
Initial Angle Estimated Controller									
INI_ANG_CTRL	A4H		Pattern 10	Pattern 32	Pattern 54				

9. MDRFD0 SFRs and Reset Value

SYMBOL	DESCRIPTION	DIRECT ADDRESS	RESET VALUE
ACC	Accumulator	E0H	00H
ADCSTR	ADC Start Convert and Setting Register	C1H	00H
ADCCONT	ADC Control Register	C2H	83H
ADC1D1	ADC Data Register 1	C3H	00H
ADC1D2	ADC Data Register 2	C4H	00H
ADCDLY	ADC Sample Delay	C5H	33H
ADC1OS_L	ADC 1 Data Offset Low byte	C9H	00H
ADC1OS_H	ADC 1 Data Offset High byte	CAH	02H
ADC2OS_L	ADC 2 Data Offset Low byte	CBH	00H
ADC2OS_H	ADC 2 Data Offset High byte	CCH	02H
AUX	Auxiliary	8EH	11H
AS	Angle Supplement	C6H	X0H
AOCPCONT	Analog OCP Control Register	EEH	C7H
B	B Register	F0H	00H
CAPCONT	Capture Control Register	DDH	03H
CAPT_L	Capture Total Count Low	D9H	FFH
CAPT_H	Capture Total Count High	DAH	FFH
CAPH_L	Capture High-level Count Low	DBH	FFH
CAPH_H	Capture High-level Count High	DCH	FFH
CPU_ANG_L	CPU Angle Data Low byte	DEH	00H
CPU_ANG_H	CPU Angle Data High byte	DFH	00H
DAC_CTRL	Digital to Analog Converter Control	E7H	00H
DAC_CHA	Digital to Analog Converter Data A	E8H	00H
DAC_CHB	Digital to Analog Converter Data B	E9H	00H
DAC_CHC	Digital to Analog Converter Data C	EAH	00H
DAC_CHD	Digital to Analog Converter Data D	EBH	00H
DPTR0:	Data Pointer 0 (2 bytes)		
DP0L	Data Pointer 0 Low	82H	00H
DP0H	Data Pointer 0 High	83H	00H
DPTR1:	Data Pointer 1 (2 bytes)		
DP1L	Data Pointer 1 Low	84H	00H
DP1H	Data Pointer 1 High	85H	00H
VDQ_OFST_L	D&Q -Axis Voltage Offset Low byte	A1H	00H
VDQ_OFST_H	D&Q -Axis Voltage Offset High byte	A2H	00H
FOCCONT	Field Oriented Control Register	D6H	00H
FOC_D1_L	Field Oriented Control Data1 Low byte	D2H	----
FOC_D1_H	Field Oriented Control Data1 High byte	D3H	----
FOC_D2_L	Field Oriented Control Data2 Low byte	D4H	----
FOC_D2_H	Field Oriented Control Data2 High byte	D5H	----
IEN0	Interrupt Enable Register 0	A8H	00H
IEN1	Interrupt Enable Register 1	B8H	00H
IP0	Interrupt Priority Register 0	A9H	00H
IP1	Interrupt Priority Register 1	B9H	00H
IRCON1	Interrupt Request Register 1	C0H	00H
MOTOR_CONT1	Motor Control Register 1	97H	00H
MOTOR_CONT2	Motor Control Register 2	9FH	00H
MD_CONT	MDU Control Register	ADH	10H
MD_MODE	MDU Control Mode Register	ACH	10H

MD0	Multiplication Division Register 0	AEH	00H
MD1	Multiplication Division Register 1	AFH	00H
MD2	Multiplication Division Register 2	B1H	00H
MD3	Multiplication Division Register 3	B2H	00H
MD4	Multiplication Division Register 4	B3H	00H
MD5	Multiplication Division Register 5	BAH	00H
MPWMCONT	MPWM Control Register	E3H	00H
MPWMDATL	MPWM Data Low	E1H	00H
MPWMDATH	MPWM Data High	E2H	00H
MPWMDB	Motor PWM Dead-band Register	E5H	78H
MPWMINV	MPWM Inverse Selection Register	E4H	00H
OCPCONT	OCP Control Register	EFH	85H
P0	Port 0	80H	FFH
P1	Port 1	90H	FFH
P2	Port 2	A0H	FFH
P3	Port 3	B0H	FFH
PCON	Power Control Register	87H	00H
PFCON	Peripheral Frequency Control Register	D1H	00H
PINCONG1	Pin Configure Register 1	F8H	AAH
PINCONG2	Pin Configure Register 2	F9H	AAH
PINCONG3	Pin Configure Register 3	FAH	A0H
PINCONG4	Pin Configure Register 4	FBH	AAH
PINCONG5	Pin Configure Register 5	FCH	AAH
PINCONG6	Pin Configure Register 6	FDH	A0H
PINCONG7	Pin Configure Register 7	C7H	0AH
PINSET1	Pin I/O Setting Register 1	F1H	AAH
PINSET2	Pin I/O Setting Register 2	F2H	AAH
PINSET3	Pin I/O Setting Register 3	F3H	0AH
PINSET4	Pin I/O Setting Register 4	F4H	00H
PINSET5	Pin I/O Setting Register 5	F5H	80H
PINSET6	Pin I/O Setting Register 6	F6H	0AH
PINSET7	Pin I/O Setting Register 7	F7H	B0H
PI_KI_L	PI-control KI Data Low byte	91H	00H
PI_KI_H	PI-control KI Data High byte	92H	00H
PI_KP_L	PI-control KP Data Low byte	93H	00H
PI_KP_H	PI-control KP Data High byte	94H	00H
PI_LMT_L	PI-control Limit Data Low byte	95H	00H
PI_LMT_H	PI-control Limit Data High byte	96H	00H
PI_CMD_L	PI-control command Data Low byte	A6H	00H
PI_CMD_H	PI-control command Data High byte	A7H	00H
PI-UI_L	PI-control Integral Data Low byte	9DH	00H
PI-UI_H	PI-control Integral Data High byte	9EH	00H
PSW	Program Status Word Register	D0H	00H
RCON	Internal RAM Control Register	86H	F0H
RSTS	Reset Source Register	FEH	0AH
SBUF	Serial Port Data Buffer	99H	00H
SCON	Serial Port Control Register	98H	00H
SFR_PAGE	Special Function Registers Page	ECH	00H
SP	Stack Pointer	81H	07H
SP_CYC	Speed Control Loop Cycle	EDH	26H
SPEED_L	Speed Register Low	D7H	00H
SPEED_H	Speed Register High	D8H	00H
SRELL	Serial Port Reload Register High	9AH	00H
SRELH	Serial Port Reload Register High	9BH	00H
SMO_D1_L	Sliding Mode Observer Data1 Low Byte	BBH	00H
SMO_D1_H	Sliding Mode Observer Data1 High Byte	BCH	00H
SMO_D2_L	Sliding Mode Observer Data2 Low Byte	BDH	00H
SMO_D2_H	Sliding Mode Observer Data2 High Byte	BEH	00H

SYNC	MOC Sync Register	8FH	00H
T2CON	Timer2 Control Register	C8H	00H
TAKEY	Time Access Key Register	FFH	00H
TCON	Timer 0/1 Control Register	88H	00H
TH0	Timer0 High byte	8CH	00H
TH1	Timer1 High byte	8DH	00H
TH2	Timer2 High byte	B5H	00H
TL0	Timer0 Low byte	8AH	00H
TL1	Timer1 Low byte	8BH	00H
TL2	Timer2 Low byte	B4H	00H
TMOD	Timer 0/1 Mode Register	89H	00H
WDTC	Watchdog Timer Control Register	B6H	04H
WDTK	Watchdog Timer Refresh Key	B7H	00H

10. Memory

The **MDRFD0** memory structure follows the general 8052 structure.
There are three memory areas: Program Memory (Flash), External Data Memory (XRAM) and Internal Data Memory (IRAM). In addition, **MDRFD0** integrates 8Kbytes Flash, 256bytes IRAM and 512bytes XRAM.

10.1. Program Memory

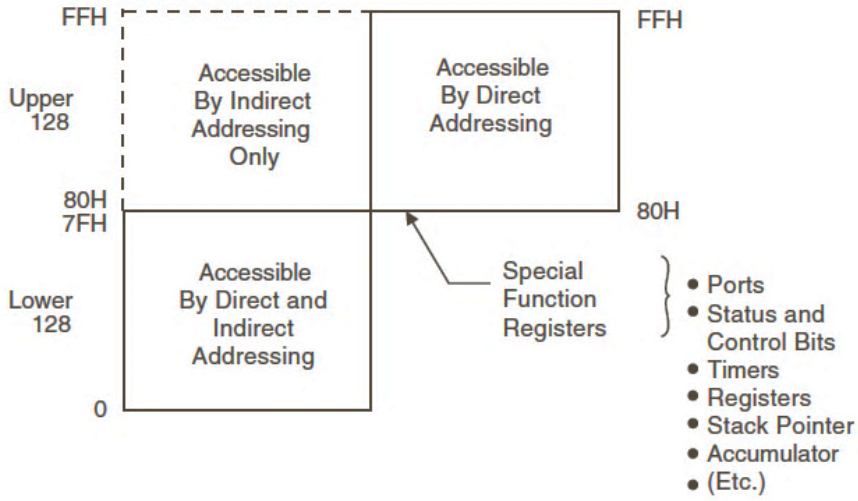
The **MDRFD0** contains 8Kbytes of on-chip Flash memory for program storage.

10.2. Data Memory

The **MDRFD0** contains 256bytes of general internal data memory (IRAM) and 512bytes of external data memory (XRAM).

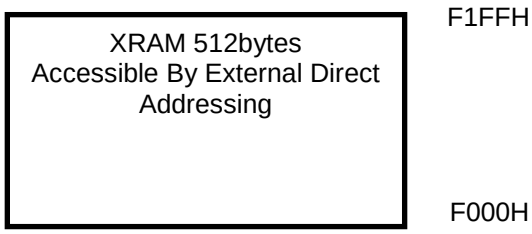
10.2.1 Data Memory (IRAM)(00H~FFH)

The lower 128 bytes of IRAM may be accessed through both direct and indirect addressing. The upper 128 bytes of IRAM and the 128 bytes of SFR registers share the same address space. The upper 128 bytes of data memory may only be accessed using indirect addressing. The SFR registers can only be accessed through direct addressing. The lowest 32 bytes (00H -1FH) of data memory are grouped into 4 banks of 8 registers each. The **RS0** and **RS1** bits (**PSW**.3 and**PSW**.4) select which register bank is in use. Instructions using register addressing will only access the currently specified bank.



10.2.2 Data Memory (XRAM)(F000H~F1FFH)

External addresses F000H to F1FFh contain the on-chip expanded SRAM. This memory can be accessed via external direct addressing mode (with **MOVX** instructions). The address space of instruction **MOVX** @Ri,A (i=0,1) is determined by **RCON** [7:0] of SFR 86H**RCON**(internal RAM control register). The default setting of **RCON** [7:0] is F0h (page0). One page of XRAM is512 bytes.



11. Instruction Set

The **MDRFD0** is fully binary compatible with the MCS-51 instruction set.

Arithmetic operations	Description	Bytes	Cycles	Hex Code
ADD A,Rn	Add register to accumulator	1	1	0x28-0x2F
ADD A,direct	Add directly addressed data to accumulator	2	2	0x25
ADD A,@Ri	Add indirectly addressed data to accumulator	1	2	0x26-0x27
ADD A,#data	Add immediate data to accumulator	2	2	0x24
ADDC A,Rn	Add register to accumulator with carry	1	1	0x38-0x3F
ADDC A,direct	Add directly addressed data to accumulator with carry	2	2	0x35
ADDC A,@Ri	Add indirectly addressed data to accumulator with carry	1	2	0x36-0x37
ADDC A,#data	Add immediate data to accumulator with carry	2	2	0x34
SUBB A,Rn	Subtract register from accumulator with borrow	1	1	0x98-0x9F
SUBB A,direct	Subtract directly addressed data from accumulator with borrow	2	2	0x95
SUBB A,@Ri	Subtract indirectly addressed data from accumulator with borrow	1	2	0x96-0x97
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2	0x94
INC A	Increment accumulator	1	1	0x04
INC Rn	Increment register	1	2	0x08-0x0F
INC direct	Increment directly addressed location	2	3	0x05
INC @Ri	Increment indirectly addressed location	1	3	0x06-0x07
INC DPTR	Increment data pointer	1	1	0xA3
DEC A	Decrement accumulator	1	1	0x14
DEC Rn	Decrement register	1	2	0x18-0x1F
DEC direct	Decrement directly addressed location	2	3	0x15
DEC @Ri	Decrement indirectly addressed location	1	3	0x16-0x17
MUL AB	Multiply A and B	1	5	0xA4
DIV	Divide A by B	1	5	0x84
DA A	Decimally adjust accumulator	1	1	0xD4

Logic operations	Description	Bytes	Cycles	Hex Code
ANL A,Rn	AND register to accumulator	1	1	0x58-0x5F
ANL A,direct	AND directly addressed data to accumulator	2	2	0x55
ANL A,@Ri	AND indirectly addressed data to accumulator	1	2	0x56-0x57
ANL A,#data	AND immediate data to accumulator	2	2	0x54
ANL direct,A	AND accumulator to directly addressed location	2	3	0x52
ANL direct,#data	AND immediate data to directly addressed location	3	4	0x53
ORL A,Rn	OR register to accumulator	1	1	0x48-0x4F
ORL A,direct	OR directly addressed data to accumulator	2	2	0x45
ORL A,@Ri	OR indirectly addressed data to accumulator	1	2	0x46-0x47
ORL A,#data	OR immediate data to accumulator	2	2	0x44
ORL direct,A	OR accumulator to directly addressed location	2	3	0x42
ORL direct,#data	OR immediate data to directly addressed location	3	4	0x43
XRL A,Rn	Exclusive OR register to accumulator	1	1	0x68-0x6F
XRL A,direct	Exclusive OR directly addressed data to accumulator	2	2	0x65
XRL A,@Ri	Exclusive OR indirectly addressed data to accumulator	1	2	0x66-0x67
XRL A,#data	Exclusive OR immediate data to accumulator	2	2	0x64
XRL direct,A	Exclusive OR accumulator to directly addressed location	2	3	0x62
XRL direct,#data	Exclusive OR immediate data to directly addressed location	3	4	0x63
CLR A	Clear accumulator	1	1	0xE4
CPL A	Complement accumulator	1	1	0xF4
RL A	Rotate accumulator left	1	1	0x23
RLC A	Rotate accumulator left through carry	1	1	0x33
RR A	Rotate accumulator right	1	1	0x03
RRC A	Rotate accumulator right through carry	1	1	0x13
SWAP A	Swap nibbles within the accumulator	1	1	0xC4

Data transfer operations	Description	Bytes	Cycles	Hex Code
MOV A,Rn	Move register to accumulator	1	1	0xE8-0xEF
MOV A,direct	Move directly addressed data to accumulator	2	2	0xE5
MOV A,@Ri	Move indirectly addressed data to accumulator	1	2	0xE6-0xE7
MOV A,#data	Move immediate data to accumulator	2	2	0x74
MOV Rn,A	Move accumulator to register	1	2	0xF8-0xFF
MOV Rn,direct	Move directly addressed data to register	2	4	0xA8-0xAF
MOV Rn,#data	Move immediate data to register	2	2	0x78-0x7F
MOV direct,A	Move accumulator to direct	2	3	0xF5
MOV direct,Rn	Move register to direct	2	3	0x88-0x8F
MOV direct1,direct2	Move directly addressed data to directly addressed location	3	4	0x85
MOV direct,@Ri	Move indirectly addressed data to directly addressed location	2	4	0x86-0x87
MOV direct,#data	Move immediate data to directly addressed location	3	3	0x75
MOV @Ri,A	Move accumulator to indirectly addressed location	1	3	0xF6-0xF7
MOV @Ri,direct	Move directly addressed data to indirectly addressed location	2	5	0xA6-0xA7
MOV @Ri,#data	Move immediate data to in directly addressed location	2	3	0x76-0x77
MOV DPTR,#data16	Load data pointer with a 16-bit immediate	3	3	0x90
MOVC A,@A+DPTR	Load accumulator with a code byte relative to DPTR	1	3	0x93
MOVC A,@A+PC	Load accumulator with a code byte relative to PC	1	3	0x83
MOVX A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	3	0xE2-0xE3
MOVX A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	3	0xE0
MOVX @Ri,A	Move accumulator to external RAM (8-bit addr.)	1	4	0xF2-0xF3
MOVX @DPTR,A	Move accumulator to external RAM (16-bit addr.)	1	4	0xF0
PUSH direct	Push directly addressed data onto stack	2	4	0xC0
POP direct	Pop directly addressed location from stack	2	3	0xD0
XCH A,Rn	Exchange register with accumulator	1	2	0xC8-0xCF
XCH A,direct	Exchange directly addressed location with accumulator	2	3	0xC5
XCH A,@Ri	Exchange indirect RAM with accumulator	1	3	0xC6-0xC7
XCHD A,@Ri	Exchange low-order nibbles of indirect and accumulator	1	3	0xD6-0xD7

Program branches	Description	Bytes	Cycles	Hex Code
ACALL addr11	Absolute subroutine call	2	6	xxx10001b
LCALL addr16	Long subroutine call	3	6	0x12
RET	Return from subroutine	1	4	0x22
RETI	Return from interrupt	1	4	0x32
AJMP addr11	Absolute jump	2	3	xxx00001b
LJMP addr16	Long jump	3	4	0x02
SJMP rel	Short jump (relative address)	2	3	0x80
JMP @A+DPTR	Jump indirect relative to the DPTR	1	2	0x73
JZ rel	Jump if accumulator is zero	2	3	0x60
JNZ rel	Jump if accumulator is not zero	2	3	0x70
JC rel	Jump if carry flag is set	2	3	0x40
JNC	Jump if carry flag is not set	2	3	0x50
JB bit,rel	Jump if directly addressed bit is set	3	4	0x20
JNB bit,rel	Jump if directly addressed bit is not set	3	4	0x30
JBC bit,rel	Jump if directly addressed bit is set and clear bit	3	4	0x10
CJNE A,direct,rel	Compare directly addressed data to accumulator and jump if not equal	3	4	0xB5
CJNE A,#data,rel	Compare immediate data to accumulator and jump if not equal	3	4	0xB4
CJNE Rn,#data,rel	Compare immediate data to register and jump if not equal	3	4	0xB8-0xBF
CJNE @Ri,#data,rel	Compare immed. to ind. and jump if not equal	3	4	0xB6-0xB7
DJNZ Rn,rel	Decrement register and jump if not zero	2	3	0xD8-0xDF
DJNZ direct,rel	Decrement directly addressed location and jump if not zero	3	4	0xD5
NOP	No operation	1	1	0

Boolean main pulation	Description	Bytes	Cycles	Hex Code
CLR C	Clear carry flag	1	1	0xC3
CLR bit	Clear directly addressed bit	2	3	0xC2
SETB C	Set carry flag	1	1	0xD3
SETB bit	Set directly addressed bit	2	3	0xD2
CPL C	Complement carry flag	1	1	0xB3
CPL bit	Complement directly addressed bit	2	3	0xB2
ANL C,bit	AND directly addressed bit to carry flag	2	2	0x82
ANL C,/bit	AND complement of directly addressed bit to carry	2	2	0xB0
ORL C,bit	OR directly addressed bit to carry flag	2	2	0x72
ORL C,/bit	OR complement of directly addressed bit to carry	2	2	0xA0
MOV C,bit	Move directly addressed bit to carry flag	2	2	0xA2
MOV bit,C	Move carry flag to directly addressed bit	2	3	0x92

12. MCU

12.1 8051 Engine

SFR	Description	address	Reset value
ACC	Accumulator	E0H	00H
B	B Register	F0H	00H
PSW	Program Status Word Register	D0H	00H
SP	Stack Pointer	81H	07H
DP0H	Data Pointer 0 High	83H	00H
DP0L	Data Pointer 0 Low	82H	00H
DP1H	Data Pointer 1 High	85H	00H
DP1L	Data Pointer 1 Low	84H	00H
AUX	Auxiliary	8EH	11H
RCON	Internal RAM Control Register	86H	F0H

12.1.1 ACC (Accumulator)

The most important of all special function registers, that's the first comment about Accumulator which is also known as ACC or A. The Accumulator (sometimes referred to as Register A also) holds the result of most of arithmetic and logic operations.

ACC Address = E0H Reset Value = 0x00H

Accumulator

Bit	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.1.2 B (B Register)

The B register is used during multiplying and division instructions. It can also be used as a scratch-pad register to hold temporary data.

B Address = F0H Reset Value = 0x00H

B Register

Bit	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.1.3 PSW (Program Status Word Register)

The PSW register contains status bits that reflect the current state of the CPU. Note that the Parity bit can only be modified by hardware upon the state of ACC register.

PSW Address = D0H Reset Value = 0x00H

Program Status Word Register

Bit	CY	AC	F0	RS1	RS0	OV	F1	P
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

CY	Carry flag : Carry bit in arithmetic operations and accumulator for Boolean operations.
AC	Auxiliary Carry flag : Set if there is a carry-out from third bit of Accumulator in BCD Operations.
F0	General purpose Flag0 : General purpose flag available for user.
RS1	Register bank select control bit 1, used to select working register bank.
RS0	Register bank select control bit 0, used to select working register bank.
OV	Overflow flag : Set in case of overflow in Accumulator during arithmetic operations.
F1	General purpose Flag 1 : General purpose flag available for user.
P	Parity flag : Reflects the number of ‘1’s in the Accumulator. P = ‘1’ if Accumulator contains an odd number of ‘1’s P = ‘0’ if Accumulator contains an even number of ‘1’s

The state of RS1 and RS0 bits selects the working register bank as follows:

RS1	RS0	Selected Register Bank	Location
0	0	Bank 0	00H – 07H
0	1	Bank 1	08H – 0FH
1	0	Bank 2	10H – 17H
1	1	Bank 3	18H – 1FH

12.1.4 SP (Stack Pointer)

This register points to the top of stack in internal data memory space. It is used to store the return address of program before executing interrupt routine or subprograms. The SP is incremented before executing PUSH or CALL instruction and it is decremented after executing POP or RET(I) instruction (it always points the top of stack). A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08.

SP — Address = 81H — Reset Value = 0x07H

Stack Pointer

Bit	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.1.5 DP0 (Data Pointer 0)

These registers are intended to hold 16-bit address in the indirect addressing mode used by MOVX (move external memory), MOVC (move program memory) or JMP (computed branch) instructions. They may be manipulated as 16-bit register or as two separate 8-bit registers. DP0H holds higher byte and DP0L holds lower byte of indirect address.

It is generally used to access external code or data space, e.g.:

MOVCA,@A+DPTR (code space)

MOVA,@DPTR (data space)

DP0L — Address = 82H — Reset Value = 0x00H

Data Pointer 0 Low Byte

Bit	DP0L[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DP0H — Address = 83H — Reset Value = 0x00H

Data Pointer 0 High Byte

Bit	DP0H[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.1.6 DP1 (Data Pointer 1)

The dual data pointer accelerates the movement of block data. The standard DPTR is a 16-bit register that is used to address external memory, or peripherals. The standard data pointer is called DPTR0 and the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit (DPS) is located in the LSB of AUX register (AUX.1).

The user switches between DPTR0 and DPTR1 by toggling the DPS bit. All DPTR-related instructions use the currently selected DPTR for any activity.

DP1L — Address = 84H — Reset Value = 0x00H

Data Pointer 1Low Byte

Bit	DP1L[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DP1H — Address = 85H — Reset Value = 0x00H

Data Pointer 1 High Byte

Bit	DP1H[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.1.7 AUX(Auxiliary Register)

AUX Address = 8EH Reset Value = 0x11H

Auxiliary Register

Bit	LVD_EN	LVD	-----	ITS	SMOD	BRS	DPS	CP
	7	6	5	4	3	2	1	0
Type	R/W	R	X	R/W	R/W	R/W	R/W	R

LVD_EN	Low voltage detect enable : 1: Enable
LVD	Low voltage detect status. : 1:Low voltage occur
ITS	MCU instruction timing select. : 0:1T 1:2T
SMOD	Serial Port (UART) baud rate select.
BRS	Serial Port (UART) baud rate generator select.
DPS	Data pointer register select : 0 : Select DPTR Register DP0H, DP0L 1 : Select DPTR Register DP1H, DP1L
CP	Code protect : 0 : Non-protect 1: Protect

12.1.8 RCON (Internal RAM Control Register)

256 bytes of on-chip expanded RAM are provided and can be accessed by external memory addressing method only (instruction MOVX). The address space of instruction MOVX @Ri,A (i= 0,1) is determined by RCON [7:0] of RCON. The default setting of RCON [7:0] is F0H.

RCON Address = 86H Reset Value = 0xF0H

Internal RAM Control Register

Bit	RCON[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.2 GPIO

Four I/O ports are available: Port0, Port1, Port2, and Port3.
All 32port pins on MDRFD0 can configure to one of four modes : quasi-bidirectional (standard 8051 port outputs),push-pull output, open drain output, or input-only. All port pins default to input-only mode after reset. Two configuration registers (PINSETx, PINCONFGx) for each port select the output mode for each port pin.

SFR	Description	address	Reset value
P0	Port 0	80H	FFH
P1	Port 1	90H	FFH
P2	Port 2	A0H	FFH
P3	Port 3	B0H	FFH
PINCONG1	Pin Configure Register 1	F8H	AAH
PINCONG2	Pin Configure Register 2	F9H	AAH
PINCONG3	Pin Configure Register 3	FAH	A0H
PINCONG4	Pin Configure Register 4	FBH	AAH
PINCONG5	Pin Configure Register 5	FCH	AAH
PINCONG6	Pin Configure Register 6	FDH	A0H
PINCONG7	Pin Configure Register 7	C7H	0AH
PINSET1	Pin I/O Setting Register 1	F1H	AAH
PINSET2	Pin I/O Setting Register 2	F2H	AAH
PINSET3	Pin I/O Setting Register 3	F3H	0AH
PINSET4	Pin I/O Setting Register 4	F4H	00H
PINSET5	Pin I/O Setting Register 5	F5H	80H
PINSET6	Pin I/O Setting Register 6	F6H	0AH
PINSET7	Pin I/O Setting Register 7	F7H	FFH

12.2.1 Port

P0 Address = 80H Reset Value = 0XFFH
Port 0

Bit	-----	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P1 Address = 90H Reset Value = 0XFFH
Port 1

Bit	-----	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P2 Address = A0H Reset Value = 0XFFH
Port 2

Bit	P2.7	P2.6	P2.5	P2.4	P2.3	-----	-----	-----
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	X	X	X

P3 Address = B0H Reset Value = 0XFFH
Port 3

Bit	-----	-----	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

12.2.2 PINCONG (Pin Configure Register)

PINCONG1 Address = F8H Reset Value = 0xAAH

Pin Configure Register 1

Bit	CH4CONG[1:0]		CH5CONG[1:0]		CH6CONG[1:0]		CH7CONG[1:0]	
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)

01 : Push-pull output

10 : Input-only (High impedance)

11 : Open drain output

PINCONG2 Address = F9H Reset Value = 0xAAH

Pin Configure Register 2

Bit	CH0P CONG[1:0]		CH1P CONG[1:0]		CH2CONG[1:0]		CH3CONG[1:0]	
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)

01 : Push-pull output

10 : Input-only (High impedance)

11 : Open drain output

PINCONG3 Address = FAH Reset Value = 0xA0H

Pin Configure Register 3

Bit	XCONG[1:0]		UCONG[1:0]		XTALO CONG[1:0]		XTALI CONG[1:0]	
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)

01 : Push-pull output

10 : Input-only (High impedance)

11 : Open drain output

PINCONG4 Address = FBH Reset Value = 0xAAH

Pin Configure Register 4

Bit	ZCONG[1:0]		WCONG[1:0]		YCONG[1:0]		VCONG[1:0]	
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)

01 : Push-pull output

10 : Input-only (High impedance)

11 : Open drain output

PINCONG5 Address = FCH Reset Value = 0xAAH

Pin Configure Register 5

Bit	DOCPNCONG[1:0]		CH1N CONG[1:0]		CH0N CONG [1:0]		AOCPCONG [1:0]	
	7	6	5	4	3	2	1	0
Ty	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)

01 : Push-pull output

10 : Input-only (High impedance)

11 : Open drain output

PINCONG6 Address = FDH Reset Value = 0xA0H

Pin Configure Register 6

Bit	DAC2PCONG [1:0]		DAC1PCONG [1:0]		RXCONG[1:0]		TXCONG[1:0]	
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)

01 : Push-pull output

10 : Input-only (High impedance)

11 : Open drain output

PINCONG7 Address = C7H Reset Value = 0x0AH

Pin Configure Register 7

Bit	-----		-----		DAC4PCONG [1:0]		DAC3PCONG [1:0]	
	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

00 : Quasi-bidirectional(standard 8051 port outputs)

01 : Push-pull output

10 : Input-only (High impedance)

11 : Open drain output

12.2.3 PINSET (Pin I/O Setting Register)

PINSET1 Address = F1H Reset Value = 0xAAH

Pin I/O Setting Register 1

Bit	CH4SET[1:0]		CH5SET[1:0]		CH6SET[1:0]		CH7SET[1:0]	
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : No pull

01 : Pull down

10 : Pull up

11 : No pull

PINSET2 Address = F2H Reset Value = 0xAAH

Pin I/O Setting Register 2

Bit	CH0PSET[1:0]		CH1P SET[1:0]		CH2SET[1:0]		CH3SET[1:0]	
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : No pull

01 : Pull down

10 : Pull up

11 : No pull

PINSET3 Address = F3H Reset Value = 0x0AH

Pin I/O Setting Register 3

Bit	XSET[1:0]		USET[1:0]		XTALO SET[1:0]		XTALI SET[1:0]	
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : No pull

01 : Pull down

10 : Pull up

11 : No pull

PINSET4 Address = F4H Reset Value = 0x00H

Pin I/O Setting Register 4

Bit	ZSET[1:0]		WSET[1:0]		YSET[1:0]		VSET[1:0]	
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : No pull

01 : Pull down

10 : Pull up

11 : No pull

PINSET5 Address = F5H Reset Value = 0x80H

Pin I/O Setting Register 5

Bit	DOCPNSET[1:0]		CH1N SET[1:0]		CH0N SET [1:0]		AOCPSET[1:0]	
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

00 : No pull

01 : Pull down

10 : Pull up

11 : No pull

PINSET6 Address = F6H Reset Value = 0x0AH

Pin I/O Setting Register 6

Bit	DAC2SET[1:0]		DAC1SET[1:0]		RXSET[1:0]		TXSET [1:0]	
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TXSET[1:0], RXSET[1:0], HUNSET[1:0]

00 : No pull

01 : Pull down

10 : Pull up

11 : No pull

PINSET7 Address = F7H Reset Value = 0xF0H

Pin I/O Setting Register 7

Bit	MOCS	----	DOCPNDBT[1:0]		DAC4 SET4[1:0]		DAC3SET[1:0]	
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MOCS

0 : U、V、W、X、Y、Z is GPIO Mode.

1: U、V、W、X、Y、Z is SVPWM Mode.(ADC CH0& CH1 Auto Converter)

MOCS=1, Pin set must to Push-pull output mode. (PINSET3 [7:4] and PINSET3 [7:0])

DOCPNDBT (De-bounce time for digital OCPN)

00 : 0nS

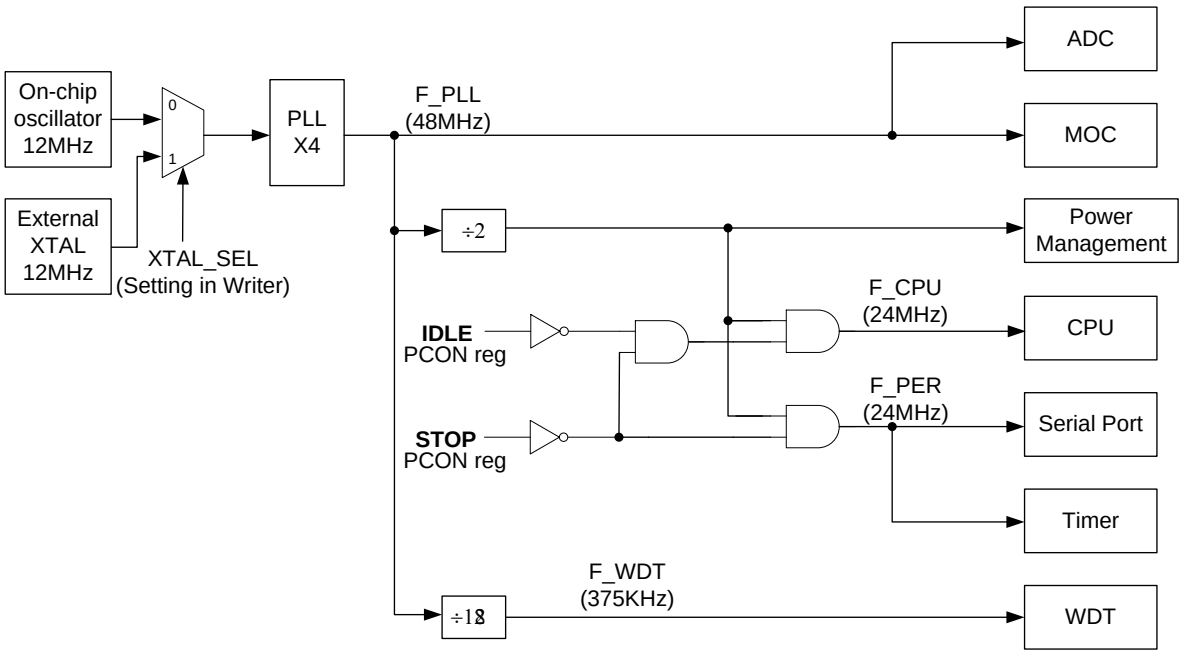
01 : 250nS

10 : 500nS

11 : 1000nS

12.3 Clock Structure

The clock source of the device may be either external, or internal. The external crystal(12MHz)is connect to pins XTALI and XTALO. The internal clock source (on-chip oscillator) is run at 12MHz. The choice of internal, or external, clock source is setting by Writer.



12.4 Timer

The MDRFD0 has three 16-bit timer/counter registers: Timer0, Timer1 and Timer2. All can be configured for counter, or timer, operations.
In addition to the “timer” or “counter” selection, Timer0 and Timer1 have four operating modes from which to select which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1,and 2 are the same for both timer/counters. Mode 3 is different.

	Timer0	Timer1	Timer2
Mode 0	13-bit timer/counter	13-bit timer/counter	13-bit timer/counter
Mode 1	16-bit timer/counter	16-bit timer/counter	16-bit timer/counter
Mode 2	8-bit auto-reload timer/counter	8-bit auto-reload timer/counter	8-bit auto-reload timer/counter
Mode 3	two independent 8-bit timers/counters	stop	8-bit timers/counters

Two Special Function registers (TMOD andTCON) are used to select the appropriate mode.

SFR	Description	address	Reset value
PFCON	Peripheral Frequency Control Register	D1H	00H
TMOD	Timer 0/1 Mode Register	89H	00H
TCON	Timer 0/1 Control Register	88H	00H
T2CON	Timer2 Control Register	C8H	00H
TH0	Timer0 High byte	8CH	00H
TL0	Timer0 Low byte	8AH	00H
TH1	Timer1 High byte	8DH	00H
TL1	Timer1 Low byte	8BH	00H
TH2	Timer2 High byte	B5H	00H
TL2	Timer2 Low byte	B4H	00H

12.4.1 PFCON (Peripheral Frequency Control Register)

PFCON Address = D1H Reset Value = 0x00H

Peripheral Frequency Control Register

Bit	7	6	5	4	3	2	1	0
	-----	-----	SRELPS[1:0]		T1PS[1:0]		T0PS[1:0]	
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

SRELPS[5:4]	Serial port (UART) Prescaler select : 00 :F_PER/64 01 :F_PER/32 10 :F_PER/16 11 :F_PER/8
T1PS[3:2]	Timer1(T1) Prescaler select : 00 :F_PER/12 01 :F_PER 10 :F_PER/96 11 :-----
T0PS[1:0]	Timer0(T0) Prescaler select : 00 :F_PER/12 01 :F_PER 10 :F_PER/96 11 :-----

12.4.2 TMOD (Timer 0/1 Mode Register)

TMOD register is used in configuration of MCUTimer0 and Timer1.

TMOD Address = 89H Reset Value = 0x00H

Timer 0/1 Mode Register

Bit	GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

GATE1	Timer1 gate control :
[7]	If set, enables external gate control (pin INT1N) for Counter1. When INT1N is high, and TR1 bit is set, the Counter1 is incremented every falling edge on INT1N input pin
C/T1	Timer1 counter/timer select :
[6]	0 : Timer
	1 : Counter
GATE0	Timer 0 gate control :
[3]	If set, enables external gate control (pin INT0N) for Counter0. When INT0N is high, and TR0 bit is set, the Counter0 is incremented every falling edge onINT0N input pin
C/T0	Timer0 counter/timer select :
[2]	0 : Timer
	1 : Counter

T1M1 /T0M1	T1M0 /T0M0	Mode	Function
0	0	Mode0	13-bit Counter/Timer, with 5 lower bits in TL0 (TL1) register and 8 bits in TH0 (TH1) register (for Timer0 or Timer1, respectively). The 3 high-order bits of TL0 (TL1) are zeroed whenever Mode 0 is enabled. (Not auto-reload)
0	1	Mode1	16-bit Counter/Timer. (Not auto-reload)
1	0	Mode2	8 -bit auto-reload Counter/Timer. The reload value is kept in TH0 (TH1), while TL0 (TL1) is incremented every clock cycle. Reloaded from TH0 (TH1) at overflow.
1	1	Mode3	For Timer1: Timer1 is stopped. For Timer0: Timer0 acts as two independent 8 bit Timers / Counters – TL0, TH0. (Not auto-reload)

12.4.3 TCON (Timer 0/1Control Register)

TCON register is used to control operation of these modules.MDRFD0 includes two external digital interrupt sources INT0N and INT1N), with dedicated interrupt sources. INT0N and INT1N are configurable as falling edge or low level. The IT0 and IT1 bits in TCON select level- or edge-sensitive.IE0 and IE1 in the TCON register serve as the interrupt-pending flags for the INT0N and INT1N external interrupts, respectively.

TCON Address = 88H Reset Value = 0x00H

Timer 0/1 Control Register

Bit	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TF1	Timer1 overflow flag : Bit set by hardware when Timer1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR1	Timer1 run control : 0 : Stop 1 : Run
TF0	Timer0 overflow flag : Bit set by hardware when Timer1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR0	Timer0run control : 0 : Stop 1 : Run
IE1	External interrupt 1 flag : Set by hardware, when External interrupt (INT1N) is observed. Cleared by hardware when interrupt is processed.
IT1	External interrupt 1 type control : 0 : External interrupt 1 is activated at low level on input pin 1 : External interrupt 1 is activated at falling edge on input pin
IE0	External interrupt 0 flag : Set by hardware, when External interrupt (INT0N) is observed. Cleared by hardware when interrupt is processed.
IT0	External interrupt 0 type control : 0 : External interrupt 0 is activated at low level on input pin 1 : External interrupt 0 is activated at falling edge on input pin

The TF0, TF1 (Timer0 andTimer1 overflow flags), IE0 and IE1 (External interrupt 0 and 1 flags) will be automatically cleared by hardware when the corresponding service routine is called.

12.4.4 T2CON (Timer2 Control Register)

T2CON is used to control Timer2 run/stop, mode, prescaler.

T2CON Address = C8H Reset Value = 0x00H

Timer2 Control Register

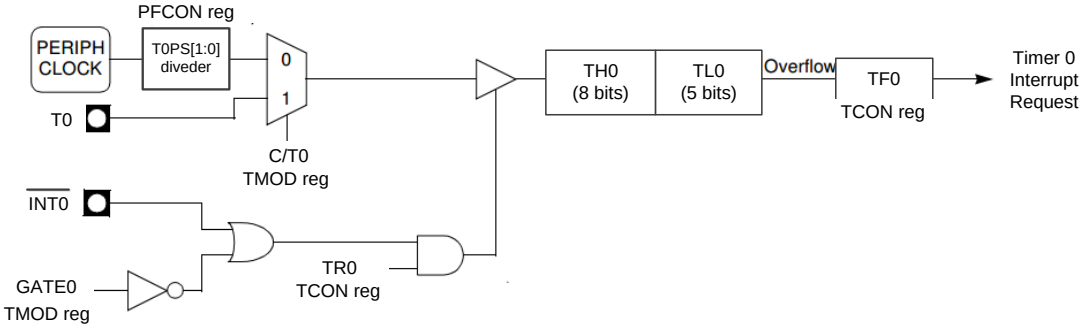
Bit	-----	-----	TF2	TR2	T2M1	T2M0	T2PS1	T2PS0
	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

TF2	Timer2 overflow flag :

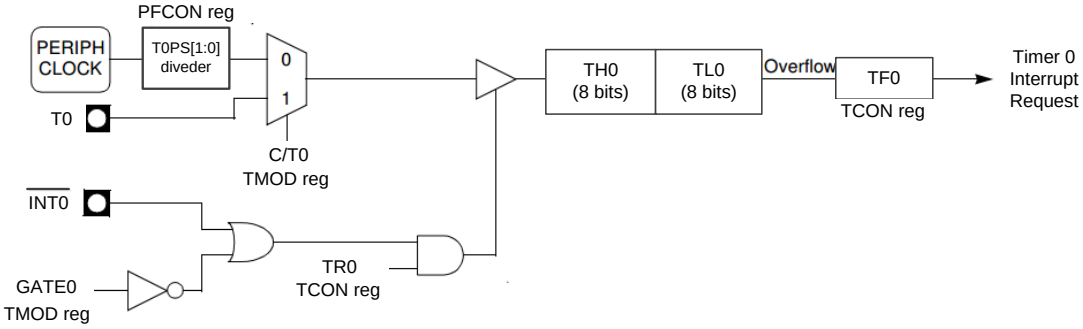
	Bit set by hardware when Timer2 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR2	Timer2run control : 0 : Stop 1 : Run
T2PS[1:0]	Timer2(T2) Prescaler select : 00 :F_PER/12 01 : F_PER 10 : F_PER/96 11 :-----

T2M1	T2M0	Mode	Function
0	0	Mode0	13-bit Timer, with 5 lower bits in TL2 register and 8 bits in TH2 register.(Not auto-reload)
0	1	Mode1	16-bit Timer. (Not auto-reload)
1	0	Mode2	8 -bit auto-reload Timer. The reload value is kept in TH2, while TL2 is incremented every clock cycle. Reloaded from TH2 at overflow.
1	1	Mode3	8 bit Timers. (Not auto-reload)

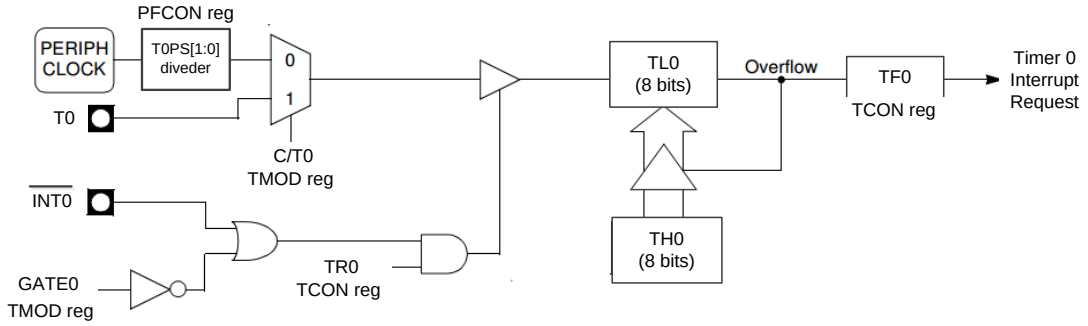
12.4.5 Timer0 Mode 0



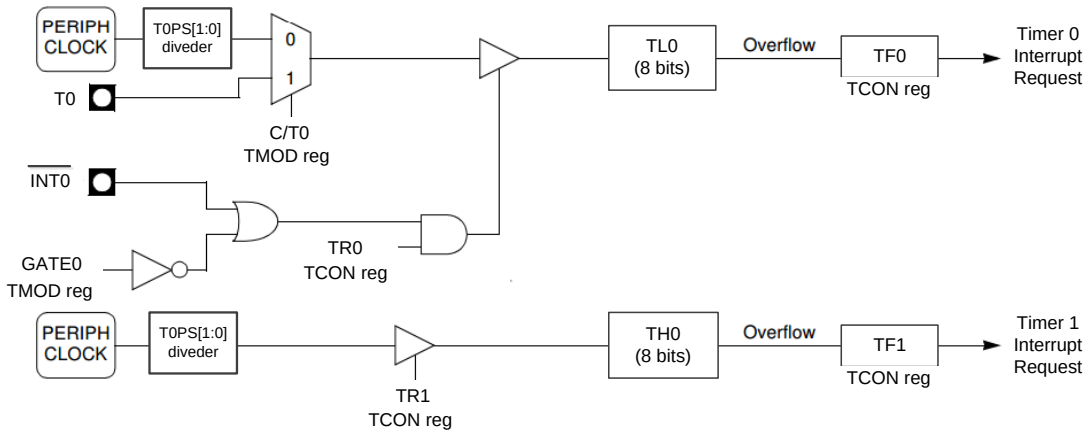
12.4.6 Timer0 Mode 1



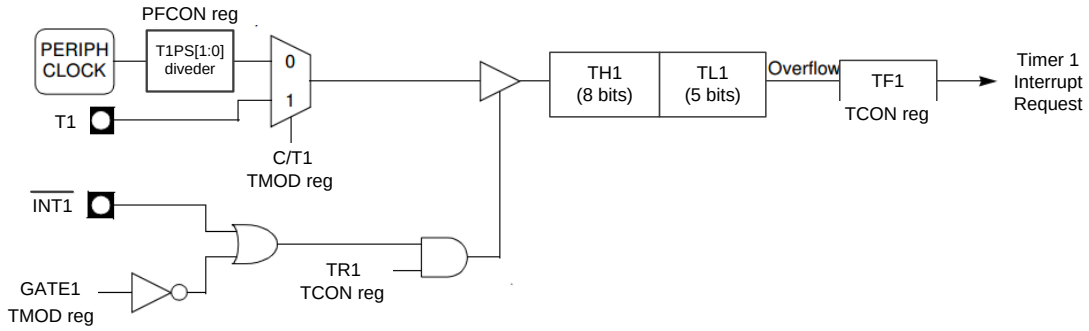
12.4.7 Timer0 Mode 2



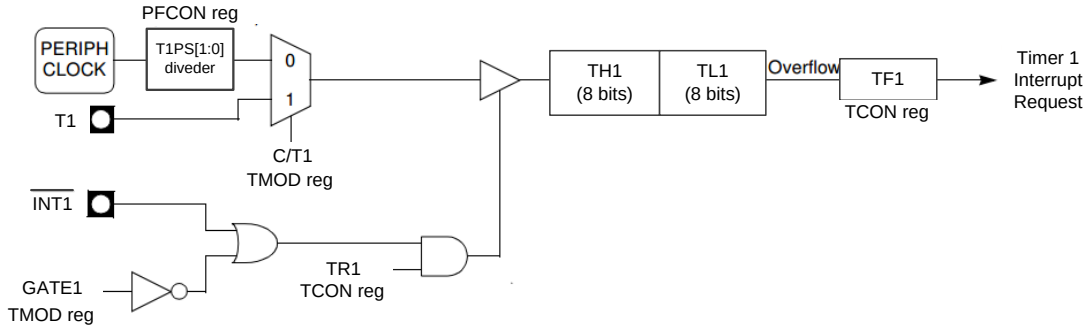
12.4.8 Timer0 Mode 3



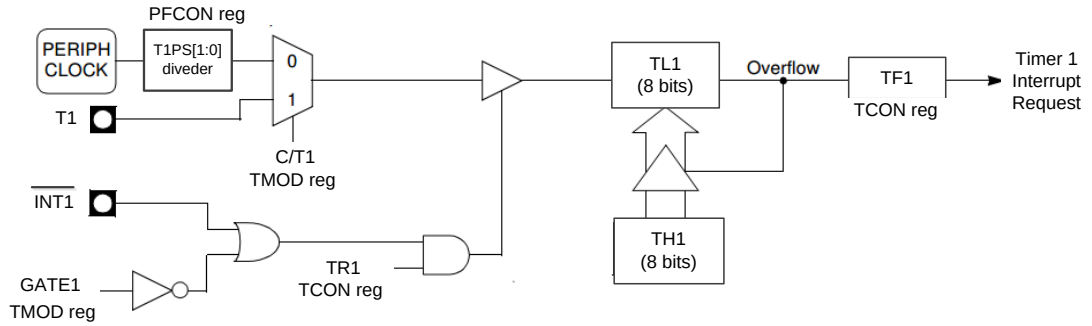
12.4.9 Timer1 Mode 0



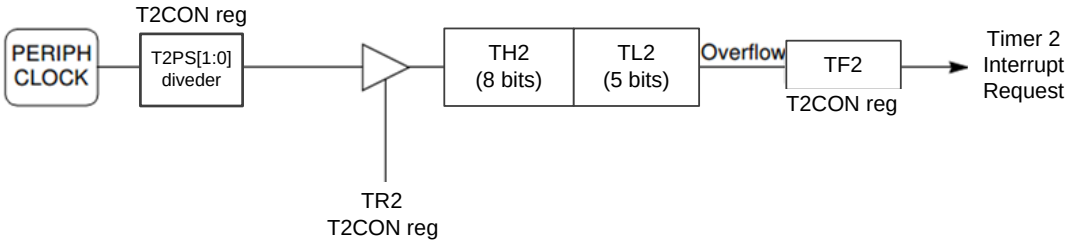
12.4.10 Timer1 Mode 1



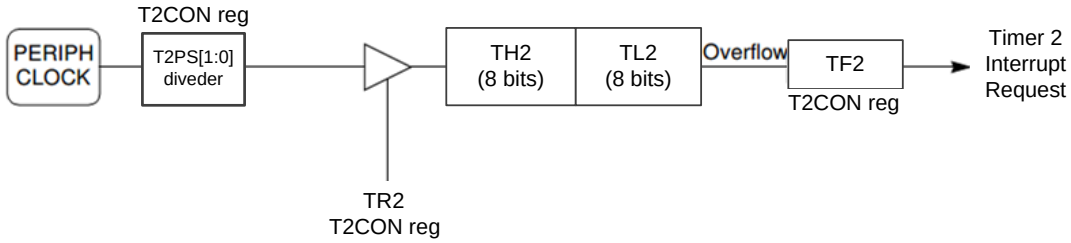
12.4.11 Timer1 Mode 2



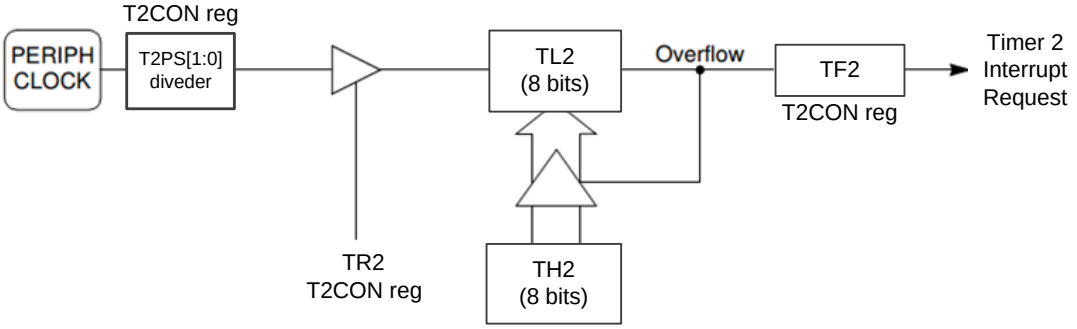
12.4.12 Timer2 Mode 0



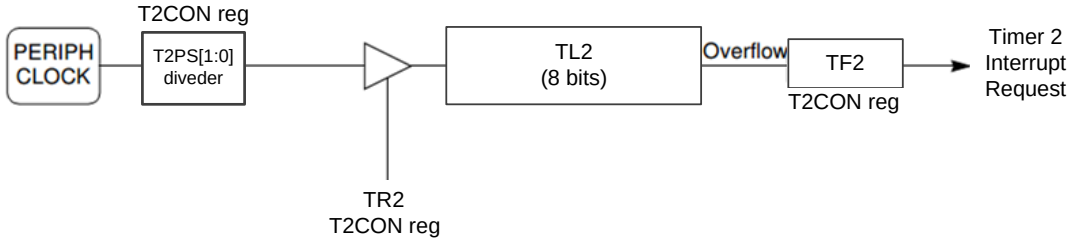
12.4.13 Timer2 Mode 1



12.4.14 Timer2 Mode 2



12.4.15 Timer2 Mode 3



12.5 Watchdog Timer

The Watchdog Timer (WDT) is a8-bit free-running counter that generates a reset signal or interrupt (WDTC.6) if it overflows. It can help the application software to recover from an abnormal condition. The WDT is independent from Timer0, Timer1, or Timer2. The F_WDT is 375KHz, it is from on-chip RC oscillator.

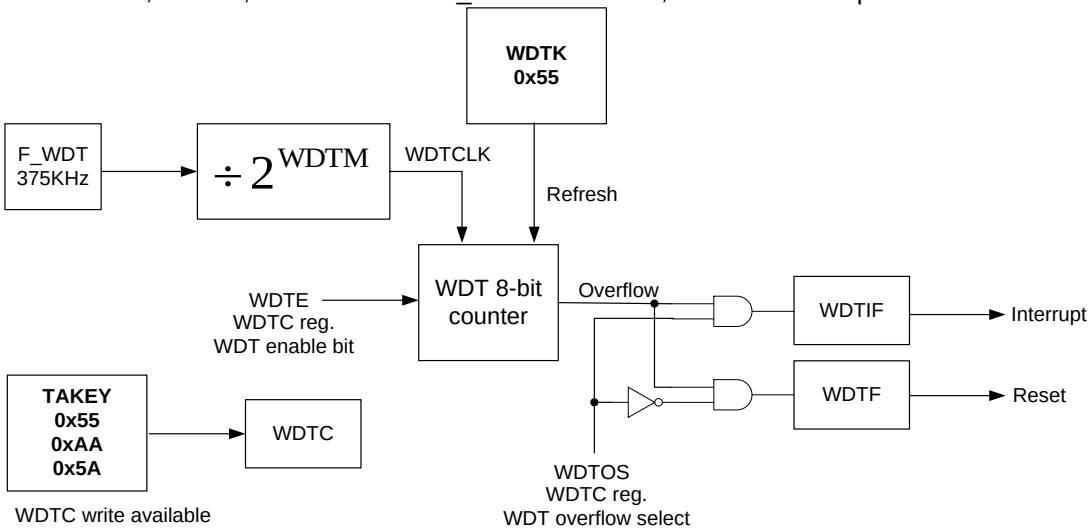


Figure 12.5.1 WDT block diagram

WDTCLK = $F\_WDT \times \frac{1}{2^{WDTM}}$

WDT (8-bit counter) overflow time = $\frac{256}{WDTCLK}$

SFR	Description	address	Reset value
RSTS	Reset Source Register	FEH	0AH
TAKEY	Time Access Key Register	FFH	00H
WDTC	Watchdog Timer Control Register	B6H	04H
WDTK	Watchdog Timer Refresh Key	B7H	00H

RSTS Address = FEH Reset Value = 0x0AH

Reset Source Register

Bit	-----	-----	-----	WDTRF	PINRF[1:0]		PORF[1:0]	
	7	6	5	4	3	2	1	0
Type	X	X	X	R/W	R/W	R/W	R/W	R/W

WDTRF	Watchdog timer reset flag. This flag is set to 1 if the Watchdog Timer Reset caused the reset.
PINRF[1:0]	$\overline{RST}$ pin reset flag. This flag is set to 10b if the $\overline{RST}$ pin caused the reset. Clear by firmware.
PORF[1:0]	POR reset flag. This flag is set to 10b if the POR caused the reset. Clear by firmware.

12.5.1 WDTC (Watchdog Timer Control Register)

WDTC Address = B6H Reset Value = 0x04H

Watchdog Timer Control Register

Bit	-----	WDTOS	WDTE	-----	WDTM[3:0]			
	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	X	R/W	R/W	R/W	R/W

WDTOS	Watchdog timer overflow select : 0 : When WDT overflow, enable WDT reset. 1 : When WDT overflow, enable WDT interrupt.
WDTE	Watchdog timer enable : 0 : Disable WDT. 1 : Enable WDT.
WDTM[3:0]	WDT clock divider : WDTCLK = $375KHz \times \frac{1}{2^{WDTM}}$ (default is 375K / 16)

12.5.2 TAKEY (Time Access Key Register)

TAKEY Address = FFH Reset Value = 0x00H

Time Access Key Register

Bit	TAKEY[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WDTC default is read only, must write three specific values 55H, AAH and 5AH to the TAKEY enable the WDTC write available.
The sequence is:
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah

12.5.3 WDTK (Watchdog Timer Refresh Key)

WDTK Address = B7H Reset Value = 0x00H

Watchdog Timer Refresh Key

Bit	WDTK[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The application must write 0x55 into the WDTK register, for the Watchdog timer to be cleared.

For example, enable the watchdog with a time-out reset period of 5.461ms.

Following write sequence:
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah ; WDTC write is available.
MOV WDTC, #23h ; WDTM [3:0] = 0111b. WDTE =1 to enable the WDT.
MOV WDTK, #55h ;Refresh WDT.

12.6 Serial Port (UART)

The Serial Port provides a flexible full-duplex synchronous/asynchronous receiver/transmitter, called UART. The communication rate can be set by configuring the baud rate in SFRs. The two serial buffers consist of two separate registers, a transmit buffer and a receive buffer. Writing data to the SFR SBUF, transfers the data to the serial output buffer and starts the transmission. Reading from the SBUF, reads data from the serial receive buffer. The serial port can simultaneously transmit and receive data. It can also buffer 1 byte at receive, which prevents the receive data from being lost if the CPU reads the second byte before the transmission of the first byte is completed.

SFR	Description	address	Reset value
AUX	Auxiliary	8EH	11H
PFCON	Peripheral Frequency Control Register	D1H	00H
SCON	Serial Port Control Register	98H	00H
SBUF	Serial Port Data Buffer	99H	00H
SRELH	Serial Port Reload Register High	9BH	00H
SRELL	Serial Port Reload Register Low	9AH	00H

AUX Address = 8EH Reset Value = 0x11H

Auxiliary Register

Bit	LVD_EN	LVD	-----	ITS	SMOD	BRS	DPS	CP
	7	6	5	4	3	2	1	0
Type	R/W	R	X	R/W	R/W	R/W	R/W	R

LVD_EN	Low voltage detect enable : 1: Enable
LVD	Low voltage detect status. : 1: Low voltage occur
ITS	MCU instruction timing select. : 0:1T 1:2T
SMOD	Serial Port (UART) baud rate select.
BRS	Serial Port (UART) baud rate generator select.
DPS	Data pointer register select : 0 : Select DPTR Register DP0H, DP0L 1 : Select DPTR Register DP1H, DP1L
CP	Code protect : 0 : Non-protect 1: Protect

MDRFD0

PFCON Address = D1H Reset Value = 0x00H

Peripheral Frequency Control Register

Bit	-----	-----	SRELPS[1:0]		T1PS[1:0]		T0PS[1:0]	
	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

SRELPS[1:0]	Serial port (UART) Prescaler select : 00 :F_PER/64 01 :F_PER/32 10 :F_PER/16 11 :F_PER/8
T1PS[1:0]	Timer1(T1) Prescaler select : 00 :F_PER/12 01 :F_PER 10 :F_PER/96 11 :-----
T0PS[1:0]	Timer0(T0) Prescaler select : 00 : F_PER/12 01 : F_PER 10 : F_PER/96 11 :-----

12.6.1 SCON (Serial Port Control Register)

The SCON register controls the function of Serial Port (UART).

SCON Address = 98H Reset Value = 0x00H

Serial Port Control Register

Bit	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SM0	SM1	Mode	Description	Baud Rate	
0	0	Mode 0	Shift register	F_PER/12	
0	1	Mode 1	8bit UART	Variable	
1	0	Mode 2	9bit UART	Depends on SMOD (AUX.3)	
				SMOD	Baud Rate
				0	F_PER/64
				1	F_PER/32
1	1	Mode 3	9bit UART	Variable	

SM2	Multiprocessor communication enable
REN	Serial reception enable : 0 : Serial reception at Serial Port is disabled. 1 :Serial reception at Serial Port is enabled.
TB8	Transmitter bit 8 : This bit is used while transmitting data through Serial Port in Modes 2 and 3. The state of this bit corresponds with the state of the 9th transmitted bit (e.g. parity check or multiprocessor communication). It is controlled by software.
RB8	Received bit 8 : This bit is used while receiving data through Serial Port 0 in Modes 2 and 3. It reflects the state of the 9th received bit. In Mode 1, if multiprocessor communication is enabled (sm2 = 0), this bit is the stop bit that was received. In Mode 0 this bit is not used.
TI	Transmit interrupt flag : (completion of a serial transmission) It is set by hardware at the end of bit 8 in mode 0 or at the beginning of a stop bit in other modes. It must be cleared by software.
RI	Receive interrupt flag : (It must be cleared by software.) It is set by hardware after completion of a serial reception at Serial Port 0. It is set by hardware at the end of bit 8 in mode 0 or in the middle of a stop bit in other modes.

Serial Port working in modes 1 or mode 3:

When BRS = 0 (AUX.2)

TIPS[1:0] = 00b

$$\text{Baud rate} = \frac{2^{SMOD}}{32\times(256\text{-TH1})} \times \frac{F\_PER}{12}$$

TIPS[1:0] = 01b

$$\text{baud rate} = \frac{2^{SMOD}}{32\times(256\text{-TH1})} \times F\_PER$$

TIPS[1:0] = 10b

$$\text{baud rate} = \frac{2^{SMOD}}{32\times(256\text{-TH1})} \times \frac{F\_PER}{96}$$

When BRS = 1 (AUX.2)

SRELPS[1:0] = 00b

$$\text{baud rate} = \frac{2^{SMOD}}{2^{10}-SREL[H,L]} \times \frac{F\_PER}{64}$$

SRELPS [1:0] = 01b

$$\text{baud rate} = \frac{2^{SMOD}}{2^{10}-SREL[H,L]} \times \frac{F\_PER}{32}$$

SRELPS [1:0] = 10b

$$\text{baud rate} = \frac{2^{SMOD}}{2^{10}-SREL[H,L]} \times \frac{F\_PER}{16}$$

SRELPS [1:0] = 11b

$$\text{baud rate} = \frac{2^{SMOD}}{2^{10}-SREL[H,L]} \times \frac{F\_PER}{8}$$

12.6.2 SBUF (Serial Port Data Buffer)

Writing data to this register sets data in serial output buffer and starts the transmission through Serial Port. Reading from the SBUF, reads data from the serial receive buffer.

SBUF	Address = 99H					Reset Value = 0x00H		
Serial Port Data Buffer								
Bit	SBUF[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.6.3 SREL (Serial Port Reload Register)

Serial Port Reload Register is used for Serial Port baud rate generation. Only 10 bits are used, where 8 bits from the SRELL as lower bits and 2 bits from the SRELH (SRELH.1, SRELH.0) as higher bits.

SRELL	Address = 9AH					Reset Value = 0x00H		
Serial Port Reload Register Low								
Bit	SREL[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SRELH	Address = 9BH					Reset Value = 0x00H		
Serial Port Reload Register High								
Bit	-----	-----	-----	-----	-----	-----	SREL.9	SREL.8
	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	X	R/W	R/W

12.7Power Management

The Power Control Register (PCON) is used to control the MDRFD0 STOP and IDLE power management modes.

PCON	Address = 87H					Reset Value = 0x00H		
Power Control Register								
Bit	-----	-----	-----	-----	-----	-----	STOP	IDLE
	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	X	R/W	R/W

STOP	Stop mode bit.
[1]	Setting this bit activates STOP operation. (read as 0)
IDLE	Idle mode bit.
[0]	Setting this bit activates IDLE mode operation. (read as 0)

12.7.1 STOP MODE

Setting the STOP Mode Select bit (PCON.1) causes the controller core to enter STOP mode as soon as the instruction that sets the bit completes execution. In STOP mode the CPU, GPIO, UART, and Timers are stopped, but the ADC, MOC, and WDT is still work.

STOP mode can terminate by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

The assertion of an enabled interrupt will cause the STOP Mode Selection bit (PCON.1) to be cleared and the CPU to resume operation.

12.7.2 IDLE MODE

Setting the IDLE Mode Select bit (PCON.0) causes the hardware to halt the CPU and enter IDLE mode as soon as the instruction that sets the bit completes execution.
In IDLE mode only the CPU is stop. All internal registers and memory maintain their original data.
IDLE mode can terminate by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.
The assertion of an enabled interrupt will cause the IDLE Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation.

12.8 Reset

The reset logic is used to place the device into a known state.
MDRFD0 provides Power-on Reset flag, External Reset RSTN flag and Watchdog timer Reset flag to monitor reset status. The source of the reset can be monitor.

12.8.1 RSTS (Reset Source Register)

RSTS Address = FEH Reset Value = 0x0AH
Reset Source Register

Bit	-----	-----	-----	WDTRF	PINRF[1:0]		PORF[1:0]	
	7	6	5	4	3	2	1	0
Type	X	X	X	R/W	R/W	R/W	R/W	R/W

WDTRF	Watchdog timer reset flag.
[4]	This flag is set to 1 if the Watchdog Timer Reset caused the reset.
PINRF	RSTN pin reset flag.
[3:2]	This flag is set to 10b if the RSTN pin caused the reset. Clear by firmware.
PORF	POR reset flag.
[1:0]	This flag is set to 10b if the POR caused the reset. Clear by firmware.

12.9 Interrupt Controller

The ISR - Interrupt Service Routine unit, is a subcomponent responsible for interrupt handling. It receives up to 13 interrupt requests. Each interrupt source has its own request flag that is located in devices which is a source of interrupt. No interrupt request flags are located directly in ISR. All interrupts are requested by high level on correspondent inputs to ISR. Each of the interrupt sources can be individually enabled or disabled by corresponding enable flag in IEN0, IEN1SFR registers. Additionally all interrupts can be globally enabled or disabled by the —EA flag in the IEN0 SFR. All interrupt sources are divided into 6 interrupts groups. Each of the interrupt groups can have one of four interrupt priority levels assigned. The interrupt priority level is defined by flags located in the IP0 and IP1 SFR registers.

Interrupt Number (use Keil C Tool)	Interrupt Vector Address	Interrupt Request Flags
0	0003H	IE0 – External interrupt 0
1	000BH	TF0 – Timer0 interrupt
2	0013H	IE1 – External interrupt 1
3	001BH	TF1 – Timer1 interrupt
4	0023H	SPIF(TI, RI)– Serial port interrupt
5	002BH	TF2 – Timer2 interrupt
6	0033H	-----
7	003BH	-----
8	0043H	OCPSIF – OCP Short interrupt
9	004BH	ADCIF –ADC interrupt
10	0053H	MPWMMINIF–MPWM MIN interrupt
11	005BH	MPWMMAXIF–MPWM MAX interrupt
12	0063H	-----
13	006BH	LVDIF – Low voltage detect interrupt
14	0073H	WDTIF – Watchdog timer interrupt
15	007BH	CAPTUREIF –CAPTURE interrupt

Table12.9.1 Interrupt vectors

Group priority	Interrupt Group	Highest priority in group		Lowest priority in group
Highest	Group0	LVDIF	IE0	-----
	Group1	WDTIF	TF0	-----
	Group2	OCPSIF	ADCIF	IE1
	Group3	MPWMMINIF	MPWMMAXIF	TF1
	Group4	-----	SPIF(TI, RI)	-----
Lowest	Group5	CAPIF	TF2	-----

Table12.9.2 Interrupt Priority Groups

SFR	Description	address	Reset value
IEN0	Interrupt Enable Register 0	A8H	00H
IEN1	Interrupt Enable Register 1	B8H	00H
IRCON1	Interrupt Request Register 1	C0H	00H
IP0	Interrupt Priority Register 0	A9H	00H
IP1	Interrupt Priority Register 1	B9H	00H

12.9.1 IEN0 (Interrupt Enable Register 0)

IEN0 Address = A8H Reset Value = 0x00H

Interrupt Enable Register 0

Bit	EA	-----	ET2	ESP	ET1	EX1	ET0	EX0
	7	6	5	4	3	2	1	0
Type	R/W	X	R/W	R/W	R/W	R/W	R/W	R/W

EA	Interrupts enable :
[7]	0 : Disable All interrupts.
	1 : Enable interrupt.
ET2	Timer2 interrupt enable:
[5]	0 : Disable Timer2 overflow interrupt.
	1 : When EA = 1, enable Timer2 overflow interrupt.
ESP	Serial port interrupt enable:
[4]	0 : Disable Serial port interrupt.
	1 : When EA = 1, enable Serial port interrupt.
ET1	Timer1 interrupt enable:
[3]	0 : Disable Timer1 overflow interrupt.
	1 : When EA = 1, enable Timer1 overflow interrupt.
EX1	External interrupt 1 enable:
[2]	0 : Disable External interrupt 1.
	1 : When EA = 1, enable External interrupt 1.
ET0	Timer0 interrupt enable:
[1]	0 : Disable Timer0 overflow interrupt.
	1 : When EA = 1, enable Timer0 overflow interrupt.
EX0	External interrupt 0 enable:
[0]	0 : Disable External interrupt 0.
	1 : When EA = 1, enable External interrupt 0.

12.9.2 IEN1 (Interrupt Enable Register 1)

IEN1 Address = B8H Reset Value = 0x00H

Interrupt Enable Register 1

Bit	CAPIE	WDTIE	LVDIE	----	MPWMMAXIE	MPWMMINIE	ADCIE	OCPSIE
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CAPIE [7]	Capture interrupt enable: 0 : Disable CAPTURE interrupt. 1 : When EA = 1, enable CAPTURE interrupt.
WDTIE [6]	Watchdog timer interrupts enable : 0 : Disable WDT interrupt. 1 : When EA = 1 and WDTOS = 1, enable WDT overflow interrupt.
LVDIE [5]	LVD (Low voltage detect) interrupt enable: 0 : Disable LVD interrupt. 1 : When EA = 1, enable LVD interrupt.
MPWMMAXIE [3]	MPWM maximum interrupt enable: 0 : Disable MPWM maximum interrupt. 1 : When EA = 1, enable MPWM maximum interrupt.
MPWMMINIE [2]	MPWM minimum interrupt enable: 0 : Disable MPWM minimum interrupt . 1 : When EA = 1, enable MPWM minimum interrupt.
ADCIE [1]	ADC interrupt enable: 0 : Disable ADC interrupt. 1 : When EA = 1, enable ADC interrupt.
OCPSIE [0]	OCP (Over current protect) Short interrupt enable: 0 : Disable OCP Short interrupt . 1 : When EA = 1, enable OCP Short interrupt.

12.9.3 IRCON1 (Interrupt Request Register 1)

IRCON1 Address = C0H Reset Value = 0x00H

Interrupt Request Register 1

Bit	CAPTUREIF	WDTIF	LVDIF	----	MPWMMAXIF	MPWMMINIF	ADCIF	OCPSIF
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CAPTIF[7]	Capture interrupt (Counter Over flow and Rising trigger) flag.
WDTIF[6]	Watchdog timer interrupts flag.
LVDIF[5]	LVD (Low voltage detect) interrupt flag.
MPWMMAXIF[3]	MPWM maximum interrupt flag.
MPWMMINIF[2]	MPWM minimum interrupt flag.
ADCIF[1]	ADC interrupt flag.
OCPSIF[0]	OCP Short interrupt flag.(AOCP and DOCPN)

12.9.4 IP (Interrupt Priority Register)

The 13 interrupt sources are grouped into 6 priority groups. For each of the groups, one of four priority levels can be selected. It is achieved by setting appropriate values in IP0 and IP1 registers. The contents of the Interrupt Priority Registers define the priority levels for each interrupt source according to the tables below.

IP0 Address = A9H Reset Value = 0x10H

Interrupt Priority Register 0

Bit	-----	-----	G5IP0	G4IP0	G3IP0	G2IP0	G1IP0	G0IP0
	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

G5IP0[5]	Group5 interrupt priority bit 0
G4IP0[4]	Group4 interrupt priority bit 0
G3IP0[3]	Group3 interrupt priority bit 0
G2IP0[2]	Group2 interrupt priority bit 0
G1IP0[1]	Group1 interrupt priority bit 0
G0IP0[0]	Group0 interrupt priority bit 0

IP1 Address = B9H Reset Value = 0x00H

Interrupt Priority Register 1

Bit	-----	-----	G5IP1	G4IP1	G3IP1	G2IP1	G1IP1	G0IP1
	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

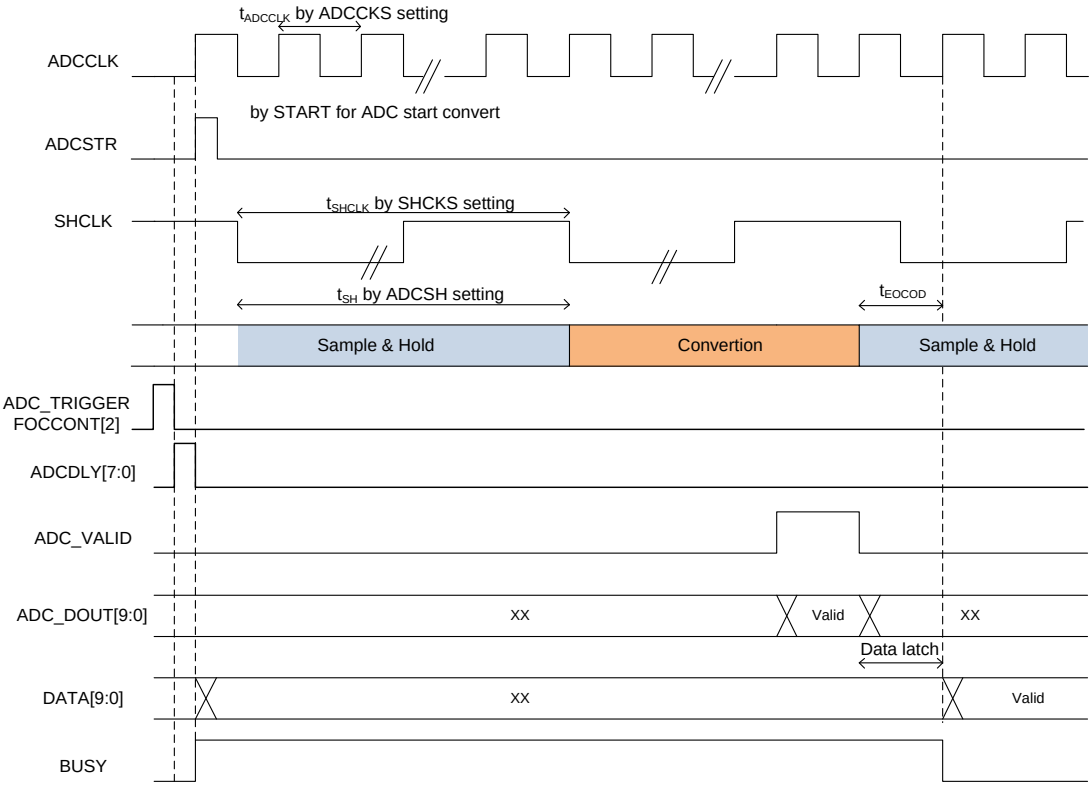
G5IP1[5]	Group5 interrupt priority bit 1
G4IP1[4]	Group4 interrupt priority bit 1
G3IP1[3]	Group3 interrupt priority bit 1
G2IP1[2]	Group2 interrupt priority bit 1
G1IP1[1]	Group1 interrupt priority bit 1
G0IP1[0]	Group0 interrupt priority bit 1

		Group x	
Level	Priority	IP1[GxIP1]	IP0 [GxIP0]
Level 0	Lowest	0	0
Level 1		0	1
Level 2		1	0
Level 3	Highest	1	1
x : 0~5			

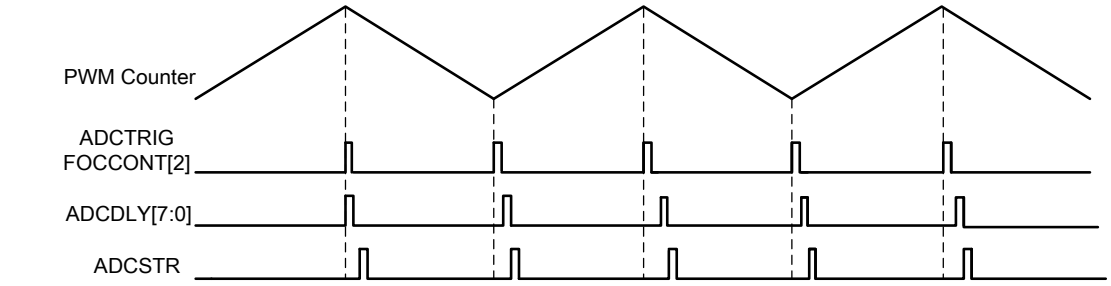
13. 10-bit Analog-to-Digital Converter (ADC)

The MDRFD0 provides eight channels 10-bit ADC. The result of the conversion is provided at ADCD [9:0].

SFR	Description	address	Reset value
ADCCONT	ADC Control Register	C2H	00H
ADCDLY	ADC Sample Delay (For CH0&CH1)	C5H	33H
ADCSTR	ADC Start Convert and Setting Register	C1H	00H
ADCD1	ADC Data Register 1	C3H	00H
ADCD2	ADC Data Register 2	C4H	00H
ADC1OS_L	ADC1 Offset Value Register Low Byte	C9H	00H
ADC1OS_H	ADC1 Offset Value Register High Byte	CAH	02H
ADC2OS_L	ADC2 Offset Value Register Low Byte	CBH	00H
ADC2OS_H	ADC2 Offset Value Register High Byte	CCH	02H



ADC conversion timing



ADC CH0 and CH1 conversion

13.1 ADCCONT (ADC Control Register)

ADCCONT — Address = C2H — Reset Value = 0x80H

ADC Control Register

Bit	ADCPD	ADCSH[1:0]		ADCDS	ADCCKS	ADDCH[2:0]		
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ADCPD [7]

ADC power down control register :

0 : Normal

1 : Power down

ADCSH [5:6]

ADC sample and hold time : (base on SHCLK)

00 : 1 clock

01 : 2 clock

10 : 3 clock

11 : 4 clock

ADCDS [4]

ADC data select :

	MSB	10 bit result		LSB
0 :	ADCD2[7:0]		ADCD1.1	ADCD1.0
1 :	ADCD1.1	ADCD1.0	ADCD2[7:0]	

ADCCKS [3]

ADC conversion clock select : (ADCCLK)

0 : 24MHz

1 : 12MHz

ADCCH [2:0]

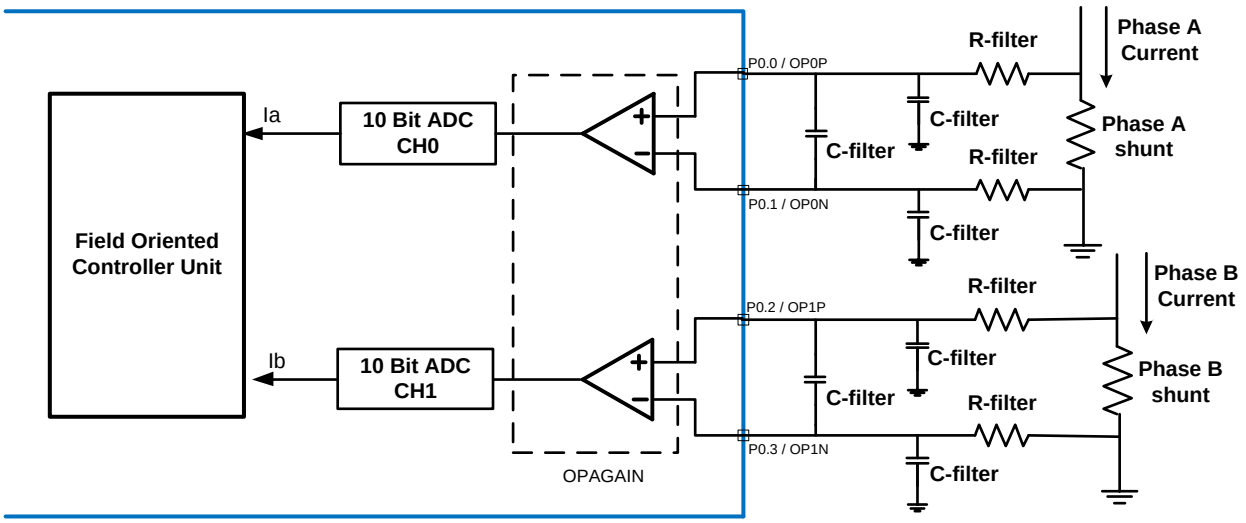
ADC conversion channel select :

000 :CH0	100 :CH4
001 :CH1	101 :CH5
010 :CH2	110 :CH6
011 : CH3	111 : CH7

13.2 ADCSTR (ADC Start Convert and Setting Register)

ADCSTR			Address = C1H			Reset Value = 0x00H	
ADC Start Convert and Setting Register							
Bit	SHCKS[1:0]		OPAGAIN		BUSY	-----	START
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R	X	X	W

SHCKS	ADC sample and hold clock select : (SHCLK)	
[6:7]	00 : 6MHz	10 : 2.4MHz
	01 : 3MHz	11 : 2MHz
OPAGAIN	OPAmp Gain	
[5:4]	00 : 1	10 : 5
	01 : 2.5	11 : 10
BUSY	ADC conversion busy flag :	
[3]	0 : ADC conversion finish	
	1 : ADC conversion busy	
START	ADC start conversion register : (write 1 only)	
[0]	1 : ADC start conversion	



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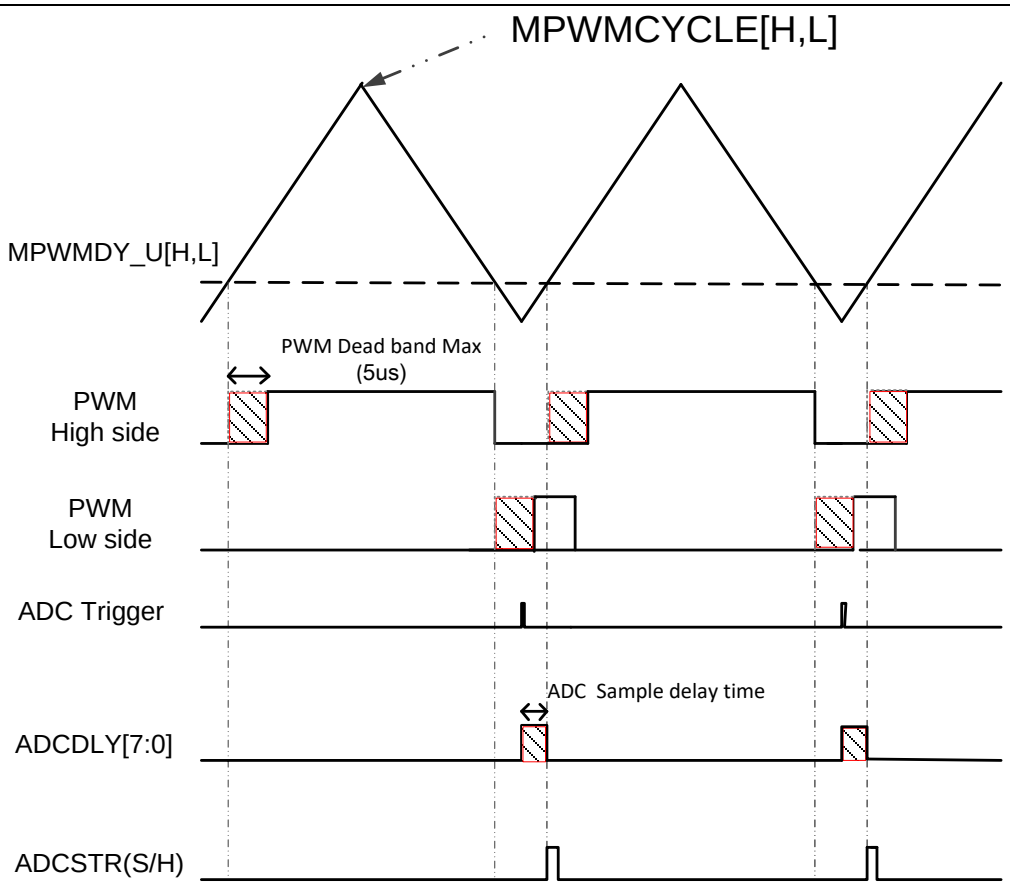
13.3 ADCDLY (ADC Sample Delay Register)

ADCDLY ADC Sample Delay		Address = C5H				Reset Value =0x33H		
Bit	ADCDLY[7:0]							
	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W



$$\text{ADC Sample delay time} = \frac{\text{ADCDLY}}{\text{PWM Frequency}}$$

13.4 ADC Data Register

ADCD1 Address = C3H Reset Value = 0x00H

ADC Data Register1

Bit	ADCD1 [1:0]							
	---	---	---	---	---	---	1	0
Type	R	R	R	R	R	R	R	R

ADCD2 Address = C4H Reset Value = 0x00H

ADC Data Register 2

Bit	ADCD2 [7:0]							
	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

13.5 ADC1Offset Value Register

ADC1OS_L Address = C9H Reset Value =0x00H

ADC1Offset Value Register Low Byte

Bit	ADC1OS_L[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ADC1OS_H Address = CAH Reset Value = 0x02H

ADC1Offset Value Register High Byte

Bit	ADC1OS_H [15:8]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.6ADC2Offset Value Register

ADC2OS_L Address = CBH Reset Value = 0x00H

ADC2Offset Value Register Low Byte

Bit	ADC2OS_L[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ADC2OS_H Address = CCH Reset Value = 0x02H

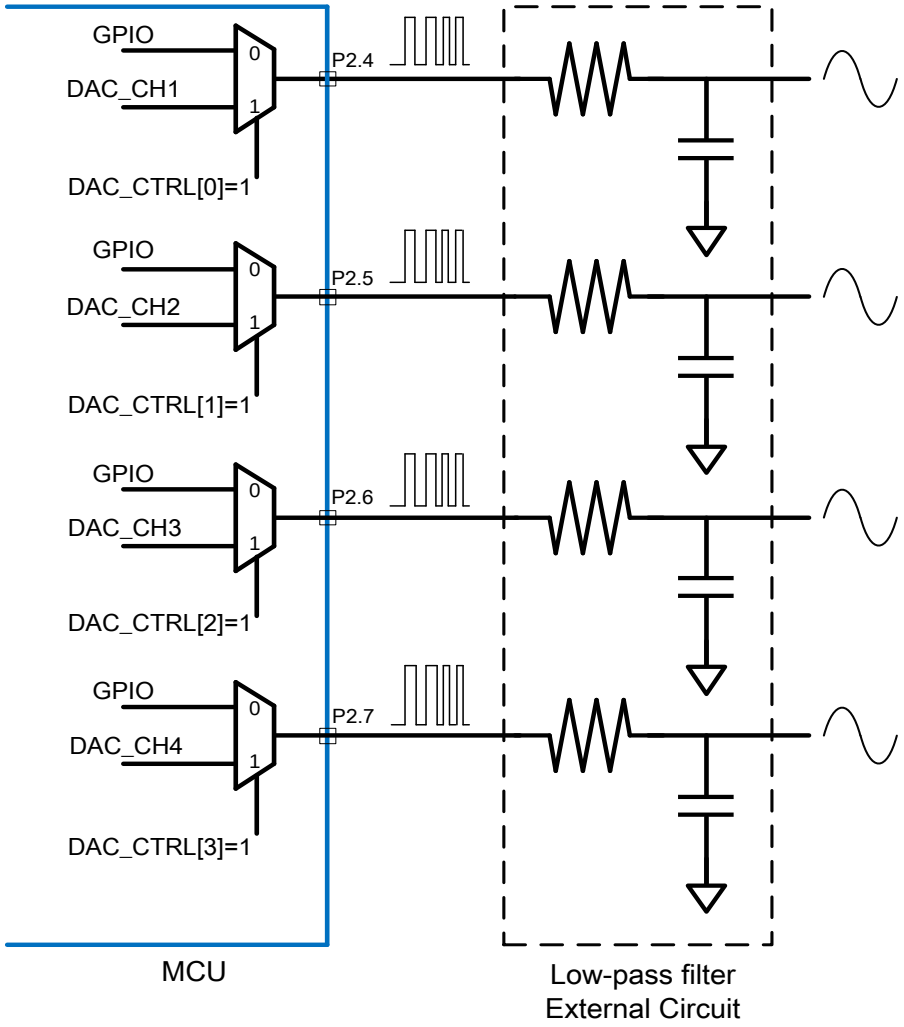
ADC2 Offset Value Register High Byte

Bit	ADC2OS_H [15:8]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

14. Digital to Analog Converter (DAC)

The MDRFD0 provides four channels 10-bit DAC. The result of the conversion is provided at DAC_CHX [3:0]. DAC_CHX Output is 180KHz PWM, External low pass filter of R:300Ohm C:0.1uF.

SFR	Description	address	Reset value
DAC_CTRL	DAC Control Register	E7H	00H
DAC Data Register			
DAC_CH1	DAC Data Register 1	E8H	00H
DAC_CH2	DAC Data Register 2	E9H	00H
DAC_CH3	DAC Data Register 3	EAH	00H
DAC_CH4	DAC Data Register 4	EBH	00H



14.1DAC_CTRL (DAC Control Register)

DAC_CTRL Address = E7H Reset Value = 0x00H

DAC Control Register

	----	----	----	----	DAC4 EN	DAC3 EN	DAC2 EN	DAC1 EN
Bit	7	6	5	4	3	2	1	0
Type	----	----	----	----	R/W	R/W	R/W	R/W

DAC1EN [3]	DAC Chanel1enable(P2.4): 0 : Disable (I/O Mode) 1: Enable .
DAC2EN [2]	DAC Chanel 2enable(P2.5): 0 : Disable (I/O Mode) 1 : Enable .
DAC3EN [1]	DAC Chanel 3enable(P2.6): 0 : Disable (I/O Mode). 1 : Enable.
DAC4EN [0]	DAC Chanel 4enable(P2.7): 0 : Disable (I/O Mode). 1 : Enable .

14.2 DAC Output Chanel(DAC_CH1–DAC_CH4)

DAC_CH1 Address = E8H Reset Value = 0x00H

DAC Data Register 1

Bit	DAC_CHA [7:0]							
	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

DAC_CH2 Address = E9H Reset Value = 0x00H

DAC Data Register 2

Bit	DAC_CHB [7:0]							
	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

DAC_CH3 Address = EAH Reset Value = 0x00H

DAC Data Register 3

Bit	DAC_CHC[7:0]							
	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

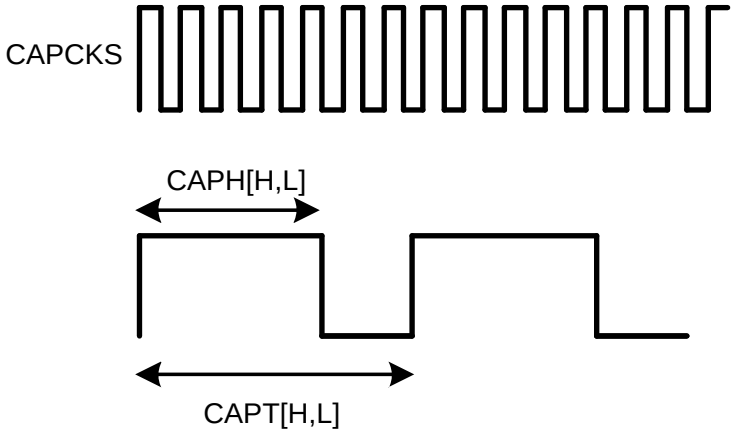
DAC_CH4 Address = EBH Reset Value = 0x00H

DAC Data Register 4

Bit	DAC_CHD [7:0]							
	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

15. Capture

SFR	Description	address	Reset value
CAPCONT	Capture Control Register	DDH	03H
Capture Total Count:			
CAPT_L	Capture Total Count Low	D9H	00H
CAPT_H	Capture Total Count High	DAH	00H
Capture Count:			
CAPH_L	Capture High-level Count Low	DBH	00H
CAPH_H	Capture High-level Count High	DCH	00H



15.1 CAPCONT (Capture Control Register)

CAPCONT Address = DDH Reset Value = 0x03H

Capture Control Register

Bit	-----	-----	-----	CAPPINSEL	-----	CAPCKS[2:0]		
	7	6	5	4	3	2	1	0
Type	X	X	X	R/W	X	R/W	R/W	R/W

CAPPINSEL	Capture input pin select :	
[4]	0 : CAP2(P0.7)	
	1: CAP1(P0.6)	
CAPCKS	Capture clock select :	
[2:0]	000 : 48MHz/4	100 : 48MHz/64
	001 : 48MHz/8	101 : 48MHz/128
	010 : 48MHz/16	110 : 48MHz/256
	011 : 48MHz/32	111 : 48MHz/512

15.2 Capture Total Count

CAPT_L — Address = D9H — Reset Value = 0x00H

Capture Total Count Low

Bit	CAPT[7:0]							
	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

CAPT_H — Address = DAH — Reset Value = 0x00H

Capture Total Count High

Bit	CAPT[15:8]							
	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

15.3Capture Count

CAPH_L — Address = DBH — Reset Value = 0x00H

Capture High-level Count Low

Bit	CAPH[7:0]							
	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

CAPH_H — Address = DCH — Reset Value = 0x00H

Capture High-level Count High

Bit	CAPH[15:8]							
	7	6	5	4	3	2	1	0
Type	R	R	R	R	R	R	R	R

16. Multiplication and Division Unit (MDU)

The MDU is an on-chip arithmetic co-processor which enables the MDRFD0 to perform additional extended arithmetic operations. All operations are singed/unsigned integer operations. Operands and results are stored in MD0–MD5 registers. The module is controlled by the MD_MODE and MD_CONT register. Any calculation of the MDU overwrites its operands. The MDU support five operations: Division 32-bit/16-bit, Division 16-bit/16-bit, Multiplication, Shift and Normalize.

SFR	Description	address	Reset value
MD_CONT	MDU Control Register	ADH	00H
MD_MODE	MDU Mode Control Register	ACH	10H
MD0	Multiplication Division Register 0	AEH	00H
MD1	Multiplication Division Register 1	AFH	00H
MD2	Multiplication Division Register 2	B1H	00H
MD3	Multiplication Division Register 3	B2H	00H
MD4	Multiplication Division Register 4	B3H	00H
MD5	Multiplication Division Register 5	BAH	00H

16.1 MD_MODE (MDU Control Mode)

MD_MODE Address = ACH Reset Value = 0x10H

MDU Mode Control Register

Bit	-----	-----	-----	MDUF	-----	-----	MDUS	----
	7	6	5	4	3	2	1	0
Type	X	X	X	R	X	X	R/W	X

MDUF [4]	MDU finish flag : 0 : MDU busy. 1 : MDU calculation finished.
MDUS [1]	MDU Signed select : 0 :Signed calculation. 1 :Unsigned calculation.

16.2 MD_CONT (MDU Control Register)

MD_CONT Address = ADH Reset Value = 0x10H

MDU Control Register

Bit	MDEF	MDOV	SLR	SC[4:0]				
	7	6	5	4	3	2	1	0
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W

MDEF	MDU Error flag :
[7]	Indicates an improperly performed operation (when one of the arithmetic operations has been restarted or interrupted by a new operation).
MDOV	MDU Overflow flag :
[6]	Overflow occurrence in the MDU operation.
SLR	Shift direction :
[5]	0 : shift left operation 1 : shift right operation
SC	Shift counter :
[4:0]	When set to all '0's, normalize operation is selected. After normalization, the SC[4:0] contain the number of normalizing shifts performed. When at least one of these bit is set high shift operation is selected. The number of shifts performed is determined by the number written to SC[4:0], where SC.4 is the MSB.

16.2.1 MDEF

The MDEF error flag indicates an improperly performed operation (when one of the arithmetic operations has been restarted or interrupted by a new operation). The error flag mechanism is automatically enabled with the first write operation to MD0and disabled with the final read instruction from MD3(multiplication or shift/norm) or MD5 (division) in phase three.

The error flag is set when:

There is a write access to MDx registers (any of MD0-MD5 and MD_CONT) during phase two of MDU operation (restart or calculations interrupting) There is a read access to one of MDx registers during phase two of MDU operation when the error flag mechanism is enabled. In such condition error flag is set but the calculation is not interrupted. The error flag is reset only after read access to MD_CONT register. The error flag is read only.

16.2.2 MDOV

The MDOV overflow flag is set when one of the following conditions occurs: Division by zero
Multiplication with a result greater than FFFFH
Start of normalizing if the ('MD3.7' ='1') most significant bit of MD3 is set
Any operation of the MDU that does not match the above conditions clears the overflow flag. Note that the overflow flag is exclusively controlled by hardware. It cannot be written.

16.3 MD0 – MD5 (Multiplication Division Register)

MD0 Address = AEH Reset Value = 0x00H
Multiplication Division Register 0

Bit	MD0[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD1 Address = AFH Reset Value = 0x00H
Multiplication Division Register 1

Bit	MD1[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD2 Address = B1H Reset Value = 0x00H
Multiplication Division Register 2

Bit	MD2[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD3 Address = B2H Reset Value = 0x00H
Multiplication Division Register 3

Bit	MD3[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD4 Address = B3H Reset Value = 0x00H
Multiplication Division Register 4

Bit	MD4[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD5 Address = BAH Reset Value = 0x00H
Multiplication Division Register 5

Bit	MD5[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.4 MDU Operation Description

The operation of the MDU consists of three phases:

16.4.1 Loading the MDx registers

The type of calculation the MDU has to perform is selected by the order in which the MDx registers are written to. A write to MD0 is the first transfer to be done in any case. Next writes must be done as shown in the table below to determine the MDU operation. The last write will start the selected operation.

Operation	32-bit/16-bit	16-bit/-16bit	16-bit x 16-bit	Shift/ normalizing
First write	MD0 Dividend Low	MD0 Dividend Low	MD0 Multiplicand Low	MD0 LSB
	MD1 Dividend	MD1 Dividend High	MD4 Multiplicator Low	MD1
	MD2 Dividend		MD1 Multiplicand High	MD2
	MD3 Dividend High			MD3 MSB
	MD4 Divisor Low	MD4 Divisor Low		
Last write	MD5 Divisor High	MD5 Divisor High	MD5 MultiplicatorHigh	MD_CONT start conversion

16.4.2 Executing calculation

During the calculation period, the MDU works in parallel to the CPU. When the calculation is complete, the hardware will set the MDUF bit to one (MDUF = '1'). The flag will be cleared at the next calculation.

The following table provides the execution time for each mathematical operation.

Operation	Number of clock cycles	
Division 32-bit/16-bit	17 clock cycles	
Division 16-bit/16-bit	9 clock cycles	
Multiplication	11 clock cycles	
Shift	Min 3 clock cycles (SC = 01H)	Max 18 clock cycles (SC = 1FH)
Normalize	Min 4 clock cycles (SC <= 01H)	Max 19 clock cycles (SC = 1FH)

16.4.3 Reading the result from the MDx registers

The Read-out sequence of the first "MDx" registers is not critical but the last read determines the end of a whole calculation.

Operation	32-bit/16-bit	16-bit/16-bit	16-bit x 16-bit	Shift/ normalizing
First read	MD0 Quotient Low	MD0 Quotient Low	MD0 Product Low	MD0 LSB
	MD1 Quotient	MD1 Quotient High	MD1 Product	MD1
	MD2 Quotient		MD2 Product	MD2
	MD3 Quotient High			
	MD4 Remainder Low	MD4 Remainder Low		
Last read	MD5 Remainder High	MD5 Remainder High	MD3 Product High	MD3 MSB

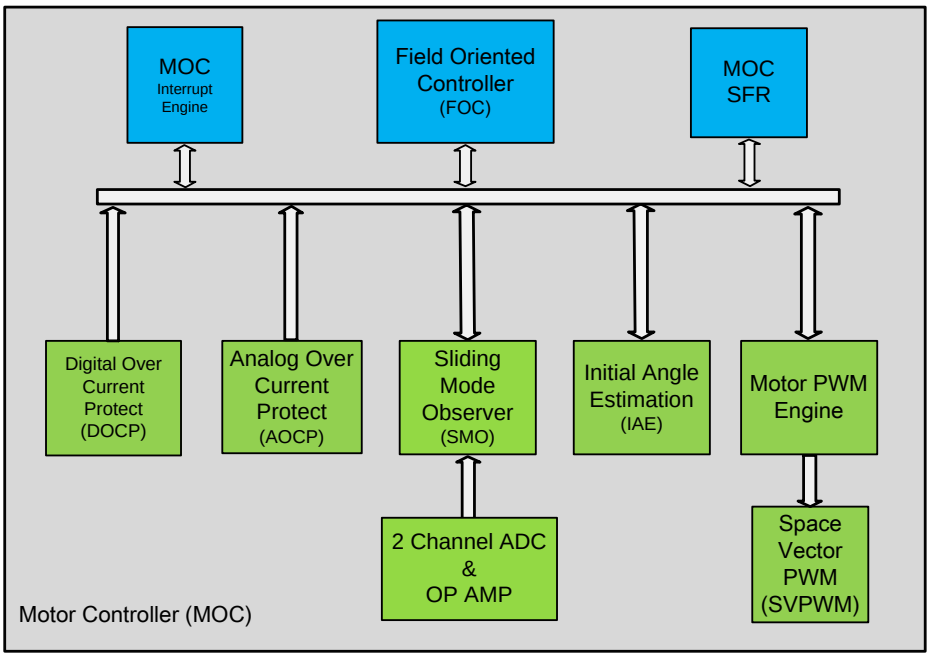
16.4.4 Shifting

In shift operation, 32-bit integer variable stored in MD0 to MD3 registers (the latter contains the most significant byte) is shifted left or right by a specified number of bits. The SLR bit (MD_CONT.5) defines the shift direction, and bits SC[4:0] (MD_CONT.4 –MD_CONT.0) specifies the shift count (which must not be 0). During shift operation, zeroes come into the left end of MD3 for shifting right or right end of the MD0 for shifting left.

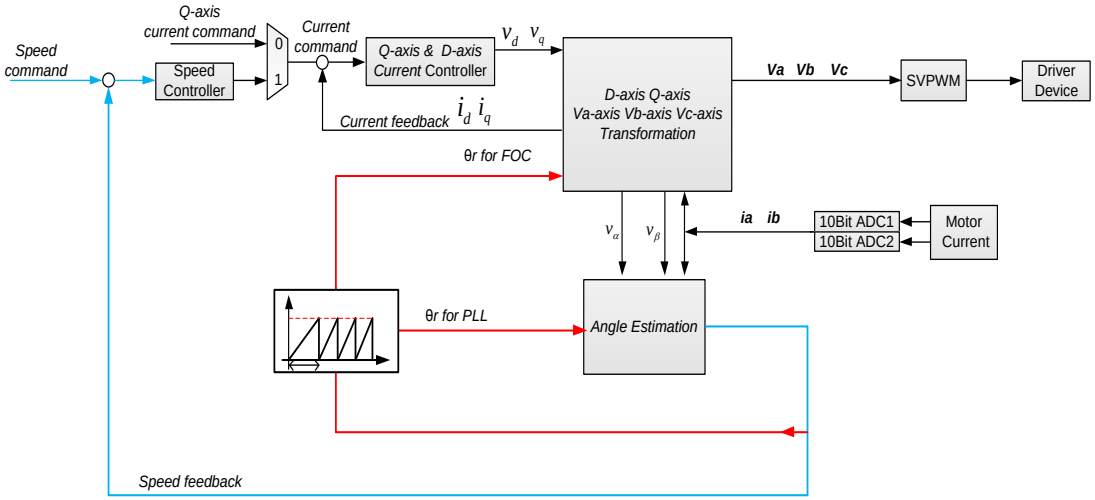
16.4.5 Normalizing

All leading zeroes of 32-bit integer variable stored in MD0 to MD3 registers, the latter contains the most significant byte are removed by shift left operations. The whole operation is completed when the MSB (most significant bit) of MD3 register contains a ‘1‘. After normalizing, bits SC[4:0] (MD_CONT.4 –MD_CONT.0) contain the number of shift left operations, which were done.

17. Motor Controller (MOC)



Motor Controller Unit Architecture



Field Oriented Controller Unit Architecture

17.1 MOC Engine

SFR	Type	Description	address	Reset value
MOTOR_CONT1	R/W	Motor Control Register 1.	97H	00H
MOTOR_CONT2	R/W	Motor Control Register 2.	9FH	00H
FOCCONT	R/W	FOC Control Register.	D6H	00H
SP_CYC	W	SPEED Loop Control Cycle.	EDH	26H
AS	W	Angle Supplement Data Register.	C6H	00H
PI-GAIN	W	PI-Control Gain Register.	E6H	F7H
CPU Angle Data Register:				
CPU_ANG_L	R/W	CPU Angle Data Low byte.	DEH	00H
CPU_ANG_H	R/W	CPU Angle Data High byte.	DFH	00H
PI-Control Data Register:				
PI_KI_L	R/W	PI-Control KI Data Low byte.	91H	00H
PI_KI_H	R/W	PI-Control KI Data High byte.	92H	00H
PI_KP_L	R/W	PI-Control KP Data Low byte.	93H	00H
PI_KP_H	R/W	PI-Control KP Data High byte.	94H	00H
PI_LMT_L	R/W	PI-Control Limit Data Low byte.	95H	00H
PI_LMT_H	R/W	PI-Control Limit Data High byte.	96H	00H
PI_CMD_L	R/W	PI- Control Command Data Low byte.	A6H	00H
PI_CMD_H	R/W	PI- Control Command Data High byte.	A7H	00H
PI-UI_L	R/W	PI- Control Integral Data Low byte.	9DH	00H
PI-UI_H	R/W	PI- Control Integral Data High byte.	9EH	00H
SMO Control Data Register:				
SMO_D1_L	R/W	SMO Data1 Low byte.	BBH	00H
SMO_D1_H	R/W	SMO Data1 High byte.	BCH	00H
SMO_D2_L	R/W	SMO Data2 Low byte.	BDH	00H
SMO_D2_H	R/W	SMO Data2 High byte.	BEH	00H
FOC Control Data Register:				
FOC_D1_L	R/W	FOC Data1 Low byte.	D2H	00H
FOC_D1_H	R/W	FOC Data1 High byte.	D3H	00H
FOC_D2_L	R/W	FOC Data2 Low byte.	D4H	00H
FOC_D2_H	R/W	FOC Data2 High byte.	D5H	00H
VDQ_OFST_L	R/W	D&Q Axis Voltage Off set Low byte.	A1H	00H
VDQ_OFST_H	R/W	D&Q Axis Voltage Off set High byte.	A2H	00H

17.1.1 MOTOR_CONT1 (Motor Control Register)

MOTOR_CONT1 Address = BFH Reset Value = 0x00H

Motor Control Register 1

Bit	SD MODE	MPWMD USEL	MPWM EN	IQINSEL	FOC ANGSEL	SHIFTED [2:0]		
	7	6	5	4	3	2	1	0
Type	x	R/W	R/W	R/W	R/W	x	x	x

MPWMDUSEL [6]	MPWM duty select : 0 : From register 1 : From SVPWM register
MPWMEN [5]	MPWM timer run control enable: 0 : Disable 1 : Enable MPWMEN =1, ADC CH1 & CH2 Auto Converter:
IQINSEL [4]	IQ-Control input select: 0 : From register 1 : From speed PI- control output
FOCANGSEL [3]	FOC input angle select: 0 : From CPU_ANG (Write value of CPU_ANG_H & CPU_ANG_L) 1 : From SMO_ANG (Estimated angle) Inverse park trans formation input select of angle

17.1.2 MOTOR_CONT2 (Motor Control Register2)

MOTOR_CONT2 Address = 9FH Reset Value = 0x00H

Motor Control Register 2

	----	----	----	SVPWM MODE	SVPWM PS	----	IAE SOFEN	----
Bit	7	6	5	4	3	2	1	0
Type	X	X	X	R/W	R/W	X	R/W	X

SVPWMMODE	SVPWM mode select:
[4]	0 : Continuous SVPWM mode.
	1 : Discontinuous SVPWM mode.
SVPWMPS	SVPWM output phase sequence:
[3]	0 : Positive sequence (A、B、C)
	1 : Negative sequence (B、A、C)
IAESOFEN	Initial Angle estimation soft start enable:
[1]	0 : Disable
	1 : Enable

17.1.3 Field Oriented Control Register

FOCCONT Address = D6H Reset Value = 0x00H

Field Oriented Control Register

Bit	PI CLEAR	ESTCR			INV ADCD	ADC TRIG	PLL EN	SPEED EN
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PICLEAR	Clear register value of PI-Control:	
[7]	0: Disable	
	1: Enable	
ESTCR	Estimation current ration:	
[6:4]	000 : Current ValueX1	100 : Current Value/2
	001 : Current ValueX2	101 : Current Value/4
	010 : Current ValueX4	110 : Current Value/8
	011 : Current ValueX8	111 : Current Value/16
INVADCD	Inverse ADC register data:	
[3]	0: Disable	
	1: Enable	
ADCTRIG	ADC Trigger (Phase A and Phase B):	
[2]	0 : PWM counter max	
	1 : PWM counter min	
PLLEN	PLL-Control enable:	
[1]	0: Disable	
	1: Enable	
SPEEDEN	SPEED-Control enable:	
[0]	0: Disable	
	1: Enable	

17.1.4 PI_GAIN (PI- Controller GAIN)

PI_GAIN Address = E6H Reset Value = 0xF7H

PI-Control x16Gain

	IQKPGEN	IQKIGEN	IDKPGEN	IDKIGEN	SPKPGEN	SPKIGEN	PLLKPEN	PLLKIGEN
Bit	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

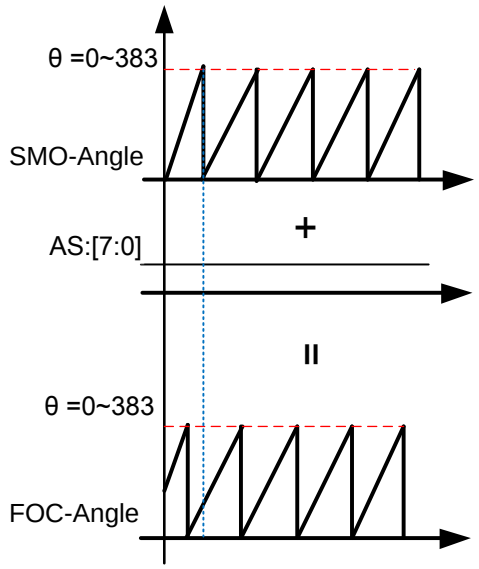
IQKPGEN [7]	IQ-KP-Gain enable: 0: Disable 1: Enable
IQKIGEN [6]	IQ-KI- Gain enable: 0: Disable 1: Enable
IDKPGEN [5]	ID-KP- Gain enable: 0: Disable 1: Enable
IDKIGEN [4]	ID-KI- Gain enable: 0: Disable 1: Enable
SPKPGEN [3]	SPEED-KP- Gain enable: 0: Disable 1: Enable
SPKIGEN [2]	SPEED-KI- Gain enable: 0: Disable 1: Enable
PLLKPGEN [1]	PLL-KP- Gain enable: 0: Disable 1: Enable
PLLKIGEN [0]	PLL-KI- Gain enable: 0: Disable 1: Enable

17.1.5 AS (Angle Supplement Data Register)

AS	Address = C6H	Reset Value =0x00H

Angle Supplement Data Register

Bit	AS[7:0]							
	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W



Angle Supplement

17.1.6 SP_CYC (SPEED Loop control cycle)

SP_CYC	Address = EDH	Reset Value = 0x26H

SPEED Loop control cycle

Bit	SP-CYC[7:0]							
	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

$$SP\text{-}CYC = \frac{\text{PWM Frequency}}{\text{SPEED Loop Frequency}}$$

17.1.7 CPU_ANG (CPU Angle Data Register)

CPU_ANG_L(SYNC) Address = DEH Reset Value = 0x00H
CPU_ Angle Register Low Byte

Bit	CPU_ANG_L[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CPU_ANG_H(SYNC) Address = DFH Reset Value = 0x00H
CPU_Angle Register High Byte

Bit	CPU_ANG_H[7:0]							
	7	6	5	4	3	2	1	0
Type	X	X	X	X	X	X	X	R/W

17.1.8 PI-Control Data Register

SFR	Description		
PI_KP_L	PI-Control KP Data Low byte		
PI_KP_H	PI-Control KP Data High byte		
	Parameters	Description	Reset Value
SFR_PAGE = 0	IQ	Parameters KP for IQ - Control	0x0000H
SFR_PAGE = 1	ID	Parameters KP for ID - Control	0x0000H
SFR_PAGE = 2	SPEED	Parameters KP for SPEED - Control	0x0000H
SFR_PAGE = 3	PLL	Parameters KP for PLL - Control	0x36B0H

PI_KP_L	Address = 93H	Reset Value = 0x00H

PI-Control KP Data Low byte

Bit	PI_KP_L [7:0]							
Type	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI_KP_H	Address = 94H	Reset Value = 0x00H

PI-Control KP Data High byte

Bit	PI_KP_H [15:8]							
Type	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SFR	Description		
PI_KI_L	PI-Control KI Data Low byte		
PI_KI_H	PI-Control KI Data High byte		
SFR_PAGE	Parameters	Description	Reset Value
SFR_PAGE = 0	IQ	Parameters KI for IQ - Control	0x0000H
SFR_PAGE = 1	ID	Parameters KI for ID - Control	0x0000H
SFR_PAGE = 2	SPEED	Parameters KI for SPEED - Control	0x0000H
SFR_PAGE = 3	PLL	Parameters KI for PLL - Control	0x09C4H

PI_KI_L	Address = 91H	Reset Value = 0x00H

PI-Control KI Data Low byte

Bit	PI_KP_L [7:0]							
Type	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI_KI_H	Address = 92H	Reset Value = 0x00H

PI-Control KI Data High byte

Bit	PI_KP_H [15:8]							
Type	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SFR	Description		
PI_LMT_L	PI-Control Limit Data Low byte		
PI_LMT_H	PI-Control Limit Data High byte		
	Parameters	Description	Reset Value
SFR_PAGE = 0	IQ	Limit value of IQ - Control	0x7FFFH
SFR_PAGE = 1	ID	Limit value of ID - Control	0x7FFFH
SFR_PAGE = 2	SPEED	Limit value of SPEED - Control	0x7FFFH
SFR_PAGE = 3	PLL	Limit value of PLL - Control	0x7FFFH

PI_LMT_L	Address = 95H	Reset Value = 0x00H

PI-Control Limit Data Low byte

Bit	PI_LMT_L [7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI_LMT_H	Address = 96H	Reset Value = 0x00H

PI-Control Limit Data High byte

Bit	PI_LMT_H [15:8]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SFR	Description		
PI_CMD_L	PI-Control Command Data Low byte		
PI_CMD_H	PI-Control Command Data High byte		
	Parameters	Description	Reset Value
SFR_PAGE = 0	IQ	Command value of IQ - Control	0x0000H
SFR_PAGE = 1	ID	Command value of ID - Control	0x0000H
SFR_PAGE = 2	SPEED	Command value of SPEED - Control	0x0000H
SFR_PAGE = 3	PLL	Command value of PLL - Control	0x0000H

PI_CMD_L	Address = A6H	Reset Value = 0x00H

PI-Control Command Data Low byte

Bit	PI_CMD_L [7:0]							
Type	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI_CMD_H	Address = A7H	Reset Value = 0x00

PI-Control Command Data High byte

Bit	PI_CMD_H [15:8]							
Type	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SFR	Description		
PI-UI_L	PI-Control Integral Data Low byte		
PI-UI_H	PI-Control Integral Data High byte		
	Parameters	Description	Reset Value
SFR_PAGE = 2	SPEED_UI	Integral value of SPEED - Control	0x0000H
SFR_PAGE = 3	PLL_UI	Integral value of PLL - Control	0x0000H

PI-UI_L	Address = 9DH	Reset Value = 0x00H					
PI-Control Integral Data Low byte							
Bit Type	PI-UI_H [7:0]						
	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PI-UI_H	Address = 9EH	Reset Value = 0x00H					
PI-Control Integral Data High byte							
Bit Type	PI-UI_L [15:8]						
	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.1.9 Sliding Mode Observer Data Register

SFR	Description		
SMO_D1_L	Sliding Mode Observer Data1 Low byte		
SMO_D1_H	Sliding Mode Observer Data1 High byte		
	Parameters	Description	Reset Value
SFR_PAGE = 0	GS	Parameters GS for angle estimation	0x7FFFH
SFR_PAGE = 1	SMO_Gain	Parameters Slide mode Gain for angle estimation	0x3E80H
SFR_PAGE = 2	Angle_Base	Parameters Angle Base for angle estimation	0x0B2FH
SFR_PAGE = 3	EST-Z_ Alpha	Estimated Value of Alpha-axis Z (Z = Feedback Alpha-axis current - estimated Alpha-axis current)	0x0000H
SFR_PAGE = 4	EST-I_ Alpha	Estimated value of Alpha-axis Current.	0x0000H
SFR_PAGE = 5	EST-E_ Alpha	Estimated value of Alpha-axis back EMF.	0x0000H
SFR_PAGE = 6	SMO-Angle	Estimated value of SMO angle Read Only	0x0000H

SMO_D1_L	Address = BBH	Reset Value = 0x00H

SMO Data1Low Byte

Bit Type	SMO_D1_L [7:0]							
	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SMO_D1_L	Address = BCH	Reset Value = 0x00H

SMO Data1 High Byte

Bit Type	SMO_D1_H [15:8]							
	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SFR	Description		
SMO_D2_L	Sliding Mode Observer Data2Low byte		
SMO_D2_H	Sliding Mode Observer Data2High byte		
	Parameters	Description	Reset Value
SFR_PAGE = 0	FS	Parameters FS for angle estimation.	0x7FFFH
SFR_PAGE = 1	SMO_Filter	Parameters SMO_Filter for angle estimation	0x0064H
SFR_PAGE = 2	Angle_Shift	Parameters Angle_Shift for angle estimation	0x0000H
SFR_PAGE = 3	EST-Z_ Beta	Estimated value of Alpha-axis Z (Z = feedback Beta-axis current -estimated Beta-axis current)	
SFR_PAGE = 4	EST-I_ Beta	Estimated value of Beta -axis Current.	
SFR_PAGE = 5	EST-E_ Beta	Estimated value of Beta -axis back EMF.	
SFR_PAGE = 6	PLL-PI-OUT	Output value of PLL-PI-Control.	

SMO_D2_L	Address = BDH	Reset Value = 0x00H

SMO Data2Low Byte

Bit Type	SMO_D2_L [7:0]							
	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SMO_D2_H	Address = BEH	Reset Value = 0x00H

SMO Data2High Byte

Bit Type	SMO_D2_H [15:8]							
	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.1.10 Field Oriented Controller Data Register

SFR	Description		
FOC_D1_L	Field Oriented Control Data1 Low byte		
FOC_D1_H	Field Oriented Control Data1 High byte		
	Parameters	Description	Reset Value
SFR_PAGE = 0	IQ_FB	IQ-Control feedback data	0x0000H
SFR_PAGE = 1	ID_FB	ID- Control feedback data	0x0000H
SFR_PAGE = 2	Ia	ADC Output of phase A current	0x0000H
SFR_PAGE = 3	Va	Inverse Clarke transformation output of Phase A voltage	0x0000H
SFR_PAGE = 4	I_Alpha	Clarke transformation output of Alpha-axis current	0x0000H
SFR_PAGE = 5	V_Alpha	Inverse Park transformation output of Alpha-axis voltage	0x0000H
SFR_PAGE = 6	FOC_Angle	Park and Inverse Park transformation angle input Read: Estimated angle. Write: Theta offset.	0x0000H

FOC_D1_L	Address = D2H	Reset Value = 0x00H

FOCData1Low Byte

Bit Type	FOC_D1_L [7:0]							
	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FOC_D1_H	Address = D3H	Reset Value = 0x00H

FOCData1High Byte

Bit Type	FOC_D1_H [15:8]							
	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SFR	Description		
FOC_D2_L	Field Oriented Control Data2 Low byte		
FOC_D2_H	Field Oriented Control Data2 High byte		
	Parameters	Description	Reset Value
SFR_PAGE = 0	IQ_PI_OUT	IQ- Control output data (Vq)	0x0000H
SFR_PAGE = 1	ID_PI_OUT	ID- Control output data (Vd)	0x0000H
SFR_PAGE = 2	Ib	ADC Output of phase B current	0x0000H
SFR_PAGE = 3	Vb	Inverse Clarke transformation output of Phase B voltage	0x0000H
SFR_PAGE = 4	I_Beta	Clarke transformation output of Beta-axis current	0x0000H
SFR_PAGE = 5	V_Beta	Inverse Park transformation output data of voltage Beta	0x0000H
SFR_PAGE = 6	SVPWM-Amp	Amplitude gain of SVPWM transformation	0x4000H

FOC_D2_L	Address = D4H	Reset Value = 0x00H

FOC Data2 Low Byte

Bit Type	FOC_D2_L [7:0]							
	7	6	5	4	3	2	1	0
	R	R	R	R	R	R	R	R

FOC_D2_H	Address = D5H	Reset Value = 0x00H

FOC Data2 High Byte

Bit Type	FOC_D2_H [15:8]							
	7	6	5	4	3	2	1	0
	R	R	R	R	R	R	R	R

SFR	Description		
VDQ_OFST_L	D&Q -Axis Voltage Offset Low byte(SYNC)		
VDQ_OFST_H	D&Q -Axis Voltage Offset High byte(SYNC)		
	Parameters	Description	Reset Value
SFR_PAGE = 0	D-Axis Voltage	D-Axis Voltage Offset	0x0000H
SFR_PAGE = 1	Q-Axis Voltage	Q-Axis Voltage Offset	0x0000H

VDQ_OFST_L	Address = A1H	Reset Value = 0x00H

D&Q -Axis Voltage Offset Low byte

Bit Type	VDQ_OFST_L [7:0]							
	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

VDQ_OFST_H	Address = A2H	Reset Value = 0x00H

D&Q -Axis Voltage Offset High byte

Bit Type	VDQ_OFST_H [15:8]							
	7	6	5	4	3	2	1	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.2 Motor PWM Engine

MPWM is count up and down timer. (fixed)

SFR	Description	address	Reset value
MPWMCONT	MPWM Control Register .	E3H	00H
MPWMDB	Motor PWM Deadband Register.	E5H	78H
MPWMINV	MPWM Inverse Selection Register.	E4H	00H
MPWMDATAL	MPWM Data Register Low.	E1H	02H
MPWMDATAH	MPWM Data Register High.	E2H	00H

17.2.1 MPWMCONT (MPWM Control Register)

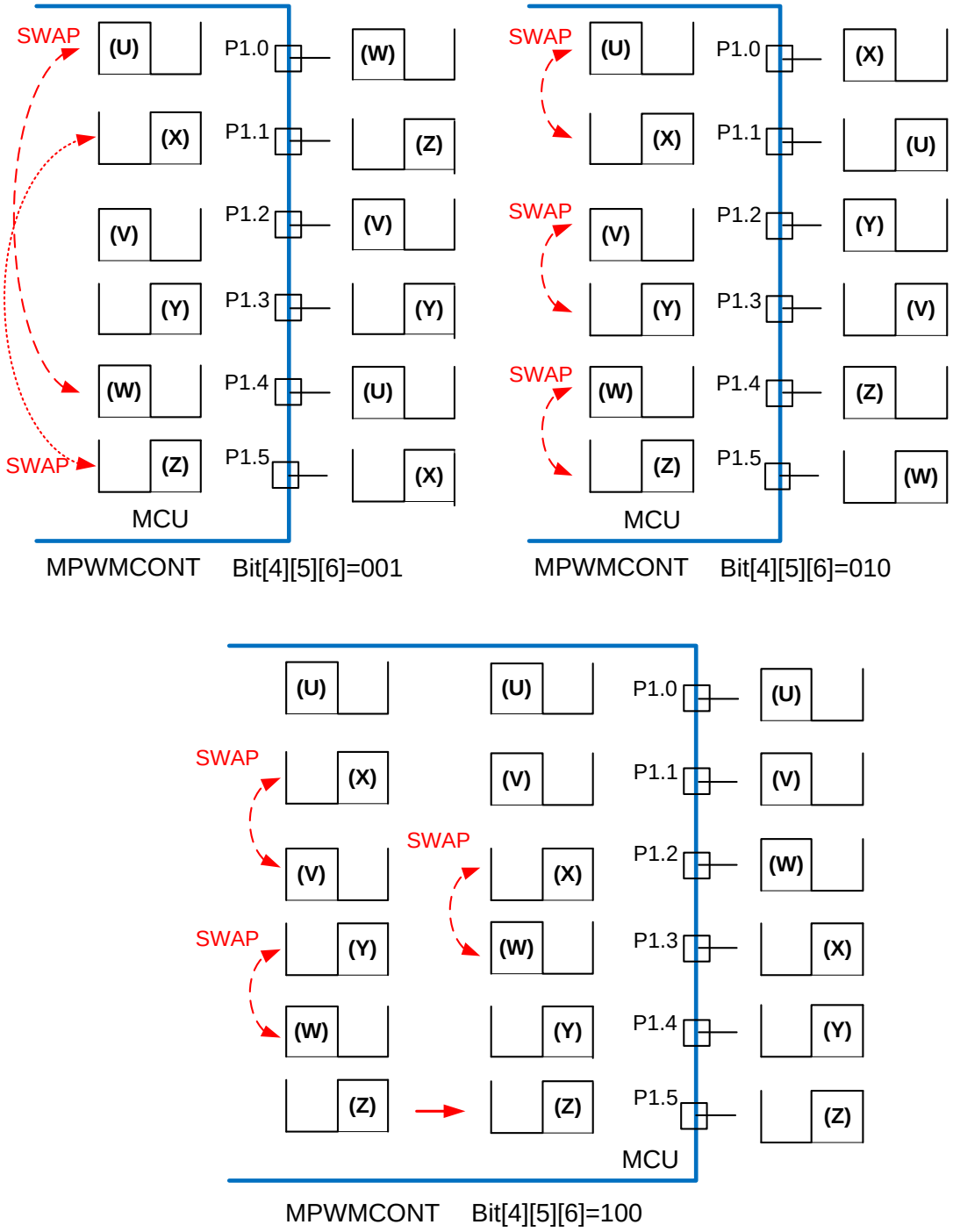
Motor PWM output mode select:

MPWMCONT(SYNC) Address = E3H Reset Value = 0x00H

MPWM Control Register

Bit	-----	HALF SWAP	ALL SWAP	UWXZ SWAP	LOWSIDE		HIGHSIDE	
	7	6	5	4	3	2	1	0
Type	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

HALFSWAP [6]	Half pin swap (X,V swap),(Y,W swap) and (X,W swap) 0: Normal 1: Half change
ALLSWAP [5]	High side and Low side pin swap(U->X , X->U、V->Y,Y->V、W->X,X->W) 0: Normal 1: Inverse
UWXZSWAP [4]	U、W pin swap and X、Z pin swap 0: Normal 1: Swap
LOWSIDE [2:3]	Low-side (X、Y、Z) 00: Force Low 10: Active High 01: Force High 11: Active Low
HIGHSIDE [1:0]	High-side (U、V、W) 00: Force Low 10: Active High 01: Force High 11: Active Low



PWM Pin swap Unit Architecture

17.2.2 MPWMDB (Motor PWM Dead band Register)

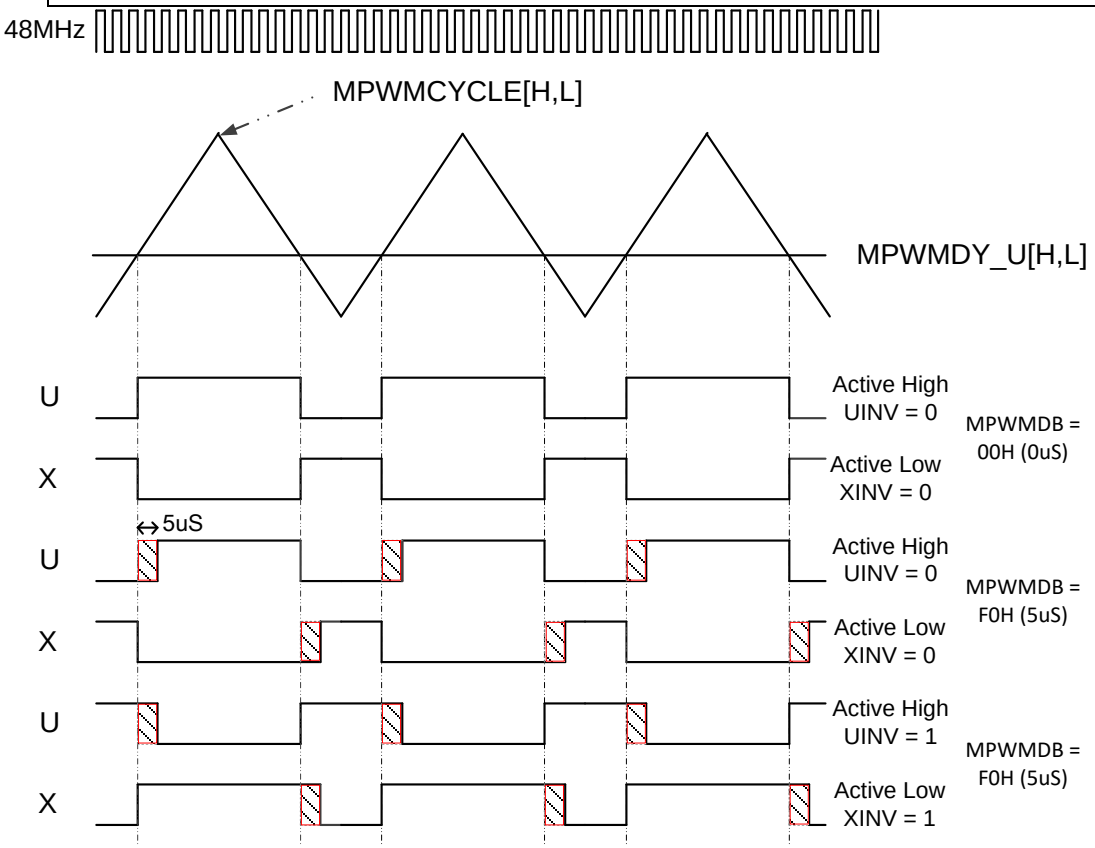
Compensation PWM output with Dead-band is use to prevent short-though between high-side and low-side power device.

The frequency of MPWMDB is 48MHz. (fixed)

MPWMDB (SYNC) Address = E5H Reset Value = 0x78H

Motor PWM Dead-band Register

Bit	MPWMDB[7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W



PWM Output with Dead band

17.2.3 MPWMINV (MPWM Inverse Selection Register)

Motor U,V,W X,Y,Z PWM output Inverse select :

MPWMINV (SYNC) Address = E4H Reset Value = 0x00H

MPWM Inverse Selection Register

Bit	-----	-----	ZINV	WINV	YINV	VINV	XINV	UINV
	7	6	5	4	3	2	1	0
Type	X	X	R/W	R/W	R/W	R/W	R/W	R/W

ZINV [5]	Low-side PWM Z output inverse select : 0 : Non-inverse 1 : Inverse
WINV [4]	High-side PWM W output inverse select : 0 : Non-inverse 1 : Inverse
YINV [3]	Low-side PWM Y output inverse select : 0 : Non-inverse 1 : Inverse
VINV [2]	High-side PWM V output inverse select : 0 : Non-inverse 1 : Inverse
XINV [1]	Low-side PWM X output inverse select : 0 : Non-inverse 1 : Inverse
UINV [0]	High-side PWM U output inverse select : 0 : Non-inverse 1 : Inverse

17.2.4 MPWM DATA (Motor PWM Data Register)

MPWM Cycle :MPWM is 16-bit timer. The frequency of MPWM timer is 48MHz. (fixed)MPWM is count up and down timer. (fixed)

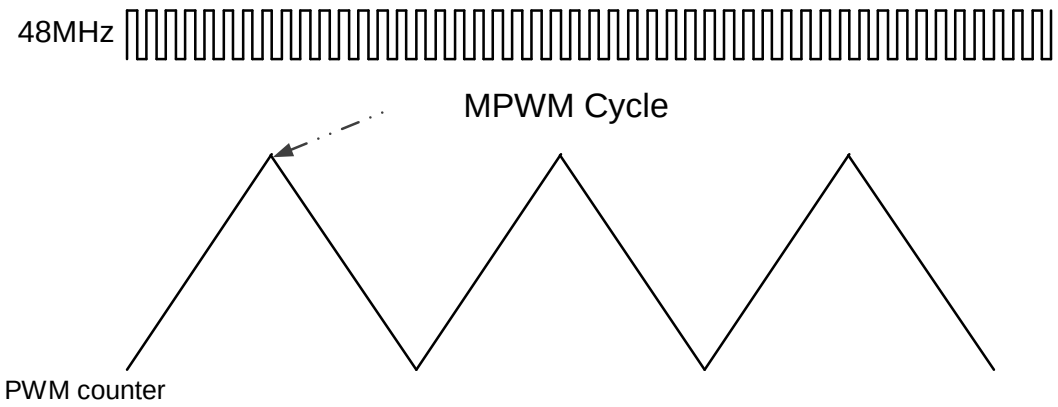
SFR	Description		
MPWMDATL	MPWM Data Low Byte(SYNC)		
MPWMDATH	MPWM Data High Byte(SYNC)		
	Parameters	Description	Reset Value
SFR_PAGE = 0	MPWM Cycle	Motor PWM cycle value	0x04B0H
SFR_PAGE = 1	Phase A	Motor PWM Duty value for Phase A	0x0258H
SFR_PAGE = 2	Phase B	Motor PWM Duty value for Phase B	0x0258H
SFR_PAGE = 3	Phase C	Motor PWM Duty value for Phase C	0x0258H

MPWMDATL	Address = E2H	Reset Value = 0x00H
Motor PWM Data Low Byte		

Bit	MPWMDATL [7:0]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MPWMDATH	Address =E1H	Reset Value = 0x00H
Motor PWM Data High Byte		

Bit	MPWMDATH [15:8]							
	7	6	5	4	3	2	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W



17.3 Over Current Protect (OCP)

SFR	Description	address	Reset value
AOCPCONT	Analog Over Current Protect Control Register	EEH	C7H
OCPNCONT	Digital Over Current Protect Control Register	EFH	85H

17.3.1 AnalogOCPControl Register(AOCPCONT)

AOCPCONT Address = EEH Reset Value = 0xC7H

Analog OCP Control Register

Bit	DOCPNEN	AOCPEN	-----	-----	-----	I_SHORT[3:0]		
Bit	7	6	5	4	3	2	1	0
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W

DOCPNEN [7]	Digital OCPN enable: 0 : Disable 1 : Enable
AOCPEN [6]	Analog OCP enable: 0 : Disable 1 : Enable
I_ SHORT [2:0]	Analog OCP SHORT level select : (OCP interrupt :OCPIF) 000 : 0.15V 001 : 0.2V 010 : 0.25V 011 : 0.3V 100 : 0.35V 101 : 0.4V 110 : 0.45V 111 : 0.5V(default)

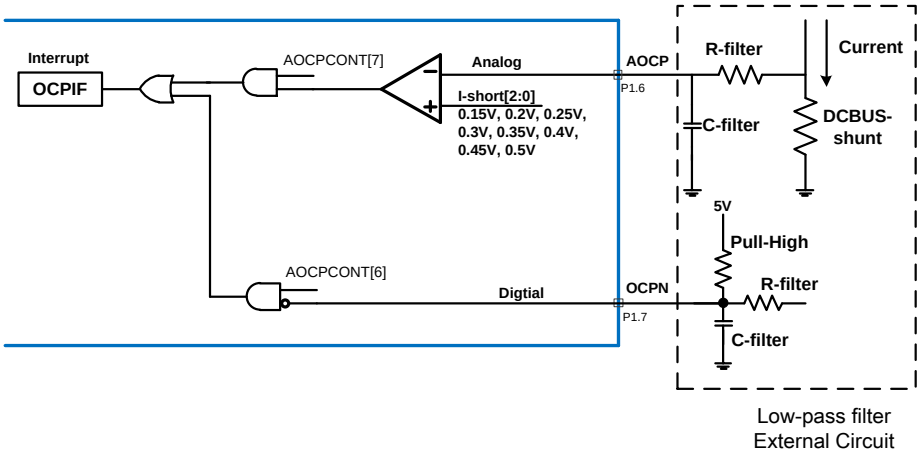
17.3.2 DOCPN Control Register (DOCPCONT)

OCPNCONT	Address = EFH	Reset Value = 0x85H

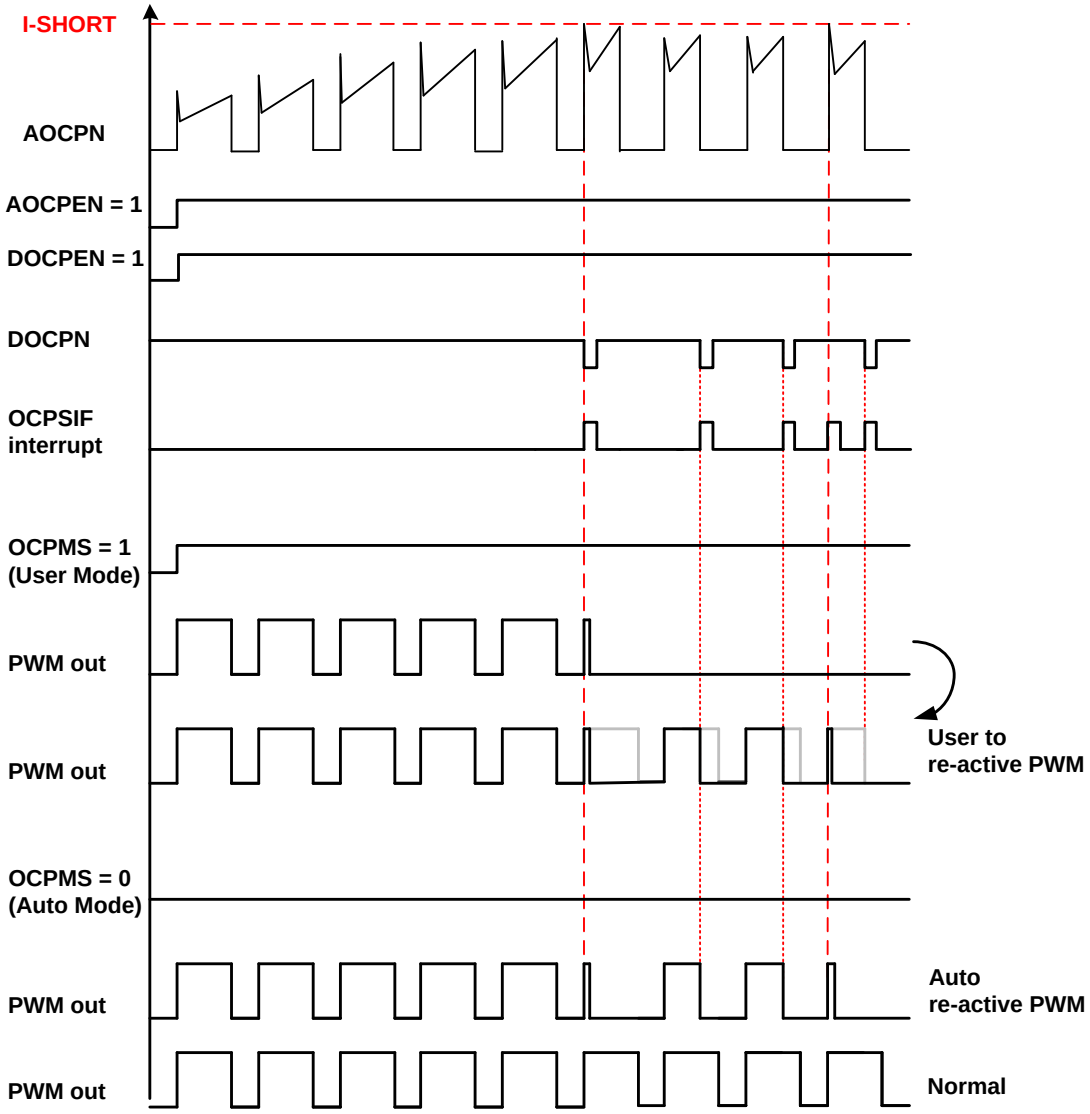
OCPN Control Register

Bit	7	6	5	4	3	2	1	0
	O	AOCPDBT[4:0]					O	O
	R	R	R	R	R	R	R/	R/

OCPST [7]	OCP Short status : 0 : No Over current Short. 1 : Over current Short occur. (hardware set OCPC = '0') Six PWM output is high-impedance.
AOCPDBT [6:2]	Analog OCP input de-bounce time (default 41.67nS) 0~31 = 0~1.291uS (48MHz/2 fixed)
OCPC [1]	OCP status clear bit : When OCP is occur, hard ware will set OCPC = '0'. In User mode, user can write '1' to clear OCP status, the PWM will output at next PWM cycle.
OCPMS [0]	OCP mode select : 0 : Auto mode. 1: User mode.



Analog OCP and Digital OCPN Unit Architecture



OCP Short occur and PWM out

17.4 Initial Angle Estimated Register (IAE)

SFR	Description	address	Reset value
INI_ANG_CTRL	Initial Angle Estimation Control Register	A5H	10H
INI_ANG_DAT	Initial Angle Estimated Data	A4H	EBH

17.4.1 IAE Control Register

INI_ANG_CTRL Address = A5H Reset Value = 0x18H

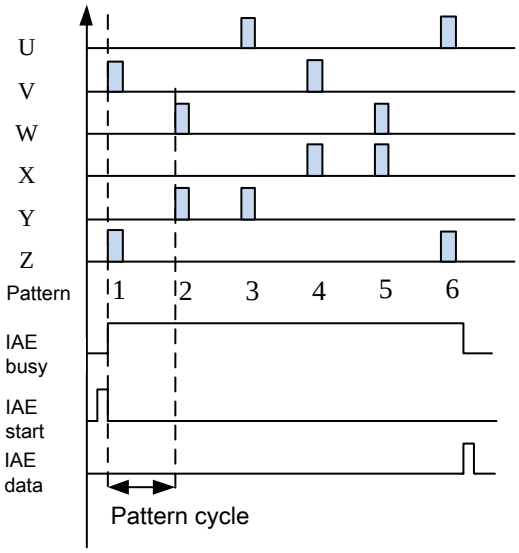
Initial Angle Control Register

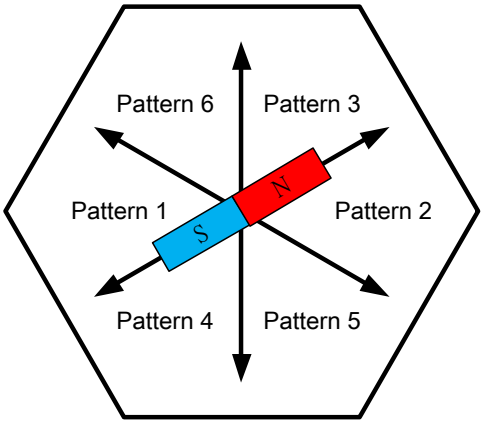
Bit	IAES	IAEPS			IAEPNS	IAECYC		IAEEN
	7	6	5	4	3	2	1	0
Type	R	R	R	R	R/W	R/W	R/W	R/W

IAES [7]	IAE State: 0:Normal 1:Busy
IAEPS [6:4]	IAE Pattern State: 001: Pattern1 010: Pattern2 011: Pattern3 100: Pattern4 101: Pattern5 110: Pattern6
IAEPNS [3]	IAE Pattern number slate: 0: 4 pattern 1: 6 pattern
IAECYC [2:1]	IAE cycle : 00: 13ms (48MHz Count) 01: 27ms (24MHz Count) 10: 54ms (12MHz Count) 11: 110ms (6MHz Count)
IAEEN [0]	IAE enable: 0: Disable 1: Enable

17.4.2 IAE Data Register

SFR	Description							
INI_ANG_DAT	Initial Angle Estimated Data							
	Parameters		Description					Reset Value
SFR_PAGE = 0	Pattern 10		IAE Pattern 1、0					0xEBH
SFR_PAGE = 1	Pattern 32		IAE Pattern 3、2					0x96H
SFR_PAGE = 2	Pattern 54		IAE Pattern 5、4					0x7DH
INI_ANG_DAT	Address = A4H		Reset Value = 0x00H					
Bit	INI_ANG_DAT [7:0]							
	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W
SFR_PAGE = 0	Pattern 1				Pattern 0			
SFR_PAGE = 1	Pattern 3				Pattern 2			
SFR_PAGE = 2	Pattern 5				Pattern 4			
	U、V、W		X、Y、Z		V、W		X、Y、Z	
	00 : -- 01 : U 10 : V 11 : W		00 : -- 01 : X 10 : Y 11 : Z		00 : -- 01 : U 10 : V 11 : W		00 : -- 01 : X 10 : Y 11 : Z	





IAE Pattern states and Rotor initial position

18. SYNC

MOC behavior is synchronized with MPWM, many MOC SFRs have shadow register that is used to update these SFRs at the same time with SYNC register. Write SYNC any value will synchronization update these SFRs at the same time.

SYNC Address = 8FH Reset Value = 00000000B

MOC Sync Register

Bit	SYNC[7:0]							
	7	6	5	4	3	2	1	0
Type	W	W	W	W	W	W	W	W

Write only.

Shadow register: (need SYNC)
MPWMCONT
MPWMDB
MPWMINV
MPWMDATAL
MPWMDATAH
CPU_ANG_L
CPU_ANG_H
VDQ_OFST_L
VDQ_OFST_H
SVPWMAMP

19. HV Gate-Driver Function Description

19.1 Low Side Power Supply (VCC15, SGND, PGND)
VCC15 is the low side supply and it provides power to both input logic and low side output power stage. In MDRFD0, input logic is referenced to SGND as well as the under-voltage detection circuit. Output power stage is referenced to PGND. PGND ground is floating respect to SGND ground with a recommended range of operation of +/-5V, which guarantees enough margin of gate to source voltage, VGS, to driver power devices such as power MOSFET.

The built-in under-voltage lockout circuit enables the device to operate at sufficient power on when a typical VCC15 supply voltage higher than VCCUV+ =9.5 is present, shown as Figure 19.1.1. The IC shuts down all the gate drivers outputs, when the VCC15 supply voltage is below VCCUV- =8.8 V, shown as Figure 19.1.1. This prevents the external power devices from extremely low gate voltage levels during on-state and therefore from excessive power dissipation.

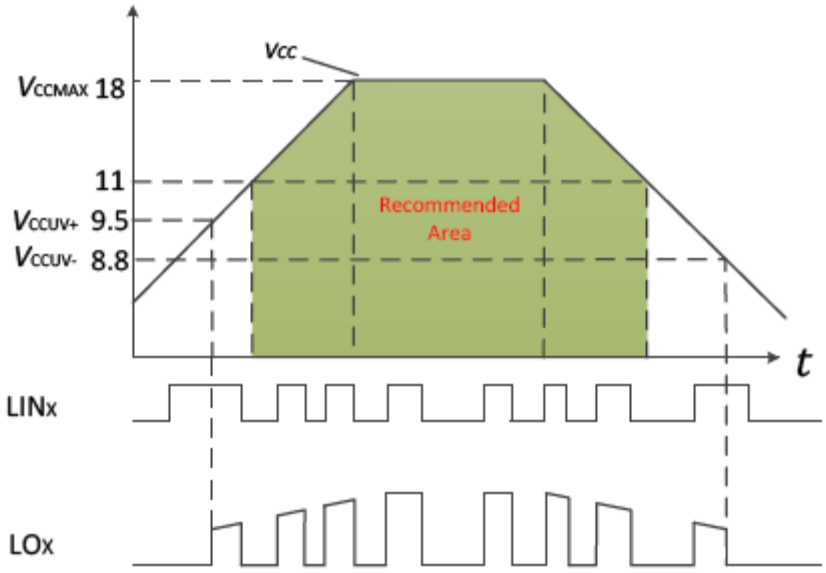


Figure 19.1.1 VCC15 supply UVLO operating area

19.2 High Side Power Supply (VBU-VSU, VBU-VSU, VBU-VSU)

VB to VS is the high side supply voltage. The totally high side circuitry can float with respect to SGND following the external high side power device emitter/source voltage. Due to the internally low power consumption, the whole high side circuitry can be supplied by bootstrap topology connected to VCC15, and it can be powered with small bootstrap capacitors.

The device operating area as a function of the supply voltage is given in Figure 19.2.1.

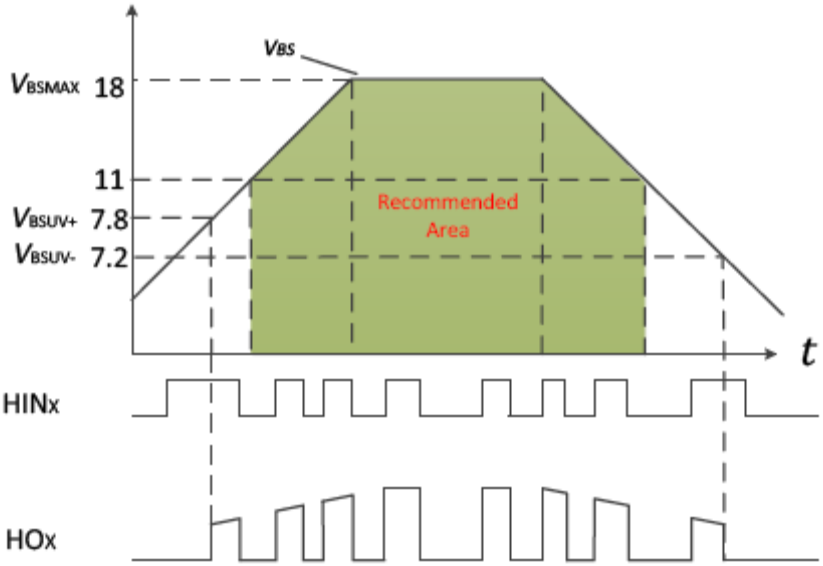


Figure 19.2.1VBS supply UVLO operating area

19.3 Low Side and High Control Input Logic (HU,V,W / LU,V,W)

The Schmitt trigger threshold of each input is designed enough low such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Input Schmitt trigger and advanced noise filter provide beneficial noise rejection to short input pulses. An internal pull-down resistor of about 200k (positive logic) pre-biases each input during VCC15 supply start-up state. It is anyway recommended for proper work of the driver not to provide input pulse-width lower than 400ns.

19.4 Shoot-Through Prevention

The IC is equipped with shoot-through prevention circuitry (also known as cross conduction prevention circuitry). Figure 19.4.1 shows how this prevention circuitry prevents both the high-side and low-side switches from conducting at the same time. During the inputs controlling high side driver and low side driver are both “high”, the both driver outputs are pulled down “low” to shut down two power devices in the same bridge.

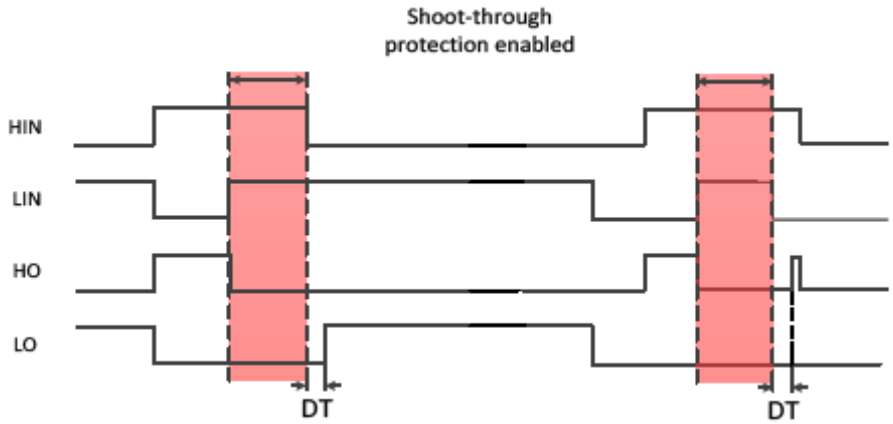


Figure 19.4.1 Shoot-through prevention

19.5 Dead-Time

The IC features integrated a fixed dead-time protection circuitry. The dead time feature inserts a time period (a minimum dead time) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum dead time is automatically inserted whenever the external dead time is shorter than DT; external dead times larger than DT are not modified by the gate driver. Figure 19.5.1 illustrates the dead time period and the relationship between the output gate signals.

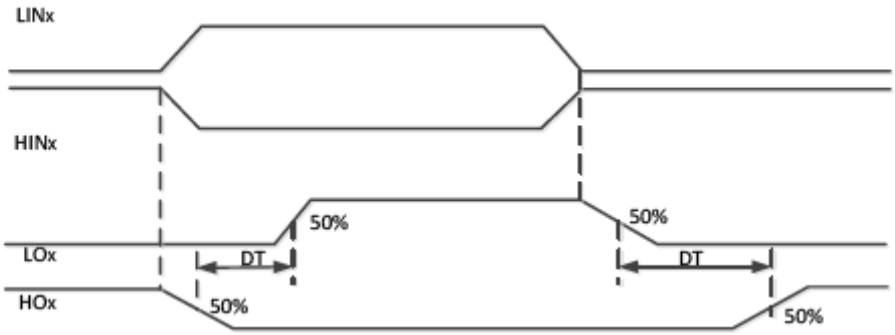


Figure 19.5.1 Dead Time

19.6 Gate Driver (HOU,V,W, LOU,V,W)

Low side and high side driver outputs are specifically designed for pulse operation and dedicated to drive the power devices such as IGBT and MOSFET. Low side outputs (i.e. LOU, V, W) are state triggered by the respective inputs, while high side outputs (i.e. HOU, V, W) are only changed at the edge of the respective inputs. In particular, after releasing from an under voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output, while after releasing from a under voltage condition of the VCC15 supply, the low side outputs can directly switch to the state of their respective inputs and don’t suffer from the trouble as high side driver.

19.7 Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device or make the function abnormal. All the voltage parameters are absolute voltages referenced to IC SGND unless otherwise stated in the table.

Parameter	Symbol	Min.	Max.	Units
High-side floating supply voltage	VB.U.V.W	-0.3	600	V
High-side offset voltage	VS.U.V.W	VB.U.V.W -18	VB.U.V.W + 0.3	
High-side gate driver output voltage	VHO.U.V.W	VS.U.V.W -0.3	VS.U.V.W +0.3	
Low-side gate driver output voltage	VLO.U.V.W	PGND-0.3	VCC15+0.3	
Logic input voltage	VH.U.V.W VL.U.V.W	-0.3	20	
Low-side supply voltage	VCC15	-0.3	20	
Logic gate driver return	PGND	VCC15-18	VCC15+0.3	
Allowable Offset Voltage Slew Rate	dV/dt		40	V/ns

19.8 Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Low-side supply voltage	VCC15	11	18	V
High-side Floating Supply Offset Voltage(note1)	VS.U.V.W	VB. -18	VB-11	
High-side Floating Supply Voltage	VB.U.V.W	-8	600	
High-side gate driver output voltage	VHO.U.V.W	VS	VB	
Low-side gate driver output voltage	VLO.U.V.W	PGND	VCC15	

Note1: For VBS=12V, normal Logic operation for VS of –8 V to 600 V. The parameter is only guaranteed by design.

19.9 Static Electrical Characteristics

（VCC15-SGND）=(VB-VS)=12V. TAMB=25℃unless otherwise specified. The VIN, VTH and IIN Parameters are reference to SGND and are applicable to all six channels. The VO and IO parameters are referenced to respective VS and PGND and are applicable to the respective output leads. The VCCUV parameters are referenced to SGND. The VBSUV parameters are referenced to VS.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Low Side Power Supply Characteristics						
VCC15 quiescent current in UVLO mode	IQVCC	VH.U.V.W =VL.U.V.W=0 or 5V	200	350	500	μA
VCC15 operating VCC15 supply current	IVCCOP	f L.U.V.W=20k, f H.U.V.W=20k,	-	1200	-	
VCC15 supply under-voltage positive going threshold	VCCUV+		8	9	10	V
VCC15 supply under-voltage negative going threshold	VCCUV-		8	8	10	
VCC15supply under-voltage lockout hysteresis	VCCHYS		-	0.7	-	
High Side Floating Power Supply Characteristics						
High side VBS supply under-voltage positive going threshold	VBSUV+		8	9	10	V
High side VBS supply under-voltage negative going threshold	VBSUV-		7	8	9	
High side VBS supply under-voltage lockout hysteresis	VBSUVHYS		-	0.6	-	
High side VBS quiescent current in UVLO mode	IQBS	VBS=12V	35	54	75	μA
Offset supply leakage current	ILK	VB=VS=600V VCC15=0V	-	-	1	
Gate Driver Output Section						
High Side Output High Short-Circuit Pulse Current	IHO+	VHO=VS=0	-	160	-	mA
High Side Output Low Short-Circuit Pulse Current	IHO-	VHO=VB=12V	-	340	-	
Low Side Output High Short-Circuit Pulse Current	ILO+	VLO=PGND=0	-	160	-	
Low Side Output Low Short-Circuit Pulse Current	ILO-	VLO=VCC15=12V	-	340	-	
Allowable Negative VS Pin Voltage for HU.V.W Signal Propagation to HOU.V.W	VSN	VBS=12V	-	-10	-	V

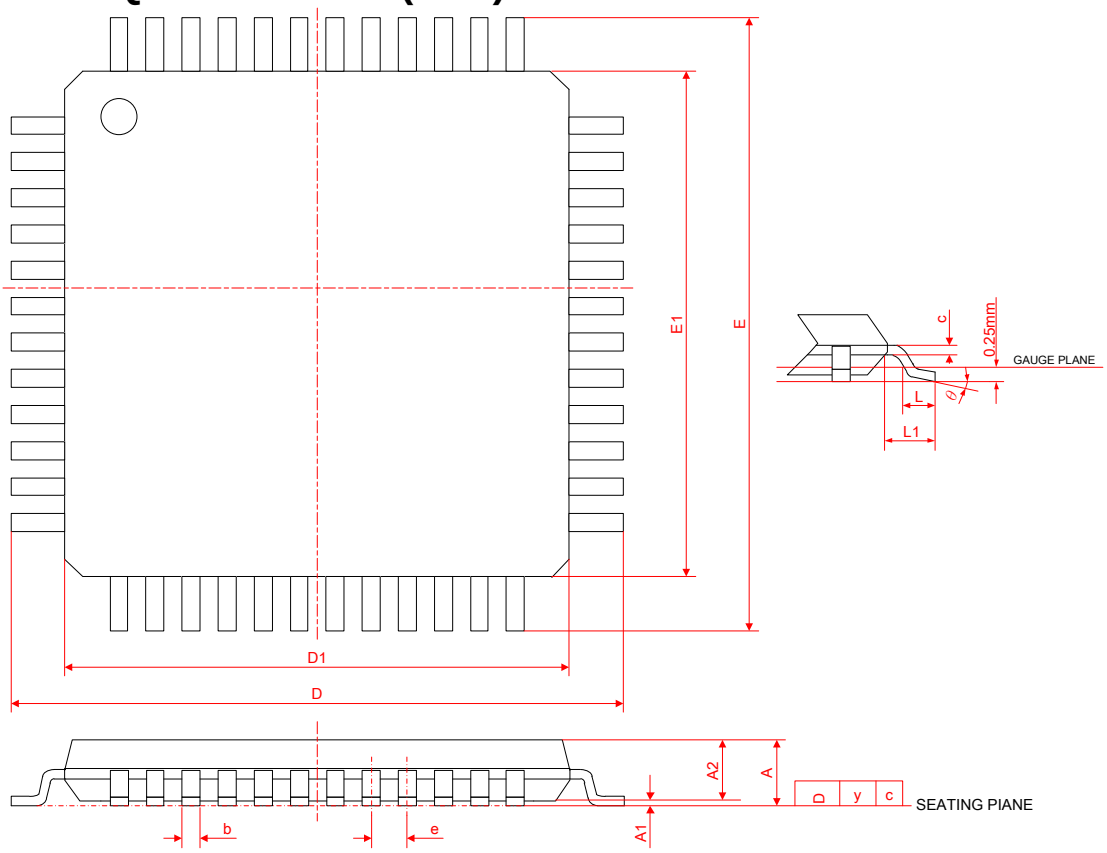
19.10 Dynamic Electrical Characteristics

（VCC15-SGND）=(VB-VS)=12V ,Vs.u.v.w=SGND=PGND, and C load=1nF unless otherwise specified, TAMB=25℃.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn-On propagation delay	tON	VH.U.V.W or VL.U.V.W=5V, VS.U.V.W=0	300	510	700	ns
Turn-Off Propagation delay	tOFF	VH.U.V.W or VL.U.V.W=0, VS.U.V.W=0	300	570	700	
Turn-On Rise time	tR	VH.U.V.W or VL.U.V.W=5V, VS.U.V.W=0	-	90	-	
Turn-Off Fall time	tF	VH.U.V.W or VL.U.V.W=0, VS.U.V.W=0	-	40	-	
Input Filtering Time	tFLT,IN			400		
Dead Time	DT		150	230	310	
Dead-Time Matching(All Six Channels)	MDT		-	-	100	
Delay Matching(All Six Channels)	MT		-	-	150	
Output Pulse-Width Matching	PM	PWIN=10us, PM=PWOUT-PWIN	-	-	100	

20. Package Information

20.1 LQFP48 7x7mm (AA2) Outline Dimensions



Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nor.	Max.	Min.	Nor.	Max.
A	—	—	1.60	—	—	63.0
A1	0.05	—	0.15	2.0	—	6.0
A2	1.35	1.40	1.45	53.0	55.0	57.0
b	0.17	0.22	0.27	6.7	8.7	10.6
c	0.178 TYP			7.0 TYP		
e	0.50 BSC			19.7 BSC		
D	8.90	9.00	9.10	350.0	354.0	358.0
D1	6.90	7.00	7.10	272.0	276.0	280.0
E	8.90	9.00	9.10	350.0	354.0	358.0
E1	6.90	7.00	7.10	272.0	276.0	280.0
L	0.50	0.60	0.70	20.0	24.0	28.0
L1	1.00 REF			1.00 REF		
y	—	—	0.10	—	—	3.9
θ	0°	3.5°	7.0°	0°	3.5°	7.0°

21. Revision History

Update Date	Version	Modify content
2023/01/31	V1.6	Delete QFN45 8x8mm (ABA) Outline Dimensions Delete QFN 45 Pin Assignments Modify Standard Product Name.

22. Disclaimers

Herein, Megawin stands for "***Megawin Technology Co., Ltd.***"

Life Support — This product is not designed for use in medical, life-saving or life-sustaining applications, or systems where malfunction of this product can reasonably be expected to result in personal injury. Customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify Megawin for any damages resulting from such improper use or sale.

Right to Make Changes — Megawin reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in mass production, relevant changes will be communicated via an Engineering Change Notification (ECN).