

MDF151A

Arm® Cortex®-M0 based 32-bit Microcontrollers

Data Sheet

Version: 0.1

Features

- Built-in dual 12V and 5V output LDO regulators
- Built-in 3 sets **150V** NN gate drivers
- Core: Arm® Cortex®-M0 32-bit MCU, operating frequency up to **60MHz**
- Hardware divider (32-bit)
- Up to **32KB** Flash program memory
- Up to **4KB** SRAM
- **3KB** independent Flash space available for program or data storage
- Wide range operating voltage is from 2.5V ~ 5.5V
- Power-on reset/Power down reset (POR/PDR), programmable voltage detector (PVD)
- Built-in 60MHz high-speed RC oscillator with factory calibration
- 40KHz LSI
- Low power stop mode with a power consumption of 100uA
- One **12-bit ADC** (analog-to-digital converter) with conversion rate up to **1M** SPS (11 input channels)
 - Supports configuration of sampling time and resolution
 - On-chip temperature sensor
 - On-chip voltage sensor
 - Conversion range: 0~V_{DD}
 - Ten external channels
 - Supports injection mode
 - Supports multiple data buffer groups
- Two analog comparators
- Two rail-to-rail operational amplifiers
- One DMA controller with 2 channels
 - Supported peripherals include Timer, ADC, and USART
- Up to **20** fast I/O ports:
 - All I/O ports can be mapped to 16 external interrupts
 - All ports support V_{DD} signal input/output
- **7 timers**
 - One 16-bit 4-channel advanced control timer (TIM1) with 4-channel PWM complimentary outputs and dead zone generation, hardware phase shifting, and brake functions
 - One 32-bit general-purpose timer (TIM2) with up to 4 input capture/output compare channels
 - Two 16-bit basic timers (TIM3, TIM4) with 1 input capture/output compare channels
 - One 16-bit timer (TIM6) supporting interrupt triggering
 - One independent watchdog timer
 - One SysTick timer with 24-bit decrementing counter
- Serial Wire Debug (SWD) interface to support debug mode
- One USART interface supporting UART and SPI communication
- 96-bit unique chip ID (UID)
- Available in QFN32, QFN40, and LQFP48 packages

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1 General Introduction

1.1. Overview

The MDF151A is a highly integrated motor control MCU that integrates three main functional blocks: 12V and 5V output LDO regulators, three integrated NN gate drivers, and a high-performance 32-bit motion control MCU to provide users with a low-cost, space-saving motor-control MCU solution.

The MCU entity built into the MDF151A is the MDF101, which uses a Cortex®-M0 core and can operate at a maximum frequency of 60MHz. It features 32KB of built-in high-speed memory and up to 26 GPIOs, of which 6 GPIOs are used for internal gate driver control, resulting in 20 actual GPIO pins. The MCU also integrates one 12-bit analog-to-digital converter (ADC) channel, two analog comparator (COMP) channels, two operational amplifier (OPAMP) channels, one 32-bit general-purpose timer, three 16-bit basic timers, and one 16-bit advanced timer. It also provides a USART interface for UART or SPI communication.

This product series features a built-in 150V gate driver and operates within a temperature range of -40°C to 105°C.

The product is available in the following package types: QFN32, QFN40, and LQFP48.

This MCU boasts a rich peripheral configuration, suitable for various applications:

Motor drives and application control

Servo fans, [Turbo fans](#), two-wheeled vehicles, power tools, garden tools

2. Specification

2.1. Model List

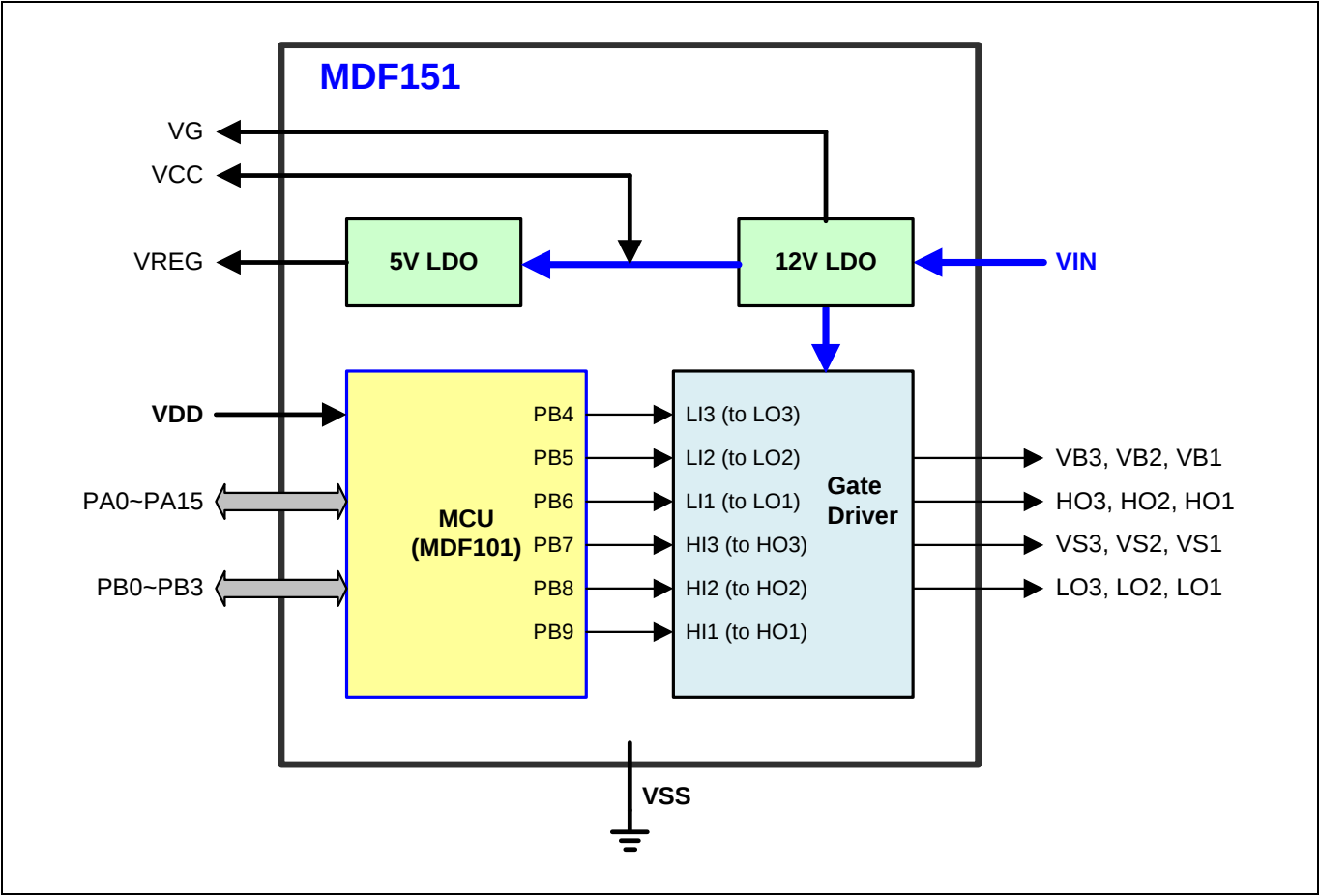
2.1.1. Ordering Information

Table 1 Ordering information

Model		MDF151AAZ32	MDF151AAY40	MDF151AAD48
Peripheral				
CPU Frequency		60MHz	60MHz	60MHz
FLASH memory KB		32	32	32
SRAM KB		4	4	4
Timer	General-purpose (32 bit)	1	1	1
	Basic	3	3	3
	Advanced	1	1	1
Communication interface	USART	1	1	1
Number of GPIO ports		20	20	20
12-bit ADC	Number	1	1	1
	Number of channels	11	11	11
Comparator		2	2	2
Operational amplifier		2	2	2
Working voltage		9V~21V	9V~21V	9V~21V
Working temperature		-40°C~ +105°C	-40°C~ +105°C	-40°C~ +105°C
Package		QFN32	QFN40	LQFP48

2.1.2. Block Diagram

Figure 1 Block diagram

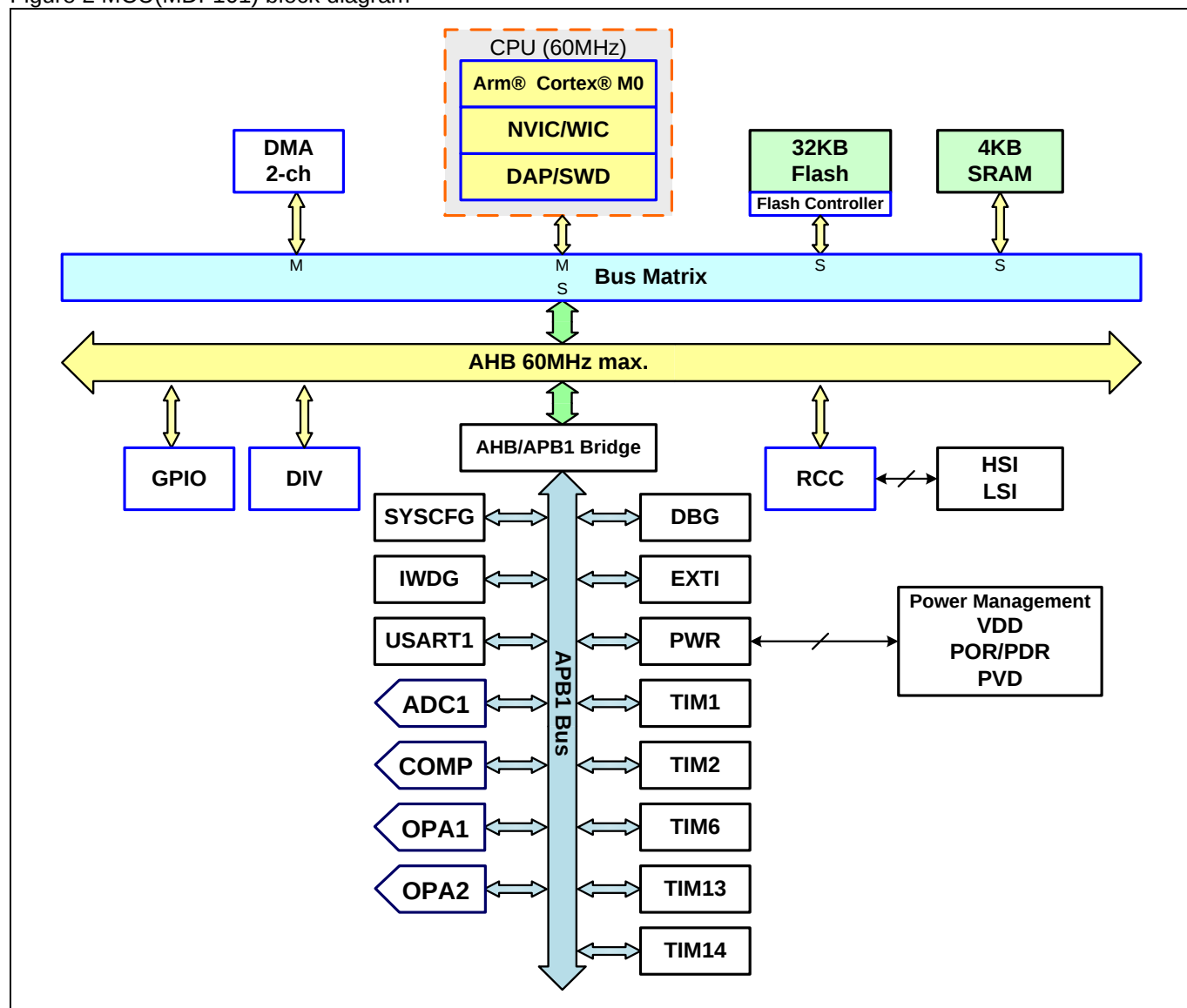


2.2. MDF151Built-in MCU Functional Description

The MCU built into the MDF151 is the standard MCU MDF101 from Shengquan. For detailed information on the functions and development environment of the MCU in the MDF151, please refer directly to the relevant data of the MDF101, such as the user manual and development toolkit. All of the aforementioned data can be found on the MDF101 product introduction page of Shengquan's official website.

2.2.1. MCU(MDF101) Core Introduction

Figure 2 MCU(MDF101) block diagram



2.2.2. MCU Core Introduction

The MDF101 core is an Arm® Cortex®-M0 processor, the latest generation of embedded Arm processors, providing a low-cost platform, reducing pin count, and lowering system power consumption to meet the needs of MCUs. It offers excellent computing performance and advanced interrupt system response.

This product features a built-in Arm core, making it compatible with all Arm tools and software.

2.2.3. Bus Overview

The MDF101A adopts a matrix bus structure, including an AHB interconnect matrix, an AHB bus, and a bridged APB bus.

2.2.4. Memory Map

Table 2 Memory map

	Address Range	Size	Peripheral
Flash	0x0000 0000 - 0x0000 7FFF	32 KB	Can be mapped as main flash memory, data memory, system memory, or SRAM, depending on the configuration of the BOOT.
	0x0000 8000 - 0x07FF FFFF	~127 MB	Reserved
	0x0800 0000 - 0x0800 7FFF	32 KB	Main memory
	0x0800 8000 - 0x1FFD FFFF	~383 MB	Reserved
	0x1FE0 0000 - 0x1FE0 0BFF	3KB	Data memory
	0x1FE0 0C00 - 0x1FFF F3FF	~2MB	Reserved
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System memory
	0x1FFF F800 - 0x1FFF F9FF	0.5KB	Option bytes
	0x1FFF FA00 - 0x1FFF FFFF	1.5KB	Reserved
SRAM	0x2000 0000 - 0x2000 0FFF	4 KB	SRAM
	0x2000 1000 - 0x2FFF FFFF	~255 MB	Reserved
APB1	0x4000 0000 - 0x4000 03FF	1KB	TIM2
	0x4000 0400 - 0x4000 0FFF	3KB	Reserved
	0x4000 1000 - 0x4000 13FF	1KB	TIM6
	0x4000 1400 - 0x4000 17FF	1KB	Reserved
	0x4000 1800 - 0x4000 1BFF	1KB	TIM13
	0x4000 1C00 - 0x4000 2FFF	5KB	Reserved
	0x4000 3000 - 0x4000 33FF	1KB	IWDG
	0x4000 3400 - 0x4000 6FFF	15KB	Reserved
	0x4000 7000 - 0x4000 73FF	1KB	PWR
	0x4000 7400 - 0x4000 8FFF	7KB	Reserved
	0x4000 9000 - 0x4000 93FF	1KB	OPA1
	0x4000 9400 - 0x4000 97FF	1KB	OPA2
	0x4000 9800 - 0x4000 FFFF	26KB	Reserved
	0x4001 0000 - 0x4001 03FF	1KB	SYSCFG
	0x4001 0400 - 0x4001 07FF	1KB	EXTI
	0x4001 0800 - 0x4001 0BFF	1KB	Reserved
	0x4001 0C00 - 0x4001 0FFF	1KB	USART1
	0x4001 1000 - 0x4001 23FF	5KB	Reserved
	0x4001 2400 - 0x4001 27FF	1KB	ADC1
	0x4001 2800 - 0x4001 2BFF	1KB	Reserved
	0x4001 2C00 - 0x4001 2FFF	1KB	TIM1
	0x4001 3000 - 0x4001 33FF	1KB	Reserved

	Address Range	Size	Peripheral
	0x4001 3400 – 0x4001 37FF	1KB	DBG
	0x4001 3800 – 0x4001 3BFF	1KB	Reserved
	0x4001 3C00 – 0x4001 3FFF	1KB	COMP
	0x4001 4000 – 0x4001 43FF	1KB	TIM14
	0x4001 4400 – 0x4001 FFFF	47KB	Reserved
AHB	0x4002 0000 – 0x4002 03FF	1KB	DMA
	0x4002 0400 – 0x4002 0FFF	3KB	Reserved
	0x4002 1000 – 0x4002 13FF	1KB	RCC
	0x4002 1400 – 0x4002 1FFF	3KB	Reserved
	0x4002 2000 – 0x4002 23FF	1KB	Flash Interface
	0x4002 2400 – 0x4002 FFFF	55KB	Reserved
	0x4003 0000 – 0x4003 03FF	1KB	HWDIV
	0x4003 0400 – 0x47FF FFFF	~128MB	Reserved
	0x4800 0000 – 0x4800 03FF	1KB	PORT A
	0x4800 0400 – 0x4800 07FF	1KB	PORT B

2.2.5. Built-in Flash

Built-in 32KB + 3KB Flash for storing programs and data.

2.2.6. Built-in SRAM

Built-in 4KB SRAM.

2.2.7. Nested Vectored Interrupt Controller (NVIC)

This product features a built-in nested vectored interrupt controller capable of handling multiple maskable interrupt channels (excluding the 16 Cortex®-M0 interrupt lines) and 4 programmable priorities.

Tightly coupled NVIC for low-latency interrupt response handling

Interrupt vector entry address directly enters the core

Allows early interrupt processing

Processes subsequent high-priority interrupts

Supports interrupt tail-chaining functionality

Automatically saves processor state

Automatically restores state upon interrupt return, requiring no additional instructions

This module provides flexible interrupt management with minimal interrupt latency.

2.2.8. External Interrupt/Event Controller (EXTI)

The external interrupt/event controller includes multiple edge detectors to capture level changes from I/O pins and generate interrupt/event requests. All I/O pins can be connected to 16 external interrupt lines. Each interrupt line can be enabled or disabled independently and configured with its own trigger mode (rising edge, falling edge, or both). A pending status register maintains the status of all interrupt requests.

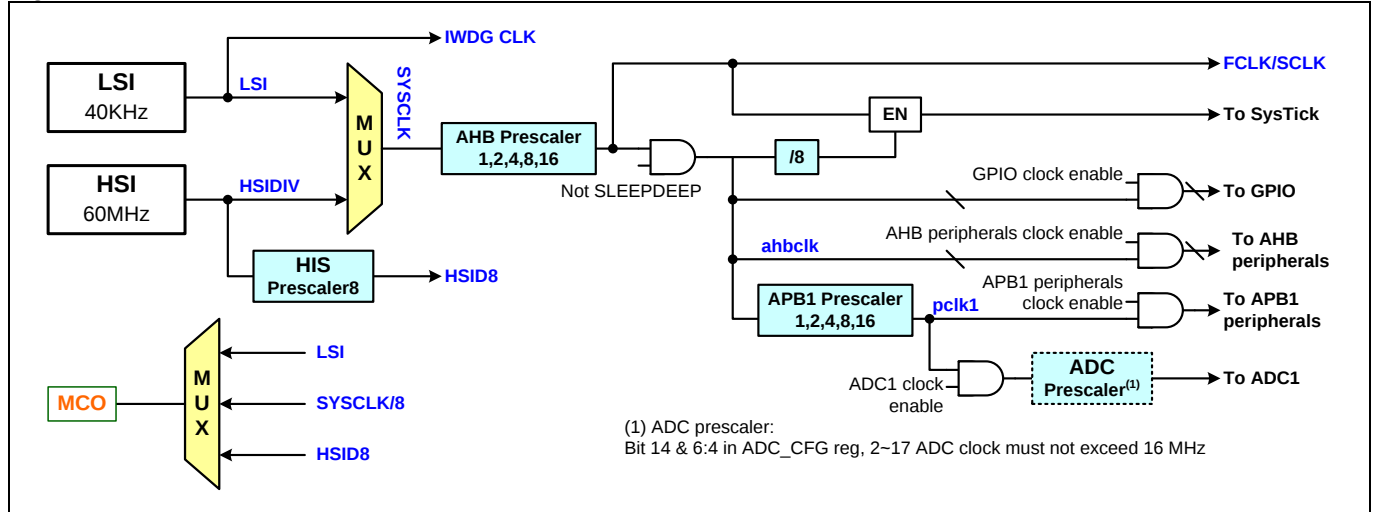
EXTI can detect level changes with a pulse width shorter than the internal AHB bus clock cycle.

2.2.9. Clock and Boot

After chip startup, a system clock is selected. Upon reset, an internal 60MHz oscillator is used as the default system clock, configured with an 8-divider. The system clock distributor configuration can be changed to increase the system frequency (wait control for Flash access must be considered).

In the clock system, multiple prescalers are used to generate clocks for the AHB bus and the high-speed APB1 bus. The clock frequencies for the AHB and high-speed APB buses can reach up to 60MHz. The clock tree of the clock system is shown in the figure below.

Figure 3 Clock tree



2.2.10. Boot Modes

During startup, one of four boot modes can be selected using the BOOT0 pin and the BOOT0SEL bit:

- Boot from the program memory
- Boot from the system memory
- Boot from the data memory
- Boot from the internal SRAM

The bootloader is located in the system memory and can be programmed via a serial interface, such as USART1.

2.2.11. Power Supply Schemes

$V_{DD} = 2.5V \sim 5.5V$: The I/O pins and internal regulators are powered through the V_{DD} pin. It provides power to the ADC, reset module, and oscillator.

2.2.12. Power Supply Supervisors

The product incorporates an internal power on reset (POR)/power down reset (PDR) circuit that is always active and ensures proper operation when the system voltage exceeds 2.5V. When V_{DD} drops below the set threshold (V_{POR}/V_{PDR}), the device is held in a reset state.

The device also includes a programmable voltage detector (PVD) that monitors the V_{DD} supply and compares it to the threshold voltage (V_{PVD}). When V_{DD} goes below or above the threshold, an interrupt is generated, and the interrupt handler can issue warning messages or transition the microcontroller into a safe mode. The PVD function needs to be enabled through software.

2.2.13. Voltage Regulator

The on-chip voltage regulator converts the external voltage to the operating voltage for the internal circuitry. The voltage regulator remains active after the chip is reset.

2.2.14. Low-Power Mode

The product supports low-power mode, which can achieve the optimal balance between low power consumption and fast startup.

Table 3 Low-power mode list

Mode	Entry	Wake-up	Impact on 1.5V domain clock	Impact on V _{DD} area clock	Voltage regulator	Impact on data and registers	Notes
Sleep Mode	WFI (Wait for Interrupt)	Any interrupt	CPU clock off, no influence on other clocks and ADC clock	No	On		Peripheral clocks continue, contents of registers and SRAM retained
	WFE (Wait for Event)	Wake-up event					
Stop Mode	Set SLEEPDEEP bit; WFI or WFE	Any external interrupt (configured in external interrupt registers) or event, IWDG interrupt (non-reset)	All clocks operating in the 1.5V domain are off	HSI off	On	Contents of registers and SRAM retained	PIOs not used before entering low-power mode should be set to analog input state

Sleep Mode

In Sleep Mode, the CPU is stopped, but all peripherals, including CPU peripherals such as NVIC and SysTick, continue to operate.

Stop Mode

Stop Mode achieves lower power consumption while preserving the contents of SRAM and registers. In Stop Mode, HSI is turned off. The microcontroller can be woken up from Stop Mode by any signal configured as EXTI, which can be one of the 16 external I/O pins or the wake-up signal from the PVD.

2.2.15. Hardware Divider (HWDIV)

The built-in hardware divider unit automatically performs signed or unsigned 32-bit integer division operations. Hardware division is particularly useful in high-performance applications.

2.2.16. Direct Memory Access Controller (DMA)

The flexible 2-channel general-purpose DMA manages data transfers between memory to memory, device to memory, and memory to device. The DMA controller supports circular buffer management, avoiding interrupts when the controller reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic and can also be triggered by software. The length of the transfer, source address, and destination address can all be set separately by software.

DMA can be used with major peripherals such as USART, ADC, and general/basic/advanced control timers TIMx.

2.2.17. Timers and Watchdog (TIMs & WDG)

The product includes 1 advanced control timer, 1 general-purpose timer, and 3 basic timers, as well as 1 watchdog timer and 1 SysTick timer. The following table compares the features of the advanced control timer, general-purpose timer, and basic timers:

Table 4 Timer function comparison

Timer type	Name	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channel	Complementary output
Advanced	TIM1	16-bit	up, down, up/down	Any integer between 1 and 65536	Yes	No/4	Yes
General-purpose	TIM2	32-bit	up, down, up/down	Any integer between 1 and 65536	Yes	4/4	No
Basic	TIM6	16-bit	up	Any integer between 1 and 65536	Yes	No	No
	TIM13/14	16-bit	up	Any integer between 1 and 65536	Yes	1/1	No

Advanced-control timer (TIM1)

The advanced control timer consists of a 16-bit counter, 4 compare channels, and a three-phase complementary PWM generator. It provides complementary PWM outputs with dead-time insertion and can also be used as a full-featured general-purpose timer. The four independent channels can be used for:

- Output comparison
- PWM generation (edge or center-aligned mode)
- Single-pulse output

When configured as a 16-bit general-purpose timer, it has the same functionality as the TIM2 timer. When configured as a 16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In debug mode, the counter can be frozen, and PWM output can be disabled, cutting off the switches controlled by these outputs.

Many features are the same as those of general-purpose timer, and the internal structure is also the same. Therefore, the advanced control timer can be used in conjunction with the general-purpose timer via timer chaining feature to provide synchronization or event chaining functionality.

32-bit general-purpose timer (TIM2)

The product has a built-in general-purpose timer (TIM2) that can run synchronously. The timer features a 32-bit auto-reload up/down counter, a 16-bit prescaler, and 4 independent channels. Each channel can be used for input capture, output compare, PWM, and single-pulse mode output.

Basic timer (TIM6)

The basic timer is based on a 16-bit programmable prescaler and a 16-bit auto-reload counter. It provides a convenient counting and timing function, and the counter clock signal is obtained by dividing the clock source with a prescaler.

Basic timer (TIM13/14)

The basic timers are based on a 16-bit programmable prescaler and a 16-bit auto-reload counter. The counter clock signal is obtained by dividing the clock source with a prescaler. TIM13/14 have multiple uses, such as input functions (measuring pulse width, frequency, etc. of input signals) and output functions (PWM output, comparison output, etc.).

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 40kHz oscillator. This oscillator runs independently of the main clock and can operate in all operating modes. The IWDG can be used to reset the entire system when a problem occurs or as a free-running timer for timeout management in applications. It can be configured as a software or hardware startup watchdog through option bytes. In debug mode, the counter can be frozen.

SysTick timer (Systick)

This timer is dedicated to real-time operating systems but can also be used as a standard down counter. It has the following features:

- 24-bit down counter
- Auto-reload feature
- Generates a mask interrupt when the counter reaches 0
- Programmable clock source

2.2.18. General Purpose Input/ Output (GPIO)

Each GPIO pin can be configured by software as an output (push-pull or open-drain), an input (with or without, pull-up or pull-down), or a multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals.

In case of need, the peripheral function of an I/O pin can be locked through a specific operation to prevent accidental writes to the I/O registers.

2.2.19. Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The USART supports asynchronous mode (UART) and synchronous mode. The UART supports single-wire half-duplex communication, and both UART and synchronous modes support modem control operations (CTS/RTS hardware automatic flow control).

The USART interface supports DMA operations and can achieve data communication with SPI in synchronous mode.

2.2.20. Analog-to-Digital Converter (ADC)

The product has a built-in 12-bit analog-to-digital converter (ADC) with 10 available external channels. It can perform single, single-cycle, and continuous scan conversions. In scan mode, it automatically converts the values in a selected set of analog input. The ADC supports DMA operations.

The analog watchdog feature allows precise monitoring of one or all selected channels. An interrupt is generated when the monitored signal exceeds a predefined threshold.

Events generated by timers (TIMx) can be connected to the trigger input of the ADC, allowing configuration of ADC conversions synchronized with the clock.

Temperature Sensor

The temperature sensor generates a voltage that varies linearly with temperature and can be connected internally to an ADC input channel.

2.2.21. Analog Comparator (COMP)

The product is embedded with two comparators that can be used independently or in combination with a timer. The COMP module can be utilized for various functions, including:

- Triggering low-power mode wakeup events by analog signals
- Supporting window control function to suppress current overshoot glitches generated when PWM is turned on
- Combining with PWM output from a timer to form a per-cycle current control loop
- Each comparator has selectable thresholds
- The internal 8-bit CRV (Comparison Reference Voltage) can be selected as VDD or a voltage value divided from the internal reference voltage
- Programmable hysteresis voltage
- Implementing Cyclic polling function with fixed periods
- Programmable speed and power consumption
- The output can be redirected to an I/O port or multiple timer input ports, triggering the following events:
 - Capture events
 - OCref clr events (per-cycle current control)
- Supporting brake events for fast PWM shutdown.

2.2.22. Operational Amplifier (OPAMP)

The chip is embedded with two operational amplifiers, and the input and output of each operational amplifier are connected to I/O, allowing them to be connected with ADC and comparators through shared I/O. Rail-to-rail input/output are also supported.

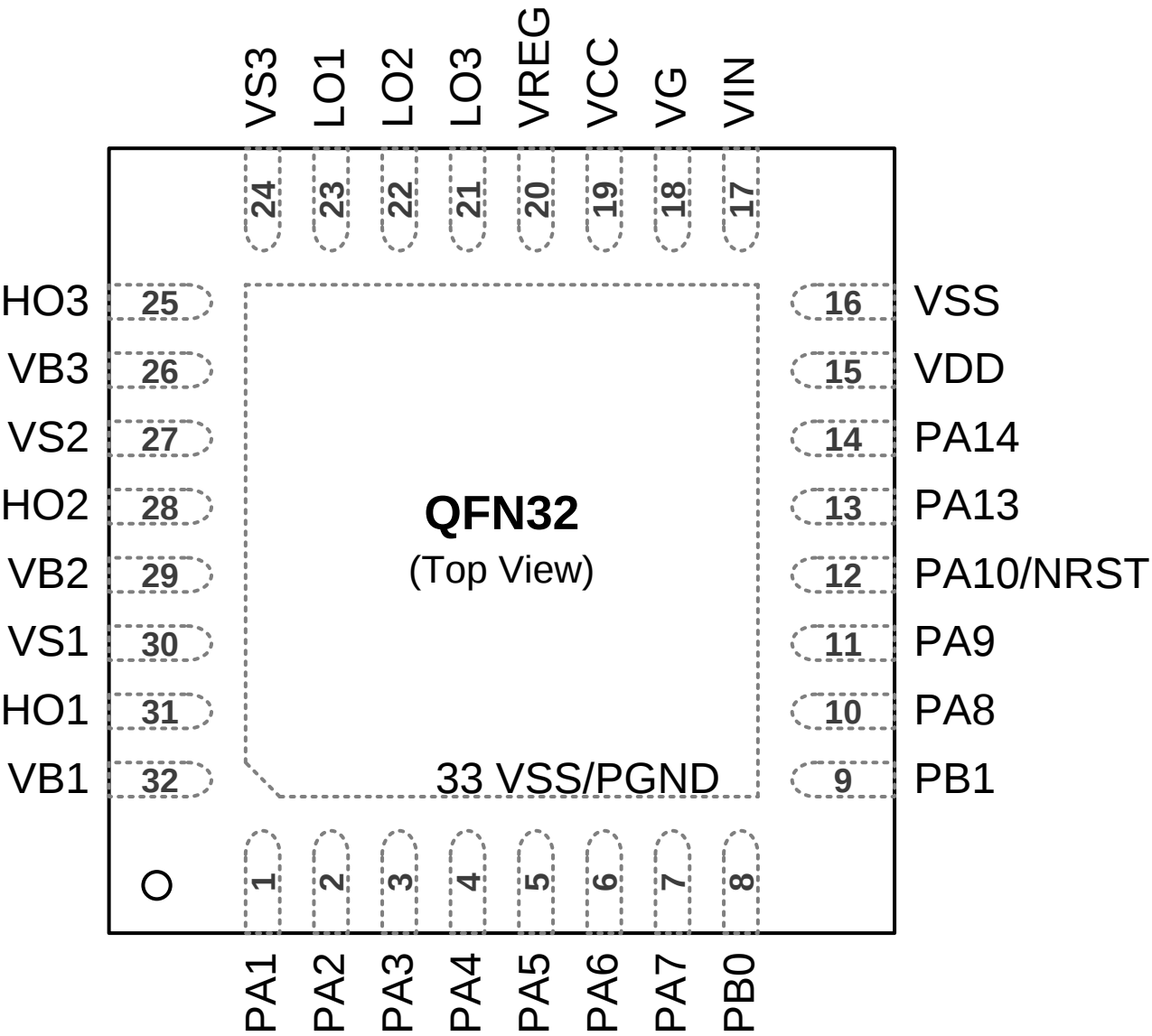
2.2.23. Serial Wire Debug (SWD)

Embedded with the Arm-standard two-wire serial debugging interface (SW-DP).

3. Pin Definition and Alternate Function

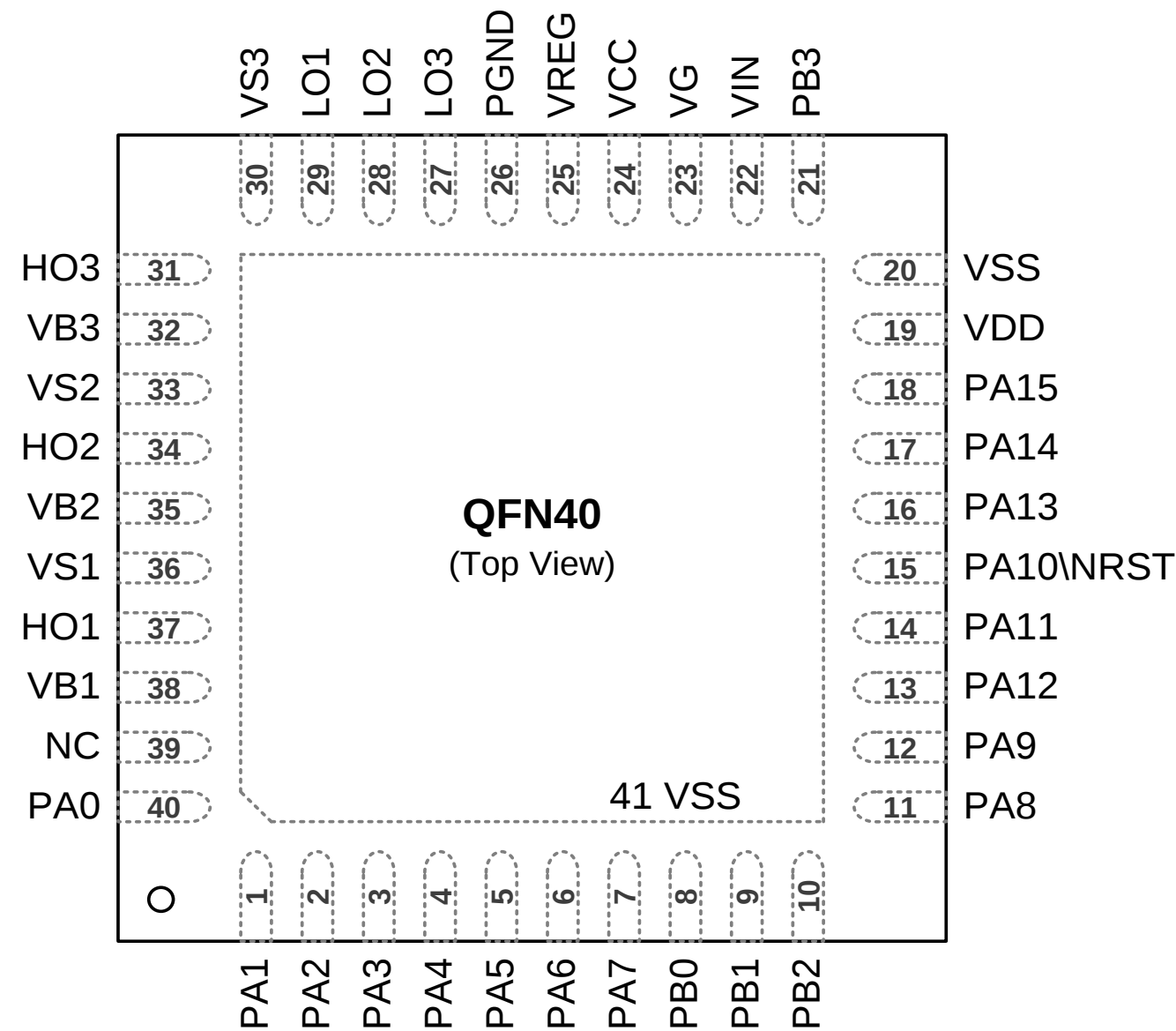
3.1. QFN32 Pinout Diagram

Figure 4 QFN32 pinout diagram



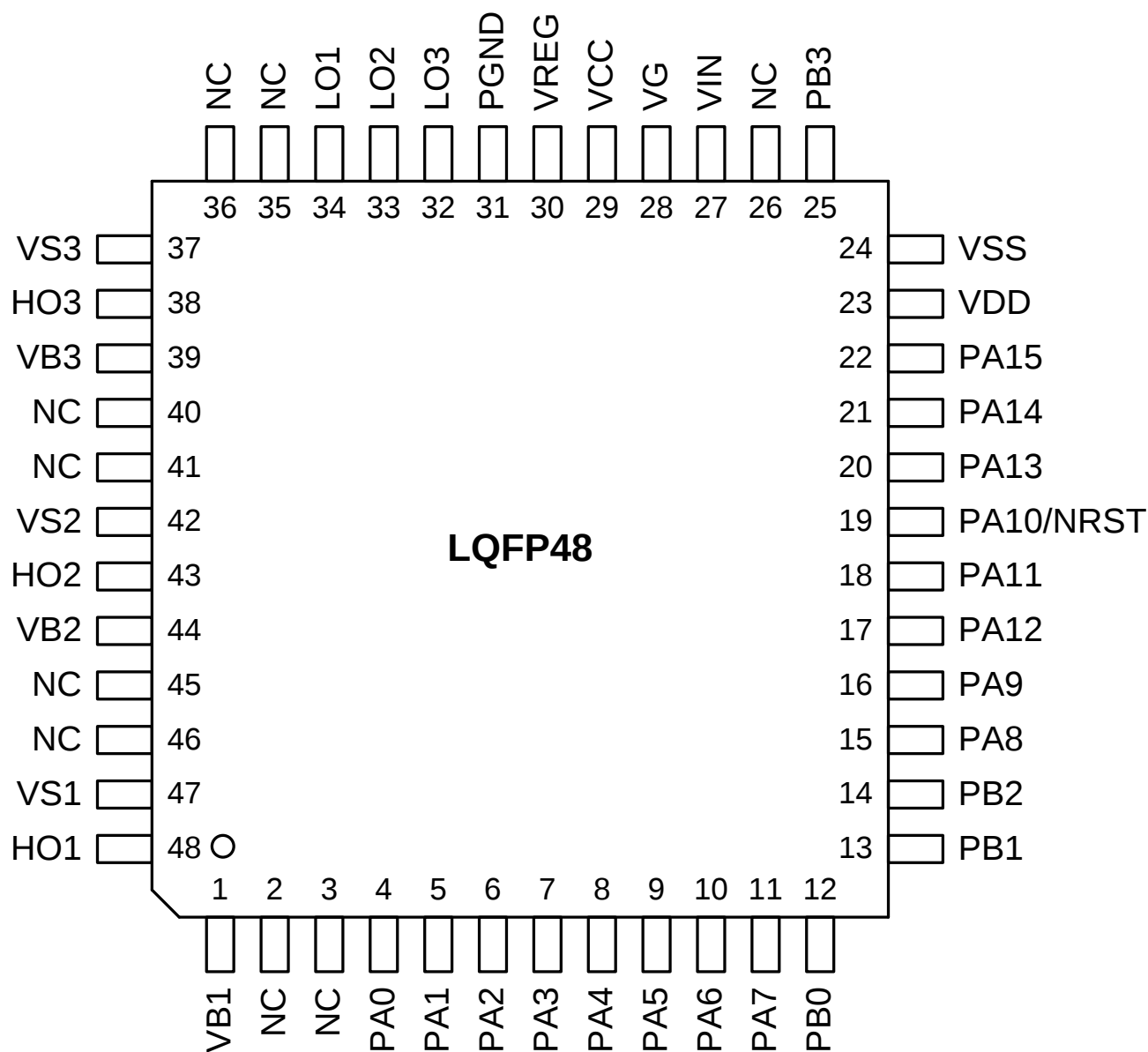
3.2. QFN40 Pinout Diagram

Figure 5 QFN40 pinout diagram



3.3. LQFP48 Pinout Diagram

Figure 6 LQFP48 pinout diagram



3.4. Pin Assignment Table

Table 5 Pin assignment table

Pin ID	Pin ID	Pin ID	Name	Type (1)	I/O level (2)	Main Function	Alternate function	Additional function
LQFP 48	QFN 40	QFN 32						
1	38	32	VB1	-	-	Bootstrap supply voltage 1	-	-
2	39	-	NC	-	-	NC	-	-
3	-	-	NC	-	-	NC	-	-
4	40	-	PA0	I/O	TC	PA0	TIM2_CH1 TIM13_CH1 TIM1_BKIN4 USART1_SCLK ADC_TRIG_O	BOOT0
5	1	1	PA1	I/O	TC	PA1	USART1_SCK USART2_TX I2C1_SDA SPI1_MOSI	-
6	2	2	PA2	I/O	TC	PA2	TIM2_ETR TIM14_CH1 TIM1_ETR TIM1_BKIN5 USART1_RX COMP2_OUT	ADC_IN1
7	3	3	PA3	I/O	TC	PA3	TIM2_CH1 TIM13_CH1 USART1_nCTS	ADC_IN2 COMP1_INP[0] OPA2_IN+
8	4	4	PA4	I/O	TC	PA4	TIM2_CH2 TIM14_CH1 USART1_nRTS	ADC_IN3 COMP1_INM[0]/ COMP2_INM[0] OPA2_IN-
9	5	5	PA5	I/O	TC	PA5	TIM2_CH3 TIM14_CH1 TIM1_ETR TIM1_BKIN6	ADC_IN4 COMP1_INP[1] OPA2_OUT
10	6	6	PA6	I/O	TC	PA6	TIM2_CH1 TIM13_CH1	COMP1_INP[2] OPA1_IN+
11	7	7	PA7	I/O	TC	PA7	TIM2_CH2 TIM14_CH1 MCO USART1_nCTS	COMP2_INM[1]/ COMP1_INM[1] OPA1_IN-
12	8	8	PB0	I/O	TC	PB0	TIM2_CH3 TIM13_CH1 USART1_nRTS	ADC_IN5 COMP2_INP[0]/ COMP1_INP[3] OPA1_OUT
13	9	9	PB1	I/O	TC	PB1	TIM2_CH4 TIM14_CH1 USART1_RX USART1_TX	ADC_IN6 COMP2_INM[2]
14	10	-	PB2	I/O	TC	PB2	TIM2_CH3 TIM13_CH1 TIM1_BKIN7	ADC_IN7 COMP2_INP[1]

Pin ID	Pin ID	Pin ID	Name	Type (1)	I/O level (2)	Main Function	Alternate function	Additional function
LQFP 48	QFN 40	QFN 32						
							USART1_SCLK	
15	11	10	PA8	I/O	TC	PA8	TIM2_CH2 TIM14_CH1 MCO USART1_TX	ADC_IN8 COMP2_INP[2]/ COMP1_INM[2]
16	12	11	PA9	I/O	TC	PA9	TIM2_CH1 TIM13_CH1 USART1_RX	ADC_IN9 COMP2_INP[3]
17	13	-	PA12	I/O	TC	PA12	TIM2_ETR TIM1_BKIN1 TIM14_CH1 USART1_RX ADC_TRIG_O COMP2_OUT	-
18	14	-	PA11	I/O	TC	PA11	TIM2_ETR ADC_TRIG_O TIM1_ETR TIM13_CH1 USART1_TX TIM2_CH1 COMP1_OUT	-
19	15	12	PA10/ NRST	I/O	TC	PA10	SPI1_MISO TIM1_CH3 TIM1_CH2 MCO USART1_TX	-
20	16	13	PA13	I/O	TC	PA13	SWDIO TIM13_CH1 USART1_SCLK USART1_RX COMP1_OUT	-
21	17	14	PA14	I/O	TC	PA14	SWDCLK TIM14_CH1 USART1_nRTS USART1_TX COMP2_OUT	-
22	18	-	PA15	I/O	TC	PA15	TIM1_CH4N TIM1_CH3 TIM1_CH4 TIM1_CH1N TIM1_CH1 TIM1_CH3N TIM13_CH1 TIM14_CH1	-
23	19	15	VDD	S	-	MCU Power Input	-	-
24	20	16	VSS	S	-	Chip Ground	-	-
25	21	-	PB3	I/O	TC	PB3	TIM1_CH4 TIM1_CH2 TIM1_CH1 TIM1_CH2N	-

MDF151A

Pin ID	Pin ID	Pin ID	Name	Type (1)	I/O level (2)	Main Function	Alternate function	Additional function
LQFP 48	QFN 40	QFN 32					TIM1_CH1N TIM1_BKIN2 TIM1_CH3N TIM1_CH3	
26	39	-	NC	-	-	NC	-	-
27	22	17	VIN	-	-	Power Supply	-	-
28	23	18	VG	-	-	12V LDO Gate Control Terminal	-	-
29	24	19	VCC	-	-	LDO 12V Output	-	-
30	25	20	VRE G	-	-	LDO 5V Output	-	-
31	26	33	PGN D	-	-	PGND	-	-
32	27	21	LO3	O	-	Gate driver low side output 3, input corresponds to PB4	-	-
33	28	22	LO2	O	-	Gate driver low side output 2, input corresponds to PB5	-	-
34	29	23	LO1	O	-	Gate driver low side output 1, input corresponds to PB6	-	-
35	39	-	NC	-	-	NC	-	-
36	39	-	NC	-	-	NC	-	-
37	30	24	VS3	-	-	High side (floating) common voltage 3	-	-
38	31	25	HO3	O	-	Gate driver high side output 3, input corresponds to PB7	-	-
39	32	26	VB3	-	-	Bootstrap supply voltage 3	-	-
40	39	-	NC	-	-	NC	-	-
41	39	-	NC	-	-	NC	-	-
42	33	27	VS2	-	-	High side (floating) common voltage 2	-	-
43	34	28	HO2	O	-	Gate driver high side output 2, input corresponds to PB8	-	-
44	35	29	VB2	-	-	Bootstrap supply voltage 2	-	-
45	39	-	NC	-	-	NC	-	-

Pin ID	Pin ID	Pin ID	Name	Type (1)	I/O level (2)	Main Function	Alternate function	Additional function
LQFP 48	QFN 40	QFN 32						
46	39	-	NC	-	-	NC	-	-
47	36	30	VS1	-	-	High side (floating) common voltage 1	-	-
48	37	31	HO1	O	-	Gate driver high side output 1, input corresponds to PB9	-	-

3.5. MCU Multiplex Function Table

Table 6 Multiplex function for PA port AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	TIM2_CH1			TIM13_CH1	TIM1_BKIN4		USART1_SCLK	ADC_TRIG_O
PA1	TIM2_ETR		TIM13_CH1	TIM2_CH2			USART1_TX	COMP1_OUT
PA2	TIM2_ETR		TIM14_CH1		TIM1_ETR	TIM1_BKIN5	USART1_RX	COMP2_OUT
PA3	TIM2_CH1		TIM13_CH1				USART1_nCTS	
PA4	TIM2_CH2		TIM14_CH1				USART1_nRTS	
PA5	TIM2_CH3		TIM14_CH1		TIM1_ETR	TIM1_BKIN6		
PA6	TIM2_CH1			TIM13_CH1				
PA7	TIM2_CH2			TIM14_CH1	MCO		USART1_nCTS	
PA8	TIM2_CH2		TIM14_CH1		MCO		USART1_TX	
PA9	TIM2_CH1		TIM13_CH1				USART1_RX	
PA10/NRST								
PA11	TIM2_ETR	ADC_TRIG_O	TIM1_ETR	TIM13_CH1		USART1_TX	TIM2_CH1	COMP1_OUT
PA12	TIM2_ETR		TIM1_BKIN1	TIM14_CH1		USART1_RX	ADC_TRIG_O	COMP2_OUT
PA13	SWDIO			TIM13_CH1		USART1_SCLK	USART1_RX	COMP1_OUT
PA14	SWDCLK			TIM14_CH1		USART1_nRTS	USART1_TX	COMP2_OUT
PA15	TIM1_CH4N	TIM1_CH3	TIM1_CH4	TIM1_CH1N	TIM1_CH1	TIM1_CH3N	TIM13_CH1	TIM14_CH1

Table 7 Multiplex function for PB port AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	TIM2_CH3			TIM13_CH1			USART1_nRTS	
PB1	TIM2_CH4			TIM14_CH1			USART1_RX	USART1_TX
PB2	TIM2_CH3		TIM13_CH1			TIM1_BKIN7	USART1_SCLK	
PB3	TIM1_CH4	TIM1_CH2	TIM1_CH1	TIM1_CH2N	TIM1_CH1N	TIM1_BKIN2	TIM1_CH3N	TIM1_CH3
PB4	TIM1_CH3N	TIM1_CH3	TIM1_CH1N	TIM1_CH1	TIM1_CH2	TIM1_CH4N	TIM1_CH4	TIM1_CH2N
PB5	TIM1_CH3	TIM1_CH4	TIM1_CH1N	TIM1_CH1	TIM1_CH2N	TIM1_CH4N	TIM1_CH3N	TIM1_CH2
PB6	TIM1_CH2N	TIM1_CH1N	TIM1_CH3N	TIM1_CH4	TIM1_CH3	TIM1_CH2	TIM1_CH1	TIM1_CH4N
PB7	TIM1_CH2	TIM1_CH2N	TIM1_CH4	TIM1_CH3	TIM1_CH3N	TIM1_CH1	TIM1_CH1N	TIM1_CH4N
PB8	TIM1_CH1N	TIM1_CH3N	TIM1_CH3	TIM1_CH2	TIM1_CH1	TIM1_BKIN3	TIM13_CH1	TIM1_CH2N
PB9	TIM1_CH1	TIM1_CH1N	TIM1_CH3N	TIM1_CH4	TIM1_CH4N	TIM1_CH3	TIM14_CH1	TIM1_CH2

Table 8 IO ports used by comparators

	INP0	INP1	INP2	INP3	INM0	INM1	INM2	OUT
COMP1	PA3	PA5	PA6	PB0	PA4	PA7	PA8	PA1/PA11/PA13
COMP2	PB0	PB2	PA8	PA9	PA4	PA7	PB1	PA2/PA12/PA14

Table 9 IO ports used by OPs

	INP	INM	OUT
OP1	PA6	PA7	PB0
OP2	PA3	PA4	PA5

4. Electrical Characteristics

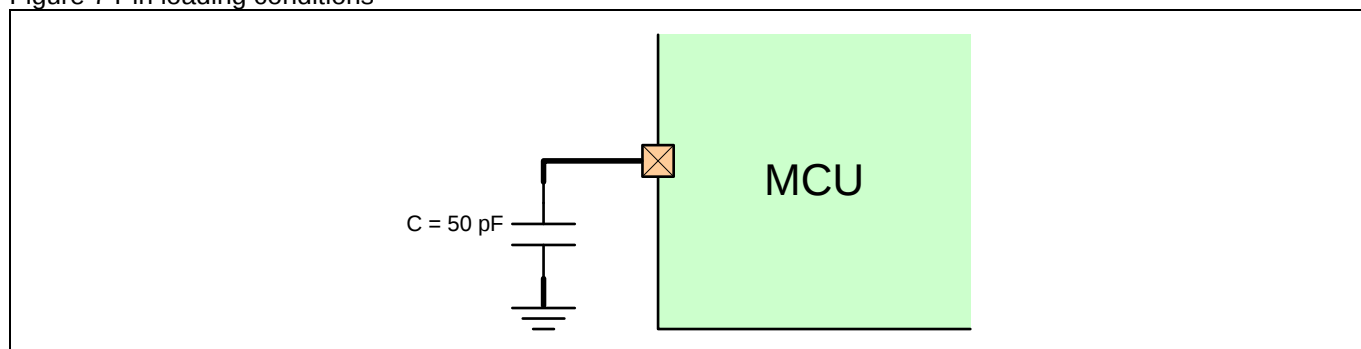
4.1. Test Condition

Unless otherwise specified, all voltages are referenced to VSS.

4.1.1. Load Capacitor

The loading conditions used for pin parameter measurement are shown in the figure below.

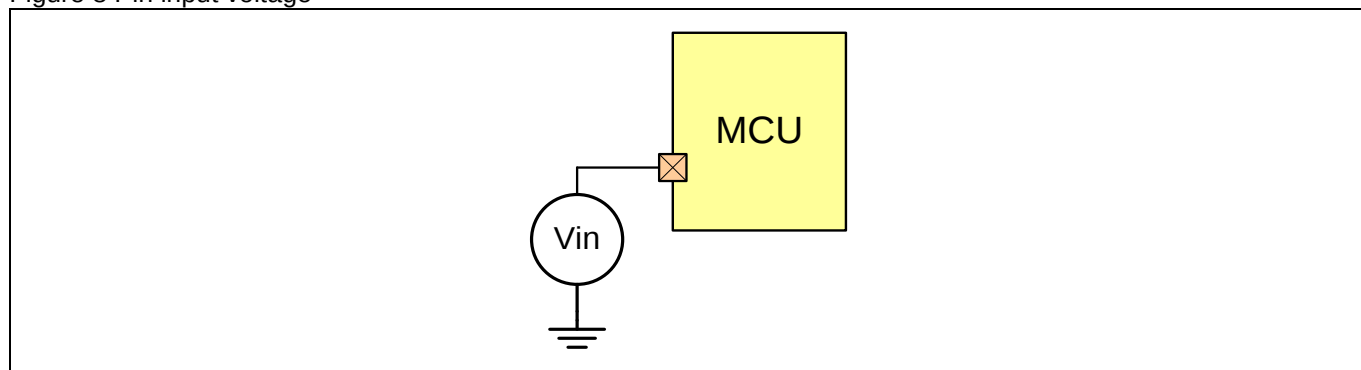
Figure 7 Pin loading conditions



4.1.2. Pin Input Voltage

The measurement method for pin input voltage is shown in the figure below.

Figure 8 Pin input voltage



4.1.3. Power Scheme

The application scheme of MDF151 is shown in the figure below.

Figure 9: MDF151 VIN > 13V Application Scheme

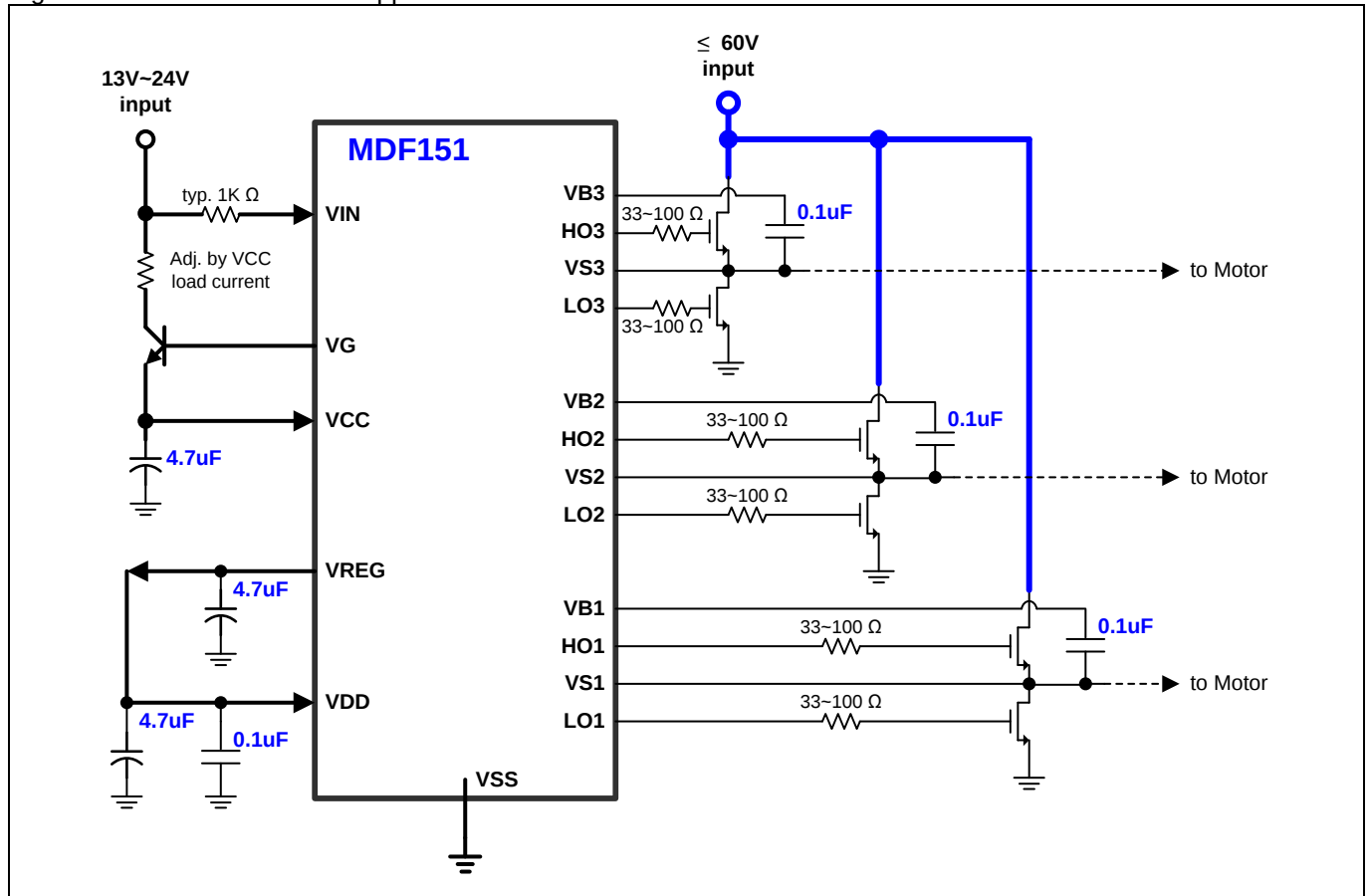
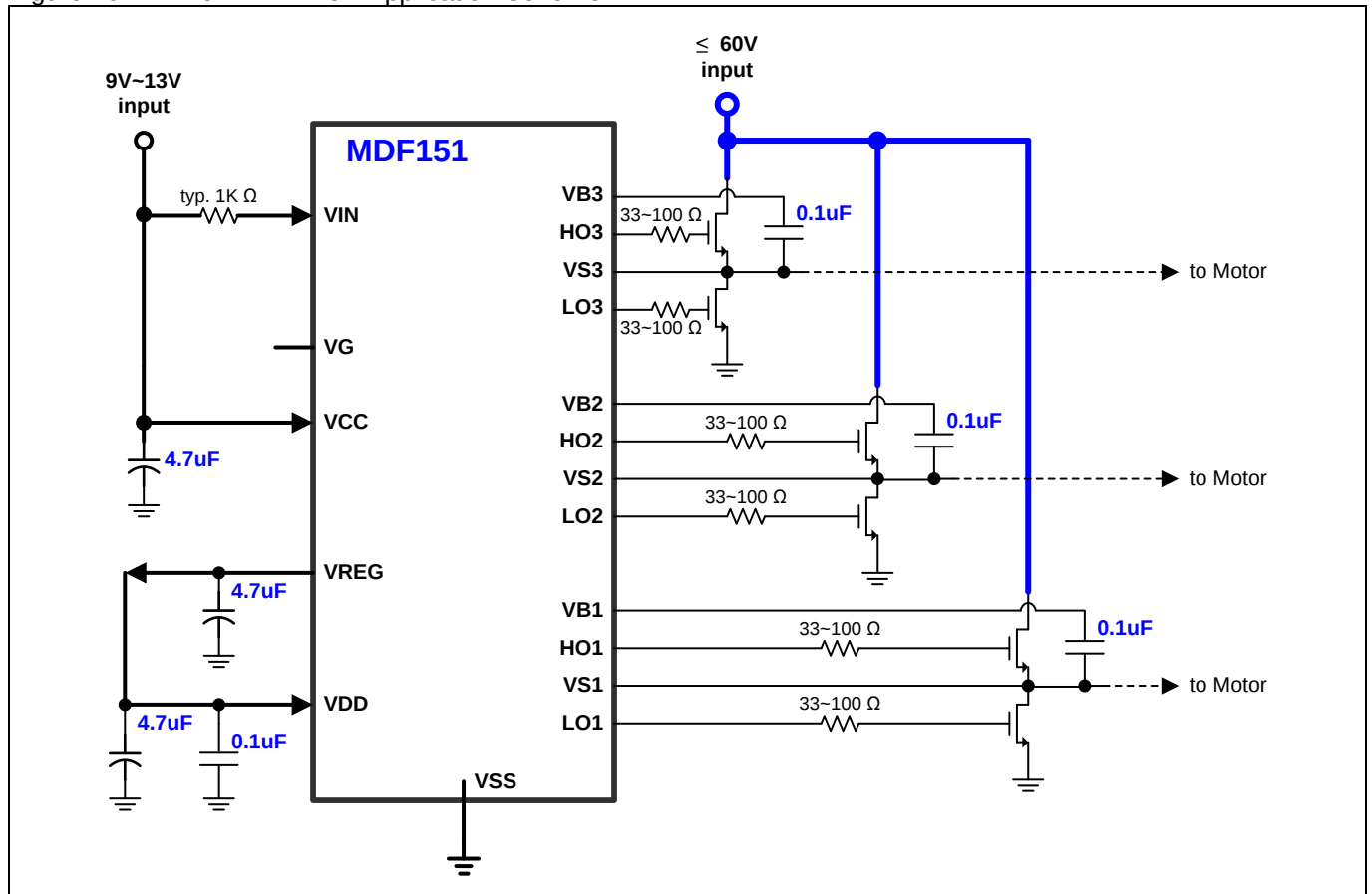


Figure 10 MDF151 VIN < 13V Application Scheme



4.2. Absolute Maximum Ratings

If the load applied to the device exceeds the values specified in the "Absolute Maximum Ratings" table (Table 10), it may result in permanent damage to the device. The maximum load values provided are only the limits that the device can withstand, and it does not imply flawless functional operation under these conditions. Prolonged operation of the device at maximum values can affect its reliability.

Table 10 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
LDO absolute maximum ratings				
VIN	LDO and gate driver Main Supply Voltage	-0.3	29	V
VCC	12V LDO Output Voltage	-0.3	17	V
VG	Low side Power Supply Bias Voltage	-0.3	25	
VREG	5V LDO Output Voltage	-0.3	5.5	V
θ_{JA}	LQFP48 Thermistor		21	°C/W
	QFN40 Thermistor		29	
	QFN32 Thermistor		35	
TJ	Junction Temperature	-40	125	°C
Gate driver absolute maximum rating				
VB1,VB2,VB3	High side bootstrap power supply	-0.3	150	V
VS1,VS2,VS3	High side (floating) common voltage	VB-17	VB+0.3	V
HO1,HO2,HO3	High side output voltage	VS-0.3	VB+0.3	V
LO1,LO2,LO3	Low side output voltage	-0.3	VCC+0.3	V
MCU absolute maximum ratings				
VDD-VSS ⁽¹⁾	External main supply voltage	-0.3	5.8	V
VIN ⁽²⁾	Input voltage on other pins	-0.3	5.8	
IVDD ⁽¹⁾	Total current through the VDD power line (source)		+60	mA
IVSS ⁽¹⁾	Total current through the VSS ground line (sink)		+60	
IO	Output sourcing current on any I/O and control pins		+20	
	Output sinking current on any I/O and control pins		-20	
IINJ (PIN) ⁽³⁾⁽⁴⁾	Injection current on the NRST pin		±5	
ΣIINJ (PIN) ⁽³⁾⁽⁵⁾	Injection current on other pins		±10	

- 1) All power (VDD) and ground (VSS) pins must always be connected to an external power supply within the allowed range.
- 2) The input voltage on pins must always comply with the range of VIN. Refer to the table below for information on the allowed maximum injection current values.
- 3) Forward/reverse injection current can interfere with the analog performance of the device.
- 4) When VIN > VDD, forward injection current is generated; when VIN < VSS, reverse injection current is generated.
- 5) When multiple inputs have injection currents simultaneously, the maximum value of ΣIINJ(PIN) is equal to the absolute sum of the forward injection current and the reverse injection current (instantaneous values).

4.3. 12V/5V LDO Operating Conditions

4.3.1. 12V LDO General Operating Conditions

$V_{IN}=21V$, $C_{IN}=C_{OUT}=4.7\mu F$, $T_J=25^{\circ}C$, unless otherwise specified.

Table 11 12V LDO characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{IN}	Power supply voltage			21	24	V
V_{CC}	12V LDO Output Voltage			12		V
I_{max1}	Maximum output current			300		mA

4.3.2. 5V LDO Electrical characteristics

$V_{CC}=12V$, $C_{IN}=C_{OUT}=4.7\mu F$, $T_J=25^{\circ}C$, Unless otherwise specified

Table 12 5V LDO characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{REG}	5V Output Power Supply	Unloaded	4.9	5.0	5.1	V
ΔV_{LINE}	Linear Regulation	$V_{CC} = 8\sim 15V$			10	mV
ΔV_{LOAD}	Load Regulation	$I_{LOAD} = 0\sim 60mA$		0.5	1.5	%
I_{SHORT}	Short Circuit Current	$V_{REG} = 0V$		50		mA
V_{DROP}	Difference Voltage	$I_{OUT}=30mA$, $\Delta V_{OUT}= 2\%$		250		mV
I_{LIMIT}	Maximum Output Current			110		mA

4.4. Gate driver working conditions

Table 13 Gate driver operating conditions

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
VS1,VS2,VS3	High side (floating) common voltage		-6		150	V
VB1,VB2,VB3	High side bootstrap power supply			VS+12	VS+15	V

4.4.1. Gate driver electrical characteristicsTable 14 Gate driver characteristics
(TA=25°C,VCC=15V)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
ISTBY	Standby current	VIN=VCC, Lix=0		175		uA
ISTBY1	High side Quiescent Current	Hlx=0		30		uA
VHOH1,2,3	High side Output High Level	Difference from VB, Io+=10mA			140	mV
VHOL1,2,3	High side Output High/Low Level	Difference from VB, Io-=10mA			70	mV
VLOH1,2,3	Low side Output High Level	Difference from VB, Io+=10mA			140	mV
VL0L1,2,3	Low side Output High/Low Level	Difference from VB, Io-=10mA			70	mV
VCCUV+ VCCUV-	VCC Undervoltage Protection Voltage			4.3		V
	VCC Undervoltage Protection Voltage			4.1		V
VBSUV+ VBSUV-	VB Undervoltage Protection Voltage			4.3		V
	VB Undervoltage Protection Voltage			4.1		V
IO+	Output Sink Current	VO=0V, VIN=High PW≤10μS		1.0		A
IO+	Output Sink Current	VO=15V, VIN=Low PW≤10μS		1.2		A
RBSD	Bootstrap Diode Internal Resistance	VCC=15V,VB=0V		40		Ω
THON	High side Output HO Rise Delay			200		ns
THOFF	High side Output HO Fall Delay			200		ns
THR	High side Output HO Rise Time			35		ns
THF	High side Output HO Fall Time			15		ns
TLOH	Low side Output LO Rise Delay			200		ns
TLOFF	Low side Output LO Fall Delay			200		ns
TLR	Low side Output LO Rise Time			35		ns
TLF	Low side Output LO Fall Time			15		ns
DT	Dead Time			100		ns
MT	Difference between Rise and Fall Dead Time			10		ns

Table 15 Truth Table of Driver Input/Output Logic (x=1,2,3)

Input		Output	
Hlx	Llx	HOx	LOx
Low	Low	Low	Low
Low	High	Low	High
High	Low	High	Low
High	High	Low	Low

Figure 5 Gate driver output waveform diagram

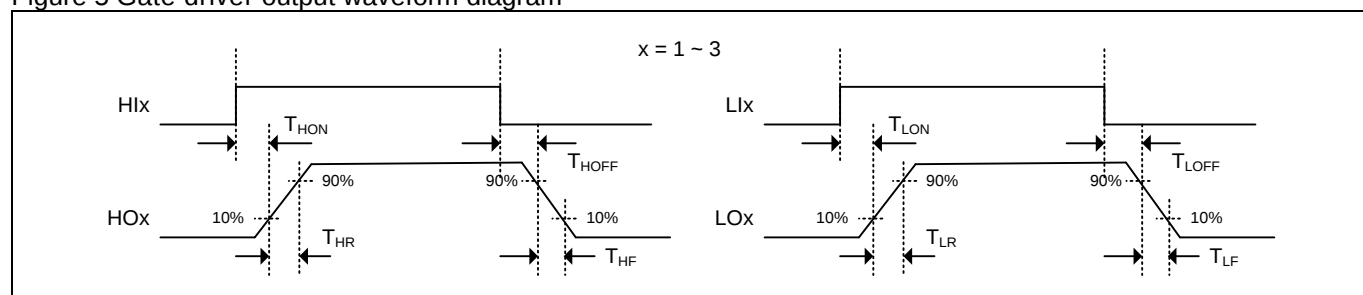
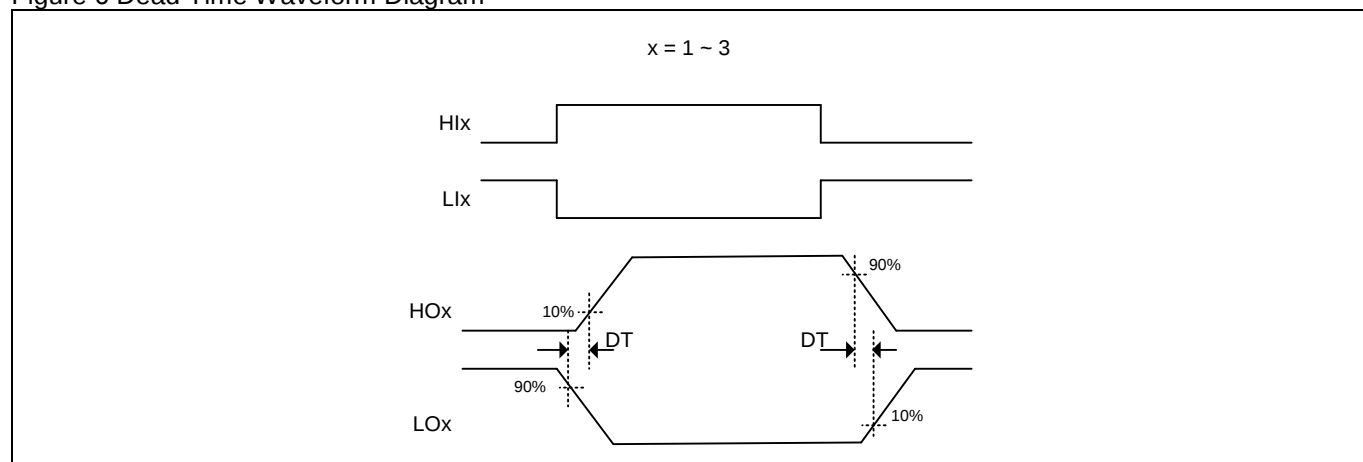


Figure 6 Dead Time Waveform Diagram



4.5. MCU Operating Conditions

Typical operating conditions of the MDF151 built-in MCU.

Table 16 General Working Conditions

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	60	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	-	60	
V_{DD}	Operating Voltage	-	2.5	-	5.5	V
T_A	Ambient temperature	VIN=24V , I_{LDO_OUT} =30mA	-40		105	°C
		VIN=12V , I_{LDO_OUT} =30mA	-40		105	°C

4.5.1. Power-on and power-off operating conditions

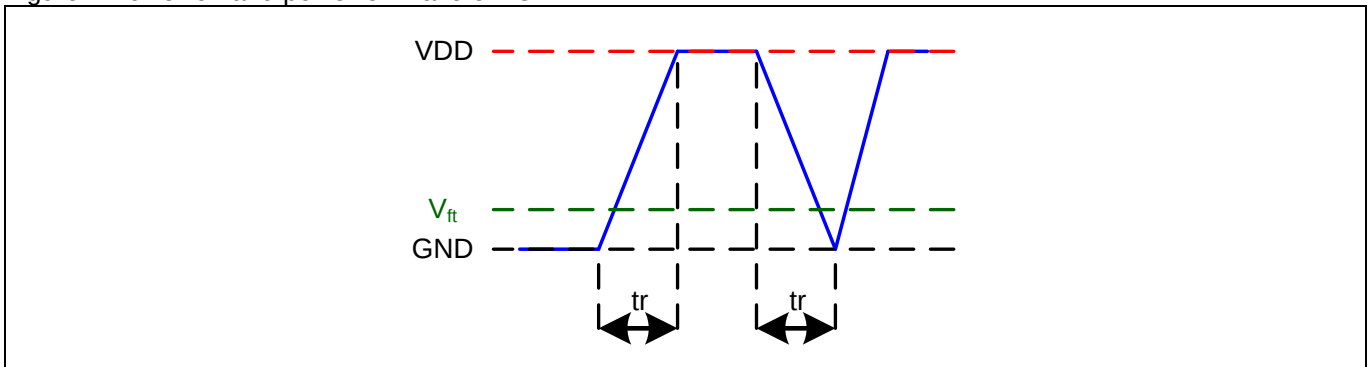
The parameters given in the table below were obtained from tests conducted under normal operating conditions.

Table 17 Power-on and Power-off Operating Conditions (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typical	Max
t_{VDD}	VDD rise time t_r	300	-	50000	us
	VDD fall time t_f	300	-	50000	
V_{ft}	Power-down threshold voltage	0	-	-	mV

- 1) Based on the overall assessment, this chip was not tested in production.
- 2) The on-chip VDD waveform during power loss should follow the t_r and t_f phases, as shown in the figure below.
- 3) The chip is powered on from 0V to ensure reliable power-on.

Figure 7 Power-on and power-off waveforms



4.5.2. Embedded Reset and Power Control Block Characteristics

The parameters given in the table below are derived from tests performed under the listed ambient temperature and V_{DD} supply voltage according to the general operating conditions table.

Table 18 Embedded reset and power control block characteristics ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{PVD}	Level selection for programmable voltage detector	PLS[3:0]=0010 (rising edge)	-	2.4	-	V
		PLS[3:0]=0010 (Falling edge)	-	2.3	-	
		PLS[3:0]=0011 (rising edge)	-	2.7	-	
		PLS[3:0]=0011 (Falling edge)	-	2.6	-	
		PLS[3:0]=0100 (rising edge)	-	3.0	-	
		PLS[3:0]=0100 (Falling edge)	-	2.9	-	
		PLS[3:0]=0101 (rising edge)	-	3.3	-	
		PLS[3:0]=0101 (Falling edge)	-	3.2	-	
		PLS[3:0]=0110 (rising edge)	-	3.6	-	
		PLS[3:0]=0110 (Falling edge)	-	3.5	-	
		PLS[3:0]=0111 (rising edge)	-	3.9	-	
		PLS[3:0]=0111 (Falling edge)	-	3.8	-	
		PLS[3:0]=1000 (rising edge)	-	4.2	-	
		PLS[3:0]=1000 (Falling edge)	-	4.1	-	
		PLS[3:0]=1001 (rising edge)	-	4.5	-	
		PLS[3:0]=1001 (Falling edge)	-	4.4	-	
		PLS[3:0]=1010 (rising edge)	-	4.8	-	
		PLS[3:0]=1010 (Falling edge)	-	4.7	-	
V_{POR}	Power-on reset threshold	-	-	2.2	-	V
$V_{hyst_POR/PDR}$	POR/PDR hysteresis	-	-	60	-	mV
$T_{RSTTEMPO}^{(2)}$	Reset duration	-	-	1.84	-	ms

1) Derived from comprehensive evaluation, not tested in production.

2) Reset Duration: Time from POR release to the execution of the user's first application code.

4.5.3. Built-in Reference Voltage

The parameters given in the table below are derived from tests under the listed ambient temperature and V_{DD} supply voltage according to the General Operating Conditions table.

Table 19 Built-in reference voltage

Symbol	Parameter	Condition	Min	Typical	Max	Unit
$V_{REFINT}^{(1)}$	Built-in reference voltage	$T_A = 25^\circ\text{C}$	1.14	1.2	1.26	V
$T_{s_vrefint}$	Sampling and Hold Time of ADC when reading Internal Reference Voltage	-	-	11.8	-	us

Current Consumption

Power supply current consumption is a comprehensive indicator of various parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin switching speed, program location in memory, and executed code.

Current consumption

The microcontroller is under the following conditions: All I/O pins are in input mode and connected to a quiescent level (VDD or VSS). All peripherals are disabled unless otherwise specified. Flash access time is adjusted to the fHCLK frequency (0 wait cycles for fHCLK 0–30 MHz, 2 wait cycles for fHCLK 30–60 MHz). Instruction prefetching is enabled. When peripherals are enabled: fHCLK = fPCLK 1.

Note: Instruction prefetching must be set before setting the clock and bus divider.

Table 20 Typical current consumption in operating mode

Symbol	Parameter	Condition	f _{HCLK} (Hz) (1)	Typical All peripherals enabled				Typical All peripherals disabled				Unit
				-40°C	25°C	85°C	105°C	-40°C	25°C	85°C	105°C	
I _{DD}	Supply current in sleep mode	Internal clock	60MHz	8.44	8.61	8.78	8.80	7.00	7.08	7.27	7.35	mA
			30MHz	5.29	5.33	5.38	5.41	4.58	4.61	4.67	4.71	
			15MHz	3.42	3.41	3.43	3.45	3.05	3.02	3.05	3.07	
			7.5MHz	2.44	2.40	2.41	2.42	2.25	2.20	2.21	2.22	
			40KHz ⁽²⁾	1.10	1.02	1.00	1.01	1.09	1.00	0.98	0.99	

- 1) The HCLK frequency is the AHB clock obtained by dividing the HSI 60MHz clock.
- 2) The LSI clock is set to 40KHz as the system clock, with the HSI turned off.

Table 21 Typical current consumption in sleep mode

Symbol	Parameter	Condition	f _{HCLK} (Hz) (1)	Typical All peripherals enabled				Typical All peripherals disabled				Unit
				-40°C	25°C	85°C	105°C	-40°C	25°C	85°C	105°C	
I _{DD}	Supply current in sleep mode	Internal clock	60MHz	3.55	3.52	3.53	3.54	2.31	2.25	2.25	2.26	mA
			30MHz	2.51	2.46	2.46	2.47	1.89	1.83	1.82	1.83	
			15MHz	1.96	1.90	1.89	1.90	1.65	1.58	1.57	1.58	
			7.5MHz	1.69	1.62	1.61	1.61	1.54	1.46	1.45	1.46	
			40KHz ⁽²⁾	1.08	1.00	0.99	1.00	1.08	1.00	0.99	1.00	

- 1) The HCLK frequency is obtained by dividing the HSI by 60MHz to get the AHB clock.
- 2) The LSI clock is set to 40kHz as the system clock; at this time, HSI is turned off.

Table 22 Typical current consumption in stop mode

Symbol	Parameter	Condition	Typical				Unit
			-40°C	25°C	85°C	105°C	
I _{DD} ⁽¹⁾	Supply current in stop mode	V _{DD} =3.3V After resetting, it enters stop mode.	113.3	106.8	111.3	118.4	μA

- 1) I/O status is analog input

Built-in Peripheral Current Consumption

The current consumption of the built-in peripherals is shown in Table 21. The MCU operates under the following conditions:

All I/O pins are in input mode and connected to a static level (VDD or VSS).

All peripherals are off unless otherwise specified.

The values given are calculated from measured current consumption:

- All peripheral clocks are off
- Only one peripheral clock is on

Ambient temperature and VDD supply voltage conditions are shown in Table 10.

Table 23 Current consumption of built-in peripherals (1)

Symbol	Peripherals	bus	Typical	Unit
I _{DD}	GPIOB	AHB	0.30	uA/MHz
	GPIOA		0.31	
	HWDIV		0.88	
	DMA		0.86	
	TIM1	APB1	4.65	
	TIM2		3.72	
	ADC1		2.98	
	USART1		1.86	
	TIM14		1.61	
	TIM13		1.60	
	TIM6		1.29	
	COMP		0.51	
	SYSCFG		0.11	
	DBG		0.05	
	PWR		0.01	
	EXTI		0.01	
	IWDG		0.01	

3) $f_{HCLK} = 60\text{MHz}$, $f_{APB1} = f_{HCLK}$, The prescaler coefficients for each peripheral are set to the default values.

Low Power Mode Wake-up Time

The wake-up times listed in the table below were measured during the wake-up phase of the internal clock HSI. All times were measured under normal operating conditions, with ambient temperature and supply voltage within specified ranges.

Table 24 Low-power mode wake-up time

Symbol	Peripherals	Condition	Typical	Unit
$t_{WUSLEEP}$	Wake up from sleep mode	The system clock is HSI	1.5	μS
t_{WUSTOP}	Wake up from stop mode	The system clock is HSI	65	μS

4.5.4. Internal Clock Source Characteristics

The characteristics listed in the table below were measured under normal operating conditions, within the specified range of ambient temperature and power supply voltage.

High-speed internal (HSI) oscillator

Table 25 HSI Oscillator Characteristics (1)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
f_{HSI}	Frequency	-	-	60	-	MHz
ACC_{HSI}	HSI Oscillator Accuracy	$T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$	-2.5	-	2.5	%
		$T_A = -10^\circ\text{C} \sim 85^\circ\text{C}$	1.5	-	1.5	%
		$T_A = 25^\circ\text{C}$	-1	-	1	%
$t_{SU(HSI)}$	HSI Oscillator Startup Time	-	-	61	-	μS
$I_{DD(HSI)}$	HSI Oscillator Power Consumption	-	145.7	183.2	239.3	μA

1) Based on comprehensive evaluation, it was determined that the test was not conducted in production.

Low-speed internal (LSI) oscillator

Table 26 LSI Oscillator Characteristics (1)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
$f_{LSI}^{(2)}$	Frequency	$T_A = -40^{\circ}\text{C} \sim 105^{\circ}\text{C}$	20	40	80	KHz
$t_{SU(LSI)}^{(2)}$	LSI oscillator startup time	-	-	-	300	μS
$I_{DD(LSI)}^{(2)}$	LSI oscillator power consumption	-	-	0.34	-	μA

1) $V_{DD} = 3.3\text{V}$, unless otherwise specified

2) Based on comprehensive evaluation, this was not tested in production.

Memory characteristics

Table 27 Characteristics of FLASH Memory

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
t_{prog}	16-bit programming time	-	-	164	-	μS
	21-bit programming time		-	177	-	
t_{ERASE}	Page (1024 bytes) erase time	-	-	5.18	-	mS
t_{ME}	Whole erase time	-	-	50.98	-	mS

Table 27 Flash memory lifespan and data retention period (1)

Symbol	Parameter	Conditions	Min	Unit
N_{END}	Erasing/Write Cycles		2	10,000 times
T_{DR}	Data Retention	$T_A = 105^{\circ}\text{C}$	10	Year

1) Based on comprehensive evaluation, it was determined that the test was not conducted in production.

4.5.5. General Input/ Output Characteristics of GPIO Ports

Unless otherwise stated, the parameters listed in the table below are from experiments conducted under the conditions summarized in the table. All I/O ports are CMOS compatible.

Table 29 Static Characteristics of I/O (1)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{IL}	Input low-level voltage	3.3V CMOS port	-	-	0.8	V
V_{IL}	Input low-level voltage	5V CMOS port	-	-	0.3 * V_{DD}	V
V_{IH}	Input high-level voltage	3.3V CMOS port	2.0	-	-	V
V_{IH}	Input high-level voltage	5V CMOS port	0.7 * V_{DD}	-	-	V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis	3.3V	0.1 * V_{DD}	0.50	-	V
V_{hy}	I/O pin Schmitt trigger voltage hysteresis	5V	0.1 * V_{DD}	0.60	-	V
I_{ikg}	Input leakage current ⁽²⁾	3.3V	-1	-	1	μA
I_{ikg}	Input leakage current ⁽²⁾	5V	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor	3.3V $V_{IN} = V_{SS}$	50	60	75	k Ω
R_{PU}	Weak pull-up equivalent resistor	5V $V_{IN} = V_{SS}$	50	60	75	k Ω
R_{PD}	Weak pull-down equivalent resistor	3.3V $V_{IN} = V_{DD}$	50	60	75	k Ω
R_{PD}	Weak pull-down equivalent resistor	5V $V_{IN} = V_{DD}$	50	60	75	k Ω
C_{IO}	I/O pin capacitance	-	-	-	10	pF

1) Derived from comprehensive evaluation, not tested in production.

2) In case of a negative current back flow in an adjacent pin, the leakage current may exceed the maximum value.

Output drive current

The GPIOs (General Purpose Input/Output) can sink or source current up to $\pm 20\text{mA}$.

In user applications, the number of I/O pins must ensure that the drive current does not exceed the absolute maximum ratings given in section 4.2:

- The sum of all I/O ports' current drawn from V_{DD} , plus the MCU's maximum operating current drawn from V_{DD} , must not exceed the absolute maximum rated value I_{VDD} .
- The sum of all I/O ports' current sunk from V_{SS} , plus the MCU's maximum operating current sunk from V_{SS} , must not exceed the absolute maximum rated value I_{VSS} .

Output current

Unless specifically stated, the parameters listed in the table below were measured under conditions where the ambient temperature and V_{DD} power supply voltage comply with the conditions in table 12. All I/O ports are CMOS compatible.

Table 28 Output current characteristics ⁽¹⁾

Symbol	Parameter	Condition	Typical	Unit
V_{OL}	Output low current	$ I_{IO} = 6\text{mA}$, $V_{DD} = 3.3\text{V}$	0.15	V
V_{OH}	Output high current		3.0	
V_{OL}	Output low current	$ I_{IO} = 8\text{mA}$, $V_{DD} = 3.3\text{V}$	0.21	
V_{OH}	Output high current		2.98	
V_{OL}	Output low current	$ I_{IO} = 20\text{mA}$, $V_{DD} = 3.3\text{V}$	0.59	
V_{OH}	Output high current		2.31	

1) Derived from comprehensive evaluation, not tested in production.

Input/output AC characteristics

The definition and values of AC characteristics of input and output are provided in Figure 15 and Table 29.

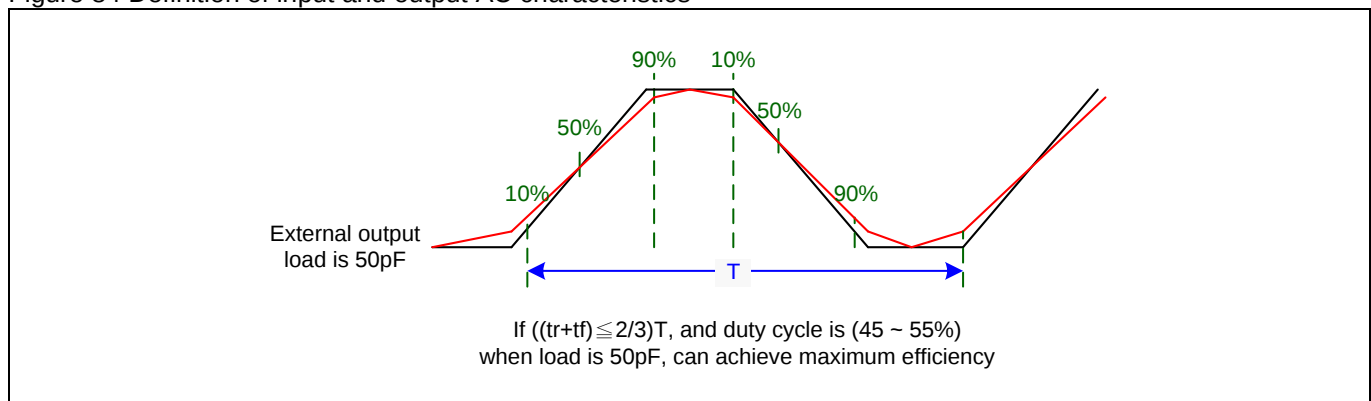
Unless otherwise specified, the parameters listed in the table are measured under the conditions of ambient temperature and supply voltage specified in the general operating conditions table.

Table 29 Input/output AC characteristics ⁽¹⁾

Symbol	Parameter	Condition	Typical	Unit
$t_{r(I/O)out}$	Output fall time	$C_L = 50\text{pF}$ $V_{DD} = 3.3\text{V}$	5.3	ns
$t_{r(I/O)out}$	Output rise time		5.8	ns

- 1) The maximum output frequency of IO is defined .
- 2) Guaranteed by design, not tested in production.

Figure 84 Definition of input and output AC characteristics



4.5.6. NRST Pin Characteristics

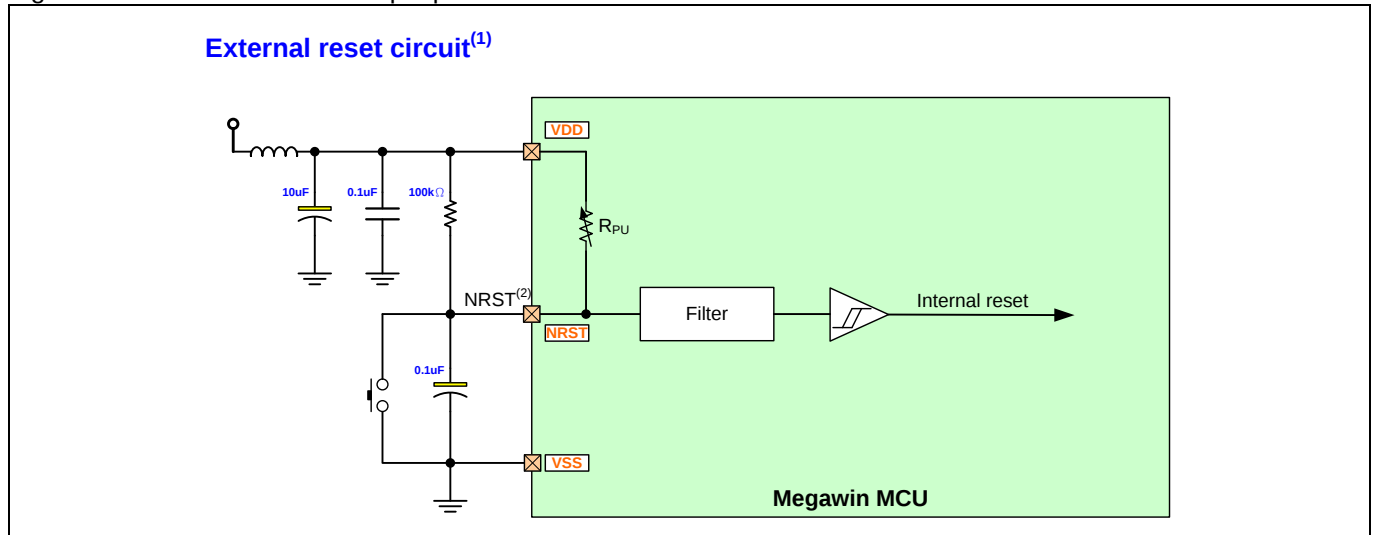
Unless otherwise stated, all parameters listed in the table below were measured at the ambient temperature and VDD power supply voltage specified in the table.

Table 30 NRST pin characteristics ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	VDD=3.3V	-	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage	VDD=3.3V	$0.7 * V_{DD}$	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	VDD=3.3V	-	0.50	-	V
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	50	60	75	k Ω
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	0.5	μ S
$V_{NF(NRST)}$	NRST input non-filtered pulse	-	0.7	-	-	μ S

1) Guaranteed by design, not tested in production.

Figure 9 Recommended NRST pin protection



1) The reset network is to prevent parasitic reset.

2) The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 30, otherwise the MCU cannot be reset.

4.5.7. Timer Characteristics

Table 31 TIMx ⁽¹⁾ characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer Resolution Time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 60MHz$	16.7	-	nS
f_{EXT}	External clock frequency for timers CH1 to CH4	-	0	-	MHz
		$f_{TIMxCLK} = 60MHz$	-	30	
Re_{TIM}	Timer resolution	-	-	16/32	Bit
$t_{COUNTER}$	Clock cycle of 16-bit counter	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 60MHz$	0.0167	1092.3	μ S
t_{MAX_COUNT}	Maximum possible counting period for of 16-bit counter (TIM_PSC adjustable)	-	-	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 60MHz$	-	71.6	S
t_{MAX_IN}	Maximum input frequency for TIM	$f_{HCLK} = 60MHz$	-	60	MHz

1) Guaranteed by design, not tested in production.

4.5.8. Communication Interfaces

USART characteristics

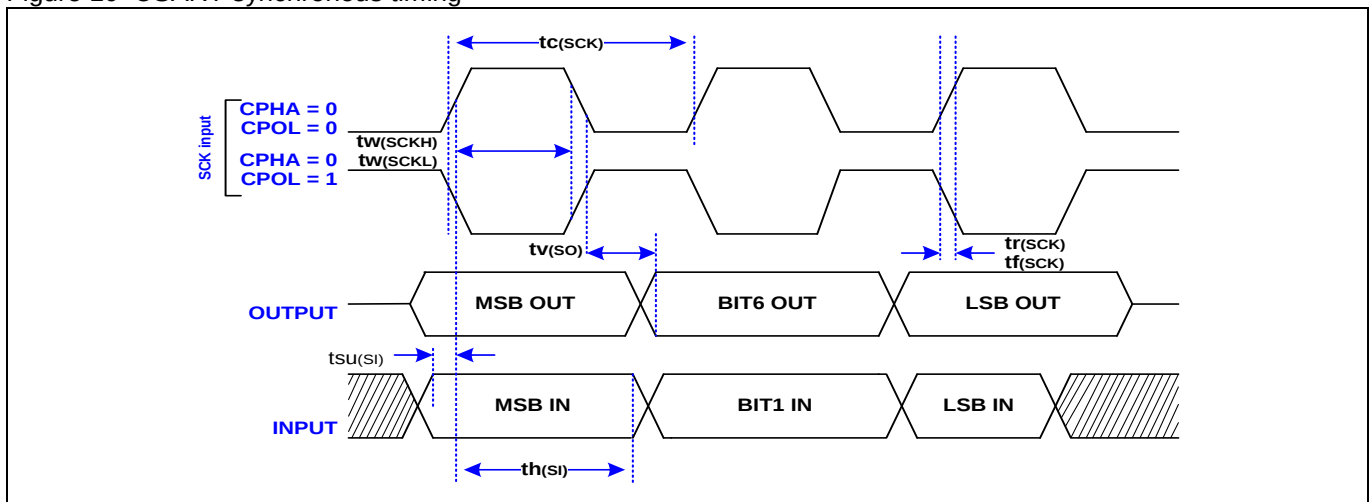
Unless otherwise stated, all parameters in Table 32 are measurements taken under the ambient temperature, fPCLK1 frequency, and VDD power supply voltage conditions specified in the table.

Table 32 USART synchronous mode characteristics ⁽¹⁾

Symbol	Parameter	Condition	Min	Max	Unit
$f_{SCK1}/t_{c(SCK)}$	SPI clock frequency	Master mode	-	7.5	MHz
		Slave mode	-	7.5	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	6	ns
$t_{f(SCK)}$	SPI clock fall time	Load capacitance: C = 15pF	-	6	ns
$t_{w(SCKH)}^{(1)}$	SCK high time	-	$t_{c(SCK)}/2 - 6$	$t_{c(SCK)}/2 + 6$	nS
$t_{w(SCKL)}^{(1)}$	SCK low time	-	$t_{c(SCK)}/2 - 6$	$t_{c(SCK)}/2 + 6$	nS
$t_{su(MI)}^{(1)}$	Data Input Setup Time	Master mode, $f_{PCLK} = 60\text{MHz}$, prescaler = 8, high-speed mode	5	-	nS
$t_{su(SI)}^{(1)}$		Slave mode	5	-	nS
$t_{h(MI)}^{(1)}$	Data input hold time	Master mode, $f_{PCLK} = 60\text{MHz}$, prescaler = 8, high-speed mode	5	-	nS
$t_{h(SI)}^{(1)}$		Slave mode	5	-	nS
$t_{v(MO)}^{(1)}$	Data output valid time	Master mode (after enabling the edge)	-	10	nS
$t_{v(SO)}^{(1)}$	Data output valid time	Slave mode (after enabling the edge)	-	26	nS

- 1) Guaranteed by design, not tested in production.
- 2) The minimum value represents the minimum time for driving the output, while the maximum value represents the maximum time for correctly acquiring data.
- 3) The minimum value represents the minimum time for disabling the output, while the maximum value represents the maximum time for putting the data line in a high-impedance state.

Figure 10 USART synchronous timing



4.5.9. ADC Characteristics

Unless otherwise specified, the parameters in the following table are measured using the ambient temperature, f_{PCLK1} frequency, and V_{DD} power supply voltage in accordance with the conditions specified in the general operating conditions table.

Table 33 ADC characteristics ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{DD}	Supply voltage	-	2.5		5.5	V
f_{ADC}	ADC clock frequency	$V_{DD} \geq 2.5V$	-	-	15	MHz
f_s	Sampling rate	12bits; $V_{DD} \geq 2.8V$	-	-	1	MHz
		12bits; $V_{DD} < 2.8V$			400	KHz
f_{TRIG}	External trigger frequency ⁽²⁾	12bits; $f_{ADC} = 15MHz$	-	-	1	MHz
		12bits	-	-	15	1/ f_{ADC}
V_{AIN}	Conversion voltage range	$V_{DD} \geq 2.5V$	0	-	V_{DD}	V
R_{AIN}	External input impedance	-	See the formula below			k Ω
R_{ADC}	Sampling switch resistance	-	-	-	1.5	k Ω
C_{ADC}	Internal sampling and holding capacitance	-	-	-	5	pF
t_{STAB}	Power-up time	-	-	-	10	μs
t_{lat}	Injection-trigger conversion delay	-	-	-	512	1/ f_{ADC}
t_{latr}	Regular-trigger conversion delay	-	-	-	512	1/ f_{ADC}
t_s	Sampling time	$f_{ADC} = 15MHz$	0.167	-	16.03	μs
		-	-	-	-	1/ f_{ADC}
t_{CONV}	Total conversion time (including sampling time)	12bits; $f_{ADC} = 15MHz$	1	-	16.87	μs
		12bits	-			1/ f_{ADC}
ENOB	Effective number of bits	12bits; $V_{DD} \geq 3.3V$; $f_{ADC} = 15MHz$	-	10.9	-	bit

1)Guaranteed by design, not tested in production.

2)For external triggering, a delay of 1/ f_{ADC} must be added to the timing.

Input Impedance Table

$$R_{AIN} < \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The above formula is used to determine the maximum external impedance to ensure that the error is less than 1/4 LSB. Here, $n = 12$ (representing 12-bit resolution) and it is measured at $f_{ADC} = 15MHz$.

Table 34 Maximum R_{AIN} at $f_{ADC} = 15MHz$ ⁽¹⁾

Table 35 $f_{ADC}=15\text{MHz}$ ⁽¹⁾ when Maximum R_{AIN}

Ts (cycle)	ts (μS)	Maximum R_{AIN} (kΩ)
2.5	0.167	1.9
3.5	0.233	3.3
4.5	0.300	4.7
5.5	0.367	6.1
6.5	0.433	7.4
7.5	0.500	8.8
8.5	0.567	10.2
14.5	0.967	18.4
29.5	1.967	39.0
42.5	2.833	56.9
56.5	3.767	76.1
72.5	4.833	98.1
240.5	16.033	328.9

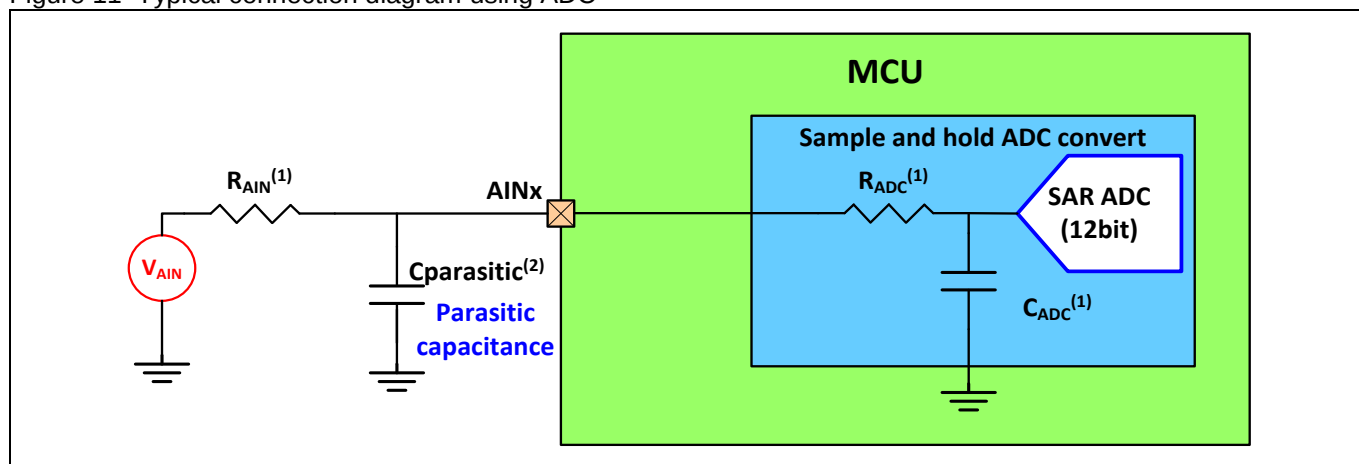
Guaranteed by design, not tested in production.

Table 36 ADC static parameter ⁽¹⁾ ⁽²⁾

Symbol	Parameter	Condition	Typical	Unit
ET	Overall error	$f_{PCLK1} = 60\text{MHz}$, $f_{ADC} = 15\text{MHz}$, $R_{AIN} < 0.1\text{ k}\Omega$, $V_{DD} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$	-6/+11	LSB
EO	Offset error		-4.8/+10.1	
EG	Gain error		-1.2/+7.1	
ED	Differential linearity error		-0.9/1.5	
EL	Integral linearity error		-4/+4.2	

- 1) The relationship between ADC accuracy and reverse injection current: It is necessary to avoid injecting reverse current into any standard analog input pin, as it significantly degrades the accuracy of the conversion performed on another analog input pin. It is recommended to add a Schottky diode between the pin and ground on standard analog pins where reverse injection current may occur.
- 2) Derived from comprehensive evaluation, not tested in production.

Figure 11 Typical connection diagram using ADC



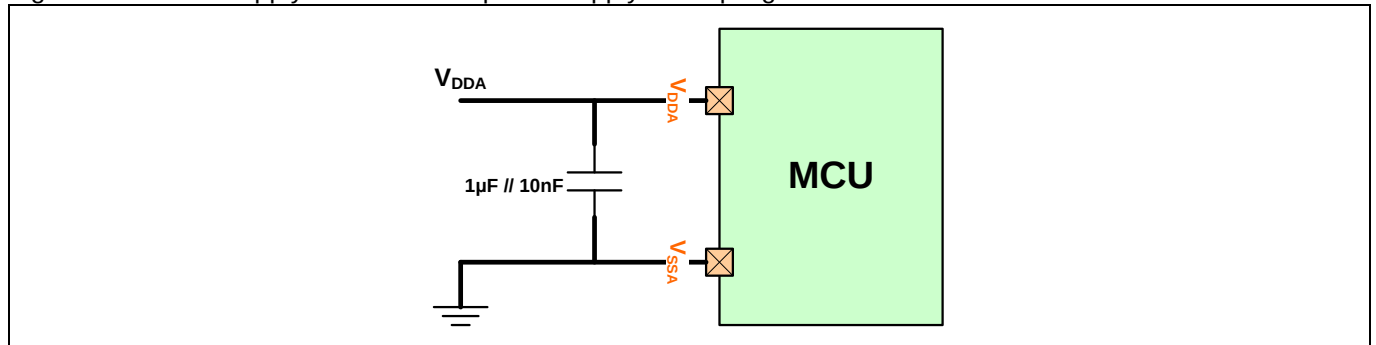
1) Refer to Table 35/36 for the values of R_{AIN} , R_{ADC} and C_{ADC} .

2) Parasitic represents the capacitance between the PCB (which is dependent on soldering and PCB layout quality) and the solder pads (approximately 7pF). A high value of Parasitic will degrade the accuracy of the conversion. To address this issue, it is recommended to reduce f_{ADC} .

PCB design recommendations

The decoupling of the power supply must be connected as shown in the figure below. The 10 nF capacitor depicted in the figure must be a ceramic capacitor and should be placed as close as possible to the MCU chip.

Figure 128 Power supply and reference power supply decoupling circuit



4.5.10. Temperature Sensor Characteristics

Table 37 Temperature sensor characteristics ⁽³⁾

Symbol	Parameter	Conditions	Min	Typical	Max
$T_L^{(1)}$	Linearity of V_{SENSE} relative to temperature	-	± 5	-	$^{\circ}\text{C}$
$\text{Avg_Slope}^{(1)}$	Average slope	-	-3.89	-	$\text{mV}/^{\circ}\text{C}$
$V_{25^{\circ}\text{C}}^{(1)}$	Voltage at 25°C	-	1.289	-	V
$t_{\text{START}}^{(2)}$	Settling time	-	1	-	μS
$t_{\text{S_temp}}^{(2)}$	ADC sampling time when reading temperature	-	11.8	-	μS

- 1) Derived from comprehensive evaluation, not tested in production.
- 2) Guaranteed by design, not tested in production.
- 3) Temperature formula: $T_{\text{sensor}} = 25 + (\text{ADCvalue} * v_{\text{dd}} - \text{offset} * 3300) / (4096 * \text{Avg_Slope})$, where the offset is stored in the lower 12 bits of address 0x1FFFF7F6.

4.5.11. Comparator Characteristics

Table 38 Comparator characteristics

Comparator characteristics						
Symbol	Parameter	Register configuration	Min	Typical	Max	Unit
V_{IN}	Input Voltage	-	0.6	-	$V_{\text{DD}}-1$	V
t_{HYST}	Hysteresis	00(hysteresis) , high power	-	0	-	mV
		00(hysteresis) , low power	-	0	-	mV
		01(hysteresis) , high power	15	22	43	mV
		01(hysteresis) , low power	13	15	23	mV
		10(hysteresis) , high power	32	45	92	mV
		10(hysteresis) , low power	25.2	32	46.7	mV
		11(hysteresis) , high power	55	85	182	mV
		11(hysteresis) , low power	25.5	60	83.9	mV
V_{OFFSET}	Offset voltage	-	-	± 6	± 10.4	mV
t_{DELAY}	Propagation Delay ⁽¹⁾	00 (high power)	3.7	10.7	43	ns

Comparator characteristics						
Symbol	Parameter	Register configuration	Min	Typical	Max	Unit
		01 (medium power)	10.5	34.9	83	ns
		10 (low power)	13.8	49	114	ns
		11 (ultra-low power)	22.2	86	194.5	ns
		00 (high power)	6.5	45	205.4	uA
I _q	Average operating current	01 (medium power)	3.3	21.7	81.3	uA
		10 (low power)	2.6	15.3	59.6	uA
		11 (ultra-low power)	1.7	8.8	35.3	uA

1) Time difference between 50% output transition and input transition.

4.5.12. Operational Amplifier Characteristics

Table 39 Operational amplifier characteristics

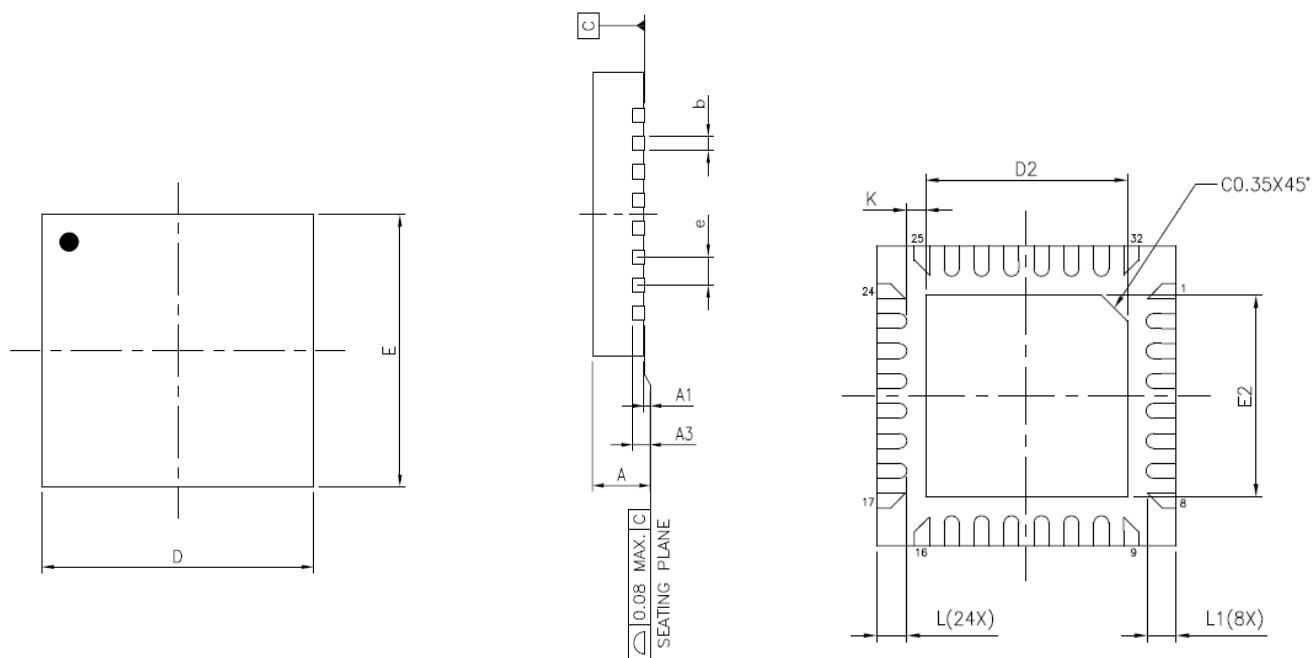
Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V _{DD}	Supply voltage	-	2.5	-	5.5	V
V _{OFFSET}	Input bias voltage	Common mode input 1/2 * V _{DD}	-6	-	6	mV
I _{LOAD}	Drive current	Drive current (sinking current) (V _{DD} =5V V _{OUT} =1V)	-	-	15	mA
C _{LOAD}	Capacitive load	-	-	-	30	pF
CMRR	Common mode rejection ratio	-	-	80	-	dB
PSRR	Power supply rejection ratio	-	-	80	-	dB
GBW	Gain-bandwidth product	-	-	12	-	MHz
SR	Slew rate	-	-	7	-	V/us
GOL	Open-loop gain	-	90	110	120	dB

1)Guaranteed by design, not tested in production.

5. Package Dimensions

5.1. Package QFN32 (4mm X 4mm X 0.85mm) Dimension

Figure 13 QFN-32 (4mm X 4mm X 0.85mm)

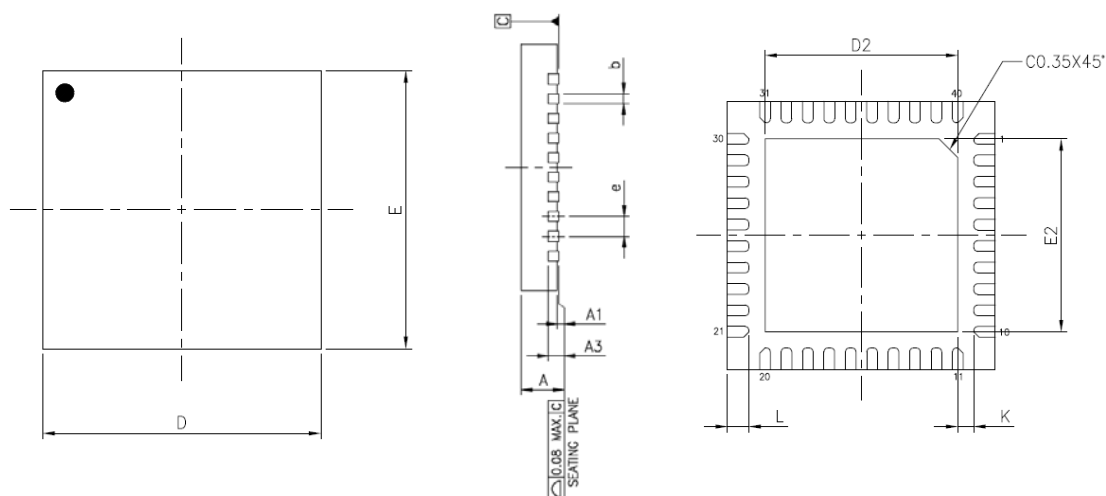


Unit	mm		
JEDEC	N/A		
Symbols	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.40 BSC		
L	0.25	0.30	0.35
L1	0.23	0.28	0.33
K	0.20	----	----
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75

This is the dimension for reference ,see the data sheet for the exact dimension for each model of IC.

5.2. Package QFN40 (5mm X 5mm X 0.75mm) Dimension

Figure 14 QFN-40 (5mm X 5mm X 0.75mm)



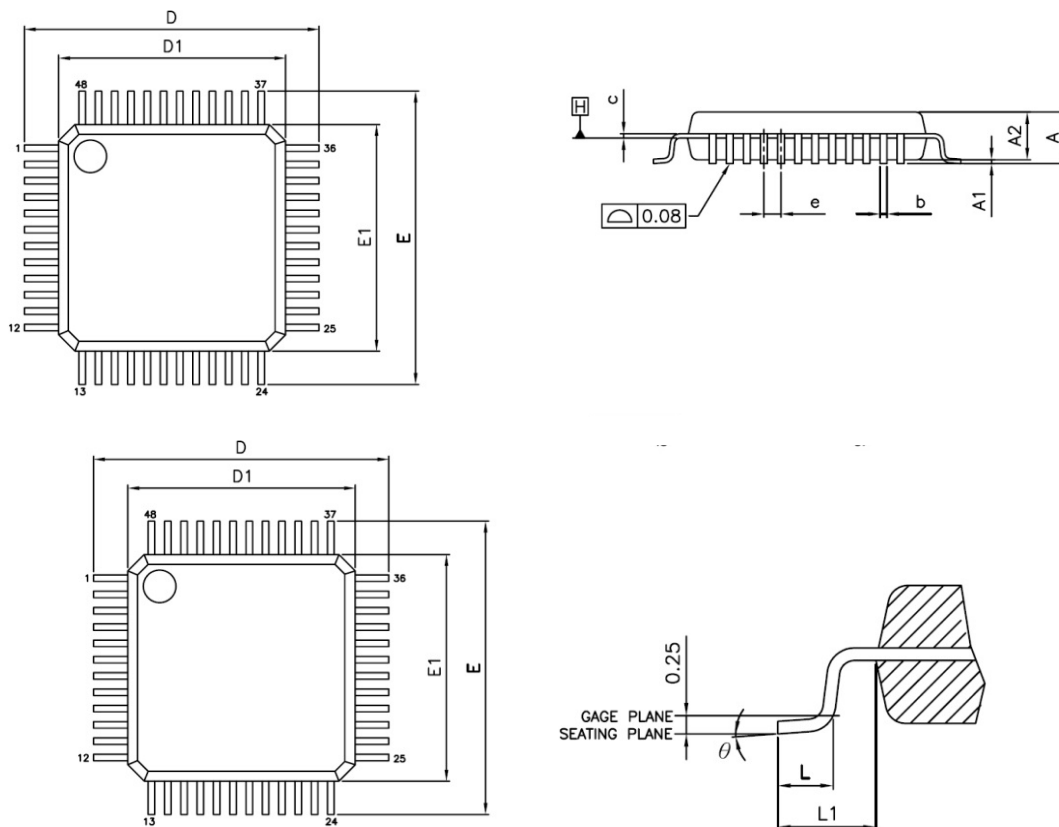
Unit	mm		
JEDEC	MO-220		
PKG	WQFN(X540)		
SYMBOLS	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.2	----	---

PAD SIZE	D2			E2			LEAD FINISH	
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF
153X15 MIL	3.25	3.30	3.35	3.25	3.30	3.35	V	X

This is the dimension for reference, see the data sheet for the exact dimension for each model of IC.

5.3. Package LQFP48 (7mm X 7mm X 1.4mm) Dimension

Figure 15 LQFP-48 (7mm X 7mm X 1.4mm)



Unit	mm		
Symbols	Min.	Nom.	Max.
A	---	---	1.60
A1	0.05	---	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	---	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

This is the dimension for reference ,see the data sheet for the exact dimension for each model of IC.

6. Revision History

Table 40 Revision history

Rev	Descriptions	Date
V0.1	1. Initial Version	2025/06/01

7. Disclaimer

Herein, Megawin stands for "***Megawin Technology Co., Ltd.***"

Life Support — This product is not designed for use in medical, life-saving or life-sustaining applications, or systems where malfunction of this product can reasonably be expected to result in personal injury. Customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify Megawin for any damages resulting from such improper use or sale.

Right to Make Changes — Megawin reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in mass production, relevant changes will be communicated via an Engineering Change Notification (ECN).