Register Document

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MG32F02A128
MG32F02U128
MG32F02A064
MG32F02U064
Register Definition Guide

Version 1.25

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List of Contents

1. Registers

1.1. IO Port Control Registers

IO Port Control	(IOP) General Purpose IO Port Control
Base Address :	0x41000000

1.1.1. PA output data register

PA_OUT	PA output data register		
Offset Address :	0x00	Reset Value :	0xFFFFFFFF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PA_OUT15	PA_OUT14	PA_OUT13	PA_OUT12	PA_OUT11	PA_OUT10	PA_OUT9	PA_OUT8
7	6	5	4	3	2	1	0
PA_OUT7	PA_OUT6	PA_OUT5	PA_OUT4	PA_OUT3	PA_OUT2	PA_OUT1	PA_OUT0

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0xFFFF
15	rw	PA_OUT15	IO pin PA15 output data bit.	0x01
14	rw	PA_OUT14	IO pin PA14 output data bit.	0x01
13	rw	PA_OUT13	IO pin PA13 output data bit.	0x01
12	rw	PA_OUT12	IO pin PA12 output data bit.	0x01
11	rw	PA_OUT11	IO pin PA11 output data bit.	0x01
10	rw	PA_OUT10	IO pin PA10 output data bit.	0x01
9	rw	PA_OUT9	IO pin PA9 output data bit.	0x01
8	rw	PA_OUT8	IO pin PA8 output data bit.	0x01
7	rw	PA_OUT7	IO pin PA7 output data bit.	0x01
6	rw	PA_OUT6	IO pin PA6 output data bit.	0x01
5	rw	PA_OUT5	IO pin PA5 output data bit.	0x01
4	rw	PA_OUT4	IO pin PA4 output data bit.	0x01
3	rw	PA_OUT3	IO pin PA3 output data bit.	0x01
2	rw	PA_OUT2	IO pin PA2 output data bit.	0x01
1	rw	PA_OUT1	IO pin PA1 output data bit.	0x01
0	rw	PA_OUT0	IO pin PA0 output data bit.	0x01

1.1.2. PA input data register

PA_IN	PA input data register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PA_IN15	PA_IN14	PA_IN13	PA_IN12	PA_IN11	PA_IN10	PA_IN9	PA_IN8
7	6	5	4	3	2	1	0
PA_IN7	PA_IN6	PA_IN5	PA_IN4	PA_IN3	PA_IN2	PA_IN1	PA_IN0

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	r	PA_IN15	IO pin PA15 input pin status.	0x00
14	r	PA_IN14	IO pin PA14 input pin status.	0x00
13	r	PA_IN13	IO pin PA13 input pin status.	0x00
12	r	PA_IN12	IO pin PA12 input pin status.	0x00

11	r	PA_IN11	IO pin PA11 input pin status.	0x00
10	r	PA_IN10	IO pin PA10 input pin status.	0x00
9	r	PA_IN9	IO pin PA9 input pin status.	0x00
8	r	PA_IN8	IO pin PA8 input pin status.	0x00
7	r	PA_IN7	IO pin PA7 input pin status.	0x00
6	r	PA_IN6	IO pin PA6 input pin status.	0x00
5	r	PA_IN5	IO pin PA5 input pin status.	0x00
4	r	PA_IN4	IO pin PA4 input pin status.	0x00
3	r	PA_IN3	IO pin PA3 input pin status.	0x00
2	r	PA_IN2	IO pin PA2 input pin status.	0x00
1	r	PA_IN1	IO pin PA1 input pin status.	0x00
0	r	PA_IN0	IO pin PA0 input pin status.	0x00

1.1.3. PA port set / clear register

PA_SC	PA port set / clear register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PA_CLR15	PA_CLR14	PA_CLR13	PA_CLR12	PA_CLR11	PA_CLR10	PA_CLR9	PA_CLR8
23	22	21	20	19	18	17	16
PA_CLR7	PA_CLR6	PA_CLR5	PA_CLR4	PA_CLR3	PA_CLR2	PA_CLR1	PA_CLR0
15	14	13	12	11	10	9	8
PA_SET15	PA_SET14	PA_SET13	PA_SET12	PA_SET11	PA_SET10	PA_SET9	PA_SET8
7	6	5	4	3	2	1	0
PA_SET7	PA_SET6	PA_SET5	PA_SET4	PA_SET3	PA_SET2	PA_SET1	PA_SET0

Bit	Attr	Bit Name	Description	Reset
31	w	PA_CLR15	IO pin PA15 clear data bit. This bit is no effect for writing 0.	0x00
30	w	PA_CLR14	IO pin PA14 clear data bit. This bit is no effect for writing 0.	0x00
29	w	PA_CLR13	IO pin PA13 clear data bit. This bit is no effect for writing 0.	0x00
28	w	PA_CLR12	IO pin PA12 clear data bit. This bit is no effect for writing 0.	0x00
27	w	PA_CLR11	IO pin PA11 clear data bit. This bit is no effect for writing 0.	0x00
26	w	PA_CLR10	IO pin PA10 clear data bit. This bit is no effect for writing 0.	0x00
25	w	PA_CLR9	IO pin PA9 clear data bit. This bit is no effect for writing 0.	0x00
24	w	PA_CLR8	IO pin PA8 clear data bit. This bit is no effect for writing 0.	0x00
23	w	PA_CLR7	IO pin PA7 clear data bit. This bit is no effect for writing 0.	0x00
22	w	PA_CLR6	IO pin PA6 clear data bit. This bit is no effect for writing 0.	0x00
21	w	PA_CLR5	IO pin PA5 clear data bit. This bit is no effect for writing 0.	0x00
20	w	PA_CLR4	IO pin PA4 clear data bit. This bit is no effect for writing 0.	0x00
19	w	PA_CLR3	IO pin PA3 clear data bit. This bit is no effect for writing 0.	0x00
18	w	PA_CLR2	IO pin PA2 clear data bit. This bit is no effect for writing 0.	0x00
17	w	PA_CLR1	IO pin PA1 clear data bit. This bit is no effect for writing 0.	0x00
16	w	PA_CLR0	IO pin PA0 clear data bit. This bit is no effect for writing 0. When the related PA_SETn bit and PA_CLRn bit of a GPIO pin are both set to 1, the related data bit is set to 1 (n={0~15}).	0x00
15	w	PA_SET15	IO pin PA15 set data bit. This bit is no effect for writing 0.	0x00
14	w	PA_SET14	IO pin PA14 set data bit. This bit is no effect for writing 0.	0x00
13	w	PA_SET13	IO pin PA13 set data bit. This bit is no effect for writing 0.	0x00
12	w	PA_SET12	IO pin PA12 set data bit. This bit is no effect for writing 0.	0x00
11	w	PA_SET11	IO pin PA11 set data bit. This bit is no effect for writing 0.	0x00
10	w	PA_SET10	IO pin PA10 set data bit. This bit is no effect for writing 0.	0x00
9	w	PA_SET9	IO pin PA9 set data bit. This bit is no effect for writing 0.	0x00
8	w	PA_SET8	IO pin PA8 set data bit. This bit is no effect for writing 0.	0x00
7	w	PA_SET7	IO pin PA7 set data bit. This bit is no effect for writing 0.	0x00
6	w	PA_SET6	IO pin PA6 set data bit. This bit is no effect for writing 0.	0x00
5	w	PA_SET5	IO pin PA5 set data bit. This bit is no effect for writing 0.	0x00
4	w	PA_SET4	IO pin PA4 set data bit. This bit is no effect for writing 0.	0x00
3	w	PA_SET3	IO pin PA3 set data bit. This bit is no effect for writing 0.	0x00

2	w	PA_SET2	IO pin PA2 set data bit. This bit is no effect for writing 0.	0x00
1	w	PA_SET1	IO pin PA1 set data bit. This bit is no effect for writing 0.	0x00
0	w	PA_SET0	IO pin PA0 set data bit. This bit is no effect for writing 0. When the related PA_SETn bit and PA_CLRn bit of a GPIO pin are both set to 1, the related data bit is set to 1 (n={0~15}).	0x00

1.1.4. PA port set and clear register 0

PA_SCR0	PA port set and clear register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PA_SC3
23	22	21	20	19	18	17	16
Reserved							PA_SC2
15	14	13	12	11	10	9	8
Reserved							PA_SC1
7	6	5	4	3	2	1	0
Reserved							PA_SC0

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PA_SC3	GPIO Port set or clear bit for PA3. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PA_SC2	GPIO Port set or clear bit for PA2. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PA_SC1	GPIO Port set or clear bit for PA1. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PA_SC0	GPIO Port set or clear bit for PA0. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.5. PA port set and clear register 1

PA_SCR1	PA port set and clear register 1		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PA_SC7
23	22	21	20	19	18	17	16
Reserved							PA_SC6
15	14	13	12	11	10	9	8
Reserved							PA_SC5
7	6	5	4	3	2	1	0
Reserved							PA_SC4

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PA_SC7	GPIO Port set or clear bit for PA7. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PA_SC6	GPIO Port set or clear bit for PA6.	0x00

Bit	Attr	Bit Name	Description	Reset
			Write 1 to set data bit and write 0 to clear data. Read for port pin status.	
15..9	-	Reserved	Reserved	0x00
8	rw	PA_SC5	GPIO Port set or clear bit for PA5. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PA_SC4	GPIO Port set or clear bit for PA4. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.6. PA port set and clear register 2

PA_SCR2	PA port set and clear register 2		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PA_SC11
23	22	21	20	19	18	17	16
Reserved							PA_SC10
15	14	13	12	11	10	9	8
Reserved							PA_SC9
7	6	5	4	3	2	1	0
Reserved							PA_SC8

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PA_SC11	GPIO Port set and clear bit for PA11. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PA_SC10	GPIO Port set or clear bit for PA10. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PA_SC9	GPIO Port set or clear bit for PA9. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PA_SC8	GPIO Port set or clear bit for PA8. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.7. PA port set and clear register 3

PA_SCR3	PA port set and clear register 3		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PA_SC15
23	22	21	20	19	18	17	16
Reserved							PA_SC14
15	14	13	12	11	10	9	8
Reserved							PA_SC13
7	6	5	4	3	2	1	0
Reserved							PA_SC12

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00

24	rw	PA_SC15	GPIO Port set or clear bit for PA15. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PA_SC14	GPIO Port set or clear bit for PA14. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PA_SC13	GPIO Port set or clear bit for PA13. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PA_SC12	GPIO Port set or clear bit for PA12. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.8. PB output data register

PB_OUT	PB output data register		
Offset Address :	0x20	Reset Value :	0xFFFFFFFF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PB_OUT15	PB_OUT14	PB_OUT13	PB_OUT12	PB_OUT11	PB_OUT10	PB_OUT9	PB_OUT8
7	6	5	4	3	2	1	0
PB_OUT7	PB_OUT6	PB_OUT5	PB_OUT4	PB_OUT3	PB_OUT2	PB_OUT1	PB_OUT0

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0xFFFF
15	rw	PB_OUT15	IO pin PB15 output data bit.	0x01
14	rw	PB_OUT14	IO pin PB14 output data bit.	0x01
13	rw	PB_OUT13	IO pin PB13 output data bit.	0x01
12	rw	PB_OUT12	IO pin PB12 output data bit.	0x01
11	rw	PB_OUT11	IO pin PB11 output data bit.	0x01
10	rw	PB_OUT10	IO pin PB10 output data bit.	0x01
9	rw	PB_OUT9	IO pin PB9 output data bit.	0x01
8	rw	PB_OUT8	IO pin PB8 output data bit.	0x01
7	rw	PB_OUT7	IO pin PB7 output data bit.	0x01
6	rw	PB_OUT6	IO pin PB6 output data bit.	0x01
5	rw	PB_OUT5	IO pin PB5 output data bit.	0x01
4	rw	PB_OUT4	IO pin PB4 output data bit.	0x01
3	rw	PB_OUT3	IO pin PB3 output data bit.	0x01
2	rw	PB_OUT2	IO pin PB2 output data bit.	0x01
1	rw	PB_OUT1	IO pin PB1 output data bit.	0x01
0	rw	PB_OUT0	IO pin PB0 output data bit.	0x01

1.1.9. PB input data register

PB_IN	PB input data register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8

PB_IN15	PB_IN14	PB_IN13	PB_IN12	PB_IN11	PB_IN10	PB_IN9	PB_IN8
7	6	5	4	3	2	1	0
PB_IN7	PB_IN6	PB_IN5	PB_IN4	PB_IN3	PB_IN2	PB_IN1	PB_IN0

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	r	PB_IN15	IO pin PB15 input pin status.	0x00
14	r	PB_IN14	IO pin PB14 input pin status.	0x00
13	r	PB_IN13	IO pin PB13 input pin status.	0x00
12	r	PB_IN12	IO pin PB12 input pin status.	0x00
11	r	PB_IN11	IO pin PB11 input pin status.	0x00
10	r	PB_IN10	IO pin PB10 input pin status.	0x00
9	r	PB_IN9	IO pin PB9 input pin status.	0x00
8	r	PB_IN8	IO pin PB8 input pin status.	0x00
7	r	PB_IN7	IO pin PB7 input pin status.	0x00
6	r	PB_IN6	IO pin PB6 input pin status.	0x00
5	r	PB_IN5	IO pin PB5 input pin status.	0x00
4	r	PB_IN4	IO pin PB4 input pin status.	0x00
3	r	PB_IN3	IO pin PB3 input pin status.	0x00
2	r	PB_IN2	IO pin PB2 input pin status.	0x00
1	r	PB_IN1	IO pin PB1 input pin status.	0x00
0	r	PB_IN0	IO pin PB0 input pin status.	0x00

1.1.10. PB port set / clear register

PB_SC	PB port set / clear register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PB_CLR15	PB_CLR14	PB_CLR13	PB_CLR12	PB_CLR11	PB_CLR10	PB_CLR9	PB_CLR8
23	22	21	20	19	18	17	16
PB_CLR7	PB_CLR6	PB_CLR5	PB_CLR4	PB_CLR3	PB_CLR2	PB_CLR1	PB_CLR0
15	14	13	12	11	10	9	8
PB_SET15	PB_SET14	PB_SET13	PB_SET12	PB_SET11	PB_SET10	PB_SET9	PB_SET8
7	6	5	4	3	2	1	0
PB_SET7	PB_SET6	PB_SET5	PB_SET4	PB_SET3	PB_SET2	PB_SET1	PB_SET0

Bit	Attr	Bit Name	Description	Reset
31	w	PB_CLR15	IO pin PB15 clear data bit. This bit is no effect for writing 0.	0x00
30	w	PB_CLR14	IO pin PB14 clear data bit. This bit is no effect for writing 0.	0x00
29	w	PB_CLR13	IO pin PB13 clear data bit. This bit is no effect for writing 0.	0x00
28	w	PB_CLR12	IO pin PB12 clear data bit. This bit is no effect for writing 0.	0x00
27	w	PB_CLR11	IO pin PB11 clear data bit. This bit is no effect for writing 0.	0x00
26	w	PB_CLR10	IO pin PB10 clear data bit. This bit is no effect for writing 0.	0x00
25	w	PB_CLR9	IO pin PB9 clear data bit. This bit is no effect for writing 0.	0x00
24	w	PB_CLR8	IO pin PB8 clear data bit. This bit is no effect for writing 0.	0x00
23	w	PB_CLR7	IO pin PB7 clear data bit. This bit is no effect for writing 0.	0x00
22	w	PB_CLR6	IO pin PB6 clear data bit. This bit is no effect for writing 0.	0x00
21	w	PB_CLR5	IO pin PB5 clear data bit. This bit is no effect for writing 0.	0x00
20	w	PB_CLR4	IO pin PB4 clear data bit. This bit is no effect for writing 0.	0x00
19	w	PB_CLR3	IO pin PB3 clear data bit. This bit is no effect for writing 0.	0x00
18	w	PB_CLR2	IO pin PB2 clear data bit. This bit is no effect for writing 0.	0x00
17	w	PB_CLR1	IO pin PB1 clear data bit. This bit is no effect for writing 0.	0x00
16	w	PB_CLR0	IO pin PB0 clear data bit. This bit is no effect for writing 0. When the related PB_SETn bit and PB_CLRn bit of a GPIO pin are both set to 1, the related data bit is set to 1 (n={0~15}).	0x00
15	w	PB_SET15	IO pin PB15 set data bit. This bit is no effect for writing 0.	0x00
14	w	PB_SET14	IO pin PB14 set data bit. This bit is no effect for writing 0.	0x00
13	w	PB_SET13	IO pin PB13 set data bit. This bit is no effect for writing 0.	0x00

12	w	PB_SET12	IO pin PB12 set data bit. This bit is no effect for writing 0.	0x00
11	w	PB_SET11	IO pin PB11 set data bit. This bit is no effect for writing 0.	0x00
10	w	PB_SET10	IO pin PB10 set data bit. This bit is no effect for writing 0.	0x00
9	w	PB_SET9	IO pin PB9 set data bit. This bit is no effect for writing 0.	0x00
8	w	PB_SET8	IO pin PB8 set data bit. This bit is no effect for writing 0.	0x00
7	w	PB_SET7	IO pin PB7 set data bit. This bit is no effect for writing 0.	0x00
6	w	PB_SET6	IO pin PB6 set data bit. This bit is no effect for writing 0.	0x00
5	w	PB_SET5	IO pin PB5 set data bit. This bit is no effect for writing 0.	0x00
4	w	PB_SET4	IO pin PB4 set data bit. This bit is no effect for writing 0.	0x00
3	w	PB_SET3	IO pin PB3 set data bit. This bit is no effect for writing 0.	0x00
2	w	PB_SET2	IO pin PB2 set data bit. This bit is no effect for writing 0.	0x00
1	w	PB_SET1	IO pin PB1 set data bit. This bit is no effect for writing 0.	0x00
0	w	PB_SET0	IO pin PB0 set data bit. This bit is no effect for writing 0. When the related PB_SETn bit and PB_CLRn bit of a GPIO pin are both set to 1, the related data bit is set to 1 (n={0~15}).	0x00

1.1.11. PB port set and clear register 0

PB_SCR0	PB port set and clear register 0		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PB_SC3
23	22	21	20	19	18	17	16
Reserved							PB_SC2
15	14	13	12	11	10	9	8
Reserved							PB_SC1
7	6	5	4	3	2	1	0
Reserved							PB_SC0

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PB_SC3	GPIO Port set or clear bit for PB3. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PB_SC2	GPIO Port set or clear bit for PB2. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PB_SC1	GPIO Port set or clear bit for PB1. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PB_SC0	GPIO Port set or clear bit for PB0. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.12. PB port set and clear register 1

PB_SCR1	PB port set and clear register 1		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PB_SC7
23	22	21	20	19	18	17	16
Reserved							PB_SC6
15	14	13	12	11	10	9	8
Reserved							PB_SC5

7	6	5	4	3	2	1	0
Reserved							PB_SC4

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PB_SC7	GPIO Port set or clear bit for PB7. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PB_SC6	GPIO Port set or clear bit for PB6. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PB_SC5	GPIO Port set or clear bit for PB5. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PB_SC4	GPIO Port set or clear bit for PB4. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.13. PB port set and clear register 2

PB_SCR2	PB port set and clear register 2		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PB_SC11
23	22	21	20	19	18	17	16
Reserved							PB_SC10
15	14	13	12	11	10	9	8
Reserved							PB_SC9
7	6	5	4	3	2	1	0
Reserved							PB_SC8

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PB_SC11	GPIO Port set or clear bit for PB11. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PB_SC10	GPIO Port set or clear bit for PB10. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PB_SC9	GPIO Port set or clear bit for PB9. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PB_SC8	GPIO Port set or clear bit for PB8. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.14. PB port set and clear register 3

PB_SCR3	PB port set and clear register 3		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24

Reserved							PB_SC15
23	22	21	20	19	18	17	16
Reserved							PB_SC14
15	14	13	12	11	10	9	8
Reserved							PB_SC13
7	6	5	4	3	2	1	0
Reserved							PB_SC12

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PB_SC15	GPIO Port set or clear bit for PB15. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PB_SC14	GPIO Port set or clear bit for PB14. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PB_SC13	GPIO Port set or clear bit for PB13. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PB_SC12	GPIO Port set or clear bit for PB12. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.15. PC output data register

PC_OUT	PC output data register		
Offset Address :	0x40	Reset Value :	0xFFFFFFFF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	PC_OUT14	PC_OUT13	PC_OUT12	PC_OUT11	PC_OUT10	PC_OUT9	PC_OUT8
7	6	5	4	3	2	1	0
PC_OUT7	PC_OUT6	PC_OUT5	PC_OUT4	PC_OUT3	PC_OUT2	PC_OUT1	PC_OUT0

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0xFFFF
15	-	Reserved	Reserved	0x01
14	rw	PC_OUT14	IO pin PC14 output data bit.	0x01
13	rw	PC_OUT13	IO pin PC13 output data bit.	0x01
12	rw	PC_OUT12	IO pin PC12 output data bit.	0x01
11	rw	PC_OUT11	IO pin PC11 output data bit.	0x01
10	rw	PC_OUT10	IO pin PC10 output data bit.	0x01
9	rw	PC_OUT9	IO pin PC9 output data bit.	0x01
8	rw	PC_OUT8	IO pin PC8 output data bit.	0x01
7	rw	PC_OUT7	IO pin PC7 output data bit.	0x01
6	rw	PC_OUT6	IO pin PC6 output data bit.	0x01
5	rw	PC_OUT5	IO pin PC5 output data bit.	0x01
4	rw	PC_OUT4	IO pin PC4 output data bit.	0x01
3	rw	PC_OUT3	IO pin PC3 output data bit.	0x01
2	rw	PC_OUT2	IO pin PC2 output data bit.	0x01
1	rw	PC_OUT1	IO pin PC1 output data bit.	0x01
0	rw	PC_OUT0	IO pin PC0 output data bit.	0x01

1.1.16. PC input data register

PC_IN	PC input data register		
Offset Address :	0x44	Reset Value :	0x00008070

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	PC_IN14	PC_IN13	PC_IN12	PC_IN11	PC_IN10	PC_IN9	PC_IN8
7	6	5	4	3	2	1	0
PC_IN7	PC_IN6	PC_IN5	PC_IN4	PC_IN3	PC_IN2	PC_IN1	PC_IN0

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	-	Reserved	Reserved	0x01
14	r	PC_IN14	IO pin PC14 input pin status.	0x00
13	r	PC_IN13	IO pin PC13 input pin status.	0x00
12	r	PC_IN12	IO pin PC12 input pin status.	0x00
11	r	PC_IN11	IO pin PC11 input pin status.	0x00
10	r	PC_IN10	IO pin PC10 input pin status.	0x00
9	r	PC_IN9	IO pin PC9 input pin status.	0x00
8	r	PC_IN8	IO pin PC8 input pin status.	0x00
7	r	PC_IN7	IO pin PC7 input pin status.	0x00
6	r	PC_IN6	IO pin PC6 input pin status.	0x01
5	r	PC_IN5	IO pin PC5 input pin status.	0x01
4	r	PC_IN4	IO pin PC4 input pin status.	0x01
3	r	PC_IN3	IO pin PC3 input pin status.	0x00
2	r	PC_IN2	IO pin PC2 input pin status.	0x00
1	r	PC_IN1	IO pin PC1 input pin status.	0x00
0	r	PC_IN0	IO pin PC0 input pin status.	0x00

1.1.17. PC port set / clear register

PC_SC	PC port set / clear register		
Offset Address :	0x48	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	PC_CLR14	PC_CLR13	PC_CLR12	PC_CLR11	PC_CLR10	PC_CLR9	PC_CLR8
23	22	21	20	19	18	17	16
PC_CLR7	PC_CLR6	PC_CLR5	PC_CLR4	PC_CLR3	PC_CLR2	PC_CLR1	PC_CLR0
15	14	13	12	11	10	9	8
Reserved	PC_SET14	PC_SET13	PC_SET12	PC_SET11	PC_SET10	PC_SET9	PC_SET8
7	6	5	4	3	2	1	0
PC_SET7	PC_SET6	PC_SET5	PC_SET4	PC_SET3	PC_SET2	PC_SET1	PC_SET0

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	w	PC_CLR14	IO pin PC14 clear data bit. This bit is no effect for writing 0.	0x00
29	w	PC_CLR13	IO pin PC13 clear data bit. This bit is no effect for writing 0.	0x00
28	w	PC_CLR12	IO pin PC12 clear data bit. This bit is no effect for writing 0.	0x00
27	w	PC_CLR11	IO pin PC11 clear data bit. This bit is no effect for writing 0.	0x00
26	w	PC_CLR10	IO pin PC10 clear data bit. This bit is no effect for writing 0.	0x00
25	w	PC_CLR9	IO pin PC9 clear data bit. This bit is no effect for writing 0.	0x00
24	w	PC_CLR8	IO pin PC8 clear data bit. This bit is no effect for writing 0.	0x00
23	w	PC_CLR7	IO pin PC7 clear data bit. This bit is no effect for writing 0.	0x00
22	w	PC_CLR6	IO pin PC6 clear data bit. This bit is no effect for writing 0.	0x00
21	w	PC_CLR5	IO pin PC5 clear data bit. This bit is no effect for writing 0.	0x00

20	w	PC_CLR4	IO pin PC4 clear data bit. This bit is no effect for writing 0.	0x00
19	w	PC_CLR3	IO pin PC3 clear data bit. This bit is no effect for writing 0.	0x00
18	w	PC_CLR2	IO pin PC2 clear data bit. This bit is no effect for writing 0.	0x00
17	w	PC_CLR1	IO pin PC1 clear data bit. This bit is no effect for writing 0.	0x00
16	w	PC_CLR0	IO pin PC0 clear data bit. This bit is no effect for writing 0. When the related PC_SETn bit and PC_CLRn bit of a GPIO pin are both set to 1, the related data bit is set to 1 (n={0~15}).	0x00
15	-	Reserved	Reserved	0x00
14	w	PC_SET14	IO pin PC14 set data bit. This bit is no effect for writing 0.	0x00
13	w	PC_SET13	IO pin PC13 set data bit. This bit is no effect for writing 0.	0x00
12	w	PC_SET12	IO pin PC12 set data bit. This bit is no effect for writing 0.	0x00
11	w	PC_SET11	IO pin PC11 set data bit. This bit is no effect for writing 0.	0x00
10	w	PC_SET10	IO pin PC10 set data bit. This bit is no effect for writing 0.	0x00
9	w	PC_SET9	IO pin PC9 set data bit. This bit is no effect for writing 0.	0x00
8	w	PC_SET8	IO pin PC8 set data bit. This bit is no effect for writing 0.	0x00
7	w	PC_SET7	IO pin PC7 set data bit. This bit is no effect for writing 0.	0x00
6	w	PC_SET6	IO pin PC6 set data bit. This bit is no effect for writing 0.	0x00
5	w	PC_SET5	IO pin PC5 set data bit. This bit is no effect for writing 0.	0x00
4	w	PC_SET4	IO pin PC4 set data bit. This bit is no effect for writing 0.	0x00
3	w	PC_SET3	IO pin PC3 set data bit. This bit is no effect for writing 0.	0x00
2	w	PC_SET2	IO pin PC2 set data bit. This bit is no effect for writing 0.	0x00
1	w	PC_SET1	IO pin PC1 set data bit. This bit is no effect for writing 0.	0x00
0	w	PC_SET0	IO pin PC0 set data bit. This bit is no effect for writing 0. When the related PC_SETn bit and PC_CLRn bit of a GPIO pin are both set to 1, the related data bit is set to 1 (n={0~15}).	0x00

1.1.18. PC port set and clear register 0

PC_SCR0	PC port set and clear register 0		
Offset Address :	0x50	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PC_SC3
23	22	21	20	19	18	17	16
Reserved							PC_SC2
15	14	13	12	11	10	9	8
Reserved							PC_SC1
7	6	5	4	3	2	1	0
Reserved							PC_SC0

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PC_SC3	GPIO Port set or clear bit for PC3. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PC_SC2	GPIO Port set or clear bit for PC2. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PC_SC1	GPIO Port set or clear bit for PC1. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PC_SC0	GPIO Port set or clear bit for PC0. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.19. PC port set and clear register 1

PC_SCR1	PC port set and clear register 1		
Offset Address :	0x54	Reset Value :	0x00010101

31	30	29	28	27	26	25	24
Reserved							PC_SC7
23	22	21	20	19	18	17	16
Reserved							PC_SC6
15	14	13	12	11	10	9	8
Reserved							PC_SC5
7	6	5	4	3	2	1	0
Reserved							PC_SC4

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PC_SC7	GPIO Port set or clear bit for PC7. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PC_SC6	GPIO Port set or clear bit for PC6. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x01
15..9	-	Reserved	Reserved	0x00
8	rw	PC_SC5	GPIO Port set or clear bit for PC5. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x01
7..1	-	Reserved	Reserved	0x00
0	rw	PC_SC4	GPIO Port set or clear bit for PC4. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x01

1.1.20. PC port set and clear register 2

PC_SCR2	PC port set and clear register 2		
Offset Address :	0x58	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PC_SC11
23	22	21	20	19	18	17	16
Reserved							PC_SC10
15	14	13	12	11	10	9	8
Reserved							PC_SC9
7	6	5	4	3	2	1	0
Reserved							PC_SC8

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PC_SC11	GPIO Port set or clear bit for PC11. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PC_SC10	GPIO Port set or clear bit for PC10. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PC_SC9	GPIO Port set or clear bit for PC9. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00

0	rw	PC_SC8	GPIO Port set or clear bit for PC8. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.21. PC port set and clear register 3

PC_SCR3	PC port set and clear register 3		
Offset Address :	0x5C	Reset Value :	0x01000000

31	30	29	28	27	26	25	24
Reserved							Reserved
23	22	21	20	19	18	17	16
Reserved							PC_SC14
15	14	13	12	11	10	9	8
Reserved							PC_SC13
7	6	5	4	3	2	1	0
Reserved							PC_SC12

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x01
23..17	-	Reserved	Reserved	0x00
16	rw	PC_SC14	GPIO Port set or clear bit for PC14. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PC_SC13	GPIO Port set or clear bit for PC13. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PC_SC12	GPIO Port set or clear bit for PC12. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.22. PD output data register

PD_OUT	PD output data register		
Offset Address :	0x60	Reset Value :	0xFFFFFFFF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_OUT15	PD_OUT14	PD_OUT13	PD_OUT12	PD_OUT11	PD_OUT10	PD_OUT9	PD_OUT8
7	6	5	4	3	2	1	0
PD_OUT7	PD_OUT6	PD_OUT5	PD_OUT4	PD_OUT3	PD_OUT2	PD_OUT1	PD_OUT0

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0xFFFF
15	rw	PD_OUT15	IO pin PD15 output data bit.	0x01
14	rw	PD_OUT14	IO pin PD14 output data bit.	0x01
13	rw	PD_OUT13	IO pin PD13 output data bit.	0x01
12	rw	PD_OUT12	IO pin PD12 output data bit.	0x01
11	rw	PD_OUT11	IO pin PD11 output data bit.	0x01
10	rw	PD_OUT10	IO pin PD10 output data bit.	0x01
9	rw	PD_OUT9	IO pin PD9 output data bit.	0x01
8	rw	PD_OUT8	IO pin PD8 output data bit.	0x01
7	rw	PD_OUT7	IO pin PD7 output data bit.	0x01

6	rw	PD_OUT6	IO pin PD6 output data bit.	0x01
5	rw	PD_OUT5	IO pin PD5 output data bit.	0x01
4	rw	PD_OUT4	IO pin PD4 output data bit.	0x01
3	rw	PD_OUT3	IO pin PD3 output data bit.	0x01
2	rw	PD_OUT2	IO pin PD2 output data bit.	0x01
1	rw	PD_OUT1	IO pin PD1 output data bit.	0x01
0	rw	PD_OUT0	IO pin PD0 output data bit.	0x01

1.1.23. PD input data register

PD_IN	PD input data register		
Offset Address :	0x64	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_IN15	PD_IN14	PD_IN13	PD_IN12	PD_IN11	PD_IN10	PD_IN9	PD_IN8
7	6	5	4	3	2	1	0
PD_IN7	PD_IN6	PD_IN5	PD_IN4	PD_IN3	PD_IN2	PD_IN1	PD_IN0

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	r	PD_IN15	IO pin PD15 input pin status.	0x00
14	r	PD_IN14	IO pin PD14 input pin status.	0x00
13	r	PD_IN13	IO pin PD13 input pin status.	0x00
12	r	PD_IN12	IO pin PD12 input pin status.	0x00
11	r	PD_IN11	IO pin PD11 input pin status.	0x00
10	r	PD_IN10	IO pin PD10 input pin status.	0x00
9	r	PD_IN9	IO pin PD9 input pin status.	0x00
8	r	PD_IN8	IO pin PD8 input pin status.	0x00
7	r	PD_IN7	IO pin PD7 input pin status.	0x00
6	r	PD_IN6	IO pin PD6 input pin status.	0x00
5	r	PD_IN5	IO pin PD5 input pin status.	0x00
4	r	PD_IN4	IO pin PD4 input pin status.	0x00
3	r	PD_IN3	IO pin PD3 input pin status.	0x00
2	r	PD_IN2	IO pin PD2 input pin status.	0x00
1	r	PD_IN1	IO pin PD1 input pin status.	0x00
0	r	PD_IN0	IO pin PD0 input pin status.	0x00

1.1.24. PD port set / clear register

PD_SC	PD port set / clear register		
Offset Address :	0x68	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PD_CLR15	PD_CLR14	PD_CLR13	PD_CLR12	PD_CLR11	PD_CLR10	PD_CLR9	PD_CLR8
23	22	21	20	19	18	17	16
PD_CLR7	PD_CLR6	PD_CLR5	PD_CLR4	PD_CLR3	PD_CLR2	PD_CLR1	PD_CLR0
15	14	13	12	11	10	9	8
PD_SET15	PD_SET14	PD_SET13	PD_SET12	PD_SET11	PD_SET10	PD_SET9	PD_SET8
7	6	5	4	3	2	1	0
PD_SET7	PD_SET6	PD_SET5	PD_SET4	PD_SET3	PD_SET2	PD_SET1	PD_SET0

Bit	Attr	Bit Name	Description	Reset
31	w	PD_CLR15	IO pin PD15 clear data bit. This bit is no effect for writing 0.	0x00
30	w	PD_CLR14	IO pin PD14 clear data bit. This bit is no effect for writing 0.	0x00
29	w	PD_CLR13	IO pin PD13 clear data bit. This bit is no effect for writing 0.	0x00

28	w	PD_CLR12	IO pin PD12 clear data bit. This bit is no effect for writing 0.	0x00
27	w	PD_CLR11	IO pin PD11 clear data bit. This bit is no effect for writing 0.	0x00
26	w	PD_CLR10	IO pin PD10 clear data bit. This bit is no effect for writing 0.	0x00
25	w	PD_CLR9	IO pin PD9 clear data bit. This bit is no effect for writing 0.	0x00
24	w	PD_CLR8	IO pin PD8 clear data bit. This bit is no effect for writing 0.	0x00
23	w	PD_CLR7	IO pin PD7 clear data bit. This bit is no effect for writing 0.	0x00
22	w	PD_CLR6	IO pin PD6 clear data bit. This bit is no effect for writing 0.	0x00
21	w	PD_CLR5	IO pin PD5 clear data bit. This bit is no effect for writing 0.	0x00
20	w	PD_CLR4	IO pin PD4 clear data bit. This bit is no effect for writing 0.	0x00
19	w	PD_CLR3	IO pin PD3 clear data bit. This bit is no effect for writing 0.	0x00
18	w	PD_CLR2	IO pin PD2 clear data bit. This bit is no effect for writing 0.	0x00
17	w	PD_CLR1	IO pin PD1 clear data bit. This bit is no effect for writing 0.	0x00
16	w	PD_CLR0	IO pin PD0 clear data bit. This bit is no effect for writing 0. When the related PD_SETn bit and PD_CLRn bit of a GPIO pin are both set to 1, the related data bit is set to 1 (n={0~15}).	0x00
15	w	PD_SET15	IO pin PD15 set data bit. This bit is no effect for writing 0.	0x00
14	w	PD_SET14	IO pin PD14 set data bit. This bit is no effect for writing 0.	0x00
13	w	PD_SET13	IO pin PD13 set data bit. This bit is no effect for writing 0.	0x00
12	w	PD_SET12	IO pin PD12 set data bit. This bit is no effect for writing 0.	0x00
11	w	PD_SET11	IO pin PD11 set data bit. This bit is no effect for writing 0.	0x00
10	w	PD_SET10	IO pin PD10 set data bit. This bit is no effect for writing 0.	0x00
9	w	PD_SET9	IO pin PD9 set data bit. This bit is no effect for writing 0.	0x00
8	w	PD_SET8	IO pin PD8 set data bit. This bit is no effect for writing 0.	0x00
7	w	PD_SET7	IO pin PD7 set data bit. This bit is no effect for writing 0.	0x00
6	w	PD_SET6	IO pin PD6 set data bit. This bit is no effect for writing 0.	0x00
5	w	PD_SET5	IO pin PD5 set data bit. This bit is no effect for writing 0.	0x00
4	w	PD_SET4	IO pin PD4 set data bit. This bit is no effect for writing 0.	0x00
3	w	PD_SET3	IO pin PD3 set data bit. This bit is no effect for writing 0.	0x00
2	w	PD_SET2	IO pin PD2 set data bit. This bit is no effect for writing 0.	0x00
1	w	PD_SET1	IO pin PD1 set data bit. This bit is no effect for writing 0.	0x00
0	w	PD_SET0	IO pin PD0 set data bit. This bit is no effect for writing 0. When the related PD_SETn bit and PD_CLRn bit of a GPIO pin are both set to 1, the related data bit is set to 1 (n={0~15}).	0x00

1.1.25. PD port set and clear register 0

PD_SCR0	PD port set and clear register 0		
Offset Address :	0x70	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PD_SC3
23	22	21	20	19	18	17	16
Reserved							PD_SC2
15	14	13	12	11	10	9	8
Reserved							PD_SC1
7	6	5	4	3	2	1	0
Reserved							PD_SC0

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PD_SC3	GPIO Port set or clear bit for PD3. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PD_SC2	GPIO Port set or clear bit for PD2. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00

8	rw	PD_SC1	GPIO Port set or clear bit for PD1. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PD_SC0	GPIO Port set or clear bit for PD0. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.26. PD port set and clear register 1

PD_SCR1	PD port set and clear register 1		
Offset Address :	0x74	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PD_SC7
23	22	21	20	19	18	17	16
Reserved							PD_SC6
15	14	13	12	11	10	9	8
Reserved							PD_SC5
7	6	5	4	3	2	1	0
Reserved							PD_SC4

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PD_SC7	GPIO Port set or clear bit for PD7. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PD_SC6	GPIO Port set or clear bit for PD6. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PD_SC5	GPIO Port set or clear bit for PD5. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PD_SC4	GPIO Port set or clear bit for PD4. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.27. PD port set and clear register 2

PD_SCR2	PD port set and clear register 2		
Offset Address :	0x78	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PD_SC11
23	22	21	20	19	18	17	16
Reserved							PD_SC10
15	14	13	12	11	10	9	8
Reserved							PD_SC9
7	6	5	4	3	2	1	0
Reserved							PD_SC8

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PD_SC11	GPIO Port set or clear bit for PD11. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

23..17	-	Reserved	Reserved	0x00
16	rw	PD_SC10	GPIO Port set or clear bit for PD10. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PD_SC9	GPIO Port set or clear bit for PD9. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PD_SC8	GPIO Port set or clear bit for PD8. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.28. PD port set and clear register 3

PD_SCR3	PD port set and clear register 3		
Offset Address :	0x7C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PD_SC15
23	22	21	20	19	18	17	16
Reserved							PD_SC14
15	14	13	12	11	10	9	8
Reserved							PD_SC13
7	6	5	4	3	2	1	0
Reserved							PD_SC12

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PD_SC15	GPIO Port set or clear bit for PD15. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PD_SC14	GPIO Port set or clear bit for PD14. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PD_SC13	GPIO Port set or clear bit for PD13. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PD_SC12	GPIO Port set or clear bit for PD12. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.29. PE output data register

PE_OUT	PE output data register		
Offset Address :	0x80	Reset Value :	0xFFFFFFFF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PE_OUT15	PE_OUT14	PE_OUT13	PE_OUT12	PE_OUT11	PE_OUT10	PE_OUT9	PE_OUT8
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	PE_OUT3	PE_OUT2	PE_OUT1	PE_OUT0

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0xFFFF
15	rw	PE_OUT15	IO pin PE15 output data bit.	0x01
14	rw	PE_OUT14	IO pin PE14 output data bit.	0x01
13	rw	PE_OUT13	IO pin PE13 output data bit.	0x01
12	rw	PE_OUT12	IO pin PE12 output data bit.	0x01
11	rw	PE_OUT11	IO pin PE11 output data bit.	0x01
10	rw	PE_OUT10	IO pin PE10 output data bit.	0x01
9	rw	PE_OUT9	IO pin PE9 output data bit.	0x01
8	rw	PE_OUT8	IO pin PE8 output data bit.	0x01
7	-	Reserved	Reserved	0x01
6	-	Reserved	Reserved	0x01
5	-	Reserved	Reserved	0x01
4	-	Reserved	Reserved	0x01
3	rw	PE_OUT3	IO pin PE3 output data bit.	0x01
2	rw	PE_OUT2	IO pin PE2 output data bit.	0x01
1	rw	PE_OUT1	IO pin PE1 output data bit.	0x01
0	rw	PE_OUT0	IO pin PE0 output data bit.	0x01

1.1.30. PE input data register

PE_IN	PE input data register		
Offset Address :	0x84	Reset Value :	0x000000F0

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PE_IN15	PE_IN14	PE_IN13	PE_IN12	PE_IN11	PE_IN10	PE_IN9	PE_IN8
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	Reserved	Reserved	Reserved	PE_IN3	PE_IN2	PE_IN1	PE_IN0

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	r	PE_IN15	IO pin PE15 input pin status.	0x00
14	r	PE_IN14	IO pin PE14 input pin status.	0x00
13	r	PE_IN13	IO pin PE13 input pin status.	0x00
12	r	PE_IN12	IO pin PE12 input pin status.	0x00
11	r	PE_IN11	IO pin PE11 input pin status.	0x00
10	r	PE_IN10	IO pin PE10 input pin status.	0x00
9	r	PE_IN9	IO pin PE9 input pin status.	0x00
8	r	PE_IN8	IO pin PE8 input pin status.	0x00
7	-	Reserved	Reserved	0x01
6	-	Reserved	Reserved	0x01
5	-	Reserved	Reserved	0x01
4	-	Reserved	Reserved	0x01
3	r	PE_IN3	IO pin PE3 input pin status.	0x00
2	r	PE_IN2	IO pin PE2 input pin status.	0x00
1	r	PE_IN1	IO pin PE1 input pin status.	0x00
0	r	PE_IN0	IO pin PE0 input pin status.	0x00

1.1.31. PE port set / clear register

PE_SC	PE port set / clear register		
Offset Address :	0x88	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PE_CLR15	PE_CLR14	PE_CLR13	PE_CLR12	PE_CLR11	PE_CLR10	PE_CLR9	PE_CLR8

23	22	21	20	19	18	17	16
Reserved	Reserved	Reserved	Reserved	PE_CLR3	PE_CLR2	PE_CLR1	PE_CLR0
15	14	13	12	11	10	9	8
PE_SET15	PE_SET14	PE_SET13	PE_SET12	PE_SET11	PE_SET10	PE_SET9	PE_SET8
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	PE_SET3	PE_SET2	PE_SET1	PE_SET0

Bit	Attr	Bit Name	Description	Reset
31	w	PE_CLR15	IO pin PE15 clear data bit. This bit is no effect for writing 0.	0x00
30	w	PE_CLR14	IO pin PE14 clear data bit. This bit is no effect for writing 0.	0x00
29	w	PE_CLR13	IO pin PE13 clear data bit. This bit is no effect for writing 0.	0x00
28	w	PE_CLR12	IO pin PE12 clear data bit. This bit is no effect for writing 0.	0x00
27	w	PE_CLR11	IO pin PE11 clear data bit. This bit is no effect for writing 0.	0x00
26	w	PE_CLR10	IO pin PE10 clear data bit. This bit is no effect for writing 0.	0x00
25	w	PE_CLR9	IO pin PE9 clear data bit. This bit is no effect for writing 0.	0x00
24	w	PE_CLR8	IO pin PE8 clear data bit. This bit is no effect for writing 0.	0x00
23	-	Reserved	Reserved	0x00
22	-	Reserved	Reserved	0x00
21	-	Reserved	Reserved	0x00
20	-	Reserved	Reserved	0x00
19	w	PE_CLR3	IO pin PE3 clear data bit. This bit is no effect for writing 0.	0x00
18	w	PE_CLR2	IO pin PE2 clear data bit. This bit is no effect for writing 0.	0x00
17	w	PE_CLR1	IO pin PE1 clear data bit. This bit is no effect for writing 0.	0x00
16	w	PE_CLR0	IO pin PE0 clear data bit. This bit is no effect for writing 0. When the related PE_SETn bit and PE_CLRn bit of a GPIO pin are both set to 1, the related data bit is set to 1 (n={0~15}).	0x00
15	w	PE_SET15	IO pin PE15 set data bit. This bit is no effect for writing 0.	0x00
14	w	PE_SET14	IO pin PE14 set data bit. This bit is no effect for writing 0.	0x00
13	w	PE_SET13	IO pin PE13 set data bit. This bit is no effect for writing 0.	0x00
12	w	PE_SET12	IO pin PE12 set data bit. This bit is no effect for writing 0.	0x00
11	w	PE_SET11	IO pin PE11 set data bit. This bit is no effect for writing 0.	0x00
10	w	PE_SET10	IO pin PE10 set data bit. This bit is no effect for writing 0.	0x00
9	w	PE_SET9	IO pin PE9 set data bit. This bit is no effect for writing 0.	0x00
8	w	PE_SET8	IO pin PE8 set data bit. This bit is no effect for writing 0.	0x00
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3	w	PE_SET3	IO pin PE3 set data bit. This bit is no effect for writing 0.	0x00
2	w	PE_SET2	IO pin PE2 set data bit. This bit is no effect for writing 0.	0x00
1	w	PE_SET1	IO pin PE1 set data bit. This bit is no effect for writing 0.	0x00
0	w	PE_SET0	IO pin PE0 set data bit. This bit is no effect for writing 0. When the related PE_SETn bit and PE_CLRn bit of a GPIO pin are both set to 1, the related data bit is set to 1 (n={0~15}).	0x00

1.1.32. PE port set and clear register 0

PE_SCR0	PE port set and clear register 0		
Offset Address :	0x90	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PE_SC3
23	22	21	20	19	18	17	16
Reserved							PE_SC2
15	14	13	12	11	10	9	8
Reserved							PE_SC1
7	6	5	4	3	2	1	0
Reserved							PE_SC0

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PE_SC3	GPIO Port set or clear bit for PE3. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PE_SC2	GPIO Port set or clear bit for PE2. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PE_SC1	GPIO Port set or clear bit for PE1. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PE_SC0	GPIO Port set or clear bit for PE0. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.33. PE port set and clear register 2

PE_SCR2	PE port set and clear register 2		
Offset Address :	0x98	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PE_SC11
23	22	21	20	19	18	17	16
Reserved							PE_SC10
15	14	13	12	11	10	9	8
Reserved							PE_SC9
7	6	5	4	3	2	1	0
Reserved							PE_SC8

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PE_SC11	GPIO Port set or clear bit for PE11. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PE_SC10	GPIO Port set or clear bit for PE10. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PE_SC9	GPIO Port set or clear bit for PE9. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PE_SC8	GPIO Port set or clear bit for PE8. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.34. PE port set and clear register 3

PE_SCR3	PE port set and clear register 3		
Offset Address :	0x9C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PE_SC15
23	22	21	20	19	18	17	16
Reserved							PE_SC14

15	14	13	12	11	10	9	8
Reserved							PE_SC13
7	6	5	4	3	2	1	0
Reserved							PE_SC12

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PE_SC15	GPIO Port set or clear bit for PE15. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	PE_SC14	GPIO Port set or clear bit for PE14. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	PE_SC13	GPIO Port set or clear bit for PE13. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	PE_SC12	GPIO Port set or clear bit for PE12. Write 1 to set data bit and write 0 to clear data. Read for port pin status.	0x00

1.1.35. IOP Register Map

IOP Register Map Register Number = 34

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	PA_OUT	Reserved																PA_OUT15	PA_OUT14	PA_OUT13	PA_OUT12	PA_OUT11	PA_OUT10	PA_OUT9	PA_OUT8	PA_OUT7	PA_OUT6	PA_OUT5	PA_OUT4	PA_OUT3	PA_OUT2	PA_OUT1	PA_OUT0
Reset	0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x04	PA_IN	Reserved																PA_IN15	PA_IN14	PA_IN13	PA_IN12	PA_IN11	PA_IN10	PA_IN9	PA_IN8	PA_IN7	PA_IN6	PA_IN5	PA_IN4	PA_IN3	PA_IN2	PA_IN1	PA_IN0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	PA_SC	PA_CLR15	PA_CLR14	PA_CLR13	PA_CLR12	PA_CLR11	PA_CLR10	PA_CLR9	PA_CLR8	PA_CLR7	PA_CLR6	PA_CLR5	PA_CLR4	PA_CLR3	PA_CLR2	PA_CLR1	PA_CLR0	PA_SET15	PA_SET14	PA_SET13	PA_SET12	PA_SET11	PA_SET10	PA_SET9	PA_SET8	PA_SET7	PA_SET6	PA_SET5	PA_SET4	PA_SET3	PA_SET2	PA_SET1	PA_SET0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	PA_SCR0	Reserved							PA_SC3	Reserved							PA_SC2	Reserved							PA_SC1	Reserved							PA_SC0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	PA_SCR1	Reserved							PA_SC7	Reserved							PA_SC6	Reserved							PA_SC5	Reserved							PA_SC4
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	PA_SCR2	Reserved							PA_SC11	Reserved							PA_SC10	Reserved							PA_SC9	Reserved							PA_SC8
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	PA_SCR3	Reserved							PA_SC15	Reserved							PA_SC14	Reserved							PA_SC13	Reserved							PA_SC12
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	PB_OUT	Reserved																PB_OUT15	PB_OUT14	PB_OUT13	PB_OUT12	PB_OUT11	PB_OUT10	PB_OUT9	PB_OUT8	PB_OUT7	PB_OUT6	PB_OUT5	PB_OUT4	PB_OUT3	PB_OUT2	PB_OUT1	PB_OUT0
Reset	0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

0x24	PB_IN	Reserved																PB_IN15	PB_IN14	PB_IN13	PB_IN12	PB_IN11	PB_IN10	PB_IN9	PB_IN8	PB_IN7	PB_IN6	PB_IN5	PB_IN4	PB_IN3	PB_IN2	PB_IN1	PB_IN0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	PB_SC	PB_CLR15	PB_CLR14	PB_CLR13	PB_CLR12	PB_CLR11	PB_CLR10	PB_CLR9	PB_CLR8	PB_CLR7	PB_CLR6	PB_CLR5	PB_CLR4	PB_CLR3	PB_CLR2	PB_CLR1	PB_CLR0	PB_SET15	PB_SET14	PB_SET13	PB_SET12	PB_SET11	PB_SET10	PB_SET9	PB_SET8	PB_SET7	PB_SET6	PB_SET5	PB_SET4	PB_SET3	PB_SET2	PB_SET1	PB_SET0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	PB_SCR0	Reserved							PB_SC3	Reserved							PB_SC2	Reserved							PB_SC1	Reserved							PB_SC0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	PB_SCR1	Reserved							PB_SC7	Reserved							PB_SC6	Reserved							PB_SC5	Reserved							PB_SC4
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	PB_SCR2	Reserved							PB_SC11	Reserved							PB_SC10	Reserved							PB_SC9	Reserved							PB_SC8
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	PB_SCR3	Reserved							PB_SC15	Reserved							PB_SC14	Reserved							PB_SC13	Reserved							PB_SC12
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	PC_OUT	Reserved																Reserved	PC_OUT14	PC_OUT13	PC_OUT12	PC_OUT11	PC_OUT10	PC_OUT9	PC_OUT8	PC_OUT7	PC_OUT6	PC_OUT5	PC_OUT4	PC_OUT3	PC_OUT2	PC_OUT1	PC_OUT0
Reset	0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x44	PC_IN	Reserved																Reserved	PC_IN14	PC_IN13	PC_IN12	PC_IN11	PC_IN10	PC_IN9	PC_IN8	PC_IN7	PC_IN6	PC_IN5	PC_IN4	PC_IN3	PC_IN2	PC_IN1	PC_IN0
Reset	0x00008070	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
0x48	PC_SC	Reserved	PC_CLR14	PC_CLR13	PC_CLR12	PC_CLR11	PC_CLR10	PC_CLR9	PC_CLR8	PC_CLR7	PC_CLR6	PC_CLR5	PC_CLR4	PC_CLR3	PC_CLR2	PC_CLR1	PC_CLR0	Reserved	PC_SET14	PC_SET13	PC_SET12	PC_SET11	PC_SET10	PC_SET9	PC_SET8	PC_SET7	PC_SET6	PC_SET5	PC_SET4	PC_SET3	PC_SET2	PC_SET1	PC_SET0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x50	PC_SCR0	Reserved							PC_SC3	Reserved							PC_SC2	Reserved							PC_SC1	Reserved							PC_SC0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x54	PC_SCR1	Reserved							PC_SC7	Reserved							PC_SC6	Reserved							PC_SC5	Reserved							PC_SC4
Reset	**0x00010101**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
0x58	PC_SCR2	Reserved							PC_SC11	Reserved							PC_SC10	Reserved							PC_SC9	Reserved							PC_SC8
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x5C	PC_SCR3	Reserved							Reserved	Reserved							PC_SC14	Reserved							PC_SC13	Reserved							PC_SC12
Reset	**0x01000000**	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x60	PD_OUT	Reserved																PD_OUT15	PD_OUT14	PD_OUT13	PD_OUT12	PD_OUT11	PD_OUT10	PD_OUT9	PD_OUT8	PD_OUT7	PD_OUT6	PD_OUT5	PD_OUT4	PD_OUT3	PD_OUT2	PD_OUT1	PD_OUT0
Reset	**0xFFFFFFFF**	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x64	PD_IN	Reserved																PD_IN15	PD_IN14	PD_IN13	PD_IN12	PD_IN11	PD_IN10	PD_IN9	PD_IN8	PD_IN7	PD_IN6	PD_IN5	PD_IN4	PD_IN3	PD_IN2	PD_IN1	PD_IN0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x68	PD_SC	PD_CLR15	PD_CLR14	PD_CLR13	PD_CLR12	PD_CLR11	PD_CLR10	PD_CLR9	PD_CLR8	PD_CLR7	PD_CLR6	PD_CLR5	PD_CLR4	PD_CLR3	PD_CLR2	PD_CLR1	PD_CLR0	PD_SET15	PD_SET14	PD_SET13	PD_SET12	PD_SET11	PD_SET10	PD_SET9	PD_SET8	PD_SET7	PD_SET6	PD_SET5	PD_SET4	PD_SET3	PD_SET2	PD_SET1	PD_SET0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x70	PD_SCR0	Reserved							PD_SC3	Reserved							PD_SC2	Reserved							PD_SC1	Reserved							PD_SC0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x74	PD_SCR1	Reserved							PD_SC7	Reserved							PD_SC6	Reserved							PD_SC5	Reserved							PD_SC4
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x78	PD_SCR2	Reserved							PD_SC11	Reserved							PD_SC10	Reserved							PD_SC9	Reserved							PD_SC8
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x7C	PD_SCR3	Reserved							PD_SC15	Reserved							PD_SC14	Reserved							PD_SC13	Reserved							PD_SC12
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x80	PE_OUT	Reserved																PE_OUT15	PE_OUT14	PE_OUT13	PE_OUT12	PE_OUT11	PE_OUT10	PE_OUT9	PE_OUT8	Reserved	Reserved	Reserved	Reserved	PE_OUT3	PE_OUT2	PE_OUT1	PE_OUT0
Reset	0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x84	PE_IN	Reserved																PE_IN15	PE_IN14	PE_IN13	PE_IN12	PE_IN11	PE_IN10	PE_IN9	PE_IN8	Reserved	Reserved	Reserved	Reserved	PE_IN3	PE_IN2	PE_IN1	PE_IN0
Reset	0x000000F0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
0x88	PE_SC	PE_CLR15	PE_CLR14	PE_CLR13	PE_CLR12	PE_CLR11	PE_CLR10	PE_CLR9	PE_CLR8	Reserved	Reserved	Reserved	Reserved	PE_CLR3	PE_CLR2	PE_CLR1	PE_CLR0	PE_SET15	PE_SET14	PE_SET13	PE_SET12	PE_SET11	PE_SET10	PE_SET9	PE_SET8	Reserved	Reserved	Reserved	Reserved	PE_SET3	PE_SET2	PE_SET1	PE_SET0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x90	PE_SCR0	Reserved							PE_SC3	Reserved							PE_SC2	Reserved							PE_SC1	Reserved							PE_SC0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x98	PE_SCR2	Reserved							PE_SC11	Reserved							PE_SC10	Reserved							PE_SC9	Reserved							PE_SC8
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x9C	PE_SCR3	Reserved							PE_SC15	Reserved							PE_SC14	Reserved							PE_SC13	Reserved							PE_SC12
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.2. Port A Configure Registers

Port A Configure	(PA) Port A IO Mode Configure
Base Address :	0x44000000

1.2.1. PA0 IO control register

PA_CR0	PA0 IO control register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PA_AFS0[3:0]				PA_FDIV0[1:0]		PA_ODC0	Reserved
7	6	5	4	3	2	1	0
PA_INV0	Reserved	PA_PU0	Reserved	PA_HS0	PA_IOM0[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PA_AFS0	PA0 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA0 0x1 = AF1 : Reserved 0x2 = AF2 : Reserved 0x3 = AF3 : Reserved 0x4 = AF4 : Reserved 0x5 = AF5 : Reserved 0x6 = AF6 : SDT_P0 0x7 = AF7 : CCL_P0 0x8 = AF8 : MA0 0x9 = AF9 : MAD0 0xA = AF10 : TM36_OC00 0xB = AF11 : URT4_TX ADC ~ ADC_I0 (IO mode set AIO & input to ADC macro)	0x00
11..10	rw	PA_FDIV0	PA0 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PA_ODC0	PA0 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PA_INV0	PA0 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PA_PU0	PA0 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PA_HS0	PA0 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PA_IOM0	PA0 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.2. PA1 IO control register

PA_CR1	PA1 IO control register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PA_AFS1[3:0]				PA_FDIV1[1:0]		PA_ODC1	Reserved
7	6	5	4	3	2	1	0
PA_INV1	Reserved	PA_PU1	Reserved	PA_HS1	PA_IOM1[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PA_AFS1	PA1 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA1 0x1 = AF1 : Reserved 0x2 = AF2 : Reserved 0x3 = AF3 : Reserved 0x4 = AF4 : Reserved 0x5 = AF5 : Reserved 0x6 = AF6 : Reserved 0x7 = AF7 : CCL_P1 0x8 = AF8 : MA1 0x9 = AF9 : MAD1 0xA = AF10 : TM36_OC10 0xB = AF11 : URT4_RX ADC ~ ADC_I1 (IO mode set AIO & input to ADC macro)	0x00
11..10	rw	PA_FDIV1	PA1 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PA_ODC1	PA1 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PA_INV1	PA1 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PA_PU1	PA1 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PA_HS1	PA1 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PA_IOM1	PA1 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.3. PA2 IO control register

PA_CR2	PA2 IO control register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PA_AFS2[3:0]				PA_FDIV2[1:0]		PA_ODC2	Reserved
7	6	5	4	3	2	1	0
PA_INV2	Reserved	PA_PU2	Reserved	PA_HS2	PA_IOM2[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PA_AFS2	PA2 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA2 0x1 = AF1 : Reserved 0x2 = AF2 : Reserved 0x3 = AF3 : Reserved 0x4 = AF4 : Reserved 0x5 = AF5 : Reserved 0x6 = AF6 : SDT_I0 0x7 = AF7 : Reserved 0x8 = AF8 : MA2 0x9 = AF9 : MAD2 0xA = AF10 : TM36_OC2 0xB = AF11 : URT5_TX ADC ~ ADC_I2 (IO mode set AIO & input to ADC macro)	0x00
11..10	rw	PA_FDIV2	PA2 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PA_ODC2	PA2 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PA_INV2	PA2 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PA_PU2	PA2 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PA_HS2	PA2 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PA_IOM2	PA2 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.4. PA3 IO control register

PA_CR3	PA3 IO control register		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PA_AFS3[3:0]				PA_FDIV3[1:0]		PA_ODC3	Reserved
7	6	5	4	3	2	1	0
PA_INV3	Reserved	PA_PU3	Reserved	PA_HS3	PA_IOM3[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PA_AFS3	PA3 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA3 0x1 = AF1 : Reserved 0x2 = AF2 : Reserved 0x3 = AF3 : Reserved 0x4 = AF4 : Reserved 0x5 = AF5 : Reserved 0x6 = AF6 : SDT_I1 0x7 = AF7 : Reserved 0x8 = AF8 : MA3 0x9 = AF9 : MAD3 0xA = AF10 : TM36_OC2N 0xB = AF11 : URT5_RX ADC ~ ADC_I3 (IO mode set AIO & input to ADC macro)	0x00
11..10	rw	PA_FDIV3	PA3 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PA_ODC3	PA3 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PA_INV3	PA3 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PA_PU3	PA3 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PA_HS3	PA3 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PA_IOM3	PA3 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.5. PA4 IO control register

PA_CR4	PA4 IO control register		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16

Reserved							
15	14	13	12	11	10	9	8
PA_AFS4[3:0]				PA_FDIV4[1:0]		PA_ODC4	Reserved
7	6	5	4	3	2	1	0
PA_INV4	Reserved	PA_PU4	Reserved	PA_HS4	PA_IOM4[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PA_AFS4	PA4 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA4 0x1 = AF1 : Reserved 0x2 = AF2 : Reserved 0x3 = AF3 : Reserved 0x4 = AF4 : Reserved 0x5 = AF5 : Reserved 0x6 = AF6 : Reserved 0x7 = AF7 : Reserved 0x8 = AF8 : MA4 0x9 = AF9 : MAD4 0xA = AF10 : TM20_OC00 0xB = AF11 : URT0_TX ADC ~ ADC_I4 (IO mode set AIO & input to ADC macro)	0x00
11..10	rw	PA_FDIV4	PA4 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PA_ODC4	PA4 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PA_INV4	PA4 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PA_PU4	PA4 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PA_HS4	PA4 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PA_IOM4	PA4 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.6. PA5 IO control register

PA_CR5	PA5 IO control register		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PA_AFS5[3:0]				PA_FDIV5[1:0]		PA_ODC5	Reserved

7	6	5	4	3	2	1	0
PA_INV5	Reserved	PA_PU5	Reserved	PA_HS5	PA_IOM5[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PA_AFS5	PA5 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA5 0x1 = AF1 : Reserved 0x2 = AF2 : Reserved 0x3 = AF3 : Reserved 0x4 = AF4 : Reserved 0x5 = AF5 : Reserved 0x6 = AF6 : Reserved 0x7 = AF7 : Reserved 0x8 = AF8 : MA5 0x9 = AF9 : MAD5 0xA = AF10 : TM20_OC10 0xB = AF11 : URT0_RX ADC ~ ADC_I5 (IO mode set AIO & input to ADC macro)	0x00
11..10	rw	PA_FDIV5	PA5 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PA_ODC5	PA5 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PA_INV5	PA5 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PA_PU5	PA5 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PA_HS5	PA5 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PA_IOM5	PA5 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.7. PA6 IO control register

PA_CR6	PA6 IO control register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PA_AFS6[3:0]				PA_FDIV6[1:0]		PA_ODC6	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PA_INV6	Reserved	PA_PU6	Reserved	PA_HS6	PA_IOM6[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PA_AFS6	PA6 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA6 0x1 = AF1 : Reserved 0x2 = AF2 : Reserved 0x3 = AF3 : Reserved 0x4 = AF4 : Reserved 0x5 = AF5 : Reserved 0x6 = AF6 : Reserved 0x7 = AF7 : SPI0_D3 0x8 = AF8 : MA6 0x9 = AF9 : MAD6 0xA = AF10 : TM20_OC0H 0xB = AF11 : URT0_CLK ADC ~ ADC_I6 (IO mode set AIO & input to ADC macro)	0x00
11..10	rw	PA_FDIV6	PA6 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PA_ODC6	PA6 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PA_INV6	PA6 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PA_PU6	PA6 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PA_HS6	PA6 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PA_IOM6	PA6 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.8. PA7 IO control register

PA_CR7	PA7 IO control register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PA_AFS7[3:0]				PA_FDIV7[1:0]		PA_ODC7	Reserved
7	6	5	4	3	2	1	0
PA_INV7	Reserved	PA_PU7	Reserved	PA_HS7	PA_IOM7[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PA_AFS7	PA7 pin alternate function select. Refer the GPIO AFS table for	0x00

			detail information. 0x0 = AF0 : GPA7 0x1 = AF1 : Reserved 0x2 = AF2 : Reserved 0x3 = AF3 : Reserved 0x4 = AF4 : Reserved 0x5 = AF5 : Reserved 0x6 = AF6 : Reserved 0x7 = AF7 : SPI0_D2 0x8 = AF8 : MA7 0x9 = AF9 : MAD7 0xA = AF10 : TM20_OC1H 0xB = AF11 : URT0_NSS ADC ~ ADC_I7 (IO mode set AIO & input to ADC macro)	
11..10	rw	**PA_FDIV7**	PA7 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	**PA_ODC7**	PA7 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	**Reserved**	Reserved	0x00
7	rw	**PA_INV7**	PA7 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	**Reserved**	Reserved	0x00
5	rw	**PA_PU7**	PA7 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	**Reserved**	Reserved	0x00
3	rw	**PA_HS7**	PA7 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	**PA_IOM7**	PA7 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.9. PA8 IO control register

PA_CR8	PA8 IO control register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PA_AFS8[3:0]				PA_FDIV8[1:0]		PA_ODC8	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PA_INV8	Reserved	PA_PU8	Reserved	PA_HS8	PA_IOM8[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..12	rw	**PA_AFS8**	PA8 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA8 0x1 = AF1 : DMA_TRG0	0x00

Bit	Attr	Bit Name	Description	Reset
			0x2 = AF2 : Reserved 0x3 = AF3 : I2C0_SCL 0x4 = AF4 : URT2_BRO 0x5 = AF5 : SDT_I0 0x6 = AF6 : TM20_IC0 0x7 = AF7 : SPI0_NSS 0x8 = AF8 : MA8 0x9 = AF9 : MAD0 0xA = AF10 : TM36_OC0H 0xB = AF11 : URT4_TX ADC ~ ADC_I8 (IO mode set AIO & input to ADC macro) CMP ~ CMP0_I0 (IO mode set AIO & input to CMP macro) ANA ~ VBG_OUT (IO mode set AIO & connect to Analog macro)	
11..10	rw	**PA_FDIV8**	PA8 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	**PA_ODC8**	PA8 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	**Reserved**	Reserved	0x00
7	rw	**PA_INV8**	PA8 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	**Reserved**	Reserved	0x00
5	rw	**PA_PU8**	PA8 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	**Reserved**	Reserved	0x00
3	rw	**PA_HS8**	PA8 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	**PA_IOM8**	PA8 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.10. PA9 IO control register

PA_CR9	PA9 IO control register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PA_AFS9[3:0]				PA_FDIV9[1:0]		PA_ODC9	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PA_INV9	Reserved	PA_PU9	Reserved	PA_HS9	PA_IOM9[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..12	rw	**PA_AFS9**	PA9 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA9 0x1 = AF1 : DMA_TRG1	0x00

			0x2 = AF2 : Reserved 0x3 = AF3 : I2C1_SCL 0x4 = AF4 : URT2_TMO 0x5 = AF5 : Reserved 0x6 = AF6 : TM20_IC1 0x7 = AF7 : SPI0_MISO 0x8 = AF8 : MA9 0x9 = AF9 : MAD1 0xA = AF10 : TM36_OC1H 0xB = AF11 : URT5_TX ADC ~ ADC_I9 (IO mode set AIO & input to ADC macro) CMP ~ CMP0_I1 (IO mode set AIO & input to CMP macro)	
11..10	rw	PA_FDIV9	PA9 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PA_ODC9	PA9 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PA_INV9	PA9 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PA_PU9	PA9 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PA_HS9	PA9 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PA_IOM9	PA9 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.11. PA10 IO control register

PA_CR10	PA10 IO control register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PA_AFS10[3:0]				PA_FDIV10[1:0]		PA_ODC10	Reserved
7	6	5	4	3	2	1	0
PA_INV10	Reserved	PA_PU10	Reserved	PA_HS10	PA_IOM10[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PA_AFS10	PA10 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA10 0x1 = AF1 : TM36_BK0 0x2 = AF2 : SPI0_D2 0x3 = AF3 : I2C0_SDA	0x00

			0x4 = AF4 : URT2_CTS 0x5 = AF5 : SDT_I1 0x6 = AF6 : TM26_IC0 0x7 = AF7 : SPI0_CLK 0x8 = AF8 : MA10 0x9 = AF9 : MAD2 0xA = AF10 : TM36_OC2H 0xB = AF11 : URT4_RX ADC ~ ADC_I10 (IO mode set AIO & input to ADC macro) CMP ~ CMP1_I0 (IO mode set AIO & input to CMP macro) ANA ~ ADC_PGA (IO mode set AIO & connect to Analog macro)	
11..10	rw	**PA_FDIV10**	PA10 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	**PA_ODC10**	PA10 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	**Reserved**	Reserved	0x00
7	rw	**PA_INV10**	PA10 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	**Reserved**	Reserved	0x00
5	rw	**PA_PU10**	PA10 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	**Reserved**	Reserved	0x00
3	rw	**PA_HS10**	PA10 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	**PA_IOM10**	PA10 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.12. PA11 IO control register

PA_CR11	PA11 IO control register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PA_AFS11[3:0]				PA_FDIV11[1:0]		PA_ODC11	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PA_INV11	Reserved	PA_PU11	Reserved	PA_HS11	PA_IOM11[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..12	rw	**PA_AFS11**	PA11 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA11 0x1 = AF1 : DAC_TRG0 0x2 = AF2 : SPI0_D3 0x3 = AF3 : I2C1_SDA	0x00

			0x4 = AF4 : URT2_RTS 0x5 = AF5 : Reserved 0x6 = AF6 : TM26_IC1 0x7 = AF7 : SPI0_MOSI 0x8 = AF8 : MA11 0x9 = AF9 : MAD3 0xA = AF10 : TM36_OC3H 0xB = AF11 : URT5_RX ADC ~ ADC_I11 (IO mode set AIO & input to ADC macro) CMP ~ CMP1_I1 (IO mode set AIO & input to CMP macro)	
11..10	rw	**PA_FDIV11**	PA11 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	**PA_ODC11**	PA11 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	**Reserved**	Reserved	0x00
7	rw	**PA_INV11**	PA11 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	**Reserved**	Reserved	0x00
5	rw	**PA_PU11**	PA11 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	**Reserved**	Reserved	0x00
3	rw	**PA_HS11**	PA11 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	**PA_IOM11**	PA11 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.13. PA12 IO control register

PA_CR12	PA12 IO control register
Offset Address : 0x30	Reset Value : 0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PA_AFS12[3:0]				PA_FDIV12[1:0]		PA_ODC12	Reserved
7	6	5	4	3	2	1	0
PA_INV12	Reserved	PA_PU12	Reserved	PA_HS12	PA_IOM12[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..12	rw	**PA_AFS12**	PA12 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA12 0x1 = AF1 : Reserved 0x2 = AF2 : USB_S0 0x3 = AF3 : Reserved 0x4 = AF4 : URT1_BRO 0x5 = AF5 : TM10_ETR	0x00

			0x6 = AF6 : TM36_IC0 0x7 = AF7 : SPI0_D5 0x8 = AF8 : MA12 0x9 = AF9 : MAD4 0xA = AF10 : TM26_OC00 0xB = AF11 : URT6_TX ADC ~ ADC_I12 (IO mode set AIO & input to ADC macro)	
11..10	rw	**PA_FDIV12**	PA12 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	**PA_ODC12**	PA12 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	**Reserved**	Reserved	0x00
7	rw	**PA_INV12**	PA12 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	**Reserved**	Reserved	0x00
5	rw	**PA_PU12**	PA12 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	**Reserved**	Reserved	0x00
3	rw	**PA_HS12**	PA12 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	**PA_IOM12**	PA12 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.14. PA13 IO control register

PA_CR13	PA13 IO control register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PA_AFS13[3:0]				PA_FDIV13[1:0]		PA_ODC13	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PA_INV13	Reserved	PA_PU13	Reserved	PA_HS13	PA_IOM13[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..12	rw	**PA_AFS13**	PA13 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA13 0x1 = AF1 : CPU_TXEV 0x2 = AF2 : USB_S1 0x3 = AF3 : URT0_BRO 0x4 = AF4 : URT1_TMO 0x5 = AF5 : TM10_TRGO 0x6 = AF6 : TM36_IC1 0x7 = AF7 : SPI0_D6 0x8 = AF8 : MA13	0x00

			0x9 = AF9 : MAD5 0xA = AF10 : TM26_OC10 0xB = AF11 : URT6_RX ADC ~ ADC_I13 (IO mode set AIO & input to ADC macro)	
11..10	rw	PA_FDIV13	PA13 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PA_ODC13	PA13 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PA_INV13	PA13 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PA_PU13	PA13 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PA_HS13	PA13 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PA_IOM13	PA13 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.15. PA14 IO control register

PA_CR14	PA14 IO control register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PA_AFS14[3:0]				PA_FDIV14[1:0]		PA_ODC14	Reserved
7	6	5	4	3	2	1	0
PA_INV14	Reserved	PA_PU14	Reserved	PA_HS14	PA_IOM14[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PA_AFS14	PA14 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA14 0x1 = AF1 : CPU_RXEV 0x2 = AF2 : OBM_I0 0x3 = AF3 : URT0_TMO 0x4 = AF4 : URT1_CTS 0x5 = AF5 : TM16_ETR 0x6 = AF6 : TM36_IC2 0x7 = AF7 : SPI0_D7 0x8 = AF8 : MA14 0x9 = AF9 : MAD6 0xA = AF10 : TM26_OC0H 0xB = AF11 : URT7_TX	0x00

			ADC ~ ADC_I14 (IO mode set AIO & input to ADC macro)	
11..10	rw	**PA_FDIV14**	PA14 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	**PA_ODC14**	PA14 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	**Reserved**	Reserved	0x00
7	rw	**PA_INV14**	PA14 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	**Reserved**	Reserved	0x00
5	rw	**PA_PU14**	PA14 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	**Reserved**	Reserved	0x00
3	rw	**PA_HS14**	PA14 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	**PA_IOM14**	PA14 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.16. PA15 IO control register

PA_CR15	**PA15 IO control register**		
Offset Address :	**0x3C**	**Reset Value :**	**0x00000000**

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PA_AFS15[3:0]				**PA_FDIV15[1:0]**		**PA_ODC15**	**Reserved**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PA_INV15	**Reserved**	**PA_PU15**	**Reserved**	**PA_HS15**	**PA_IOM15[2:0]**		

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..12	rw	**PA_AFS15**	PA15 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPA15 0x1 = AF1 : CPU_NMI 0x2 = AF2 : OBM_I1 0x3 = AF3 : URT0_DE 0x4 = AF4 : URT1_RTS 0x5 = AF5 : TM16_TRGO 0x6 = AF6 : TM36_IC3 0x7 = AF7 : SPI0_D4 0x8 = AF8 : MA15 0x9 = AF9 : MAD7 0xA = AF10 : TM26_OC1H 0xB = AF11 : URT7_RX ADC ~ ADC_I15 (IO mode set AIO & input to ADC macro)	0x00
11..10	rw	**PA_FDIV15**	PA15 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter	0x00

			0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	
9	rw	PA_ODC15	PA15 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PA_INV15	PA15 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PA_PU15	PA15 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PA_HS15	PA15 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PA_IOM15	PA15 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.2.17. PA port input filter control register

PA_FLT	PA port input filter control register		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		Reserved			PA_FCKS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5..3	-	Reserved	Reserved	0x00
2..0	rw	PA_FCKS	PA port input deglitch filter clock source select for all pins of the port. 0x0 = CLK_AHB 0x1 = CLK_AHB_Div8 : CLK_AHB divide by 8 0x2 = CLK_ILRCO 0x3 = TM00_TRGO 0x4 = CK_UT	0x00

1.2.18. PA Register Map

PA Register Map **Register Number = 17**

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	PA_CR0	Reserved																PA_AFS0[3:0]				PA_FDIV0[1:0]		PA_ODC0	Reserved	PA_INV0	Reserved	PA_PU0	Reserved	PA_HS0	PA_IOM0[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	PA_CR1	Reserved																PA_AFS1[3:0]				PA_FDIV1[1:0]		PA_ODC1	Reserved	PA_INV1	Reserved	PA_PU1	Reserved	PA_HS1	PA_IOM1[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	PA_CR2	Reserved																PA_AFS2[3:0]				PA_FDIV2[1:0]		PA_ODC2	Reserved	PA_INV2	Reserved	PA_PU2	Reserved	PA_HS2	PA_IOM2[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	PA_CR3	Reserved																PA_AFS3[3:0]				PA_FDIV3[1:0]		PA_ODC3	Reserved	PA_INV3	Reserved	PA_PU3	Reserved	PA_HS3	PA_IOM3[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	PA_CR4	Reserved																PA_AFS4[3:0]				PA_FDIV4[1:0]		PA_ODC4	Reserved	PA_INV4	Reserved	PA_PU4	Reserved	PA_HS4	PA_IOM4[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	PA_CR5	Reserved																PA_AFS5[3:0]				PA_FDIV5[1:0]		PA_ODC5	Reserved	PA_INV5	Reserved	PA_PU5	Reserved	PA_HS5	PA_IOM5[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	PA_CR6	Reserved																PA_AFS6[3:0]				PA_FDIV6[1:0]		PA_ODC6	Reserved	PA_INV6	Reserved	PA_PU6	Reserved	PA_HS6	PA_IOM6[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	PA_CR7	Reserved																PA_AFS7[3:0]				PA_FDIV7[1:0]		PA_ODC7	Reserved	PA_INV7	Reserved	PA_PU7	Reserved	PA_HS7	PA_IOM7[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset	Register	31–16	15–12	11–10	9	8	7	6	5	4	3	2–0
0x20	PA_CR8	Reserved	PA_AFS8[3:0]	PA_FDIV8[1:0]	PA_ODC8	Reserved	PA_INV8	Reserved	PA_PU8	Reserved	PA_HS8	PA_IOM8[2:0]
Reset	0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0	0	0	0	0	0	0	0	0 0 0
0x24	PA_CR9	Reserved	PA_AFS9[3:0]	PA_FDIV9[1:0]	PA_ODC9	Reserved	PA_INV9	Reserved	PA_PU9	Reserved	PA_HS9	PA_IOM9[2:0]
Reset	0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0	0	0	0	0	0	0	0	0 0 0
0x28	PA_CR10	Reserved	PA_AFS10[3:0]	PA_FDIV10[1:0]	PA_ODC10	Reserved	PA_INV10	Reserved	PA_PU10	Reserved	PA_HS10	PA_IOM10[2:0]
Reset	0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0	0	0	0	0	0	0	0	0 0 0
0x2C	PA_CR11	Reserved	PA_AFS11[3:0]	PA_FDIV11[1:0]	PA_ODC11	Reserved	PA_INV11	Reserved	PA_PU11	Reserved	PA_HS11	PA_IOM11[2:0]
Reset	0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0	0	0	0	0	0	0	0	0 0 0
0x30	PA_CR12	Reserved	PA_AFS12[3:0]	PA_FDIV12[1:0]	PA_ODC12	Reserved	PA_INV12	Reserved	PA_PU12	Reserved	PA_HS12	PA_IOM12[2:0]
Reset	0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0	0	0	0	0	0	0	0	0 0 0
0x34	PA_CR13	Reserved	PA_AFS13[3:0]	PA_FDIV13[1:0]	PA_ODC13	Reserved	PA_INV13	Reserved	PA_PU13	Reserved	PA_HS13	PA_IOM13[2:0]
Reset	0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0	0	0	0	0	0	0	0	0 0 0
0x38	PA_CR14	Reserved	PA_AFS14[3:0]	PA_FDIV14[1:0]	PA_ODC14	Reserved	PA_INV14	Reserved	PA_PU14	Reserved	PA_HS14	PA_IOM14[2:0]
Reset	0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0	0	0	0	0	0	0	0	0 0 0
0x3C	PA_CR15	Reserved	PA_AFS15[3:0]	PA_FDIV15[1:0]	PA_ODC15	Reserved	PA_INV15	Reserved	PA_PU15	Reserved	PA_HS15	PA_IOM15[2:0]
Reset	0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0	0	0	0	0	0	0	0	0 0 0
0x40	PA_FLT	Reserved	Reserved				Reserved		Reserved			PA_FCKS[2:0]
Reset	0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0	0	0	0	0	0	0	0	0 0 0

1.3. Port B Configure Registers

Port B Configure	(PB) Port B IO Mode Configure
Base Address :	0x44010000

1.3.1. PB0 IO control register

PB_CR0	PB0 IO control register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PB_AFS0[3:0]				PB_FDIV0[1:0]		PB_ODC0[1:0]	
7	6	5	4	3	2	1	0
PB_INV0	Reserved	PB_PU0	Reserved	PB_HS0	PB_IOM0[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS0	PB0 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB0 0x1 = AF1 : I2C1_SCL 0x2 = AF2 : SPI0_NSS 0x3 = AF3 : TM01_ETR 0x4 = AF4 : TM00_CKO 0x5 = AF5 : TM16_ETR 0x6 = AF6 : TM26_IC0 0x7 = AF7 : TM36_ETR 0x8 = AF8 : MA15 0x9 = AF9 : URT1_NSS 0xA = AF10 : URT2_NSS 0xB = AF11 : URT6_TX CMP ~ CMP_C0 (IO mode set AIO & input to CMP macro)	0x00
11..10	rw	PB_FDIV0	PB0 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PB_ODC0	PB0 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PB_INV0	PB0 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PB_PU0	PB0 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS0	PB0 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM0	PB0 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output	0x00

			0x2 = PPO : push pull output 0x3 = DIN : Digital input	

1.3.2. PB1 IO control register

PB_CR1	PB1 IO control register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PB_AFS1[3:0]				PB_FDIV1[1:0]		PB_ODC1[1:0]	
7	6	5	4	3	2	1	0
PB_INV1	Reserved	PB_PU1	Reserved	PB_HS1	PB_IOM1[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS1	PB1 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB1 0x1 = AF1 : I2C1_SDA 0x2 = AF2 : SPI0_MISO 0x3 = AF3 : TM01_TRGO 0x4 = AF4 : TM10_CKO 0x5 = AF5 : TM16_TRGO 0x6 = AF6 : TM26_IC1 0x7 = AF7 : TM36_TRGO 0x8 = AF8 : Reserved 0x9 = AF9 : URT1_RX 0xA = AF10 : URT2_CLK 0xB = AF11 : URT6_RX CMP ~ CMP_C1 (IO mode set AIO & input to CMP macro)	0x00
11..10	rw	PB_FDIV1	PB1 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PB_ODC1	PB1 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PB_INV1	PB1 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PB_PU1	PB1 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS1	PB1 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM1	PB1 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.3. PB2 IO control register

PB_CR2	PB2 IO control register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PB_AFS2[3:0]				PB_FDIV2[1:0]		PB_ODC2[1:0]	
7	6	5	4	3	2	1	0
PB_INV2	Reserved	PB_PU2	Reserved	PB_HS2	PB_IOM2[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS2	PB2 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB2 0x1 = AF1 : ADC0_TRG 0x2 = AF2 : SPI0_CLK 0x3 = AF3 : TM01_CKO 0x4 = AF4 : URT2_TX 0x5 = AF5 : TM16_CKO 0x6 = AF6 : TM26_OC0H 0x7 = AF7 : I2C0_SDA 0x8 = AF8 : Reserved 0x9 = AF9 : URT1_CLK 0xA = AF10 : URT0_TX 0xB = AF11 : URT7_TX ANA ~ DAC_P0 (IO mode set AIO & connect to Analog macro)	0x00
11..10	rw	PB_FDIV2	PB2 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PB_ODC2	PB2 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PB_INV2	PB2 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PB_PU2	PB2 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS2	PB2 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM2	PB2 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.4. PB3 IO control register

PB_CR3	PB3 IO control register		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PB_AFS3[3:0]				PB_FDIV3[1:0]		PB_ODC3[1:0]	
7	6	5	4	3	2	1	0
PB_INV3	Reserved	PB_PU3	Reserved	PB_HS3	PB_IOM3[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS3	PB3 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB3 0x1 = AF1 : ADC0_OUT 0x2 = AF2 : SPI0_MOSI 0x3 = AF3 : NCO_P0 0x4 = AF4 : URT2_RX 0x5 = AF5 : TM36_CKO 0x6 = AF6 : TM26_OC1H 0x7 = AF7 : I2C0_SCL 0x8 = AF8 : Reserved 0x9 = AF9 : URT1_TX 0xA = AF10 : URT0_RX 0xB = AF11 : URT7_RX	0x00
11..10	rw	PB_FDIV3	PB3 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PB_ODC3	PB3 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PB_INV3	PB3 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PB_PU3	PB3 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS3	PB3 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM3	PB3 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.5. PB4 IO control register

PB_CR4	PB4 IO control register		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PB_AFS4[3:0]				PB_FDIV4[1:0]		PB_ODC4[1:0]	
7	6	5	4	3	2	1	0
PB_INV4	Reserved	PB_PU4	Reserved	PB_HS4	PB_IOM4[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS4	PB4 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB4 0x1 = AF1 : TM01_CKO 0x2 = AF2 : SPI0_D3 0x3 = AF3 : TM26_TRGO 0x4 = AF4 : URT2_CLK 0x5 = AF5 : TM20_IC0 0x6 = AF6 : TM36_IC0 0x7 = AF7 : Reserved 0x8 = AF8 : MALE 0x9 = AF9 : MAD8 0xA = AF10 : Reserved 0xB = AF11 : Reserved	0x00
11..10	rw	PB_FDIV4	PB4 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PB_ODC4	PB4 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PB_INV4	PB4 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PB_PU4	PB4 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS4	PB4 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM4	PB4 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.6. PB5 IO control register

PB_CR5	PB5 IO control register		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16

Reserved							
15	14	13	12	11	10	9	8
PB_AFS5[3:0]				PB_FDIV5[1:0]		PB_ODC5[1:0]	
7	6	5	4	3	2	1	0
PB_INV5	Reserved	PB_PU5	Reserved	PB_HS5	PB_IOM5[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS5	PB5 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB5 0x1 = AF1 : TM16_CKO 0x2 = AF2 : SPI0_D2 0x3 = AF3 : TM26_ETR 0x4 = AF4 : URT2_NSS 0x5 = AF5 : TM20_IC1 0x6 = AF6 : TM36_IC1 0x7 = AF7 : Reserved 0x8 = AF8 : MOE 0x9 = AF9 : MAD9 0xA = AF10 : Reserved 0xB = AF11 : Reserved	0x00
11..10	rw	PB_FDIV5	PB5 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PB_ODC5	PB5 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PB_INV5	PB5 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PB_PU5	PB5 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS5	PB5 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM5	PB5 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.7. PB6 IO control register

PB_CR6	PB6 IO control register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PB_AFS6[3:0]				PB_FDIV6[1:0]		PB_ODC6	Reserved

7	6	5	4	3	2	1	0
PB_INV6	Reserved	PB_PU6	Reserved	PB_HS6	PB_IOM6[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS6	PB6 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB6 0x1 = AF1 : CPU_RXEV 0x2 = AF2 : SPI0_NSSI 0x3 = AF3 : URT0_BRO 0x4 = AF4 : URT2_CTS 0x5 = AF5 : TM20_ETR 0x6 = AF6 : TM36_IC2 0x7 = AF7 : Reserved 0x8 = AF8 : MWE 0x9 = AF9 : MAD10 0xA = AF10 : Reserved 0xB = AF11 : URT2_TX	0x00
11..10	rw	PB_FDIV6	PB6 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PB_ODC6	PB6 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PB_INV6	PB6 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PB_PU6	PB6 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS6	PB6 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM6	PB6 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.8. PB7 IO control register

PB_CR7	PB7 IO control register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PB_AFS7[3:0]				PB_FDIV7[1:0]		PB_ODC7	Reserved
7	6	5	4	3	2	1	0
PB_INV7	Reserved	PB_PU7	Reserved	PB_HS7	PB_IOM7[2:0]		

Bit	Attr	Bit Name	Description	Reset

31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS7	PB7 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB7 0x1 = AF1 : CPU_TXEV 0x2 = AF2 : Reserved 0x3 = AF3 : URT0_TMO 0x4 = AF4 : URT2_RTS 0x5 = AF5 : TM20_TRGO 0x6 = AF6 : TM36_IC3 0x7 = AF7 : Reserved 0x8 = AF8 : MCE 0x9 = AF9 : MALE2 0xA = AF10 : Reserved 0xB = AF11 : URT2_RX	0x00
11..10	rw	PB_FDIV7	PB7 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PB_ODC7	PB7 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PB_INV7	PB7 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PB_PU7	PB7 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS7	PB7 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM7	PB7 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.9. PB8 IO control register

PB_CR8	PB8 IO control register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PB_AFS8[3:0]				PB_FDIV8[1:0]		PB_ODC8[1:0]	
7	6	5	4	3	2	1	0
PB_INV8	Reserved	PB_PU8	Reserved	PB_HS8	PB_IOM8[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS8	PB8 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB8	0x00

Bit	Attr	Bit Name	Description	Reset
			0x1 = AF1 : CMP0_P0 0x2 = AF2 : RTC_OUT 0x3 = AF3 : URT0_TX 0x4 = AF4 : URT2_BRO 0x5 = AF5 : TM20_OC01 0x6 = AF6 : TM36_OC01 0x7 = AF7 : SPI0_D3 0x8 = AF8 : MAD0 0x9 = AF9 : SDT_P0 0xA = AF10 : OBM_P0 0xB = AF11 : URT4_TX	
11..10	rw	PB_FDIV8	PB8 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PB_ODC8	PB8 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PB_INV8	PB8 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PB_PU8	PB8 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS8	PB8 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM8	PB8 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.10. PB9 IO control register

PB_CR9	PB9 IO control register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PB_AFS9[3:0]				PB_FDIV9[1:0]		PB_ODC9[1:0]	
7	6	5	4	3	2	1	0
PB_INV9	Reserved	PB_PU9	Reserved	PB_HS9	PB_IOM9[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS9	PB9 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB9 0x1 = AF1 : CMP1_P0 0x2 = AF2 : RTC_TS 0x3 = AF3 : URT0_RX	0x00

			0x4 = AF4 : URT2_TMO 0x5 = AF5 : TM20_OC02 0x6 = AF6 : TM36_OC02 0x7 = AF7 : SPI0_D2 0x8 = AF8 : MAD1 0x9 = AF9 : MAD8 0xA = AF10 : OBM_P1 0xB = AF11 : URT4_RX	
11..10	rw	**PB_FDIV9**	PB9 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	**PB_ODC9**	PB9 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	**PB_INV9**	PB9 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	**Reserved**	Reserved	0x00
5	rw	**PB_PU9**	PB9 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	**Reserved**	Reserved	0x00
3	rw	**PB_HS9**	PB9 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	**PB_IOM9**	PB9 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.11. PB10 IO control register

PB_CR10	PB10 IO control register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PB_AFS10[3:0]				PB_FDIV10[1:0]		PB_ODC10	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PB_INV10	Reserved	PB_PU10	Reserved	PB_HS10	PB_IOM10[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..12	rw	**PB_AFS10**	PB10 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB10 0x1 = AF1 : Reserved 0x2 = AF2 : I2C0_SCL 0x3 = AF3 : URT0_NSS 0x4 = AF4 : URT2_DE 0x5 = AF5 : TM20_OC11 0x6 = AF6 : TM36_OC11	0x00

			0x7 = AF7 : URT1_TX 0x8 = AF8 : MAD2 0x9 = AF9 : MAD1 0xA = AF10 : SPI0_NSSI 0xB = AF11 : Reserved	
11..10	rw	**PB_FDIV10**	PB10 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	**PB_ODC10**	PB10 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	**Reserved**	Reserved	0x00
7	rw	**PB_INV10**	PB10 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	**Reserved**	Reserved	0x00
5	rw	**PB_PU10**	PB10 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	**Reserved**	Reserved	0x00
3	rw	**PB_HS10**	PB10 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	**PB_IOM10**	PB10 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.12. PB11 IO control register

PB_CR11	PB11 IO control register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PB_AFS11[3:0]				PB_FDIV11[1:0]		PB_ODC11	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PB_INV11	Reserved	PB_PU11	Reserved	PB_HS11	PB_IOM11[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..12	rw	**PB_AFS11**	PB11 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB11 0x1 = AF1 : Reserved 0x2 = AF2 : I2C0_SDA 0x3 = AF3 : URT0_DE 0x4 = AF4 : IR_OUT 0x5 = AF5 : TM20_OC12 0x6 = AF6 : TM36_OC12 0x7 = AF7 : URT1_RX 0x8 = AF8 : MAD3 0x9 = AF9 : MAD9 0xA = AF10 : DMA_TRG0	0x00

			0xB = AF11 : URT0_CLK	
11..10	rw	PB_FDIV11	PB11 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PB_ODC11	PB11 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PB_INV11	PB11 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PB_PU11	PB11 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS11	PB11 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM11	PB11 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.13. PB12 IO control register

PB_CR12	PB12 IO control register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PB_AFS12[3:0]				PB_FDIV12[1:0]		PB_ODC12	Reserved
7	6	5	4	3	2	1	0
PB_INV12	Reserved	PB_PU12	Reserved	PB_HS12	PB_IOM12[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS12	PB12 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB12 0x1 = AF1 : DMA_TRG0 0x2 = AF2 : NCO_P0 0x3 = AF3 : USB_S0 0x4 = AF4 : Reserved 0x5 = AF5 : Reserved 0x6 = AF6 : Reserved 0x7 = AF7 : URT1_CLK 0x8 = AF8 : MAD4 0x9 = AF9 : MAD2 0xA = AF10 : Reserved 0xB = AF11 : URT5_TX	0x00
11..10	rw	PB_FDIV12	PB12 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1	0x00

Bit	Attr	Bit Name	Description	Reset
			0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	
9	rw	PB_ODC12	PB12 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PB_INV12	PB12 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PB_PU12	PB12 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS12	PB12 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM12	PB12 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.14. PB13 IO control register

PB_CR13	PB13 IO control register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PB_AFS13[3:0]				PB_FDIV13[1:0]		PB_ODC13	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PB_INV13	Reserved	PB_PU13	Reserved	PB_HS13	PB_IOM13[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS13	PB13 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB13 0x1 = AF1 : DAC_TRG0 0x2 = AF2 : TM00_ETR 0x3 = AF3 : URT0_CTS 0x4 = AF4 : Reserved 0x5 = AF5 : TM20_ETR 0x6 = AF6 : TM36_ETR 0x7 = AF7 : URT0_CLK 0x8 = AF8 : MAD5 0x9 = AF9 : MAD10 0xA = AF10 : CCL_P0 0xB = AF11 : URT4_RX	0x00
11..10	rw	PB_FDIV13	PB13 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PB_ODC13	PB13 pin output drive strength select. 0x0 = Level0 : Drive strength-full	0x00

			0x1 = Level2 : Drive strength-1/4	
8	-	Reserved	Reserved	0x00
7	rw	PB_INV13	PB13 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PB_PU13	PB13 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS13	PB13 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM13	PB13 pin IO mode control bits. This pin is using the crystal pad and is fixed output drive strength. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.15. PB14 IO control register

PB_CR14	PB14 IO control register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PB_AFS14[3:0]				PB_FDIV14[1:0]		PB_ODC14	Reserved
7	6	5	4	3	2	1	0
PB_INV14	Reserved	PB_PU14	Reserved	PB_HS14	PB_IOM14[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS14	PB14 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB14 0x1 = AF1 : DMA_TRG0 0x2 = AF2 : TM00_TRGO 0x3 = AF3 : URT0_RTS 0x4 = AF4 : Reserved 0x5 = AF5 : TM20_TRGO 0x6 = AF6 : TM36_BK0 0x7 = AF7 : URT0_NSS 0x8 = AF8 : MAD6 0x9 = AF9 : MAD3 0xA = AF10 : CCL_P1 0xB = AF11 : URT4_TX	0x00
11..10	rw	PB_FDIV14	PB14 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PB_ODC14	PB14 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PB_INV14	PB14 pin input inverse enable bit.	0x00

			0 = Disable 1 = Enable	
6	-	Reserved	Reserved	0x00
5	rw	PB_PU14	PB14 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS14	PB14 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM14	PB14 pin IO mode control bits. This pin is using the crystal pad and is fixed output drive strength. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.16. PB15 IO control register

PB_CR15	PB15 IO control register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PB_AFS15[3:0]				PB_FDIV15[1:0]		PB_ODC15	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PB_INV15	Reserved	PB_PU15	Reserved	PB_HS15	PB_IOM15[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PB_AFS15	PB15 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPB15 0x1 = AF1 : IR_OUT 0x2 = AF2 : NCO_CK0 0x3 = AF3 : USB_S1 0x4 = AF4 : Reserved 0x5 = AF5 : Reserved 0x6 = AF6 : Reserved 0x7 = AF7 : URT1_NSS 0x8 = AF8 : MAD7 0x9 = AF9 : MAD11 0xA = AF10 : Reserved 0xB = AF11 : URT5_RX	0x00
11..10	rw	PB_FDIV15	PB15 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PB_ODC15	PB15 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PB_INV15	PB15 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00

5	rw	PB_PU15	PB15 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PB_HS15	PB15 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PB_IOM15	PB15 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.3.17. PB port input filter control register

PB_FLT	PB port input filter control register		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		Reserved			PB_FCKS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5..3	-	Reserved	Reserved	0x00
2..0	rw	PB_FCKS	PB port input deglitch filter clock source select for all pins of the port. 0x0 = CLK_AHB 0x1 = CLK_AHB_Div8 : CLK_AHB divide by 8 0x2 = CLK_ILRCO 0x3 = TM00_TRGO 0x4 = CK_UT	0x00

1.3.18. PB Register Map

PB Register Map Register Number = 17

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	PB_CR0	Reserved																PB_AFS0[3:0]				PB_FDIV0[1:0]		PB_ODC0[1:0]		PB_INV0	Reserved	PB_PU0	Reserved	PB_HS0	PB_IOM0[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	PB_CR1	Reserved																PB_AFS1[3:0]				PB_FDIV1[1:0]		PB_ODC1[1:0]		PB_INV1	Reserved	PB_PU1	Reserved	PB_HS1	PB_IOM1[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	PB_CR2	Reserved																PB_AFS2[3:0]				PB_FDIV2[1:0]		PB_ODC2[1:0]		PB_INV2	Reserved	PB_PU2	Reserved	PB_HS2	PB_IOM2[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	PB_CR3	Reserved																PB_AFS3[3:0]				PB_FDIV3[1:0]		PB_ODC3[1:0]		PB_INV3	Reserved	PB_PU3	Reserved	PB_HS3	PB_IOM3[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	PB_CR4	Reserved																PB_AFS4[3:0]				PB_FDIV4[1:0]		PB_ODC4[1:0]		PB_INV4	Reserved	PB_PU4	Reserved	PB_HS4	PB_IOM4[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	PB_CR5	Reserved																PB_AFS5[3:0]				PB_FDIV5[1:0]		PB_ODC5[1:0]		PB_INV5	Reserved	PB_PU5	Reserved	PB_HS5	PB_IOM5[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	PB_CR6	Reserved																PB_AFS6[3:0]				PB_FDIV6[1:0]		PB_ODC6	Reserved	PB_INV6	Reserved	PB_PU6	Reserved	PB_HS6	PB_IOM6[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	PB_CR7	Reserved																PB_AFS7[3:0]				PB_FDIV7[1:0]		PB_ODC7	Reserved	PB_INV7	Reserved	PB_PU7	Reserved	PB_HS7	PB_IOM7[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x20	PB_CR8	Reserved																PB_AFS8[3:0]				PB_FDIV8[1:0]		PB_ODC8[1:0]		PB_INV8	Reserved	PB_PU8	Reserved	PB_HS8	PB_IOM8[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	PB_CR9	Reserved																PB_AFS9[3:0]				PB_FDIV9[1:0]		PB_ODC9[1:0]		PB_INV9	Reserved	PB_PU9	Reserved	PB_HS9	PB_IOM9[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	PB_CR10	Reserved																PB_AFS10[3:0]				PB_FDIV10[1:0]		PB_ODC10	Reserved	PB_INV10	Reserved	PB_PU10	Reserved	PB_HS10	PB_IOM10[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	PB_CR11	Reserved																PB_AFS11[3:0]				PB_FDIV11[1:0]		PB_ODC11	Reserved	PB_INV11	Reserved	PB_PU11	Reserved	PB_HS11	PB_IOM11[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	PB_CR12	Reserved																PB_AFS12[3:0]				PB_FDIV12[1:0]		PB_ODC12	Reserved	PB_INV12	Reserved	PB_PU12	Reserved	PB_HS12	PB_IOM12[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	PB_CR13	Reserved																PB_AFS13[3:0]				PB_FDIV13[1:0]		PB_ODC13	Reserved	PB_INV13	Reserved	PB_PU13	Reserved	PB_HS13	PB_IOM13[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	PB_CR14	Reserved																PB_AFS14[3:0]				PB_FDIV14[1:0]		PB_ODC14	Reserved	PB_INV14	Reserved	PB_PU14	Reserved	PB_HS14	PB_IOM14[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	PB_CR15	Reserved																PB_AFS15[3:0]				PB_FDIV15[1:0]		PB_ODC15	Reserved	PB_INV15	Reserved	PB_PU15	Reserved	PB_HS15	PB_IOM15[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	PB_FLT	Reserved																Reserved								Reserved		Reserved			PB_FCKS[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.4. Port C Configure Registers

Port C Configure	(PC) Port C IO Mode Configure
Base Address :	0x44020000

1.4.1. PC0 IO control register

PC_CR0	PC0 IO control register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS0[3:0]				PC_FDIV0[1:0]		PC_ODC0	Reserved
7	6	5	4	3	2	1	0
PC_INV0	Reserved	PC_PU0	Reserved	PC_HS0	PC_IOM0[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PC_AFS0	PC0 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPC0 0x1 = AF1 : ICKO 0x2 = AF2 : TM00_CKO 0x3 = AF3 : URT0_CLK 0x4 = AF4 : URT2_CLK 0x5 = AF5 : TM20_OC00 0x6 = AF6 : TM36_OC00 0x7 = AF7 : I2C0_SCL 0x8 = AF8 : MCLK 0x9 = AF9 : MWE 0xA = AF10 : URT0_TX 0xB = AF11 : URT5_TX	0x00
11..10	rw	PC_FDIV0	PC0 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PC_ODC0	PC0 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV0	PC0 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU0	PC0 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PC_HS0	PC0 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM0	PC0 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

			0x4 = QB : Quasi-Bidirectional output drive high one CLK	

1.4.2. PC1 IO control register

PC_CR1	PC1 IO control register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS1[3:0]				PC_FDIV1[1:0]		PC_ODC1	Reserved
7	6	5	4	3	2	1	0
PC_INV1	Reserved	PC_PU1	Reserved	PC_HS1	PC_IOM1[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PC_AFS1	PC1 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPC1 0x1 = AF1 : ADC0_TRG 0x2 = AF2 : TM01_CKO 0x3 = AF3 : TM36_IC0 0x4 = AF4 : URT1_CLK 0x5 = AF5 : TM20_OC0N 0x6 = AF6 : TM36_OC0N 0x7 = AF7 : I2C0_SDA 0x8 = AF8 : MAD8 0x9 = AF9 : MAD4 0xA = AF10 : URT0_RX 0xB = AF11 : URT5_RX	0x00
11..10	rw	PC_FDIV1	PC1 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PC_ODC1	PC1 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV1	PC1 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU1	PC1 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PC_HS1	PC1 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM1	PC1 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	0x00

1.4.3. PC2 IO control register

PC_CR2	PC2 IO control register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS2[3:0]				PC_FDIV2[1:0]		PC_ODC2	Reserved
7	6	5	4	3	2	1	0
PC_INV2	Reserved	PC_PU2	Reserved	PC_HS2	PC_IOM2[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PC_AFS2	PC2 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPC2 0x1 = AF1 : ADC0_OUT 0x2 = AF2 : TM10_CKO 0x3 = AF3 : OBM_P0 0x4 = AF4 : URT2_CLK 0x5 = AF5 : TM20_OC10 0x6 = AF6 : TM36_OC10 0x7 = AF7 : SDT_I0 0x8 = AF8 : MAD9 0x9 = AF9 : MAD12 0xA = AF10 : Reserved 0xB = AF11 : Reserved	0x00
11..10	rw	PC_FDIV2	PC2 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PC_ODC2	PC2 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV2	PC2 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU2	PC2 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PC_HS2	PC2 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM2	PC2 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	0x000

1.4.4. PC3 IO control register

PC_CR3	PC3 IO control register

Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS3[3:0]				PC_FDIV3[1:0]		PC_ODC3	Reserved
7	6	5	4	3	2	1	0
PC_INV3	Reserved	PC_PU3	Reserved	PC_HS3	PC_IOM3[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PC_AFS3	PC3 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPC3 0x1 = AF1 : OBM_P1 0x2 = AF2 : TM16_CKO 0x3 = AF3 : URT0_CLK 0x4 = AF4 : URT1_CLK 0x5 = AF5 : TM20_OC1N 0x6 = AF6 : TM36_OC1N 0x7 = AF7 : SDT_I1 0x8 = AF8 : MAD10 0x9 = AF9 : MAD5 0xA = AF10 : Reserved 0xB = AF11 : Reserved	0x00
11..10	rw	PC_FDIV3	PC3 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PC_ODC3	PC3 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV3	PC3 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU3	PC3 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PC_HS3	PC3 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM3	PC3 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	0x00

1.4.5. PC4 IO control register

PC_CR4	PC4 IO control register		
Offset Address :	0x10	Reset Value :	0x00000024

31	30	29	28	27	26	25	24

PC_LCK4	Reserved						
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS4[3:0]				PC_FDIV4[1:0]		PC_ODC4	Reserved
7	6	5	4	3	2	1	0
PC_INV4	Reserved	PC_PU4	Reserved	PC_HS4	PC_IOM4[2:0]		

Bit	Attr	Bit Name	Description	Reset
31	rw	PC_LCK4	PC4 pin control register write un-locked control. When locked, disables the register PC_AFS4 write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	0x00
30..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..12	rw	PC_AFS4	PC4 pin alternate function select. Refer the GPIO AFS table for detail information. This register default value is affected by the hardware configure register CFG_SWD_PIN after chip reset. 0x0 = AF0 : GPC4 0x1 = AF1 : SWCLK 0x2 = AF2 : I2C0_SCL 0x3 = AF3 : URT0_RX 0x4 = AF4 : URT1_RX 0x5 = AF5 : Reserved 0x6 = AF6 : TM36_OC2 0x7 = AF7 : SDT_I0 0x8 = AF8 : Reserved 0x9 = AF9 : Reserved 0xA = AF10 : Reserved 0xB = AF11 : URT6_RX	0x00
11..10	rw	PC_FDIV4	PC4 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PC_ODC4	PC4 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV4	PC4 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU4	PC4 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x01
4	-	Reserved	Reserved	0x00
3	rw	PC_HS4	PC4 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM4	PC4 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	0x04

1.4.6. PC5 IO control register

PC_CR5	PC5 IO control register		
Offset Address :	0x14	Reset Value :	0x00000024

31	30	29	28	27	26	25	24
PC_LCK5	Reserved						
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS5[3:0]				PC_FDIV5[1:0]		PC_ODC5	Reserved
7	6	5	4	3	2	1	0
PC_INV5	Reserved	PC_PU5	Reserved	PC_HS5	PC_IOM5[2:0]		

Bit	Attr	Bit Name	Description	Reset
31	rw	PC_LCK5	PC5 pin control register write un-locked control. When locked, disables the register PC_AFS5 write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	0x00
30..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..12	rw	PC_AFS5	PC5 pin alternate function select. Refer the GPIO AFS table for detail information. This register default value is affected by the hardware configure register CFG_SWD_PIN after chip reset. 0x0 = AF0 : GPC5 0x1 = AF1 : SWDIO 0x2 = AF2 : I2C0_SDA 0x3 = AF3 : URT0_TX 0x4 = AF4 : URT1_TX 0x5 = AF5 : Reserved 0x6 = AF6 : TM36_OC3 0x7 = AF7 : SDT_I1 0x8 = AF8 : Reserved 0x9 = AF9 : Reserved 0xA = AF10 : Reserved 0xB = AF11 : URT6_TX	0x00
11..10	rw	PC_FDIV5	PC5 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PC_ODC5	PC5 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV5	PC5 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU5	PC5 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x01
4	-	Reserved	Reserved	0x00
3	rw	PC_HS5	PC5 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM5	PC5 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x04

			0x4 = QB : Quasi-Bidirectional output drive high one CLK	

1.4.7. PC6 IO control register

PC_CR6	PC6 IO control register		
Offset Address :	0x18	Reset Value :	0x00000024

31	30	29	28	27	26	25	24
PC_LCK6	Reserved						
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS6[3:0]				PC_FDIV6[1:0]		Reserved	Reserved
7	6	5	4	3	2	1	0
PC_INV6	Reserved	PC_PU6	Reserved	PC_HS6	PC_IOM6[2:0]		

Bit	Attr	Bit Name	Description	Reset
31	rw	PC_LCK6	PC6 pin control register write un-locked control. When locked, disables the register PC_AFS6 write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	0x00
30..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..12	rw	PC_AFS6	PC6 pin alternate function select. Refer the GPIO AFS table for detail information. This register default value is affected by the hardware configure register CFG_EXRST_PIN after chip reset. 0x0 = AF0 : GPC6 0x1 = AF1 : RSTN 0x2 = AF2 : RTC_TS 0x3 = AF3 : URT0_NSS 0x4 = AF4 : URT1_NSS 0x5 = AF5 : TM20_ETR 0x6 = AF6 : TM26_ETR 0x7 = AF7 : Reserved 0x8 = AF8 : MBW1 0x9 = AF9 : MALE 0xA = AF10 : Reserved 0xB = AF11 : Reserved	0x00
11..10	rw	PC_FDIV6	PC6 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV6	PC6 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU6	PC6 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x01
4	-	Reserved	Reserved	0x00
3	rw	PC_HS6	PC6 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM6	PC6 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output	0x04

			0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	

1.4.8. PC7 IO control register

PC_CR7	PC7 IO control register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS7[3:0]				PC_FDIV7[1:0]		PC_ODC7	Reserved
7	6	5	4	3	2	1	0
PC_INV7	Reserved	PC_PU7	Reserved	PC_HS7	PC_IOM7[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PC_AFS7	PC7 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPC7 0x1 = AF1 : ADC0_TRG 0x2 = AF2 : RTC_OUT 0x3 = AF3 : URT0_DE 0x4 = AF4 : URT1_NSS 0x5 = AF5 : Reserved 0x6 = AF6 : TM36_TRGO 0x7 = AF7 : Reserved 0x8 = AF8 : MBW0 0x9 = AF9 : MCE 0xA = AF10 : Reserved 0xB = AF11 : Reserved	0x00
11..10	rw	PC_FDIV7	PC7 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PC_ODC7	PC7 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV7	PC7 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU7	PC7 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PC_HS7	PC7 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM7	PC7 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	0x00

1.4.9. PC8 IO control register

PC_CR8	PC8 IO control register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS8[3:0]				PC_FDIV8[1:0]		PC_ODC8	Reserved
7	6	5	4	3	2	1	0
PC_INV8	Reserved	PC_PU8	Reserved	PC_HS8	PC_IOM8[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PC_AFS8	PC8 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPC8 0x1 = AF1 : ADC0_OUT 0x2 = AF2 : I2C0_SCL 0x3 = AF3 : URT0_BRO 0x4 = AF4 : URT1_TX 0x5 = AF5 : TM20_OC0H 0x6 = AF6 : TM36_OC0H 0x7 = AF7 : TM36_OC0N 0x8 = AF8 : MAD11 0x9 = AF9 : MAD13 0xA = AF10 : CCL_P0 0xB = AF11 : URT6_TX	0x00
11..10	rw	PC_FDIV8	PC8 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PC_ODC8	PC8 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV8	PC8 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU8	PC8 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PC_HS8	PC8 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM8	PC8 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	0x00

1.4.10. PC9 IO control register

PC_CR9	PC9 IO control register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS9[3:0]				PC_FDIV9[1:0]		PC_ODC9	Reserved
7	6	5	4	3	2	1	0
PC_INV9	Reserved	PC_PU9	Reserved	PC_HS9	PC_IOM9[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PC_AFS9	PC9 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPC9 0x1 = AF1 : CMP0_P0 0x2 = AF2 : I2C0_SDA 0x3 = AF3 : URT0_TMO 0x4 = AF4 : URT1_RX 0x5 = AF5 : TM20_OC1H 0x6 = AF6 : TM36_OC1H 0x7 = AF7 : TM36_OC1N 0x8 = AF8 : MAD12 0x9 = AF9 : MAD6 0xA = AF10 : CCL_P1 0xB = AF11 : URT6_RX	0x00
11..10	rw	PC_FDIV9	PC9 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PC_ODC9	PC9 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV9	PC9 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU9	PC9 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PC_HS9	PC9 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM9	PC9 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	0x00

1.4.11. PC10 IO control register

PC_CR10	PC10 IO control register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS10[3:0]				PC_FDIV10[1:0]		PC_ODC10	Reserved
7	6	5	4	3	2	1	0
PC_INV10	Reserved	PC_PU10	Reserved	PC_HS10	PC_IOM10[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PC_AFS10	PC10 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPC10 0x1 = AF1 : CMP1_P0 0x2 = AF2 : I2C1_SCL 0x3 = AF3 : URT0_TX 0x4 = AF4 : URT2_TX 0x5 = AF5 : URT1_TX 0x6 = AF6 : TM36_OC2H 0x7 = AF7 : TM36_OC2N 0x8 = AF8 : MAD13 0x9 = AF9 : MAD14 0xA = AF10 : Reserved 0xB = AF11 : URT7_TX	0x00
11..10	rw	PC_FDIV10	PC10 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PC_ODC10	PC10 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV10	PC10 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU10	PC10 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PC_HS10	PC10 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM10	PC10 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	0x00

1.4.12. PC11 IO control register

PC_CR11	PC11 IO control register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16

Reserved							
15	14	13	12	11	10	9	8
PC_AFS11[3:0]				PC_FDIV11[1:0]		PC_ODC11	Reserved
7	6	5	4	3	2	1	0
PC_INV11	Reserved	PC_PU11	Reserved	PC_HS11	PC_IOM11[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PC_AFS11	PC11 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPC11 0x1 = AF1 : Reserved 0x2 = AF2 : I2C1_SDA 0x3 = AF3 : URT0_RX 0x4 = AF4 : URT2_RX 0x5 = AF5 : URT1_RX 0x6 = AF6 : TM36_OC3H 0x7 = AF7 : TM26_OC01 0x8 = AF8 : MAD14 0x9 = AF9 : MAD7 0xA = AF10 : Reserved 0xB = AF11 : URT7_RX	0x00
11..10	rw	PC_FDIV11	PC11 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PC_ODC11	PC11 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV11	PC11 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU11	PC11 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PC_HS11	PC11 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM11	PC11 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	0x00

1.4.13. PC12 IO control register

PC_CR12	PC12 IO control register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS12[3:0]				PC_FDIV12[1:0]		PC_ODC12	Reserved

7	6	5	4	3	2	1	0
PC_INV12	Reserved	PC_PU12	Reserved	PC_HS12	PC_IOM12[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PC_AFS12	PC12 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPC12 0x1 = AF1 : Reserved 0x2 = AF2 : IR_OUT 0x3 = AF3 : DAC_TRG0 0x4 = AF4 : URT1_DE 0x5 = AF5 : TM10_TRGO 0x6 = AF6 : TM36_OC3 0x7 = AF7 : TM26_OC02 0x8 = AF8 : MAD15 0x9 = AF9 : SDT_P0 0xA = AF10 : URT1_CLK 0xB = AF11 : MAM1	0x00
11..10	rw	PC_FDIV12	PC12 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PC_ODC12	PC12 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV12	PC12 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU12	PC12 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PC_HS12	PC12 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM12	PC12 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	0x000

1.4.14. PC13 IO control register

PC_CR13	PC13 IO control register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS13[3:0]				PC_FDIV13[1:0]		Reserved	Reserved
7	6	5	4	3	2	1	0
PC_INV13	Reserved	PC_PU13	Reserved	Reserved	PC_IOM13[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PC_AFS13	PC13 pin alternate function select. Refer the GPIO AFS table for detail information. When both PC_AFS13=XIN and PC_AFS14=XOUT, the XOSC analog part is enabled. Others the XOSC analog part is disabled. This register default value is affected by the hardware configure register CFG_XOSC_EN after chip reset. 0x0 = AF0 : GPC13 0x1 = AF1 : XIN 0x2 = AF2 : URT1_NSS 0x3 = AF3 : URT0_CTS 0x4 = AF4 : URT2_RX 0x5 = AF5 : TM10_ETR 0x6 = AF6 : TM26_ETR 0x7 = AF7 : TM36_OC00 0x8 = AF8 : TM20_IC0 0x9 = AF9 : SDT_I0 0xA = AF10 : Reserved 0xB = AF11 : URT6_RX	0x00
11..10	rw	PC_FDIV13	PC13 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV13	PC13 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU13	PC13 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	-	Reserved	Reserved	0x00
2..0	rw	PC_IOM13	PC13 pin IO mode control bits. This pin is using the crystal pad and is fixed output drive strength. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	0x00

1.4.15. PC14 IO control register

PC_CR14	PC14 IO control register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PC_AFS14[3:0]				PC_FDIV14[1:0]		Reserved	Reserved
7	6	5	4	3	2	1	0
PC_INV14	Reserved	PC_PU14	Reserved	PC_HS14	PC_IOM14[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000

15..12	rw	PC_AFS14	PC14 pin alternate function select. Refer the GPIO AFS table for detail information. When both PC_AFS13=XIN and PC_AFS14=XOUT, the XOSC analog part is enabled. Others the XOSC analog part is disabled. This register default value is affected by the hardware configure register CFG_XOSC_EN after chip reset. 0x0 = AF0 : GPC14 0x1 = AF1 : XOUT 0x2 = AF2 : URT1_TMO 0x3 = AF3 : URT0_RTS 0x4 = AF4 : URT2_TX 0x5 = AF5 : TM10_CKO 0x6 = AF6 : TM26_TRGO 0x7 = AF7 : TM36_OC10 0x8 = AF8 : TM20_IC1 0x9 = AF9 : SDT_I1 0xA = AF10 : Reserved 0xB = AF11 : URT6_TX	0x00
11..10	rw	PC_FDIV14	PC14 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	rw	PC_INV14	PC14 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PC_PU14	PC14 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PC_HS14	PC14 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PC_IOM14	PC14 pin IO mode control bits. This pin is using the crystal pad and is fixed output drive strength. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input 0x4 = QB : Quasi-Bidirectional output drive high one CLK	0x00

1.4.16. PC port input filter control register

PC_FLT	PC port input filter control register		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		Reserved			PC_FCKS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000

15..8	-	**Reserved**	Reserved	0x00
7..6	-	**Reserved**	Reserved	0x00
5..3	-	**Reserved**	Reserved	0x00
2..0	rw	**PC_FCKS**	PC port input deglitch filter clock source select for all pins of the port. 0x0 = CLK_AHB 0x1 = CLK_AHB_Div8 : CLK_AHB divide by 8 0x2 = CLK_ILRCO 0x3 = TM00_TRGO 0x4 = CK_UT	0x00

1.4.17. PC Register Map

PC Register Map Register Number = 16

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	PC_CR0	Reserved																PC_AFS0[3:0]				PC_FDIV0[1:0]		PC_ODC0	Reserved	PC_INV0	Reserved	PC_PU0	Reserved	PC_HS0	PC_IOM0[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	PC_CR1	Reserved																PC_AFS1[3:0]				PC_FDIV1[1:0]		PC_ODC1	Reserved	PC_INV1	Reserved	PC_PU1	Reserved	PC_HS1	PC_IOM1[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	PC_CR2	Reserved																PC_AFS2[3:0]				PC_FDIV2[1:0]		PC_ODC2	Reserved	PC_INV2	Reserved	PC_PU2	Reserved	PC_HS2	PC_IOM2[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	PC_CR3	Reserved																PC_AFS3[3:0]				PC_FDIV3[1:0]		PC_ODC3	Reserved	PC_INV3	Reserved	PC_PU3	Reserved	PC_HS3	PC_IOM3[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	PC_CR4	PC_LCK4	Reserved							Reserved								PC_AFS4[3:0]				PC_FDIV4[1:0]		PC_ODC4	Reserved	PC_INV4	Reserved	PC_PU4	Reserved	PC_HS4	PC_IOM4[2:0]		
Reset	**0x00000024**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0
0x14	PC_CR5	PC_LCK5	Reserved							Reserved								PC_AFS5[3:0]				PC_FDIV5[1:0]		PC_ODC5	Reserved	PC_INV5	Reserved	PC_PU5	Reserved	PC_HS5	PC_IOM5[2:0]		
Reset	**0x00000024**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0
0x18	PC_CR6	PC_LCK6	Reserved							Reserved								PC_AFS6[3:0]				PC_FDIV6[1:0]		Reserved	Reserved	PC_INV6	Reserved	PC_PU6	Reserved	PC_HS6	PC_IOM6[2:0]		
Reset	**0x00000024**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0
0x1C	PC_CR7	Reserved																PC_AFS7[3:0]				PC_FDIV7[1:0]		PC_ODC7	Reserved	PC_INV7	Reserved	PC_PU7	Reserved	PC_HS7	PC_IOM7[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x20	PC_CR8	Reserved																PC_AFS8[3:0]				PC_FDIV8[1:0]		PC_ODC8	Reserved	PC_INV8	Reserved	PC_PU8	Reserved	PC_HS8	PC_IOM8[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	PC_CR9	Reserved																PC_AFS9[3:0]				PC_FDIV9[1:0]		PC_ODC9	Reserved	PC_INV9	Reserved	PC_PU9	Reserved	PC_HS9	PC_IOM9[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	PC_CR10	Reserved																PC_AFS10[3:0]				PC_FDIV10[1:0]		PC_ODC10	Reserved	PC_INV10	Reserved	PC_PU10	Reserved	PC_HS10	PC_IOM10[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	PC_CR11	Reserved																PC_AFS11[3:0]				PC_FDIV11[1:0]		PC_ODC11	Reserved	PC_INV11	Reserved	PC_PU11	Reserved	PC_HS11	PC_IOM11[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	PC_CR12	Reserved																PC_AFS12[3:0]				PC_FDIV12[1:0]		PC_ODC12	Reserved	PC_INV12	Reserved	PC_PU12	Reserved	PC_HS12	PC_IOM12[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	PC_CR13	Reserved																PC_AFS13[3:0]				PC_FDIV13[1:0]		Reserved	Reserved	PC_INV13	Reserved	PC_PU13	Reserved	Reserved	PC_IOM13[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	PC_CR14	Reserved																PC_AFS14[3:0]				PC_FDIV14[1:0]		Reserved	Reserved	PC_INV14	Reserved	PC_PU14	Reserved	PC_HS14	PC_IOM14[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	PC_FLT	Reserved																Reserved								Reserved		Reserved			PC_FCKS[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.5. Port D Configure Registers

Port D Configure	(PD) Port D IO Mode Configure
Base Address :	0x44030000

1.5.1. PD0 IO control register

PD_CR0	PD0 IO control register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_AFS0[3:0]				PD_FDIV0[1:0]		PD_ODC0[1:0]	
7	6	5	4	3	2	1	0
PD_INV0	Reserved	PD_PU0	Reserved	PD_HS0	PD_IOM0[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS0	PD0 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD0 0x1 = AF1 : OBM_I0 0x2 = AF2 : TM10_CKO 0x3 = AF3 : URT0_CLK 0x4 = AF4 : TM26_OC1N 0x5 = AF5 : TM20_CKO 0x6 = AF6 : TM36_OC2 0x7 = AF7 : SPI0_NSS 0x8 = AF8 : MA0 0x9 = AF9 : MCLK 0xA = AF10 : Reserved 0xB = AF11 : URT2_NSS	0x00
11..10	rw	PD_FDIV0	PD0 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PD_ODC0	PD0 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PD_INV0	PD0 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU0	PD0 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS0	PD0 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM0	PD0 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.2. PD1 IO control register

PD_CR1	PD1 IO control register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_AFS1[3:0]				PD_FDIV1[1:0]		PD_ODC1[1:0]	
7	6	5	4	3	2	1	0
PD_INV1	Reserved	PD_PU1	Reserved	PD_HS1	PD_IOM1[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS1	PD1 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD1 0x1 = AF1 : OBM_I1 0x2 = AF2 : TM16_CKO 0x3 = AF3 : URT0_CLK 0x4 = AF4 : NCO_CK0 0x5 = AF5 : TM26_CKO 0x6 = AF6 : TM36_OC2N 0x7 = AF7 : SPI0_CLK 0x8 = AF8 : MA1 0x9 = AF9 : Reserved 0xA = AF10 : Reserved 0xB = AF11 : URT2_CLK	0x00
11..10	rw	PD_FDIV1	PD1 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PD_ODC1	PD1 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PD_INV1	PD1 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU1	PD1 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS1	PD1 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM1	PD1 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.3. PD2 IO control register

PD_CR2	PD2 IO control register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_AFS2[3:0]				PD_FDIV2[1:0]		PD_ODC2[1:0]	
7	6	5	4	3	2	1	0
PD_INV2	Reserved	PD_PU2	Reserved	PD_HS2	PD_IOM2[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS2	PD2 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD2 0x1 = AF1 : USB_S0 0x2 = AF2 : TM00_CKO 0x3 = AF3 : URT1_CLK 0x4 = AF4 : TM26_OC00 0x5 = AF5 : TM20_CKO 0x6 = AF6 : TM36_CKO 0x7 = AF7 : SPI0_MOSI 0x8 = AF8 : MA2 0x9 = AF9 : MAD4 0xA = AF10 : Reserved 0xB = AF11 : URT2_TX	0x00
11..10	rw	PD_FDIV2	PD2 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PD_ODC2	PD2 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PD_INV2	PD2 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU2	PD2 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS2	PD2 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM2	PD2 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.4. PD3 IO control register

PD_CR3	PD3 IO control register		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_AFS3[3:0]				PD_FDIV3[1:0]		PD_ODC3[1:0]	
7	6	5	4	3	2	1	0
PD_INV3	Reserved	PD_PU3	Reserved	PD_HS3	PD_IOM3[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS3	PD3 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD3 0x1 = AF1 : USB_S1 0x2 = AF2 : TM01_CKO 0x3 = AF3 : URT1_CLK 0x4 = AF4 : Reserved 0x5 = AF5 : SPI0_MISO 0x6 = AF6 : TM26_CKO 0x7 = AF7 : SPI0_D3 0x8 = AF8 : MA3 0x9 = AF9 : MAD7 0xA = AF10 : TM36_TRGO 0xB = AF11 : URT2_RX	0x00
11..10	rw	PD_FDIV3	PD3 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PD_ODC3	PD3 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PD_INV3	PD3 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU3	PD3 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS3	PD3 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM3	PD3 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.5. PD4 IO control register

PD_CR4	PD4 IO control register		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16

Reserved							
15	14	13	12	11	10	9	8
PD_AFS4[3:0]				PD_FDIV4[1:0]		PD_ODC4[1:0]	
7	6	5	4	3	2	1	0
PD_INV4	Reserved	PD_PU4	Reserved	PD_HS4	PD_IOM4[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS4	PD4 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD4 0x1 = AF1 : TM00_TRGO 0x2 = AF2 : TM01_TRGO 0x3 = AF3 : URT1_TX 0x4 = AF4 : Reserved 0x5 = AF5 : Reserved 0x6 = AF6 : TM26_OC00 0x7 = AF7 : SPI0_D2 0x8 = AF8 : MA4 0x9 = AF9 : MAD6 0xA = AF10 : Reserved 0xB = AF11 : URT2_TX ANA ~ DM (IO mode set AIO & connect to Analog macro)	0x00
11..10	rw	PD_FDIV4	PD4 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PD_ODC4	PD4 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PD_INV4	PD4 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU4	PD4 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS4	PD4 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM4	PD4 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.6. PD5 IO control register

PD_CR5	PD5 IO control register		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8

PD_AFS5[3:0]				PD_FDIV5[1:0]		PD_ODC5[1:0]	
7	6	5	4	3	2	1	0
PD_INV5	Reserved	PD_PU5	Reserved	PD_HS5	PD_IOM5[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS5	PD5 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD5 0x1 = AF1 : TM00_ETR 0x2 = AF2 : I2C0_SCL 0x3 = AF3 : URT1_RX 0x4 = AF4 : Reserved 0x5 = AF5 : Reserved 0x6 = AF6 : TM26_OC01 0x7 = AF7 : SPI0_MISO 0x8 = AF8 : MA5 0x9 = AF9 : MAD5 0xA = AF10 : Reserved 0xB = AF11 : URT2_RX ANA ~ DP (IO mode set AIO & connect to Analog macro)	0x00
11..10	rw	PD_FDIV5	PD5 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PD_ODC5	PD5 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PD_INV5	PD5 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU5	PD5 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS5	PD5 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM5	PD5 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.7. PD6 IO control register

PD_CR6	PD6 IO control register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_AFS6[3:0]				PD_FDIV6[1:0]		PD_ODC6	Reserved
7	6	5	4	3	2	1	0

PD_INV6	Reserved	PD_PU6	Reserved	PD_HS6	PD_IOM6[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS6	PD6 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD6 0x1 = AF1 : CPU_NMI 0x2 = AF2 : I2C0_SDA 0x3 = AF3 : URT1_NSS 0x4 = AF4 : Reserved 0x5 = AF5 : SPI0_NSSI 0x6 = AF6 : TM26_OC02 0x7 = AF7 : SPI0_NSS 0x8 = AF8 : MA6 0x9 = AF9 : SDT_P0 0xA = AF10 : Reserved 0xB = AF11 : URT2_NSS ANA ~ V33 (IO mode set AIO & connect to Analog macro)	0x00
11..10	rw	PD_FDIV6	PD6 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PD_ODC6	PD6 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PD_INV6	PD6 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU6	PD6 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS6	PD6 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM6	PD6 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.8. PD7 IO control register

PD_CR7	PD7 IO control register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_AFS7[3:0]				PD_FDIV7[1:0]		PD_ODC7[1:0]	
7	6	5	4	3	2	1	0
PD_INV7	Reserved	PD_PU7	Reserved	PD_HS7	PD_IOM7[2:0]		

Bit	Attr	Bit Name	Description	Reset

31..16	-	**Reserved**	Reserved	0x0000
15..12	rw	**PD_AFS7**	PD7 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD7 0x1 = AF1 : TM00_CKO 0x2 = AF2 : TM01_ETR 0x3 = AF3 : URT1_DE 0x4 = AF4 : Reserved 0x5 = AF5 : SPI0_MISO 0x6 = AF6 : TM26_OC0N 0x7 = AF7 : SPI0_D4 0x8 = AF8 : MA7 0x9 = AF9 : MAD0 0xA = AF10 : TM36_IC0 0xB = AF11 : Reserved	0x00
11..10	rw	**PD_FDIV7**	PD7 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	**PD_ODC7**	PD7 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	**PD_INV7**	PD7 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	**Reserved**	Reserved	0x00
5	rw	**PD_PU7**	PD7 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	**Reserved**	Reserved	0x00
3	rw	**PD_HS7**	PD7 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	**PD_IOM7**	PD7 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.9. PD8 IO control register

PD_CR8	**PD8 IO control register**		
Offset Address :	**0x20**	**Reset Value :**	**0x00000000**

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PD_AFS8[3:0]				PD_FDIV8[1:0]		PD_ODC8[1:0]	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PD_INV8	Reserved	PD_PU8	Reserved	PD_HS8	PD_IOM8[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..12	rw	**PD_AFS8**	PD8 pin alternate function select. Refer the GPIO AFS table for detail information.	0x00

			0x0 = AF0 : GPD8 0x1 = AF1 : CPU_TXEV 0x2 = AF2 : TM01_TRGO 0x3 = AF3 : URT1_RTS 0x4 = AF4 : Reserved 0x5 = AF5 : SPI0_D2 0x6 = AF6 : TM26_OC10 0x7 = AF7 : SPI0_D7 0x8 = AF8 : MA8 0x9 = AF9 : MAD3 0xA = AF10 : TM36_IC1 0xB = AF11 : SPI0_CLK	
11..10	rw	PD_FDIV8	PD8 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PD_ODC8	PD8 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PD_INV8	PD8 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU8	PD8 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS8	PD8 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM8	PD8 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.10. PD9 IO control register

PD_CR9	PD9 IO control register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_AFS9[3:0]				PD_FDIV9[1:0]		PD_ODC9	Reserved
7	6	5	4	3	2	1	0
PD_INV9	Reserved	PD_PU9	Reserved	PD_HS9	PD_IOM9[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS9	PD9 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD9 0x1 = AF1 : CPU_RXEV 0x2 = AF2 : TM00_TRGO	0x00

			0x3 = AF3 : URT1_CTS 0x4 = AF4 : Reserved 0x5 = AF5 : SPI0_NSSI 0x6 = AF6 : TM26_OC11 0x7 = AF7 : SPI0_D6 0x8 = AF8 : MA9 0x9 = AF9 : MAD2 0xA = AF10 : TM36_IC2 0xB = AF11 : SPI0_NSS	
11..10	rw	PD_FDIV9	PD9 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PD_ODC9	PD9 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PD_INV9	PD9 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU9	PD9 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS9	PD9 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM9	PD9 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.11. PD10 IO control register

PD_CR10	PD10 IO control register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_AFS10[3:0]				PD_FDIV10[1:0]		PD_ODC10	Reserved
7	6	5	4	3	2	1	0
PD_INV10	Reserved	PD_PU10	Reserved	PD_HS10	PD_IOM10[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS10	PD10 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD10 0x1 = AF1 : CPU_NMI 0x2 = AF2 : TM00_ETR 0x3 = AF3 : URT1_BRO 0x4 = AF4 : Reserved 0x5 = AF5 : RTC_OUT 0x6 = AF6 : TM26_OC12	0x00

			0x7 = AF7 : SPI0_D5 0x8 = AF8 : MA10 0x9 = AF9 : MAD1 0xA = AF10 : TM36_IC3 0xB = AF11 : SPI0_MOSI	
11..10	rw	PD_FDIV10	PD10 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PD_ODC10	PD10 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PD_INV10	PD10 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU10	PD10 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS10	PD10 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM10	PD10 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.12. PD11 IO control register

PD_CR11	PD11 IO control register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_AFS11[3:0]				PD_FDIV11[1:0]		PD_ODC11	Reserved
7	6	5	4	3	2	1	0
PD_INV11	Reserved	PD_PU11	Reserved	PD_HS11	PD_IOM11[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS11	PD11 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD11 0x1 = AF1 : CPU_NMI 0x2 = AF2 : DMA_TRG1 0x3 = AF3 : URT1_TMO 0x4 = AF4 : Reserved 0x5 = AF5 : SPI0_D3 0x6 = AF6 : TM26_OC1N 0x7 = AF7 : SPI0_NSS 0x8 = AF8 : MA11 0x9 = AF9 : MWE 0xA = AF10 : Reserved	0x00

			0xB = AF11 : Reserved	
11..10	rw	PD_FDIV11	PD11 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PD_ODC11	PD11 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PD_INV11	PD11 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU11	PD11 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS11	PD11 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM11	PD11 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.13. PD12 IO control register

PD_CR12	PD12 IO control register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_AFS12[3:0]				PD_FDIV12[1:0]		PD_ODC12	Reserved
7	6	5	4	3	2	1	0
PD_INV12	Reserved	PD_PU12	Reserved	PD_HS12	PD_IOM12[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS12	PD12 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD12 0x1 = AF1 : CMP0_P0 0x2 = AF2 : TM10_CKO 0x3 = AF3 : OBM_P0 0x4 = AF4 : TM00_CKO 0x5 = AF5 : SPI0_CLK 0x6 = AF6 : TM20_OC0H 0x7 = AF7 : TM26_OC0H 0x8 = AF8 : MA12 0x9 = AF9 : MALE2 0xA = AF10 : Reserved 0xB = AF11 : Reserved	0x00
11..10	rw	PD_FDIV12	PD12 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1	0x00

Bit	Attr	Bit Name	Description	Reset
			0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	
9	rw	PD_ODC12	PD12 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PD_INV12	PD12 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU12	PD12 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS12	PD12 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM12	PD12 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.14. PD13 IO control register

PD_CR13	PD13 IO control register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PD_AFS13[3:0]				PD_FDIV13[1:0]		PD_ODC13	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PD_INV13	Reserved	PD_PU13	Reserved	PD_HS13	PD_IOM13[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS13	PD13 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD13 0x1 = AF1 : CMP1_P0 0x2 = AF2 : TM10_TRGO 0x3 = AF3 : OBM_P1 0x4 = AF4 : TM00_TRGO 0x5 = AF5 : NCO_CK0 0x6 = AF6 : TM20_OC1H 0x7 = AF7 : TM26_OC1H 0x8 = AF8 : MA13 0x9 = AF9 : MCE 0xA = AF10 : Reserved 0xB = AF11 : Reserved	0x00
11..10	rw	PD_FDIV13	PD13 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PD_ODC13	PD13 pin output drive strength select. 0x0 = Level0 : Drive strength-full	0x00

			0x1 = Level2 : Drive strength-1/4	
8	-	Reserved	Reserved	0x00
7	rw	PD_INV13	PD13 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU13	PD13 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS13	PD13 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM13	PD13 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.15. PD14 IO control register

PD_CR14	PD14 IO control register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_AFS14[3:0]				PD_FDIV14[1:0]		PD_ODC14	Reserved
7	6	5	4	3	2	1	0
PD_INV14	Reserved	PD_PU14	Reserved	PD_HS14	PD_IOM14[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS14	PD14 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD14 0x1 = AF1 : Reserved 0x2 = AF2 : TM10_ETR 0x3 = AF3 : DAC_TRG0 0x4 = AF4 : TM00_ETR 0x5 = AF5 : Reserved 0x6 = AF6 : TM20_IC0 0x7 = AF7 : TM26_IC0 0x8 = AF8 : MA14 0x9 = AF9 : MOE 0xA = AF10 : CCL_P0 0xB = AF11 : URT5_TX	0x00
11..10	rw	PD_FDIV14	PD14 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PD_ODC14	PD14 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PD_INV14	PD14 pin input inverse enable bit. 0 = Disable	0x00

			1 = Enable	
6	-	Reserved	Reserved	0x00
5	rw	PD_PU14	PD14 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PD_HS14	PD14 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM14	PD14 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.16. PD15 IO control register

PD_CR15	PD15 IO control register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PD_AFS15[3:0]				PD_FDIV15[1:0]		PD_ODC15	Reserved
7	6	5	4	3	2	1	0
PD_INV15	Reserved	PD_PU15	Reserved	PD_HS15	PD_IOM15[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PD_AFS15	PD15 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPD15 0x1 = AF1 : Reserved 0x2 = AF2 : NCO_P0 0x3 = AF3 : IR_OUT 0x4 = AF4 : DMA_TRG0 0x5 = AF5 : Reserved 0x6 = AF6 : TM20_IC1 0x7 = AF7 : TM26_IC1 0x8 = AF8 : MA15 0x9 = AF9 : Reserved 0xA = AF10 : CCL_P1 0xB = AF11 : URT5_RX	0x00
11..10	rw	PD_FDIV15	PD15 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PD_ODC15	PD15 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PD_INV15	PD15 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PD_PU15	PD15 pin pull-up resister enable bit. 0 = Disable	0x00

			1 = Enable	
4	-	Reserved	Reserved	0x00
3	rw	PD_HS15	PD15 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PD_IOM15	PD15 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.5.17. PD port input filter control register

PD_FLT	PD port input filter control register		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		Reserved			PD_FCKS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5..3	-	Reserved	Reserved	0x00
2..0	rw	PD_FCKS	PD port input deglitch filter clock source select for all pins of the port. 0x0 = CLK_AHB 0x1 = CLK_AHB_Div8 : CLK_AHB divide by 8 0x2 = CLK_ILRCO 0x3 = TM00_TRGO 0x4 = CK_UT	0x00

1.5.18. PD Register Map

PD Register Map **Register Number = 17**

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	PD_CR0	Reserved																PD_AFS0[3:0]				PD_FDIV0[1:0]		PD_ODC0[1:0]		PD_INV0	Reserved	PD_PU0	Reserved	PD_HS0	PD_IOM0[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	PD_CR1	Reserved																PD_AFS1[3:0]				PD_FDIV1[1:0]		PD_ODC1[1:0]		PD_INV1	Reserved	PD_PU1	Reserved	PD_HS1	PD_IOM1[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	PD_CR2	Reserved																PD_AFS2[3:0]				PD_FDIV2[1:0]		PD_ODC2[1:0]		PD_INV2	Reserved	PD_PU2	Reserved	PD_HS2	PD_IOM2[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	PD_CR3	Reserved																PD_AFS3[3:0]				PD_FDIV3[1:0]		PD_ODC3[1:0]		PD_INV3	Reserved	PD_PU3	Reserved	PD_HS3	PD_IOM3[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	PD_CR4	Reserved																PD_AFS4[3:0]				PD_FDIV4[1:0]		PD_ODC4[1:0]		PD_INV4	Reserved	PD_PU4	Reserved	PD_HS4	PD_IOM4[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	PD_CR5	Reserved																PD_AFS5[3:0]				PD_FDIV5[1:0]		PD_ODC5[1:0]		PD_INV5	Reserved	PD_PU5	Reserved	PD_HS5	PD_IOM5[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	PD_CR6	Reserved																PD_AFS6[3:0]				PD_FDIV6[1:0]		PD_ODC6	Reserved	PD_INV6	Reserved	PD_PU6	Reserved	PD_HS6	PD_IOM6[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	PD_CR7	Reserved																PD_AFS7[3:0]				PD_FDIV7[1:0]		PD_ODC7[1:0]		PD_INV7	Reserved	PD_PU7	Reserved	PD_HS7	PD_IOM7[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x20	PD_CR8	Reserved																PD_AFS8[3:0]				PD_FDIV8[1:0]		PD_ODC8[1:0]		PD_INV8	Reserved	PD_PU8	Reserved	PD_HS8	PD_IOM8[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	PD_CR9	Reserved																PD_AFS9[3:0]				PD_FDIV9[1:0]		PD_ODC9	Reserved	PD_INV9	Reserved	PD_PU9	Reserved	PD_HS9	PD_IOM9[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	PD_CR10	Reserved																PD_AFS10[3:0]				PD_FDIV10[1:0]		PD_ODC10	Reserved	PD_INV10	Reserved	PD_PU10	Reserved	PD_HS10	PD_IOM10[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	PD_CR11	Reserved																PD_AFS11[3:0]				PD_FDIV11[1:0]		PD_ODC11	Reserved	PD_INV11	Reserved	PD_PU11	Reserved	PD_HS11	PD_IOM11[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	PD_CR12	Reserved																PD_AFS12[3:0]				PD_FDIV12[1:0]		PD_ODC12	Reserved	PD_INV12	Reserved	PD_PU12	Reserved	PD_HS12	PD_IOM12[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	PD_CR13	Reserved																PD_AFS13[3:0]				PD_FDIV13[1:0]		PD_ODC13	Reserved	PD_INV13	Reserved	PD_PU13	Reserved	PD_HS13	PD_IOM13[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	PD_CR14	Reserved																PD_AFS14[3:0]				PD_FDIV14[1:0]		PD_ODC14	Reserved	PD_INV14	Reserved	PD_PU14	Reserved	PD_HS14	PD_IOM14[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	PD_CR15	Reserved																PD_AFS15[3:0]				PD_FDIV15[1:0]		PD_ODC15	Reserved	PD_INV15	Reserved	PD_PU15	Reserved	PD_HS15	PD_IOM15[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	PD_FLT	Reserved																Reserved								Reserved		Reserved			PD_FCKS[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.6. Port E Configure Registers

Port E Configure	(PE) Port E IO Mode Configure
Base Address :	0x44040000

1.6.1. PE0 IO control register

PE_CR0	PE0 IO control register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PE_AFS0[3:0]				PE_FDIV0[1:0]		PE_ODC0[1:0]	
7	6	5	4	3	2	1	0
PE_INV0	Reserved	PE_PU0	Reserved	PE_HS0	PE_IOM0[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PE_AFS0	PE0 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPE0 0x1 = AF1 : OBM_I0 0x2 = AF2 : Reserved 0x3 = AF3 : URT0_TX 0x4 = AF4 : DAC_TRG0 0x5 = AF5 : SPI0_NSS 0x6 = AF6 : TM20_OC00 0x7 = AF7 : TM26_OC00 0x8 = AF8 : MALE 0x9 = AF9 : MAD8 0xA = AF10 : Reserved 0xB = AF11 : URT4_TX	0x00
11..10	rw	PE_FDIV0	PE0 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PE_ODC0	PE0 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PE_INV0	PE0 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PE_PU0	PE0 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PE_HS0	PE0 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PE_IOM0	PE0 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output	0x00

			0x3 = DIN : Digital input	

1.6.2. PE1 IO control register

PE_CR1	PE1 IO control register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PE_AFS1[3:0]				PE_FDIV1[1:0]		PE_ODC1[1:0]	
7	6	5	4	3	2	1	0
PE_INV1	Reserved	PE_PU1	Reserved	PE_HS1	PE_IOM1[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PE_AFS1	PE1 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPE1 0x1 = AF1 : OBM_I1 0x2 = AF2 : Reserved 0x3 = AF3 : URT0_RX 0x4 = AF4 : DMA_TRG1 0x5 = AF5 : SPI0_MISO 0x6 = AF6 : TM20_OC01 0x7 = AF7 : TM26_OC01 0x8 = AF8 : MOE 0x9 = AF9 : MAD9 0xA = AF10 : TM36_OC0H 0xB = AF11 : URT4_RX	0x00
11..10	rw	PE_FDIV1	PE1 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PE_ODC1	PE1 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PE_INV1	PE1 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PE_PU1	PE1 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PE_HS1	PE1 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PE_IOM1	PE1 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.6.3. PE2 IO control register

PE_CR2	PE2 IO control register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PE_AFS2[3:0]				PE_FDIV2[1:0]		PE_ODC2[1:0]	
7	6	5	4	3	2	1	0
PE_INV2	Reserved	PE_PU2	Reserved	PE_HS2	PE_IOM2[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PE_AFS2	PE2 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPE2 0x1 = AF1 : OBM_P0 0x2 = AF2 : I2C1_SCL 0x3 = AF3 : URT1_TX 0x4 = AF4 : NCO_P0 0x5 = AF5 : SPI0_CLK 0x6 = AF6 : TM20_OC02 0x7 = AF7 : TM26_OC02 0x8 = AF8 : MWE 0x9 = AF9 : MAD10 0xA = AF10 : TM36_OC1H 0xB = AF11 : URT5_TX	0x00
11..10	rw	PE_FDIV2	PE2 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PE_ODC2	PE2 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PE_INV2	PE2 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PE_PU2	PE2 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PE_HS2	PE2 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PE_IOM2	PE2 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.6.4. PE3 IO control register

PE_CR3	PE3 IO control register		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PE_AFS3[3:0]				PE_FDIV3[1:0]		PE_ODC3[1:0]	
7	6	5	4	3	2	1	0
PE_INV3	Reserved	PE_PU3	Reserved	PE_HS3	PE_IOM3[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PE_AFS3	PE3 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPE3 0x1 = AF1 : OBM_P1 0x2 = AF2 : I2C1_SDA 0x3 = AF3 : URT1_RX 0x4 = AF4 : NCO_CK0 0x5 = AF5 : SPI0_MOSI 0x6 = AF6 : TM20_OC0N 0x7 = AF7 : TM26_OC0N 0x8 = AF8 : MCE 0x9 = AF9 : MALE2 0xA = AF10 : Reserved 0xB = AF11 : URT5_RX	0x00
11..10	rw	PE_FDIV3	PE3 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9..8	rw	PE_ODC3	PE3 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level1 : Drive strength-1/2 0x2 = Level2 : Drive strength-1/4 0x3 = Level3 : Drive strength-1/8	0x00
7	rw	PE_INV3	PE3 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PE_PU3	PE3 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PE_HS3	PE3 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PE_IOM3	PE3 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.6.5. PE8 IO control register

PE_CR8	PE8 IO control register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16

Reserved							
15	14	13	12	11	10	9	8
PE_AFS8[3:0]				PE_FDIV8[1:0]		PE_ODC8	Reserved
7	6	5	4	3	2	1	0
PE_INV8	Reserved	PE_PU8	Reserved	PE_HS8	PE_IOM8[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PE_AFS8	PE8 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPE8 0x1 = AF1 : CPU_TXEV 0x2 = AF2 : OBM_I0 0x3 = AF3 : URT2_TX 0x4 = AF4 : SDT_I0 0x5 = AF5 : TM36_CKO 0x6 = AF6 : TM20_CKO 0x7 = AF7 : TM26_CKO 0x8 = AF8 : Reserved 0x9 = AF9 : MAD11 0xA = AF10 : Reserved 0xB = AF11 : URT4_TX	0x00
11..10	rw	PE_FDIV8	PE8 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PE_ODC8	PE8 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PE_INV8	PE8 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PE_PU8	PE8 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PE_HS8	PE8 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PE_IOM8	PE8 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.6.6. PE9 IO control register

PE_CR9	PE9 IO control register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PE_AFS9[3:0]				PE_FDIV9[1:0]		PE_ODC9	Reserved
7	6	5	4	3	2	1	0

PE_INV9	Reserved	PE_PU9	Reserved	PE_HS9	PE_IOM9[2:0]

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PE_AFS9	PE9 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPE9 0x1 = AF1 : CPU_RXEV 0x2 = AF2 : OBM_I1 0x3 = AF3 : URT2_RX 0x4 = AF4 : SDT_I1 0x5 = AF5 : TM36_TRGO 0x6 = AF6 : TM20_TRGO 0x7 = AF7 : TM26_TRGO 0x8 = AF8 : Reserved 0x9 = AF9 : MOE 0xA = AF10 : Reserved 0xB = AF11 : URT4_RX	0x00
11..10	rw	PE_FDIV9	PE9 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PE_ODC9	PE9 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PE_INV9	PE9 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PE_PU9	PE9 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PE_HS9	PE9 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PE_IOM9	PE9 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.6.7. PE12 IO control register

PE_CR12	PE12 IO control register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PE_AFS12[3:0]				PE_FDIV12[1:0]		PE_ODC12	Reserved
7	6	5	4	3	2	1	0
PE_INV12	Reserved	PE_PU12	Reserved	PE_HS12	PE_IOM12[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000

15..12	rw	PE_AFS12	PE12 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPE12 0x1 = AF1 : ADC0_TRG 0x2 = AF2 : USB_S0 0x3 = AF3 : Reserved 0x4 = AF4 : TM01_CKO 0x5 = AF5 : TM16_CKO 0x6 = AF6 : TM20_OC10 0x7 = AF7 : TM26_OC10 0x8 = AF8 : MBW0 0x9 = AF9 : Reserved 0xA = AF10 : Reserved 0xB = AF11 : URT6_TX	0x00
11..10	rw	PE_FDIV12	PE12 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PE_ODC12	PE12 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PE_INV12	PE12 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PE_PU12	PE12 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PE_HS12	PE12 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PE_IOM12	PE12 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.6.8. PE13 IO control register

PE_CR13	PE13 IO control register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PE_AFS13[3:0]				PE_FDIV13[1:0]		PE_ODC13	Reserved
7	6	5	4	3	2	1	0
PE_INV13	Reserved	PE_PU13	Reserved	PE_HS13	PE_IOM13[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PE_AFS13	PE13 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPE13 0x1 = AF1 : ADC0_OUT	0x00

			0x2 = AF2 : USB_S1 0x3 = AF3 : Reserved 0x4 = AF4 : TM01_TRGO 0x5 = AF5 : TM16_TRGO 0x6 = AF6 : TM20_OC11 0x7 = AF7 : TM26_OC11 0x8 = AF8 : MBW1 0x9 = AF9 : Reserved 0xA = AF10 : TM36_OC2H 0xB = AF11 : URT6_RX	
11..10	rw	**PE_FDIV13**	PE13 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	**PE_ODC13**	PE13 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	**Reserved**	Reserved	0x00
7	rw	**PE_INV13**	PE13 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	**Reserved**	Reserved	0x00
5	rw	**PE_PU13**	PE13 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	**Reserved**	Reserved	0x00
3	rw	**PE_HS13**	PE13 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	**PE_IOM13**	PE13 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.6.9. PE14 IO control register

PE_CR14	PE14 IO control register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PE_AFS14[3:0]				PE_FDIV14[1:0]		PE_ODC14	Reserved
7	6	5	4	3	2	1	0
PE_INV14	Reserved	PE_PU14	Reserved	PE_HS14	PE_IOM14[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..12	rw	**PE_AFS14**	PE14 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPE14 0x1 = AF1 : RTC_OUT 0x2 = AF2 : I2C1_SCL 0x3 = AF3 : Reserved 0x4 = AF4 : TM01_ETR 0x5 = AF5 : TM16_ETR	0x00

			0x6 = AF6 : TM20_OC12 0x7 = AF7 : TM26_OC12 0x8 = AF8 : MALE2 0x9 = AF9 : CCL_P0 0xA = AF10 : TM36_OC3H 0xB = AF11 : URT7_TX	
11..10	rw	PE_FDIV14	PE14 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	PE_ODC14	PE14 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	Reserved	Reserved	0x00
7	rw	PE_INV14	PE14 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	PE_PU14	PE14 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	PE_HS14	PE14 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	PE_IOM14	PE14 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.6.10. PE15 IO control register

PE_CR15	PE15 IO control register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PE_AFS15[3:0]				PE_FDIV15[1:0]		PE_ODC15	Reserved
7	6	5	4	3	2	1	0
PE_INV15	Reserved	PE_PU15	Reserved	PE_HS15	PE_IOM15[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	rw	PE_AFS15	PE15 pin alternate function select. Refer the GPIO AFS table for detail information. 0x0 = AF0 : GPE15 0x1 = AF1 : RTC_TS 0x2 = AF2 : I2C1_SDA 0x3 = AF3 : Reserved 0x4 = AF4 : TM36_BK0 0x5 = AF5 : TM36_ETR 0x6 = AF6 : TM20_OC1N 0x7 = AF7 : TM26_OC1N 0x8 = AF8 : MALE 0x9 = AF9 : CCL_P1	0x00

			0xA = AF10 : Reserved 0xB = AF11 : URT7_RX	
11..10	rw	**PE_FDIV15**	PE15 pin input deglitch filter clock divider select. 0x0 = Bypass : Bypass filter 0x1 = Div1 : Divided by 1 0x2 = Div4 : Divided by 4 0x3 = Div16 : Divided by 16	0x00
9	rw	**PE_ODC15**	PE15 pin output drive strength select. 0x0 = Level0 : Drive strength-full 0x1 = Level2 : Drive strength-1/4	0x00
8	-	**Reserved**	Reserved	0x00
7	rw	**PE_INV15**	PE15 pin input inverse enable bit. 0 = Disable 1 = Enable	0x00
6	-	**Reserved**	Reserved	0x00
5	rw	**PE_PU15**	PE15 pin pull-up resister enable bit. 0 = Disable 1 = Enable	0x00
4	-	**Reserved**	Reserved	0x00
3	rw	**PE_HS15**	PE15 pin output high speed mode enable bit. 0 = Disable 1 = Enable	0x00
2..0	rw	**PE_IOM15**	PE15 pin IO mode control bits. 0x0 = AIO : analog IO 0x1 = ODO : open drain output 0x2 = PPO : push pull output 0x3 = DIN : Digital input	0x00

1.6.11. PE port input filter control register

PE_FLT	**PE port input filter control register**		
Offset Address :	**0x40**	**Reset Value :**	**0x00000000**

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		**Reserved**			**PE_FCKS[2:0]**		

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..8	-	**Reserved**	Reserved	0x00
7..6	-	**Reserved**	Reserved	0x00
5..3	-	**Reserved**	Reserved	0x00
2..0	rw	**PE_FCKS**	PE port input deglitch filter clock source select for all pins of the port. 0x0 = CLK_AHB 0x1 = CLK_AHB_Div8 : CLK_AHB divide by 8 0x2 = CLK_ILRCO 0x3 = TM00_TRGO 0x4 = CK_UT	0x00

1.6.12. PE Register Map

PE Register Map **Register Number = 11**

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	PE_CR0	Reserved																PE_AFS0[3:0]				PE_FDIV0[1:0]		PE_ODC0[1:0]		PE_INV0	Reserved	PE_PU0	Reserved	PE_HS0	PE_IOM0[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	PE_CR1	Reserved																PE_AFS1[3:0]				PE_FDIV1[1:0]		PE_ODC1[1:0]		PE_INV1	Reserved	PE_PU1	Reserved	PE_HS1	PE_IOM1[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	PE_CR2	Reserved																PE_AFS2[3:0]				PE_FDIV2[1:0]		PE_ODC2[1:0]		PE_INV2	Reserved	PE_PU2	Reserved	PE_HS2	PE_IOM2[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	PE_CR3	Reserved																PE_AFS3[3:0]				PE_FDIV3[1:0]		PE_ODC3[1:0]		PE_INV3	Reserved	PE_PU3	Reserved	PE_HS3	PE_IOM3[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	PE_CR8	Reserved																PE_AFS8[3:0]				PE_FDIV8[1:0]		PE_ODC8	Reserved	PE_INV8	Reserved	PE_PU8	Reserved	PE_HS8	PE_IOM8[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	PE_CR9	Reserved																PE_AFS9[3:0]				PE_FDIV9[1:0]		PE_ODC9	Reserved	PE_INV9	Reserved	PE_PU9	Reserved	PE_HS9	PE_IOM9[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	PE_CR12	Reserved																PE_AFS12[3:0]				PE_FDIV12[1:0]		PE_ODC12	Reserved	PE_INV12	Reserved	PE_PU12	Reserved	PE_HS12	PE_IOM12[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	PE_CR13	Reserved																PE_AFS13[3:0]				PE_FDIV13[1:0]		PE_ODC13	Reserved	PE_INV13	Reserved	PE_PU13	Reserved	PE_HS13	PE_IOM13[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x38	PE_CR14	Reserved																PE_AFS14[3:0]				PE_FDIV14[1:0]		PE_ODC14	Reserved	PE_INV14	Reserved	PE_PU14	Reserved	PE_HS14	PE_IOM14[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	PE_CR15	Reserved																PE_AFS15[3:0]				PE_FDIV15[1:0]		PE_ODC15	Reserved	PE_INV15	Reserved	PE_PU15	Reserved	PE_HS15	PE_IOM15[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	PE_FLT	Reserved																Reserved								Reserved		Reserved			PE_FCKS[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.7. GPL Control Registers

GPL Control	(GPL) General Purpose Logic Control
Base Address :	0x4B000000

1.7.1. GPL status register

GPL_STA	GPL status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved	GPL_PAR32_OUT	GPL_PAR16_OUT[1:0]		GPL_PAR8_OUT[3:0]			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					GPL_DIVZEF	GPL_DIVCF	Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	-	Reserved	Reserved	0x00
14	r	GPL_PAR32_OUT	GPL 32-bit data parity check output.	0x00
13..12	r	GPL_PAR16_OUT	GPL 16-bit data parity check output.	0x00
11..8	r	GPL_PAR8_OUT	GPL 8-bit data parity check output.	0x00
7..3	-	Reserved	Reserved	0x00
2	r	GPL_DIVZEF	Divider division by zero error flag. 0 = Normal : divisor is not zero 1 = Happened : divisor is zero	0x00
1	r	GPL_DIVCF	Divider calculation complete flag. 0 = Not : divider calculating 1 = Complete : calculation complete	0x00
0	-	Reserved	Reserved	0x00

1.7.2. GPL control register 0

GPL_CR0	GPL control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
GPL_DMA_EN	Reserved	Reserved					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved					GPL_PAR_POL	Reserved	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	GPL_IN_INV	Reserved	GPL_BEND16_EN	GPL_BREV_MDS[1:0]		GPL_BEND_EN	Reserved

Bit	Attr	Bit Name	Description	Reset
31	rw	GPL_DMA_EN	Direct memory access enable bit. When enables, hardware can receive the data from DMA to do GPL process. 0 = Disable 1 = Enable	0x00
30	-	Reserved	Reserved	0x00
29..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..11	-	Reserved	Reserved	0x00
10	rw	GPL_PAR_POL	Data parity check polarity select. 0 = Even 1 = Odd	0x00

9..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	rw	GPL_IN_INV	Inverse input data enable. 0 = Disable 1 = Enable	0x00
5	-	Reserved	Reserved	0x00
4	rw	GPL_BEND16_EN	Data byte Big/little endian change mode enable for 16-bit range. 0 = Disable 1 = Enable	0x00
3..2	rw	GPL_BREV_MDS	Data bit order reverse change mode select. 0x0 = Disable 0x1 = 8bit : 8-bit range bit order reverse 0x2 = 16bit : 16-bit range bit order reverse 0x3 = 32bit : 32-bit range bit order reverse	0x00
1	rw	GPL_BEND_EN	Data byte Big/little endian change mode enable for 32-bit range. 0 = Disable 1 = Enable	0x00
0	-	Reserved	Reserved	0x00

1.7.3. GPL control register 1

GPL_CR1	GPL control register 1		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							GPL_DIV_START
23	22	21	20	19	18	17	16
Reserved							GPL_DIV_TYPE
15	14	13	12	11	10	9	8
Reserved						Reserved	
7	6	5	4	3	2	1	0
GPL_CRC_BREV[1:0]		GPL_CRC_DSIZE[1:0]		GPL_CRC_MDS[1:0]		Reserved	GPL_CRC_EN

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	GPL_DIV_START	Hardware divider start calculation control bit. (set by software and clear by hardware) 0 = No : no operation 1 = Start : start division	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	GPL_DIV_TYPE	Hardware divider division type selection. When selects 'Signed', the calculation value is with signed bit and divison by two's complement control. 0 = Unsigned : unsigned value division 1 = Signed : value with two's complemented	0x00
15..10	-	Reserved	Reserved	0x00
9..8	-	Reserved	Reserved	0x00
7..6	rw	GPL_CRC_BREV	CRC data output bit order reverse change mode select. 0x0 = Disable 0x1 = 8bit : 8-bit range bit order reverse 0x2 = 16bit : 16-bit range bit order reverse 0x3 = 32bit : 32-bit range bit order reverse	0x00
5..4	rw	GPL_CRC_DSIZE	CRC operation data size. When DMA enable bit is set in GPL_DMA_EN and DMA_FGBUS_SEL=0, the register is fixed 8-bit setting by hardware. When DMA enable bit is set in GPL_DMA_EN and DMA_FGBUS_SEL=1, the register is fixed 32-bit setting by hardware. 0x0 = 8bit	0x00

			0x1 = 16bit 0x2 = 32bit 0x3 = Reserved	
3..2	rw	GPL_CRC_MDS	CRC mode select. 0x0 = CCITT16 : polynomial 0x1021 0x1 = CRC8 : polynomial 0x07 0x2 = CRC16 : polynomial 0x8005 0x3 = CRC32 : polynomial 0x4C11DB7	0x00
1	-	Reserved	Reserved	0x00
0	rw	GPL_CRC_EN	CRC function enable bit. 0 = Disable 1 = Enable	0x00

1.7.4. GPL data input register

GPL_DIN	GPL data input register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
GPL_DIN[31:24]							
23	22	21	20	19	18	17	16
GPL_DIN[23:16]							
15	14	13	12	11	10	9	8
GPL_DIN[15:8]							
7	6	5	4	3	2	1	0
GPL_DIN[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	GPL_DIN	GPL data input register. For write operation, this register is used to write new calculation data.	0x00000000

1.7.5. GPL data output register

GPL_DOUT	GPL data output register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
GPL_DOUT[31:24]							
23	22	21	20	19	18	17	16
GPL_DOUT[23:16]							
15	14	13	12	11	10	9	8
GPL_DOUT[15:8]							
7	6	5	4	3	2	1	0
GPL_DOUT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	GPL_DOUT	GPL data output register.	0x00000000

1.7.6. GPL CRC initial register

GPL_CRCINIT	GPL CRC initial register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
GPL_CRC_INIT[31:24]							
23	22	21	20	19	18	17	16
GPL_CRC_INIT[23:16]							
15	14	13	12	11	10	9	8
GPL_CRC_INIT[15:8]							

7	6	5	4	3	2	1	0
GPL_CRC_INIT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	GPL_CRC_INIT	Programmable initial CRC value. The CRC calculator data can be initialized to this value by write operation for this register. This register needs to be initialized every time doing CRC process.	0x00000000

1.7.7. GPL divider dividend data register

GPL_DIVD	GPL divider dividend data register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
GPL_DIVIDEND[31:24]							
23	22	21	20	19	18	17	16
GPL_DIVIDEND[23:16]							
15	14	13	12	11	10	9	8
GPL_DIVIDEND[15:8]							
7	6	5	4	3	2	1	0
GPL_DIVIDEND[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	GPL_DIVIDEND	This register is used to specify the dividend value for the division calculation.	0x00000000

1.7.8. GPL divider divisor data register

GPL_DIVS	GPL divider divisor data register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
GPL_DIVISOR[31:24]							
23	22	21	20	19	18	17	16
GPL_DIVISOR[23:16]							
15	14	13	12	11	10	9	8
GPL_DIVISOR[15:8]							
7	6	5	4	3	2	1	0
GPL_DIVISOR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	GPL_DIVISOR	This register is used to specify the divisor value for the division calculation.	0x00000000

1.7.9. GPL divider quotient data register

GPL_QUT	GPL divider quotient data register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
GPL_QUOTIENT[31:24]							
23	22	21	20	19	18	17	16
GPL_QUOTIENT[23:16]							
15	14	13	12	11	10	9	8
GPL_QUOTIENT[15:8]							
7	6	5	4	3	2	1	0
GPL_QUOTIENT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	GPL_QUOTIENT	This register is used to record the quotient value for the division calculation.	0x00000000

1.7.10. GPL divider remainder data register

GPL_REM	GPL divider remainder data register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
GPL_REMAINDER[31:24]							
23	22	21	20	19	18	17	16
GPL_REMAINDER[23:16]							
15	14	13	12	11	10	9	8
GPL_REMAINDER[15:8]							
7	6	5	4	3	2	1	0
GPL_REMAINDER[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	GPL_REMAINDER	This register is used to record the remainder value for the division calculation.	0x00000000

1.7.11. GPL Register Map

GPL Register Map Register Number = 10

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	GPL_STA	Reserved																Reserved	GPL_PAR32_OUT	GPL_PAR16_OUT [1:0]		GPL_PAR8_OUT [3:0]				Reserved					GPL_DIVZEF	GPL_DIVCF	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	GPL_CR0	GPL_DMA_EN	Reserved	Reserved						Reserved								Reserved					GPL_PAR_POL	Reserved		Reserved	GPL_IN_INV	Reserved	GPL_BEND16_EN	GPL_BREV_MDS [1:0]		GPL_BEND_EN	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	GPL_CR1	Reserved							GPL_DIV_START	Reserved							GPL_DIV_TYPE	Reserved						Reserved		GPL_CRC_BREV [1:0]		GPL_CRC_DSIZE [1:0]		GPL_CRC_MDS [1:0]		Reserved	GPL_CRC_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	GPL_DIN	GPL_DIN[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	GPL_DOUT	GPL_DOUT[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	GPL_CRCINIT	GPL_CRC_INIT [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	GPL_DIVD	GPL_DIVIDEND [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	GPL_DIVS	GPL_DIVISOR [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x38	GPL_QUT	GPL_QUOTIENT [31:0]
Reset	0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0x3C	GPL_REM	GPL_REMAINDER [31:0]
Reset	0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

1.8. DMA Control Registers

DMA Control	(DMA) Direct Memory Access Control
Base Address :	0x4BF00000

1.8.1. DMA status register

DMA_STA	DMA status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved				DMA_CH4_ERRF	DMA_CH4_THF	DMA_CH4_TCF	DMA_CH4_GIF
15	14	13	12	11	10	9	8
DMA_CH3_ERRF	DMA_CH3_THF	DMA_CH3_TCF	DMA_CH3_GIF	DMA_CH2_ERRF	DMA_CH2_THF	DMA_CH2_TCF	DMA_CH2_GIF
7	6	5	4	3	2	1	0
DMA_CH1_ERRF	DMA_CH1_THF	DMA_CH1_TCF	DMA_CH1_GIF	DMA_CH0_ERRF	DMA_CH0_THF	DMA_CH0_TCF	DMA_CH0_GIF

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..20	-	Reserved	Reserved	0x00
19	rw	DMA_CH4_ERRF	DMA channel-4 transfer error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
18	rw	DMA_CH4_THF	DMA channel-4 transfer half flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
17	rw	DMA_CH4_TCF	DMA channel-4 transfer complete flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
16	r	DMA_CH4_GIF	DMA channel-4 global interrupt flag. This bit will be set if any of other channel event interrupt flag is set. 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
15	rw	DMA_CH3_ERRF	DMA channel-3 transfer error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
14	rw	DMA_CH3_THF	DMA channel-3 transfer half flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
13	rw	DMA_CH3_TCF	DMA channel-3 transfer complete flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
12	r	DMA_CH3_GIF	DMA channel-3 global interrupt flag. This bit will be set if any of other channel event interrupt flag is set. 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
11	rw	DMA_CH2_ERRF	DMA channel-2 transfer error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
10	rw	DMA_CH2_THF	DMA channel-2 transfer half flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred)	0x00

			1 = Happened (reset event happened)	
9	rw	DMA_CH2_TCF	DMA channel-2 transfer complete flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
8	r	DMA_CH2_GIF	DMA channel-2 global interrupt flag. This bit will be set if any of other channel event interrupt flag is set. 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
7	rw	DMA_CH1_ERRF	DMA channel-1 transfer error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
6	rw	DMA_CH1_THF	DMA channel-1 transfer half flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
5	rw	DMA_CH1_TCF	DMA channel-1 transfer complete flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
4	r	DMA_CH1_GIF	DMA channel-1 global interrupt flag. This bit will be set if any of other channel event interrupt flag is set. 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
3	rw	DMA_CH0_ERRF	DMA channel-0 transfer error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
2	rw	DMA_CH0_THF	DMA channel-0 transfer half flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
1	rw	DMA_CH0_TCF	DMA channel-0 transfer complete flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
0	r	DMA_CH0_GIF	DMA channel-0 global interrupt flag. This bit will be set if any of other channel event interrupt flag is set. 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00

1.8.2. DMA interrupt enable register

DMA_INT	DMA interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							DMA_IEA

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..1	-	Reserved	Reserved	0x00

0	rw	DMA_IEA	DMA interrupt all enable. When disables, the INT_DMA global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.8.3. DMA global control register 0

DMA_CR0	DMA global control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			DMA_CH4_ENB	DMA_CH3_ENB	DMA_CH2_ENB	DMA_CH1_ENB	DMA_CH0_ENB
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	DMA_GPL_CHS[2:0]			Reserved	DMA_FGBUS_SEL	DMA_PRI_MDS	DMA_EN

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..21	-	Reserved	Reserved	0x00
20	rw	DMA_CH4_ENB	DMA channel-4 operation enable bit. This bit is as same as DMA_CH4_EN. 0 = Disable 1 = Enable	0x00
19	rw	DMA_CH3_ENB	DMA channel-3 operation enable bit. This bit is as same as DMA_CH3_EN. 0 = Disable 1 = Enable	0x00
18	rw	DMA_CH2_ENB	DMA channel-2 operation enable bit. This bit is as same as DMA_CH2_EN. 0 = Disable 1 = Enable	0x00
17	rw	DMA_CH1_ENB	DMA channel-1 operation enable bit. This bit is as same as DMA_CH1_EN. 0 = Disable 1 = Enable	0x00
16	rw	DMA_CH0_ENB	DMA channel-0 operation enable bit. This bit is as same as DMA_CH0_EN. 0 = Disable 1 = Enable	0x00
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6..4	rw	DMA_GPL_CHS	DMA channel select for extra GPL function. These bits are used to disable or select one channel to send the channel transfer data extra to GPL. The choice channel processes the DMA operation which one request source transfers to another destination. The GPL is including of CRC, byte order change, bit order change, …. 0x0 = Disable : no any channel with GPL function 0x1 = CH0 0x2 = CH1 0x3 = CH2 0x4 = CH3 0x5 = CH4	0x00
3	-	Reserved	Reserved	0x00
2	rw	DMA_FGBUS_SEL	DMA flash-to-GPL transfer bus width select. When selects 1BYTE, the byte number is 1-byte for each transferred data	0x00

			cycle. When selects 4BYTE, the byte number is 4-byte for each transferred data cycle. User can set 4BYTE only for flash-to-GPL DMA data transfer with DMA channel-0 using only. It muse set 1BYTE for other DMA data transfer conditions. 0 = 1BYTE (8-bit) 1 = 4BYTE (32-bit)	
1	rw	DMA_PRI_MDS	DMA channel priority mode select. 0 = Round : control by Round Robin method 1 = Level : control by channel priority level	0x00
0	rw	DMA_EN	DMA controller enable. 0 = Disable 1 = Enable	0x00

1.8.4. DMA channel-0 control register 0

DMA_CH0A	DMA channel-0 control register 0		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				DMA_CH0_ERR2F	DMA_CH0_TH2F	DMA_CH0_TC2F	Reserved
23	22	21	20	19	18	17	16
Reserved				DMA_CH0_EIE	DMA_CH0_HIE	DMA_CH0_CIE	Reserved
15	14	13	12	11	10	9	8
DMA_CH0_REQ	Reserved	DMA_CH0_BSIZE[1:0]		DMA_CH0_PLS[1:0]		DMA_CH0_XMDS[1:0]	
7	6	5	4	3	2	1	0
Reserved	DMA_CH0_LAST	Reserved		DMA_CH0_ADSEL	DMA_CH0_LOOP	DMA_CH0_HOLD	DMA_CH0_EN

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	DMA_CH0_ERR2F	DMA channel-0 transfer error flag. This bit is same as DMA_CH0_ERRF. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
26	rw	DMA_CH0_TH2F	DMA channel-0 transfer half flag. This bit is same as DMA_CH0_THF. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
25	rw	DMA_CH0_TC2F	DMA channel-0 transfer complete flag. This bit is same as DMA_CH0_TCF. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
24	-	Reserved	Reserved	0x00
23..20	-	Reserved	Reserved	0x00
19	rw	DMA_CH0_EIE	DMA channel-0 transfer error interrupt enable. 0 = Disable 1 = Enable	0x00
18	rw	DMA_CH0_HIE	DMA channel-0 transfer half interrupt enable. 0 = Disable 1 = Enable	0x00
17	rw	DMA_CH0_CIE	DMA channel-0 transfer complete interrupt enable. 0 = Disable 1 = Enable	0x00
16	-	Reserved	Reserved	0x00
15	rw	DMA_CH0_REQ	DMA channel data transfer request enable. This bit is auto clear by hardware after transfer complete. 0 = No : no effect 1 = Enable	0x00

14	-	**Reserved**	Reserved	0x00
13..12	rw	**DMA_CH0_BSIZE**	DMA transfer burst size. Indicates the number of transfers that make up a single DMA data transfer. This value must be set to the data size of the peripheral. For example, set Two or Four for ADC 16-bit or 32-bit data transfer setting. 0x0 = One 0x1 = Two 0x2 = Reserved 0x3 = Four	0x00
11..10	rw	**DMA_CH0_PLS**	DMA channel priority level select. 0x0 = LV0 : lowest priority 0x1 = LV1 : normal priority 0x2 = LV2 : high priority 0x3 = LV3 : highest priority	0x00
9..8	rw	**DMA_CH0_XMDS**	DMA channel external pin trigger request mode select. When selects value 1~3, the DMA request is forced from external pin and disables internal peripheral connections or software request by DMA_CHn_REQ setting. (n=channel index) 0x0 = Disable : disable external request pin input 0x1 = Single : single request mode 0x2 = Block : block request mode 0x3 = Demand : demand request mode(active high)	0x00
7	-	**Reserved**	Reserved	0x00
6	rw	**DMA_CH0_LAST**	DMA Channel-0 last loop command. When the DMA channel is enabled the loop mode, this bit is set to command DMA controller to indicate the next loop is the last loop. This bit is set by software and hardware cleared after last loop DMA process finished. 0 = Not 1 = Yes	0x00
5..4	-	**Reserved**	Reserved	0x00
3	rw	**DMA_CH0_ADSEL**	DMA address increased mode select. When selects Skip3 mode, the Lsb word address is increased from 0 to 1, 1 to 2, 2 to 0 and skip address 3. 0 = Normal : sequential increment 1 1 = SKIP3 : address increment from 0 to 1,2 then return 0	0x00
2	rw	**DMA_CH0_LOOP**	DMA loop mode enable. When enables, the number of transaction data is automatically reloaded with the initial value in DMA_CHn_NUM and the DMA requests will be continuous. Also the source and destination memory transfer current address counters are automatically reloaded with the initial value in DMA_CHn_SSA and DMA_CHn_DSA. (n=channel index) 0 = Disable 1 = Enable	0x00
1	rw	**DMA_CH0_HOLD**	DMA channel operation hold enable. When enables, the DMA transfer operation is hold until this bit is disabled. The hold function is no effect for external pin trigger request mode. 0 = Disable 1 = Enable	0x00
0	rw	**DMA_CH0_EN**	DMA channel operation enable. When enables, this channel can be configure. When disables, this channel will be reset. 0 = Disable 1 = Enable	0x00

1.8.5. DMA channel-0 control register 1

DMA_CH0B	**DMA channel-0 control register 1**		
Offset Address :	**0x24**	**Reset Value :**	**0x00030000**

31	30	29	28	27	26	25	24

Reserved							DMA_CH0_XPIN
23	22	21	20	19	18	17	16
Reserved		Reserved		DMA_CH0_DSYNC	DMA_CH0_SSYNC	DMA_CH0_DINC	DMA_CH0_SINC
15	14	13	12	11	10	9	8
Reserved				DMA_CH0_DET[3:0]			
7	6	5	4	3	2	1	0
Reserved				DMA_CH0_SRC[3:0]			

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	DMA_CH0_XPIN	DMA channel external trigger pin select. 0x0 = TRG0 : DMA_TRG0 pin 0x1 = TRG1 : DMA_TRG1 pin	0x00
23..22	-	Reserved	Reserved	0x00
21..20	-	Reserved	Reserved	0x00
19	rw	DMA_CH0_DSYNC	DMA destination process synchronization enable bit. When the destination process clock frequency equals to DMA process clock frequency, suggests enabling this bit to improve DMA performance. 0 = Disable 1 = Enable	0x00
18	rw	DMA_CH0_SSYNC	DMA source process synchronization enable bit. When the source process clock frequency equals to DMA process clock frequency, suggests enabling this bit to improve DMA performance. 0 = Disable 1 = Enable	0x00
17	rw	DMA_CH0_DINC	DMA destination memory transfer address auto increased enable. When disables, the address is fixed after each burst data transfer complete. 0 = Disable 1 = Enable	0x01
16	rw	DMA_CH0_SINC	DMA source memory transfer address auto increased enable. When disables, the address is fixed after each burst data transfer complete. 0 = Disable 1 = Enable	0x01
15..12	-	Reserved	Reserved	0x00
11..8	rw	DMA_CH0_DET	DMA channel transfer peripheral destination select. Refer the DMA function table for detail information.	0x00
7..4	-	Reserved	Reserved	0x00
3..0	rw	DMA_CH0_SRC	DMA channel transfer peripheral source select. Refer the DMA function table for detail information.	0x00

1.8.6. DMA channel-0 control register 1

DMA_CH0NUM	DMA channel-0 control register 1		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							DMA_CH0_NUM
15	14	13	12	11	10	9	8
DMA_CH0_NUM[15:8]							
7	6	5	4	3	2	1	0
DMA_CH0_NUM[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00

23..17	-	Reserved	Reserved	0x00
16..0	rw	DMA_CH0_NUM	DMA transfer data count initial number. Value 0 is meaning that 131072 data needs to be transferred and value 0x1FFFF is transferred 131071 data. This register value must equal the integer multiples of DMA_CH0_BSIZE setting size.	0x000000

1.8.7. DMA channel-0 control register 1

DMA_CH0CNT	DMA channel-0 control register 1		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							DMA_CH0_CNT
15	14	13	12	11	10	9	8
DMA_CH0_CNT[15:8]							
7	6	5	4	3	2	1	0
DMA_CH0_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..17	-	Reserved	Reserved	0x00
16..0	r	DMA_CH0_CNT	DMA transfer data count current value. Value 0 is meaning that data transfer is finished or 131072 data wants to be transferred and value 0x1FFFF is still necessary to transfer 131071 data. This register is read to indicate the remaining bytes to be transmitted. This register decreases after each DMA transfer. When DMA_CH0_LOOP is enabled, this register will be reloaded automatically by DMA_CH0_NUM after previous transfer is completed.	0x000000

1.8.8. DMA channel-0 source start address register

DMA_CH0SSA	DMA channel-0 source start address register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH0_SSA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH0_SSA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH0_SSA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH0_SSA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	DMA_CH0_SSA	DMA source memory transfer start address.	0x00000000

1.8.9. DMA channel-0 source current address register

DMA_CH0SCA	DMA channel-0 source current address register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH0_SCA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH0_SCA[23:16]							
15	14	13	12	11	10	9	8

DMA_CH0_SCA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH0_SCA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	DMA_CH0_SCA	DMA source memory transfer current address. The address operation range is limited in a 128K aligned address space. When the address is operating over the 128K boundary, the address is rolling up to 0x0000 of the 128K aligned address space.	0x00000000

1.8.10. DMA channel-0 destination start address register

DMA_CH0DSA	DMA channel-0 destination start address register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH0_DSA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH0_DSA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH0_DSA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH0_DSA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	DMA_CH0_DSA	DMA destination memory transfer start address.	0x00000000

1.8.11. DMA channel-0 destination current address register

DMA_CH0DCA	DMA channel-0 destination current address register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH0_DCA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH0_DCA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH0_DCA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH0_DCA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	DMA_CH0_DCA	DMA destination memory transfer current address. The address operation range is limited in a 64K aligned address space. When the address is operating over the 64K boundary, the address is rolling up to 0x0000 of the 64K aligned address space.	0x00000000

1.8.12. DMA channel-1 control register 0

DMA_CH1A	DMA channel-1 control register 0		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				DMA_CH1_ERR2F	DMA_CH1_TH2F	DMA_CH1_TC2F	Reserved
23	22	21	20	19	18	17	16
Reserved				DMA_CH1_EIE	DMA_CH1_HIE	DMA_CH1_CIE	Reserved
15	14	13	12	11	10	9	8

DMA_CH1_REQ	Reserved	DMA_CH1_BSIZE[1:0]		DMA_CH1_PLS[1:0]		DMA_CH1_XMDS[1:0]	
7	6	5	4	3	2	1	0
Reserved	DMA_CH1_LAST	Reserved		DMA_CH1_ADSEL	DMA_CH1_LOOP	DMA_CH1_HOLD	DMA_CH1_EN

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	DMA_CH1_ERR2F	DMA channel-1 transfer error flag. This bit is same as DMA_CH1_ERRF. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
26	rw	DMA_CH1_TH2F	DMA channel-1 transfer half flag. This bit is same as DMA_CH1_THF .(set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
25	rw	DMA_CH1_TC2F	DMA channel-1 transfer complete flag. This bit is same as DMA_CH1_TCF. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
24	-	Reserved	Reserved	0x00
23..20	-	Reserved	Reserved	0x00
19	rw	DMA_CH1_EIE	DMA channel-1 transfer error interrupt enable. 0 = Disable 1 = Enable	0x00
18	rw	DMA_CH1_HIE	DMA channel-1 transfer half interrupt enable. 0 = Disable 1 = Enable	0x00
17	rw	DMA_CH1_CIE	DMA channel-1 transfer complete interrupt enable. 0 = Disable 1 = Enable	0x00
16	-	Reserved	Reserved	0x00
15	rw	DMA_CH1_REQ	DMA channel data transfer request enable. This bit is auto clear by hardware after transfer complete. 0 = No : no effect 1 = Enable	0x00
14	-	Reserved	Reserved	0x00
13..12	rw	DMA_CH1_BSIZE	DMA transfer burst size. Indicates the number of transfers that make up a single DMA data transfer. This value must be set to the data size of the peripheral. For example, set Two or Four for ADC 16-bit or 32-bit data transfer setting. 0x0 = One 0x1 = Two 0x2 = Reserved 0x3 = Four	0x00
11..10	rw	DMA_CH1_PLS	DMA channel priority level select. 0x0 = LV0 : lowest priority 0x1 = LV1 : normal priority 0x2 = LV2 : high priority 0x3 = LV3 : highest priority	0x00
9..8	rw	DMA_CH1_XMDS	DMA channel external pin trigger request mode select. When selects value 1~3, the DMA request is forced from external pin and disables internal peripheral connections or software request by DMA_CHn_REQ setting. (n=channel index) 0x0 = Disable : disable external request pin input 0x1 = Single : single request mode 0x2 = Block : block request mode 0x3 = Demand : demand request mode(active high)	0x00
7	-	Reserved	Reserved	0x00

6	rw	DMA_CH1_LAST	DMA Channel last loop command. When the DMA channel is enabled the loop mode, this bit is set to command DMA controller to indicate the next loop is the last loop. This bit is set by software and hardware cleared after last loop DMA process finished. 0 = Not 1 = Yes	0x00
5..4	-	Reserved	Reserved	0x00
3	rw	DMA_CH1_ADSEL	DMA address increased mode select. When selects Skip3 mode, the Lsb word address is increased from 0 to 1, 1 to 2, 2 to 0 and skip address 3. 0 = Normal : sequential increment 1 1 = SKIP3 : address increment from 0 to 1,2 then return 0	0x00
2	rw	DMA_CH1_LOOP	DMA loop mode enable. When enables, the number of transaction data is automatically reloaded with the initial value in DMA_CHn_NUM and the DMA requests will be continuous. Also the source and destination memory transfer current address counters are automatically reloaded with the initial value in DMA_CHn_SSA and DMA_CHn_DSA. (n=channel index) 0 = Disable 1 = Enable	0x00
1	rw	DMA_CH1_HOLD	DMA channel operation hold enable. When enables, the DMA transfer operation is hold until this bit is disabled. The hold function is no effect for external pin trigger request mode. 0 = Disable 1 = Enable	0x00
0	rw	DMA_CH1_EN	DMA channel operation enable. When enables, this channel can be configure. When disables, this channel will be reset. 0 = Disable 1 = Enable	0x00

1.8.13. DMA channel-1 control register 1

DMA_CH1B	DMA channel-1 control register 1		
Offset Address :	0x44	Reset Value :	0x00030000

31	30	29	28	27	26	25	24
Reserved							DMA_CH1_XPIN
23	22	21	20	19	18	17	16
Reserved		Reserved		DMA_CH1_DSYNC	DMA_CH1_SSYNC	DMA_CH1_DINC	DMA_CH1_SINC
15	14	13	12	11	10	9	8
Reserved				DMA_CH1_DET[3:0]			
7	6	5	4	3	2	1	0
Reserved				DMA_CH1_SRC[3:0]			

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	DMA_CH1_XPIN	DMA channel external trigger pin select. 0x0 = TRG0 : DMA_TRG0 pin 0x1 = TRG1 : DMA_TRG1 pin	0x00
23..22	-	Reserved	Reserved	0x00
21..20	-	Reserved	Reserved	0x00
19	rw	DMA_CH1_DSYNC	DMA destination process synchronization enable bit. When the destination process clock frequency equals to DMA process clock frequency, suggests enabling this bit to improve DMA performance. 0 = Disable 1 = Enable	0x00
18	rw	DMA_CH1_SSYNC	DMA source process synchronization enable bit. When the	0x00

			source process clock frequency equals to DMA process clock frequency, suggests enabling this bit to improve DMA performance. 0 = Disable 1 = Enable	
17	rw	DMA_CH1_DINC	DMA destination memory transfer address auto increased enable. When disables, the address is fixed after each burst data transfer complete. 0 = Disable 1 = Enable	0x01
16	rw	DMA_CH1_SINC	DMA source memory transfer address auto increased enable. When disables, the address is fixed after each burst data transfer complete. 0 = Disable 1 = Enable	0x01
15..12	-	Reserved	Reserved	0x00
11..8	rw	DMA_CH1_DET	DMA channel transfer peripheral destination select. Refer the DMA function table for detail information.	0x00
7..4	-	Reserved	Reserved	0x00
3..0	rw	DMA_CH1_SRC	DMA channel transfer peripheral source select. Refer the DMA function table for detail information.	0x00

1.8.14. DMA channel-1 control register 1

DMA_CH1NUM	DMA channel-1 control register 1		
Offset Address :	0x48	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
DMA_CH1_NUM[15:8]							
7	6	5	4	3	2	1	0
DMA_CH1_NUM[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	DMA_CH1_NUM	DMA transfer data count initial number. Value 0 is meaning that 65536 data needs to be transferred and value 0xFFFF is transferred 65535 data. This register value must equal the integer multiples of DMA_CH1_BSIZE setting size.	0x0000

1.8.15. DMA channel-1 control register 1

DMA_CH1CNT	DMA channel-1 control register 1		
Offset Address :	0x4C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
DMA_CH1_CNT[15:8]							
7	6	5	4	3	2	1	0
DMA_CH1_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000

15..0	r	DMA_CH1_CNT	DMA transfer data count current value. Value 0 is meaning that data transfer is finished or 65536 data wants to be transferred and value 0xFFFF is still necessary to transfer 65535 data. This register is read to indicate the remaining bytes to be transmitted. This register decreases after each DMA transfer. When DMA_CH1_LOOP is enabled, this register will be reloaded automatically by DMA_CH1_NUM after previous transfer is completed.	0x0000

1.8.16. DMA channel-1 source start address register

DMA_CH1SSA	DMA channel-1 source start address register		
Offset Address :	0x50	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH1_SSA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH1_SSA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH1_SSA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH1_SSA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	DMA_CH1_SSA	DMA source memory transfer start address.	0x00000000

1.8.17. DMA channel-1 source current address register

DMA_CH1SCA	DMA channel-1 source current address register		
Offset Address :	0x54	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH1_SCA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH1_SCA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH1_SCA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH1_SCA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	DMA_CH1_SCA	DMA source memory transfer current address. The address operation range is limited in a 64K aligned address space. When the address is operating over the 64K boundary, the address is rolling up to 0x0000 of the 64K aligned address space.	0x00000000

1.8.18. DMA channel-1 destination start address register

DMA_CH1DSA	DMA channel-1 destination start address register		
Offset Address :	0x58	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH1_DSA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH1_DSA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH1_DSA[15:8]							
7	6	5	4	3	2	1	0

DMA_CH1_DSA[7:0]

Bit	Attr	Bit Name	Description	Reset
31..0	rw	DMA_CH1_DSA	DMA destination memory transfer start address.	0x00000000

1.8.19. DMA channel-1 destination current address register

DMA_CH1DCA	DMA channel-1 destination current address register		
Offset Address :	0x5C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH1_DCA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH1_DCA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH1_DCA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH1_DCA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	DMA_CH1_DCA	DMA destination memory transfer current address. The address operation range is limited in a 64K aligned address space. When the address is operating over the 64K boundary, the address is rolling up to 0x0000 of the 64K aligned address space.	0x00000000

1.8.20. DMA channel-2 control register 0

DMA_CH2A	DMA channel-2 control register 0		
Offset Address :	0x60	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				DMA_CH2_ERR2F	DMA_CH2_TH2F	DMA_CH2_TC2F	Reserved
23	22	21	20	19	18	17	16
Reserved				DMA_CH2_EIE	DMA_CH2_HIE	DMA_CH2_CIE	Reserved
15	14	13	12	11	10	9	8
DMA_CH2_REQ	Reserved	DMA_CH2_BSIZE[1:0]		DMA_CH2_PLS[1:0]		DMA_CH2_XMDS[1:0]	
7	6	5	4	3	2	1	0
Reserved	DMA_CH2_LAST	Reserved		DMA_CH2_ADSEL	DMA_CH2_LOOP	DMA_CH2_HOLD	DMA_CH2_EN

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	DMA_CH2_ERR2F	DMA channel-2 transfer error flag. This bit is same as DMA_CH2_ERRF. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
26	rw	DMA_CH2_TH2F	DMA channel-2 transfer half flag. This bit is same as DMA_CH2_THF .(set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
25	rw	DMA_CH2_TC2F	DMA channel-2 transfer complete flag. This bit is same as DMA_CH2_TCF. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
24	-	Reserved	Reserved	0x00
23..20	-	Reserved	Reserved	0x00

19	rw	**DMA_CH2_EIE**	DMA channel-2 transfer error interrupt enable. 0 = Disable 1 = Enable	0x00
18	rw	**DMA_CH2_HIE**	DMA channel-2 transfer half interrupt enable. 0 = Disable 1 = Enable	0x00
17	rw	**DMA_CH2_CIE**	DMA channel-2 transfer complete interrupt enable. 0 = Disable 1 = Enable	0x00
16	-	**Reserved**	Reserved	0x00
15	rw	**DMA_CH2_REQ**	DMA channel data transfer request enable. This bit is auto clear by hardware after transfer complete. 0 = No : no effect 1 = Enable	0x00
14	-	**Reserved**	Reserved	0x00
13..12	rw	**DMA_CH2_BSIZE**	DMA transfer burst size. Indicates the number of transfers that make up a single DMA data transfer. This value must be set to the data size of the peripheral. For example, set Two or Four for ADC 16-bit or 32-bit data transfer setting. 0x0 = One 0x1 = Two 0x2 = Reserved 0x3 = Four	0x00
11..10	rw	**DMA_CH2_PLS**	DMA channel priority level select. 0x0 = LV0 : lowest priority 0x1 = LV1 : normal priority 0x2 = LV2 : high priority 0x3 = LV3 : highest priority	0x00
9..8	rw	**DMA_CH2_XMDS**	DMA channel external pin trigger request mode select. When selects value 1~3, the DMA request is forced from external pin and disables internal peripheral connections or software request by DMA_CHn_REQ setting. (n=channel index) 0x0 = Disable : disable external request pin input 0x1 = Single : single request mode 0x2 = Block : block request mode 0x3 = Demand : demand request mode(active high)	0x00
7	-	**Reserved**	Reserved	0x00
6	rw	**DMA_CH2_LAST**	DMA Channel last loop command. When the DMA channel is enabled the loop mode, this bit is set to command DMA controller to indicate the next loop is the last loop. This bit is set by software and hardware cleared after last loop DMA process finished. 0 = Not 1 = Yes	0x00
5..4	-	**Reserved**	Reserved	0x00
3	rw	**DMA_CH2_ADSEL**	DMA address increased mode select. When selects Skip3 mode, the Lsb word address is increased from 0 to 1, 1 to 2, 2 to 0 and skip address 3. 0 = Normal : sequential increment 1 1 = SKIP3 : address increment from 0 to 1,2 then return 0	0x00
2	rw	**DMA_CH2_LOOP**	DMA loop mode enable. When enables, the number of transaction data is automatically reloaded with the initial value in DMA_CHn_NUM and the DMA requests will be continuous. Also the source and destination memory transfer current address counters are automatically reloaded with the initial value in DMA_CHn_SSA and DMA_CHn_DSA. (n=channel index) 0 = Disable 1 = Enable	0x00
1	rw	**DMA_CH2_HOLD**	DMA channel operation hold enable. When enables, the DMA transfer operation is hold until this bit is disabled. The hold	0x00

			function is no effect for external pin trigger request mode. 0 = Disable 1 = Enable	
0	rw	DMA_CH2_EN	DMA channel operation enable. When enables, this channel can be configure. When disables, this channel will be reset. 0 = Disable 1 = Enable	0x00

1.8.21. DMA channel-2 control register 1

DMA_CH2B	DMA channel-2 control register 1		
Offset Address :	0x64	Reset Value :	0x00030000

31	30	29	28	27	26	25	24
Reserved							DMA_CH2_XPIN
23	22	21	20	19	18	17	16
Reserved		Reserved		DMA_CH2_DSYNC	DMA_CH2_SSYNC	DMA_CH2_DINC	DMA_CH2_SINC
15	14	13	12	11	10	9	8
Reserved				DMA_CH2_DET[3:0]			
7	6	5	4	3	2	1	0
Reserved				DMA_CH2_SRC[3:0]			

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	DMA_CH2_XPIN	DMA channel external trigger pin select. 0x0 = TRG0 : DMA_TRG0 pin 0x1 = TRG1 : DMA_TRG1 pin	0x00
23..22	-	Reserved	Reserved	0x00
21..20	-	Reserved	Reserved	0x00
19	rw	DMA_CH2_DSYNC	DMA destination process synchronization enable bit. When the destination process clock frequency equals to DMA process clock frequency, suggests enabling this bit to improve DMA performance. 0 = Disable 1 = Enable	0x00
18	rw	DMA_CH2_SSYNC	DMA source process synchronization enable bit. When the source process clock frequency equals to DMA process clock frequency, suggests enabling this bit to improve DMA performance. 0 = Disable 1 = Enable	0x00
17	rw	DMA_CH2_DINC	DMA destination memory transfer address auto increased enable. When disables, the address is fixed after each burst data transfer complete. 0 = Disable 1 = Enable	0x01
16	rw	DMA_CH2_SINC	DMA source memory transfer address auto increased enable. When disables, the address is fixed after each burst data transfer complete. 0 = Disable 1 = Enable	0x01
15..12	-	Reserved	Reserved	0x00
11..8	rw	DMA_CH2_DET	DMA channel transfer peripheral destination select. Refer the DMA function table for detail information.	0x00
7..4	-	Reserved	Reserved	0x00
3..0	rw	DMA_CH2_SRC	DMA channel transfer peripheral source select. Refer the DMA function table for detail information.	0x00

1.8.22. DMA channel-2 control register 1

DMA_CH2NUM	DMA channel-2 control register 1		
Offset Address :	0x68	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
DMA_CH2_NUM[15:8]							
7	6	5	4	3	2	1	0
DMA_CH2_NUM[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	DMA_CH2_NUM	DMA transfer data count initial number. Value 0 is meaning that 65536 data needs to be transferred and value 0xFFFF is transferred 65535 data. This register value must equal the integer multiples of DMA_CH2_BSIZE setting size.	0x0000

1.8.23. DMA channel-2 control register 1

DMA_CH2CNT	DMA channel-2 control register 1		
Offset Address :	0x6C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
DMA_CH2_CNT[15:8]							
7	6	5	4	3	2	1	0
DMA_CH2_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	r	DMA_CH2_CNT	DMA transfer data count current value. Value 0 is meaning that data transfer is finished or 65536 data wants to be transferred and value 0xFFFF is still necessary to transfer 65535 data. This register is read to indicate the remaining bytes to be transmitted. This register decreases after each DMA transfer. When DMA_CH2_LOOP is enabled, this register will be reloaded automatically by DMA_CH2_NUM after previous transfer is completed.	0x0000

1.8.24. DMA channel-2 source start address register

DMA_CH2SSA	DMA channel-2 source start address register		
Offset Address :	0x70	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH2_SSA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH2_SSA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH2_SSA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH2_SSA[7:0]							

Bit	Attr	Bit Name	Description	Reset

31..0	rw	DMA_CH2_SSA	DMA source memory transfer start address.	0x00000000

1.8.25. DMA channel-2 source current address register

DMA_CH2SCA	DMA channel-2 source current address register		
Offset Address :	0x74	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH2_SCA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH2_SCA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH2_SCA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH2_SCA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	DMA_CH2_SCA	DMA source memory transfer current address. The address operation range is limited in a 64K aligned address space. When the address is operating over the 64K boundary, the address is rolling up to 0x0000 of the 64K aligned address space.	0x00000000

1.8.26. DMA channel-2 destination start address register

DMA_CH2DSA	DMA channel-2 destination start address register		
Offset Address :	0x78	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH2_DSA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH2_DSA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH2_DSA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH2_DSA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	DMA_CH2_DSA	DMA destination memory transfer start address.	0x00000000

1.8.27. DMA channel-2 destination current address register

DMA_CH2DCA	DMA channel-2 destination current address register		
Offset Address :	0x7C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH2_DCA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH2_DCA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH2_DCA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH2_DCA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	DMA_CH2_DCA	DMA destination memory transfer current address. The address operation range is limited in a 64K aligned address space. When the address is operating over the 64K boundary, the address is rolling up to 0x0000 of the 64K aligned address	0x00000000

			space.	

1.8.28. DMA channel-3 control register 0

DMA_CH3A	DMA channel-3 control register 0		
Offset Address :	0x80	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				DMA_CH3_ERR2F	DMA_CH3_TH2F	DMA_CH3_TC2F	Reserved
23	22	21	20	19	18	17	16
Reserved				DMA_CH3_EIE	DMA_CH3_HIE	DMA_CH3_CIE	Reserved
15	14	13	12	11	10	9	8
DMA_CH3_REQ	Reserved	DMA_CH3_BSIZE[1:0]		DMA_CH3_PLS[1:0]		DMA_CH3_XMDS[1:0]	
7	6	5	4	3	2	1	0
Reserved	DMA_CH3_LAST	Reserved		DMA_CH3_ADSEL	DMA_CH3_LOOP	DMA_CH3_HOLD	DMA_CH3_EN

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	DMA_CH3_ERR2F	DMA channel-3 transfer error flag. This bit is same as DMA_CH3_ERRF. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
26	rw	DMA_CH3_TH2F	DMA channel-3 transfer half flag. This bit is same as DMA_CH3_THF .(set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
25	rw	DMA_CH3_TC2F	DMA channel-3 transfer complete flag. This bit is same as DMA_CH3_TCF. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
24	-	Reserved	Reserved	0x00
23..20	-	Reserved	Reserved	0x00
19	rw	DMA_CH3_EIE	DMA channel-3 transfer error interrupt enable. 0 = Disable 1 = Enable	0x00
18	rw	DMA_CH3_HIE	DMA channel-3 transfer half interrupt enable. 0 = Disable 1 = Enable	0x00
17	rw	DMA_CH3_CIE	DMA channel-3 transfer complete interrupt enable. 0 = Disable 1 = Enable	0x00
16	-	Reserved	Reserved	0x00
15	rw	DMA_CH3_REQ	DMA channel data transfer request enable. This bit is auto clear by hardware after transfer complete. 0 = No : no effect 1 = Enable	0x00
14	-	Reserved	Reserved	0x00
13..12	rw	DMA_CH3_BSIZE	DMA transfer burst size. Indicates the number of transfers that make up a single DMA data transfer. This value must be set to the data size of the peripheral. For example, set Two or Four for ADC 16-bit or 32-bit data transfer setting. 0x0 = One 0x1 = Two 0x2 = Reserved 0x3 = Four	0x00
11..10	rw	DMA_CH3_PLS	DMA channel priority level select. 0x0 = LV0 : lowest priority	0x00

			0x1 = LV1 : normal priority 0x2 = LV2 : high priority 0x3 = LV3 : highest priority	
9..8	rw	DMA_CH3_XMDS	DMA channel external pin trigger request mode select. When selects value 1~3, the DMA request is forced from external pin and disables internal peripheral connections or software request by DMA_CHn_REQ setting. (n=channel index) 0x0 = Disable : disable external request pin input 0x1 = Single : single request mode 0x2 = Block : block request mode 0x3 = Demand : demand request mode(active high)	0x00
7	-	Reserved	Reserved	0x00
6	rw	DMA_CH3_LAST	DMA Channel last loop command. When the DMA channel is enabled the loop mode, this bit is set to command DMA controller to indicate the next loop is the last loop. This bit is set by software and hardware cleared after last loop DMA process finished. 0 = Not 1 = Yes	0x00
5..4	-	Reserved	Reserved	0x00
3	rw	DMA_CH3_ADSEL	DMA address increased mode select. When selects Skip3 mode, the Lsb word address is increased from 0 to 1, 1 to 2, 2 to 0 and skip address 3. 0 = Normal : sequential increment 1 1 = SKIP3 : address increment from 0 to 1,2 then return 0	0x00
2	rw	DMA_CH3_LOOP	DMA loop mode enable. When enables, the number of transaction data is automatically reloaded with the initial value in DMA_CHn_NUM and the DMA requests will be continuous. Also the source and destination memory transfer current address counters are automatically reloaded with the initial value in DMA_CHn_SSA and DMA_CHn_DSA. (n=channel index) 0 = Disable 1 = Enable	0x00
1	rw	DMA_CH3_HOLD	DMA channel operation hold enable. When enables, the DMA transfer operation is hold until this bit is disabled. The hold function is no effect for external pin trigger request mode. 0 = Disable 1 = Enable	0x00
0	rw	DMA_CH3_EN	DMA channel operation enable. When enables, this channel can be configure. When disables, this channel will be reset. 0 = Disable 1 = Enable	0x00

1.8.29. DMA channel-3 control register 1

DMA_CH3B	DMA channel-3 control register 1		
Offset Address :	0x84	Reset Value :	0x00030000

31	30	29	28	27	26	25	24
Reserved							DMA_CH3_XPIN
23	22	21	20	19	18	17	16
Reserved		Reserved		DMA_CH3_DSYNC	DMA_CH3_SSYNC	DMA_CH3_DINC	DMA_CH3_SINC
15	14	13	12	11	10	9	8
Reserved				DMA_CH3_DET[3:0]			
7	6	5	4	3	2	1	0
Reserved				DMA_CH3_SRC[3:0]			

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00

24	rw	DMA_CH3_XPIN	DMA channel external trigger pin select. 0x0 = TRG0 : DMA_TRG0 pin 0x1 = TRG1 : DMA_TRG1 pin	0x00
23..22	-	Reserved	Reserved	0x00
21..20	-	Reserved	Reserved	0x00
19	rw	DMA_CH3_DSYNC	DMA destination process synchronization enable bit. When the destination process clock frequency equals to DMA process clock frequency, suggests enabling this bit to improve DMA performance. 0 = Disable 1 = Enable	0x00
18	rw	DMA_CH3_SSYNC	DMA source process synchronization enable bit. When the source process clock frequency equals to DMA process clock frequency, suggests enabling this bit to improve DMA performance. 0 = Disable 1 = Enable	0x00
17	rw	DMA_CH3_DINC	DMA destination memory transfer address auto increased enable. When disables, the address is fixed after each burst data transfer complete. 0 = Disable 1 = Enable	0x01
16	rw	DMA_CH3_SINC	DMA source memory transfer address auto increased enable. When disables, the address is fixed after each burst data transfer complete. 0 = Disable 1 = Enable	0x01
15..12	-	Reserved	Reserved	0x00
11..8	rw	DMA_CH3_DET	DMA channel transfer peripheral destination select. Refer the DMA function table for detail information.	0x00
7..4	-	Reserved	Reserved	0x00
3..0	rw	DMA_CH3_SRC	DMA channel transfer peripheral source select. Refer the DMA function table for detail information.	0x00

1.8.30. DMA channel-3 control register 1

DMA_CH3NUM	DMA channel-3 control register 1		
Offset Address :	0x88	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							DMA_CH3_NUM
15	14	13	12	11	10	9	8
DMA_CH3_NUM[15:8]							
7	6	5	4	3	2	1	0
DMA_CH3_NUM[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..17	-	Reserved	Reserved	0x00
16..0	rw	DMA_CH3_NUM	DMA transfer data count initial number. Value 0 is meaning that 131072 data needs to be transferred and value 0x1FFFF is transferred 131071 data. This register value must equal the integer multiples of DMA_CH3_BSIZE setting size.	0x000000

1.8.31. DMA channel-3 control register 1

DMA_CH3CNT	DMA channel-3 control register 1		
Offset Address :	0x8C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							DMA_CH3_CNT
15	14	13	12	11	10	9	8
DMA_CH3_CNT[15:8]							
7	6	5	4	3	2	1	0
DMA_CH3_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..17	-	Reserved	Reserved	0x00
16..0	r	DMA_CH3_CNT	DMA transfer data count current value. Value 0 is meaning that data transfer is finished or 131072 data wants to be transferred and value 0x1FFFF is still necessary to transfer 131071 data. This register is read to indicate the remaining bytes to be transmitted. This register decreases after each DMA transfer. When DMA_CH3_LOOP is enabled, this register will be reloaded automatically by DMA_CH3_NUM after previous transfer is completed.	0x000000

1.8.32. DMA channel-3 source start address register

DMA_CH3SSA	DMA channel-3 source start address register		
Offset Address :	0x90	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH3_SSA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH3_SSA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH3_SSA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH3_SSA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	DMA_CH3_SSA	DMA source memory transfer start address.	0x00000000

1.8.33. DMA channel-3 source current address register

DMA_CH3SCA	DMA channel-3 source current address register		
Offset Address :	0x94	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH3_SCA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH3_SCA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH3_SCA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH3_SCA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	DMA_CH3_SCA	DMA source memory transfer current address. The address operation range is limited in a 128K aligned address space. When the address is operating over the 128K boundary, the address is rolling up to 0x0000 of the 128K aligned address space.	0x00000000

1.8.34. DMA channel-3 destination start address register

DMA_CH3DSA	DMA channel-3 destination start address register		
Offset Address :	0x98	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH3_DSA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH3_DSA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH3_DSA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH3_DSA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	DMA_CH3_DSA	DMA destination memory transfer start address.	0x00000000

1.8.35. DMA channel-3 destination current address register

DMA_CH3DCA	DMA channel-3 destination current address register		
Offset Address :	0x9C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH3_DCA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH3_DCA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH3_DCA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH3_DCA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	DMA_CH3_DCA	DMA destination memory transfer current address. The address operation range is limited in a 64K aligned address space. When the address is operating over the 64K boundary, the address is rolling up to 0x0000 of the 64K aligned address space.	0x00000000

1.8.36. DMA channel-4 control register 0

DMA_CH4A	DMA channel-4 control register 0		
Offset Address :	0xA0	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				DMA_CH4_ERR2F	DMA_CH4_TH2F	DMA_CH4_TC2F	Reserved
23	22	21	20	19	18	17	16
Reserved				DMA_CH4_EIE	DMA_CH4_HIE	DMA_CH4_CIE	Reserved
15	14	13	12	11	10	9	8
DMA_CH4_REQ	Reserved	DMA_CH4_BSIZE[1:0]		DMA_CH4_PLS[1:0]		DMA_CH4_XMDS[1:0]	
7	6	5	4	3	2	1	0
Reserved	DMA_CH4_LAST	Reserved		DMA_CH4_ADSEL	DMA_CH4_LOOP	DMA_CH4_HOLD	DMA_CH4_EN

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	DMA_CH4_ERR2F	DMA channel-4 transfer error flag. This bit is same as DMA_CH4_ERRF. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred)	0x00

			1 = Happened (reset event happened)	
26	rw	DMA_CH4_TH2F	DMA channel-4 transfer half flag. This bit is same as DMA_CH4_THF .(set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
25	rw	DMA_CH4_TC2F	DMA channel-4 transfer complete flag. This bit is same as DMA_CH4_TCF. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
24	-	Reserved	Reserved	0x00
23..20	-	Reserved	Reserved	0x00
19	rw	DMA_CH4_EIE	DMA channel-4 transfer error interrupt enable. 0 = Disable 1 = Enable	0x00
18	rw	DMA_CH4_HIE	DMA channel-4 transfer half interrupt enable. 0 = Disable 1 = Enable	0x00
17	rw	DMA_CH4_CIE	DMA channel-4 transfer complete interrupt enable. 0 = Disable 1 = Enable	0x00
16	-	Reserved	Reserved	0x00
15	rw	DMA_CH4_REQ	DMA channel data transfer request enable. This bit is auto clear by hardware after transfer complete. 0 = No : no effect 1 = Enable	0x00
14	-	Reserved	Reserved	0x00
13..12	rw	DMA_CH4_BSIZE	DMA transfer burst size. Indicates the number of transfers that make up a single DMA data transfer. This value must be set to the data size of the peripheral. For example, set Two or Four for ADC 16-bit or 32-bit data transfer setting. 0x0 = One 0x1 = Two 0x2 = Reserved 0x3 = Four	0x00
11..10	rw	DMA_CH4_PLS	DMA channel priority level select. 0x0 = LV0 : lowest priority 0x1 = LV1 : normal priority 0x2 = LV2 : high priority 0x3 = LV3 : highest priority	0x00
9..8	rw	DMA_CH4_XMDS	DMA channel external pin trigger request mode select. When selects value 1~3, the DMA request is forced from external pin and disables internal peripheral connections or software request by DMA_CHn_REQ setting. (n=channel index) 0x0 = Disable : disable external request pin input 0x1 = Single : single request mode 0x2 = Block : block request mode 0x3 = Demand : demand request mode(active high)	0x00
7	-	Reserved	Reserved	0x00
6	rw	DMA_CH4_LAST	DMA Channel last loop command. When the DMA channel is enabled the loop mode, this bit is set to command DMA controller to indicate the next loop is the last loop. This bit is set by software and hardware cleared after last loop DMA process finished. 0 = Not 1 = Yes	0x00
5..4	-	Reserved	Reserved	0x00
3	rw	DMA_CH4_ADSEL	DMA address increased mode select. When selects Skip3 mode, the Lsb word address is increased from 0 to 1, 1 to 2, 2 to 0 and skip address 3.	0x00

			0 = Normal : sequential increment 1 1 = SKIP3 : address increment from 0 to 1,2 then return 0	
2	rw	DMA_CH4_LOOP	DMA loop mode enable. When enables, the number of transaction data is automatically reloaded with the initial value in DMA_CHn_NUM and the DMA requests will be continuous. Also the source and destination memory transfer current address counters are automatically reloaded with the initial value in DMA_CHn_SSA and DMA_CHn_DSA. (n=channel index) 0 = Disable 1 = Enable	0x00
1	rw	DMA_CH4_HOLD	DMA channel operation hold enable. When enables, the DMA transfer operation is hold until this bit is disabled. The hold function is no effect for external pin trigger request mode. 0 = Disable 1 = Enable	0x00
0	rw	DMA_CH4_EN	DMA channel operation enable. When enables, this channel can be configure. When disables, this channel will be reset. 0 = Disable 1 = Enable	0x00

1.8.37. DMA channel-4 control register 1

DMA_CH4B	DMA channel-4 control register 1		
Offset Address :	0xA4	Reset Value :	0x00030000

31	30	29	28	27	26	25	24
Reserved							DMA_CH4_XPIN
23	22	21	20	19	18	17	16
Reserved		Reserved		DMA_CH4_DSYNC	DMA_CH4_SSYNC	DMA_CH4_DINC	DMA_CH4_SINC
15	14	13	12	11	10	9	8
Reserved				DMA_CH4_DET[3:0]			
7	6	5	4	3	2	1	0
Reserved				DMA_CH4_SRC[3:0]			

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	DMA_CH4_XPIN	DMA channel external trigger pin select. 0x0 = TRG0 : DMA_TRG0 pin 0x1 = TRG1 : DMA_TRG1 pin	0x00
23..22	-	Reserved	Reserved	0x00
21..20	-	Reserved	Reserved	0x00
19	rw	DMA_CH4_DSYNC	DMA destination process synchronization enable bit. When the destination process clock frequency equals to DMA process clock frequency, suggests enabling this bit to improve DMA performance. 0 = Disable 1 = Enable	0x00
18	rw	DMA_CH4_SSYNC	DMA source process synchronization enable bit. When the source process clock frequency equals to DMA process clock frequency, suggests enabling this bit to improve DMA performance. 0 = Disable 1 = Enable	0x00
17	rw	DMA_CH4_DINC	DMA destination memory transfer address auto increased enable. When disables, the address is fixed after each burst data transfer complete. 0 = Disable 1 = Enable	0x01
16	rw	DMA_CH4_SINC	DMA source memory transfer address auto increased enable.	0x01

			When disables, the address is fixed after each burst data transfer complete. 0 = Disable 1 = Enable	
15..12	-	Reserved	Reserved	0x00
11..8	rw	DMA_CH4_DET	DMA channel transfer peripheral destination select. Refer the DMA function table for detail information.	0x00
7..4	-	Reserved	Reserved	0x00
3..0	rw	DMA_CH4_SRC	DMA channel transfer peripheral source select. Refer the DMA function table for detail information.	0x00

1.8.38. DMA channel-4 control register 1

DMA_CH4NUM	DMA channel-4 control register 1		
Offset Address :	0xA8	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
DMA_CH4_NUM[15:8]							
7	6	5	4	3	2	1	0
DMA_CH4_NUM[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	DMA_CH4_NUM	DMA transfer data count initial number. Value 0 is meaning that 65536 data needs to be transferred and value 0xFFFF is transferred 65535 data. This register value must equal the integer multiples of DMA_CH4_BSIZE setting size.	0x0000

1.8.39. DMA channel-4 control register 1

DMA_CH4CNT	DMA channel-4 control register 1		
Offset Address :	0xAC	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
DMA_CH4_CNT[15:8]							
7	6	5	4	3	2	1	0
DMA_CH4_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	r	DMA_CH4_CNT	DMA transfer data count current value. Value 0 is meaning that data transfer is finished or 65536 data wants to be transferred and value 0xFFFF is still necessary to transfer 65535 data. This register is read to indicate the remaining bytes to be transmitted. This register decreases after each DMA transfer. When DMA_CH4_LOOP is enabled, this register will be reloaded automatically by DMA_CH4_NUM after previous transfer is completed.	0x0000

1.8.40. DMA channel-4 source start address register

DMA_CH4SSA	DMA channel-4 source start address register		
Offset Address :	0xB0	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH4_SSA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH4_SSA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH4_SSA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH4_SSA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	DMA_CH4_SSA	DMA source memory transfer start address.	0x00000000

1.8.41. DMA channel-4 source current address register

DMA_CH4SCA	DMA channel-4 source current address register		
Offset Address :	0xB4	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH4_SCA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH4_SCA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH4_SCA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH4_SCA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	DMA_CH4_SCA	DMA source memory transfer current address. The address operation range is limited in a 64K aligned address space. When the address is operating over the 64K boundary, the address is rolling up to 0x0000 of the 64K aligned address space.	0x00000000

1.8.42. DMA channel-4 destination start address register

DMA_CH4DSA	DMA channel-4 destination start address register		
Offset Address :	0xB8	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DMA_CH4_DSA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH4_DSA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH4_DSA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH4_DSA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	DMA_CH4_DSA	DMA destination memory transfer start address.	0x00000000

1.8.43. DMA channel-4 destination current address register

DMA_CH4DCA	DMA channel-4 destination current address register		
Offset Address :	0xBC	Reset Value :	0x00000000

31	30	29	28	27	26	25	24

DMA_CH4_DCA[31:24]							
23	22	21	20	19	18	17	16
DMA_CH4_DCA[23:16]							
15	14	13	12	11	10	9	8
DMA_CH4_DCA[15:8]							
7	6	5	4	3	2	1	0
DMA_CH4_DCA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	DMA_CH4_DCA	DMA destination memory transfer current address. The address operation range is limited in a 64K aligned address space. When the address is operating over the 64K boundary, the address is rolling up to 0x0000 of the 64K aligned address space.	0x00000000

1.8.44. DMA Register Map

DMA Register Map **Register Number = 43**

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	DMA_STA	Reserved								Reserved				DMA_CH4_ERRF	DMA_CH4_THF	DMA_CH4_TCF	DMA_CH4_GIF	DMA_CH3_ERRF	DMA_CH3_THF	DMA_CH3_TCF	DMA_CH3_GIF	DMA_CH2_ERRF	DMA_CH2_THF	DMA_CH2_TCF	DMA_CH2_GIF	DMA_CH1_ERRF	DMA_CH1_THF	DMA_CH1_TCF	DMA_CH1_GIF	DMA_CH0_ERRF	DMA_CH0_THF	DMA_CH0_TCF	DMA_CH0_GIF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	DMA_INT	Reserved																Reserved								Reserved							DMA_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	DMA_CR0	Reserved								Reserved			DMA_CH4_ENB	DMA_CH3_ENB	DMA_CH2_ENB	DMA_CH1_ENB	DMA_CH0_ENB	Reserved								Reserved	DMA_GPL_CHS [2:0]			Reserved	DMA_FGBUS_SEL	DMA_PRI_MDS	DMA_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	DMA_CH0A	Reserved				DMA_CH0_ERR2F	DMA_CH0_TH2F	DMA_CH0_TC2F	Reserved	Reserved				DMA_CH0_EIE	DMA_CH0_HIE	DMA_CH0_CIE	Reserved	DMA_CH0_REQ	Reserved	DMA_CH0_BSIZE [1:0]		DMA_CH0_PLS [1:0]		DMA_CH0_XMDS [1:0]		Reserved	DMA_CH0_LAST	Reserved		DMA_CH0_ADSEL	DMA_CH0_LOOP	DMA_CH0_HOLD	DMA_CH0_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	DMA_CH0B	Reserved							DMA_CH0_XPIN	Reserved		Reserved		DMA_CH0_DSYNC	DMA_CH0_SSYNC	DMA_CH0_DINC	DMA_CH0_SINC	Reserved				DMA_CH0_DET [3:0]				Reserved				DMA_CH0_SRC [3:0]			
Reset	**0x00030000**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	DMA_CH0NUM	Reserved								Reserved							DMA_CH0_NUM [16:0]																
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	DMA_CH0CNT	Reserved								Reserved							DMA_CH0_CNT [16:0]																
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	DMA_CH0SSA	DMA_CH0_SSA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x34	DMA_CH0SCA	DMA_CH0_SCA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	DMA_CH0DSA	DMA_CH0_DSA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	DMA_CH0DCA	DMA_CH0_DCA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	DMA_CH1A	Reserved				DMA_CH1_ERR2F	DMA_CH1_TH2F	DMA_CH1_TC2F	Reserved	Reserved				DMA_CH1_EIE	DMA_CH1_HIE	DMA_CH1_CIE	Reserved	DMA_CH1_REQ	Reserved	DMA_CH1_BSIZE [1:0]		DMA_CH1_PLS [1:0]		DMA_CH1_XMDS [1:0]		Reserved	DMA_CH1_LAST	Reserved		DMA_CH1_ADSEL	DMA_CH1_LOOP	DMA_CH1_HOLD	DMA_CH1_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x44	DMA_CH1B	Reserved							DMA_CH1_XPIN	Reserved		Reserved		DMA_CH1_DSYNC	DMA_CH1_SSYNC	DMA_CH1_DINC	DMA_CH1_SINC	Reserved				DMA_CH1_DET [3:0]				Reserved				DMA_CH1_SRC [3:0]			
Reset	0x00030000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x48	DMA_CH1NUM	Reserved																DMA_CH1_NUM [15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x4C	DMA_CH1CNT	Reserved																DMA_CH1_CNT [15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	DMA_CH1SSA	DMA_CH1_SSA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x54	DMA_CH1SCA	DMA_CH1_SCA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x58	DMA_CH1DSA	DMA_CH1_DSA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x5C	DMA_CH1DCA	DMA_CH1_DCA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x60	DMA_CH2A	Reserved				DMA_CH2_ERR2F	DMA_CH2_TH2F	DMA_CH2_TC2F	Reserved	Reserved				DMA_CH2_EIE	DMA_CH2_HIE	DMA_CH2_CIE	Reserved	DMA_CH2_REQ	Reserved	DMA_CH2_BSIZE [1:0]		DMA_CH2_PLS [1:0]		DMA_CH2_XMDS [1:0]		Reserved	DMA_CH2_LAST	Reserved		DMA_CH2_ADSEL	DMA_CH2_LOOP	DMA_CH2_HOLD	DMA_CH2_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x64	DMA_CH2B	Reserved							DMA_CH2_XPIN	Reserved		Reserved		DMA_CH2_DSYNC	DMA_CH2_SSYNC	DMA_CH2_DINC	DMA_CH2_SINC	Reserved				DMA_CH2_DET [3:0]				Reserved				DMA_CH2_SRC [3:0]			
Reset	0x00030000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x68	DMA_CH2NUM	Reserved																DMA_CH2_NUM [15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x6C	DMA_CH2CNT	Reserved																DMA_CH2_CNT [15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x70	DMA_CH2SSA	DMA_CH2_SSA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x74	DMA_CH2SCA	DMA_CH2_SCA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x78	DMA_CH2DSA	DMA_CH2_DSA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x7C	DMA_CH2DCA	DMA_CH2_DCA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x80	DMA_CH3A	Reserved				DMA_CH3_ERR2F	DMA_CH3_TH2F	DMA_CH3_TC2F	Reserved	Reserved				DMA_CH3_EIE	DMA_CH3_HIE	DMA_CH3_CIE	Reserved	DMA_CH3_REQ	Reserved	DMA_CH3_BSIZE [1:0]		DMA_CH3_PLS [1:0]		DMA_CH3_XMDS [1:0]		Reserved	DMA_CH3_LAST	Reserved		DMA_CH3_ADSEL	DMA_CH3_LOOP	DMA_CH3_HOLD	DMA_CH3_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x84	DMA_CH3B	Reserved							DMA_CH3_XPIN	Reserved		Reserved		DMA_CH3_DSYNC	DMA_CH3_SSYNC	DMA_CH3_DINC	DMA_CH3_SINC	Reserved				DMA_CH3_DET [3:0]				Reserved				DMA_CH3_SRC [3:0]			
Reset	0x00030000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x88	DMA_CH3NUM	Reserved								Reserved							DMA_CH3_NUM [16:0]																
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x8C	DMA_CH3CNT	Reserved								Reserved							DMA_CH3_CNT [16:0]																
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x90	DMA_CH3SSA	DMA_CH3_SSA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x94	DMA_CH3SCA	DMA_CH3_SCA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x98	DMA_CH3DSA	DMA_CH3_DSA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x9C	DMA_CH3DCA	DMA_CH3_DCA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0xA0	DMA_CH4A	Reserved				DMA_CH4_ERR2F	DMA_CH4_TH2F	DMA_CH4_TC2F	Reserved	Reserved				DMA_CH4_EIE	DMA_CH4_HIE	DMA_CH4_CIE	Reserved	DMA_CH4_REQ	Reserved	DMA_CH4_BSIZE [1:0]		DMA_CH4_PLS [1:0]		DMA_CH4_XMDS [1:0]		Reserved	DMA_CH4_LAST	Reserved		DMA_CH4_ADSEL	DMA_CH4_LOOP	DMA_CH4_HOLD	DMA_CH4_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xA4	DMA_CH4B	Reserved							DMA_CH4_XPIN	Reserved		Reserved		DMA_CH4_DSYNC	DMA_CH4_SSYNC	DMA_CH4_DINC	DMA_CH4_SINC	Reserved				DMA_CH4_DET [3:0]				Reserved				DMA_CH4_SRC [3:0]			
Reset	**0x00030000**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xA8	DMA_CH4NUM	Reserved																DMA_CH4_NUM [15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xAC	DMA_CH4CNT	Reserved																DMA_CH4_CNT [15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xB0	DMA_CH4SSA	DMA_CH4_SSA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xB4	DMA_CH4SCA	DMA_CH4_SCA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xB8	DMA_CH4DSA	DMA_CH4_DSA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xBC	DMA_CH4DCA	DMA_CH4_DCA [31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.9. Reset Control Registers

Reset Control	(RST) Reset Source Controller
Base Address :	0x4C000000

1.9.1. RST Reset status register

RST_STA	RST Reset status register		
Offset Address :	0x00	Reset Value :	0xC0000001

31	30	29	28	27	26	25	24
RST_CRF	RST_WRF	Reserved					
23	22	21	20	19	18	17	16
Reserved				Reserved	Reserved	RST_CMP1F	RST_CMP0F
15	14	13	12	11	10	9	8
Reserved		RST_ADCF	RST_WWDTF	RST_IWDTF	RST_MEMF	Reserved	RST_CSCF
7	6	5	4	3	2	1	0
RST_BOD2F	RST_LPMF	RST_BOD1F	RST_BOD0F	RST_CPUF	RST_EXF	RST_SWF	RST_PORF

Bit	Attr	Bit Name	Description	Reset
31	rw	RST_CRF	Cold reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x01
30	rw	RST_WRF	Warm reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x01
29..24	-	Reserved	Reserved	0x00
23..20	-	Reserved	Reserved	0x00
19	-	Reserved	Reserved	0x00
18	-	Reserved	Reserved	0x00
17	rw	RST_CMP1F	Comparator CMP1 threshold comparison reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
16	rw	RST_CMP0F	Comparator CMP0 threshold comparison reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
15..14	-	Reserved	Reserved	0x00
13	rw	RST_ADCF	ADC analog voltage watch-dog reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
12	rw	RST_WWDTF	WWDT reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
11	rw	RST_IWDTF	IWDT reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
10	rw	RST_MEMF	Flash memory read/write protect or illegal address error reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00

9	-	Reserved	Reserved	0x00
8	rw	RST_CSCF	CSC missing clock detect reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
7	rw	RST_BOD2F	BOD2 reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
6	rw	RST_LPMF	Low power mode reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
5	rw	RST_BOD1F	BOD1 reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
4	rw	RST_BOD0F	BOD0 reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
3	rw	RST_CPUF	CPU SYSRESETREQ bit system reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
2	rw	RST_EXF	External input reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
1	rw	RST_SWF	Software forced reset flag. Software write 1 to clear and is no effect by writing 0. (This bit only reset by POR reset) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
0	rw	RST_PORF	Power-on reset flag. Software write 1 to clear and is no effect by writing 0. This bit reset by POR reset and set after POR reset. 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x01

1.9.2. RST write protected Key register

RST_KEY	RST write protected Key register		
Offset Address :	0x0C	Reset Value :	0x00000001

31	30	29	28	27	26	25	24
RST_LOCK[15:8]							
23	22	21	20	19	18	17	16
RST_LOCK[7:0]							
15	14	13	12	11	10	9	8
RST_KEY[15:8]							
7	6	5	4	3	2	1	0
RST_KEY[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	rw	RST_LOCK	Reset lock register. Write value 0x712A to lock the register write access except RST_STA, RST_KEY registers. When locks, the registers cannot change until Cold reset. Write other value except 0x712A is no effect. For read access : 0 = Unlocked	0x0000

			1 = Locked	
15..0	rw	RST_KEY	Reset key register. Write value 0xA217 to unprotect the register write access. Write other value except 0xA217 to protect the registers except RST_STA , RST_KEY registers. For read access : 0 = Unprotected 1 = Protected	0x0001

1.9.3. RST control register 0

RST_CR0	RST control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved						RST_USB_RCTL	RST_WWDT_WDIS
23	22	21	20	19	18	17	16
Reserved						RST_PE_DIS1	RST_PE_DIS0
15	14	13	12	11	10	9	8
RST_PD_DIS1	RST_PD_DIS0	RST_PC_DIS1	RST_PC_DIS0	RST_PB_DIS1	RST_PB_DIS0	RST_PA_DIS1	RST_PA_DIS0
7	6	5	4	3	2	1	0
Reserved		Reserved	Reserved	Reserved	Reserved	RST_SW_EN	Reserved

Bit	Attr	Bit Name	Description	Reset
31..26	-	Reserved	Reserved	0x00
25	rw	RST_USB_RCTL	USB module software reset control. When selects 'All', chip will auto reset USB all blocks and registers. When selects 'LV1', chip will reset all blocks and and registers except USB_EN, USB_XTR_EN, USB_V33_EN (V33 LDO) and USB_DPU_EN (DP 1.5k pull-up) control. 0 = All : USB Reset Level-0 1 = LV1 : USB Reset Level-1	0x00
24	rw	RST_WWDT_WDIS	WWDT module Warm reset disable bit. When disables, the WWDT module cannot reset by Warm reset and only reset by Cold reset. 0 = Enable 1 = Disable	0x00
23..18	-	Reserved	Reserved	0x00
17	rw	RST_PE_DIS1	Warm reset disable for PE[9:8] pins. It is including of IO mode setting and port latch value. (The register is reset to default value only after Cold reset.) 0 = Enable 1 = Disable	0x00
16	rw	RST_PE_DIS0	Warm reset disable for PE[3:0] pins. It is including of IO mode setting and port latch value. (The register is reset to default value only after Cold reset.) 0 = Enable 1 = Disable	0x00
15	rw	RST_PD_DIS1	Warm reset disable for PD[11:8] pins. It is including of IO mode setting and port latch value. (The register is reset to default value only after Cold reset.) 0 = Enable 1 = Disable	0x00
14	rw	RST_PD_DIS0	Warm reset disable for PD[3:0] pins. It is including of IO mode setting and port latch value. (The register is reset to default value only after Cold reset.) 0 = Enable 1 = Disable	0x00
13	rw	RST_PC_DIS1	Warm reset disable for PC[11:8] pins. It is including of IO mode setting and port latch value. (The register is reset to default value only after Cold reset.)	0x00

			0 = Enable 1 = Disable	
12	rw	RST_PC_DIS0	Warm reset disable for PC[3:0] pins. It is including of IO mode setting and port latch value. (The register is reset to default value only after Cold reset.) 0 = Enable 1 = Disable	0x00
11	rw	RST_PB_DIS1	Warm reset disable for PB[11:8] pins. It is including of IO mode setting and port latch value. (The register is reset to default value only after Cold reset.) 0 = Enable 1 = Disable	0x00
10	rw	RST_PB_DIS0	Warm reset disable for PB[3:0] pins. It is including of IO mode setting and port latch value. (The register is reset to default value only after Cold reset.) 0 = Enable 1 = Disable	0x00
9	rw	RST_PA_DIS1	Warm reset disable for PA[11:8] pins. It is including of IO mode setting and port latch value. (The register is reset to default value only after Cold reset.) 0 = Enable 1 = Disable	0x00
8	rw	RST_PA_DIS0	Warm reset disable for PA[3:0] pins. It is including of IO mode setting and port latch value. (The register is reset to default value only after Cold reset.) 0 = Enable 1 = Disable	0x00
7..6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	rw	RST_SW_EN	System software forced reset enable for whole chip reset 0 = No operation 1 = Generate reset	0x00
0	-	Reserved	Reserved	0x00

1.9.4. RST Cold reset enable register

RST_CE	RST Cold reset enable register		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved				Reserved	Reserved	RST_CMP1_CE	RST_CMP0_CE
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved		RST_ADC_CE	RST_WWDT_CE	RST_IWDT_CE	RST_MEM_CE	Reserved	RST_CSC_CE
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RST_BOD2_CE	RST_LPM_CE	RST_BOD1_CE	RST_BOD0_CE	RST_CPU_CE	RST_EX_CE	RST_SW_CE	Reserved

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..20	-	Reserved	Reserved	0x00
19	-	Reserved	Reserved	0x00
18	-	Reserved	Reserved	0x00
17	rw	RST_CMP1_CE	Comparator CMP1 threshold comparison Cold reset enable. (This bit only reset by POR reset) 0 = Disable 1 = Enable	0x00

16	rw	RST_CMP0_CE	Comparator CMP0 threshold comparison Cold reset enable. (This bit only reset by POR reset) 0 = Disable 1 = Enable	0x00
15..14	-	Reserved	Reserved	0x00
13	rw	RST_ADC_CE	ADC analog voltage watch-dog Cold reset enable. (This bit only reset by POR reset) 0 = Disable 1 = Enable	0x00
12	rw	RST_WWDT_CE	WWDT Cold reset enable. (This bit only reset by POR reset) 0 = Disable 1 = Enable	0x00
11	rw	RST_IWDT_CE	IWDT Cold reset enable. (This bit only reset by POR reset) 0 = Disable 1 = Enable	0x00
10	rw	RST_MEM_CE	Flash memory read/write protect or illegal address error Cold reset enable. (This bit only reset by POR reset) 0 = Disable 1 = Enable	0x00
9	-	Reserved	Reserved	0x00
8	rw	RST_CSC_CE	CSC missing clock detect Cold reset enable. (This bit only reset by POR reset) 0 = Disable 1 = Enable	0x00
7	rw	RST_BOD2_CE	BOD2 Cold reset enable. 0 = Disable 1 = Enable	0x00
6	rw	RST_LPM_CE	Low power STOP mode Cold reset enable. (This bit only reset by POR reset) 0 = Disable 1 = Enable	0x00
5	rw	RST_BOD1_CE	BOD1 Cold reset enable. 0 = Disable 1 = Enable	0x00
4	rw	RST_BOD0_CE	BOD0 Cold reset enable. 0 = Disable 1 = Enable	0x00
3	rw	RST_CPU_CE	CPU SYSRESETREQ bit forced Cold reset enable. (This bit only reset by POR reset) 0 = Disable 1 = Enable	0x00
2	rw	RST_EX_CE	External input Cold reset enable. (This bit only reset by POR reset) 0 = Disable 1 = Enable	0x00
1	rw	RST_SW_CE	Software forced Cold reset enable. (This bit only reset by POR reset) 0 = Disable 1 = Enable	0x00
0	-	Reserved	Reserved	0x00

1.9.5. RST Warm reset enable register

RST_WE	RST Warm reset enable register		
Offset Address :	0x18	Reset Value :	0x0000000E

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved				Reserved	Reserved	RST_CMP1_WE	RST_CMP0_WE

15	14	13	12	11	10	9	8
Reserved		RST_ADC_WE	RST_WWDT_WE	RST_IWDT_WE	RST_MEM_WE	Reserved	RST_CSC_WE
7	6	5	4	3	2	1	0
RST_BOD2_WE	RST_LPM_WE	RST_BOD1_WE	RST_BOD0_WE	RST_CPU_WE	RST_EX_WE	RST_SW_WE	Reserved

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..20	-	Reserved	Reserved	0x00
19	-	Reserved	Reserved	0x00
18	-	Reserved	Reserved	0x00
17	rw	RST_CMP1_WE	Comparator CMP1 threshold comparison Warm reset enable. 0 = Disable 1 = Enable	0x00
16	rw	RST_CMP0_WE	Comparator CMP0 threshold comparison Warm reset enable. 0 = Disable 1 = Enable	0x00
15..14	-	Reserved	Reserved	0x00
13	rw	RST_ADC_WE	ADC analog voltage watch-dog Warm reset enable. 0 = Disable 1 = Enable	0x00
12	rw	RST_WWDT_WE	WWDT Warm reset enable. 0 = Disable 1 = Enable	0x00
11	rw	RST_IWDT_WE	IWDT Warm reset enable. (The register is reset and loaded from CFG OR only after Cold reset.) 0 = Disable 1 = Enable	0x00
10	rw	RST_MEM_WE	Flash memory read/write protect or illegal address error Warm reset enable. 0 = Disable 1 = Enable	0x00
9	-	Reserved	Reserved	0x00
8	rw	RST_CSC_WE	CSC missing clock detect Warm reset enable. 0 = Disable 1 = Enable	0x00
7	rw	RST_BOD2_WE	BOD2 Warm reset enable. (The register is reset and loaded from CFG OR only after Cold reset.) 0 = Disable 1 = Enable	0x00
6	rw	RST_LPM_WE	Low power STOP mode Warm reset enable. 0 = Disable 1 = Enable	0x00
5	rw	RST_BOD1_WE	BOD1 Warm reset enable. (The register is reset and loaded from CFG OR only after Cold reset.) 0 = Disable 1 = Enable	0x00
4	rw	RST_BOD0_WE	BOD0 Warm reset enable. (The register is reset and loaded from CFG OR only after Cold reset.) 0 = Disable 1 = Enable	0x00
3	rw	RST_CPU_WE	CPU SYSRESETREQ bit forced Warm reset enable. 0 = Disable 1 = Enable	0x01
2	rw	RST_EX_WE	External input Warm reset enable. (The register is set to enable after Cold reset. if OR CFG_EXRST_PIN is enabled.) 0 = Disable 1 = Enable	0x01
1	rw	RST_SW_WE	Software forced Warm reset enable. 0 = Disable 1 = Enable	0x01

0	-	Reserved	Reserved	0x00

1.9.6. RST AHB reset register

RST_AHB	RST AHB reset register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved	Reserved	Reserved	RST_EMB_EN	Reserved			RST_GPL_EN
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			RST_IOPE_EN	RST_IOPD_EN	RST_IOPC_EN	RST_IOPB_EN	RST_IOPA_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	-	Reserved	Reserved	0x00
14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	rw	RST_EMB_EN	System software forced reset enable for EMB module. 0 = No-Reset 1 = Reset	0x00
11..9	-	Reserved	Reserved	0x00
8	rw	RST_GPL_EN	System software forced reset enable for GPL module. 0 = No-Reset 1 = Reset	0x00
7..5	-	Reserved	Reserved for IOPF~IOPH	0x00
4	rw	RST_IOPE_EN	System software forced reset enable for IO Port-E. 0 = No-Reset 1 = Reset	0x00
3	rw	RST_IOPD_EN	System software forced reset enable for IO Port-D. 0 = No-Reset 1 = Reset	0x00
2	rw	RST_IOPC_EN	System software forced reset enable for IO Port-C. 0 = No-Reset 1 = Reset	0x00
1	rw	RST_IOPB_EN	System software forced reset enable for IO Port-B. 0 = No-Reset 1 = Reset	0x00
0	rw	RST_IOPA_EN	System software forced reset enable for IO Port-A. 0 = No-Reset 1 = Reset	0x00

1.9.7. RST APB reset register 0

RST_APB0	RST APB reset register 0		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved		RST_APX_EN	RST_USB_EN	Reserved			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RST_URT7_EN	RST_URT6_EN	RST_URT5_EN	RST_URT4_EN	Reserved	RST_URT2_EN	RST_URT1_EN	RST_URT0_EN
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved		Reserved	RST_SPI0_EN	Reserved		RST_I2C1_EN	RST_I2C0_EN
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RST_WWDT_EN	RST_IWDT_EN	RST_RTC_EN	Reserved	RST_DAC_EN	RST_CMP_EN	Reserved	RST_ADC0_EN

Bit	Attr	Bit Name	Description	Reset
31..30	-	Reserved	Reserved	0x00
29	rw	RST_APX_EN	System software forced reset enable for APB module. 0 = No-Reset 1 = Reset	0x00
28	rw	RST_USB_EN	System software forced reset enable for USB module. 0 = No-Reset 1 = Reset	0x00
27..24	-	Reserved	Reserved	0x00
23	rw	RST_URT7_EN	System software forced reset enable for URT7 module. 0 = No-Reset 1 = Reset	0x00
22	rw	RST_URT6_EN	System software forced reset enable for URT6 module. 0 = No-Reset 1 = Reset	0x00
21	rw	RST_URT5_EN	System software forced reset enable for URT5 module. 0 = No-Reset 1 = Reset	0x00
20	rw	RST_URT4_EN	System software forced reset enable for URT4 module. 0 = No-Reset 1 = Reset	0x00
19	-	Reserved	Reserved	0x00
18	rw	RST_URT2_EN	System software forced reset enable for URT2 module. 0 = No-Reset 1 = Reset	0x00
17	rw	RST_URT1_EN	System software forced reset enable for URT1 module. 0 = No-Reset 1 = Reset	0x00
16	rw	RST_URT0_EN	System software forced reset enable for URT0 module. 0 = No-Reset 1 = Reset	0x00
15..14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	rw	RST_SPI0_EN	System software forced reset enable for SP00 module. 0 = No-Reset 1 = Reset	0x00
11..10	-	Reserved	Reserved	0x00
9	rw	RST_I2C1_EN	System software forced reset enable for I2C1 module. 0 = No-Reset 1 = Reset	0x00
8	rw	RST_I2C0_EN	System software forced reset enable for I2C0 module. 0 = No-Reset 1 = Reset	0x00
7	rw	RST_WWDT_EN	System software forced reset enable for WWDT module. 0 = No-Reset 1 = Reset	0x00
6	rw	RST_IWDT_EN	System software forced reset enable for IWDT module. 0 = No-Reset 1 = Reset	0x00
5	rw	RST_RTC_EN	System software forced reset enable for RTC module. 0 = No-Reset 1 = Reset	0x00
4	-	Reserved	Reserved	0x00
3	rw	RST_DAC_EN	System software forced reset enable for DAC module. 0 = No operation 1 = Generate reset	0x00
2	rw	RST_CMP_EN	System software forced reset enable for CMP module. 0 = No-Reset 1 = Reset	0x00
1	-	Reserved	Reserved	0x00

0	rw	RST_ADC0_EN	System software forced reset enable for ADC0 module. 0 = No operation 1 = Generate reset	0x00

1.9.8. RST APB reset register 1

RST_APB1	RST APB reset register 1		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
RST_TM36_EN	Reserved		Reserved	RST_TM26_EN	Reserved	Reserved	RST_TM20_EN
7	6	5	4	3	2	1	0
RST_TM16_EN	Reserved	Reserved	RST_TM10_EN	Reserved		RST_TM01_EN	RST_TM00_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	RST_TM36_EN	System software forced reset enable for TM36 module. 0 = No-Reset 1 = Reset	0x00
14..13	-	Reserved	Reserved	0x00
12	-	Reserved	Reserved	0x00
11	rw	RST_TM26_EN	System software forced reset enable for TM26 module. 0 = No-Reset 1 = Reset	0x00
10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	rw	RST_TM20_EN	System software forced reset enable for TM20 module. 0 = No-Reset 1 = Reset	0x00
7	rw	RST_TM16_EN	System software forced reset enable for TM16 module. 0 = No-Reset 1 = Reset	0x00
6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	rw	RST_TM10_EN	System software forced reset enable for TM10 module. 0 = No-Reset 1 = Reset	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	RST_TM01_EN	System software forced reset enable for TM01 module. 0 = No-Reset 1 = Reset	0x00
0	rw	RST_TM00_EN	System software forced reset enable for TM00 module. 0 = No-Reset 1 = Reset	0x00

1.9.9. RST Register Map

RST Register Map Register Number = 8

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	RST_STA	RST_CRF	RST_WRF	Reserved						Reserved				Reserved	Reserved	RST_CMP1F	RST_CMP0F	Reserved		RST_ADCF	RST_WWDTF	RST_IWDTF	RST_MEMF	Reserved	RST_CSCF	RST_BOD2F	RST_LPMF	RST_BOD1F	RST_BOD0F	RST_CPUF	RST_EXF	RST_SWF	RST_PORF
Reset	0xC0000001	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x0C	RST_KEY	RST_LOCK[15:0]																RST_KEY[15:0]															
Reset	0x00000001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x10	RST_CR0	Reserved						RST_USB_RCTL	RST_WWDT_WDIS	Reserved						RST_PE_DIS1	RST_PE_DIS0	RST_PD_DIS1	RST_PD_DIS0	RST_PC_DIS1	RST_PC_DIS0	RST_PB_DIS1	RST_PB_DIS0	RST_PA_DIS1	RST_PA_DIS0	Reserved		Reserved	Reserved	Reserved	Reserved	RST_SW_EN	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	RST_CE	Reserved								Reserved				Reserved	Reserved	RST_CMP1_CE	RST_CMP0_CE	Reserved		RST_ADC_CE	RST_WWDT_CE	RST_IWDT_CE	RST_MEM_CE	Reserved	RST_CSC_CE	RST_BOD2_CE	RST_LPM_CE	RST_BOD1_CE	RST_BOD0_CE	RST_CPU_CE	RST_EX_CE	RST_SW_CE	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	RST_WE	Reserved								Reserved				Reserved	Reserved	RST_CMP1_WE	RST_CMP0_WE	Reserved		RST_ADC_WE	RST_WWDT_WE	RST_IWDT_WE	RST_MEM_WE	Reserved	RST_CSC_WE	RST_BOD2_WE	RST_LPM_WE	RST_BOD1_WE	RST_BOD0_WE	RST_CPU_WE	RST_EX_WE	RST_SW_WE	Reserved
Reset	0x0000000E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
0x1C	RST_AHB	Reserved																Reserved	Reserved	Reserved	RST_EMB_EN	Reserved			RST_GPL_EN	Reserved			RST_IOPE_EN	RST_IOPD_EN	RST_IOPC_EN	RST_IOPB_EN	RST_IOPA_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	RST_APB0	Reserved		RST_APX_EN	RST_USB_EN	Reserved				RST_URT7_EN	RST_URT6_EN	RST_URT5_EN	RST_URT4_EN	Reserved	RST_URT2_EN	RST_URT1_EN	RST_URT0_EN	Reserved		Reserved	RST_SPI0_EN	Reserved		RST_I2C1_EN	RST_I2C0_EN	RST_WWDT_EN	RST_IWDT_EN	RST_RTC_EN	Reserved	RST_DAC_EN	RST_CMP_EN	Reserved	RST_ADC0_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	RST_APB1	Reserved																RST_TM36_EN	Reserved		Reserved	RST_TM26_EN	Reserved	Reserved	RST_TM20_EN	RST_TM16_EN	Reserved	Reserved	RST_TM10_EN	Reserved		RST_TM01_EN	RST_TM00_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.10. Clock Control Registers

Clock Control	(CSC) Clock Source Controller
Base Address :	0x4C010000

1.10.1. CSC status register

CSC_STA	CSC status register		
Offset Address :	0x00	Reset Value :	0x00020000

31	30	29	28	27	26	25	24
CSC_PLL_STA	CSC_IHRCO_STA	CSC_ILRCO_STA	CSC_XOSC_STA	Reserved	CSC_MAIN_STA[2:0]		
23	22	21	20	19	18	17	16
CSC_HS_STA[3:0]				CSC_LS_STA[3:0]			
15	14	13	12	11	10	9	8
Reserved		CSC_PLLI_STA[1:0]		CSC_HS2_STA[3:0]			
7	6	5	4	3	2	1	0
CSC_MCDF	CSC_PLLF	CSC_IHRCOF	CSC_ILRCOF	Reserved		CSC_XOSCF	Reserved

Bit	Attr	Bit Name	Description	Reset
31	r	CSC_PLL_STA	PLL clock stable and ready status after PLL enabled. 0 = Unready 1 = Ready	0x00
30	r	CSC_IHRCO_STA	IHRCO clock stable and ready status after IHRCO enabled. 0 = Unready 1 = Ready	0x00
29	r	CSC_ILRCO_STA	ILRCO clock stable and ready status after ILRCO enabled. 0 = Unready 1 = Ready	0x00
28	r	CSC_XOSC_STA	XOSC clock stable and ready status after XOSC enabled. 0 = Unready 1 = Ready	0x00
27	-	Reserved	Reserved	0x00
26..24	r	CSC_MAIN_STA	System main clock source select MUX switching status. If the readback value is not following list, it indicates the clock source select MUX is switching and clock is not yet stable. 0x0 = Switching : MUX is switching and clock is not yet stable 0x1 = CK_HS : MUX has switched and clock is ready 0x2 = CK_PLLI : MUX has switched and clock is ready 0x4 = CK_PLLO : MUX has switched and clock is ready	0x00
23..20	r	CSC_HS_STA	Input high speed clock source select MUX switching status. If the readback value is not following list, it indicates the clock source select MUX is switching and clock is not yet stable. 0x0 = Switching : MUX is switching and clock is not yet stable 0x1 = IHRCO 0x2 = XOSC 0x4 = ILRCO 0x8 = CK_EXT	0x00
19..16	r	CSC_LS_STA	Input low speed clock source select MUX switching status. If the readback value is not following list, it indicates the clock source select MUX is switching and clock is not yet stable. 0x0 = Switching : MUX is switching and clock is not yet stable 0x2 = XOSC 0x4 = ILRCO 0x8 = CK_EXT	0x02
15..14	-	Reserved	Reserved	0x00
13..12	r	CSC_PLLI_STA	PLL input clock source select MUX switching status. If the readback value is not following list, it indicates the clock source select MUX is switching and clock is not yet stable. 0x0 = Switching : MUX is switching and clock is not yet stable 0x1 = CK_HS	0x00

			0x2 = CK_HS2	
11..8	r	CSC_HS2_STA	Input high speed clock source-2 select MUX switching status. If the readback value is not following list, it indicates the clock source select MUX is switching and clock is not yet stable. 0x0 = Switching : MUX is switching and clock is not yet stable 0x1 = IHRCO 0x2 = XOSC 0x4 = Reserved 0x8 = CK_EXT	0x00
7	rw	CSC_MCDF	XOSC missing clock detect failure event flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	rw	CSC_PLLF	PLL clock stable and ready detect flag. This flag will be asserted after PLL is enabled. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	rw	CSC_IHRCOF	IHRCO clock stable and ready detect flag. This flag will be asserted after IHRCO is enabled. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	CSC_ILRCOF	ILRCO clock stable and ready detect flag. This flag will be asserted after ILRCO is enabled. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	CSC_XOSCF	XOSC clock stable and ready detect flag. This flag will be asserted after XOSC is enabled. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	-	Reserved	Reserved	0x00

1.10.2. CSC interrupt enable register

CSC_INT	CSC interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
CSC_MCD_IE	CSC_PLL_IE	CSC_IHRCO_IE	CSC_ILRCO_IE	Reserved		CSC_XOSC_IE	CSC_IEA

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	rw	CSC_MCD_IE	XOSC missing clock detect failure event interrupt enable. 0 = Disable 1 = Enable	0x00
6	rw	CSC_PLL_IE	PLL clock stable interrupt enable. 0 = Disable 1 = Enable	0x00
5	rw	CSC_IHRCO_IE	IHRCO clock stable interrupt enable.	0x00

			0 = Disable 1 = Enable	
4	rw	CSC_ILRCO_IE	ILRCO clock stable interrupt enable. 0 = Disable 1 = Enable	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	CSC_XOSC_IE	XOSC clock stable interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	CSC_IEA	CSC interrupt all enable. When disables, the CSC global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.10.3. CSC OSC and PLL control register

CSC_PLL	CSC OSC and PLL control register		
Offset Address :	0x08	Reset Value :	0x00000004

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						CSC_XOSC_GN[1:0]	
15	14	13	12	11	10	9	8
Reserved	CSC_PLL_MULX[5:0]						CSC_PLL_MUL
7	6	5	4	3	2	1	0
Reserved	Reserved				Reserved	CSC_PLLI_SEL	CSC_PLL_MDS

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..18	-	Reserved	Reserved	0x00
17..16	rw	CSC_XOSC_GN	Gain control bits of XOSC. (The default value is loaded from CFG OR after Warm reset) 0x0 = 32K_Normal (for 32KHz crystal) 0x1 = Medium 0x2 = 32K_Lowest (for 32KHz crystal) 0x3 = Reserved	0x00
15	-	Reserved	Reserved	0x00
14..9	rw	CSC_PLL_MULX	CSC PLL multiplication value. These bits are no effect when CSC_PLL_MDS=0. The PLL multiplication value (MUL) is this register value +1 and the PLL output is input clock x MUL. The valid register value range is 3~31 (PLL multiplication value 4~32).	0x00
8	rw	CSC_PLL_MUL	CSC PLL multiplication factor select. These bits are no effect when CSC_PLL_MDS=1. 0 = 16 : PLL input clock x 16 1 = 24 : PLL input clock x 24	0x00
7	-	Reserved	Reserved	0x00
6..3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x01
1	rw	CSC_PLLI_SEL	CSC PLL input clock source select. 0 = CK_HS 1 = CK_HS2	0x00
0	rw	CSC_PLL_MDS	CSC PLL multiplication mode select. 0 = MUL : Use CSC_PLL_MUL as PLL multiplication value 1 = MULX : Use CSC_PLL_MULX as PLL multiplication value	0x00

1.10.4. CSC write protected Key register

CSC_KEY	CSC write protected Key register		
Offset Address :	0x0C	Reset Value :	0x00000001

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
CSC_KEY[15:8]							
7	6	5	4	3	2	1	0
CSC_KEY[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	CSC_KEY	CSC key register. Write value 0xA217 to unprotect the register write access. Write other value except 0xA217 to protect the registers except CSC_STA, CSC_KEY registers. For read access : 0 = Unprotected 1 = Protected	0x0001

1.10.5. CSC clock source control register 0

CSC_CR0	CSC clock source control register 0		
Offset Address :	0x10	Reset Value :	0x00000200

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
CSC_MCD_SEL[1:0]		Reserved			CSC_IHRCO_SEL	Reserved	CSC_ST_SEL
15	14	13	12	11	10	9	8
CSC_MAIN_SEL[1:0]		CSC_HS2_SEL[1:0]		CSC_HS_SEL[1:0]		CSC_LS_SEL[1:0]	
7	6	5	4	3	2	1	0
Reserved		CSC_PLL_EN	CSC_MCD_DIS	CSC_IHRCO_EN	Reserved		

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..22	rw	CSC_MCD_SEL	Missing clock detection duration select. 0x0 = 125us 0x1 = 250us 0x2 = 500us 0x3 = 1ms	0x00
21..19	-	Reserved	Reserved	0x00
18	rw	CSC_IHRCO_SEL	IHRCO clock frequency trimming set select. 0 = 12 : 12MHz from trimming set 0 1 = 11 : 11.059MHz from trimming set 1	0x00
17	-	Reserved	Reserved	0x00
16	rw	CSC_ST_SEL	System tick timer external clock source select. 0 = HCLK8 : HCLK divided by 8 1 = CK_LS2 : CK_LS divided by 2	0x00
15..14	rw	CSC_MAIN_SEL	System main clock source select. 0x0 = CK_HS 0x1 = CK_PLLI 0x2 = CK_PLLO 0x3 = Reserved	0x00
13..12	rw	CSC_HS2_SEL	Input high speed clock-2 source select. 0x0 = IHRCO 0x1 = XOSC 0x2 = Reserved 0x3 = CK_EXT	0x00

11..10	rw	CSC_HS_SEL	Input high speed clock source select. (The default setting is IHRCO or ILRCO which value is loaded from CFG OR after Warm reset) 0x0 = IHRCO 0x1 = XOSC 0x2 = ILRCO 0x3 = CK_EXT	0x00
9..8	rw	CSC_LS_SEL	Input low speed clock source select 0x0 = Reserved 0x1 = XOSC 0x2 = ILRCO 0x3 = CK_EXT	0x02
7..6	-	Reserved	Reserved	0x00
5	rw	CSC_PLL_EN	PLL circuit enable. 0 = Disable 1 = Enable	0x00
4	rw	CSC_MCD_DIS	MCD missing clock detector circuit disable. 0 = Enable 1 = Disable	0x00
3	rw	CSC_IHRCO_EN	IHRCO circuit enable. (The register is reset and loaded from CFG OR only after Warm reset.) 0 = Disable 1 = Enable	0x00
2..0	-	Reserved	Reserved	0x00

1.10.6. CSC clock divider register

CSC_DIV	CSC clock divider register		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				CSC_UT_DIV[1:0]		Reserved	Reserved
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved		CSC_USB_DIV[1:0]		Reserved	CSC_APB_DIV[2:0]		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved				CSC_AHB_DIV[3:0]			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		CSC_PLLO_DIV[1:0]		Reserved		CSC_PLLI_DIV[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27..26	rw	CSC_UT_DIV	Unit time clock source divider. 0x0 = DIV32 : divided by 32 0x1 = DIV8 : divided by 8 0x2 = DIV16 : divided by 16 0x3 = DIV128 : divided by 128	0x00
25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23..22	-	Reserved	Reserved	0x00
21..20	rw	CSC_USB_DIV	USB SIE clock input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV3 : divided by 3 0x3 = DIV4 : divided by 4	0x00
19	-	Reserved	Reserved	0x00
18..16	rw	CSC_APB_DIV	APB clock source divider. Value 0~4 mean to divide by 1,2,4,8,16. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4	0x00

			0x3 = DIV8 : divided by 8 0x4 = DIV16 : divided by 16	
15..12	-	Reserved	Reserved	0x00
11..8	rw	CSC_AHB_DIV	AHB clock source divider. Value 0~9 mean to divide by 1,2,4,8,16,32,64,128,256,512. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8 0x4 = DIV16 : divided by 16 0x5 = DIV32 : divided by 32 0x6 = DIV64 : divided by 64 0x7 = DIV128 : divided by 128 0x8 = DIV256 : divided by 256 0x9 = DIV512 : divided by 512	0x00
7..6	-	Reserved	Reserved	0x00
5..4	rw	CSC_PLLO_DIV	PLL output clock source divider 0x0 = DIV4 : divided by 4 0x1 = DIV3 : divided by 3 0x2 = DIV2 : divided by 2 0x3 = DIV1 : divided by 1	0x00
3..2	-	Reserved	Reserved	0x00
1..0	rw	CSC_PLLI_DIV	PLL input clock source divider 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV6 : divided by 6	0x00

1.10.7. CSC internal clock output control register

CSC_CKO	CSC internal clock output control register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	CSC_CKO_SEL[2:0]			CSC_CKO_DIV[1:0]		Reserved	CSC_CKO_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6..4	rw	CSC_CKO_SEL	Internal clock output source select 0x0 = CK_MAIN 0x1 = CK_AHB 0x2 = CK_APB 0x3 = CK_HS 0x4 = CK_LS 0x5 = CK_XOSC	0x00
3..2	rw	CSC_CKO_DIV	Internal clock output divider 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
1	-	Reserved	Reserved	0x00
0	rw	CSC_CKO_EN	Internal clock output enable. When enables, it will reset the	0x00

			output divider. 0x0 = Disable 0x1 = Enable	

1.10.8. CSC AHB clock control register

CSC_AHB	CSC AHB clock control register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
CSC_DMA_EN	Reserved		CSC_EMB_EN	Reserved			CSC_GPL_EN
7	6	5	4	3	2	1	0
Reserved			CSC_IOPE_EN	CSC_IOPD_EN	CSC_IOPC_EN	CSC_IOPB_EN	CSC_IOPA_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	CSC_DMA_EN	DMA clock source enable. 0 = Disable 1 = Enable	0x00
14..13	-	Reserved	Reserved	0x00
12	rw	CSC_EMB_EN	External memory bus clock source enable. 0 = Disable 1 = Enable	0x00
11..9	-	Reserved	Reserved	0x00
8	rw	CSC_GPL_EN	GPL clock source enable. 0 = Disable 1 = Enable	0x00
7..5	-	Reserved	Reserved for IOPF~IOPH	0x00
4	rw	CSC_IOPE_EN	IO Port E clock source enable. When disables, the data port register PE_OUT is still able to read but is disabled to write. 0 = Disable 1 = Enable	0x00
3	rw	CSC_IOPD_EN	IO Port D clock source enable. When disables, the data port register PD_OUT is still able to read but is disabled to write. 0 = Disable 1 = Enable	0x00
2	rw	CSC_IOPC_EN	IO Port C clock source enable. When disables, the data port register PC_OUT is still able to read but is disabled to write. 0 = Disable 1 = Enable	0x00
1	rw	CSC_IOPB_EN	IO Port B clock source enable. When disables, the data port register PB_OUT is still able to read but is disabled to write. 0 = Disable 1 = Enable	0x00
0	rw	CSC_IOPA_EN	IO Port A clock source enable. When disables, the data port register PA_OUT is still able to read but is disabled to write. 0 = Disable 1 = Enable	0x00

1.10.9. CSC APB clock control register 0

CSC_APB0	CSC APB clock control register 0		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved		CSC_APX_EN	CSC_USB_EN	Reserved			

23	22	21	20	19	18	17	16
CSC_URT7_EN	CSC_URT6_EN	CSC_URT5_EN	CSC_URT4_EN	Reserved	CSC_URT2_EN	CSC_URT1_EN	CSC_URT0_EN
15	14	13	12	11	10	9	8
Reserved		Reserved	CSC_SPI0_EN	Reserved		CSC_I2C1_EN	CSC_I2C0_EN
7	6	5	4	3	2	1	0
CSC_WWDT_EN	CSC_IWDT_EN	CSC_RTC_EN	Reserved	CSC_DAC_EN	CSC_CMP_EN	Reserved	CSC_ADC0_EN

Bit	Attr	Bit Name	Description	Reset
31..30	-	Reserved	Reserved	0x00
29	rw	CSC_APX_EN	APB module clock source enable. 0 = Disable 1 = Enable	0x00
28	rw	CSC_USB_EN	USB module clock source enable. 0 = Disable 1 = Enable	0x00
27..24	-	Reserved	Reserved	0x00
23	rw	CSC_URT7_EN	URT7 UART module clock source enable. 0 = Disable 1 = Enable	0x00
22	rw	CSC_URT6_EN	URT6 UART module clock source enable. 0 = Disable 1 = Enable	0x00
21	rw	CSC_URT5_EN	URT5 UART module clock source enable. 0 = Disable 1 = Enable	0x00
20	rw	CSC_URT4_EN	URT4 UART module clock source enable. 0 = Disable 1 = Enable	0x00
19	-	Reserved	Reserved	0x00
18	rw	CSC_URT2_EN	URT2 UART module clock source enable. 0 = Disable 1 = Enable	0x00
17	rw	CSC_URT1_EN	URT1 UART module clock source enable. 0 = Disable 1 = Enable	0x00
16	rw	CSC_URT0_EN	URT0 UART module clock source enable. 0 = Disable 1 = Enable	0x00
15..14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	rw	CSC_SPI0_EN	SPI0 module clock source enable. 0 = Disable 1 = Enable	0x00
11..10	-	Reserved	Reserved	0x00
9	rw	CSC_I2C1_EN	I2C1 module clock source enable. 0 = Disable 1 = Enable	0x00
8	rw	CSC_I2C0_EN	I2C0 module clock source enable. 0 = Disable 1 = Enable	0x00
7	rw	CSC_WWDT_EN	WWDT module clock source enable. (This register is reset only by Cold reset.) 0 = Disable 1 = Enable	0x00
6	rw	CSC_IWDT_EN	IWDT module clock source enable. This bit is control by IWDT_LOCK/CSC_KEY for register lock and protect functions. (This register is reset only by Cold reset.) 0 = Disable 1 = Enable	0x00
5	rw	CSC_RTC_EN	RTC module clock source enable. This bit is control by	0x00

			RTL_LOCK/CSC_KEY for register lock and protect functions. (This register is reset only by Cold reset.) 0 = Disable 1 = Enable	
4	-	Reserved	Reserved	0x00
3	rw	CSC_DAC_EN	DAC module clock source enable. 0 = Disable 1 = Enable	0x00
2	rw	CSC_CMP_EN	CMP module clock source enable. 0 = Disable 1 = Enable	0x00
1	-	Reserved	Reserved	0x00
0	rw	CSC_ADC0_EN	ADC module clock source enable. 0 = Disable 1 = Enable	0x00

1.10.10. CSC APB clock control register 1

CSC_APB1	CSC APB clock control register 1
Offset Address : 0x24	Reset Value : 0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
CSC_TM36_EN	Reserved			CSC_TM26_EN	Reserved		CSC_TM20_EN
7	6	5	4	3	2	1	0
CSC_TM16_EN	Reserved		CSC_TM10_EN	Reserved		CSC_TM01_EN	CSC_TM00_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	CSC_TM36_EN	TM36 module clock source enable. 0 = Disable 1 = Enable	0x00
14..12	-	Reserved	Reserved	0x00
11	rw	CSC_TM26_EN	TM26 module clock source enable. 0 = Disable 1 = Enable	0x00
10..9	-	Reserved	Reserved	0x00
8	rw	CSC_TM20_EN	TM20 module clock source enable. 0 = Disable 1 = Enable	0x00
7	rw	CSC_TM16_EN	TM11 module clock source enable. 0 = Disable 1 = Enable	0x00
6..5	-	Reserved	Reserved	0x00
4	rw	CSC_TM10_EN	TM10 module clock source enable. 0 = Disable 1 = Enable	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	CSC_TM01_EN	TM01 module clock source enable. 0 = Disable 1 = Enable	0x00
0	rw	CSC_TM00_EN	TM00 module clock source enable. 0 = Disable 1 = Enable	0x00

1.10.11. CSC SLEEP mode clock enable register 0

CSC_SLP0	CSC SLEEP mode clock enable register 0		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved		CSC_SLP_APX	CSC_SLP_USB	Reserved			
23	22	21	20	19	18	17	16
CSC_SLP_URT7	CSC_SLP_URT6	CSC_SLP_URT5	CSC_SLP_URT4	Reserved	CSC_SLP_URT2	CSC_SLP_URT1	CSC_SLP_URT0
15	14	13	12	11	10	9	8
Reserved			CSC_SLP_SPI0	Reserved		CSC_SLP_I2C1	CSC_SLP_I2C0
7	6	5	4	3	2	1	0
CSC_SLP_WWDT	CSC_SLP_IWDT	CSC_SLP_RTC	Reserved	CSC_SLP_DAC	CSC_SLP_CMP	Reserved	CSC_SLP_ADC0

Bit	Attr	Bit Name	Description	Reset
31..30	-	Reserved	Reserved	0x00
29	rw	CSC_SLP_APX	APB module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
28	rw	CSC_SLP_USB	USB module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
27..24	-	Reserved	Reserved	0x00
23	rw	CSC_SLP_URT7	URT7 UART module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
22	rw	CSC_SLP_URT6	URT6 UART module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
21	rw	CSC_SLP_URT5	URT5 UART module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
20	rw	CSC_SLP_URT4	URT4 UART module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
19	-	Reserved	Reserved	0x00
18	rw	CSC_SLP_URT2	URT2 UART module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
17	rw	CSC_SLP_URT1	URT1 UART module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
16	rw	CSC_SLP_URT0	URT0 UART module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
15..13	-	Reserved	Reserved	0x00
12	rw	CSC_SLP_SPI0	SPI0 module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
11..10	-	Reserved	Reserved	0x00
9	rw	CSC_SLP_I2C1	I2C1 module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
8	rw	CSC_SLP_I2C0	I2C0 module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
7	rw	CSC_SLP_WWDT	WWDT module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
6	rw	CSC_SLP_IWDT	IWDT module clock enable in SLEEP mode. This bit is control by IWDT_LOCK/CSC_KEY for register lock and protect functions. (The register is loaded from CFG OR only after Cold	0x00

			reset.) 0 = Disable 1 = Enable	
5	rw	CSC_SLP_RTC	IWDT module clock enable in SLEEP mode. This bit is control by RTC_LOCK/CSC_KEY for register lock and protect functions. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	CSC_SLP_DAC	DAC module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
2	rw	CSC_SLP_CMP	CMP module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
1	-	Reserved	Reserved	0x00
0	rw	CSC_SLP_ADC0	ADC module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00

1.10.12. CSC SLEEP mode clock enable register 1

CSC_SLP1	CSC SLEEP mode clock enable register 1		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	CSC_SLP_EMB	CSC_SLP_DMA	Reserved			CSC_SLP_FLASH	CSC_SLP_SRAM
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
CSC_SLP_TM36	Reserved			CSC_SLP_TM26	Reserved		CSC_SLP_TM20
7	6	5	4	3	2	1	0
CSC_SLP_TM16	Reserved		CSC_SLP_TM10	Reserved		CSC_SLP_TM01	CSC_SLP_TM00

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	CSC_SLP_EMB	EMB module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
29	rw	CSC_SLP_DMA	DMA module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
28..26	-	Reserved	Reserved	0x00
25	rw	CSC_SLP_FLASH	Embedded Flash memory clock enable in SLEEP mode. The bit is no effect and the embedded Flash memory clock is always disabled if CSC_SLP_DMA is disabled. 0 = Disable 1 = Enable	0x00
24	rw	CSC_SLP_SRAM	Embedded SRAM memory clock enable in SLEEP mode. The bit is no effect and the embedded SRAM memory clock is always disabled if CSC_SLP_DMA is disabled. 0 = Disable 1 = Enable	0x00
23..16	-	Reserved	Reserved	0x00
15	rw	CSC_SLP_TM36	TM36 module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
14..12	-	Reserved	Reserved	0x00
11	rw	CSC_SLP_TM26	TM26 module clock enable in SLEEP mode. 0 = Disable	0x00

			1 = Enable	
10..9	-	Reserved	Reserved	0x00
8	rw	CSC_SLP_TM20	TM20 module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
7	rw	CSC_SLP_TM16	TM11 module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
6..5	-	Reserved	Reserved	0x00
4	rw	CSC_SLP_TM10	TM10 module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	CSC_SLP_TM01	TM01 module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00
0	rw	CSC_SLP_TM00	TM00 module clock enable in SLEEP mode. 0 = Disable 1 = Enable	0x00

1.10.13. CSC STOP mode clock enable register 0

CSC_STP0	CSC STOP mode clock enable register 0		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	CSC_STP_IWDT	CSC_STP_RTC	Reserved	Reserved	Reserved	Reserved	Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	rw	CSC_STP_IWDT	IWDT module clock enable in STOP mode. This bit is control by IWDT_LOCK/ICSC_KEY for register lock and protect functions. (The register is loaded from CFG OR only after Cold reset.) 0 = Disable 1 = Enable	0x00
5	rw	CSC_STP_RTC	IWDT module clock enable in STOP mode. This bit is control by RTC_LOCK/CSC_KEY for register lock and protect functions. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	-	Reserved	Reserved	0x00
0	-	Reserved	Reserved	0x00

1.10.14. CSC clock source select register 0

CSC_CKS0	CSC clock source select register 0		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved					CSC_APX_CKS	Reserved	CSC_USB_CKS
7	6	5	4	3	2	1	0
Reserved		CSC_DAC_CKS	CSC_CMP_CKS	Reserved			CSC_ADC0_CKS

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..11	-	Reserved	Reserved	0x00
10	rw	CSC_APX_CKS	APB module process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
9	-	Reserved	Reserved	0x00
8	rw	CSC_USB_CKS	USB SIE clock source select. 0 = CK_PLL : PLL clock out 1 = CK_SYS : CPU System Clock.	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	CSC_DAC_CKS	DAC process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
4	rw	CSC_CMP_CKS	CMP process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
3..1	-	Reserved	Reserved	0x00
0	rw	CSC_ADC0_CKS	ADC0 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00

1.10.15. CSC clock source select register 1

CSC_CKS1	CSC clock source select register 1		
Offset Address :	0x44	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	CSC_URT7_CKS	Reserved	CSC_URT6_CKS	Reserved	CSC_URT5_CKS	Reserved	CSC_URT4_CKS
23	22	21	20	19	18	17	16
Reserved	Reserved	Reserved	CSC_URT2_CKS	Reserved	CSC_URT1_CKS	Reserved	CSC_URT0_CKS
15	14	13	12	11	10	9	8
Reserved							CSC_SPI0_CKS
7	6	5	4	3	2	1	0
Reserved					CSC_I2C1_CKS	Reserved	CSC_I2C0_CKS

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	CSC_URT7_CKS	URT7 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
29	-	Reserved	Reserved	0x00
28	rw	CSC_URT6_CKS	URT6 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
27	-	Reserved	Reserved	0x00
26	rw	CSC_URT5_CKS	URT5 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
25	-	Reserved	Reserved	0x00

24	rw	CSC_URT4_CKS	URT4 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
23	-	Reserved	Reserved	0x00
22	-	Reserved	Reserved	0x00
21	-	Reserved	Reserved	0x00
20	rw	CSC_URT2_CKS	URT2 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
19	-	Reserved	Reserved	0x00
18	rw	CSC_URT1_CKS	URT1 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
17	-	Reserved	Reserved	0x00
16	rw	CSC_URT0_CKS	URT0 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
15..9	-	Reserved	Reserved	0x00
8	rw	CSC_SPI0_CKS	SPI0 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
7..3	-	Reserved	Reserved	0x00
2	rw	CSC_I2C1_CKS	I2C1 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
1	-	Reserved	Reserved	0x00
0	rw	CSC_I2C0_CKS	I2C0 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00

1.10.16. CSC clock source select register 2

CSC_CKS2	CSC clock source select register 2		
Offset Address :	0x48	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	CSC_TM36_CKS	Reserved					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved	CSC_TM26_CKS	Reserved					CSC_TM20_CKS
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved	CSC_TM16_CKS	Reserved					CSC_TM10_CKS
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					CSC_TM01_CKS	Reserved	CSC_TM00_CKS

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	CSC_TM36_CKS	TM36 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
29..24	-	Reserved	Reserved	0x00
23	-	Reserved	Reserved	0x00
22	rw	CSC_TM26_CKS	TM26 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
21..17	-	Reserved	Reserved	0x00
16	rw	CSC_TM20_CKS	TM20 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
15	-	Reserved	Reserved	0x00
14	rw	CSC_TM16_CKS	TM11 process clock source select.	0x00

			0x0 = CK_APB 0x1 = CK_AHB	
13..9	-	**Reserved**	Reserved	0x00
8	rw	**CSC_TM10_CKS**	TM10 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
7..3	-	**Reserved**	Reserved	0x00
2	rw	**CSC_TM01_CKS**	TM01 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00
1	-	**Reserved**	Reserved	0x00
0	rw	**CSC_TM00_CKS**	TM00 process clock source select. 0x0 = CK_APB 0x1 = CK_AHB	0x00

1.10.17. CSC Register Map

CSC Register Map **Register Number = 16**

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	CSC_STA	CSC_PLL_STA	CSC_IHRCO_STA	CSC_ILRCO_STA	CSC_XOSC_STA	Reserved	CSC_MAIN_STA [2:0]			CSC_HS_STA[3:0]				CSC_LS_STA[3:0]				Reserved		CSC_PLLI_STA [1:0]		CSC_HS2_STA [3:0]				CSC_MCDF	CSC_PLLF	CSC_IHRCOF	CSC_ILRCOF	Reserved		CSC_XOSCF	Reserved
Reset	0x00020000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	CSC_INT	Reserved																Reserved								CSC_MCD_IE	CSC_PLL_IE	CSC_IHRCO_IE	CSC_ILRCO_IE	Reserved		CSC_XOSC_IE	CSC_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	CSC_PLL	Reserved								Reserved						CSC_XOSC_GN [1:0]		Reserved	CSC_PLL_MULX [5:0]						CSC_PLL_MUL	Reserved	Reserved				Reserved	CSC_PLLI_SEL	CSC_PLL_MDS
Reset	0x00000004	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0x0C	CSC_KEY	Reserved																CSC_KEY[15:0]															
Reset	0x00000001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x10	CSC_CR0	Reserved								CSC_MCD_SEL [1:0]		Reserved			CSC_IHRCO_SEL	Reserved	CSC_ST_SEL	CSC_MAIN_SEL [1:0]		CSC_HS2_SEL [1:0]		CSC_HS_SEL[1:0]		CSC_LS_SEL[1:0]		Reserved		CSC_PLL_EN	CSC_MCD_DIS	CSC_IHRCO_EN	Reserved		
Reset	0x00000200	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0x14	CSC_DIV	Reserved				CSC_UT_DIV[1:0]		Reserved	Reserved	Reserved		CSC_USB_DIV [1:0]		Reserved	CSC_APB_DIV [2:0]			Reserved				CSC_AHB_DIV [3:0]				Reserved		CSC_PLLO_DIV [1:0]		Reserved		CSC_PLLI_DIV [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	CSC_CKO	Reserved																Reserved								Reserved	CSC_CKO_SEL [2:0]			CSC_CKO_DIV [1:0]		Reserved	CSC_CKO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	CSC_AHB	Reserved																CSC_DMA_EN	Reserved		CSC_EMB_EN	Reserved			CSC_GPL_EN	Reserved			CSC_IOPE_EN	CSC_IOPD_EN	CSC_IOPC_EN	CSC_IOPB_EN	CSC_IOPA_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x20	CSC_APB0	Reserved		CSC_APX_EN	CSC_USB_EN	Reserved				CSC_URT7_EN	CSC_URT6_EN	CSC_URT5_EN	CSC_URT4_EN	Reserved	CSC_URT2_EN	CSC_URT1_EN	CSC_URT0_EN	Reserved		Reserved	CSC_SPI0_EN	Reserved		CSC_I2C1_EN	CSC_I2C0_EN	CSC_WWDT_EN	CSC_IWDT_EN	CSC_RTC_EN	Reserved	CSC_DAC_EN	CSC_CMP_EN	Reserved	CSC_ADC0_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	CSC_APB1	Reserved																CSC_TM36_EN	Reserved			CSC_TM26_EN	Reserved		CSC_TM20_EN	CSC_TM16_EN	Reserved		CSC_TM10_EN	Reserved		CSC_TM01_EN	CSC_TM00_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	CSC_SLP0	Reserved		CSC_SLP_APX	CSC_SLP_USB	Reserved				CSC_SLP_URT7	CSC_SLP_URT6	CSC_SLP_URT5	CSC_SLP_URT4	Reserved	CSC_SLP_URT2	CSC_SLP_URT1	CSC_SLP_URT0	Reserved			CSC_SLP_SPI0	Reserved		CSC_SLP_I2C1	CSC_SLP_I2C0	CSC_SLP_WWDT	CSC_SLP_IWDT	CSC_SLP_RTC	Reserved	CSC_SLP_DAC	CSC_SLP_CMP	Reserved	CSC_SLP_ADC0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	CSC_SLP1	Reserved	CSC_SLP_EMB	CSC_SLP_DMA	Reserved			CSC_SLP_FLASH	CSC_SLP_SRAM	Reserved								CSC_SLP_TM36	Reserved			CSC_SLP_TM26	Reserved		CSC_SLP_TM20	CSC_SLP_TM16	Reserved		CSC_SLP_TM10	Reserved		CSC_SLP_TM01	CSC_SLP_TM00
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	CSC_STP0	Reserved																Reserved								Reserved	CSC_STP_IWDT	CSC_STP_RTC	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	CSC_CKS0	Reserved																Reserved					CSC_APX_CKS	Reserved	CSC_USB_CKS	Reserved		CSC_DAC_CKS	CSC_CMP_CKS	Reserved			CSC_ADC0_CKS
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x44	CSC_CKS1	Reserved	CSC_URT7_CKS	Reserved	CSC_URT6_CKS	Reserved	CSC_URT5_CKS	Reserved	CSC_URT4_CKS	Reserved	Reserved	Reserved	CSC_URT2_CKS	Reserved	CSC_URT1_CKS	Reserved	CSC_URT0_CKS	Reserved							CSC_SPI0_CKS	Reserved					CSC_I2C1_CKS	Reserved	CSC_I2C0_CKS
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x48	CSC_CKS2	Reserved	CSC_TM36_CKS	Reserved						Reserved	CSC_TM26_CKS	Reserved					CSC_TM20_CKS	Reserved	CSC_TM16_CKS	Reserved					CSC_TM10_CKS	Reserved					CSC_TM01_CKS	Reserved	CSC_TM00_CKS
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.11. Power Control Registers

Power Control	(PW) Power Management Controller
Base Address :	0x4C020000

1.11.1. PW status register

PW_STA	PW status register		
Offset Address :	0x00	Reset Value :	0x00000002

31	30	29	28	27	26	25	24
Reserved					PW_BOD2_S	PW_BOD1_S	Reserved
23	22	21	20	19	18	17	16
Reserved		PW_WKMODE[1:0]		Reserved		PW_STATE[1:0]	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
PW_WKF	PW_BOD2F	PW_BOD1F	PW_BOD0F	Reserved	Reserved	PW_PORF	Reserved

Bit	Attr	Bit Name	Description	Reset
31..27	-	Reserved	Reserved	0x00
26	r	PW_BOD2_S	Brown-Out detect BOD2 status. 0 = High : VDD is high than BOD2 threshold 1 = Low : VDD is lower than BOD2 threshold	0x00
25	r	PW_BOD1_S	Brown-Out detect BOD1 status. 0 = High : VDD is high than BOD1 threshold 1 = Low : VDD is lower than BOD1 threshold	0x00
24	-	Reserved	Reserved	0x00
23..22	-	Reserved	Reserved	0x00
21..20	r	PW_WKMODE	System wakeup from which power-down mode status. 0x0 = NONE : Never wakeup from power-down mode. 0x1 = SLEEP 0x2 = STOP 0x3 = Reserved	0x00
19..18	-	Reserved	Reserved	0x00
17..16	r	PW_STATE	System operation power mode state. These status bits are used for internal debugging only. 0x0 = ON 0x1 = SLEEP 0x2 = STOP 0x3 = Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7	rw	PW_WKF	System received wakeup event flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	rw	PW_BOD2F	BOD2 brown-out detection interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	rw	PW_BOD1F	BOD1 brown-out detection interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	PW_BOD0F	BOD0 brown-out detection interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal : No event occurred and VDD is than high BOD0 threshold 1 = Happened : Event happened and VDD is lower than BOD0 threshold	0x00
3	-	Reserved	Reserved	0x00

2	-	Reserved	Reserved	0x00
1	rw	PW_PORF	Power-On reset status flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x01
0	-	Reserved	Reserved	0x00

1.11.2. PW interrupt enable register

PW_INT	PW interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
PW_WK_IE	PW_BOD2_IE	PW_BOD1_IE	PW_BOD0_IE	Reserved			PW_IEA

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	rw	PW_WK_IE	System received wakeup event interrupt enable bit. 0 = Disable 1 = Enable	0x00
6	rw	PW_BOD2_IE	BOD2 brown-out detection interrupt enable. 0 = Disable 1 = Enable	0x00
5	rw	PW_BOD1_IE	BOD1 brown-out detection interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	PW_BOD0_IE	BOD0 brown-out detection interrupt enable. 0 = Disable 1 = Enable	0x00
3..1	-	Reserved	Reserved	0x00
0	rw	PW_IEA	PW interrupt all enable. When disables, the PW global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.11.3. PW write protected Key register

PW_KEY	PW write protected Key register		
Offset Address :	0x0C	Reset Value :	0x00000001

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
PW_KEY[15:8]							
7	6	5	4	3	2	1	0
PW_KEY[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000

15..0	rw	PW_KEY	PW key register. Write value 0xA217 to unprotect the register write access. Write other value except 0xA217 to protect the registers except PW_STA, PW_KEY registers. For read access : 0 = Unprotected 1 = Protected	0x0001

1.11.4. PW control register 0

PW_CR0	PW control register 0		
Offset Address :	0x10	Reset Value :	0x00000080

31	30	29	28	27	26	25	24
Reserved				Reserved		Reserved	
23	22	21	20	19	18	17	16
Reserved		PW_WKSTP_DSEL[1:0]		Reserved	PW_WKSLP_MDS	Reserved	
15	14	13	12	11	10	9	8
PW_BOD2_TRGS[1:0]		PW_BOD2_EN	Reserved	PW_BOD1_TH[1:0]		PW_BOD1_TRGS[1:0]	
7	6	5	4	3	2	1	0
PW_LDO_STP	PW_LDO_ON	PW_BOD1_EN	PW_BOD0_EN	Reserved	Reserved	PW_IVR_EN	Reserved

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27..26	-	Reserved	Reserved	0x00
25..24	-	Reserved	Reserved	0x00
23..22	-	Reserved	Reserved	0x00
21..20	rw	PW_WKSTP_DSEL	Wakeup delay time selection from STOP mode. The wakeup time is including of this wakeup delay time and ILRCO start up time if ILRCO is off in STOP mode. It is calculation from wakeup event trigger to CPU wakeup running. Also both the ILRCO and chip LDO output are stable. (The register is loaded from OR only after Cold reset.) 0x0 = DT0 (16~32us) 0x1 = DT1 (32~48us) 0x2 = DT2 (64~80us) 0x3 = DT3 (128~144us)	0x00
19	-	Reserved	Reserved	0x00
18	rw	PW_WKSLP_MDS	Wakeup mode selection from SLEEP mode . When selects 'Normal', the MCU wakeup from SLEEP mode is about 5 AHB clock and MCU current consumption is normal in SLEEP mode. When selects 'Low Power', the MCU wakeup from SLEEP mode is slower but MCU current consumption is lower in SLEEP mode. 0 = Normal 1 = Low Power	0x00
17..16	-	Reserved	Reserved	0x00
15..14	rw	PW_BOD2_TRGS	BOD2 Interrupt trigger selection. 0x0 = Reserved 0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	0x00
13	rw	PW_BOD2_EN	BOD2 voltage detect enable. 0 = Disable 1 = Enable	0x00
12	-	Reserved	Reserved	0x00
11..10	rw	PW_BOD1_TH	BOD1 detect voltage threshold select. (The register is loaded from OR only after Cold reset.) 0x0 = 2.0v 0x1 = 2.4v 0x2 = 3.7v	0x00

			0x3 = 4.2v	
9..8	rw	PW_BOD1_TRGS	BOD1 Interrupt trigger selection. 0x0 = Reserved 0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	0x00
7	rw	PW_LDO_STP	Core voltage LDO mode select when STOP mode. (default=1) 0 = Normal 1 = Low Power	0x01
6	rw	PW_LDO_ON	Core voltage LDO mode select when ON or SLEEP mode. 0 = Normal 1 = Low Power	0x00
5	rw	PW_BOD1_EN	BOD1 voltage detect enable. 0 = Disable 1 = Enable	0x00
4	rw	PW_BOD0_EN	BOD0 voltage detect enable. 0 = Disable 1 = Enable	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	rw	PW_IVR_EN	Internal voltage reference source enable. The internal voltage reference(VBUF) source is using for ADC and Analog comparator analog part. 0 = Disable 1 = Enable	0x00
0	-	Reserved	Reserved	0x00

1.11.5. PW control register 1

PW_CR1	PW control register 1		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved			PW_STP_USB	Reserved			PW_SLP_USB
23	22	21	20	19	18	17	16
Reserved	Reserved	PW_STP_CMP1	PW_STP_CMP0	Reserved	Reserved	PW_SLP_CMP1	PW_SLP_CMP0
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	PW_STP_BOD2	PW_STP_BOD1	PW_STP_BOD0	Reserved		PW_STP_POR	Reserved

Bit	Attr	Bit Name	Description	Reset
31..29	-	Reserved	Reserved	0x00
28	rw	PW_STP_USB	USB0 power-on configuration after enter STOP mode. 0 = Disable 1 = power-on	0x00
27..25	-	Reserved	Reserved	0x00
24	rw	PW_SLP_USB	USB0 power-on configuration after enter SLEEP mode. 0 = Disable 1 = power-on	0x00
23	-	Reserved	Reserved	0x00
22	-	Reserved	Reserved	0x00
21	rw	PW_STP_CMP1	Analog comparator CMP1 power-on configuration after enter STOP mode. 0 = Disable 1 = power-on	0x00
20	rw	PW_STP_CMP0	Analog comparator CMP0 power-on configuration after enter STOP mode. 0 = Disable 1 = power-on	0x00

19	-	Reserved	Reserved	0x00
18	-	Reserved	Reserved	0x00
17	rw	PW_SLP_CMP1	Analog comparator CMP1 power-on configuration after enter SLEEP mode. 0 = Disable 1 = power-on	0x00
16	rw	PW_SLP_CMP0	Analog comparator CMP0 power-on configuration after enter SLEEP mode. 0 = Disable 1 = power-on	0x00
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	rw	PW_STP_BOD2	BOD2 power-on configuration after enter STOP mode. 0 = Disable 1 = Enable	0x00
5	rw	PW_STP_BOD1	BOD1 power-on configuration after enter STOP mode. 0 = Disable 1 = Enable	0x00
4	rw	PW_STP_BOD0	BOD0 power-on configuration after enter STOP mode 0 = Disable 1 = Enable	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	PW_STP_POR	POR power-on configuration after enter STOP mode. 0 = Disable 1 = Enable	0x00
0	-	Reserved	Reserved	0x00

1.11.6. PW STOP mode wakeup control register 0

PW_WKSTP0	PW STOP mode wakeup control register 0		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							PW_WKSTP_USB
23	22	21	20	19	18	17	16
Reserved				Reserved	Reserved	PW_WKSTP_CMP1	PW_WKSTP_CMP0
15	14	13	12	11	10	9	8
Reserved				Reserved	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0
Reserved	PW_WKSTP_BOD2	PW_WKSTP_BOD1	PW_WKSTP_BOD0	Reserved			

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	rw	PW_WKSTP_USB	USB0 module event wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
23..20	-	Reserved	Reserved	0x00
19	-	Reserved	Reserved	0x00
18	-	Reserved	Reserved	0x00
17	rw	PW_WKSTP_CMP1	Analog comparator CMP1 voltage detection wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
16	rw	PW_WKSTP_CMP0	Analog comparator CMP0 voltage detection wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
15..12	-	Reserved	Reserved	0x00
11	-	Reserved	Reserved	0x00
10	-	Reserved	Reserved	0x00

9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	rw	PW_WKSTP_BOD2	BOD1 voltage detection wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
5	rw	PW_WKSTP_BOD1	BOD1 voltage detection wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
4	rw	PW_WKSTP_BOD0	BOD0 voltage detection wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
3..0	-	Reserved	Reserved	0x00

1.11.7. PW STOP mode wakeup control register 1

PW_WKSTP1	PW STOP mode wakeup control register 1		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	Reserved						
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						PW_WKSTP_I2C1	PW_WKSTP_I2C0
7	6	5	4	3	2	1	0
Reserved	PW_WKSTP_IWDT	PW_WKSTP_RTC	Reserved	Reserved		Reserved	Reserved

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..10	-	Reserved	Reserved	0x00
9	rw	PW_WKSTP_I2C1	I2C1 slave address detection event wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
8	rw	PW_WKSTP_I2C0	I2C0 slave address detection wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
7	-	Reserved	Reserved	0x00
6	rw	PW_WKSTP_IWDT	IWDT module events wakeup from STOP mode enable bit. This bit is control by IWDT_LOCK/PW_KEY for register lock and protect functions. 0 = Disable 1 = Enable	0x00
5	rw	PW_WKSTP_RTC	RTC module events wakeup from STOP mode enable bit. This bit is control by RTC_LOCK/PW_KEY for register lock and protect functions. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3..2	-	Reserved	Reserved	0x00
1	-	Reserved	Reserved	0x00
0	-	Reserved	Reserved	0x00

1.11.8. PW Register Map

PW Register Map Register Number = 7

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	PW_STA	Reserved					PW_BOD2_S	PW_BOD1_S	Reserved	Reserved		PW_WKMODE[1:0]		Reserved		PW_STATE[1:0]		Reserved								PW_WKF	PW_BOD2F	PW_BOD1F	PW_BOD0F	Reserved	Reserved	PW_PORF	Reserved
Reset	0x00000002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0x04	PW_INT	Reserved																Reserved								PW_WK_IE	PW_BOD2_IE	PW_BOD1_IE	PW_BOD0_IE	Reserved			PW_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	PW_KEY	Reserved																PW_KEY[15:0]															
Reset	0x00000001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x10	PW_CR0	Reserved				Reserved		Reserved		Reserved		PW_WKSTP_DSEL[1:0]		Reserved	PW_WKSLP_MDS	Reserved		PW_BOD2_TRGS[1:0]		PW_BOD2_EN	Reserved	PW_BOD1_TH[1:0]		PW_BOD1_TRGS[1:0]		PW_LDO_STP	PW_LDO_ON	PW_BOD1_EN	PW_BOD0_EN	Reserved	Reserved	PW_IVR_EN	Reserved
Reset	0x00000080	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0x14	PW_CR1	Reserved			PW_STP_USB	Reserved			PW_SLP_USB	Reserved	Reserved	PW_STP_CMP1	PW_STP_CMP0	Reserved	Reserved	PW_SLP_CMP1	PW_SLP_CMP0	Reserved								Reserved	PW_STP_BOD2	PW_STP_BOD1	PW_STP_BOD0	Reserved		PW_STP_POR	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	PW_WKSTP0	Reserved							PW_WKSTP_USB	Reserved				Reserved	Reserved	PW_WKSTP_CMP1	PW_WKSTP_CMP0	Reserved				Reserved	Reserved	Reserved	Reserved	Reserved	PW_WKSTP_BOD2	PW_WKSTP_BOD1	PW_WKSTP_BOD0	Reserved			
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	PW_WKSTP1	Reserved	Reserved							Reserved								Reserved						PW_WKSTP_I2C1	PW_WKSTP_I2C0	Reserved	PW_WKSTP_IWDT	PW_WKSTP_RTC	Reserved	Reserved		Reserved	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.12. System Control Registers

System Control	(SYS) System and Chip Control
Base Address :	0x4C030000

1.12.1. SYS interrupt enable register

SYS_INT	SYS interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SYS_IEA

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	SYS_IEA	System interrupt all enable. When disables, the INT_SYS global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.12.2. SYS chip manufacture identification code

SYS_MID	SYS chip manufacture identification code		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
SYS_MID[31:24]							
23	22	21	20	19	18	17	16
SYS_MID[23:16]							
15	14	13	12	11	10	9	8
SYS_MID[15:8]							
7	6	5	4	3	2	1	0
SYS_MID[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	SYS_MID	Chip manufacture identification code.	0x00000000

1.12.3. SYS System control register 0

SYS_CR0	SYS System control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
SYS_GPR[7:0]							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	rw	SYS_GPR	General purpose data register bits.	0x00
15..8	-	Reserved	Reserved	0x00
7..0	-	Reserved	Reserved	0x00

1.12.4. SYS Backup register 0

SYS_BKP0	SYS Backup register 0		
Offset Address :	0x20	Reset Value :	0xFFFFFFFF

31	30	29	28	27	26	25	24
SYS_BKP0[31:24]							
23	22	21	20	19	18	17	16
SYS_BKP0[23:16]							
15	14	13	12	11	10	9	8
SYS_BKP0[15:8]							
7	6	5	4	3	2	1	0
SYS_BKP0[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	SYS_BKP0	This register is used for application firmware without any hardware control. It can be written or read but not reset by POR or other cold/warm reset.	0xFFFFFFFF

1.12.5. SYS Register Map

SYS Register Map **Register Number = 4**

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x04	SYS_INT	Reserved																Reserved								Reserved							SYS_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	SYS_MID	SYS_MID[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	SYS_CR0	Reserved								SYS_GPR[7:0]								Reserved								Reserved							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	SYS_BKP0	SYS_BKP0[31:0]																															
Reset	0xFFFFFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1.13. Memory Control Registers

Memory Control	(MEM) Internal Memory Controller
Base Address :	0x4D000000

1.13.1. MEM status register

MEM_STA	MEM status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved					Reserved	Reserved	MEM_IAPSEF
15	14	13	12	11	10	9	8
Reserved						Reserved	Reserved
7	6	5	4	3	2	1	0
Reserved	MEM_RPEF	MEM_WPEF	MEM_IAEF	Reserved	Reserved	MEM_EOPF	MEM_FBUSYF

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..19	-	Reserved	Reserved	0x00
18	-	Reserved	Reserved	0x00
17	-	Reserved	Reserved	0x00
16	r	MEM_IAPSEF	IAP Flash memory size setting error flag. 0 = Normal (Not busy) 1 = ERR (Size over maximum value error)	0x00
15..10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	rw	MEM_RPEF	Flash memory read protect error detection flag. When read the flash memory, this flag will be asserted if the operated command setting or address area is error. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
5	rw	MEM_WPEF	Flash memory write protect error detection flag. When write or erase the flash memory, this flag will be asserted if the operated command setting, address area is error or IHRCO device is disabled. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
4	rw	MEM_IAEF	Memory code execution illegal address error detection flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	rw	MEM_EOPF	Flash memory end of processing flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
0	r	MEM_FBUSYF	Flash memory access busy flag. 0 = Normal (Not busy) 1 = Busy	0x00

1.13.2. MEM interrupt enable register

MEM_INT	MEM interrupt enable register

Offset Address : 0x04 Reset Value : 0x00000000

31	30	29	28	27	26	25	24
Reserved						Reserved	Reserved
23	22	21	20	19	18	17	16
Reserved	MEM_RPE_RE	MEM_WPE_RE	MEM_IAE_RE	Reserved	Reserved		
15	14	13	12	11	10	9	8
Reserved						Reserved	Reserved
7	6	5	4	3	2	1	0
Reserved	MEM_RPE_IE	MEM_WPE_IE	MEM_IAE_IE	Reserved	Reserved	MEM_EOP_IE	MEM_IEA

Bit	Attr	Bit Name	Description	Reset
31..26	-	Reserved	Reserved	0x00
25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23	-	Reserved	Reserved	0x00
22	rw	MEM_RPE_RE	Flash memory read protect error detection reset enable. 0 = Disable 1 = Enable	0x00
21	rw	MEM_WPE_RE	Flash memory write protect error detection reset enable. 0 = Disable 1 = Enable	0x00
20	rw	MEM_IAE_RE	Memory code execution illegal address detection reset enable. 0 = Disable 1 = Enable	0x00
19	-	Reserved	Reserved	0x00
18..16	-	Reserved	Reserved	0x00
15..10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	rw	MEM_RPE_IE	Flash memory read protect error detection interrupt enable. 0 = Disable 1 = Enable	0x00
5	rw	MEM_WPE_IE	Flash memory write protect error detection interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	MEM_IAE_IE	Memory code execution illegal address error detection interrupt enable. 0 = Disable 1 = Enable	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	rw	MEM_EOP_IE	Flash memory end of processing interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	MEM_IEA	Memory controller interrupt all enable. When disables, the INT_MEM global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.13.3. MEM write protected key register

MEM_KEY	MEM write protected key register

Offset Address : 0x0C Reset Value : 0x00010001

31	30	29	28	27	26	25	24
MEM_KEY2[15:8]							

23	22	21	20	19	18	17	16
MEM_KEY2[7:0]							
15	14	13	12	11	10	9	8
MEM_KEY[15:8]							
7	6	5	4	3	2	1	0
MEM_KEY[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	rw	MEM_KEY2	Reset key register-2. Write value 0xA217 to unprotect the register bits of MEM_ISP_WEN and MEM_ISP_REN write access. Write other value except 0xA217 to protect the register bits. For read access : 0 = Unprotected 1 = Protected	0x0001
15..0	rw	MEM_KEY	Reset key register. Write value 0xA217 to unprotect the register write access. Write other value except 0xA217 to protect the registers except MEM_STA, MEM_KEY registers. For read access : 0 = Unprotected 1 = Protected	0x0001

1.13.4. MEM control register 0

MEM_CR0	MEM control register 0		
Offset Address :	0x10	Reset Value :	0x00200002

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved		MEM_IAP_AEN	MEM_HSP_EN	Reserved		MEM_BOOT_MS[1:0]	
15	14	13	12	11	10	9	8
Reserved		MEM_FWAIT[1:0]		Reserved	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0
MEM_MDS[3:0]				Reserved	Reserved	MEM_HF_EN	MEM_EN

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..22	-	Reserved	Reserved	0x00
21	rw	MEM_IAP_AEN	IAP memory size MEM_IAP_SIZE register access enable. This bit is only able to write value 0. That is on effect to write value 1. (The register is loaded from CFG OR only after Cold reset.) 0 = Disable : Register access lock 1 = Enable	0x01
20	rw	MEM_HSP_EN	Flash memory read high speed mode enable during reset. When enables, the chip will read flash with no delay after cold reset. (The default value is loaded from CFG OR after Warm reset) 0 = Disable 1 = Enable	0x00
19..18	-	Reserved	Reserved	0x00
17..16	rw	MEM_BOOT_MS	System reset memory select and memory is mapped at 0x0000 0000. (The register is loaded from CFG OR only after Cold reset.) 0x0 = Application Flash 0x1 = Boot Flash 0x2 = Embedded SRAM 0x3 = Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13..12	rw	MEM_FWAIT	Flash memory read access wait state selection. These bits select the latency timer of the CK_AHB period to the flash	0x00

			access time. 0x0 = Zero : Zero wait state if 25 MHz > CK_AHB 0x1 = One : One wait state if 50MHz >CK_AHB> 25 MHz 0x3 = Two : Two wait state if 75MHz >CK_AHB> 50 MHz	
11	-	Reserved	Reserved	0x00
10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7..4	rw	MEM_MDS	AP/IAP flash memory access mode select. 0x0 = No (No Operation) 0x1 = Write (Write AP/IAP/ISPD Flash) 0x2 = Erase (Erase a page of AP/IAP/ISPD Flash) 0x3 = Reserved	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	rw	MEM_HF_EN	Flash memory data access error HardFault enable. When memory data read error has happened and MEM_RPE_IE / MEM_RPE_RE are disabled, it will induce HardFault if this bit is enabled. When memory data write error has happened and MEM_WPE_IE / MEM_WPE_RE are disabled, it will induce HardFault if this bit is enabled. 0 = Disable 1 = Enable	0x01
0	rw	MEM_EN	Memory controller enable. 0 = Disable 1 = Enable	0x00

1.13.5. MEM control register 1

MEM_CR1	MEM control register 1		
Offset Address :	0x14	Reset Value :	0x00000010

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				Reserved	Reserved	MEM_ISP_REN	MEM_ISP_WEN
7	6	5	4	3	2	1	0
Reserved			MEM_IAP_EXEC	MEM_ISPD_REN	MEM_ISPD_WEN	MEM_IAP_WEN	MEM_AP_WEN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	-	Reserved	Reserved	0x00
11	-	Reserved	Reserved	0x00
10	-	Reserved	Reserved	0x00
9	rw	MEM_ISP_REN	Flash ISP Boot memory read enable for AP program. (This register is protected by MEM_KEY2 register.) The ISP flash memory is always reading enabled when CPU is running in ISP program (ISP address space domain). This register is only able to set when boots from ISP mode. And it can clear or disable for all boot modes. 0 = Disable 1 = Enable	0x00
8	rw	MEM_ISP_WEN	Flash ISP Boot memory write enable. (This register is protected by MEM_KEY2 register.) This register is only able to set when boots from ISP mode. And it can clear or disable for all boot modes. 0 = Disable 1 = Enable	0x00

7..5	-	Reserved	Reserved	0x00
4	rw	MEM_IAP_EXEC	Flash IAP data memory code execution function enable. 0 = Disable 1 = Enable	0x01
3	rw	MEM_ISPD_REN	Flash ISP data memory read enable for ISP program. This register is able to set and clear when boots from ISP mode. It can only clear to disable but not set for other boot modes. 0 = Disable 1 = Enable	0x00
2	rw	MEM_ISPD_WEN	Flash ISP data memory write enable for ISP program. This register is only able to change when boots from ISP mode. The ISPD flash memory always can not be writtern in other boot modes. 0 = Disable 1 = Enable	0x00
1	rw	MEM_IAP_WEN	Flash IAP memory write enable. 0 = Disable 1 = Enable	0x00
0	rw	MEM_AP_WEN	Flash AP memory write enable. 0 = Disable 1 = Enable	0x00

1.13.6. MEM Flash memory protected key register

MEM_SKEY	MEM Flash memory protected key register		
Offset Address :	0x1C	Reset Value :	0x00000007

31	30	29	28	27	26	25	24
MEM_SKEY2[15:8]							
23	22	21	20	19	18	17	16
MEM_SKEY2[7:0]							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
MEM_SKEY[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	rw	MEM_SKEY2	Reserved for internal using	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	MEM_SKEY	MEM sequential key register for AP/IAP/ISPD flash. It uses for AP/IAP/ISPD flash memory program or erase operation. Write sequential value 0x46,0xB9 for single write or 0x46,0xBE for multiple write. Write any value, it will end the operation and enter protected condition for multiple write. For read access, the following independent bit define the related flash access sequential key locked status. The bit value definition is 0->Unlocked , 1->Locke. Bit-0 : AP/IAP/ISPD flash Bit-1 : ISP flash Bit-2 : OB flash	0x07

1.13.7. MEM Flash memory IAP size register

MEM_IAPSZ	MEM Flash memory IAP size register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
MEM_IAP_SIZE[15:8]							
7	6	5	4	3	2	1	0
MEM_IAP_SIZE[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	MEM_IAP_SIZE	IAP memory size select. Value 0 indicates the IAP memory size 0K-byte. The valid register bits are only bit 15-to-7 and bit 6-to-0 muse be 0. Value 0x0080 indicates the IAP memory size 512-byte. This register write access is no effect when MEM_IAP_AEN=0. (The default value is loaded from CFG OR after Warm reset.)	0x0000

1.13.8. MEM Register Map

MEM Register Map Register Number = 7

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	MEM_STA	Reserved								Reserved					Reserved	Reserved	MEM_IAPSEF	Reserved						Reserved	Reserved	Reserved	MEM_RPEF	MEM_WPEF	MEM_IAEF	Reserved	Reserved	MEM_EOPF	MEM_FBUSYF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	MEM_INT	Reserved						Reserved	Reserved	Reserved	MEM_RPE_RE	MEM_WPE_RE	MEM_IAE_RE	Reserved	Reserved			Reserved						Reserved	Reserved	Reserved	MEM_RPE_IE	MEM_WPE_IE	MEM_IAE_IE	Reserved	Reserved	MEM_EOP_IE	MEM_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	MEM_KEY	MEM_KEY2[15:0]																MEM_KEY[15:0]															
Reset	0x00010001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x10	MEM_CR0	Reserved								Reserved		MEM_IAP_AEN	MEM_HSP_EN	Reserved		MEM_BOOT_MS [1:0]		Reserved		MEM_FWAIT[1:0]		Reserved	Reserved	Reserved	Reserved	MEM_MDS[3:0]				Reserved	Reserved	MEM_HF_EN	MEM_EN
Reset	0x00200002	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0x14	MEM_CR1	Reserved																Reserved				Reserved	Reserved	MEM_ISP_REN	MEM_ISP_WEN	Reserved			MEM_IAP_EXEC	MEM_ISPD_REN	MEM_ISPD_WEN	MEM_IAP_WEN	MEM_AP_WEN
Reset	0x00000010	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0x1C	MEM_SKEY	MEM_SKEY2[15:0]																Reserved								MEM_SKEY[7:0]							
Reset	0x00000007	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0x28	MEM_IAPSZ	Reserved																MEM_IAP_SIZE [15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.14. Ext Memory Bus Registers

Ext Memory Bus	(EMB) External Memory Bus Controller
Base Address :	0x4D020000

1.14.1. EMB status register

EMB_STA	EMB status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				EMB_IAEF	EMB_WPEF	EMB_BWEF	EMB_BUSYF

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	EMB_IAEF	EMB bus access illegal address error detection flag. The flag is asserted when CPU access out of the EMB_ADR_SEL setting address in the EMB 2GB memory space. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
2	rw	EMB_WPEF	EMB bus write-protect error detect flag. This bit is set when write a write-protected address. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
1	rw	EMB_BWEF	EMB bus byte-write error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
0	r	EMB_BUSYF	EMB write/read access busy flag.	0x00

1.14.2. EMB interrupt enable register

EMB_INT	EMB interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				EMB_IAE_IE	EMB_WPE_IE	EMB_BWE_IE	EMB_IEA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	EMB_IAE_IE	EMB bus access illegal address error detection interrupt	0x00

			enable. 0 = Disable 1 = Enable	
2	rw	EMB_WPE_IE	EMB bus write-protect error detect interrupt enable. 0 = Disable 1 = Enable	0x00
1	rw	EMB_BWE_IE	EMB bus byte-write error detect interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	EMB_IEA	EMB controller interrupt all enable. When disables, the INT_EMB global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.14.3. EMB clock source register

EMB_CLK	EMB clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	EMB_CK_PSC[2:0]			Reserved			

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6..4	rw	EMB_CK_PSC	EMB output clock MCLK prescaler. The value range 0~7 is indicated divider 1~8.	0x00
3..0	-	Reserved	Reserved	0x00

1.14.4. EMB control register 0

EMB_CR0	EMB control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EMB_DMA_EN	Reserved			EMB_WE_CTL	EMB_OE_CTL	Reserved	EMB_ALE2_MDS
23	22	21	20	19	18	17	16
Reserved			Reserved	Reserved	Reserved	EMB_CE_MDS[1:0]	
15	14	13	12	11	10	9	8
Reserved	Reserved	EMB_ADR_SEL[1:0]		EMB_ADR_TWO	EMB_BUS_MDS	EMB_MAM1_EN	EMB_BUS_DSIZE
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved		Reserved	EMB_BW_EN	EMB_WEN	EMB_EN

Bit	Attr	Bit Name	Description	Reset
31	rw	EMB_DMA_EN	Direct memory access enable. 0 = Disable 1 = Enable	0x00
30..28	-	Reserved	Reserved	0x00
27	rw	EMB_WE_CTL	EMB MWE control timing select. 0x0 = TOGGLE : high-to-low change	0x00

			0x1 = LOW : drive low during write access	
26	rw	EMB_OE_CTL	EMB MOE control timing select. 0x0 = TOGGLE : high-to-low change 0x1 = LOW : drive low during read access	0x00
25	-	Reserved	Reserved	0x00
24	rw	EMB_ALE2_MDS	EMB MALE2 signal mode select. When EMB_MAM1_SEL=ALES, this register bit is no effect. 0x0 = ALE2 : 2nd phase address latch enable 0x1 = ALE : same as ALE timing	0x00
23..21	-	Reserved	Reserved	0x00
20	-	Reserved	Reserved	0x00
19	-	Reserved	Reserved	0x00
18	-	Reserved	Reserved	0x00
17..16	rw	EMB_CE_MDS	EMB MCE signal mode select. 0x0 = CE : chip enable signal 0x1 = ALE : same as ALE timing 0x2 = ALE2 : 2nd phase address latch enable 0x3 = Reserved	0x00
15	-	Reserved	Reserved	0x00
14	-	Reserved	Reserved	0x00
13..12	rw	EMB_ADR_SEL	EMB bus address range select. When selects 16bit and (1) EMB_BUS_DSIZE = 8-bit : the memory space is 64K-byte (2) EMB_BUS_DSIZE = 16-bit : the memory space is 128K-byte. Also that is the same for 24bit and 30bit. When EMB_MAM1_EN is enabled and EMB_BUS_DSIZE is 8-bit, this register selected address range is extended one bit from 16-bit/24-bit to 17-bit/25-bit but the 30-bit is kept the same 30-bit. 0x0 = 16bit :17bit if EMB_MAM1_EN is enabled 0x1 = 24bit :25bit if EMB_MAM1_EN is enabled 0x2 = 30bit 0x3 = Reserved	0x00
11	rw	EMB_ADR_TWO	EMB two address phase timing mode enable. When disables, it will be no address phase if EMB_BUS_MDS = Separated and one address phase if EMB_BUS_MDS = Multiplex. When enables, it will be two address phase and EMB_BUS_MDS must be Multiplex. 0 = Disable 1 = Enable	0x00
10	rw	EMB_BUS_MDS	EMB address and data bus mode select. 0 = Multiplex 1 = Separated	0x00
9	rw	EMB_MAM1_EN	EMB internal memory address A-1 signal output enable. The bit is only effective if EMB bus is 8-bit (EMD_BUS_DSIZE=0). When enables, the address LSB is MAM1 pin. When disables, the address LSB is MA0. 0 = Disable 1 = Enable	0x00
8	rw	EMB_BUS_DSIZE	EMB bus access data size. 0x0 = 8-bit 0x1 = 16-bit	0x00
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5..4	-	Reserved	Reserved	0x00
3	-	Reserved	Reserved	0x00
2	rw	EMB_BW_EN	EMB bus byte-write access enable bit. When EMB_WEN is enabled and EMB_BUS_DSIZE sets 16-bit, this bit is used to enable byte-write access function for 16-bit EMB data bus. 0 = Disable 1 = Enable	0x00

1	rw	EMB_WEN	EMB write access enable bit. 0 = Disable 1 = Enable	0x00
0	rw	EMB_EN	EMB controller enable bit. 0 = Disable 1 = Enable	0x00

1.14.5. EMB control register 1

EMB_CR1	EMB control register 1		
Offset Address :	0x14	Reset Value :	0x00000006

31	30	29	28	27	26	25	24
EMB_WE_MUX[1:0]		EMB_OE_MUX[1:0]		Reserved		EMB_BW1_SWO	EMB_BW1_SWEN
23	22	21	20	19	18	17	16
EMB_BW0_SWO	EMB_BW0_SWEN	EMB_ALE2_SWO	EMB_ALE2_SWEN	EMB_ALE_SWO	EMB_ALE_SWEN	EMB_CE_SWO	EMB_CE_SWEN
15	14	13	12	11	10	9	8
Reserved		EMB_MAM1_SEL[1:0]		Reserved	EMB_MAD_BSWAP	EMB_MAD_SWAP	EMB_MA_SWAP
7	6	5	4	3	2	1	0
Reserved			Reserved	EMB_CLK_INV	EMB_ALE2_INV	EMB_ALE_INV	EMB_CE_INV

Bit	Attr	Bit Name	Description	Reset
31..30	rw	EMB_WE_MUX	MWE output signal select. 0x0 = WE : EMB Write Enable signal 0x1 = TM10 : TM10_CKO 0x2 = TM16 : TM16_CKO 0x3 = TM20 : TM20_CKO	0x00
29..28	rw	EMB_OE_MUX	MOE output signal select. 0x0 = OE : EMB Output Enable signal 0x1 = TM10 : TM10_CKO 0x2 = TM16 : TM16_CKO 0x3 = TM20 : TM20_CKO	0x00
27..26	-	Reserved	Reserved	0x00
25	rw	EMB_BW1_SWO	EMB BW0 signal software control output data bit. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
24	rw	EMB_BW1_SWEN	EMB BW0 signal output software control enable bit. When disables, this signal is control by hardware. 0 = Disable 1 = Enable	0x00
23	rw	EMB_BW0_SWO	EMB BW0 signal software control output data bit. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
22	rw	EMB_BW0_SWEN	EMB BW0 signal output software control enable bit. When disables, this signal is control by hardware. 0 = Disable 1 = Enable	0x00
21	rw	EMB_ALE2_SWO	EMB MALE2 signal software control output data bit. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
20	rw	EMB_ALE2_SWEN	EMB MALE2 signal output software control enable bit. When disables, this signal is control by hardware. 0 = Disable 1 = Enable	0x00
19	rw	EMB_ALE_SWO	EMB MALE signal software control output data bit. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
18	rw	EMB_ALE_SWEN	EMB MALE signal output software control enable bit. When disables, this signal is control by hardware. 0 = Disable	0x00

			1 = Enable	
17	rw	EMB_CE_SWO	EMB MCE signal software control output data bit. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
16	rw	EMB_CE_SWEN	EMB MCE signal output software control enable bit. When disables, this signal is control by hardware. 0 = Disable 1 = Enable	0x00
15..14	-	Reserved	Reserved	0x00
13..12	rw	EMB_MAM1_SEL	EMB internal memory address A-1 signal output pin select. 0x0 = No : not output A-1 signal 0x1 = Reserved 0x2 = MBW1 0x3 = MALE2	0x00
11	-	Reserved	Reserved	0x00
10	rw	EMB_MAD_BSWAP	EMB MAD[15:8] and MAD[7:0] signals byte swap enable bit. 0 = Disable 1 = Enable	0x00
9	rw	EMB_MAD_SWAP	EMB MAD[15:0] signals Msb/Lsb swap enable bit. 0 = Disable 1 = Enable	0x00
8	rw	EMB_MA_SWAP	EMB MA[15:0] signals Msb/Lsb swap enable bit. 0 = Disable 1 = Enable	0x00
7..5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3	rw	EMB_CLK_INV	EMB MCLK clock output inverse enable bit. 0 = Disable 1 = Enable	0x00
2	rw	EMB_ALE2_INV	EMB MALE2 output inverse enable bit. The hardware active level is default logic high. 0 = Disable 1 = Enable	0x01
1	rw	EMB_ALE_INV	EMB MALE output inverse enable bit. The hardware active level is default logic high. 0 = Disable 1 = Enable	0x01
0	rw	EMB_CE_INV	EMB MCE output inverse enable bit. The hardware active level is default logic low. 0 = Disable 1 = Enable	0x00

1.14.6. EMB control register 2

EMB_CR2	EMB control register 2		
Offset Address :	0x18	Reset Value :	0x00100100

31	30	29	28	27	26	25	24
Reserved				Reserved		EMB_IDLE[1:0]	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved			EMB_ACCH	EMB_ACCW[3:0]			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved			EMB_ACCS	Reserved			EMB_ALEH
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	EMB_ALEW[2:0]			Reserved			EMB_ALES

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27..26	-	Reserved	Reserved	0x00
25..24	rw	EMB_IDLE	EMB SRAM/NOR bus idle time between two successive	0x00

			cycles. Value 0 indicates 0 MCLK clock time. Time = EMB_IDLE * MCLK	
23..21	-	**Reserved**	Reserved	0x00
20	rw	**EMB_ACCH**	EMB SRAM/NOR bus data write access hold time. When read access, the data hold time is fixed to 0 MCLK clock time. Value 0 indicates 0 MCLK clock time. Time = EMB_ACCH * MCLK	0x01
19..16	rw	**EMB_ACCW**	EMB SRAM/NOR bus data access time. Value 0 indicates 1 MCLK clock time. Time = (EMB_ACCW+1) * MCLK	0x00
15..13	-	**Reserved**	Reserved	0x00
12	rw	**EMB_ACCS**	EMB SRAM/NOR bus data access setup time. Value 0 indicates 0 MCLK clock time. Time = EMB_ACCS * MCLK	0x00
11..9	-	**Reserved**	Reserved	0x00
8	rw	**EMB_ALEH**	EMB SRAM/NOR bus ALE/ALE2 hold time. Value 0 indicates 0 MCLK clock time. Time = EMB_ALEH * MCLK	0x01
7	-	**Reserved**	Reserved	0x00
6..4	rw	**EMB_ALEW**	EMB SRAM/NOR bus ALE/ALE2 pulse width. Value 0 indicates 1 MCLK clock time. Pulse width = (EMB_ALEW+1) * MCLK	0x00
3..1	-	**Reserved**	Reserved	0x00
0	rw	**EMB_ALES**	EMB SRAM/NOR bus ALE/ALE2 setup time. Value 0 indicates 0 MCLK clock time. Time = EMB_ALES * MCLK	0x00

1.14.7. EMB Register Map

EMB Register Map Register Number = 6

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	EMB_STA	Reserved																Reserved								Reserved				EMB_IAEF	EMB_WPEF	EMB_BWEF	EMB_BUSYF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	EMB_INT	Reserved								Reserved								Reserved								Reserved				EMB_IAE_IE	EMB_WPE_IE	EMB_BWE_IE	EMB_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	EMB_CLK	Reserved																Reserved								Reserved	EMB_CK_PSC[2:0]			Reserved			
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	EMB_CR0	EMB_DMA_EN	Reserved			EMB_WE_CTL	EMB_OE_CTL	Reserved	EMB_ALE2_MDS	Reserved			Reserved	Reserved	Reserved	EMB_CE_MDS[1:0]		Reserved	Reserved	EMB_ADR_SEL [1:0]		EMB_ADR_TWO	EMB_BUS_MDS	EMB_MAM1_EN	EMB_BUS_DSIZE	Reserved	Reserved	Reserved		Reserved	EMB_BW_EN	EMB_WEN	EMB_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	EMB_CR1	EMB_WE_MUX[1:0]		EMB_OE_MUX[1:0]		Reserved		EMB_BW1_SWO	EMB_BW1_SWEN	EMB_BW0_SWO	EMB_BW0_SWEN	EMB_ALE2_SWO	EMB_ALE2_SWEN	EMB_ALE_SWO	EMB_ALE_SWEN	EMB_CE_SWO	EMB_CE_SWEN	Reserved		EMB_MAM1_SEL [1:0]		Reserved	EMB_MAD_BSWAP	EMB_MAD_SWAP	EMB_MA_SWAP	Reserved			Reserved	EMB_CLK_INV	EMB_ALE2_INV	EMB_ALE_INV	EMB_CE_INV
Reset	**0x00000006**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
0x18	EMB_CR2	Reserved				Reserved		EMB_IDLE[1:0]		Reserved			EMB_ACCH	EMB_ACCW[3:0]				Reserved			EMB_ACCS	Reserved			EMB_ALEH	Reserved	EMB_ALEW[2:0]			Reserved			EMB_ALES
Reset	**0x00100100**	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

1.15. Hardware Configure Registers

Hardware Configure	(CFG) Hardware Option Bytes Configure Control
Base Address :	0x4FF00000

1.15.1. CFG write protected Key register

CFG_KEY	CFG write protected Key register		
Offset Address :	0x0C	Reset Value :	0x00000001

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
CFG_KEY[15:8]							
7	6	5	4	3	2	1	0
CFG_KEY[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	CFG_KEY	CFG key register. Write value 0xA217 to unprotect the register write access. Write other value except 0xA217 to protect the registers except CFG_KEY registers. For read access : 0 = Unprotected 1 = Protected	0x0001

1.15.2. CFG option byte register 00

CFG_OR00	CFG option byte register 00		
Offset Address :	0x10	Reset Value :	0x00330001

31	30	29	28	27	26	25	24
Reserved					CFG_BOD2_WE	CFG_BOD1_WE	CFG_BOD0_WE
23	22	21	20	19	18	17	16
Reserved		Reserved		Reserved		CFG_BOD1_TH[1:0]	
15	14	13	12	11	10	9	8
Reserved							CFG_LOCK_DIS
7	6	5	4	3	2	1	0
Reserved	Reserved					CFG_BOOT_MS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..27	-	Reserved	Reserved	0x00
26	r	CFG_BOD2_WE	BOD2 trigger Warm reset enable. When enables, BOD1 will trigger a reset to CPU if the voltage threshold detect event happened. When Cold reset, this value is load to RST_BOD2_WE and PW_BOD2_EN. (This bit is loaded by inverting from option byte flash data.) 0 = Disable 1 = Enable	0x00
25	r	CFG_BOD1_WE	BOD1 trigger Warm reset enable. When enables, BOD1 will trigger a reset to CPU if the voltage threshold detect event happened. When Cold reset, this value is load to RST_BOD1_WE and PW_BOD1_EN. (This bit is loaded by inverting from option byte flash data.) 0 = Disable 1 = Enable	0x00
24	r	CFG_BOD0_WE	BOD0 trigger Warm reset enable. When enables, BOD0 will trigger a reset to CPU if the voltage threshold detect event happened. When Cold reset, this value is load to RST_BOD0_WE and PW_BOD0_EN. (This bit is loaded by	0x00

			inverting from option byte flash data.) 0 = Disable 1 = Enable	
23..22	-	Reserved	Reserved	0x00
21..20	-	Reserved	Reserved	0x03
19..18	-	Reserved	Reserved	0x00
17..16	r	CFG_BOD1_TH	BOD1 detect voltage threshold select. 0x0 = 2.0v 0x1 = 2.4v 0x2 = 3.7v 0x3 = 4.2v	0x03
15..9	-	Reserved	Reserved	0x00
8	r	CFG_LOCK_DIS	Main Flash code locked enable. When enables, code dump on ICP/SWD is always 0xFF, page-erase and program is also disabled. 0 = Enable 1 = Disable (Code dump on Writer is transparent)	0x00
7	-	Reserved	Reserved	0x00
6..2	-	Reserved	Reserved	0x00
1..0	r	CFG_BOOT_MS	System cold reset boot memory select and memory is mapped at 0x0000 0000. These bits are not load into MEM_BOOT_MS after Warm reset. (These bits are loaded by inverting from option byte flash data.) 0x0 = Application Flash 0x1 = Boot Flash 0x2 = Embedded SRAM 0x3 = Reserved	0x01

1.15.3. CFG option byte register 01

CFG_OR01	CFG option byte register 01		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
CFG_IAP_SIZE[15:8]							
7	6	5	4	3	2	1	0
CFG_IAP_SIZE[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	r	CFG_IAP_SIZE	IAP memory size select. Value 0 indicates the IAP memory size 0K-byte. The valid register bits are only bit 15-to-7 and bit 6-to-0 muse be 0. Value 0x0080 indicates the IAP memory size 512-byte. (These bits are loaded by inverting from option byte flash data.)	0x0000

1.15.4. CFG option byte register 02

CFG_OR02	CFG option byte register 02		
Offset Address :	0x18	Reset Value :	0x00000200

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8

CFG_ISP_SIZE[15:8]							
7	6	5	4	3	2	1	0
CFG_ISP_SIZE[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	r	CFG_ISP_SIZE	ISP memory size select. Value 0 indicates the ISP memory size 0K-byte. The valid register bits are only bit 15-to-7 and bit 6-to-0 muse be 0. Value 0x0080 indicates the ISP memory size 512-byte. (These bits are loaded by inverting from option byte flash data.)	0x0200

1.15.5. CFG option byte register 03

CFG_OR03	CFG option byte register 03		
Offset Address :	0x1C	Reset Value :	0x000000F0

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						CFG_IWDT_STP	CFG_IWDT_SLP
7	6	5	4	3	2	1	0
CFG_IWDT_DIV[3:0]				Reserved	CFG_IWDT_WE	CFG_IWDT_WP	CFG_IWDT_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..10	-	Reserved	Reserved	0x00
9	r	CFG_IWDT_STP	IWDT counting control when chip in STOP mode. Force ILRCO running for IWDT in STOP mode. (This bit is loaded by inverting from option byte flash data.) 0 = Stop : Stop counting 1 = Keep : Keep counting	0x00
8	r	CFG_IWDT_SLP	IWDT counting control when chip in SLEEP mode. (This bit is loaded by inverting from option byte flash data.) 0 = Stop : Stop counting 1 = Keep : Keep counting	0x00
7..4	r	CFG_IWDT_DIV	IWDT internal clock CK_IWDT_INT input divider select. When CFG_IWDT_EN is enabled, these bits will be loaded to IWDT control registers. When the value is 0xD, 0xE, 0xF, the divider is DIV4096 and the same as 0xC definition. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8 0x4 = DIV16 : divided by 16 0x5 = DIV32 : divided by 32 0x6 = DIV64 : divided by 64 0x7 = DIV128 : divided by 128 0x8 = DIV256 : divided by 256 0x9 = DIV512 : divided by 512 0xA = DIV1024 : divided by 1024 0xB = DIV2048 : divided by 2048 0xC = DIV4096 : divided by 4096	0x0F
3	-	Reserved	Reserved	0x00
2	r	CFG_IWDT_WE	IWDT reset generation enable option. (This bit is loaded by inverting from option byte flash data.) 0 = Disable 1 = Enable	0x00

1	r	CFG_IWDT_WP	IWDT registers write protected enable. When enables, the IWDT registers of wakeup enable, interrupt enable and status bits are always not protected. (This bit is loaded by inverting from option byte flash data.) 0 = Disable 1 = Enable : Write-protected	0x00
0	r	CFG_IWDT_EN	IWDT enable after Cold reset. (This bit is loaded by inverting from option byte flash data.) 0 = Disable 1 = Enable	0x00

1.15.6. CFG option byte register 05

CFG_OR05	CFG option byte register 05		
Offset Address :	0x24	Reset Value :	0x11E00100

31	30	29	28	27	26	25	24
CFG_XOSC_EN	Reserved	Reserved	Reserved	Reserved		Reserved	
23	22	21	20	19	18	17	16
Reserved		Reserved		Reserved		CFG_HS_SEL	Reserved
15	14	13	12	11	10	9	8
Reserved							Reserved
7	6	5	4	3	2	1	0
Reserved				CFG_PC_IOM	CFG_EXRST_SEL	CFG_SWD_PIN	CFG_EXRST_PIN

Bit	Attr	Bit Name	Description	Reset
31	r	CFG_XOSC_EN	XOSC crystal oscillation circuit enable. When enables, the related pins are forced to do as internal OSC input/output pins and overrides the AFS setting. (This bit is loaded by inverting from option byte flash data.) 0 = Disable 1 = Enable	0x00
30	-	Reserved	Reserved	0x00
29	-	Reserved	Reserved	0x00
28	-	Reserved	Reserved	0x01
27..26	-	Reserved	Reserved	0x00
25..24	-	Reserved	Reserved	0x01
23..22	-	Reserved	Reserved	0x03
21..20	-	Reserved	Reserved	0x02
19..18	-	Reserved	Reserved	0x00
17	r	CFG_HS_SEL	CK_HS clock source select after power-on (Cold reset). After Cold reset, the selected clock source will be enabled automatically. (These bits are loaded by inverting from option byte flash data.) 0 = IHRCO 1 = ILRCO	0x00
16	-	Reserved	Reserved	0x00
15..9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x01
7..4	-	Reserved	Reserved	0x00
3	r	CFG_PC_IOM	Port C default IO mode select after power-on . All the port-C PCn pins are default AIO mode or QB mode by this setting except PC4/5/6/13/14 pins. The IO modes of PC4/5/6 pins are always default QB mode. The IO modes of PC13/14 pins are directly control by chip if CFG_XOSC_EN is enabled. When CFG_XOSC_EN is disabled, the IO modes of PC13/14 pins are control by this register setting. (This bit is loaded by inverting from option byte flash data.) 0 = AIO : Analog IO 1 = QB : Quasi-Bidirectional output drive high one CLK	0x00

2	r	CFG_EXRST_SEL	External reset power on default warm-reset or cold-reset select. When selets 'Warm', the external reset is power on default warm reset and it can be programmed to cold reset by RST_EX_CE. (This bit is loaded by inverting from option byte flash data.) 0 = Warm : Power-on warm reset 1 = Cold : Power-on cold reset	0x00
1	r	CFG_SWD_PIN	SWD interface pin control after power-on. When enables, the related pins are default forced to do as SWD interface pins and set as the AFS default setting after reset. (This bit is loaded by inverting from option byte flash data.) 0 = Enable 1 = Disable	0x00
0	r	CFG_EXRST_PIN	External reset pin control after power-on. When enables, the related pin is default forced to do as external reset pin and sets as the AFS default setting after reset. (This bit is loaded by inverting from option byte flash data.) 0 = Enable 1 = Disable	0x00

1.15.7. CFG option byte register 06

CFG_OR06	CFG option byte register 06		
Offset Address :	0x28	Reset Value :	0x000000BF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						Reserved	Reserved
7	6	5	4	3	2	1	0
CFG_UTR_EN	Reserved	CFG_UTR_INTV[1:0]		CFG_UTR_OFINE	CFG_UTR_RES[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	rw	CFG_UTR_EN	USB UTR function enable. 0 = Disable 1 = Enable	0x01
6	-	Reserved	Reserved	0x00
5..4	rw	CFG_UTR_INTV	USB UTR interval value select. 0x0 = 1ms 0x1 = 8ms 0x2 = 4ms 0x3 = 2ms	0x03
3	rw	CFG_UTR_OFINE	USB UTR HFOSC frequency trimming mode select. 0 = Normal : UTR use both rough and fine tune bit for frequency trimming. 1 = Fine : UTR only use fine tune bit for frequency trimming.	0x01
2..0	rw	CFG_UTR_RES	USB UTR resolution value. 0x0 = 32 : 0.267% 0x1 = 48 : 0.4% 0x2 = 20x : 0.167% 0x3 = 24x : 0.2% 0x4 = 12 : 0.1% 0x5 = 16 : 0.133% 0x6 = 20 : 0.167%	0x07

			0x7 = 24 : 0.2%	

1.15.8. CFG option byte register 16

CFG_OR16	CFG option byte register 16		
Offset Address :	0x48	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				CFG_TEMP_CAL1[11:8]			
23	22	21	20	19	18	17	16
CFG_TEMP_CAL1[7:0]							
15	14	13	12	11	10	9	8
Reserved				CFG_TEMP_CAL0[11:8]			
7	6	5	4	3	2	1	0
CFG_TEMP_CAL0[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27..16	rw	CFG_TEMP_CAL1	Temperature Sensor calibration value acquired at 60 degree-C. The default value is set by chip manufacture trimming process.	0x0000
15..12	-	Reserved	Reserved	0x00
11..0	rw	CFG_TEMP_CAL0	Temperature Sensor calibration value acquired at 25 degree-C. The default value is set by chip manufacture trimming process.	0x0000

1.15.9. CFG option byte register 17

CFG_OR17	CFG option byte register 17		
Offset Address :	0x4C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved			CFG_ADC_OFFT[4:0]				
23	22	21	20	19	18	17	16
Reserved			Reserved				
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					Reserved		

Bit	Attr	Bit Name	Description	Reset
31..29	-	Reserved	Reserved	0x00
28..24	rw	CFG_ADC_OFFT	ADC offset adjust bits. ADC output code is equal ADC conversion code minus this offset code. Value 0x00,0x01 to 0x0E,0x0F are adjusted offset -31LSB, -29LSB to -3LSB, -1LSB. Value 0x10,0x11 to0x1E, 0x1F are adjusted offset 1LSB, 3LSB to 29LSB, 31LSB.	0x00
23..21	-	Reserved	Reserved	0x00
20..16	-	Reserved	Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7..3	-	Reserved	Reserved	0x00
2..0	-	Reserved	Reserved	0x00

1.15.10. CFG Register Map

CFG Register Map Register Number = 9

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0C	CFG_KEY	Reserved																CFG_KEY[15:0]															
Reset	0x00000001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x10	CFG_OR00	Reserved					CFG_BOD2_WE	CFG_BOD1_WE	CFG_BOD0_WE	Reserved		Reserved		Reserved		CFG_BOD1_TH [1:0]		Reserved							CFG_LOCK_DIS	Reserved	Reserved					CFG_BOOT_MS [1:0]	
Reset	0x00330001	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x14	CFG_OR01	Reserved																CFG_IAP_SIZE [15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	CFG_OR02	Reserved																CFG_ISP_SIZE [15:0]															
Reset	0x00000200	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0x1C	CFG_OR03	Reserved																Reserved						CFG_IWDT_STP	CFG_IWDT_SLP	CFG_IWDT_DIV [3:0]				Reserved	CFG_IWDT_WE	CFG_IWDT_WP	CFG_IWDT_EN
Reset	0x000000F0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
0x24	CFG_OR05	CFG_XOSC_EN	Reserved	Reserved	Reserved	Reserved		Reserved		Reserved		Reserved		Reserved		CFG_HS_SEL	Reserved	Reserved							Reserved	Reserved				CFG_PC_IOM	CFG_EXRST_SEL	CFG_SWD_PIN	CFG_EXRST_PIN
Reset	0x11E00100	0	0	0	1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0x28	CFG_OR06	Reserved																Reserved						Reserved	Reserved	CFG_UTR_EN	Reserved	CFG_UTR_INTV [1:0]		CFG_UTR_OFINE	CFG_UTR_RES [2:0]		
Reset	0x000000BF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
0x48	CFG_OR16	Reserved				CFG_TEMP_CAL1 [11:0]												Reserved				CFG_TEMP_CAL0 [11:0]											
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x4C	CFG_OR17	Reserved			CFG_ADC_OFFT [4:0]					Reserved			Reserved					Reserved								Reserved					Reserved		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.16. EXIC Interrupt Registers

EXIC Interrupt	(EXIC) External Interrupt Controller
Base Address :	0x50000000

1.16.1. EXIC interrupt status register

EXIC_STA	EXIC interrupt status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						EXIC_PE_AF	EXIC_PE_OF
15	14	13	12	11	10	9	8
Reserved		EXIC_PD_AF	EXIC_PD_OF	Reserved		EXIC_PC_AF	EXIC_PC_OF
7	6	5	4	3	2	1	0
Reserved		EXIC_PB_AF	EXIC_PB_OF	Reserved		EXIC_PA_AF	EXIC_PA_OF

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..18	-	Reserved	Reserved	0x00
17	rw	EXIC_PE_AF	External interrupt PEx AND path interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
16	r	EXIC_PE_OF	External interrupt PEx OR path interrupt flag. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15..14	-	Reserved	Reserved	0x00
13	rw	EXIC_PD_AF	External interrupt PDx AND path interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
12	r	EXIC_PD_OF	External interrupt PDx OR path interrupt flag. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
11..10	-	Reserved	Reserved	0x00
9	rw	EXIC_PC_AF	External interrupt PCx AND path interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
8	r	EXIC_PC_OF	External interrupt PCx OR path interrupt flag. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	EXIC_PB_AF	External interrupt PBx AND path interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	r	EXIC_PB_OF	External interrupt PBx OR path interrupt flag. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	EXIC_PA_AF	External interrupt PAx AND path interrupt flag (set by hardware and clear by software writing 1) 0 = Normal (No event occurred)	0x00

			1 = Happened (Event happened)	
0	r	EXIC_PA_OF	External interrupt PAx OR path interrupt flag. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00

1.16.2. EXIC interrupt enable register

EXIC_INT	EXIC interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			EXIC_PE_IEA	EXIC_PD_IEA	EXIC_PC_IEA	EXIC_PB_IEA	EXIC_PA_IEA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7..5	-	Reserved	Reserved	0x00
4	rw	EXIC_PE_IEA	EXIC port PE external interrupt all enable. When disables, the EXIC port PE global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00
3	rw	EXIC_PD_IEA	EXIC port PD external interrupt all enable. When disables, the EXIC port PD global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00
2	rw	EXIC_PC_IEA	EXIC port PC external interrupt all enable. When disables, the EXIC port PC global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00
1	rw	EXIC_PB_IEA	EXIC port PB external interrupt all enable. When disables, the EXIC port PB global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00
0	rw	EXIC_PA_IEA	EXIC port PA external interrupt all enable. When disables, the EXIC port PA global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.16.3. EXIC control register 0

EXIC_CR0	EXIC control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved			EXIC_PE_AINV	EXIC_PD_AINV	EXIC_PC_AINV	EXIC_PB_AINV	EXIC_PA_AINV
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
EXIC_NMI_SEL	EXIC_NMI_MUX[4:0]					EXIC_EM_RXEV	EXIC_EM_NMI
7	6	5	4	3	2	1	0
Reserved						EXIC_NMI_SW	Reserved

Bit	Attr	Bit Name	Description	Reset
31..29	-	Reserved	Reserved	0x00
28	rw	EXIC_PE_AINV	External interrupt PEx AND path signal inverse enable bit. 0 = Disable 1 = Enable	0x00
27	rw	EXIC_PD_AINV	External interrupt PDx AND path signal inverse enable bit. 0 = Disable 1 = Enable	0x00
26	rw	EXIC_PC_AINV	External interrupt PCx AND path signal inverse enable bit. 0 = Disable 1 = Enable	0x00
25	rw	EXIC_PB_AINV	External interrupt PBx AND path signal inverse enable bit. 0 = Disable 1 = Enable	0x00
24	rw	EXIC_PA_AINV	External interrupt PAx AND path signal inverse enable bit. 0 = Disable 1 = Enable	0x00
23..16	-	Reserved	Reserved	0x00
15	rw	EXIC_NMI_SEL	NMI interrupt internal or external source select. When selects INT, the NMI interrupt source is selected from interrupt peripheral interrupt souce. 0 = EXT : external pin 1 = INT : internal interupt source	0x00
14..10	rw	EXIC_NMI_MUX	NMI interrupt internal source MUX selection. The register is used to select the NMI interrupt source from one of the peripheral interrupt.	0x00
9	rw	EXIC_EM_RXEV	Interrupt event mask control bit for RXEV. 0 = Disable (Mask) 1 = Enable	0x00
8	rw	EXIC_EM_NMI	Interrupt event mask control bit for NMI. 0 = Disable (Mask) 1 = Enable	0x00
7..2	-	Reserved	Reserved	0x00
1	rw	EXIC_NMI_SW	Software NMI trigger bit. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
0	-	Reserved	Reserved	0x00

1.16.4. EXIC PA input interrupt pending flag register

EXIC_PA_PF	EXIC PA input interrupt pending flag register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
EXIC_PA15_PF	EXIC_PA14_PF	EXIC_PA13_PF	EXIC_PA12_PF	EXIC_PA11_PF	EXIC_PA10_PF	EXIC_PA9_PF	EXIC_PA8_PF

7	6	5	4	3	2	1	0
EXIC_PA7_PF	EXIC_PA6_PF	EXIC_PA5_PF	EXIC_PA4_PF	EXIC_PA3_PF	EXIC_PA2_PF	EXIC_PA1_PF	EXIC_PA0_PF

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	EXIC_PA15_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
14	rw	EXIC_PA14_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
13	rw	EXIC_PA13_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
12	rw	EXIC_PA12_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
11	rw	EXIC_PA11_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
10	rw	EXIC_PA10_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
9	rw	EXIC_PA9_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
8	rw	EXIC_PA8_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
7	rw	EXIC_PA7_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
6	rw	EXIC_PA6_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
5	rw	EXIC_PA5_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
4	rw	EXIC_PA4_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
3	rw	EXIC_PA3_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
2	rw	EXIC_PA2_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
1	rw	EXIC_PA1_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
0	rw	EXIC_PA0_PF	EXIC pin input interrupt pending flag x for external input interrupt pin PAx. It set by hardware and software write 1 to clear the interrupt pending flag. ([x] is the related pin index = {0~15}) Read the interrupt pending bit x on related external input interrupt pin : 0 = Normal : No event occurred 1 = Happened : Event happened	0x00

1.16.5. EXIC PA Pad input trigger select register

EXIC_PA_TRGS	EXIC PA Pad input trigger select register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_PA15_TRGS[1:0]		EXIC_PA14_TRGS[1:0]		EXIC_PA13_TRGS[1:0]		EXIC_PA12_TRGS[1:0]	
23	22	21	20	19	18	17	16
EXIC_PA11_TRGS[1:0]		EXIC_PA10_TRGS[1:0]		EXIC_PA9_TRGS[1:0]		EXIC_PA8_TRGS[1:0]	
15	14	13	12	11	10	9	8
EXIC_PA7_TRGS[1:0]		EXIC_PA6_TRGS[1:0]		EXIC_PA5_TRGS[1:0]		EXIC_PA4_TRGS[1:0]	
7	6	5	4	3	2	1	0
EXIC_PA3_TRGS[1:0]		EXIC_PA2_TRGS[1:0]		EXIC_PA1_TRGS[1:0]		EXIC_PA0_TRGS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..30	rw	EXIC_PA15_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
29..28	rw	EXIC_PA14_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
27..26	rw	EXIC_PA13_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
25..24	rw	EXIC_PA12_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
23..22	rw	EXIC_PA11_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
21..20	rw	EXIC_PA10_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
19..18	rw	EXIC_PA9_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
17..16	rw	EXIC_PA8_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
15..14	rw	EXIC_PA7_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
13..12	rw	EXIC_PA6_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag	0x00

			0x1 = Level 0x2 = Edge 0x3 = Dual-edge	
11..10	rw	EXIC_PA5_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
9..8	rw	EXIC_PA4_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
7..6	rw	EXIC_PA3_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
5..4	rw	EXIC_PA2_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
3..2	rw	EXIC_PA1_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
1..0	rw	EXIC_PA0_TRGS	External interrupt pin edge/level trigger event select. When set 0 to disable external interrupt pending flag bit EXIC_PAn_PF to be update. Set the input signal inversion bit of PA_INVn to select low/high level or rising/falling edge. When PA_INVn=0, select low level for EXIC_PAn_TRGS=0x01 and falling edge for EXIC_PAn_TRGS=0x02. On STOP mode, this function is forced to 'Level' by hardware however any setting value. ([n] is the related pin index = {0~15}) 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00

1.16.6. EXIC PA AOI Mask register

EXIC_PA_MSK	EXIC PA AOI Mask register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_PA15_AM	EXIC_PA14_AM	EXIC_PA13_AM	EXIC_PA12_AM	EXIC_PA11_AM	EXIC_PA10_AM	EXIC_PA9_AM	EXIC_PA8_AM
23	22	21	20	19	18	17	16
EXIC_PA7_AM	EXIC_PA6_AM	EXIC_PA5_AM	EXIC_PA4_AM	EXIC_PA3_AM	EXIC_PA2_AM	EXIC_PA1_AM	EXIC_PA0_AM
15	14	13	12	11	10	9	8
EXIC_PA15_OM	EXIC_PA14_OM	EXIC_PA13_OM	EXIC_PA12_OM	EXIC_PA11_OM	EXIC_PA10_OM	EXIC_PA9_OM	EXIC_PA8_OM
7	6	5	4	3	2	1	0
EXIC_PA7_OM	EXIC_PA6_OM	EXIC_PA5_OM	EXIC_PA4_OM	EXIC_PA3_OM	EXIC_PA2_OM	EXIC_PA1_OM	EXIC_PA0_OM

Bit	Attr	Bit Name	Description	Reset
31	rw	EXIC_PA15_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
30	rw	EXIC_PA14_AM	Refer to the register descriptions of EXIC_PA0_AM.	0x00

			0 = Disable (Mask) 1 = Enable	
29	rw	**EXIC_PA13_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
28	rw	**EXIC_PA12_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
27	rw	**EXIC_PA11_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
26	rw	**EXIC_PA10_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
25	rw	**EXIC_PA9_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
24	rw	**EXIC_PA8_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
23	rw	**EXIC_PA7_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
22	rw	**EXIC_PA6_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
21	rw	**EXIC_PA5_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
20	rw	**EXIC_PA4_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
19	rw	**EXIC_PA3_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
18	rw	**EXIC_PA2_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
17	rw	**EXIC_PA1_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
16	rw	**EXIC_PA0_AM**	External interrupt PAx AND mask bit x. Each bit is used to disable (mask) or enable the related PAx input line. ([x] is the related pin index = {0~15}) 0 = Disable (Mask) 1 = Enable	0x00
15	rw	**EXIC_PA15_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
14	rw	**EXIC_PA14_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
13	rw	**EXIC_PA13_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
12	rw	**EXIC_PA12_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
11	rw	**EXIC_PA11_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00

10	rw	EXIC_PA10_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
9	rw	EXIC_PA9_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
8	rw	EXIC_PA8_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
7	rw	EXIC_PA7_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
6	rw	EXIC_PA6_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
5	rw	EXIC_PA5_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
4	rw	EXIC_PA4_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
3	rw	EXIC_PA3_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
2	rw	EXIC_PA2_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
1	rw	EXIC_PA1_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
0	rw	EXIC_PA0_OM	External interrupt PAx OR mask bit x. Each bit is used to disable (mask) or enable the related PAx input line. ([x] is the related pin index = {0~15}) 0 = Disable (Mask) 1 = Enable	0x00

1.16.7. EXIC PB input interrupt pending flag register

EXIC_PB_PF	EXIC PB input interrupt pending flag register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
EXIC_PB15_PF	EXIC_PB14_PF	EXIC_PB13_PF	EXIC_PB12_PF	EXIC_PB11_PF	EXIC_PB10_PF	EXIC_PB9_PF	EXIC_PB8_PF
7	6	5	4	3	2	1	0
EXIC_PB7_PF	EXIC_PB6_PF	EXIC_PB5_PF	EXIC_PB4_PF	EXIC_PB3_PF	EXIC_PB2_PF	EXIC_PB1_PF	EXIC_PB0_PF

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	EXIC_PB15_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
14	rw	EXIC_PB14_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
13	rw	EXIC_PB13_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred	0x00

			1 = Happened : Event happened	
12	rw	EXIC_PB12_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
11	rw	EXIC_PB11_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
10	rw	EXIC_PB10_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
9	rw	EXIC_PB9_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
8	rw	EXIC_PB8_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
7	rw	EXIC_PB7_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
6	rw	EXIC_PB6_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
5	rw	EXIC_PB5_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
4	rw	EXIC_PB4_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
3	rw	EXIC_PB3_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
2	rw	EXIC_PB2_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
1	rw	EXIC_PB1_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
0	rw	EXIC_PB0_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00

1.16.8. EXIC PB Pad input trigger select register

EXIC_PB_TRGS	EXIC PB Pad input trigger select register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_PB15_TRGS[1:0]		EXIC_PB14_TRGS[1:0]		EXIC_PB13_TRGS[1:0]		EXIC_PB12_TRGS[1:0]	
23	22	21	20	19	18	17	16
EXIC_PB11_TRGS[1:0]		EXIC_PB10_TRGS[1:0]		EXIC_PB9_TRGS[1:0]		EXIC_PB8_TRGS[1:0]	
15	14	13	12	11	10	9	8
EXIC_PB7_TRGS[1:0]		EXIC_PB6_TRGS[1:0]		EXIC_PB5_TRGS[1:0]		EXIC_PB4_TRGS[1:0]	
7	6	5	4	3	2	1	0
EXIC_PB3_TRGS[1:0]		EXIC_PB2_TRGS[1:0]		EXIC_PB1_TRGS[1:0]		EXIC_PB0_TRGS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..30	rw	EXIC_PB15_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge	0x00

			0x3 = Dual-edge	
29..28	rw	**EXIC_PB14_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
27..26	rw	**EXIC_PB13_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
25..24	rw	**EXIC_PB12_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
23..22	rw	**EXIC_PB11_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
21..20	rw	**EXIC_PB10_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
19..18	rw	**EXIC_PB9_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
17..16	rw	**EXIC_PB8_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
15..14	rw	**EXIC_PB7_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
13..12	rw	**EXIC_PB6_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
11..10	rw	**EXIC_PB5_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
9..8	rw	**EXIC_PB4_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
7..6	rw	**EXIC_PB3_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00

5..4	rw	EXIC_PB2_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
3..2	rw	EXIC_PB1_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
1..0	rw	EXIC_PB0_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00

1.16.9. EXIC PB AOI Mask register

EXIC_PB_MSK	EXIC PB AOI Mask register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_PB15_AM	EXIC_PB14_AM	EXIC_PB13_AM	EXIC_PB12_AM	EXIC_PB11_AM	EXIC_PB10_AM	EXIC_PB9_AM	EXIC_PB8_AM
23	22	21	20	19	18	17	16
EXIC_PB7_AM	EXIC_PB6_AM	EXIC_PB5_AM	EXIC_PB4_AM	EXIC_PB3_AM	EXIC_PB2_AM	EXIC_PB1_AM	EXIC_PB0_AM
15	14	13	12	11	10	9	8
EXIC_PB15_OM	EXIC_PB14_OM	EXIC_PB13_OM	EXIC_PB12_OM	EXIC_PB11_OM	EXIC_PB10_OM	EXIC_PB9_OM	EXIC_PB8_OM
7	6	5	4	3	2	1	0
EXIC_PB7_OM	EXIC_PB6_OM	EXIC_PB5_OM	EXIC_PB4_OM	EXIC_PB3_OM	EXIC_PB2_OM	EXIC_PB1_OM	EXIC_PB0_OM

Bit	Attr	Bit Name	Description	Reset
31	rw	EXIC_PB15_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
30	rw	EXIC_PB14_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
29	rw	EXIC_PB13_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
28	rw	EXIC_PB12_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
27	rw	EXIC_PB11_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
26	rw	EXIC_PB10_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
25	rw	EXIC_PB9_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
24	rw	EXIC_PB8_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
23	rw	EXIC_PB7_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
22	rw	EXIC_PB6_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask)	0x00

			1 = Enable	
21	rw	**EXIC_PB5_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
20	rw	**EXIC_PB4_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
19	rw	**EXIC_PB3_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
18	rw	**EXIC_PB2_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
17	rw	**EXIC_PB1_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
16	rw	**EXIC_PB0_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
15	rw	**EXIC_PB15_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
14	rw	**EXIC_PB14_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
13	rw	**EXIC_PB13_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
12	rw	**EXIC_PB12_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
11	rw	**EXIC_PB11_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
10	rw	**EXIC_PB10_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
9	rw	**EXIC_PB9_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
8	rw	**EXIC_PB8_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
7	rw	**EXIC_PB7_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
6	rw	**EXIC_PB6_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
5	rw	**EXIC_PB5_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
4	rw	**EXIC_PB4_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
3	rw	**EXIC_PB3_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
2	rw	**EXIC_PB2_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask)	0x00

			1 = Enable	
1	rw	EXIC_PB1_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
0	rw	EXIC_PB0_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00

1.16.10. EXIC PC input interrupt pending flag register

EXIC_PC_PF	EXIC PC input interrupt pending flag register		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	EXIC_PC14_PF	EXIC_PC13_PF	EXIC_PC12_PF	EXIC_PC11_PF	EXIC_PC10_PF	EXIC_PC9_PF	EXIC_PC8_PF
7	6	5	4	3	2	1	0
EXIC_PC7_PF	EXIC_PC6_PF	EXIC_PC5_PF	EXIC_PC4_PF	EXIC_PC3_PF	EXIC_PC2_PF	EXIC_PC1_PF	EXIC_PC0_PF

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	-	Reserved	Reserved	0x00
14	rw	EXIC_PC14_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
13	rw	EXIC_PC13_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
12	rw	EXIC_PC12_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
11	rw	EXIC_PC11_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
10	rw	EXIC_PC10_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
9	rw	EXIC_PC9_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
8	rw	EXIC_PC8_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
7	rw	EXIC_PC7_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
6	rw	EXIC_PC6_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
5	rw	EXIC_PC5_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
4	rw	EXIC_PC4_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
3	rw	EXIC_PC3_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred	0x00

			1 = Happened : Event happened	
2	rw	EXIC_PC2_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
1	rw	EXIC_PC1_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
0	rw	EXIC_PC0_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00

1.16.11. EXIC PC Pad input trigger select register

EXIC_PC_TRGS	EXIC PC Pad input trigger select register		
Offset Address :	0x44	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved		EXIC_PC14_TRGS[1:0]		EXIC_PC13_TRGS[1:0]		EXIC_PC12_TRGS[1:0]	
23	22	21	20	19	18	17	16
EXIC_PC11_TRGS[1:0]		EXIC_PC10_TRGS[1:0]		EXIC_PC9_TRGS[1:0]		EXIC_PC8_TRGS[1:0]	
15	14	13	12	11	10	9	8
EXIC_PC7_TRGS[1:0]		EXIC_PC6_TRGS[1:0]		EXIC_PC5_TRGS[1:0]		EXIC_PC4_TRGS[1:0]	
7	6	5	4	3	2	1	0
EXIC_PC3_TRGS[1:0]		EXIC_PC2_TRGS[1:0]		EXIC_PC1_TRGS[1:0]		EXIC_PC0_TRGS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..30	-	Reserved	Reserved	0x00
29..28	rw	EXIC_PC14_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
27..26	rw	EXIC_PC13_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
25..24	rw	EXIC_PC12_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
23..22	rw	EXIC_PC11_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
21..20	rw	EXIC_PC10_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
19..18	rw	EXIC_PC9_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
17..16	rw	EXIC_PC8_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level	0x00

			0x2 = Edge 0x3 = Dual-edge	
15..14	rw	EXIC_PC7_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
13..12	rw	EXIC_PC6_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
11..10	rw	EXIC_PC5_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
9..8	rw	EXIC_PC4_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
7..6	rw	EXIC_PC3_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
5..4	rw	EXIC_PC2_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
3..2	rw	EXIC_PC1_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
1..0	rw	EXIC_PC0_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00

1.16.12. EXIC PC AOI Mask register

EXIC_PC_MSK	EXIC PC AOI Mask register		
Offset Address :	0x48	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	EXIC_PC14_AM	EXIC_PC13_AM	EXIC_PC12_AM	EXIC_PC11_AM	EXIC_PC10_AM	EXIC_PC9_AM	EXIC_PC8_AM
23	22	21	20	19	18	17	16
EXIC_PC7_AM	EXIC_PC6_AM	EXIC_PC5_AM	EXIC_PC4_AM	EXIC_PC3_AM	EXIC_PC2_AM	EXIC_PC1_AM	EXIC_PC0_AM
15	14	13	12	11	10	9	8
Reserved	EXIC_PC14_OM	EXIC_PC13_OM	EXIC_PC12_OM	EXIC_PC11_OM	EXIC_PC10_OM	EXIC_PC9_OM	EXIC_PC8_OM
7	6	5	4	3	2	1	0
EXIC_PC7_OM	EXIC_PC6_OM	EXIC_PC5_OM	EXIC_PC4_OM	EXIC_PC3_OM	EXIC_PC2_OM	EXIC_PC1_OM	EXIC_PC0_OM

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	EXIC_PC14_AM	Refer to the register descriptions of EXIC_PA0_AM.	0x00

			0 = Disable (Mask) 1 = Enable	
29	rw	**EXIC_PC13_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
28	rw	**EXIC_PC12_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
27	rw	**EXIC_PC11_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
26	rw	**EXIC_PC10_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
25	rw	**EXIC_PC9_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
24	rw	**EXIC_PC8_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
23	rw	**EXIC_PC7_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
22	rw	**EXIC_PC6_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
21	rw	**EXIC_PC5_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
20	rw	**EXIC_PC4_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
19	rw	**EXIC_PC3_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
18	rw	**EXIC_PC2_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
17	rw	**EXIC_PC1_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
16	rw	**EXIC_PC0_AM**	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
15	-	**Reserved**	Reserved	0x00
14	rw	**EXIC_PC14_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
13	rw	**EXIC_PC13_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
12	rw	**EXIC_PC12_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
11	rw	**EXIC_PC11_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
10	rw	**EXIC_PC10_OM**	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00

9	rw	EXIC_PC9_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
8	rw	EXIC_PC8_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
7	rw	EXIC_PC7_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
6	rw	EXIC_PC6_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
5	rw	EXIC_PC5_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
4	rw	EXIC_PC4_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
3	rw	EXIC_PC3_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
2	rw	EXIC_PC2_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
1	rw	EXIC_PC1_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
0	rw	EXIC_PC0_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00

1.16.13. EXIC PD input interrupt pending flag register

EXIC_PD_PF	EXIC PD input interrupt pending flag register		
Offset Address :	0x50	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
EXIC_PD15_PF	EXIC_PD14_PF	EXIC_PD13_PF	EXIC_PD12_PF	EXIC_PD11_PF	EXIC_PD10_PF	EXIC_PD9_PF	EXIC_PD8_PF
7	6	5	4	3	2	1	0
EXIC_PD7_PF	EXIC_PD6_PF	EXIC_PD5_PF	EXIC_PD4_PF	EXIC_PD3_PF	EXIC_PD2_PF	EXIC_PD1_PF	EXIC_PD0_PF

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	EXIC_PD15_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
14	rw	EXIC_PD14_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
13	rw	EXIC_PD13_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
12	rw	EXIC_PD12_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
11	rw	EXIC_PD11_PF	Refer to the register descriptions of EXIC_PA0_PF.	0x00

			0 = Normal : No event occurred 1 = Happened : Event happened	
10	rw	EXIC_PD10_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
9	rw	EXIC_PD9_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
8	rw	EXIC_PD8_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
7	rw	EXIC_PD7_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
6	rw	EXIC_PD6_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
5	rw	EXIC_PD5_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
4	rw	EXIC_PD4_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
3	rw	EXIC_PD3_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
2	rw	EXIC_PD2_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
1	rw	EXIC_PD1_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
0	rw	EXIC_PD0_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00

1.16.14. EXIC PD Pad input trigger select register

EXIC_PD_TRGS	EXIC PD Pad input trigger select register		
Offset Address :	0x54	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_PD15_TRGS[1:0]		EXIC_PD14_TRGS[1:0]		EXIC_PD13_TRGS[1:0]		EXIC_PD12_TRGS[1:0]	
23	22	21	20	19	18	17	16
EXIC_PD11_TRGS[1:0]		EXIC_PD10_TRGS[1:0]		EXIC_PD9_TRGS[1:0]		EXIC_PD8_TRGS[1:0]	
15	14	13	12	11	10	9	8
EXIC_PD7_TRGS[1:0]		EXIC_PD6_TRGS[1:0]		EXIC_PD5_TRGS[1:0]		EXIC_PD4_TRGS[1:0]	
7	6	5	4	3	2	1	0
EXIC_PD3_TRGS[1:0]		EXIC_PD2_TRGS[1:0]		EXIC_PD1_TRGS[1:0]		EXIC_PD0_TRGS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..30	rw	EXIC_PD15_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
29..28	rw	EXIC_PD14_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge	0x00

			0x3 = Dual-edge	
27..26	rw	**EXIC_PD13_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
25..24	rw	**EXIC_PD12_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
23..22	rw	**EXIC_PD11_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
21..20	rw	**EXIC_PD10_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
19..18	rw	**EXIC_PD9_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
17..16	rw	**EXIC_PD8_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
15..14	rw	**EXIC_PD7_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
13..12	rw	**EXIC_PD6_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
11..10	rw	**EXIC_PD5_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
9..8	rw	**EXIC_PD4_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
7..6	rw	**EXIC_PD3_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
5..4	rw	**EXIC_PD2_TRGS**	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00

3..2	rw	EXIC_PD1_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
1..0	rw	EXIC_PD0_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No updated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00

1.16.15. EXIC PD AOI Mask register

EXIC_PD_MSK	EXIC PD AOI Mask register		
Offset Address :	0x58	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_PD15_AM	EXIC_PD14_AM	EXIC_PD13_AM	EXIC_PD12_AM	EXIC_PD11_AM	EXIC_PD10_AM	EXIC_PD9_AM	EXIC_PD8_AM
23	22	21	20	19	18	17	16
EXIC_PD7_AM	EXIC_PD6_AM	EXIC_PD5_AM	EXIC_PD4_AM	EXIC_PD3_AM	EXIC_PD2_AM	EXIC_PD1_AM	EXIC_PD0_AM
15	14	13	12	11	10	9	8
EXIC_PD15_OM	EXIC_PD14_OM	EXIC_PD13_OM	EXIC_PD12_OM	EXIC_PD11_OM	EXIC_PD10_OM	EXIC_PD9_OM	EXIC_PD8_OM
7	6	5	4	3	2	1	0
EXIC_PD7_OM	EXIC_PD6_OM	EXIC_PD5_OM	EXIC_PD4_OM	EXIC_PD3_OM	EXIC_PD2_OM	EXIC_PD1_OM	EXIC_PD0_OM

Bit	Attr	Bit Name	Description	Reset
31	rw	EXIC_PD15_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
30	rw	EXIC_PD14_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
29	rw	EXIC_PD13_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
28	rw	EXIC_PD12_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
27	rw	EXIC_PD11_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
26	rw	EXIC_PD10_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
25	rw	EXIC_PD9_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
24	rw	EXIC_PD8_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
23	rw	EXIC_PD7_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
22	rw	EXIC_PD6_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
21	rw	EXIC_PD5_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
20	rw	EXIC_PD4_AM	Refer to the register descriptions of EXIC_PA0_AM.	0x00

			0 = Disable (Mask) 1 = Enable	
19	rw	EXIC_PD3_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
18	rw	EXIC_PD2_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
17	rw	EXIC_PD1_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
16	rw	EXIC_PD0_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
15	rw	EXIC_PD15_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
14	rw	EXIC_PD14_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
13	rw	EXIC_PD13_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
12	rw	EXIC_PD12_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
11	rw	EXIC_PD11_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
10	rw	EXIC_PD10_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
9	rw	EXIC_PD9_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
8	rw	EXIC_PD8_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
7	rw	EXIC_PD7_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
6	rw	EXIC_PD6_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
5	rw	EXIC_PD5_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
4	rw	EXIC_PD4_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
3	rw	EXIC_PD3_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
2	rw	EXIC_PD2_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
1	rw	EXIC_PD1_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
0	rw	EXIC_PD0_OM	Refer to the register descriptions of EXIC_PA0_OM.	0x00

			0 = Disable (Mask) 1 = Enable	

1.16.16. EXIC Interrupt source identity register 0

EXIC_SRC0	EXIC Interrupt source identity register 0		
Offset Address :	0x60	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_ID3[7:0]							
23	22	21	20	19	18	17	16
EXIC_ID2[7:0]							
15	14	13	12	11	10	9	8
EXIC_ID1[7:0]							
7	6	5	4	3	2	1	0
EXIC_ID0[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	r	EXIC_ID3	Interrupt source-3 identity. 0x1 = EXINT0 (PA external interrupt) 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
23..16	r	EXIC_ID2	Interrupt source-2 identity. 0x1 = Reserved 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
15..8	r	EXIC_ID1	Interrupt source-1 identity. 0x1 = IWDT 0x2 = PW 0x4 = Reserved 0x8 = RTC 0x10 = CSC 0x20 = APB 0x40 = MEM 0x80 = EMB	0x00
7..0	r	EXIC_ID0	Interrupt source-0 identity. 0x1 = WWDT 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00

1.16.17. EXIC interrupt source identity register 1

EXIC_SRC1	EXIC interrupt source identity register 1		
Offset Address :	0x64	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_ID7[7:0]							
23	22	21	20	19	18	17	16
EXIC_ID6[7:0]							
15	14	13	12	11	10	9	8
EXIC_ID5[7:0]							
7	6	5	4	3	2	1	0
EXIC_ID4[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	r	EXIC_ID7	Interrupt source-7 identity. 0x1 = CMP	0x00

			0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	
23..16	r	EXIC_ID6	Interrupt source-6 identity. 0x1 = EXINT3 (PD external interrupt) 0x2 = EXINT4 (PE external interrupt) 0x4 = Reserved 0x8 = Reserved	0x00
15..8	r	EXIC_ID5	Interrupt source-5 identity. 0x1 = EXINT2 (PC external interrupt) 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
7..0	r	EXIC_ID4	Interrupt source-4 identity. 0x1 = EXINT1 (PB external interrupt) 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00

1.16.18. EXIC interrupt source identity register 2

EXIC_SRC2	EXIC interrupt source identity register 2		
Offset Address :	0x68	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_ID11[7:0]							
23	22	21	20	19	18	17	16
EXIC_ID10[7:0]							
15	14	13	12	11	10	9	8
EXIC_ID9[7:0]							
7	6	5	4	3	2	1	0
EXIC_ID8[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	r	EXIC_ID11	Interrupt source-11 identity. 0x1 = DAC 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
23..16	r	EXIC_ID10	Interrupt source-10 identity. 0x1 = ADC 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
15..8	r	EXIC_ID9	Interrupt source-9 identity. 0x1 = Reserved 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
7..0	r	EXIC_ID8	Interrupt source-8 identity. 0x1 = DMA 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00

1.16.19. EXIC interrupt source identity register 3

EXIC_SRC3	EXIC interrupt source identity register 3		
Offset Address :	0x6C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_ID15[7:0]							
23	22	21	20	19	18	17	16
EXIC_ID14[7:0]							
15	14	13	12	11	10	9	8
EXIC_ID13[7:0]							
7	6	5	4	3	2	1	0
EXIC_ID12[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	r	EXIC_ID15	Interrupt source-15 identity. 0x1 = TM20 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
23..16	r	EXIC_ID14	Interrupt source-14 identity. 0x1 = Reserved 0x2 = Reserved 0x4 = TM16 0x8 = Reserved	0x00
15..8	r	EXIC_ID13	Interrupt source-13 identity. 0x1 = TM10 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
7..0	r	EXIC_ID12	Interrupt source-12 identity. 0x1 = TM00 0x2 = TM01 0x4 = Reserved 0x8 = Reserved	0x00

1.16.20. EXIC interrupt source identity register 4

EXIC_SRC4	EXIC interrupt source identity register 4		
Offset Address :	0x70	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_ID19[7:0]							
23	22	21	20	19	18	17	16
EXIC_ID18[7:0]							
15	14	13	12	11	10	9	8
EXIC_ID17[7:0]							
7	6	5	4	3	2	1	0
EXIC_ID16[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	r	EXIC_ID19	Interrupt source-19 identity. 0x1 = Reserved 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
23..16	r	EXIC_ID18	Interrupt source-18 identity. 0x1 = Reserved 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
15..8	r	EXIC_ID17	Interrupt source-17 identity. 0x1 = Reserved 0x2 = Reserved 0x4 = TM36	0x00

			0x8 = Reserved	
7..0	r	EXIC_ID16	Interrupt source-16 identity. 0x1 = Reserved 0x2 = Reserved 0x4 = TM26 0x8 = Reserved	0x00

1.16.21. EXIC interrupt source identity register 5

EXIC_SRC5	EXIC interrupt source identity register 5		
Offset Address :	0x74	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_ID23[7:0]							
23	22	21	20	19	18	17	16
EXIC_ID22[7:0]							
15	14	13	12	11	10	9	8
EXIC_ID21[7:0]							
7	6	5	4	3	2	1	0
EXIC_ID20[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	r	EXIC_ID23	Interrupt source-23 identity. 0x1 = Reserved 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
23..16	r	EXIC_ID22	Interrupt source-22 identity. 0x1 = URT4 0x2 = URT5 0x4 = URT6 0x8 = URT7	0x00
15..8	r	EXIC_ID21	Interrupt source-21 identity. 0x1 = URT1 0x2 = URT2 0x4 = Reserved 0x8 = Reserved	0x00
7..0	r	EXIC_ID20	Interrupt source-20 identity. 0x1 = URT0 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00

1.16.22. EXIC interrupt source identity register 6

EXIC_SRC6	EXIC interrupt source identity register 6		
Offset Address :	0x78	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_ID27[7:0]							
23	22	21	20	19	18	17	16
EXIC_ID26[7:0]							
15	14	13	12	11	10	9	8
EXIC_ID25[7:0]							
7	6	5	4	3	2	1	0
EXIC_ID24[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	r	EXIC_ID27	Interrupt source-27 identity. 0x1 = Reserved	0x00

			0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	
23..16	r	EXIC_ID26	Interrupt source-26 identity. 0x1 = Reserved 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
15..8	r	EXIC_ID25	Interrupt source-25 identity. 0x1 = Reserved 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
7..0	r	EXIC_ID24	Interrupt source-24 identity. 0x1 = SPI0 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00

1.16.23. EXIC interrupt source identity register 7

EXIC_SRC7	EXIC interrupt source identity register 7		
Offset Address :	0x7C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_ID31[7:0]							
23	22	21	20	19	18	17	16
EXIC_ID30[7:0]							
15	14	13	12	11	10	9	8
EXIC_ID29[7:0]							
7	6	5	4	3	2	1	0
EXIC_ID28[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	r	EXIC_ID31	Interrupt source-31 identity. 0x1 = APX 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
23..16	r	EXIC_ID30	Interrupt source-30 identity. 0x1 = USB 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
15..8	r	EXIC_ID29	Interrupt source-29 identity. 0x1 = I2C1 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00
7..0	r	EXIC_ID28	Interrupt source-28 identity. 0x1 = I2C0 0x2 = Reserved 0x4 = Reserved 0x8 = Reserved	0x00

1.16.24. EXIC PE input interrupt pending flag register

EXIC_PE_PF	EXIC PE input interrupt pending flag register		
Offset Address :	0x80	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
EXIC_PE15_PF	EXIC_PE14_PF	EXIC_PE13_PF	EXIC_PE12_PF	EXIC_PE11_PF	EXIC_PE10_PF	EXIC_PE9_PF	EXIC_PE8_PF
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	EXIC_PE3_PF	EXIC_PE2_PF	EXIC_PE1_PF	EXIC_PE0_PF

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	EXIC_PE15_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
14	rw	EXIC_PE14_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
13	rw	EXIC_PE13_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
12	rw	EXIC_PE12_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
11	rw	EXIC_PE11_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
10	rw	EXIC_PE10_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
9	rw	EXIC_PE9_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
8	rw	EXIC_PE8_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3	rw	EXIC_PE3_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
2	rw	EXIC_PE2_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
1	rw	EXIC_PE1_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00
0	rw	EXIC_PE0_PF	Refer to the register descriptions of EXIC_PA0_PF. 0 = Normal : No event occurred 1 = Happened : Event happened	0x00

1.16.25. EXIC PE Pad input trigger select register

EXIC_PE_TRGS	EXIC PE Pad input trigger select register		
Offset Address :	0x84	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_PE15_TRGS[1:0]		EXIC_PE14_TRGS[1:0]		EXIC_PE13_TRGS[1:0]		EXIC_PE12_TRGS[1:0]	
23	22	21	20	19	18	17	16

EXIC_PE11_TRGS[1:0]		EXIC_PE10_TRGS[1:0]		EXIC_PE9_TRGS[1:0]		EXIC_PE8_TRGS[1:0]	
15	14	13	12	11	10	9	8
Reserved		Reserved		Reserved		Reserved	
7	6	5	4	3	2	1	0
EXIC_PE3_TRGS[1:0]		EXIC_PE2_TRGS[1:0]		EXIC_PE1_TRGS[1:0]		EXIC_PE0_TRGS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..30	rw	EXIC_PE15_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No uPEated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
29..28	rw	EXIC_PE14_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No uPEated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
27..26	rw	EXIC_PE13_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No uPEated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
25..24	rw	EXIC_PE12_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No uPEated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
23..22	rw	EXIC_PE11_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No uPEated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
21..20	rw	EXIC_PE10_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No uPEated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
19..18	rw	EXIC_PE9_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No uPEated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
17..16	rw	EXIC_PE8_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No uPEated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
15..14	-	Reserved	Reserved	0x00
13..12	-	Reserved	Reserved	0x00
11..10	-	Reserved	Reserved	0x00
9..8	-	Reserved	Reserved	0x00
7..6	rw	EXIC_PE3_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No uPEated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
5..4	rw	EXIC_PE2_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No uPEated flag 0x1 = Level 0x2 = Edge	0x00

			0x3 = Dual-edge	
3..2	rw	EXIC_PE1_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No uPEated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00
1..0	rw	EXIC_PE0_TRGS	Refer to the register descriptions of EXIC_PA0_TRGS. 0x0 = No : No uPEated flag 0x1 = Level 0x2 = Edge 0x3 = Dual-edge	0x00

1.16.26. EXIC PE AOI Mask register

EXIC_PE_MSK	EXIC PE AOI Mask register		
Offset Address :	0x88	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
EXIC_PE15_AM	EXIC_PE14_AM	EXIC_PE13_AM	EXIC_PE12_AM	EXIC_PE11_AM	EXIC_PE10_AM	EXIC_PE9_AM	EXIC_PE8_AM
23	22	21	20	19	18	17	16
Reserved	Reserved	Reserved	Reserved	EXIC_PE3_AM	EXIC_PE2_AM	EXIC_PE1_AM	EXIC_PE0_AM
15	14	13	12	11	10	9	8
EXIC_PE15_OM	EXIC_PE14_OM	EXIC_PE13_OM	EXIC_PE12_OM	EXIC_PE11_OM	EXIC_PE10_OM	EXIC_PE9_OM	EXIC_PE8_OM
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	EXIC_PE3_OM	EXIC_PE2_OM	EXIC_PE1_OM	EXIC_PE0_OM

Bit	Attr	Bit Name	Description	Reset
31	rw	EXIC_PE15_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
30	rw	EXIC_PE14_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
29	rw	EXIC_PE13_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
28	rw	EXIC_PE12_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
27	rw	EXIC_PE11_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
26	rw	EXIC_PE10_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
25	rw	EXIC_PE9_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
24	rw	EXIC_PE8_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
23	-	Reserved	Reserved	0x00
22	-	Reserved	Reserved	0x00
21	-	Reserved	Reserved	0x00
20	-	Reserved	Reserved	0x00
19	rw	EXIC_PE3_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
18	rw	EXIC_PE2_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask)	0x00

			1 = Enable	
17	rw	EXIC_PE1_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
16	rw	EXIC_PE0_AM	Refer to the register descriptions of EXIC_PA0_AM. 0 = Disable (Mask) 1 = Enable	0x00
15	rw	EXIC_PE15_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
14	rw	EXIC_PE14_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
13	rw	EXIC_PE13_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
12	rw	EXIC_PE12_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
11	rw	EXIC_PE11_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
10	rw	EXIC_PE10_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
9	rw	EXIC_PE9_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
8	rw	EXIC_PE8_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3	rw	EXIC_PE3_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
2	rw	EXIC_PE2_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
1	rw	EXIC_PE1_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00
0	rw	EXIC_PE0_OM	Refer to the register descriptions of EXIC_PA0_OM. 0 = Disable (Mask) 1 = Enable	0x00

1.16.27. EXIC Register Map

EXIC Register Map Register Number = 26

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	EXIC_STA	Reserved								Reserved						EXIC_PE_AF	EXIC_PE_OF	Reserved		EXIC_PD_AF	EXIC_PD_OF	Reserved		EXIC_PC_AF	EXIC_PC_OF	Reserved		EXIC_PB_AF	EXIC_PB_OF	Reserved		EXIC_PA_AF	EXIC_PA_OF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	EXIC_INT	Reserved								Reserved								Reserved								Reserved			EXIC_PE_IEA	EXIC_PD_IEA	EXIC_PC_IEA	EXIC_PB_IEA	EXIC_PA_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	EXIC_CR0	Reserved			EXIC_PE_AINV	EXIC_PD_AINV	EXIC_PC_AINV	EXIC_PB_AINV	EXIC_PA_AINV	Reserved								EXIC_NMI_SEL	EXIC_NMI_MUX [4:0]					EXIC_EM_RXEV	EXIC_EM_NMI	Reserved						EXIC_NMI_SW	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	EXIC_PA_PF	Reserved																EXIC_PA15_PF	EXIC_PA14_PF	EXIC_PA13_PF	EXIC_PA12_PF	EXIC_PA11_PF	EXIC_PA10_PF	EXIC_PA9_PF	EXIC_PA8_PF	EXIC_PA7_PF	EXIC_PA6_PF	EXIC_PA5_PF	EXIC_PA4_PF	EXIC_PA3_PF	EXIC_PA2_PF	EXIC_PA1_PF	EXIC_PA0_PF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	EXIC_PA_TRGS	EXIC_PA15_TRGS [1:0]		EXIC_PA14_TRGS [1:0]		EXIC_PA13_TRGS [1:0]		EXIC_PA12_TRGS [1:0]		EXIC_PA11_TRGS [1:0]		EXIC_PA10_TRGS [1:0]		EXIC_PA9_TRGS [1:0]		EXIC_PA8_TRGS [1:0]		EXIC_PA7_TRGS [1:0]		EXIC_PA6_TRGS [1:0]		EXIC_PA5_TRGS [1:0]		EXIC_PA4_TRGS [1:0]		EXIC_PA3_TRGS [1:0]		EXIC_PA2_TRGS [1:0]		EXIC_PA1_TRGS [1:0]		EXIC_PA0_TRGS [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	EXIC_PA_MSK	EXIC_PA15_AM	EXIC_PA14_AM	EXIC_PA13_AM	EXIC_PA12_AM	EXIC_PA11_AM	EXIC_PA10_AM	EXIC_PA9_AM	EXIC_PA8_AM	EXIC_PA7_AM	EXIC_PA6_AM	EXIC_PA5_AM	EXIC_PA4_AM	EXIC_PA3_AM	EXIC_PA2_AM	EXIC_PA1_AM	EXIC_PA0_AM	EXIC_PA15_OM	EXIC_PA14_OM	EXIC_PA13_OM	EXIC_PA12_OM	EXIC_PA11_OM	EXIC_PA10_OM	EXIC_PA9_OM	EXIC_PA8_OM	EXIC_PA7_OM	EXIC_PA6_OM	EXIC_PA5_OM	EXIC_PA4_OM	EXIC_PA3_OM	EXIC_PA2_OM	EXIC_PA1_OM	EXIC_PA0_OM
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	EXIC_PB_PF	Reserved																EXIC_PB15_PF	EXIC_PB14_PF	EXIC_PB13_PF	EXIC_PB12_PF	EXIC_PB11_PF	EXIC_PB10_PF	EXIC_PB9_PF	EXIC_PB8_PF	EXIC_PB7_PF	EXIC_PB6_PF	EXIC_PB5_PF	EXIC_PB4_PF	EXIC_PB3_PF	EXIC_PB2_PF	EXIC_PB1_PF	EXIC_PB0_PF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	EXIC_PB_TRGS	EXIC_PB15_TRGS [1:0]		EXIC_PB14_TRGS [1:0]		EXIC_PB13_TRGS [1:0]		EXIC_PB12_TRGS [1:0]		EXIC_PB11_TRGS [1:0]		EXIC_PB10_TRGS [1:0]		EXIC_PB9_TRGS [1:0]		EXIC_PB8_TRGS [1:0]		EXIC_PB7_TRGS [1:0]		EXIC_PB6_TRGS [1:0]		EXIC_PB5_TRGS [1:0]		EXIC_PB4_TRGS [1:0]		EXIC_PB3_TRGS [1:0]		EXIC_PB2_TRGS [1:0]		EXIC_PB1_TRGS [1:0]		EXIC_PB0_TRGS [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x38	EXIC_PB_MSK	EXIC_PB15_AM	EXIC_PB14_AM	EXIC_PB13_AM	EXIC_PB12_AM	EXIC_PB11_AM	EXIC_PB10_AM	EXIC_PB9_AM	EXIC_PB8_AM	EXIC_PB7_AM	EXIC_PB6_AM	EXIC_PB5_AM	EXIC_PB4_AM	EXIC_PB3_AM	EXIC_PB2_AM	EXIC_PB1_AM	EXIC_PB0_AM	EXIC_PB15_OM	EXIC_PB14_OM	EXIC_PB13_OM	EXIC_PB12_OM	EXIC_PB11_OM	EXIC_PB10_OM	EXIC_PB9_OM	EXIC_PB8_OM	EXIC_PB7_OM	EXIC_PB6_OM	EXIC_PB5_OM	EXIC_PB4_OM	EXIC_PB3_OM	EXIC_PB2_OM	EXIC_PB1_OM	EXIC_PB0_OM
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	EXIC_PC_PF	Reserved																Reserved	EXIC_PC14_PF	EXIC_PC13_PF	EXIC_PC12_PF	EXIC_PC11_PF	EXIC_PC10_PF	EXIC_PC9_PF	EXIC_PC8_PF	EXIC_PC7_PF	EXIC_PC6_PF	EXIC_PC5_PF	EXIC_PC4_PF	EXIC_PC3_PF	EXIC_PC2_PF	EXIC_PC1_PF	EXIC_PC0_PF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x44	EXIC_PC_TRGS	Reserved		EXIC_PC14_TRGS [1:0]		EXIC_PC13_TRGS [1:0]		EXIC_PC12_TRGS [1:0]		EXIC_PC11_TRGS [1:0]		EXIC_PC10_TRGS [1:0]		EXIC_PC9_TRGS [1:0]		EXIC_PC8_TRGS [1:0]		EXIC_PC7_TRGS [1:0]		EXIC_PC6_TRGS [1:0]		EXIC_PC5_TRGS [1:0]		EXIC_PC4_TRGS [1:0]		EXIC_PC3_TRGS [1:0]		EXIC_PC2_TRGS [1:0]		EXIC_PC1_TRGS [1:0]		EXIC_PC0_TRGS [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x48	EXIC_PC_MSK	Reserved	EXIC_PC14_AM	EXIC_PC13_AM	EXIC_PC12_AM	EXIC_PC11_AM	EXIC_PC10_AM	EXIC_PC9_AM	EXIC_PC8_AM	EXIC_PC7_AM	EXIC_PC6_AM	EXIC_PC5_AM	EXIC_PC4_AM	EXIC_PC3_AM	EXIC_PC2_AM	EXIC_PC1_AM	EXIC_PC0_AM	Reserved	EXIC_PC14_OM	EXIC_PC13_OM	EXIC_PC12_OM	EXIC_PC11_OM	EXIC_PC10_OM	EXIC_PC9_OM	EXIC_PC8_OM	EXIC_PC7_OM	EXIC_PC6_OM	EXIC_PC5_OM	EXIC_PC4_OM	EXIC_PC3_OM	EXIC_PC2_OM	EXIC_PC1_OM	EXIC_PC0_OM
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	EXIC_PD_PF	Reserved																EXIC_PD15_PF	EXIC_PD14_PF	EXIC_PD13_PF	EXIC_PD12_PF	EXIC_PD11_PF	EXIC_PD10_PF	EXIC_PD9_PF	EXIC_PD8_PF	EXIC_PD7_PF	EXIC_PD6_PF	EXIC_PD5_PF	EXIC_PD4_PF	EXIC_PD3_PF	EXIC_PD2_PF	EXIC_PD1_PF	EXIC_PD0_PF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x54	EXIC_PD_TRGS	EXIC_PD15_TRGS [1:0]		EXIC_PD14_TRGS [1:0]		EXIC_PD13_TRGS [1:0]		EXIC_PD12_TRGS [1:0]		EXIC_PD11_TRGS [1:0]		EXIC_PD10_TRGS [1:0]		EXIC_PD9_TRGS [1:0]		EXIC_PD8_TRGS [1:0]		EXIC_PD7_TRGS [1:0]		EXIC_PD6_TRGS [1:0]		EXIC_PD5_TRGS [1:0]		EXIC_PD4_TRGS [1:0]		EXIC_PD3_TRGS [1:0]		EXIC_PD2_TRGS [1:0]		EXIC_PD1_TRGS [1:0]		EXIC_PD0_TRGS [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x58	EXIC_PD_MSK	EXIC_PD15_AM	EXIC_PD14_AM	EXIC_PD13_AM	EXIC_PD12_AM	EXIC_PD11_AM	EXIC_PD10_AM	EXIC_PD9_AM	EXIC_PD8_AM	EXIC_PD7_AM	EXIC_PD6_AM	EXIC_PD5_AM	EXIC_PD4_AM	EXIC_PD3_AM	EXIC_PD2_AM	EXIC_PD1_AM	EXIC_PD0_AM	EXIC_PD15_OM	EXIC_PD14_OM	EXIC_PD13_OM	EXIC_PD12_OM	EXIC_PD11_OM	EXIC_PD10_OM	EXIC_PD9_OM	EXIC_PD8_OM	EXIC_PD7_OM	EXIC_PD6_OM	EXIC_PD5_OM	EXIC_PD4_OM	EXIC_PD3_OM	EXIC_PD2_OM	EXIC_PD1_OM	EXIC_PD0_OM
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x60	EXIC_SRC0	EXIC_ID3[7:0]								EXIC_ID2[7:0]								EXIC_ID1[7:0]								EXIC_ID0[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x64	EXIC_SRC1	EXIC_ID7[7:0]								EXIC_ID6[7:0]								EXIC_ID5[7:0]								EXIC_ID4[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x68	EXIC_SRC2	EXIC_ID11[7:0]								EXIC_ID10[7:0]								EXIC_ID9[7:0]								EXIC_ID8[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x6C	EXIC_SRC3	EXIC_ID15[7:0]								EXIC_ID14[7:0]								EXIC_ID13[7:0]								EXIC_ID12[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x70	EXIC_SRC4	EXIC_ID19[7:0]								EXIC_ID18[7:0]								EXIC_ID17[7:0]								EXIC_ID16[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x74	EXIC_SRC5	EXIC_ID23[7:0]								EXIC_ID22[7:0]								EXIC_ID21[7:0]								EXIC_ID20[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x78	EXIC_SRC6	EXIC_ID27[7:0]								EXIC_ID26[7:0]								EXIC_ID25[7:0]								EXIC_ID24[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x7C	EXIC_SRC7	EXIC_ID31[7:0]								EXIC_ID30[7:0]								EXIC_ID29[7:0]								EXIC_ID28[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x80	EXIC_PE_PF	Reserved																EXIC_PE15_PF	EXIC_PE14_PF	EXIC_PE13_PF	EXIC_PE12_PF	EXIC_PE11_PF	EXIC_PE10_PF	EXIC_PE9_PF	EXIC_PE8_PF	Reserved	Reserved	Reserved	Reserved	EXIC_PE3_PF	EXIC_PE2_PF	EXIC_PE1_PF	EXIC_PE0_PF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x84	EXIC_PE_TRGS	EXIC_PE15_TRGS [1:0]		EXIC_PE14_TRGS [1:0]		EXIC_PE13_TRGS [1:0]		EXIC_PE12_TRGS [1:0]		EXIC_PE11_TRGS [1:0]		EXIC_PE10_TRGS [1:0]		EXIC_PE9_TRGS [1:0]		EXIC_PE8_TRGS [1:0]		Reserved		Reserved		Reserved		Reserved		EXIC_PE3_TRGS [1:0]		EXIC_PE2_TRGS [1:0]		EXIC_PE1_TRGS [1:0]		EXIC_PE0_TRGS [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x88	EXIC_PE_MSK	EXIC_PE15_AM	EXIC_PE14_AM	EXIC_PE13_AM	EXIC_PE12_AM	EXIC_PE11_AM	EXIC_PE10_AM	EXIC_PE9_AM	EXIC_PE8_AM	Reserved	Reserved	Reserved	Reserved	EXIC_PE3_AM	EXIC_PE2_AM	EXIC_PE1_AM	EXIC_PE0_AM	EXIC_PE15_OM	EXIC_PE14_OM	EXIC_PE13_OM	EXIC_PE12_OM	EXIC_PE11_OM	EXIC_PE10_OM	EXIC_PE9_OM	EXIC_PE8_OM	Reserved	Reserved	Reserved	Reserved	EXIC_PE3_OM	EXIC_PE2_OM	EXIC_PE1_OM	EXIC_PE0_OM
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.17. I2C0 Control Registers

I2C0 Control	(I2C0) I2C Control Module-0
Base Address :	0x51000000

1.17.1. I2C0 status register

I2C0_STA	I2C0 status register		
Offset Address :	0x00	Reset Value :	0x00000080

31	30	29	28	27	26	25	24
Reserved							Reserved
23	22	21	20	19	18	17	16
I2C0_BERRF	I2C0_ALOSF	I2C0_NACKF	I2C0_TOVRF	I2C0_ROVRF	I2C0_TXRF	I2C0_STPSTRF	I2C0_TSCF
15	14	13	12	11	10	9	8
I2C0_RWF	I2C0_MSTF	I2C0_SLAF	I2C0_SADRF	I2C0_ERRCF	I2C0_CNTF	I2C0_STOPF	I2C0_RSTRF
7	6	5	4	3	2	1	0
I2C0_TXF	I2C0_RXF	I2C0_WUPF	I2C0_TMOUTF	I2C0_ERRF	I2C0_BUFF	I2C0_EVENTF	I2C0_BUSYF

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23	rw	I2C0_BERRF	I2C bus error flag for invalid Stop/Start state. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
22	rw	I2C0_ALOSF	I2C bus arbitration lost error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
21	rw	I2C0_NACKF	I2C Not Acknowledge received error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
20	rw	I2C0_TOVRF	I2C data buffer transmit underrun error flag. Under the conditions, slave mode enables data buffer mode and clock stretching is disabled. When the data buffer is underrun, this bit is set and interrupt is generated if I2C0_ERR_IE is enabled. Also, the I2C0_ERRF is set. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19	rw	I2C0_ROVRF	I2C data buffer receive overrun error flag. Under the conditions, slave mode enables data buffer mode and clock stretching is disabled. When the data buffer is overrun, this bit is set and interrupt is generated if I2C0_ERR_IE is enabled. Also, the I2C0_ERRF is set. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
18	rw	I2C0_TXRF	I2C transmit data register remained status. (set and clear by hardware) When occurs bus NACK error and I2C0_NACKF is asserted, this bit is used to check the data register content whether has remain data. The I2C master will STOP and firmware can calculate the corrected total transfer count by I2C0_ACNT. It is cleared in slave address matched state and updated after last byte NACK state. 0 = No data 1 = Remained data	0x00
17	rw	I2C0_STPSTRF	I2C Stop or Start detection flag. (set by hardware and clear	0x00

			by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	
16	rw	I2C0_TSCF	I2C shadow buffer transfer complete flag. (set by hardware and clear by hardware or software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	r	I2C0_RWF	I2C read or write transfer direction status. It always update at slave address read/write state. 0 = Write 1 = Read	0x00
14	r	I2C0_MSTF	I2C master mode detection status. It set by Start command and clear by Stop state.	0x00
13	r	I2C0_SLAF	I2C slave mode detection status. It set by Slave address matched condition and clear by Start/Stop conditions.	0x00
12	rw	I2C0_SADRF	I2C slave mode slave address matched flag. This flag is also asserted for master mode if transmit mode slave address unmatched or received mode slave address asserted. When wakeup from STOP mode by detection matched slave address, user needs to clear this bit to disable the clock stretching and releases clock signal for external master. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
11	rw	I2C0_ERRCF	I2C master mode NACK error flag and state control bit. (set by hardware and clear by software writing 1 or hardware auto clear during START/STOP state) This bit is asserted if occurs NACK during slave-address cycle or data cycle of receive access. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
10	rw	I2C0_CNTF	I2C buffer count I2C0_BUF_CNT empty status. (set by hardware and clear by software writing 1 or I2C0_BUF_CNT written) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
9	rw	I2C0_STOPF	I2C stop detection flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
8	rw	I2C0_RSTRF	I2C repeat start asserted flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
7	rw	I2C0_TXF	I2C Transmit data register empty. (set by hardware and clear by hardware or software writing 1) This bit is cleared when I2C_DAT is written or this flag set to 1 by software. The flag is set after I2C reset or Idle state. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x01
6	rw	I2C0_RXF	I2C Receive data register not empty. (set by hardware and clear by hardware or software writing 1) This bit is cleared when I2C0_DAT is read or this flag set to 1 by software. But it does not be cleared when I2C0_DAT is read by SWD debugging. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	rw	I2C0_WUPF	I2C wakeup from STOP mode flag. When hardware detect that the slave address is matched to I2C0_SADR (I2C0_SADR_EN=1) during STOP mode, this flag is	0x00

			asserted.(set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	
4	rw	I2C0_TMOUTF	I2C time-out detect flag. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	I2C0_ERRF	I2C error interrupt flag for invalid no ack, bus arbitration lost bus error or data overrun error. (set by hardware , clear by software setting 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	I2C0_BUFF	I2C buffer mode event flag. (set by hardware , clear by software setting 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	rw	I2C0_EVENTF	I2C status event interrupt Flag. For Byte mode, this bit must be cleared and hardware can process to next state (set by hardware , clear by software setting 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	r	I2C0_BUSYF	I2C busy flag. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Busy (Event happened)	0x00

1.17.2. I2C0 interrupt enable register

I2C0_INT	I2C0 interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
I2C0_SDAF	I2C0_SCLF	Reserved					Reserved
23	22	21	20	19	18	17	16
Reserved						I2C0_STPSTR_IE	Reserved
15	14	13	12	11	10	9	8
Reserved						Reserved	Reserved
7	6	5	4	3	2	1	0
Reserved	Reserved	I2C0_WUP_IE	I2C0_TMOUT_IE	I2C0_ERR_IE	I2C0_BUF_IE	I2C0_EVENT_IE	I2C0_IEA

Bit	Attr	Bit Name	Description	Reset
31	r	I2C0_SDAF	I2C SDA line status bit.	0x00
30	r	I2C0_SCLF	I2C SCL line status bit.	0x00
29..25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23..18	-	Reserved	Reserved	0x00
17	rw	I2C0_STPSTR_IE	I2C Stop or Start detection interrupt enable. 0 = Disable 1 = Enable	0x00
16	-	Reserved	Reserved	0x00
15..10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5	rw	I2C0_WUP_IE	I2C wakeup from STOP mode interrupt enable on slave address matched. 0 = Disable 1 = Enable	0x00
4	rw	I2C0_TMOUT_IE	I2C timeout error interrupt enable. 0 = Disable 1 = Enable	0x00

3	rw	I2C0_ERR_IE	I2C no ack error, bus arbitration lost, bus error or data overrun interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	I2C0_BUF_IE	I2C buffer mode event Interrupt enable. When enables, it will generate the interrupt if the flag of I2C0_RXF, I2C0_TXF, I2C0_RSTRF, I2C0_STOPF or I2C0_SADRF is set. 0 = Disable 1 = Enable	0x00
1	rw	I2C0_EVENT_IE	I2C status event interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	I2C0_IEA	I2C interrupt all enable. When disables, the I2C0 global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.17.3. I2C0 clock source register

I2C0_CLK	I2C0 clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved			I2C0_TMO_CKS	I2C0_CK_PSC[3:0]			
7	6	5	4	3	2	1	0
Reserved	I2C0_CK_DIV[2:0]			I2C0_CK_SEL[1:0]		Reserved	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..13	-	Reserved	Reserved	0x00
12	rw	I2C0_TMO_CKS	I2C timeout clock source select. 0 = CK_UT 1 = DIV64 (CK_I2C0_PSC divided by 64)	0x00
11..8	rw	I2C0_CK_PSC	I2C internal clock CK_I2C0_INT prescaler. The value range 1~15 is indicated divider 2~16.	0x00
7	-	Reserved	Reserved	0x00
6..4	rw	I2C0_CK_DIV	I2C internal clock CK_I2C0_INT input divider. [CK_I2C0_INT frequency = (I2C0_CK_PSC+1) * 2 ^(I2C0_CK_DIV)] 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8 0x4 = DIV16 : divided by 16 0x5 = DIV32 : divided by 32 0x6 = DIV64 : divided by 64 0x7 = DIV128 : divided by 128	0x00
3..2	rw	I2C0_CK_SEL	I2C internal clock CK_I2C0 source select. 0x0 = PROC : CK_I2C0_PR process clock from CSC 0x1 = Reserved 0x2 = TM00_TRGO 0x3 = Reserved	0x00
1..0	-	Reserved	Reserved	0x00

1.17.4. I2C0 slave mode slave address code register

I2C0_SAC	I2C0 slave mode slave address code register		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
I2C0_SA_CODE[6:0]							I2C0_SA_RW

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..1	r	I2C0_SA_CODE	I2C slave mode grabbed slave address code. When slave mode, I2C controller will grab the slave address code always.	0x00
0	r	I2C0_SA_RW	I2C slave mode grabbed read/write bit.	0x00

1.17.5. I2C0 control register 0

I2C0_CR0	I2C0 control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
I2C0_DMA_TXEN	I2C0_DMA_RXEN	Reserved					
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
I2C0_PDRV_SEL[1:0]		Reserved	I2C0_SCLS_DIS	I2C0_SFBD_EN	Reserved	Reserved	
7	6	5	4	3	2	1	0
I2C0_GC_EN	I2C0_BUF_EN	I2C0_MDS[1:0]		I2C0_NACK_EN	I2C0_SADR2_EN	I2C0_SADR_EN	I2C0_EN

Bit	Attr	Bit Name	Description	Reset
31	rw	I2C0_DMA_TXEN	Direct memory access enable to transmit. When enables, hardware can receive the data from DMA and transmit to output. 0 = Disable 1 = Enable	0x00
30	rw	I2C0_DMA_RXEN	Direct memory access enable to receive. When enables, hardware can receive the data from input and send to DMA. 0 = Disable 1 = Enable	0x00
29..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..14	rw	I2C0_PDRV_SEL	I2C pre-drive time select for both SCL and SDA by CK_I2C0 clock time. 0x0 = 0T (disable pre-drive) 0x1 = 1T 0x2 = 2T 0x3 = 3T	0x00
13	-	Reserved	Reserved	0x00
12	rw	I2C0_SCLS_DIS	I2C slave mode clock SCL stretching low control disable. This bit is only using for buffer mode. 0 = Enable 1 = Disable	0x00
11	rw	I2C0_SFBD_EN	I2C SDA first bit drive high enable when data transmitted. This bit is no effect and disabled when I2C0_PDRV_SEL=0. 0 = Disable 1 = Enable	0x00

Bit	Attr	Bit Name	Description	Reset
10	-	Reserved	Reserved	0x00
9..8	-	Reserved	Reserved	0x00
7	rw	I2C0_GC_EN	I2C general call address 0x00 recognized enable bit. 0 = Disable 1 = Enable	0x00
6	rw	I2C0_BUF_EN	I2C data buffer enable bit. When enables, the I2C is operation in Buffer mode and a shadow buffer is using for data flow control. The I2C0_RXF and I2C0_TXF register flags will use to indicate the data register receiving not-empty and transmission empty. When disables, the I2C is operation in Byte mode by event code control. 0 = Disable 1 = Enable	0x00
5..4	rw	I2C0_MDS	I2C operation mode select. The monitor mode is only support for Buffer mode. 0x0 = I2C : Single/Multi-Master/ Slave mode 0x1 = Monitor : Monitor-Slave mode 0x2 = Reserved 0x3 = Reserved	0x00
3	rw	I2C0_NACK_EN	I2C master transmit ignore receiving NACK enable for Buffer mode. When enables, the I2C will continuously transmit next data when receive a NACK bit for master transmission mode. 0 = Disable 1 = Enable	0x00
2	rw	I2C0_SADR2_EN	I2C slave mode 2nd slave address detect enable. When enables , the I2C slave address I2C0_SADR is not allowed to be updated. 0 = Disable 1 = Enable	0x00
1	rw	I2C0_SADR_EN	I2C slave mode main slave address detect enable. When enables , the I2C slave address I2C0_SADR is not allowed to be updated. 0 = Disable 1 = Enable	0x00
0	rw	I2C0_EN	I2C function enable bit. When disables, the I2C0_SCL and I2C0_SDA pin state are switched to data port state. 0 = Disable 1 = Enable	0x00

1.17.6. I2C0 control register 1

I2C0_CR1	I2C0 control register 1		
Offset Address :	0x14	Reset Value :	0x00000504

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved			I2C0_HT[4:0]				
7	6	5	4	3	2	1	0
Reserved			I2C0_LT[4:0]				

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..13	-	Reserved	Reserved	0x00
12..8	rw	I2C0_HT	I2C SCL high cycle time by CK_I2C0_INT clock time. It write setting value for master mode. (SCL High time = START hold time = STOP setup time)	0x05
7..5	-	Reserved	Reserved	0x00

4..0	rw	I2C0_LT	I2C SCL low cycle time by CK_I2C0_INT clock time. It write setting value for master mode. (SCL Low time = START setup time = Bus free time between STOP and START)	0x04

1.17.7. I2C0 control register 2

I2C0_CR2	I2C0 control register 2		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved					I2C0_PAA	I2C0_PSTO	I2C0_PSTA
23	22	21	20	19	18	17	16
Reserved					I2C0_ACNT[2:0]		
15	14	13	12	11	10	9	8
Reserved					I2C0_BUF_CNT[2:0]		
7	6	5	4	3	2	1	0
Reserved	I2C0_AA_LCK	I2C0_STO_LCK	I2C0_STA_LCK	I2C0_CMD_TC	I2C0_AA	I2C0_STO	I2C0_STA

Bit	Attr	Bit Name	Description	Reset
31..27	-	Reserved	Reserved	0x00
26	rw	I2C0_PAA	I2C preload bit for Acknowledge enable bit.	0x00
25	rw	I2C0_PSTO	I2C preload bit for STOP enable bit.	0x00
24	rw	I2C0_PSTA	I2C preload bit forSTART enable bit.	0x00
23..19	-	Reserved	Reserved	0x00
18..16	r	I2C0_ACNT	I2C transmitted or received data actual byte count value. When transmitted or received data complete by last data transfer or error conditions, the actual transmitted or received data byte number is recorded in this register. The count value is not calculated and included the NACK error byte. For other conditions, this register value is no meaning. 0x0 = 0-byte 0x1 = 1-byte 0x2 = 2-byte 0x3 = 3-byte 0x4 = 4-byte	0x00
15..11	-	Reserved	Reserved	0x00
10..8	rw	I2C0_BUF_CNT	I2C transmitted or received data byte count threshold. When transmitted or received data arrives at the threshold and the interrupt enable bit of I2C0_BUFF_IE is enabled, the interrupt is generated. When writes this register, hardware will auto clear the I2C0_CNTF. 0x0 = Reserved 0x1 = 1-byte 0x2 = 2-byte 0x3 = 3-byte 0x4 = 4-byte	0x00
7	-	Reserved	Reserved	0x00
6	rw	I2C0_AA_LCK	I2C0_AA and I2C0_PAA bits write access protected control. When selects locked, disables the register bit write access. I2C0_AA and I2C0_PAA are written effectively only by written 1 to this bit simultaneously. 0 = Locked 1 = un-Locked	0x00
5	rw	I2C0_STO_LCK	I2C0_STO and I2C0_PSTO bits write access protected control. When selects locked, disables the register bit write access.I2C0_STO and I2C0_PSTO are written effectively only by written 1 to this bit simultaneously. 0 = Locked 1 = un-Locked	0x00
4	rw	I2C0_STA_LCK	I2C0_STA and I2C0_PSTA bits write access protected control.	0x00

			When selects locked, disables the register bit write access. I2C0_STA and I2C0_PSTA are written effectively only by written 1 to this bit simultaneously. 0 = Locked 1 = un-Locked	
3	rw	I2C0_CMD_TC	I2C command preload enable control bit. When enables, it will write hold until I2C0_TCF set for I2C0_STA, I2C0_STO, I2C0_AA register bits. When disables, write these command bits that will directly execute the setting command. This bit is no effect if I2C0_BUF_EN=0. 0 = Disable 1 = Enable	0x00
2	rw	I2C0_AA	I2C assert Acknowledge enable bit. If the AA bit is set to '1', an ACK will be returned during the ACK clock pulse on the SCL line when: 1) The own slave address has been received. 2) A data byte has been received while I2C is in the master/receiver mode. 3) A data byte has been received while I2C is in the addressed slave/receiver mode. If the AA flag is reset to '0', a NACK will be returned during the ACK clock pulse on SCL when: 1) A data has been received while I2C is in the master/receiver mode. 2) A data byte has been received while I2C is in the addressed slave/receiver mode.	0x00
1	rw	I2C0_STO	I2C STOP enable bit. When the STO bit is set while I2C is in a master mode, a STOP condition is transmitted to the serial bus. When the STOP condition is detected on the bus, the I2C hardware clears the STO flag. In a slave mode, the STO flag may be set to recover from a bus error condition. In this case, no STOP condition is transmitted to the bus. However, the I2C hardware behaves as if a STOP condition has been received and switches to the defined not addressed slave receiver mode. The STO flag is automatically cleared by hardware. If the STA and STO bits are both set, then a STOP condition is transmitted to the bus if I2C is in a master mode (in a slave mode, I2C generates an internal STOP condition which is not transmitted), and then transmits a START condition.	0x00
0	rw	I2C0_STA	I2C START enable bit. When the STA bit is set to enter a master mode, the I2C hardware checks the status of the serial bus and generates a START condition if the bus is free. If the bus is not free, then I2C waits for a STOP condition and generates a START condition after a delay. If STA is set while I2C is already in a master mode and one or more bytes are transmitted or received, I2C transmits a repeated START condition. STA may be set at any time. STA may also be set when I2C is an addressed slave. When the STA bit is reset, no START condition or repeated START condition will be generated.	0x00

1.17.8. I2C0 slave address detect register

I2C0_SADR	I2C0 slave address detect register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							

15	14	13	12	11	10	9	8
I2C0_SADR2[6:0]							Reserved
7	6	5	4	3	2	1	0
I2C0_SADR[6:0]							Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..9	rw	I2C0_SADR2	I2C slave mode 2nd slave address detection request address value.	0x00
8	-	Reserved	Reserved	0x00
7..1	rw	I2C0_SADR	I2C slave mode main slave address detection request address value.	0x00
0	-	Reserved	Reserved	0x00

1.17.9. I2C0 timeout control register

I2C0_TMOUT	I2C0 timeout control register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
I2C0_TMO_CNT[7:0]							
7	6	5	4	3	2	1	0
Reserved				I2C0_TMO_MDS[1:0]		I2C0_TMO_CTL	I2C0_TMO_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	rw	I2C0_TMO_CNT	I2C timeout setting value.	0x00
7..4	-	Reserved	Reserved	0x00
3..2	rw	I2C0_TMO_MDS	I2C timeout detection mode select. When set value to 0x2, the timeout detection timer is able to use as a universal counter. 0x0 = SCL-low (SCL low timeout) 0x1 = SCL-SDA-high (both SCL and SDA high timeout for bus idle condition) 0x2 = General (general counter)	0x00
1	rw	I2C0_TMO_CTL	I2C timeout event happened I2C reset control enable bit. When enables, the I2C is reset and I2C0_EN is set to 0 if timeout is happened. 0 = Disable 1 = Enable	0x00
0	rw	I2C0_TMO_EN	I2C timeout detect enable. 0 = Disable 1 = Enable	0x00

1.17.10. I2C0 status register 2

I2C0_STA2	I2C0 status register 2		
Offset Address :	0x28	Reset Value :	0x000000F8

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							I2C0_EVENTF2
7	6	5	4	3	2	1	0

I2C0_EVENT[7:0]

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..9	-	Reserved	Reserved	0x00
8	rw	I2C0_EVENTF2	I2C status event interrupt Flag. This bit same as I2C_EVENTF (set by hardware , clear by software setting 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
7..0	r	I2C0_EVENT	I2C0 status event code	0xF8

1.17.11. I2C0 data shift buffer register

I2C0_SBUF	I2C0 data shift buffer register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
I2C0_SBUF[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	I2C0_SBUF	I2C data shift buffer register. Notify that read this register will get I2C0_DAT content in I2C Byte mode.	0x00

1.17.12. I2C0 data register

I2C0_DAT	I2C0 data register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
I2C0_DAT[31:24]							
23	22	21	20	19	18	17	16
I2C0_DAT[23:16]							
15	14	13	12	11	10	9	8
I2C0_DAT[15:8]							
7	6	5	4	3	2	1	0
I2C0_DAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	I2C0_DAT	I2C data byte register. When buffer mode is enabled, read this register will clear the I2C0_RXF and write this register will clear I2C0_TXF.	0x00000000

1.17.13. I2C0 slave address detect register

I2C0_MASK	I2C0 slave address detect register		
Offset Address :	0x34	Reset Value :	0x000000FE

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C0_SA_MSK[6:0]							Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..1	rw	I2C0_SA_MSK	I2C slave address I2C0_SADR mask register. Zero bit in this result is considered as 'don't care'. The mask register is no effect on I2C0_SADR2 register setting.	0x7F
0	-	Reserved	Reserved	0x00

1.17.14. I2C0 Register Map

I2C0 Register Map **Register Number = 13**

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	I2C0_STA	Reserved							Reserved	I2C0_BERRF	I2C0_ALOSF	I2C0_NACKF	I2C0_TOVRF	I2C0_ROVRF	I2C0_TXRF	I2C0_STPSTRF	I2C0_TSCF	I2C0_RWF	I2C0_MSTF	I2C0_SLAF	I2C0_SADRF	I2C0_ERRCF	I2C0_CNTF	I2C0_STOPF	I2C0_RSTRF	I2C0_TXF	I2C0_RXF	I2C0_WUPF	I2C0_TMOUTF	I2C0_ERRF	I2C0_BUFF	I2C0_EVENTF	I2C0_BUSYF
Reset	0x00000080	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0x04	I2C0_INT	I2C0_SDAF	I2C0_SCLF	Reserved					Reserved	Reserved						I2C0_STPSTR_IE	Reserved	Reserved						Reserved	Reserved	Reserved	Reserved	I2C0_WUP_IE	I2C0_TMOUT_IE	I2C0_ERR_IE	I2C0_BUF_IE	I2C0_EVENT_IE	I2C0_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	I2C0_CLK	Reserved																Reserved			I2C0_TMO_CKS	I2C0_CK_PSC [3:0]				Reserved	I2C0_CK_DIV [2:0]			I2C0_CK_SEL [1:0]		Reserved	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	I2C0_SAC	Reserved																Reserved								I2C0_SA_CODE [6:0]							I2C0_SA_RW
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	I2C0_CR0	I2C0_DMA_TXEN	I2C0_DMA_RXEN	Reserved						Reserved								I2C0_PDRV_SEL [1:0]		Reserved	I2C0_SCLS_DIS	I2C0_SFBD_EN	Reserved	Reserved		I2C0_GC_EN	I2C0_BUF_EN	I2C0_MDS[1:0]		I2C0_NACK_EN	I2C0_SADR2_EN	I2C0_SADR_EN	I2C0_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	I2C0_CR1	Reserved																Reserved			I2C0_HT[4:0]					Reserved			I2C0_LT[4:0]				
Reset	0x00000504	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0
0x18	I2C0_CR2	Reserved					I2C0_PAA	I2C0_PSTO	I2C0_PSTA	Reserved					I2C0_ACNT[2:0]			Reserved					I2C0_BUF_CNT [2:0]			Reserved	I2C0_AA_LCK	I2C0_STO_LCK	I2C0_STA_LCK	I2C0_CMD_TC	I2C0_AA	I2C0_STO	I2C0_STA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	I2C0_SADR	Reserved																I2C0_SADR2[6:0]							Reserved	I2C0_SADR[6:0]							Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x20	I2C0_TMOUT	Reserved																I2C0_TMO_CNT[7:0]								Reserved				I2C0_TMO_MDS[1:0]		I2C0_TMO_CTL	I2C0_TMO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	I2C0_STA2	Reserved																Reserved							I2C0_EVENTF2	I2C0_EVENT[7:0]							
Reset	0x000000F8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0
0x2C	I2C0_SBUF	Reserved																Reserved								I2C0_SBUF[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	I2C0_DAT	I2C0_DAT[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	I2C0_MASK	Reserved																Reserved								I2C0_SA_MSK[6:0]							Reserved
Reset	0x000000FE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0

1.18. I2C1 Control Registers

I2C1 Control	(I2C1) I2C Control Module-1
Base Address :	0x51010000

1.18.1. I2C1 status register

I2C1_STA	I2C1 status register		
Offset Address :	0x00	Reset Value :	0x00000080

31	30	29	28	27	26	25	24
Reserved							Reserved
23	22	21	20	19	18	17	16
I2C1_BERRF	I2C1_ALOSF	I2C1_NACKF	I2C1_TOVRF	I2C1_ROVRF	I2C1_TXRF	I2C1_STPSTRF	I2C1_TSCF
15	14	13	12	11	10	9	8
I2C1_RWF	I2C1_MSTF	I2C1_SLAF	I2C1_SADRF	I2C1_ERRCF	I2C1_CNTF	I2C1_STOPF	I2C1_RSTRF
7	6	5	4	3	2	1	0
I2C1_TXF	I2C1_RXF	I2C1_WUPF	I2C1_TMOUTF	I2C1_ERRF	I2C1_BUFF	I2C1_EVENTF	I2C1_BUSYF

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23	rw	I2C1_BERRF	I2C bus error flag for invalid Stop/Start state. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
22	rw	I2C1_ALOSF	I2C bus arbitration lost error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
21	rw	I2C1_NACKF	I2C Not Acknowledge received error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
20	rw	I2C1_TOVRF	I2C data buffer transmit underrun error flag. Under the conditions, slave mode enables data buffer mode and clock stretching is disabled. When the data buffer is underrun, this bit is set and interrupt is generated if I2C1_ERR_IE is enabled. Also, the I2C1_ERRF is set. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19	rw	I2C1_ROVRF	I2C data buffer receive overrun error flag. Under the conditions, slave mode enables data buffer mode and clock stretching is disabled. When the data buffer is overrun, this bit is set and interrupt is generated if I2C1_ERR_IE is enabled. Also, the I2C1_ERRF is set. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
18	rw	I2C1_TXRF	I2C transmit data register remained status. (set and clear by hardware) When occurs bus NACK error and I2C1_NACKF is asserted, this bit is used to check the data register content whether has remain data. The I2C master will STOP and firmware can calculate the corrected total transfer count by I2C1_ACNT. It is cleared in slave address matched state and updated after last byte NACK state. 0 = No data 1 = Remained data	0x00
17	rw	I2C1_STPSTRF	I2C Stop or Start detection flag. (set by hardware and clear by software writing 1)	0x00

			0 = Normal (No event occurred) 1 = Happened (Event happened)	
16	rw	**I2C1_TSCF**	I2C shadow buffer transfer complete flag. (set by hardware and clear by hardware or software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	r	**I2C1_RWF**	I2C read or write transfer direction status. It always update at slave address r/w state. 0 = Write 1 = Read	0x00
14	r	**I2C1_MSTF**	I2C master mode detection status. It set by Start command and clear by Stop state.	0x00
13	r	**I2C1_SLAF**	I2C slave mode detection status. It set by Slave address matched condition and clear by Start/Stop conditions.	0x00
12	rw	**I2C1_SADRF**	I2C slave mode slave address matched flag. This flag is also asserted for master mode if transmit mode slave address unmatched or received mode slave address asserted. When wakeup from STOP mode by detection matched slave address, user needs to clear this bit to disable the clock stretching and releases clock signal for external master. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
11	rw	**I2C1_ERRCF**	I2C master mode NACK error flag and state control bit. (set by hardware and clear by software writing 1 or hardware auto clear during START/STOP state) This bit is asserted if occurs NACK during slave-address cycle or data cycle of receive access. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
10	rw	**I2C1_CNTF**	I2C buffer count I2C1_BUF_CNT empty status. (set by hardware and clear by software writing 1 or I2C1_BUF_CNT written) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
9	rw	**I2C1_STOPF**	I2C stop detection flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
8	rw	**I2C1_RSTRF**	I2C repeat start asserted flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
7	rw	**I2C1_TXF**	I2C Transmit data register empty. (set by hardware and clear by hardware or software writing 1) This bit is cleared when I2C1_DAT is written or this flag set to 1 by software. The flag is set after I2C reset or Idle state. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x01
6	rw	**I2C1_RXF**	I2C Receive data register not empty. (set by hardware and clear by hardware or software writing 1) This bit is cleared when I2C1_DAT is read or this flag set to 1 by software. But it does not be cleared when I2C1_DAT is read by SWD debugging. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	rw	**I2C1_WUPF**	I2C wakeup from STOP mode flag. When hardware detect that the slave address is matched to I2C1_SADR (I2C1_SADR_EN=1) during STOP mode, this flag is asserted.(set by hardware and clear by software writing 1)	0x00

			0 = Normal (No event occurred) 1 = Happened (Event happened)	
4	rw	I2C1_TMOUTF	I2C time-out detect flag. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	I2C1_ERRF	I2C error interrupt flag for invalid no ack, bus arbitration lost bus error or data overrun error. (set by hardware , clear by software setting 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	I2C1_BUFF	I2C buffer mode event flag. (set by hardware , clear by software setting 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	rw	I2C1_EVENTF	I2C status event interrupt Flag. For Byte mode, this bit must be cleared and hardware can process to next state (set by hardware , clear by software setting 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	r	I2C1_BUSYF	I2C busy flag. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Busy (Event happened)	0x00

1.18.2. I2C1 interrupt enable register

I2C1_INT	I2C1 interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
I2C1_SDAF	I2C1_SCLF	Reserved					Reserved
23	22	21	20	19	18	17	16
Reserved						Reserved	Reserved
15	14	13	12	11	10	9	8
Reserved						Reserved	Reserved
7	6	5	4	3	2	1	0
Reserved	Reserved	I2C1_WUP_IE	I2C1_TMOUT_IE	I2C1_ERR_IE	I2C1_BUF_IE	I2C1_EVENT_IE	I2C1_IEA

Bit	Attr	Bit Name	Description	Reset
31	r	I2C1_SDAF	I2C SDA line status bit.	0x00
30	r	I2C1_SCLF	I2C SCL line status bit.	0x00
29..25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23..18	-	Reserved	Reserved	0x00
17	-	Reserved	Reserved	0x00
16	-	Reserved	Reserved	0x00
15..10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5	rw	I2C1_WUP_IE	I2C wakeup from STOP mode interrupt enable on slave address matched. 0 = Disable 1 = Enable	0x00
4	rw	I2C1_TMOUT_IE	I2C timeout error interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	I2C1_ERR_IE	I2C no ack error, bus arbitration lost, bus error or data overrun interrupt enable. 0 = Disable	0x00

			1 = Enable	
2	rw	**I2C1_BUF_IE**	I2C buffer mode event Interrupt enable. When enables, it will generate the interrupt if the flag of I2C1_RXF, I2C1_TXF, I2C1_RSTRF, I2C1_STOPF or I2C1_SADRF is set. 0 = Disable 1 = Enable	0x00
1	rw	**I2C1_EVENT_IE**	I2C status event interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	**I2C1_IEA**	I2C interrupt all enable. When disables, the I2C1 global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.18.3. I2C1 clock source register

I2C1_CLK	**I2C1 clock source register**		
Offset Address :	**0x08**	**Reset Value :**	**0x00000000**

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved			I2C1_TMO_CKS	I2C1_CK_PSC[3:0]			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	I2C1_CK_DIV[2:0]			I2C1_CK_SEL[1:0]		Reserved	

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..13	-	**Reserved**	Reserved	0x00
12	rw	**I2C1_TMO_CKS**	I2C timeout clock source select. 0 = CK_UT 1 = DIV64 (CK_I2C1_PSC divided by 64)	0x00
11..8	rw	**I2C1_CK_PSC**	I2C internal clock CK_I2C0_INT prescaler. The value range 1~15 is indicated divider 2~16.	0x00
7	-	**Reserved**	Reserved	0x00
6..4	rw	**I2C1_CK_DIV**	I2C internal clock CK_I2C1_INT input divider. [CK_I2C1_INT frequency = (I2C1_CK_PSC+1) * 2 ^(I2C1_CK_DIV)] 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8 0x4 = DIV16 : divided by 16 0x5 = DIV32 : divided by 32 0x6 = DIV64 : divided by 64 0x7 = DIV128 : divided by 128	0x00
3..2	rw	**I2C1_CK_SEL**	I2C internal clock CK_I2C1 source select. 0x0 = PROC : CK_I2C1_PR process clock from CSC 0x1 = Reserved 0x2 = TM00_TRGO 0x3 = Reserved	0x00
1..0	-	**Reserved**	Reserved	0x00

1.18.4. I2C1 slave mode slave address code register

I2C1_SAC	**I2C1 slave mode slave address code register**		
Offset Address :	**0x0C**	**Reset Value :**	**0x00000000**

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
I2C1_SA_CODE[6:0]							I2C1_SA_RW

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..1	r	I2C1_SA_CODE	I2C slave mode grabbed slave address code. When slave mode, I2C controller will grab the slave address code always.	0x00
0	r	I2C1_SA_RW	I2C slave mode grabbed read/write bit.	0x00

1.18.5. I2C1 control register 0

I2C1_CR0	I2C1 control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
I2C1_DMA_TXEN	I2C1_DMA_RXEN	Reserved					
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
I2C1_PDRV_SEL[1:0]		Reserved	I2C1_SCLS_DIS	I2C1_SFBD_EN	Reserved	Reserved	
7	6	5	4	3	2	1	0
I2C1_GC_EN	I2C1_BUF_EN	I2C1_MDS[1:0]		I2C1_NACK_EN	I2C1_SADR2_EN	I2C1_SADR_EN	I2C1_EN

Bit	Attr	Bit Name	Description	Reset
31	rw	I2C1_DMA_TXEN	Direct memory access enable to transmit. When enables, hardware can receive the data from DMA and transmit to output. 0 = Disable 1 = Enable	0x00
30	rw	I2C1_DMA_RXEN	Direct memory access enable to receive. When enables, hardware can receive the data from input and send to DMA. 0 = Disable 1 = Enable	0x00
29..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..14	rw	I2C1_PDRV_SEL	I2C pre-drive time select for both SCL and SDA by CK_I2C1 clock time. 0x0 = 0T (disable pre-drive) 0x1 = 1T 0x2 = 2T 0x3 = 3T	0x00
13	-	Reserved	Reserved	0x00
12	rw	I2C1_SCLS_DIS	I2C slave mode clock SCL stretching low control disable. This bit is only using for buffer mode. 0 = Enable 1 = Disable	0x00
11	rw	I2C1_SFBD_EN	I2C SDA first bit drive high enable when data transmitted. This bit is no effect and disabled when I2C0_PDRV_SEL=0. 0 = Disable 1 = Enable	0x00
10	-	Reserved	Reserved	0x00
9..8	-	Reserved	Reserved	0x00
7	rw	I2C1_GC_EN	I2C general call address 0x00 recognized enable bit.	0x00

			0 = Disable 1 = Enable	
6	rw	I2C1_BUF_EN	I2C data buffer enable bit. When enables, the I2C is operation in Buffer mode and a shadow buffer is using for data flow control. The I2C1_RXF and I2C1_TXF register flags will use to indicate the data register receiving not-empty and transmission empty. When disables, the I2C is operation in Byte mode by event code control. 0 = Disable 1 = Enable	0x00
5..4	rw	I2C1_MDS	I2C operation mode select. The monitor mode is only support for Buffer mode. 0x0 = I2C : Single/Multi-Master/ Slave mode 0x1 = Monitor : Monitor-Slave mode 0x2 = Reserved 0x3 = Reserved	0x00
3	rw	I2C1_NACK_EN	I2C master transmit ignore receiving NACK enable for Buffer mode. When enables, the I2C will continuously transmit next data when receive a NACK bit for master transmission mode. 0 = Disable 1 = Enable	0x00
2	rw	I2C1_SADR2_EN	I2C slave mode 2nd slave address detect enable. When enables , the I2C slave address I2C_SADR is not allowed to be updated. 0 = Disable 1 = Enable	0x00
1	rw	I2C1_SADR_EN	I2C slave mode main slave address detect enable. When enables , the I2C slave address I2C_SADR is not allowed to be updated. 0 = Disable 1 = Enable	0x00
0	rw	I2C1_EN	I2C function enable bit. When disables, the I2C1_SCL and I2C1_SDA pin state are switched to data port state. 0 = Disable 1 = Enable	0x00

1.18.6. I2C1 control register 1

I2C1_CR1	I2C1 control register 1		
Offset Address :	0x14	Reset Value :	0x00000504

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved			I2C1_HT[4:0]				
7	6	5	4	3	2	1	0
Reserved			I2C1_LT[4:0]				

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..13	-	Reserved	Reserved	0x00
12..8	rw	I2C1_HT	I2C SCL high cycle time by CK_I2C1_INT clock time. It write setting value for master mode. (SCL High time = START hold time = STOP setup time)	0x05
7..5	-	Reserved	Reserved	0x00
4..0	rw	I2C1_LT	I2C SCL low cycle time by CK_I2C1_INT clock time. It write setting value for master mode. (SCL Low time = START setup time = Bus free time between STOP and START)	0x04

1.18.7. I2C1 control register 2

I2C1_CR2	I2C1 control register 2		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved					I2C1_PAA	I2C1_PSTO	I2C1_PSTA
23	22	21	20	19	18	17	16
Reserved					I2C1_ACNT[2:0]		
15	14	13	12	11	10	9	8
Reserved					I2C1_BUF_CNT[2:0]		
7	6	5	4	3	2	1	0
Reserved	I2C1_AA_LCK	I2C1_STO_LCK	I2C1_STA_LCK	I2C1_CMD_TC	I2C1_AA	I2C1_STO	I2C1_STA

Bit	Attr	Bit Name	Description	Reset
31..27	-	Reserved	Reserved	0x00
26	rw	I2C1_PAA	I2C preload bit for Acknowledge enable bit.	0x00
25	rw	I2C1_PSTO	I2C preload bit for STOP enable bit.	0x00
24	rw	I2C1_PSTA	I2C preload bit forSTART enable bit.	0x00
23..19	-	Reserved	Reserved	0x00
18..16	r	I2C1_ACNT	I2C transmitted or received data actual byte count value. When transmitted or received data complete by last data transfer or error conditions, the actual transmitted or received data byte number is recorded in this register. The count value is not calculated and included the NACK error byte. For other conditions, this register value is no meaning. 0x0 = 0-byte 0x1 = 1-byte 0x2 = 2-byte 0x3 = 3-byte 0x4 = 4-byte	0x00
15..11	-	Reserved	Reserved	0x00
10..8	rw	I2C1_BUF_CNT	I2C transmitted or received data byte count threshold. When transmitted or received data arrives at the threshold and the interrupt enable bit of I2C1_BUFF_IE is enabled, the interrupt is generated. When writes this register, hardware will auto clear the I2C1_CNTF. 0x0 = Reserved 0x1 = 1-byte 0x2 = 2-byte 0x3 = 3-byte 0x4 = 4-byte	0x00
7	-	Reserved	Reserved	0x00
6	rw	I2C1_AA_LCK	I2C1_AA and I2C1_PAA bits write access protected control. When selects locked, disables the register bit write access. I2C0_AA and I2C0_PAA are written effectively only by written 1 to this bit simultaneously. 0 = Locked 1 = un-Locked	0x00
5	rw	I2C1_STO_LCK	I2C1_STO and I2C1_PSTO bits write access protected control. When selects locked, disables the register bit write access.I2C1_STO and I2C1_PSTO are written effectively only by written 1 to this bit simultaneously. 0 = Locked 1 = un-Locked	0x00
4	rw	I2C1_STA_LCK	I2C1_STA and I2C1_PSTA bits write access protected control. When selects locked, disables the register bit write access. I2C1_STA and I2C1_PSTA are written effectively only by written 1 to this bit simultaneously.	0x00

			0 = Locked 1 = un-Locked	
3	rw	**I2C1_CMD_TC**	I2C command preload enable control bit. When enables, it will write hold until I2C1_TCF set for I2C1_STA, I2C1_STO, I2C1_AA register bits. When disables, write these command bits that will directly execute the setting command. This bit is no effect if I2C0_BUF_EN=0. 0 = Disable 1 = Enable	0x00
2	rw	**I2C1_AA**	I2C assert Acknowledge enable bit. If the AA flag is set to '1', an ACK will be returned during the ACK clock pulse on the SCL line when: 1) The own slave address has been received. 2) A data byte has been received while I2C is in the master/receiver mode. 3) A data byte has been received while I2C is in the addressed slave/receiver mode. If the AA flag is reset to '0', a NACK will be returned during the ACK clock pulse on SCL when: 1) A data has been received while I2C is in the master/receiver mode. 2) A data byte has been received while I2C is in the addressed slave/receiver mode.	0x00
1	rw	**I2C1_STO**	I2C STOP enable bit. When the STO bit is set while I2C is in a master mode, a STOP condition is transmitted to the serial bus. When the STOP condition is detected on the bus, the I2C hardware clears the STO flag. In a slave mode, the STO flag may be set to recover from a bus error condition. In this case, no STOP condition is transmitted to the bus. However, the I2C hardware behaves as if a STOP condition has been received and switches to the defined not addressed slave receiver mode. The STO flag is automatically cleared by hardware. If the STA and STO bits are both set, then a STOP condition is transmitted to the bus if I2C is in a master mode (in a slave mode, I2C generates an internal STOP condition which is not transmitted), and then transmits a START condition.	0x00
0	rw	**I2C1_STA**	I2C START enable bit. When the STA bit is set to enter a master mode, the I2C hardware checks the status of the serial bus and generates a START condition if the bus is free. If the bus is not free, then I2C waits for a STOP condition and generates a START condition after a delay. If STA is set while I2C is already in a master mode and one or more bytes are transmitted or received, I2C transmits a repeated START condition. STA may be set at any time. STA may also be set when I2C is an addressed slave. When the STA bit is reset, no START condition or repeated START condition will be generated.	0x00

1.18.8. I2C1 slave address detect register

I2C1_SADR	**I2C1 slave address detect register**		
Offset Address :	**0x1C**	**Reset Value :**	**0x00000000**

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
I2C1_SADR2[6:0]							**Reserved**
7	6	5	4	3	2	1	0

I2C1_SADR[6:0]							Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..9	rw	I2C1_SADR2	I2C slave mode 2nd slave address detection request address value.	0x00
8	-	Reserved	Reserved	0x00
7..1	rw	I2C1_SADR	I2C slave mode main slave address detection request address value.	0x00
0	-	Reserved	Reserved	0x00

1.18.9. I2C1 timeout control register

I2C1_TMOUT	I2C1 timeout control register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
I2C1_TMO_CNT[7:0]							
7	6	5	4	3	2	1	0
Reserved				I2C1_TMO_MDS[1:0]		I2C1_TMO_CTL	I2C1_TMO_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	rw	I2C1_TMO_CNT	I2C timeout setting value.	0x00
7..4	-	Reserved	Reserved	0x00
3..2	rw	I2C1_TMO_MDS	I2C timeout detection mode select. When set value to 0x2, the timeout detection timer is able to use as a universal counter. 0x0 = SCL-low (SCL low timeout) 0x1 = SCL-SDA-high (both SCL and SDA high timeout for bus idle condition) 0x2 = General (general counter)	0x00
1	rw	I2C1_TMO_CTL	I2C timeout event happened I2C reset control enable bit. When enables, the I2C is reset and I2C1_EN is set to 0 if timeout is happened. 0 = Disable 1 = Enable	0x00
0	rw	I2C1_TMO_EN	I2C timeout detect enable. 0 = Disable 1 = Enable	0x00

1.18.10. I2C1 status register 2

I2C1_STA2	I2C1 status register 2		
Offset Address :	0x28	Reset Value :	0x000000F8

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							I2C1_EVENTF2
7	6	5	4	3	2	1	0
I2C1_EVENT[7:0]							

Bit	Attr	Bit Name	Description	Reset

31..16	-	Reserved	Reserved	0x0000
15..9	-	Reserved	Reserved	0x00
8	rw	I2C1_EVENTF2	I2C status event interrupt Flag. This bit same as I2C1_EVENTF (set by hardware , clear by software setting 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
7..0	r	I2C1_EVENT	I2C0 status event code	0xF8

1.18.11. I2C1 data shift buffer register

I2C1_SBUF	I2C1 data shift buffer register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
I2C1_SBUF[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	I2C1_SBUF	I2C data shift buffer register. Notify that read this register will get I2C1_DAT content in I2C Byte mode.	0x00

1.18.12. I2C1 data register

I2C1_DAT	I2C1 data register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
I2C1_DAT[31:24]							
23	22	21	20	19	18	17	16
I2C1_DAT[23:16]							
15	14	13	12	11	10	9	8
I2C1_DAT[15:8]							
7	6	5	4	3	2	1	0
I2C1_DAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	I2C1_DAT	I2C data byte register. When buffer mode is enabled, read this register will clear the I2C1_RXF and write this register will clear I2C1_TXF.	0x00000000

1.18.13. I2C1 slave address detect register

I2C1_MASK	I2C1 slave address detect register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0

I2C1_SA_MSK[6:0]	Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..8	-	**Reserved**	Reserved	0x00
7..1	rw	**I2C1_SA_MSK**	I2C slave address mask register. Zero bit in this result is considered as 'don't care'.	0x00
0	-	**Reserved**	Reserved	0x00

1.18.14. I2C1 Register Map

I2C1 Register Map Register Number = 13

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	I2C1_STA	Reserved							Reserved	I2C1_BERRF	I2C1_ALOSF	I2C1_NACKF	I2C1_TOVRF	I2C1_ROVRF	I2C1_TXRF	I2C1_STPSTRF	I2C1_TSCF	I2C1_RWF	I2C1_MSTF	I2C1_SLAF	I2C1_SADRF	I2C1_ERRCF	I2C1_CNTF	I2C1_STOPF	I2C1_RSTRF	I2C1_TXF	I2C1_RXF	I2C1_WUPF	I2C1_TMOUTF	I2C1_ERRF	I2C1_BUFF	I2C1_EVENTF	I2C1_BUSYF
Reset	0x00000080	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0x04	I2C1_INT	I2C1_SDAF	I2C1_SCLF	Reserved					Reserved	Reserved						Reserved	Reserved	Reserved						Reserved	Reserved	Reserved	Reserved	I2C1_WUP_IE	I2C1_TMOUT_IE	I2C1_ERR_IE	I2C1_BUF_IE	I2C1_EVENT_IE	I2C1_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	I2C1_CLK	Reserved																Reserved			I2C1_TMO_CKS	I2C1_CK_PSC [3:0]				Reserved	I2C1_CK_DIV [2:0]			I2C1_CK_SEL [1:0]		Reserved	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	I2C1_SAC	Reserved																Reserved								I2C1_SA_CODE [6:0]							I2C1_SA_RW
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	I2C1_CR0	I2C1_DMA_TXEN	I2C1_DMA_RXEN	Reserved						Reserved								I2C1_PDRV_SEL [1:0]		Reserved	I2C1_SCLS_DIS	I2C1_SFBD_EN	Reserved	Reserved		I2C1_GC_EN	I2C1_BUF_EN	I2C1_MDS[1:0]		I2C1_NACK_EN	I2C1_SADR2_EN	I2C1_SADR_EN	I2C1_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	I2C1_CR1	Reserved																Reserved			I2C1_HT[4:0]					Reserved			I2C1_LT[4:0]				
Reset	0x00000504	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0
0x18	I2C1_CR2	Reserved					I2C1_PAA	I2C1_PSTO	I2C1_PSTA	Reserved					I2C1_ACNT[2:0]			Reserved					I2C1_BUF_CNT [2:0]			Reserved	I2C1_AA_LCK	I2C1_STO_LCK	I2C1_STA_LCK	I2C1_CMD_TC	I2C1_AA	I2C1_STO	I2C1_STA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	I2C1_SADR	Reserved																I2C1_SADR2[6:0]							Reserved	I2C1_SADR[6:0]							Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x20	I2C1_TMOUT	Reserved																I2C1_TMO_CNT [7:0]								Reserved				I2C1_TMO_MDS [1:0]		I2C1_TMO_CTL	I2C1_TMO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	I2C1_STA2	Reserved																Reserved							I2C1_EVENTF2	I2C1_EVENT[7:0]							
Reset	0x000000F8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0
0x2C	I2C1_SBUF	Reserved																Reserved								I2C1_SBUF[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	I2C1_DAT	I2C1_DAT[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	I2C1_MASK	Reserved																Reserved								I2C1_SA_MSK [6:0]							Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.19. URT0 Control Registers

URT0 Control	(URT0) UART Control Module-0
Base Address :	0x52000000

1.19.1. URT0 status register 1

URT0_STA	URT0 status register 1		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	URT0_CALTMOF	URT0_BKTMOF	URT0_IDTMOF	URT0_RXTMOF	Reserved	URT0_TUDRF	URT0_TXEF
23	22	21	20	19	18	17	16
URT0_ROVRF	URT0_NCEF	URT0_FEF	URT0_PEF	Reserved	URT0_CTSF	URT0_IDLF	URT0_BKF
15	14	13	12	11	10	9	8
URT0_CALOVF	URT0_CALUDF	URT0_CALCF	URT0_TMOF	URT0_BRTF	URT0_SADRF	Reserved	Reserved
7	6	5	4	3	2	1	0
URT0_TXF	URT0_RXF	URT0_RXDF	URT0_LSF	URT0_ERRF	URT0_TCF	URT0_UGF	URT0_RHF

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	URT0_CALTMOF	UART auto baud-rate calibration sync field receive time-out time out flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
29	rw	URT0_BKTMOF	UART break receive time out flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
28	rw	URT0_IDTMOF	UART idle state time out flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
27	rw	URT0_RXTMOF	UART receive time out flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
26	-	Reserved	Reserved	0x00
25	rw	URT0_TUDRF	UART SPI slave mode transmit underrun flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
24	rw	URT0_TXEF	UART TX error detect flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of URTx_TXE_MDS for detail. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
23	rw	URT0_ROVRF	UART receive overrun error flag. (set by hardware and clear by software writing 1) When receive overrun, hardware will stop to receive next data into data shadow buffer until this flag is cleared. This flag is indicated for following two conditions. (1) When RX shadow buffer is arrived over the RX threshold and the data register has not read out. If shift buffer is filled of next data, this flag is asserted. (2) When Parity error, Frame error, Break detect or Slave-Address detect, has happened and caused RX shadow buffer input holding. If shift buffer is filled of next data, this flag is asserted. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
22	rw	URT0_NCEF	UART receive noised character error flag. (set by hardware	0x00

			and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	
21	rw	URT0_FEF	UART frame error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
20	rw	URT0_PEF	UART parity error flag. (set by hardware and clear by software writing 1) When multi-processor mode, the parity value is including of address bit. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19	-	Reserved	Reserved	0x00
18	rw	URT0_CTSF	UART CTS change detect interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	rw	URT0_IDLF	UART idle line detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
16	rw	URT0_BKF	UART break condition detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	r	URT0_CALOVF	UART auto baud-rate calibration overflow status flag. This flag is asserted when the baud-rate calibration counter is changed overflow during baud-rate calibration (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
14	r	URT0_CALUDF	UART auto baud-rate calibration underflow status flag. This flag is asserted when the baud-rate calibration counter is changed to zero during baud-rate calibration (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
13	rw	URT0_CALCF	UART auto baud-rate calibration complete flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
12	rw	URT0_TMOF	UART timeout timer timeout flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
11	rw	URT0_BRTF	UART baud-rate generator timer timeout flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
10	rw	URT0_SADRF	UART slave address matched flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	rw	URT0_TXF	UART transmit data register empty. (set by hardware and clear by hardware or software writing 1) When transmitted shadow buffer is empty and the data register URTx_TDAT will copy to the shadow buffer, this flag is set. This bit is cleared when URTx_TDAT is written or this flag set to 1 by software. The flag is set after UART reset or Idle state.	0x00

			0 = Normal (No event occurred) 1 = Happened (Event happened)	
6	rw	URT0_RXF	UART receive data register not empty. (set by hardware and clear by hardware or software writing 1) When received shadow buffer level URTx_RX_LVL is greater than or equal to the shadow buffer threshold URTx_RX_TH setting, this flag is set and the shadow buffer content copy to data register URTx_RDAT. This bit is cleared when URTx_RDAT is read or this flag set to 1 by software. But it does not be cleared when URTx_RDAT is read by SWD debugging. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	r	URT0_RXDF	UART received data byte number is different from previous received data byte number for URTx_RDAT register. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	URT0_LSF	UART line statue flag for break condition, idle line, CTS detect. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	URT0_ERRF	UART error interrupt flag for parity error, frame error, overrun error, receive time out and noise error. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	URT0_TCF	UART transmission complete flag. When both shadow buffer and data register are empty and shift buffer shift out complete, then set this flag. (set by hardware and clear by hardware or software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	rw	URT0_UGF	UART general event flag. It indicates each of URTx_SADRF , URTx_BRTF , URTx_TMOF or URTx_CALCF flag is asserted when this flag is set. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	rw	URT0_RHF	UART receive hold flag. It indicates one of hardware hold event is happened when this flag is set. In the condition, the shift buffer is held and do not load data to shadow buffer until this bit is cleared. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00

1.19.2. UART interrupt enable register

URT0_INT	UART interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	URT0_CALTMO_IE	URT0_BKTMO_IE	URT0_IDTMO_IE	URT0_RXTMO_IE	Reserved	URT0_TUDR_IE	URT0_TXE_IE
23	22	21	20	19	18	17	16
URT0_ROVR_IE	URT0_NCE_IE	URT0_FE_IE	URT0_PE_IE	Reserved	URT0_CTS_IE	URT0_IDL_IE	URT0_BK_IE
15	14	13	12	11	10	9	8
Reserved		URT0_CALC_IE	URT0_TMO_IE	URT0_BRT_IE	URT0_SADR_IE	Reserved	Reserved
7	6	5	4	3	2	1	0
URT0_TX_IE	URT0_RX_IE	Reserved	URT0_LS_IE	URT0_ERR_IE	URT0_TC_IE	URT0_UG_IE	URT0_IEA

Bit	Attr	Bit Name	Description	Reset

31	-	**Reserved**	Reserved	0x00
30	rw	**URT0_CALTMO_IE**	UART auto baud-rate calibration sync field receive time-out time out interrupt enable. 0 = Disable 1 = Enable	0x00
29	rw	**URT0_BKTMO_IE**	UART break receive time out interrupt enable. 0 = Disable 1 = Enable	0x00
28	rw	**URT0_IDTMO_IE**	UART idle state time out interrupt enable. 0 = Disable 1 = Enable	0x00
27	rw	**URT0_RXTMO_IE**	UART receive time out interrupt enable. 0 = Disable 1 = Enable	0x00
26	-	**Reserved**	Reserved	0x00
25	rw	**URT0_TUDR_IE**	UART SPI slave mode transmit underrun interrupt enable. 0 = Disable 1 = Enable	0x00
24	rw	**URT0_TXE_IE**	UART TX error detect interrupt enable. Refer to the register descriptions of URTx_TXE_MDS for detail. 0 = Disable 1 = Enable	0x00
23	rw	**URT0_ROVR_IE**	UART receive overrun error interrupt enable. Refer to the register descriptions of URTx_ROVRF for the detail. 0 = Disable 1 = Enable	0x00
22	rw	**URT0_NCE_IE**	UART receive noised character interrupt enable. 0 = Disable 1 = Enable	0x00
21	rw	**URT0_FE_IE**	UART frame error interrupt enable. 0 = Disable 1 = Enable	0x00
20	rw	**URT0_PE_IE**	UART parity error interrupt enable. 0 = Disable 1 = Enable	0x00
19	-	**Reserved**	Reserved	0x00
18	rw	**URT0_CTS_IE**	UART CTS change detect interrupt enable. 0 = Disable 1 = Enable	0x00
17	rw	**URT0_IDL_IE**	UART idle line detect interrupt enable. 0 = Disable 1 = Enable	0x00
16	rw	**URT0_BK_IE**	UART break condition detect interrupt enable. 0 = Disable 1 = Enable	0x00
15..14	-	**Reserved**	Reserved	0x00
13	rw	**URT0_CALC_IE**	UART auto baud-rate calibration complete interrupt enable. 0 = Disable 1 = Enable	0x00
12	rw	**URT0_TMO_IE**	UART timeout timer timeout interrupt enable. 0 = Disable 1 = Enable	0x00
11	rw	**URT0_BRT_IE**	UART baud-rate generator timer timeout interrupt enable. 0 = Disable 1 = Enable	0x00
10	rw	**URT0_SADR_IE**	UART slave address matched interrupt enable. 0 = Disable 1 = Enable	0x00
9	-	**Reserved**	Reserved	0x00
8	-	**Reserved**	Reserved	0x00

7	rw	URT0_TX_IE	UART transmit data register empty interrupt enable. Refer to the register descriptions of URTx_TXF for the detail. 0 = Disable 1 = Enable	0x00
6	rw	URT0_RX_IE	UART receive data register not empty interrupt enable. Refer to the register descriptions of URTx_RXF for the detail. 0 = Disable 1 = Enable	0x00
5	-	Reserved	Reserved	0x00
4	rw	URT0_LS_IE	UART line statue flag for break condition, idle line, CTS detect. 0 = Disable 1 = Enable	0x00
3	rw	URT0_ERR_IE	UART error interrupt enable for parity error, frame error, overrun error, receive time out and noise error. 0 = Disable 1 = Enable	0x00
2	rw	URT0_TC_IE	UART transmission complete interrupt enable. (set by hardware and clear by hardware or software writing 1) 0 = Disable 1 = Enable	0x00
1	rw	URT0_UG_IE	UART general event interrupt enable for URTx_SADRF , URTx_TF , URTx_RCNTF or URTx_TCNTF events. 0 = Disable 1 = Enable	0x00
0	rw	URT0_IEA	UART interrupt all enable. When disables, the UART global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.19.3. URT0 clock source register

URT0_CLK	URT0 clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	URT0_BR_CKS	URT0_CKO_LCK	URT0_CKO_STA	URT0_BRO_LCK	URT0_BRO_STA	URT0_BR_MDS	URT0_BR_EN
23	22	21	20	19	18	17	16
Reserved		URT0_TX_CKS[1:0]		Reserved		URT0_RX_CKS[1:0]	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
URT0_ECK_CKS	Reserved	URT0_CLK_CKS	URT0_CLK_EN	URT0_CK_SEL[2:0]			Reserved

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	URT0_BR_CKS	UART baud-rate timer clock source select. 0 = PSC : CK_URTx_PSC from clock prescaler output 1 = CK_URTx : CK_URTx from UART internal clock input	0x00
29	rw	URT0_CKO_LCK	UART PSC clock output signal initial state control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	0x00
28	rw	URT0_CKO_STA	UART PSC clock output signal initial state. The bit is written effectively only by written 1 to URTx_CKO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
27	rw	URT0_BRO_LCK	UART baud-rate timer timeout signal initial state control. When	0x00

			locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	
26	rw	URT0_BRO_STA	UART baud-rate timer timeout signal initial state. The bit is written effectively only by written 1 to URTx_BRO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
25	rw	URT0_BR_MDS	UART baud-rate timer mode select. Combined mode is only using for general purpose counter. When SmartCard mode, this bit need set to 'Separated' for SmartCard clock output from PSC output. 0 = Separated : Separated PSC and CNT counters for UART baud-rate generator 1 = Combined : Combine to a linear counter for general using timer	0x00
24	rw	URT0_BR_EN	UART baud-rate timer enable. When enables, the baud-rate timer 0 = Disable 1 = Enable	0x00
23..22	-	Reserved	Reserved	0x00
21..20	rw	URT0_TX_CKS	UART transmission clock source select. 0x0 = Internal : UART internal clock source CK_URTx_INT 0x1 = TM01_TRGO 0x2 = TM10_TRGO 0x3 = EXT_CLK (external clock from URTx_CLK pin)	0x00
19..18	-	Reserved	Reserved	0x00
17..16	rw	URT0_RX_CKS	UART receive clock source select. 0x0 = Internal : UART internal clock source CK_URTx_INT 0x1 = TM01_TRGO 0x2 = TM10_TRGO 0x3 = EXT_CLK (external clock from URTx_CLK pin)	0x00
15..8	-	Reserved	Reserved	0x00
7	rw	URT0_ECK_CKS	UART external clock IO select. When select 'RX', the external clock is connected to the selected signal which is selected from URTx_RX or URTx_TX by URTx_IO_SWAP. 0 = CLK : URTx_CLK pin 1 = RX : receiving signal	0x00
6	-	Reserved	Reserved	0x00
5	rw	URT0_CLK_CKS	UART external clock output source select. 0 = OUT : CK_URTx_OUT from clock output divider 1 = SC : CK_URTx_SC from clock input prescaler	0x00
4	rw	URT0_CLK_EN	URTx_CLK signal output enable. 0 = Disable 1 = Enable	0x00
3..1	rw	URT0_CK_SEL	UART internal clock CK_URTx source select. 0x0 = PROC : CK_URTx_PR process clock from CSC 0x1 = NCO_P0 0x2 = CK_LS 0x3 = TM00_TRGO 0x4 = EXT_CLK (external clock from URTx_ECK signal)	0x00
0	-	Reserved	Reserved	0x00

1.19.4. URT0 status register 2

URT0_STA2	URT0 status register 2		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24

Reserved	URT0_TX_LVL[2:0]			Reserved	URT0_RX_LVL[2:0]		
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	URT0_CTS	Reserved		Reserved	Reserved
7	6	5	4	3	2	1	0
URT0_IR_BUSYF	URT0_BKBF	URT0_NCF	Reserved	Reserved	URT0_ADR	URT0_PAR	URT0_BUSYF

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30..28	r	URT0_TX_LVL	UART data buffer transmission remained level indications. 0x0 = 0 (0-byte,empty) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	0x00
27	-	Reserved	Reserved	0x00
26..24	r	URT0_RX_LVL	UART data buffer received level indications. 0x0 = 0 (0-byte,empty) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	0x00
23..16	-	Reserved	Reserved	0x00
15	-	Reserved	Reserved	0x00
14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	r	URT0_CTS	UART CTS line status bit. This bit reflects the CTS line status which is the watched point behind the CTS input inverter.	0x00
11..10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	r	URT0_IR_BUSYF	UART IrDA data received busy flag. 0 = No (No IrDA signal detect) 1 = Busy (detect some IrDA signal)	0x00
6	r	URT0_BKBF	UART send break busy flag. (set and clear by hardware) 0 = Normal (No break transmitted or transmit finished) 1 = Busy (Event happened)	0x00
5	r	URT0_NCF	UART receive noised character flag. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	-	Reserved	Reserved	0x00
3	-	Reserved	Reserved	0x00
2	r	URT0_ADR	UART data receive slave address bit of shift buffer.	0x00
1	r	URT0_PAR	UART data receive parity bit of shift buffer. When multi-processor mode, the parity value is including of address bit.	0x00
0	r	URT0_BUSYF	UART RX busy flag. (set and clear by hardware) When detect valid start bit, this bit is set and clear after stop bit. 0 = Normal (No event occurred) 1 = Busy (Event happened)	0x00

1.19.5. URT0 control register 0

URT0_CR0	URT0 control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT0_DMA_TXEN	URT0_DMA_RXEN	URT0_DDTX_EN	Reserved	Reserved	Reserved		Reserved
23	22	21	20	19	18	17	16

URT0_LBM_EN	URT0_NCHAR_DIS	URT0_NCHAR_HE	URT0_IDL_MDS	Reserved		URT0_RX_TH[1:0]	
15	14	13	12	11	10	9	8
URT0_DE_GT[1:0]		URT0_DE_INV	URT0_DE_EN	URT0_TX_INV	URT0_RX_INV	URT0_SYNC_MDS	URT0_IO_SWP
7	6	5	4	3	2	1	0
URT0_GSA_EN	URT0_MDS[2:0]			URT0_DAT_LINE	URT0_HDX_EN	URT0_OS_MDS	URT0_EN

Bit	Attr	Bit Name	Description	Reset
31	rw	URT0_DMA_TXEN	Direct memory access enable to transmit. When enables, hardware can receive the data from DMA and transmit to output. This bit is enabled to write if URTx_TX_EN=0. 0 = Disable 1 = Enable	0x00
30	rw	URT0_DMA_RXEN	Direct memory access enable to receive. When enables, hardware can receive the data from input and send to DMA. This bit is enabled to write if URTx_RX_EN=0. 0 = Disable 1 = Enable	0x00
29	rw	URT0_DDTX_EN	Hardware force to disable DMA TX function enable bit when detects a break condition. When enables, hardware will disable the URTx_DMA_TXEN bit if hardware detects a break condition. Also, the URTx_DMA_RXEN bit is disabled in this condition. When disables, hardware will keep to do DMA TX function if hardware detects a break condition. 0 = Disable 1 = Enable	0x00
28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26..25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23	rw	URT0_LBM_EN	UART loop back mode enable bit. When enables, the received input is taken from transmitted output to replace from input pin(RX ->TX ,CTS -> RTS). 0 = Disable 1 = Enable	0x00
22	rw	URT0_NCHAR_DIS	UART receiving noised character disable bit. When disables, the received noised character is skipped and does not assert the URTx_RXF interrupt. Also the noised character will copy to URTx_RCAP data register. When enables, the noised character is accepted for receiving. 0 = Enable (Accept noised character) 1 = Disable (Skip noised character)	0x00
21	rw	URT0_NCHAR_HE	UART receiving hold enable bit if receives a noised character. This bit is no effect when URTx_NCHAR_DIS=0. When enables and URTx_NCHAR_DIS=1, the received data will be hold from shift buffer to shadow buffer and the URTx_RHF will be active after received noised character. Until the URTx_RHF is cleared, chip will release the hold function. 0 = Disable 1 = Enable	0x00
20	rw	URT0_IDL_MDS	UART idle line detect management mode select. When selects 'Load' and detects idle line, chip will load shadow buffer into URTx_RDAT register even though it is not over the receive threshold URTx_RX_TH if shadow buffer is not empty. 0 = No (No operation) 1 = Load (Force to load shadow buffer)	0x00
19..18	-	Reserved	Reserved	0x00
17..16	rw	URT0_RX_TH	UART data buffer high threshold for received access. This register will set to '0' (1byte) and is no effect for register written if URTx_DMA_RXEN is enabled. 0x0 = 1byte (default) 0x1 = 2byte	0x00

			0x2 = 3byte 0x3 = 4byte	
15..14	rw	URT0_DE_GT	URTx_DE signal output guard time select by unit of bit time. The selection set both asserted time before START bit and deasserted time after last STOP bit. 0x0 = 1/4 0x1 = 1/2 0x2 = 1 0x3 = 2	0x00
13	rw	URT0_DE_INV	URTx_DE signal inverse enable. The hardware DE output default is low level. 0 = Disable 1 = Enable	0x00
12	rw	URT0_DE_EN	URTx_DE signal output enable. 0 = Disable 1 = Enable	0x00
11	rw	URT0_TX_INV	URTx_TX output signal inverse enable. 0 = Disable 1 = Enable	0x00
10	rw	URT0_RX_INV	URTx_RX input signal inverse enable. 0 = Disable 1 = Enable	0x00
9	rw	URT0_SYNC_MDS	UART SYNC mode(SPI) select. 0 = Master : SPI Master 1 = Slave : SPI Slave	0x00
8	rw	URT0_IO_SWP	URTx_RX/URTx_TX swap enable bit. 0 = Disable 1 = Enable	0x00
7	rw	URT0_GSA_EN	UART multi-processor global slave address enable.	0x00
6..4	rw	URT0_MDS	UART mode select. The Idle-line and Address-bit modes are using for multi-processor control. When selects IDLE or ADR mode, both URTx_MUTE_AEN0 and URTx_MUTE_AEX0 must be enabled. 0x0 = UART : UART mode 0x1 = SYNC : Synchronous/SPI mode 0x2 = IDLE : Idle-line mode for multi-processor 0x3 = ADR : Address-bit mode for multi-processor	0x00
3	rw	URT0_DAT_LINE	UART communication data line select. 0 = 2 : 2-lines separated ~ URTx_RX , URTx_TX 1 = 1 : 1-line Bidirectional ~URTx_TX only.	0x00
2	rw	URT0_HDX_EN	UART Half-duplex mode enable. When enables and UART is during transmission data, the URTx_RX input is no using and the data does not transfer into shadow buffer. 0 = Disable 1 = Enable	0x00
1	rw	URT0_OS_MDS	UART RX data oversampling majority vote select. 0 = Three : Three sample bits method 1 = One : One sample bit method and noise free	0x00
0	rw	URT0_EN	UART function enable bit. 0 = Disable 1 = Enable	0x00

1.19.6. URT0 control register 1

URT0_CR1	URT0 control register 1		
Offset Address :	0x14	Reset Value :	0x0F400F40

31	30	29	28	27	26	25	24
Reserved	Reserved		URT0_TXOS_NUM[4:0]				
23	22	21	20	19	18	17	16

<table>
<tr><td colspan="2">URT0_TXSTP_LEN[1:0]</td><td>URT0_TXMSB_EN</td><td>URT0_TXPAR_STK</td><td>URT0_TXPAR_POL</td><td>URT0_TXPAR_EN</td><td colspan="2">URT0_TXDSIZE[1:0]</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">Reserved</td><td colspan="5">URT0_RXOS_NUM[4:0]</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">URT0_RXSTP_LEN[1:0]</td><td>URT0_RXMSB_EN</td><td>URT0_RXPAR_STK</td><td>URT0_RXPAR_POL</td><td>URT0_RXPAR_EN</td><td colspan="2">URT0_RXDSIZE[1:0]</td></tr>
</table>

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30..29	-	Reserved	Reserved	0x00
28..24	rw	URT0_TXOS_NUM	UART TX data oversampling samples select. When selects SYNC Master mode, the valid value is from 1 to 31 for oversampling number from 2 to 32. When selects other modes, the valid value is from 3 to 31 for oversampling samples from 4 to 32. (This register is written no effect if UART_TX_EN set 1.)	0x0F
23..22	rw	URT0_TXSTP_LEN	UART TX stop bit length select. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = 0.5bit 0x1 = 1bit 0x2 = 1.5bit 0x3 = 2bit	0x01
21	rw	URT0_TXMSB_EN	UART TX data order Msb first enable. When disables , the Lsb bit will be the first bit. (This register is written no effect if URTx_TX_EN set 1.) 0 = Disable 1 = Enable	0x00
20	rw	URT0_TXPAR_STK	UART stuck parity bit output enable. When enables and URTx_TXPAR_EN=1, parity bit output fixed value by URTx_TXPAR_POL value setting. 0 = Disable 1 = Enable	0x00
19	rw	URT0_TXPAR_POL	UART TX parity bit polarity. This bit is no effect for SPI and SYNC mods. 0x0 = Even 0x1 = Odd	0x00
18	rw	URT0_TXPAR_EN	UART TX parity bit enable. This bit does not be set for SYNC mods. (This register is written no effect if URTx_TX_EN set 1.) 0 = Disable 1 = Enable	0x00
17..16	rw	URT0_TXDSIZE	UART TX data bit length. It is not including START, STOP, ADR or PARITY bits. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = 8bit 0x1 = 7bit 0x2 = Reserved 0x3 = Reserved	0x00
15..13	-	Reserved	Reserved	0x00
12..8	rw	URT0_RXOS_NUM	UART RX data oversampling samples select. When selects SYNC Master mode, the valid value is from 1 to 31 for oversampling number from 2 to 32. When selects other modes, the valid value is from 3 to 31 for oversampling samples from 4 to 32. (This register is written no effect if UART_RX_EN set 1.)	0x0F
7..6	rw	URT0_RXSTP_LEN	UART RX stop bit length select. (This register is written no effect if URTx_RX_EN set 1.) 0x0 = 0.5bit 0x1 = 1bit 0x2 = 1.5bit 0x3 = 2bit	0x01
5	rw	URT0_RXMSB_EN	UART RX data order Msb first enable. When disables , the Lsb bit will be the first bit. (This register is written no effect if URTx_RX_EN set 1.) 0 = Disable	0x00

			1 = Enable	
4	rw	URT0_RXPAR_STK	UART stuck parity bit input enable. When enables and URTx_RXPAR_EN=1, parity bit input fixed value by URTx_RXPAR_POL value setting. 0 = Disable 1 = Enable	0x00
3	rw	URT0_RXPAR_POL	UART RX parity bit polarity. This bit is no effect for SYNC mods. 0x0 = Even 0x1 = Odd	0x00
2	rw	URT0_RXPAR_EN	UART RX parity bit enable. This bit does not be set for SYNC mods. (This register is written no effect if URTx_RX_EN set 1.) 0 = Disable 1 = Enable	0x00
1..0	rw	URT0_RXDSIZE	UART RX data bit length. It is not including START, STOP, ADR or PARITY bits. This bit is no effect for SPI and SYNC mods. (This register is written no effect if URTx_RX_EN set 1.) 0x0 = 8bit 0x1 = 7bit 0x2 = Reserved 0x3 = Reserved	0x00

1.19.7. URT0 control register 2

URT0_CR2	URT0 control register 2		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT0_DOUT_IDL[1:0]		URT0_DOUT_MDS	Reserved	URT0_NSSI_EN	URT0_NSS_SWEN	URT0_NSS_INV	URT0_NSSI_INV
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved						URT0_NSS_SWI	URT0_NSS_SWO
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			URT0_TX_HALT	URT0_TX_EN	URT0_RX_EN	URT0_ADR_TX	URT0_BK_TX

Bit	Attr	Bit Name	Description	Reset
31..30	rw	URT0_DOUT_IDL	UART SPI mode idle state data output value. When SPI master mode URTx_DOUT_MDS is enabled, the URTx_TX output is with driving during idle state and the output level is set by this bit. 0x0 = LBIT (Last data bit) 0x1 = Reserved 0x2 = 0 (Output 0) 0x3 = 1 (Output 1)	0x00
29	rw	URT0_DOUT_MDS	UART SPI master standard mode idle state data output mode select. When disables and data transfers during idle state, the MOSI will output with tristate for master mode. When enables and data transfers during idle state, the MOSI will output with driving for master mode. 0 = Disable : Output with tristate 1 = Enable : Output with driving	0x00
28	-	Reserved	Reserved	0x00
27	rw	URT0_NSSI_EN	UART NSS signal input function enable when UART configure to synchronous mode SPI Slave. 0 = Disable 1 = Enable	0x00
26	rw	URT0_NSS_SWEN	UART NSS signal output set by software control function enable bit. 0 = Disable 1 = Enable	0x00

25	rw	URT0_NSS_INV	UART NSS output signal inverse enable. The hardware NSS output default is low active level. 0 = Disable 1 = Enable	0x00
24	rw	URT0_NSSI_INV	UART NSS input signal inverse enable. 0 = Disable 1 = Enable	0x00
23..18	-	Reserved	Reserved	0x00
17	r	URT0_NSS_SWI	UART NSS signal software input status bit.	0x00
16	rw	URT0_NSS_SWO	UART NSS signal software output control bit when URTx_NSS_SWEN is enable.	0x00
15..8	-	Reserved	Reserved	0x00
7..5	-	Reserved	Reserved	0x00
4	rw	URT0_TX_HALT	UART transmitter halt enable. 0 = Disable 1 = Enable	0x00
3	rw	URT0_TX_EN	UART transmitter enable. 0 = Disable 1 = Enable	0x00
2	rw	URT0_RX_EN	UART receiver enable. When URTx_MDS selects SYNC mode and URTx_DAT_LINE sets 1-line, enables this bit is used to set receiver mode only and disables this bit is used to set transmission mode only. 0 = Disable 1 = Enable	0x00
1	rw	URT0_ADR_TX	UART slave address for next data transmitted. This bit will clear by hardware after slave address sending end. If this bit and URTx_BK_TX are both set to 1, only the URTx_BK_TX function is action. Refer the URTx_TXGT_LEN register descriptions for more information. (set by software and clear by hardware) 0 = Normal 1 = Send : Send Address	0x00
0	rw	URT0_BK_TX	UART break condition for next data transmitted. This bit will clear by hardware after break condition sending end. If this bit and URTx_ADR_TX are both set to 1, only the URTx_BK_TX function is action. (set by software and clear by hardware) 0 = Normal 1 = Send : Send Break	0x00

1.19.8. URT0 control register 3

URT0_CR3	URT0 control register 3		
Offset Address :	0x1C	Reset Value :	0x00000A00

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT0_TXGT_LEN[7:0]							
15	14	13	12	11	10	9	8
URT0_DET_IDL[7:0]							
7	6	5	4	3	2	1	0
Reserved			URT0_DET_BK	Reserved	URT0_CPHA	URT0_CPOL	Reserved

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	rw	URT0_TXGT_LEN	UART TX guard time or idle-line length. (1)URTx_MDS=UART,SYNC,ADR modes: This register use as TX guard time between adjacent characters' transmission in the unit of bit time. The time is starting after STOP bit of the	0x00

			last character. Value 0 indicates 0 bit time. (for SmartCard minimum guard-time, counting start at Start bit = 12+{0~254} bit time) (2)URTx_MDS=IDLE mode: This register use as the idle-line length in the unit of bit time.	
15..8	rw	URT0_DET_IDL	UART idle line detect threshold value by using receive bit time. The timeout threshold is starting after STOP bit of the last character and value 1 indicates 2 bit time. The value 0 is invalid.	0x0A
7..5	-	Reserved	Reserved	0x00
4	rw	URT0_DET_BK	UART bit time select for break detection or transmission. For data receiving, the detect time is a character time plus this value after last STOP bit cycle. For data transmission, the break generation guard time is a character time plus this value+3 bit time. 0x0 = 1Bit 0x1 = 3Bit	0x00
3	-	Reserved	Reserved	0x00
2	rw	URT0_CPHA	UART clock phase select. It is used to select the data sampling on leading edge or trailing edge of SPI clock. 0 = Leading edge 1 = Trailing edge	0x00
1	rw	URT0_CPOL	UART clock polarity select. It is used to select the SPI clock level in idle state. 0 = Low 1 = High	0x00
0	-	Reserved	Reserved	0x00

1.19.9. URT0 control register 4

URT0_CR4	URT0 control register 4		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	URT0_TNUM[2:0]			Reserved	URT0_RNUM[2:0]		
7	6	5	4	3	2	1	0
URT0_TDAT_CLR	URT0_RDAT_CLR	URT0_TDAT_INV	URT0_RDAT_INV	Reserved	Reserved	Reserved	Reserved

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15	-	Reserved	Reserved	0x00
14..12	r	URT0_TNUM	UART remained data byte number in data register. Value 0~4 is valid only. 0x0 = 0 (0-byte) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	0x00
11	-	Reserved	Reserved	0x00
10..8	rw	URT0_RNUM	UART received data byte number when data shadow buffer last transfer to URTx_RDAT register. Firmware can write an initial value for received byte number comparison for URTx_RXDF status bit. Value 0~4 is valid only. 0x0 = 0 (0-byte) 0x1 = 1 (1-byte)	0x00

			0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	
7	w	**URT0_TDAT_CLR**	UART transmitted data clear enable. When enables, the transmitted data buffer will be flushed and URTx_TXF flag is set. Also URTx_TNUM and URTx_TX_LVL are cleared. It allows discarding the data when data has not been send under NACK error and frame error is active for SmartCard mode. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
6	w	**URT0_RDAT_CLR**	UART received data clear enable. When enables, the received data buffer will be flushed and URTx_RXF flag is cleared. Also URTx_RNUM and URTx_RX_LVL are cleared. It allows discarding the data without reading it and avoid a data overrun condition. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
5	rw	**URT0_TDAT_INV**	UART inverse transmitted data enable. When enables, the transmitted data bits are inverted but Start, Stop, Address and Parity bits are not inverted. 0 = Disable 1 = Enable	0x00
4	rw	**URT0_RDAT_INV**	UART inverse received data enable. When enables, the received data bits are inverted but Start, Stop, Address and Parity bits are not inverted. 0 = Disable 1 = Enable	0x00
3	-	**Reserved**	Reserved	0x00
2	-	**Reserved**	Reserved	0x00
1	-	**Reserved**	Reserved	0x00
0	-	**Reserved**	Reserved	0x00

1.19.10. URT0 baud-rate clock counter reload register

URT0_RLR	URT0 baud-rate clock counter reload register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		URT0_PSR[5:0]					
7	6	5	4	3	2	1	0
URT0_RLR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..14	-	**Reserved**	Reserved	0x00
13..8	rw	**URT0_PSR**	UART baud-rate clock prescaler reload register. Actual value equals the register value plus one.	0x00
7..0	rw	**URT0_RLR**	UART baud-rate clock counter reload register. Actual value equals the register value plus one.	0x00

1.19.11. URT0 baud-rate clock counter register

URT0_CNT	URT0 baud-rate clock counter register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		URT0_PSC[5:0]					
7	6	5	4	3	2	1	0
URT0_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..8	r	URT0_PSC	UART baud-rate clock prescaler value register.	0x00
7..0	r	URT0_CNT	UART baud-rate clock counter value register.	0x00

1.19.12. URT0 RX data capture register

URT0_RCAP	URT0 RX data capture register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved					URT0_RCAP_ADR	URT0_RCAP_PAR	URT0_RCAP_STP
7	6	5	4	3	2	1	0
URT0_RCAP_DAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..11	-	Reserved	Reserved	0x00
10	rw	URT0_RCAP_ADR	UART capture address bit from RX shift buffer.	0x00
9	rw	URT0_RCAP_PAR	UART capture parity bit from RX shift buffer.	0x00
8	rw	URT0_RCAP_STP	UART capture stop bit from RX shift buffer.	0x00
7..0	rw	URT0_RCAP_DAT	UART capture data from RX shift buffer for Parity error / Frame error / Break detect / Slave-Address detect matched / Calibration Sync Character / Noise Character. The capture function is disabled for synchronous mode. The capture data is affected by data order Msb first setting in URTx_RXMSB_EN. But it not affected by received data inverse setting in URTx_RDAT_INV.	0x00

1.19.13. URT0 RX data register

URT0_RDAT	URT0 RX data register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT0_RDAT[31:24]							
23	22	21	20	19	18	17	16
URT0_RDAT[23:16]							
15	14	13	12	11	10	9	8
URT0_RDAT[15:8]							
7	6	5	4	3	2	1	0
URT0_RDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	URT0_RDAT	UART received data register. Read this register will clear the	0x00000000

			URTx_RXF. Hardware will force to logic 0 for non-updated byte(s) by URTx_RX_TH setting.	

1.19.14. URT0 TX data register

URT0_TDAT	URT0 TX data register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT0_TDAT[31:24]							
23	22	21	20	19	18	17	16
URT0_TDAT[23:16]							
15	14	13	12	11	10	9	8
URT0_TDAT[15:8]							
7	6	5	4	3	2	1	0
URT0_TDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	URT0_TDAT	UART transmitted data register. Write this register will clear the URTx_TXF. When write data by word, half-word or byte operation, chip will transfer 4-byte, 2-byte, or 1-byte data to shadow buffer. (write-only)	0x00000000

1.19.15. URT0 TX data 3-byte register

URT0_TDAT3	URT0 TX data 3-byte register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT0_TDAT3[23:16]							
15	14	13	12	11	10	9	8
URT0_TDAT3[15:8]							
7	6	5	4	3	2	1	0
URT0_TDAT3[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..0	w	URT0_TDAT3	UART transmitted data register for 3-byte data write only. Write this register will clear the URTx_TXF and force to transfer all 24-bit data to shadow buffer. This register is only allowed to access by a 32-bit word instruction.	0x000000

1.19.16. URT0 data shift buffer register

URT0_SBUF	URT0 data shift buffer register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
URT0_TSBUF[7:0]							
7	6	5	4	3	2	1	0
URT0_RSBUF[7:0]							

Bit	Attr	Bit Name	Description	Reset

31..16	-	Reserved	Reserved	0x0000
15..8	r	URT0_TSBUF	UART TX data shift buffer register.	0x00
7..0	r	URT0_RSBUF	UART RX data shift buffer register.	0x00

1.19.17. URT0 timeout control register

URT0_TMOUT	URT0 timeout control register		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT0_CALTMO_TH[3:0]				URT0_BKTMO_TH[3:0]			
23	22	21	20	19	18	17	16
URT0_RXTMO_TH[7:0]							
15	14	13	12	11	10	9	8
URT0_TMO_LCK	URT0_TMO_STA	Reserved			URT0_TMO_CKS[2:0]		
7	6	5	4	3	2	1	0
URT0_CALTMO_EN	URT0_BKTMO_EN	URT0_RXTMO_EN	URT0_IDTMO_EN	URT0_TMO_MDS[1:0]		URT0_TMO_RST	URT0_TMO_EN

Bit	Attr	Bit Name	Description	Reset
31..28	rw	URT0_CALTMO_TH	UART calibration timeout detect threshold value for TMO counter value comparison. When the TMO counter over the threshold, the calibration timeout is happened. The timeout threshold equals (register value)*BASE. When URT0_BR_MDS sets 'Separated', the BASE value is 0x10 and value 0 indicates counter overflow value 0xFF. When URT0_BR_MDS sets 'Combined', the BASE value is 0x100 and value 0 indicates counter overflow value 0xFFF. When calibration has finished, the TMO counter value will be copied to update the baud-rate generator BRO timer. If calibration timeout is happened, the BRO timer will keep the old baud-rate setting.	0x00
27..24	rw	URT0_BKTMO_TH	UART receive Break timeout detect threshold value by using receive bit time. The timeout threshold is starting after URTx_BKF bit asserting when hardware detect a Break character. Value 0 indicates 1 bit time.	0x00
23..16	rw	URT0_RXTMO_TH	UART RX data buffer timeout detect threshold value by using receive bit time. The timeout threshold is starting after STOP bit of the last character. The timeout threshold equal (register value+1)*8 (receive bit time) and value 0 indicates 8 bits time.	0x00
15	rw	URT0_TMO_LCK	UART timeout timer timeout signal initial state control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	0x00
14	rw	URT0_TMO_STA	UART timeout timer timeout signal initial state. The bit is written effectively only by written 1 to URTx_TMO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
13..11	-	Reserved	Reserved	0x00
10..8	rw	URT0_TMO_CKS	UART timeout timer clock source select. When URTx_TMO_MDS selects 'UART' mode, this register must select CK_URTx_BIT(UART) as TMO timer clock for normal operation. When selects 'Noise' and sets URTx_TMO_EN=1, the number of received noise bit is able to read from URTx_TMO_CNT. 0x0 = UART (CK_URTx_BIT clock) 0x1 = Input (CK_UART clock input) 0x2 = Noise (Noise bit receive event) 0x3 = Reserved	0x00

7	rw	URT0_CALTMO_EN	UART Calibration timeout detection enable bit. When enables and URTx_CAL_AUTO=1 if Break condition has detected, chip will trigger timer-out timer to start counting. After the Calibration timeout detection and the corrected auto-sync-field has not received, UART will assert Calibration timeout flag and do not update the BR counter reload value of calibration result. 0 = Disable 1 = Enable	0x00
6	rw	URT0_BKTMO_EN	UART Break timeout detection enable bit. When enables and Break condition has detected, chip will trigger time-out timer to start counting. After Break timeout detection, UART will assert Break timeout flag. 0 = Disable 1 = Enable	0x00
5	rw	URT0_RXTMO_EN	UART RX timeout enable bit for shadow buffer data loading into URTx_RDAT. When timeout happened and shadow buffer storing data >=1 byte, chip will load shadow buffer into URTx_RDAT register even though it is not over the receive threshold URTx_RX_TH. User can read data to speed process. 0 = Disable 1 = Enable	0x00
4	rw	URT0_IDTMO_EN	UART Idle timeout detection enable bit. When enables and Idle timeout has detected, UART will assert idle timeout flag. The time is starting after STOP bit of the last character. (for SmartCard maximum guard-time) 0 = Disable 1 = Enable	0x00
3..2	rw	URT0_TMO_MDS	UART timeout timer mode select. When selects general timer, the timer auto reload function is enabled and URTx_IDTMO_TH is used as the auto reload register. 0x0 = UART : UART timeout timer 0x1 = General : general using timer	0x00
1	rw	URT0_TMO_RST	UART timeout timer force reset enable. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
0	rw	URT0_TMO_EN	UART timeout timer enable. 0 = Disable 1 = Enable	0x00

1.19.18. URT0 timeout control register 2

URT0_TMOUT2	URT0 timeout control register 2		
Offset Address :	0x44	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT0_TMO_CNT[15:8]							
23	22	21	20	19	18	17	16
URT0_TMO_CNT[7:0]							
15	14	13	12	11	10	9	8
URT0_IDTMO_TH[15:8]							
7	6	5	4	3	2	1	0
URT0_IDTMO_TH[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	rw	URT0_TMO_CNT	UART timeout counter value.	0x0000
15..0	rw	URT0_IDTMO_TH	UART receive idle timeout detect threshold value by using receive bit time. The timeout threshold is starting after STOP	0x0000

			bit of the last character and value 1 indicates 1 bit time. When selects general timer in URTx_TMO_MDS, the timer auto reload function is enabled and URTx_IDTMO_TH is used as the auto reload register.	

1.19.19. URT0 SmartCard control register

URT0_SC	URT0 SmartCard control register		
Offset Address :	0x48	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	URT0_RXE_NUM[2:0]			Reserved	URT0_TXE_NUM[2:0]		
7	6	5	4	3	2	1	0
Reserved			URT0_RXE_LEN	URT0_TXE_MDS[1:0]		URT0_RXE_MDS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	-	Reserved	Reserved	0x00
14..12	rw	URT0_RXE_NUM	UART RX parity error detect and NACK transmission retry maximum number. When the register value >0, chip will retry to pull low on RX line and receive data. This register set the retry maximum number for continuous RX error retry. Value 0 indicates to disable hardware auto retry.	0x00
11	-	Reserved	Reserved	0x00
10..8	rw	URT0_TXE_NUM	UART TX error detect and data resend maximum number. When the register value >0, chip will resend the shift buffer data. This register set the resend maximum number for continuous TX error detection. Value 0 indicates to disable hardware auto resending.	0x00
7..5	-	Reserved	Reserved	0x00
4	rw	URT0_RXE_LEN	UART RX parity error detect and NACK transmission (pull low on RX line) bit time length select. 0x0 = 1Bit 0x1 = 2Bit	0x00
3..2	rw	URT0_TXE_MDS	UART TX error detect mode select. It must be noticed that the URTx_TX pin needs to set open-drain mode when enables the TX error detect function. 0x0 = Disable 0x1 = CHK_Low : check asserted low by RX device (for SmartCard) 0x2 = CHK_TX : check TX data by RX input data (for LIN mode) 0x3 = Reserved	0x00
1..0	rw	URT0_RXE_MDS	UART RX parity error detect control mode select. When enables and detects parity error, chip will pull low on RX line during STOP bit cycle and retry to receive new data but not assert interrupt. It must be noticed that the URTx_RX pin needs to set open-drain mode when enables the parity error detect function. Value 0 indicates to disable hardware auto retry. 0x0 = Disable 0x1 = Enable : hardware RX auto retry number by setting URTx_RXE_NUM 0x2 = Auto : hardware RX auto retry always unless receiving parity correct character	0x00

1.19.20. URT0 slave address detect register

URT0_SADR	URT0 slave address detect register		
Offset Address :	0x4C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
URT0_SA_MSK[7:0]							
7	6	5	4	3	2	1	0
URT0_SA_RX[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..8	rw	URT0_SA_MSK	UART multi-processor slave address mask register. URTx_SA_RX register is combined with URTx_SA_MSK register to form Given/Broadcast Address for automatic address recognition. In fact, URTx_SA_MSK functions as the 'mask' register for URTx_SA_RX register. The slave address is created by taking the logical OR of URTx_SA_RX and URTx_SA_MSK. Zero in this result is considered as 'don't care'. (Value 0x00 indicates to enter multi-processor monitor mode.)	0x00
7..0	rw	URT0_SA_RX	UART multi-processor mode received slave address. When URTx_MDS select multi-processor mode and URTx_SA_MSK=0x00, UART enter multi-processor monitor mode and the input slave address value can be read from URTx_RCAP register.	0x00

1.19.21. URT0 calibration control register

URT0_CAL	URT0 calibration control register		
Offset Address :	0x50	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				Reserved			
7	6	5	4	3	2	1	0
URT0_CALC_HE	Reserved	Reserved		URT0_CAL_MDS[1:0]		URT0_CAL_AUTO	URT0_CAL_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	-	Reserved	Reserved	0x00
11..8	-	Reserved	Reserved	0x00
7	rw	URT0_CALC_HE	UART auto baud-rate calibration complete data receive hold enable. When enables, the receive data will be hold from shift buffer to shadow buffer after auto baud-rate calibration complete. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5..4	-	Reserved	Reserved	0x00
3..2	rw	URT0_CAL_MDS	UART auto baud-rate calibration mode select. 0x0 = Start : measure the start bit	0x00

			0x1 = Edge : measure start falling edge to next falling edge 0x2 = Reserved 0x3 = Reserved	
1	rw	URT0_CAL_AUTO	UART Break detection and auto baud-rate calibration enable. When enables, hardware will auto enable baud-rate calibration after detect Break condition. When the calibration is finished and the URTx_CALCF is asserted. 0 = Disable 1 = Enable	0x00
0	rw	URT0_CAL_EN	UART baud-rate calibration enable. When enables, calibration will start after receive expected character. This bit will clear by hardware after calibration stop. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00

1.19.22. URT0 IrDA control register

URT0_IRDA	URT0 IrDA control register		
Offset Address :	0x54	Reset Value :	0x00000300

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved				URT0_IR_PW[3:0]			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved						URT0_IR_MDS	URT0_IR_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	-	Reserved	Reserved	0x00
11..8	rw	URT0_IR_PW	UART IrDA output pulse width select. IrDA pulse width = (URTx_IR_PW+1) * T<CK_URTx_TX>. The value needs small than URTx_TXOS_NUM. Note : (1) When URTx_IR_PW value equals URTx_TXOS_NUM value, the output is keep low during data bit cycle. (2) When URTx_IR_PW value is large URTx_TXOS_NUM value, the output is keep high during data bit cycle.	0x03
7..2	-	Reserved	Reserved	0x00
1	rw	URT0_IR_MDS	UART IrDA data received mode select. When selects Normal and over-sampling mode URTx_OS_MDS sets Three, the IrDA sampling sequence value need equal 000 then output bit value 0 and others output 1. When selects Wide and over-sampling mode URTx_OS_MDS sets Three, the IrDA sampling sequence value need equal 000,001,010,100 then output bit value 0 and others output 1. 0 = Normal 1 = Wide	0x00
0	rw	URT0_IR_EN	UART IrDA data format enable. When enables, the IrDA encoder and decoder enable for data stream. 0 = Disable 1 = Enable	0x00

1.19.23. URT0 hardware flow control register

URT0_HFC	URT0 hardware flow control register		
Offset Address :	0x58	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	URT0_RTS_OUT	URT0_RTS_INV	URT0_CTS_INV	URT0_RTS_EN	URT0_CTS_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	rw	URT0_RTS_OUT	URTx_RTS output control data bit. This bit is no effect when URTx_RTS_EN is set. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
3	rw	URT0_RTS_INV	URTx_RTS output inverse enable. When URTx_EN is disabled and the RTS output is set by URTx_RTS_OUT register, the bit does not affect the RTS output. 0 = Disable 1 = Enable	0x00
2	rw	URT0_CTS_INV	URTx_CTS input inverse enable. 0 = Disable 1 = Enable	0x00
1	rw	URT0_RTS_EN	UART RTS hardware flow control enable. When enables, URTx_RTS signal will output high if RX buffer is full. It will change URTx_RTS to low when RX buffer is not full or under threshold. 0 = Disable 1 = Enable	0x00
0	rw	URT0_CTS_EN	UART CTS hardware flow control enable. When enables, transmitter will hold data transmission and enter idle state if detect URTx_RTS signal high. It will automatically transmit next data when URTx_RTS change to low. 0 = Disable 1 = Enable	0x00

1.19.24. URT0 mute control register

URT0_MUTE	URT0 mute control register		
Offset Address :	0x5C	Reset Value :	0x00010100

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved					URT0_MUTE_AEX2	URT0_MUTE_AEX1	URT0_MUTE_AEX0
15	14	13	12	11	10	9	8
Reserved						URT0_MUTE_AEN1	URT0_MUTE_AEN0
7	6	5	4	3	2	1	0
Reserved							URT0_MUTE_EN

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..19	-	Reserved	Reserved	0x00
18	rw	URT0_MUTE_AEX2	UART auto exit mute mode and receive data by idle line detection enable bit. When UART enters mute mode and this bit enables, it will disable mute condition and exit mute mode if has	0x00

			detected the defined idle-line by setting threshold timer in URTx_DET_IDL. 0 = Disable 1 = Enable	
17	rw	**URT0_MUTE_AEX1**	UART auto exit mute mode and receive data by Break condition detection enable bit. When UART enters mute mode and this bit enables, it will disable mute condition and exit mute mode if has detected Break condition. 0 = Disable 1 = Enable	0x00
16	rw	**URT0_MUTE_AEX0**	UART auto exit mute mode and receive data by multi-processor slave address matched condition enable bit.. When UART enters mute mode and this bit enables, it will disable mute condition and exit mute mode if has received the defined address in URTx_SADR(URTx_MDS=0x2 or 0x3).(Default 1) 0 = Disable 1 = Enable	0x01
15..10	-	**Reserved**	Reserved	0x00
9	rw	**URT0_MUTE_AEN1**	UART mute mode auto enter by idle line detection enable bit. When enables auto mode, UART will enter mute mode after detect the defined idle-line by setting threshold timer in URTx_DET_IDL. 0 = Disable 1 = Enable	0x00
8	rw	**URT0_MUTE_AEN0**	UART mute mode auto enter by multi-processor slave address unmatched condition enable bit. When enables auto mode, UART will enter mute mode after received the unmatched address in URTx_SADR(URTx_MDS=0x2 or 0x3). 0 = Disable 1 = Enable	0x01
7..1	-	**Reserved**	Reserved	0x00
0	rw	**URT0_MUTE_EN**	UART mute mode enable. When enables, only receives the characters those are idle-line for multi-processor Idle-line mode , data with address bit for multi-processor Address-bit mode or break condition for UART auto calibration mode. Also, the non-address or non-break characters are not received and does not assert the URTx_RXF interrupt. If an address is received, user software can validate the address and reset this bit to continue receiving data. 0 = Disable 1 = Enable	0x00

1.19.25. URT0 Register Map

URT0 Register Map Register Number = 24

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	URT0_STA	Reserved	URT0_CALTMOF	URT0_BKTMOF	URT0_IDTMOF	URT0_RXTMOF	Reserved	URT0_TUDRF	URT0_TXEF	URT0_ROVRF	URT0_NCEF	URT0_FEF	URT0_PEF	Reserved	URT0_CTSF	URT0_IDLF	URT0_BKF	URT0_CALOVF	URT0_CALUDF	URT0_CALCF	URT0_TMOF	URT0_BRTF	URT0_SADRF	Reserved	Reserved	URT0_TXF	URT0_RXF	URT0_RXDF	URT0_LSF	URT0_ERRF	URT0_TCF	URT0_UGF	URT0_RHF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	URT0_INT	Reserved	URT0_CALTMO_IE	URT0_BKTMO_IE	URT0_IDTMO_IE	URT0_RXTMO_IE	Reserved	URT0_TUDR_IE	URT0_TXE_IE	URT0_ROVR_IE	URT0_NCE_IE	URT0_FE_IE	URT0_PE_IE	Reserved	URT0_CTS_IE	URT0_IDL_IE	URT0_BK_IE	Reserved		URT0_CALC_IE	URT0_TMO_IE	URT0_BRT_IE	URT0_SADR_IE	Reserved	Reserved	URT0_TX_IE	URT0_RX_IE	Reserved	URT0_LS_IE	URT0_ERR_IE	URT0_TC_IE	URT0_UG_IE	URT0_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	URT0_CLK	Reserved	URT0_BR_CKS	URT0_CKO_LCK	URT0_CKO_STA	URT0_BRO_LCK	URT0_BRO_STA	URT0_BR_MDS	URT0_BR_EN	Reserved		URT0_TX_CKS [1:0]		Reserved		URT0_RX_CKS [1:0]		Reserved								URT0_ECK_CKS	Reserved	URT0_CLK_CKS	URT0_CLK_EN	URT0_CK_SEL [2:0]			Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	URT0_STA2	Reserved	URT0_TX_LVL [2:0]			Reserved	URT0_RX_LVL [2:0]			Reserved								Reserved	Reserved	Reserved	URT0_CTS	Reserved		Reserved	Reserved	URT0_IR_BUSYF	URT0_BKBF	URT0_NCF	Reserved	Reserved	URT0_ADR	URT0_PAR	URT0_BUSYF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	URT0_CR0	URT0_DMA_TXEN	URT0_DMA_RXEN	URT0_DDTX_EN	Reserved	Reserved	Reserved		Reserved	URT0_LBM_EN	URT0_NCHAR_DIS	URT0_NCHAR_HE	URT0_IDL_MDS	Reserved		URT0_RX_TH[1:0]		URT0_DE_GT[1:0]		URT0_DE_INV	URT0_DE_EN	URT0_TX_INV	URT0_RX_INV	URT0_SYNC_MDS	URT0_IO_SWP	URT0_GSA_EN	URT0_MDS[2:0]			URT0_DAT_LINE	URT0_HDX_EN	URT0_OS_MDS	URT0_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	URT0_CR1	Reserved	Reserved		URT0_TXOS_NUM [4:0]					URT0_TXSTP_LEN [1:0]		URT0_TXMSB_EN	URT0_TXPAR_STK	URT0_TXPAR_POL	URT0_TXPAR_EN	URT0_TXDSIZE [1:0]		Reserved			URT0_RXOS_NUM [4:0]					URT0_RXSTP_LEN [1:0]		URT0_RXMSB_EN	URT0_RXPAR_STK	URT0_RXPAR_POL	URT0_RXPAR_EN	URT0_RXDSIZE [1:0]	
Reset	0x0F400F40	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
0x18	URT0_CR2	URT0_DOUT_IDL [1:0]		URT0_DOUT_MDS	Reserved	URT0_NSSI_EN	URT0_NSS_SWEN	URT0_NSS_INV	URT0_NSSI_INV	Reserved						URT0_NSS_SWI	URT0_NSS_SWO	Reserved								Reserved			URT0_TX_HALT	URT0_TX_EN	URT0_RX_EN	URT0_ADR_TX	URT0_BK_TX
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	URT0_CR3	Reserved								URT0_TXGT_LEN [7:0]								URT0_DET_IDL [7:0]								Reserved			URT0_DET_BK	Reserved	URT0_CPHA	URT0_CPOL	Reserved
Reset	0x00000A00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0

0x20	URT0_CR4	Reserved								Reserved								Reserved	URT0_TNUM[2:0]			Reserved	URT0_RNUM[2:0]			URT0_TDAT_CLR	URT0_RDAT_CLR	URT0_TDAT_INV	URT0_RDAT_INV	Reserved	Reserved	Reserved	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	URT0_RLR	Reserved																Reserved		URT0_PSR[5:0]						URT0_RLR[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	URT0_CNT	Reserved																Reserved		URT0_PSC[5:0]						URT0_CNT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	URT0_RCAP	Reserved																Reserved					URT0_RCAP_ADR	URT0_RCAP_PAR	URT0_RCAP_STP	URT0_RCAP_DAT [7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	URT0_RDAT	URT0_RDAT[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	URT0_TDAT	URT0_TDAT[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	URT0_TDAT3	Reserved								URT0_TDAT3[23:0]																							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	URT0_SBUF	Reserved																URT0_TSBUF[7:0]								URT0_RSBUF[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	URT0_TMOUT	URT0_CALTMO_TH [3:0]				URT0_BKTMO_TH [3:0]				URT0_RXTMO_TH [7:0]								URT0_TMO_LCK	URT0_TMO_STA	Reserved			URT0_TMO_CKS [2:0]			URT0_CALTMO_EN	URT0_BKTMO_EN	URT0_RXTMO_EN	URT0_IDTMO_EN	URT0_TMO_MDS [1:0]		URT0_TMO_RST	URT0_TMO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x44	URT0_TMOUT2	URT0_TMO_CNT [15:0]																URT0_IDTMO_TH [15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x48	URT0_SC	Reserved																Reserved	URT0_RXE_NUM [2:0]			Reserved	URT0_TXE_NUM [2:0]			Reserved			URT0_RXE_LEN	URT0_TXE_MDS [1:0]		URT0_RXE_MDS [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x4C	URT0_SADR	Reserved								Reserved								URT0_SA_MSK [7:0]								URT0_SA_RX[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	URT0_CAL	Reserved																Reserved				Reserved				URT0_CALC_HE	Reserved	Reserved		URT0_CAL_MDS [1:0]		URT0_CAL_AUTO	URT0_CAL_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x54	URT0_IRDA	Reserved																Reserved				URT0_IR_PW[3:0]				Reserved						URT0_IR_MDS	URT0_IR_EN
Reset	**0x00000300**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
0x58	URT0_HFC	Reserved																Reserved								Reserved	Reserved	Reserved	URT0_RTS_OUT	URT0_RTS_INV	URT0_CTS_INV	URT0_RTS_EN	URT0_CTS_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x5C	URT0_MUTE	Reserved								Reserved					URT0_MUTE_AEX2	URT0_MUTE_AEX1	URT0_MUTE_AEX0	Reserved						URT0_MUTE_AEN1	URT0_MUTE_AEN0	Reserved							URT0_MUTE_EN
Reset	**0x00010100**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

1.20. URT1 Control Registers

URT1 Control	(URT1) UART Control Module-1
Base Address :	0x52010000

1.20.1. URT1 status register 1

URT1_STA	URT1 status register 1		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	URT1_CALTMOF	URT1_BKTMOF	URT1_IDTMOF	URT1_RXTMOF	Reserved	URT1_TUDRF	URT1_TXEF
23	22	21	20	19	18	17	16
URT1_ROVRF	URT1_NCEF	URT1_FEF	URT1_PEF	Reserved	URT1_CTSF	URT1_IDLF	URT1_BKF
15	14	13	12	11	10	9	8
URT1_CALOVF	URT1_CALUDF	URT1_CALCF	URT1_TMOF	URT1_BRTF	URT1_SADRF	Reserved	Reserved
7	6	5	4	3	2	1	0
URT1_TXF	URT1_RXF	URT1_RXDF	URT1_LSF	URT1_ERRF	URT1_TCF	URT1_UGF	URT1_RHF

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	URT1_CALTMOF	UART auto baud-rate calibration sync field receive time-out time out flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
29	rw	URT1_BKTMOF	UART break receive time out flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
28	rw	URT1_IDTMOF	UART idle state time out flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
27	rw	URT1_RXTMOF	UART receive time out flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
26	-	Reserved	Reserved	0x00
25	rw	URT1_TUDRF	UART SPI slave mode transmit underrun flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
24	rw	URT1_TXEF	UART TX error detect flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of URTx_TXE_MDS for detail. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
23	rw	URT1_ROVRF	UART receive overrun error flag. (set by hardware and clear by software writing 1) When receive overrun, hardware will stop to receive next data into data shadow buffer until this flag is cleared. This flag is indicated for following two conditions. (1) When RX shadow buffer is arrived over the RX threshold and the data register has not read out. If shift buffer is filled of next data, this flag is asserted. (2) When Parity error, Frame error, Break detect or Slave-Address detect, has happened and caused RX shadow buffer input holding. If shift buffer is filled of next data, this flag is asserted. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
22	rw	URT1_NCEF	UART receive noised character error flag. (set by hardware	0x00

			and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	
21	rw	URT1_FEF	UART frame error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
20	rw	URT1_PEF	UART parity error flag. (set by hardware and clear by software writing 1) When multi-processor mode, the parity value is including of address bit. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19	-	Reserved	Reserved	0x00
18	rw	URT1_CTSF	UART CTS change detect interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	rw	URT1_IDLF	UART idle line detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
16	rw	URT1_BKF	UART break condition detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	r	URT1_CALOVF	UART auto baud-rate calibration overflow status flag. This flag is asserted when the baud-rate calibration counter is changed overflow during baud-rate calibration (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
14	r	URT1_CALUDF	UART auto baud-rate calibration underflow status flag. This flag is asserted when the baud-rate calibration counter is changed to zero during baud-rate calibration (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
13	rw	URT1_CALCF	UART auto baud-rate calibration complete flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
12	rw	URT1_TMOF	UART timeout timer timeout flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
11	rw	URT1_BRTF	UART baud-rate generator timer timeout flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
10	rw	URT1_SADRF	UART slave address matched flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	rw	URT1_TXF	UART transmit data register empty. (set by hardware and clear by hardware or software writing 1) When transmitted shadow buffer is empty and the data register URTx_TDAT will copy to the shadow buffer, this flag is set. This bit is cleared when URTx_TDAT is written or this flag set to 1 by software. The flag is set after UART reset or Idle state.	0x00

			0 = Normal (No event occurred) 1 = Happened (Event happened)	
6	rw	URT1_RXF	UART receive data register not empty. (set by hardware and clear by hardware or software writing 1) When received shadow buffer level URTx_RX_LVL is greater than or equal to the shadow buffer threshold URTx_RX_TH setting, this flag is set and the shadow buffer content copy to data register URTx_RDAT. This bit is cleared when URTx_RDAT is read or this flag set to 1 by software. But it does not be cleared when URTx_RDAT is read by SWD debugging. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	r	URT1_RXDF	UART received data byte number is different from previous received data byte number for URTx_RDAT register. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	URT1_LSF	UART line statue flag for break condition, idle line, CTS detect. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	URT1_ERRF	UART error interrupt flag for parity error, frame error, overrun error, receive time out and noise error. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	URT1_TCF	UART transmission complete flag. When both shadow buffer and data register are empty and shift buffer shift out complete, then set this flag. (set by hardware and clear by hardware or software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	rw	URT1_UGF	UART general event flag. It indicates each of URTx_SADRF , URTx_BRTF , URTx_TMOF or URTx_CALCF flag is asserted when this flag is set. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	rw	URT1_RHF	UART receive hold flag. It indicates one of hardware hold event is happened when this flag is set. In the condition, the shift buffer is held and do not load data to shadow buffer until this bit is cleared. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00

1.20.2. URT1 interrupt enable register

URT1_INT	URT1 interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	URT1_CALTMO_IE	URT1_BKTMO_IE	URT1_IDTMO_IE	URT1_RXTMO_IE	Reserved	URT1_TUDR_IE	URT1_TXE_IE
23	22	21	20	19	18	17	16
URT1_ROVR_IE	URT1_NCE_IE	URT1_FE_IE	URT1_PE_IE	Reserved	URT1_CTS_IE	URT1_IDL_IE	URT1_BK_IE
15	14	13	12	11	10	9	8
Reserved		URT1_CALC_IE	URT1_TMO_IE	URT1_BRT_IE	URT1_SADR_IE	Reserved	Reserved
7	6	5	4	3	2	1	0
URT1_TX_IE	URT1_RX_IE	Reserved	URT1_LS_IE	URT1_ERR_IE	URT1_TC_IE	URT1_UG_IE	URT1_IEA

Bit	Attr	Bit Name	Description	Reset

31	-	Reserved	Reserved	0x00
30	rw	URT1_CALTMO_IE	UART auto baud-rate calibration sync field receive time-out time out interrupt enable. 0 = Disable 1 = Enable	0x00
29	rw	URT1_BKTMO_IE	UART break receive time out interrupt enable. 0 = Disable 1 = Enable	0x00
28	rw	URT1_IDTMO_IE	UART idle state time out interrupt enable. 0 = Disable 1 = Enable	0x00
27	rw	URT1_RXTMO_IE	UART receive time out interrupt enable. 0 = Disable 1 = Enable	0x00
26	-	Reserved	Reserved	0x00
25	rw	URT1_TUDR_IE	UART SPI slave mode transmit underrun interrupt enable. 0 = Disable 1 = Enable	0x00
24	rw	URT1_TXE_IE	UART TX error detect interrupt enable. Refer to the register descriptions of URTx_TXE_MDS for detail. 0 = Disable 1 = Enable	0x00
23	rw	URT1_ROVR_IE	UART receive overrun error interrupt enable. Refer to the register descriptions of URTx_ROVRF for the detail. 0 = Disable 1 = Enable	0x00
22	rw	URT1_NCE_IE	UART receive noised character interrupt enable. 0 = Disable 1 = Enable	0x00
21	rw	URT1_FE_IE	UART frame error interrupt enable. 0 = Disable 1 = Enable	0x00
20	rw	URT1_PE_IE	UART parity error interrupt enable. 0 = Disable 1 = Enable	0x00
19	-	Reserved	Reserved	0x00
18	rw	URT1_CTS_IE	UART CTS change detect interrupt enable. 0 = Disable 1 = Enable	0x00
17	rw	URT1_IDL_IE	UART idle line detect interrupt enable. 0 = Disable 1 = Enable	0x00
16	rw	URT1_BK_IE	UART break condition detect interrupt enable. 0 = Disable 1 = Enable	0x00
15..14	-	Reserved	Reserved	0x00
13	rw	URT1_CALC_IE	UART auto baud-rate calibration complete interrupt enable. 0 = Disable 1 = Enable	0x00
12	rw	URT1_TMO_IE	UART timeout timer timeout interrupt enable. 0 = Disable 1 = Enable	0x00
11	rw	URT1_BRT_IE	UART baud-rate generator timer timeout interrupt enable. 0 = Disable 1 = Enable	0x00
10	rw	URT1_SADR_IE	UART slave address matched interrupt enable. 0 = Disable 1 = Enable	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00

7	rw	URT1_TX_IE	UART transmit data register empty interrupt enable. Refer to the register descriptions of URTx_TXF for the detail. 0 = Disable 1 = Enable	0x00
6	rw	URT1_RX_IE	UART receive data register not empty interrupt enable. Refer to the register descriptions of URTx_RXF for the detail. 0 = Disable 1 = Enable	0x00
5	-	Reserved	Reserved	0x00
4	rw	URT1_LS_IE	UART line statue flag for break condition, idle line, CTS detect. 0 = Disable 1 = Enable	0x00
3	rw	URT1_ERR_IE	UART error interrupt enable for parity error, frame error, overrun error, receive time out and noise error. 0 = Disable 1 = Enable	0x00
2	rw	URT1_TC_IE	UART transmission complete interrupt enable.　(set by hardware and clear by hardware or software writing 1) 0 = Disable 1 = Enable	0x00
1	rw	URT1_UG_IE	UART general event interrupt enable for URTx_SADRF , URTx_TF , URTx_RCNTF or URTx_TCNTF events. 0 = Disable 1 = Enable	0x00
0	rw	URT1_IEA	UART interrupt all enable. When disables, the UART global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.20.3. URT1 clock source register

URT1_CLK	URT1 clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	URT1_BR_CKS	URT1_CKO_LCK	URT1_CKO_STA	URT1_BRO_LCK	URT1_BRO_STA	URT1_BR_MDS	URT1_BR_EN
23	22	21	20	19	18	17	16
Reserved		URT1_TX_CKS[1:0]		Reserved		URT1_RX_CKS[1:0]	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
URT1_ECK_CKS	Reserved	URT1_CLK_CKS	URT1_CLK_EN	URT1_CK_SEL[2:0]			Reserved

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	URT1_BR_CKS	UART baud-rate timer clock source select. 0 = PSC : CK_URTx_PSC from clock prescaler output 1 = CK_URTx : CK_URTx from UART internal clock input	0x00
29	rw	URT1_CKO_LCK	UART PSC clock output signal initial state control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	0x00
28	rw	URT1_CKO_STA	UART PSC clock output signal initial state. The bit is written effectively only by written 1 to URTx_CKO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
27	rw	URT1_BRO_LCK	UART baud-rate timer timeout signal initial state control. When	0x00

			locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	
26	rw	**URT1_BRO_STA**	UART baud-rate timer timeout signal initial state. The bit is written effectively only by written 1 to URTx_BRO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
25	rw	**URT1_BR_MDS**	UART baud-rate timer mode select. Combined mode is only using for general purpose counter. When SmartCard mode, this bit need set to 'Separated' for SmartCard clock output from PSC output. 0 = Separated : Separated PSC and CNT counters for UART baud-rate generator 1 = Combined : Combine to a linear counter for general using timer	0x00
24	rw	**URT1_BR_EN**	UART baud-rate timer enable. When enables, the baud-rate timer 0 = Disable 1 = Enable	0x00
23..22	-	**Reserved**	Reserved	0x00
21..20	rw	**URT1_TX_CKS**	UART transmission clock source select. 0x0 = Internal : UART internal clock source CK_URTx_INT 0x1 = TM01_TRGO 0x2 = TM10_TRGO 0x3 = EXT_CLK (external clock from URTx_CLK pin)	0x00
19..18	-	**Reserved**	Reserved	0x00
17..16	rw	**URT1_RX_CKS**	UART receive clock source select. 0x0 = Internal : UART internal clock source CK_URTx_INT 0x1 = TM01_TRGO 0x2 = TM10_TRGO 0x3 = EXT_CLK (external clock from URTx_CLK pin)	0x00
15..8	-	**Reserved**	Reserved	0x00
7	rw	**URT1_ECK_CKS**	UART external clock IO select. When select 'RX', the external clock is connected to the selected signal which is selected from URTx_RX or URTx_TX by URTx_IO_SWAP. 0 = CLK : URTx_CLK pin 1 = RX : receiving signal	0x00
6	-	**Reserved**	Reserved	0x00
5	rw	**URT1_CLK_CKS**	UART external clock output source select. 0 = OUT : CK_URTx_OUT from clock output divider 1 = SC : CK_URTx_SC from clock input prescaler	0x00
4	rw	**URT1_CLK_EN**	URTx_CLK signal output enable. 0 = Disable 1 = Enable	0x00
3..1	rw	**URT1_CK_SEL**	UART internal clock CK_URTx source select. 0x0 = PROC : CK_URTx_PR process clock from CSC 0x1 = NCO_P0 0x2 = CK_LS 0x3 = TM00_TRGO 0x4 = EXT_CLK (external clock from URTx_ECK signal)	0x00
0	-	**Reserved**	Reserved	0x00

1.20.4. URT1 status register 2

URT1_STA2	**URT1 status register 2**		
Offset Address :	**0x0C**	**Reset Value :**	**0x00000000**

31	30	29	28	27	26	25	24

Reserved	URT1_TX_LVL[2:0]			Reserved	URT1_RX_LVL[2:0]		
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	URT1_CTS	Reserved		Reserved	Reserved
7	6	5	4	3	2	1	0
URT1_IR_BUSYF	URT1_BKBF	URT1_NCF	Reserved	Reserved	URT1_ADR	URT1_PAR	URT1_BUSYF

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30..28	r	URT1_TX_LVL	UART data buffer transmission remained level indications. 0x0 = 0 (0-byte,empty) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	0x00
27	-	Reserved	Reserved	0x00
26..24	r	URT1_RX_LVL	UART data buffer received level indications. 0x0 = 0 (0-byte,empty) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	0x00
23..16	-	Reserved	Reserved	0x00
15	-	Reserved	Reserved	0x00
14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	r	URT1_CTS	UART CTS line status bit. This bit reflects the CTS line status which is the watched point behind the CTS input inverter.	0x00
11..10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	r	URT1_IR_BUSYF	UART IrDA data received busy flag. 0 = No (No IrDA signal detect) 1 = Busy (detect some IrDA signal)	0x00
6	r	URT1_BKBF	UART send break busy flag. (set and clear by hardware) 0 = Normal (No break transmitted or transmit finished) 1 = Busy (Event happened)	0x00
5	r	URT1_NCF	UART receive noised character flag. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	-	Reserved	Reserved	0x00
3	-	Reserved	Reserved	0x00
2	r	URT1_ADR	UART data receive slave address bit of shift buffer.	0x00
1	r	URT1_PAR	UART data receive parity bit of shift buffer. When multi-processor mode, the parity value is including of address bit.	0x00
0	r	URT1_BUSYF	UART RX busy flag. (set and clear by hardware) When detect valid start bit, this bit is set and clear after stop bit. 0 = Normal (No event occurred) 1 = Busy (Event happened)	0x00

1.20.5. URT1 control register 0

URT1_CR0	URT1 control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT1_DMA_TXEN	URT1_DMA_RXEN	URT1_DDTX_EN	Reserved	Reserved	Reserved		Reserved
23	22	21	20	19	18	17	16

URT1_LBM_EN	URT1_NCHAR_DIS	URT1_NCHAR_HE	URT1_IDL_MDS	Reserved		URT1_RX_TH[1:0]	
15	14	13	12	11	10	9	8
URT1_DE_GT[1:0]		URT1_DE_INV	URT1_DE_EN	URT1_TX_INV	URT1_RX_INV	URT1_SYNC_MDS	URT1_IO_SWP
7	6	5	4	3	2	1	0
URT1_GSA_EN	URT1_MDS[2:0]			URT1_DAT_LINE	URT1_HDX_EN	URT1_OS_MDS	URT1_EN

Bit	Attr	Bit Name	Description	Reset
31	rw	URT1_DMA_TXEN	Direct memory access enable to transmit. When enables, hardware can receive the data from DMA and transmit to output. This bit is enabled to write if URTx_TX_EN=0. 0 = Disable 1 = Enable	0x00
30	rw	URT1_DMA_RXEN	Direct memory access enable to receive. When enables, hardware can receive the data from input and send to DMA. This bit is enabled to write if URTx_RX_EN=0. 0 = Disable 1 = Enable	0x00
29	rw	URT1_DDTX_EN	Hardware force to disable DMA TX function enable bit when detects a break condition. When enables, hardware will disable the URTx_DMA_TXEN bit if hardware detects a break condition. Also, the URTx_DMA_RXEN bit is disabled in this condition. When disables, hardware will keep to do DMA TX function if hardware detects a break condition. 0 = Disable 1 = Enable	0x00
28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26..25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23	rw	URT1_LBM_EN	UART loop back mode enable bit. When enables, the received input is taken from transmitted output to replace from input pin(RX ->TX ,CTS -> RTS). 0 = Disable 1 = Enable	0x00
22	rw	URT1_NCHAR_DIS	UART receiving noised character disable bit. When disables, the received noised character is skipped and does not assert the URTx_RXF interrupt. Also the noised character will copy to URTx_RCAP data register. When enables, the noised character is accepted for receiving. 0 = Enable (Accept noised character) 1 = Disable (Skip noised character)	0x00
21	rw	URT1_NCHAR_HE	UART receiving hold enable bit if receives a noised character. This bit is no effect when URTx_NCHAR_DIS=0. When enables and URTx_NCHAR_DIS=1, the received data will be hold from shift buffer to shadow buffer and the URTx_RHF will be active after received noised character. Until the URTx_RHF is cleared, chip will release the hold function. 0 = Disable 1 = Enable	0x00
20	rw	URT1_IDL_MDS	UART idle line detect management mode select. When selects 'Load' and detects idle line, chip will load shadow buffer into URTx_RDAT register even though it is not over the receive threshold URTx_RX_TH if shadow buffer is not empty. 0 = No (No operation) 1 = Load (Force to load shadow buffer)	0x00
19..18	-	Reserved	Reserved	0x00
17..16	rw	URT1_RX_TH	UART data buffer high threshold for received access. This register will set to '0' (1byte) and is no effect for register written if UART1_DMA_RXEN is enabled. 0x0 = 1byte (default) 0x1 = 2byte	0x00

			0x2 = 3byte 0x3 = 4byte	
15..14	rw	URT1_DE_GT	URTx_DE signal output guard time select by unit of bit time. The selection set both asserted time before START bit and deasserted time after last STOP bit. 0x0 = 1/4 0x1 = 1/2 0x2 = 1 0x3 = 2	0x00
13	rw	URT1_DE_INV	URTx_DE signal inverse enable. The hardware DE output default is low level. 0 = Disable 1 = Enable	0x00
12	rw	URT1_DE_EN	URTx_DE signal output enable. 0 = Disable 1 = Enable	0x00
11	rw	URT1_TX_INV	URTx_TX output signal inverse enable. 0 = Disable 1 = Enable	0x00
10	rw	URT1_RX_INV	URTx_RX input signal inverse enable. 0 = Disable 1 = Enable	0x00
9	rw	URT1_SYNC_MDS	UART SYNC mode(SPI) select. 0 = Master : SPI Master 1 = Slave : SPI Slave	0x00
8	rw	URT1_IO_SWP	URTx_RX/URTx_TX swap enable bit. 0 = Disable 1 = Enable	0x00
7	rw	URT1_GSA_EN	UART multi-processor global slave address enable.	0x00
6..4	rw	URT1_MDS	UART mode select. The Idle-line and Address-bit modes are using for multi-processor control. When selects IDLE or ADR mode, both URTx_MUTE_AEN0 and URTx_MUTE_AEX0 must be enabled. 0x0 = UART : UART mode 0x1 = SYNC : Synchronous/Shift-Register mode 0x2 = IDLE : Idle-line mode for multi-processor 0x3 = ADR : Address-bit mode for multi-processor	0x00
3	rw	URT1_DAT_LINE	UART communication data line select. 0 = 2 : 2-lines separated ~ URTx_RX , URTx_TX 1 = 1 : 1-line Bidirectional ~URTx_TX only.	0x00
2	rw	URT1_HDX_EN	UART Half-duplex mode enable. When enables and UART is during transmission data, the URTx_RX input is no using and the data does not transfer into shadow buffer. 0 = Disable 1 = Enable	0x00
1	rw	URT1_OS_MDS	UART RX data oversampling majority vote select. 0 = Three : Three sample bits method 1 = One : One sample bit method and noise free	0x00
0	rw	URT1_EN	UART function enable bit. 0 = Disable 1 = Enable	0x00

1.20.6. URT1 control register 1

URT1_CR1	URT1 control register 1		
Offset Address :	0x14	Reset Value :	0x0F400F40

31	30	29	28	27	26	25	24
Reserved	Reserved		URT1_TXOS_NUM[4:0]				
23	22	21	20	19	18	17	16

URT1_TXSTP_LEN[1:0]		URT1_TXMSB_EN	URT1_TXPAR_STK	URT1_TXPAR_POL	URT1_TXPAR_EN	URT1_TXDSIZE[1:0]	
15	14	13	12	11	10	9	8
Reserved			URT1_RXOS_NUM[4:0]				
7	6	5	4	3	2	1	0
URT1_RXSTP_LEN[1:0]		URT1_RXMSB_EN	URT1_RXPAR_STK	URT1_RXPAR_POL	URT1_RXPAR_EN	URT1_RXDSIZE[1:0]	

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30..29	-	Reserved	Reserved	0x00
28..24	rw	URT1_TXOS_NUM	UART TX data oversampling samples select. When selects SYNC Master mode, the valid value is from 1 to 31 for oversampling number from 2 to 32. When selects other modes, the valid value is from 3 to 31 for oversampling samples from 4 to 32. (This register is written no effect if UART_TX_EN set 1.)	0x0F
23..22	rw	URT1_TXSTP_LEN	UART TX stop bit length select. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = 0.5bit 0x1 = 1bit 0x2 = 1.5bit 0x3 = 2bit	0x01
21	rw	URT1_TXMSB_EN	UART TX data order Msb first enable. When disables , the Lsb bit will be the first bit. (This register is written no effect if URTx_TX_EN set 1.) 0 = Disable 1 = Enable	0x00
20	rw	URT1_TXPAR_STK	UART stuck parity bit output enable. When enables and URTx_TXPAR_EN=1, parity bit output fixed value by URTx_TXPAR_POL value setting. 0 = Disable 1 = Enable	0x00
19	rw	URT1_TXPAR_POL	UART TX parity bit polarity. This bit is no effect for SPI and SYNC mods. 0x0 = Even 0x1 = Odd	0x00
18	rw	URT1_TXPAR_EN	UART TX parity bit enable. This bit does not be set for SYNC mods. (This register is written no effect if URTx_TX_EN set 1.) 0 = Disable 1 = Enable	0x00
17..16	rw	URT1_TXDSIZE	UART TX data bit length. It is not including START, STOP, ADR or PARITY bits. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = 8bit 0x1 = 7bit 0x2 = Reserved 0x3 = Reserved	0x00
15..13	-	Reserved	Reserved	0x00
12..8	rw	URT1_RXOS_NUM	UART RX data oversampling samples select. When selects SYNC Master mode, the valid value is from 1 to 31 for oversampling number from 2 to 32. When selects other modes, the valid value is from 3 to 31 for oversampling samples from 4 to 32. (This register is written no effect if UART_RX_EN set 1.)	0x0F
7..6	rw	URT1_RXSTP_LEN	UART RX stop bit length select. (This register is written no effect if URTx_RX_EN set 1.) 0x0 = 0.5bit 0x1 = 1bit 0x2 = 1.5bit 0x3 = 2bit	0x01
5	rw	URT1_RXMSB_EN	UART RX data order Msb first enable. When disables , the Lsb bit will be the first bit. (This register is written no effect if URTx_RX_EN set 1.) 0 = Disable	0x00

			1 = Enable	
4	rw	**URT1_RXPAR_STK**	UART stuck parity bit input enable. When enables and URTx_RXPAR_EN=1, parity bit input fixed value by URTx_RXPAR_POL value setting. 0 = Disable 1 = Enable	0x00
3	rw	**URT1_RXPAR_POL**	UART RX parity bit polarity. This bit is no effect for SYNC mods. 0x0 = Even 0x1 = Odd	0x00
2	rw	**URT1_RXPAR_EN**	UART RX parity bit enable. This bit does not be set for SYNC mods. (This register is written no effect if URTx_RX_EN set 1.) 0 = Disable 1 = Enable	0x00
1..0	rw	**URT1_RXDSIZE**	UART RX data bit length. It is not including START, STOP, ADR or PARITY bits. This bit is no effect for SPI and SYNC mods. (This register is written no effect if URTx_RX_EN set 1.) 0x0 = 8bit 0x1 = 7bit 0x2 = Reserved 0x3 = Reserved	0x00

1.20.7. URT1 control register 2

URT1_CR2	URT1 control register 2		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT1_DOUT_IDL[1:0]		URT1_DOUT_MDS	Reserved	URT1_NSSI_EN	URT1_NSS_SWEN	URT1_NSS_INV	URT1_NSSI_INV
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved						URT1_NSS_SWI	URT1_NSS_SWO
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			URT1_TX_HALT	URT1_TX_EN	URT1_RX_EN	URT1_ADR_TX	URT1_BK_TX

Bit	Attr	Bit Name	Description	Reset
31..30	rw	**URT1_DOUT_IDL**	UART SPI mode idle state data output value. When SPI master mode URTx_DOUT_MDS is enabled, the URTx_TX output is with driving during idle state and the output level is set by this bit. 0x0 = LBIT (Last data bit) 0x1 = Reserved 0x2 = 0 (Output 0) 0x3 = 1 (Output 1)	0x00
29	rw	**URT1_DOUT_MDS**	UART SPI master standard mode idle state data output mode select. When disables and data transfers during idle state, the MOSI will output with tristate for master mode. When enables and data transfers during idle state, the MOSI will output with driving for master mode. 0 = Disable : Output with tristate 1 = Enable : Output with driving	0x00
28	-	**Reserved**	Reserved	0x00
27	rw	**URT1_NSSI_EN**	UART NSS signal input function enable when UART configure to synchronous mode SPI Slave. 0 = Disable 1 = Enable	0x00
26	rw	**URT1_NSS_SWEN**	UART NSS signal output use software control bit enable. 0 = Disable 1 = Enable	0x00
25	rw	**URT1_NSS_INV**	UART NSS output signal inverse enable. The hardware NSS	0x00

			output default is low active level. 0 = Disable 1 = Enable	
24	rw	URT1_NSSI_INV	UART NSS input signal inverse enable. 0 = Disable 1 = Enable	0x00
23..18	-	Reserved	Reserved	0x00
17	r	URT1_NSS_SWI	UART NSS signal software input status bit.	0x00
16	rw	URT1_NSS_SWO	UART NSS signal software output control bit when URTx_NSS_SWEN is disable.	0x00
15..8	-	Reserved	Reserved	0x00
7..5	-	Reserved	Reserved	0x00
4	rw	URT1_TX_HALT	UART transmitter halt enable. 0 = Disable 1 = Enable	0x00
3	rw	URT1_TX_EN	UART transmitter enable. 0 = Disable 1 = Enable	0x00
2	rw	URT1_RX_EN	UART receiver enable. When URTx_MDS selects SYNC mode and URTx_DAT_LINE sets 1-line, enables this bit is used to set receiver mode only and disables this bit is used to set transmission mode only. 0 = Disable 1 = Enable	0x00
1	rw	URT1_ADR_TX	UART slave address for next data transmitted. This bit will clear by hardware after slave address sending end. If this bit and URTx_BK_TX are both set to 1, only the URTx_BK_TX function is action. Refer the URTx_TXGT_LEN register descriptions for more information. (set by software and clear by hardware) 0 = Normal 1 = Send : Send Address	0x00
0	rw	URT1_BK_TX	UART break condition for next data transmitted. This bit will clear by hardware after break condition sending end. If this bit and URTx_ADR_TX are both set to 1, only the URTx_BK_TX function is action. (set by software and clear by hardware) 0 = Normal 1 = Send : Send Break	0x00

1.20.8. URT1 control register 3

URT1_CR3	URT1 control register 3		
Offset Address :	0x1C	Reset Value :	0x00000A00

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT1_TXGT_LEN[7:0]							
15	14	13	12	11	10	9	8
URT1_DET_IDL[7:0]							
7	6	5	4	3	2	1	0
Reserved			URT1_DET_BK	Reserved	URT1_CPHA	URT1_CPOL	Reserved

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	rw	URT1_TXGT_LEN	UART TX guard time or idle-line length. (1)URTx_MDS=UART,SYNC,ADR modes: This register use as TX guard time between adjacent characters' transmission in the unit of bit time. The time is starting after STOP bit of the last character. Value 0 indicates 0 bit time. (for SmartCard	0x00

			minimum guard-time, counting start at Start bit = 12+{0~254} bit time) (2)URTx_MDS=IDLE mode: This register use as the idle-line length in the unit of bit time.	
15..8	rw	URT1_DET_IDL	UART idle line detect threshold value by using receive bit time. The timeout threshold is starting after STOP bit of the last character and value 1 indicates 2 bit time. The value 0 is invalid.	0x0A
7..5	-	Reserved	Reserved	0x00
4	rw	URT1_DET_BK	UART bit time select for break detection or transmission. For data receiving, the detect time is a character time plus this value after last STOP bit cycle. For data transmission, the break generation guard time is a character time plus this value+3 bit time. 0x0 = 1Bit 0x1 = 3Bit	0x00
3	-	Reserved	Reserved	0x00
2	rw	URT1_CPHA	UART clock phase select. It is used to select the data sampling on leading edge or trailing edge of SPI clock. 0 = Leading edge 1 = Trailing edge	0x00
1	rw	URT1_CPOL	UART clock polarity select. It is used to select the SPI clock level in idle state. 0 = Low 1 = High	0x00
0	-	Reserved	Reserved	0x00

1.20.9. URT1 control register 4

URT1_CR4	URT1 control register 4		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	URT1_TNUM[2:0]			Reserved	URT1_RNUM[2:0]		
7	6	5	4	3	2	1	0
URT1_TDAT_CLR	URT1_RDAT_CLR	URT1_TDAT_INV	URT1_RDAT_INV	Reserved			

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15	-	Reserved	Reserved	0x00
14..12	r	URT1_TNUM	UART remained data byte number in data register. Value 0~4 is valid only. 0x0 = 0 (0-byte) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	0x00
11	-	Reserved	Reserved	0x00
10..8	rw	URT1_RNUM	UART received data byte number when data shadow buffer last transfer to URTx_RDAT register. Firmware can write an initial value for received byte number comparison for URTx_RXDF status bit. Value 0~4 is valid only. 0x0 = 0 (0-byte) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte)	0x00

			0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	
7	w	**URT1_TDAT_CLR**	UART transmitted data clear enable. When enables, the transmitted data buffer will be flushed and URTx_TXF flag is set. Also URTx_TNUM and URTx_TX_LVL are cleared. It allows discarding the data when data has not been send under NACK error and frame error is active for SmartCard mode. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
6	w	**URT1_RDAT_CLR**	UART received data clear enable. When enables, the received data buffer will be flushed and URTx_RXF flag is cleared. Also URTx_RNUM and URTx_RX_LVL are cleared. It allows discarding the data without reading it and avoid a data overrun condition. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
5	rw	**URT1_TDAT_INV**	UART inverse transmitted data enable. When enables, the transmitted data bits are inverted but Start, Stop, Address and Parity bits are not inverted. 0 = Disable 1 = Enable	0x00
4	rw	**URT1_RDAT_INV**	UART inverse received data enable. When enables, the received data bits are inverted but Start, Stop, Address and Parity bits are not inverted. 0 = Disable 1 = Enable	0x00
3..0	-	**Reserved**	Reserved	0x00

1.20.10. URT1 baud-rate clock counter reload register

URT1_RLR	URT1 baud-rate clock counter reload register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved		URT1_PSR[5:0]					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
URT1_RLR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..14	-	**Reserved**	Reserved	0x00
13..8	rw	**URT1_PSR**	UART baud-rate clock prescaler reload register. Actual value equals the register value plus one.	0x00
7..0	rw	**URT1_RLR**	UART baud-rate clock counter reload register. Actual value equals the register value plus one.	0x00

1.20.11. URT1 baud-rate clock counter register

URT1_CNT	URT1 baud-rate clock counter register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							

15	14	13	12	11	10	9	8
Reserved		URT1_PSC[5:0]					
7	6	5	4	3	2	1	0
URT1_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..8	r	URT1_PSC	UART baud-rate clock prescaler value register.	0x00
7..0	r	URT1_CNT	UART baud-rate clock counter value register.	0x00

1.20.12. URT1 RX data capture register

URT1_RCAP	URT1 RX data capture register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved					URT1_RCAP_ADR	URT1_RCAP_PAR	URT1_RCAP_STP
7	6	5	4	3	2	1	0
URT1_RCAP_DAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..11	-	Reserved	Reserved	0x00
10	rw	URT1_RCAP_ADR	UART capture address bit from RX shift buffer.	0x00
9	rw	URT1_RCAP_PAR	UART capture parity bit from RX shift buffer.	0x00
8	rw	URT1_RCAP_STP	UART capture stop bit from RX shift buffer.	0x00
7..0	rw	URT1_RCAP_DAT	UART capture data from RX shift buffer for Parity error / Frame error / Break detect / Slave-Address detect matched / Calibration Sync Character / Noise Character. The capture function is disabled for synchronous mode. The capture data is affected by data order Msb first setting in URTx_RXMSB_EN. But it not affected by received data inverse setting in URTx_RDAT_INV.	0x00

1.20.13. URT1 RX data register

URT1_RDAT	URT1 RX data register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT1_RDAT[31:24]							
23	22	21	20	19	18	17	16
URT1_RDAT[23:16]							
15	14	13	12	11	10	9	8
URT1_RDAT[15:8]							
7	6	5	4	3	2	1	0
URT1_RDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	URT1_RDAT	UART received data register. Read this register will clear the URTx_RXF. Hardware will force to logic 0 for non-updated byte(s) by URTx_RX_TH setting.	0x00000000

1.20.14. URT1 TX data register

URT1_TDAT	URT1 TX data register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT1_TDAT[31:24]							
23	22	21	20	19	18	17	16
URT1_TDAT[23:16]							
15	14	13	12	11	10	9	8
URT1_TDAT[15:8]							
7	6	5	4	3	2	1	0
URT1_TDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	URT1_TDAT	UART transmitted data register. Write this register will clear the URTx_TXF. When write data by word, half-word or byte operation, chip will transfer 4-byte, 2-byte, or 1-byte data to shadow buffer. (write-only)	0x00000000

1.20.15. URT1 TX data 3-byte register

URT1_TDAT3	URT1 TX data 3-byte register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT1_TDAT3[23:16]							
15	14	13	12	11	10	9	8
URT1_TDAT3[15:8]							
7	6	5	4	3	2	1	0
URT1_TDAT3[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..0	w	URT1_TDAT3	UART transmitted data register for 3-byte data write only. Write this register will clear the URTx_TXF and force to transfer all 24-bit data to shadow buffer. This register is only allowed to access by a 32-bit word instruction.	0x000000

1.20.16. URT1 data shift buffer register

URT1_SBUF	URT1 data shift buffer register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
URT1_TSBUF[7:0]							
7	6	5	4	3	2	1	0
URT1_RSBUF[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	r	URT1_TSBUF	UART TX data shift buffer register.	0x00
7..0	r	URT1_RSBUF	UART RX data shift buffer register.	0x00

1.20.17. URT1 timeout control register

URT1_TMOUT	URT1 timeout control register		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT1_CALTMO_TH[3:0]				URT1_BKTMO_TH[3:0]			
23	22	21	20	19	18	17	16
URT1_RXTMO_TH[7:0]							
15	14	13	12	11	10	9	8
URT1_TMO_LCK	URT1_TMO_STA	Reserved			URT1_TMO_CKS[2:0]		
7	6	5	4	3	2	1	0
URT1_CALTMO_EN	URT1_BKTMO_EN	URT1_RXTMO_EN	URT1_IDTMO_EN	URT1_TMO_MDS[1:0]		URT1_TMO_RST	URT1_TMO_EN

Bit	Attr	Bit Name	Description	Reset
31..28	rw	URT1_CALTMO_TH	UART calibration timeout detect threshold value for TMO counter value comparison. When the TMO counter over the threshold, the calibration timeout is happened. The timeout threshold equals (register value)*BASE. When URT0_BR_MDS sets 'Separated', the BASE value is 0x10 and value 0 indicates counter overflow value 0xFF. When URT0_BR_MDS sets 'Combined', the BASE value is 0x100 and value 0 indicates counter overflow value 0xFFF. When calibration has finished, the TMO counter value will be copied to update the baud-rate generator BRO timer. If calibration timeout is happened, the BRO timer will keep the old baud-rate setting.	0x00
27..24	rw	URT1_BKTMO_TH	UART receive Break timeout detect threshold value by using receive bit time. The timeout threshold is starting after URTx_BKF bit asserting when hardware detect a Break character. Value 0 indicates 1 bit time.	0x00
23..16	rw	URT1_RXTMO_TH	UART RX data buffer timeout detect threshold value by using receive bit time. The timeout threshold is starting after STOP bit of the last character. The timeout threshold equal (register value+1)*8 (receive bit time) and value 0 indicates 8 bits time.	0x00
15	rw	URT1_TMO_LCK	UART timeout timer timeout signal initial state control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	0x00
14	rw	URT1_TMO_STA	UART timeout timer timeout signal initial state. The bit is written effectively only by written 1 to URTx_TMO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
13..11	-	Reserved	Reserved	0x00
10..8	rw	URT1_TMO_CKS	UART timeout timer clock source select. When URTx_TMO_MDS selects 'UART' mode, this register must select CK_URTx_BIT(UART) as TMO timer clock for normal operation. When selects 'Noise' and sets URTx_TMO_EN=1, the number of received noise bit is able to read from URTx_TMO_CNT. 0x0 = UART (CK_URTx_BIT clock) 0x1 = Input (CK_UART clock input) 0x2 = Noise (Noise bit receive event) 0x3 = Reserved	0x00
7	rw	URT1_CALTMO_EN	UART Calibration timeout detection enable bit. When enables and URTx_CAL_AUTO=1 if Break condition has detected, chip will trigger timer-out timer to start counting. After the Calibration timeout detection and the corrected auto-sync-field has not received, UART will assert Calibration timeout flag	0x00

Bit	Attr	Bit Name	Description	Reset
			and do not update the BR counter reload value of calibration result. 0 = Disable 1 = Enable	
6	rw	URT1_BKTMO_EN	UART Break timeout detection enable bit. When enables and Break condition has detected, chip will trigger time-out timer to start counting. After Break timeout detection, UART will assert Break timeout flag. 0 = Disable 1 = Enable	0x00
5	rw	URT1_RXTMO_EN	UART RX timeout enable bit for shadow buffer data loading into URTx_RDAT. When timeout happened and shadow buffer storing data >=1 byte, chip will load shadow buffer into URTx_RDAT register even though it is not over the receive threshold URTx_RX_TH. User can read data to speed process. 0 = Disable 1 = Enable	0x00
4	rw	URT1_IDTMO_EN	UART Idle timeout detection enable bit. When enables and Idle timeout has detected, UART will assert idle timeout flag. The time is starting after STOP bit of the last character. (for SmartCard maximum guard-time) 0 = Disable 1 = Enable	0x00
3..2	rw	URT1_TMO_MDS	UART timeout timer mode select. When selects general timer, the timer auto reload function is enabled and URTx_IDTMO_TH is used as the auto reload register. 0x0 = UART (UART timeout timer) 0x1 = General (general timer)	0x00
1	rw	URT1_TMO_RST	UART timeout timer force reset enable. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
0	rw	URT1_TMO_EN	UART timeout timer enable. 0 = Disable 1 = Enable	0x00

1.20.18. URT1 timeout control register 2

URT1_TMOUT2	URT1 timeout control register 2		
Offset Address :	0x44	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT1_TMO_CNT[15:8]							
23	22	21	20	19	18	17	16
URT1_TMO_CNT[7:0]							
15	14	13	12	11	10	9	8
URT1_IDTMO_TH[15:8]							
7	6	5	4	3	2	1	0
URT1_IDTMO_TH[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	rw	URT1_TMO_CNT	UART timeout counter value.	0x0000
15..0	rw	URT1_IDTMO_TH	UART receive idle timeout detect threshold value by using receive bit time. The timeout threshold is starting after STOP bit of the last character and value 1 indicates 1 bit time. When selects general timer in URTx_TMO_MDS, the timer auto reload function is enabled and URTx_IDTMO_TH is used as the auto reload register.	0x0000

1.20.19. URT1 SmartCard control register

URT1_SC	URT1 SmartCard control register		
Offset Address :	0x48	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	URT1_RXE_NUM[2:0]			Reserved	URT1_TXE_NUM[2:0]		
7	6	5	4	3	2	1	0
Reserved			URT1_RXE_LEN	URT1_TXE_MDS[1:0]		URT1_RXE_MDS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	-	Reserved	Reserved	0x00
14..12	rw	URT1_RXE_NUM	UART RX parity error detect and NACK transmission retry maximum number. When the register value >0, chip will retry to pull low on RX line and receive data. This register set the retry maximum number for continuous RX error retry. Value 0 indicates to disable hardware auto retry.	0x00
11	-	Reserved	Reserved	0x00
10..8	rw	URT1_TXE_NUM	UART TX error detect and data resend maximum number. When the register value >0, chip will resend the shift buffer data. This register set the resend maximum number for continuous TX error detection. Value 0 indicates to disable hardware auto resending.	0x00
7..5	-	Reserved	Reserved	0x00
4	rw	URT1_RXE_LEN	UART RX parity error detect and NACK transmission (pull low on RX line) bit time length select. 0x0 = 1Bit 0x1 = 2Bit	0x00
3..2	rw	URT1_TXE_MDS	UART TX error detect mode select. It must be noticed that the URTx_TX pin needs to set open-drain mode when enables the TX error detect function. 0x0 = Disable 0x1 = CHK_Low : check asserted low by RX device (for SmartCard) 0x2 = CHK_TX : check TX data by RX input data (for LIN mode) 0x3 = Reserved	0x00
1..0	rw	URT1_RXE_MDS	UART RX parity error detect control mode select. When enables and detects parity error, chip will pull low on RX line during STOP bit cycle and retry to receive new data but not assert interrupt. It must be noticed that the URTx_RX pin needs to set open-drain mode when enables the parity error detect function. Value 0 indicates to disable hardware auto retry. 0x0 = Disable 0x1 = Enable : hardware RX auto retry number by setting URTx_RXE_NUM 0x2 = Auto : hardware RX auto retry always unless receiving parity correct character	0x00

1.20.20. URT1 slave address detect register

URT1_SADR	URT1 slave address detect register		
Offset Address :	0x4C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
URT1_SA_MSK[7:0]							
7	6	5	4	3	2	1	0
URT1_SA_RX[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..8	rw	URT1_SA_MSK	UART multi-processor slave address mask register. URTx_SA_RX register is combined with URTx_SA_MSK register to form Given/Broadcast Address for automatic address recognition. In fact, URTx_SA_MSK functions as the 'mask' register for URTx_SA_RX register. The slave address is created by taking the logical OR of URTx_SA_RX and URTx_SA_MSK. Zero in this result is considered as 'don't care'. (Value 0x00 indicates to enter multi-processor monitor mode.)	0x00
7..0	rw	URT1_SA_RX	UART multi-processor mode received slave address. When URTx_MDS select multi-processor mode and URTx_SA_MSK=0x00, UART enter multi-processor monitor mode and the input slave address value can be read from URTx_RCAP register.	0x00

1.20.21. URT1 calibration control register

URT1_CAL	URT1 calibration control register		
Offset Address :	0x50	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
URT1_CALC_HE	Reserved			URT1_CAL_MDS[1:0]		URT1_CAL_AUTO	URT1_CAL_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	rw	URT1_CALC_HE	UART auto baud-rate calibration complete data receive hold enable. When enables, the receive data will be hold from shift buffer to shadow buffer after auto baud-rate calibration complete. 0 = Disable 1 = Enable	0x00
6..4	-	Reserved	Reserved	0x00
3..2	rw	URT1_CAL_MDS	UART auto baud-rate calibration mode select. 0x0 = Start : measure the start bit 0x1 = Edge : measure start falling edge to next falling edge 0x2 = Reserved 0x3 = Reserved	0x00
1	rw	URT1_CAL_AUTO	UART Break detection and auto baud-rate calibration enable. When enables, hardware will auto enable baud-rate calibration after detect Break condition. When the calibration is finished and the URTx_CALCF is asserted.	0x00

			0 = Disable 1 = Enable	
0	rw	URT1_CAL_EN	UART baud-rate calibration enable. When enables, calibration will start after receive expected character. This bit will clear by hardware after calibration stop. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00

1.20.22. URT1 IrDA control register

URT1_IRDA	URT1 IrDA control register		
Offset Address :	0x54	Reset Value :	0x00000300

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				URT1_IR_PW[3:0]			
7	6	5	4	3	2	1	0
Reserved						URT1_IR_MDS	URT1_IR_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	-	Reserved	Reserved	0x00
11..8	rw	URT1_IR_PW	UART IrDA output pulse width select. IrDA pulse width = (URTx_IR_PW+1) * T<CK_URTx_TX>. The value needs small than URTx_TXOS_NUM. Note : (1) When URTx_IR_PW value equals URTx_TXOS_NUM value, the output is keep low during data bit cycle. (2) When URTx_IR_PW value is large URTx_TXOS_NUM value, the output is keep high during data bit cycle.	0x03
7..2	-	Reserved	Reserved	0x00
1	rw	URT1_IR_MDS	UART IrDA data received mode select. When selects Normal and over-sampling mode URTx_OS_MDS sets Three, the IrDA sampling sequence value need equal 000 then output bit value 0 and others output 1. When selects Wide and over-sampling mode URTx_OS_MDS sets Three, the IrDA sampling sequence value need equal 000,001,010,100 then output bit value 0 and others output 1. 0 = Normal 1 = Wide	0x00
0	rw	URT1_IR_EN	UART IrDA data format enable. When enables, the IrDA encoder and decoder enable for data stream. 0 = Disable 1 = Enable	0x00

1.20.23. URT1 hardware flow control register

URT1_HFC	URT1 hardware flow control register		
Offset Address :	0x58	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0

Reserved	Reserved	Reserved	URT1_RTS_OUT	URT1_RTS_INV	URT1_CTS_INV	URT1_RTS_EN	URT1_CTS_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	rw	URT1_RTS_OUT	URTx_RTS output control data bit. This bit is no effect when URTx_RTS_EN is set. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
3	rw	URT1_RTS_INV	URTx_RTS output inverse enable. When URTx_EN is disabled and the RTS output is set by URTx_RTS_OUT register, the bit does not affect the RTS output. 0 = Disable 1 = Enable	0x00
2	rw	URT1_CTS_INV	URTx_CTS input inverse enable. 0 = Disable 1 = Enable	0x00
1	rw	URT1_RTS_EN	UART RTS hardware flow control enable. When enables, URTx_RTS signal will output high if RX buffer is full. It will change URTx_RTS to low when RX buffer is not full or under threshold. 0 = Disable 1 = Enable	0x00
0	rw	URT1_CTS_EN	UART CTS hardware flow control enable. When enables, transmitter will hold data transmission and enter idle state if detect URTx_RTS signal high. It will automatically transmit next data when URTx_RTS change to low. 0 = Disable 1 = Enable	0x00

1.20.24. URT1 mute control register

URT1_MUTE	URT1 mute control register		
Offset Address :	0x5C	Reset Value :	0x00010100

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved					URT1_MUTE_AEX2	URT1_MUTE_AEX1	URT1_MUTE_AEX0
15	14	13	12	11	10	9	8
Reserved						URT1_MUTE_AEN1	URT1_MUTE_AEN0
7	6	5	4	3	2	1	0
Reserved							URT1_MUTE_EN

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..19	-	Reserved	Reserved	0x00
18	rw	URT1_MUTE_AEX2	UART auto exit mute mode and receive data by idle line detection enable bit. When UART enters mute mode and this bit enables, it will disable mute condition and exit mute mode if has detected the defined idle-line by setting threshold timer in URTx_DET_IDL. 0 = Disable 1 = Enable	0x00
17	rw	URT1_MUTE_AEX1	UART auto exit mute mode and receive data by Break condition detection enable bit. When UART enters mute mode and this bit enables, it will disable mute condition and exit mute mode if has	0x00

			detected Break condition. 0 = Disable 1 = Enable	
16	rw	**URT1_MUTE_AEX0**	UART auto exit mute mode and receive data by multi-processor slave address matched condition enable bit.. When UART enters mute mode and this bit enables, it will disable mute condition and exit mute mode if has received the defined address in URTx_SADR(URTx_MDS=0x2 or 0x3).(Default 1) 0 = Disable 1 = Enable	0x01
15..10	-	**Reserved**	Reserved	0x00
9	rw	**URT1_MUTE_AEN1**	UART mute mode auto enter by idle line detection enable bit. When enables auto mode, UART will enter mute mode after detect the defined idle-line by setting threshold timer in URTx_DET_IDL. 0 = Disable 1 = Enable	0x00
8	rw	**URT1_MUTE_AEN0**	UART mute mode auto enter by multi-processor slave address unmatched condition enable bit. When enables auto mode, UART will enter mute mode after received the unmatched address in URTx_SADR(URTx_MDS=0x2 or 0x3). 0 = Disable 1 = Enable	0x01
7..1	-	**Reserved**	Reserved	0x00
0	rw	**URT1_MUTE_EN**	UART mute mode enable. When enables, only receives the characters those are idle-line for multi-processor Idle-line mode , data with address bit for multi-processor Address-bit mode or break condition for UART auto calibration mode. Also, the non-address or non-break characters are not received and does not assert the URTx_RXF interrupt. If an address is received, user software can validate the address and reset this bit to continue receiving data. 0 = Disable 1 = Enable	0x00

1.20.25. URT1 Register Map

URT1 Register Map Register Number = 24

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	URT1_STA	Reserved	URT1_CALTMOF	URT1_BKTMOF	URT1_IDTMOF	URT1_RXTMOF	Reserved	URT1_TUDRF	URT1_TXEF	URT1_ROVRF	URT1_NCEF	URT1_FEF	URT1_PEF	Reserved	URT1_CTSF	URT1_IDLF	URT1_BKF	URT1_CALOVF	URT1_CALUDF	URT1_CALCF	URT1_TMOF	URT1_BRTF	URT1_SADRF	Reserved	Reserved	URT1_TXF	URT1_RXF	URT1_RXDF	URT1_LSF	URT1_ERRF	URT1_TCF	URT1_UGF	URT1_RHF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	URT1_INT	Reserved	URT1_CALTMO_IE	URT1_BKTMO_IE	URT1_IDTMO_IE	URT1_RXTMO_IE	Reserved	URT1_TUDR_IE	URT1_TXE_IE	URT1_ROVR_IE	URT1_NCE_IE	URT1_FE_IE	URT1_PE_IE	Reserved	URT1_CTS_IE	URT1_IDL_IE	URT1_BK_IE	Reserved		URT1_CALC_IE	URT1_TMO_IE	URT1_BRT_IE	URT1_SADR_IE	Reserved	Reserved	URT1_TX_IE	URT1_RX_IE	Reserved	URT1_LS_IE	URT1_ERR_IE	URT1_TC_IE	URT1_UG_IE	URT1_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	URT1_CLK	Reserved	URT1_BR_CKS	URT1_CKO_LCK	URT1_CKO_STA	URT1_BRO_LCK	URT1_BRO_STA	URT1_BR_MDS	URT1_BR_EN	Reserved		URT1_TX_CKS [1:0]		Reserved		URT1_RX_CKS [1:0]		Reserved								URT1_ECK_CKS	Reserved	URT1_CLK_CKS	URT1_CLK_EN	URT1_CK_SEL [2:0]			Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	URT1_STA2	Reserved	URT1_TX_LVL [2:0]			Reserved	URT1_RX_LVL [2:0]			Reserved								Reserved	Reserved	Reserved	URT1_CTS	Reserved		Reserved	Reserved	URT1_IR_BUSYF	URT1_BKBF	URT1_NCF	Reserved	Reserved	URT1_ADR	URT1_PAR	URT1_BUSYF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	URT1_CR0	URT1_DMA_TXEN	URT1_DMA_RXEN	URT1_DDTX_EN	Reserved	Reserved	Reserved		Reserved	URT1_LBM_EN	URT1_NCHAR_DIS	URT1_NCHAR_HE	URT1_IDL_MDS	Reserved		URT1_RX_TH[1:0]		URT1_DE_GT[1:0]		URT1_DE_INV	URT1_DE_EN	URT1_TX_INV	URT1_RX_INV	URT1_SYNC_MDS	URT1_IO_SWP	URT1_GSA_EN	URT1_MDS[2:0]			URT1_DAT_LINE	URT1_HDX_EN	URT1_OS_MDS	URT1_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	URT1_CR1	Reserved	Reserved		URT1_TXOS_NUM [4:0]					URT1_TXSTP_LEN [1:0]		URT1_TXMSB_EN	URT1_TXPAR_STK	URT1_TXPAR_POL	URT1_TXPAR_EN	URT1_TXDSIZE [1:0]		Reserved			URT1_RXOS_NUM [4:0]					URT1_RXSTP_LEN [1:0]		URT1_RXMSB_EN	URT1_RXPAR_STK	URT1_RXPAR_POL	URT1_RXPAR_EN	URT1_RXDSIZE [1:0]	
Reset	0x0F400F40	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
0x18	URT1_CR2	URT1_DOUT_IDL [1:0]		URT1_DOUT_MDS	Reserved	URT1_NSSI_EN	URT1_NSS_SWEN	URT1_NSS_INV	URT1_NSSI_INV	Reserved						URT1_NSS_SWI	URT1_NSS_SWO	Reserved								Reserved			URT1_TX_HALT	URT1_TX_EN	URT1_RX_EN	URT1_ADR_TX	URT1_BK_TX
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	URT1_CR3	Reserved								URT1_TXGT_LEN [7:0]								URT1_DET_IDL [7:0]								Reserved			URT1_DET_BK	Reserved	URT1_CPHA	URT1_CPOL	Reserved
Reset	0x00000A00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0

0x20	URT1_CR4	Reserved								Reserved								Reserved	URT1_TNUM[2:0]			Reserved	URT1_RNUM[2:0]			URT1_TDAT_CLR	URT1_RDAT_CLR	URT1_TDAT_INV	URT1_RDAT_INV	Reserved			
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	URT1_RLR	Reserved																Reserved		URT1_PSR[5:0]						URT1_RLR[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	URT1_CNT	Reserved																Reserved		URT1_PSC[5:0]						URT1_CNT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	URT1_RCAP	Reserved																Reserved					URT1_RCAP_ADR	URT1_RCAP_PAR	URT1_RCAP_STP	URT1_RCAP_DAT [7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	URT1_RDAT	URT1_RDAT[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	URT1_TDAT	URT1_TDAT[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	URT1_TDAT3	Reserved								URT1_TDAT3[23:0]																							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	URT1_SBUF	Reserved																URT1_TSBUF[7:0]								URT1_RSBUF[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	URT1_TMOUT	URT1_CALTMO_TH [3:0]				URT1_BKTMO_TH [3:0]				URT1_RXTMO_TH [7:0]								URT1_TMO_LCK	URT1_TMO_STA	Reserved			URT1_TMO_CKS [2:0]			URT1_CALTMO_EN	URT1_BKTMO_EN	URT1_RXTMO_EN	URT1_IDTMO_EN	URT1_TMO_MDS [1:0]		URT1_TMO_RST	URT1_TMO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x44	URT1_TMOUT2	URT1_TMO_CNT [15:0]																URT1_IDTMO_TH [15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x48	URT1_SC	Reserved																Reserved	URT1_RXE_NUM [2:0]			Reserved	URT1_TXE_NUM [2:0]			Reserved			URT1_RXE_LEN	URT1_TXE_MDS [1:0]		URT1_RXE_MDS [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x4C	URT1_SADR	Reserved								Reserved								URT1_SA_MSK [7:0]								URT1_SA_RX[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	URT1_CAL	Reserved																Reserved								URT1_CALC_HE	Reserved			URT1_CAL_MDS [1:0]		URT1_CAL_AUTO	URT1_CAL_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x54	URT1_IRDA	Reserved																Reserved				URT1_IR_PW[3:0]				Reserved						URT1_IR_MDS	URT1_IR_EN
Reset	**0x00000300**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
0x58	URT1_HFC	Reserved																Reserved								Reserved	Reserved	Reserved	URT1_RTS_OUT	URT1_RTS_INV	URT1_CTS_INV	URT1_RTS_EN	URT1_CTS_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x5C	URT1_MUTE	Reserved								Reserved					URT1_MUTE_AEX2	URT1_MUTE_AEX1	URT1_MUTE_AEX0	Reserved						URT1_MUTE_AEN1	URT1_MUTE_AEN0	Reserved							URT1_MUTE_EN
Reset	**0x00010100**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

1.21. URT2 Control Registers

URT2 Control	(URT2) UART Control Module-2
Base Address :	0x52020000

1.21.1. URT2 status register 1

URT2_STA	URT2 status register 1		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	URT2_CALTMOF	URT2_BKTMOF	URT2_IDTMOF	URT2_RXTMOF	Reserved	URT2_TUDRF	URT2_TXEF
23	22	21	20	19	18	17	16
URT2_ROVRF	URT2_NCEF	URT2_FEF	URT2_PEF	Reserved	URT2_CTSF	URT2_IDLF	URT2_BKF
15	14	13	12	11	10	9	8
URT2_CALOVF	URT2_CALUDF	URT2_CALCF	URT2_TMOF	URT2_BRTF	URT2_SADRF	Reserved	Reserved
7	6	5	4	3	2	1	0
URT2_TXF	URT2_RXF	URT2_RXDF	URT2_LSF	URT2_ERRF	URT2_TCF	URT2_UGF	URT2_RHF

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	URT2_CALTMOF	UART auto baud-rate calibration sync field receive time-out time out flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
29	rw	URT2_BKTMOF	UART break receive time out flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
28	rw	URT2_IDTMOF	UART idle state time out flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
27	rw	URT2_RXTMOF	UART receive time out flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
26	-	Reserved	Reserved	0x00
25	rw	URT2_TUDRF	UART SPI slave mode transmit underrun flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
24	rw	URT2_TXEF	UART TX error detect flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of URTx_TXE_MDS for detail. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
23	rw	URT2_ROVRF	UART receive overrun error flag. (set by hardware and clear by software writing 1) When receive overrun, hardware will stop to receive next data into data shadow buffer until this flag is cleared. This flag is indicated for following two conditions. (1) When RX shadow buffer is arrived over the RX threshold and the data register has not read out. If shift buffer is filled of next data, this flag is asserted. (2) When Parity error, Frame error, Break detect or Slave-Address detect, has happened and caused RX shadow buffer input holding. If shift buffer is filled of next data, this flag is asserted. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
22	rw	URT2_NCEF	UART receive noised character error flag. (set by hardware	0x00

			and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	
21	rw	URT2_FEF	UART frame error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
20	rw	URT2_PEF	UART parity error flag. (set by hardware and clear by software writing 1) When multi-processor mode, the parity value is including of address bit. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19	-	Reserved	Reserved	0x00
18	rw	URT2_CTSF	UART CTS change detect interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	rw	URT2_IDLF	UART idle line detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
16	rw	URT2_BKF	UART break condition detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	r	URT2_CALOVF	UART auto baud-rate calibration overflow status flag. This flag is asserted when the baud-rate calibration counter is changed overflow during baud-rate calibration (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
14	r	URT2_CALUDF	UART auto baud-rate calibration underflow status flag. This flag is asserted when the baud-rate calibration counter is changed to zero during baud-rate calibration (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
13	rw	URT2_CALCF	UART auto baud-rate calibration complete flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
12	rw	URT2_TMOF	UART timeout timer timeout flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
11	rw	URT2_BRTF	UART baud-rate generator timer timeout flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
10	rw	URT2_SADRF	UART slave address matched flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	rw	URT2_TXF	UART transmit data register empty. (set by hardware and clear by hardware or software writing 1) When transmitted shadow buffer is empty and the data register URTx_TDAT will copy to the shadow buffer, this flag is set. This bit is cleared when URTx_TDAT is written or this flag set to 1 by software. The flag is set after UART reset or Idle state.	0x00

			0 = Normal (No event occurred) 1 = Happened (Event happened)	
6	rw	URT2_RXF	UART receive data register not empty. (set by hardware and clear by hardware or software writing 1) When received shadow buffer level URTx_RX_LVL is greater than or equal to the shadow buffer threshold URTx_RX_TH setting, this flag is set and the shadow buffer content copy to data register URTx_RDAT. This bit is cleared when URTx_RDAT is read or this flag set to 1 by software. But it does not be cleared when URTx_RDAT is read by SWD debugging. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	r	URT2_RXDF	UART received data byte number is different from previous received data byte number for URTx_RDAT register. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	URT2_LSF	UART line statue flag for break condition, idle line, CTS detect. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	URT2_ERRF	UART error interrupt flag for parity error, frame error, overrun error, receive time out and noise error. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	URT2_TCF	UART transmission complete flag. When both shadow buffer and data register are empty and shift buffer shift out complete, then set this flag. (set by hardware and clear by hardware or software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	rw	URT2_UGF	UART general event flag. It indicates each of URTx_SADRF , URTx_BRTF , URTx_TMOF or URTx_CALCF flag is asserted when this flag is set. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	rw	URT2_RHF	UART receive hold flag. It indicates one of hardware hold event is happened when this flag is set. In the condition, the shift buffer is held and do not load data to shadow buffer until this bit is cleared. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00

1.21.2. URT2 interrupt enable register

URT2_INT	URT2 interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	URT2_CALTMO_IE	URT2_BKTMO_IE	URT2_IDTMO_IE	URT2_RXTMO_IE	Reserved	URT2_TUDR_IE	URT2_TXE_IE
23	22	21	20	19	18	17	16
URT2_ROVR_IE	URT2_NCE_IE	URT2_FE_IE	URT2_PE_IE	Reserved	URT2_CTS_IE	URT2_IDL_IE	URT2_BK_IE
15	14	13	12	11	10	9	8
Reserved		URT2_CALC_IE	URT2_TMO_IE	URT2_BRT_IE	URT2_SADR_IE	Reserved	Reserved
7	6	5	4	3	2	1	0
URT2_TX_IE	URT2_RX_IE	Reserved	URT2_LS_IE	URT2_ERR_IE	URT2_TC_IE	URT2_UG_IE	URT2_IEA

Bit	Attr	Bit Name	Description	Reset

31	-	**Reserved**	Reserved	0x00
30	rw	**URT2_CALTMO_IE**	UART auto baud-rate calibration sync field receive time-out time out interrupt enable. 0 = Disable 1 = Enable	0x00
29	rw	**URT2_BKTMO_IE**	UART break receive time out interrupt enable. 0 = Disable 1 = Enable	0x00
28	rw	**URT2_IDTMO_IE**	UART idle state time out interrupt enable. 0 = Disable 1 = Enable	0x00
27	rw	**URT2_RXTMO_IE**	UART receive time out interrupt enable. 0 = Disable 1 = Enable	0x00
26	-	**Reserved**	Reserved	0x00
25	rw	**URT2_TUDR_IE**	UART SPI slave mode transmit underrun interrupt enable. 0 = Disable 1 = Enable	0x00
24	rw	**URT2_TXE_IE**	UART TX error detect interrupt enable. Refer to the register descriptions of URTx_TXE_MDS for detail. 0 = Disable 1 = Enable	0x00
23	rw	**URT2_ROVR_IE**	UART receive overrun error interrupt enable. Refer to the register descriptions of URTx_ROVRF for the detail. 0 = Disable 1 = Enable	0x00
22	rw	**URT2_NCE_IE**	UART receive noised character interrupt enable. 0 = Disable 1 = Enable	0x00
21	rw	**URT2_FE_IE**	UART frame error interrupt enable. 0 = Disable 1 = Enable	0x00
20	rw	**URT2_PE_IE**	UART parity error interrupt enable. 0 = Disable 1 = Enable	0x00
19	-	**Reserved**	Reserved	0x00
18	rw	**URT2_CTS_IE**	UART CTS change detect interrupt enable. 0 = Disable 1 = Enable	0x00
17	rw	**URT2_IDL_IE**	UART idle line detect interrupt enable. 0 = Disable 1 = Enable	0x00
16	rw	**URT2_BK_IE**	UART break condition detect interrupt enable. 0 = Disable 1 = Enable	0x00
15..14	-	**Reserved**	Reserved	0x00
13	rw	**URT2_CALC_IE**	UART auto baud-rate calibration complete interrupt enable. 0 = Disable 1 = Enable	0x00
12	rw	**URT2_TMO_IE**	UART timeout timer timeout interrupt enable. 0 = Disable 1 = Enable	0x00
11	rw	**URT2_BRT_IE**	UART baud-rate generator timer timeout interrupt enable. 0 = Disable 1 = Enable	0x00
10	rw	**URT2_SADR_IE**	UART slave address matched interrupt enable. 0 = Disable 1 = Enable	0x00
9	-	**Reserved**	Reserved	0x00
8	-	**Reserved**	Reserved	0x00

7	rw	URT2_TX_IE	UART transmit data register empty interrupt enable. Refer to the register descriptions of URTx_TXF for the detail. 0 = Disable 1 = Enable	0x00
6	rw	URT2_RX_IE	UART receive data register not empty interrupt enable. Refer to the register descriptions of URTx_RXF for the detail. 0 = Disable 1 = Enable	0x00
5	-	Reserved	Reserved	0x00
4	rw	URT2_LS_IE	UART line statue flag for break condition, idle line, CTS detect. 0 = Disable 1 = Enable	0x00
3	rw	URT2_ERR_IE	UART error interrupt enable for parity error, frame error, overrun error, receive time out and noise error. 0 = Disable 1 = Enable	0x00
2	rw	URT2_TC_IE	UART transmission complete interrupt enable. (set by hardware and clear by hardware or software writing 1) 0 = Disable 1 = Enable	0x00
1	rw	URT2_UG_IE	UART general event interrupt enable for URTx_SADRF , URTx_TF , URTx_RCNTF or URTx_TCNTF events. 0 = Disable 1 = Enable	0x00
0	rw	URT2_IEA	UART interrupt all enable. When disables, the UART global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.21.3. URT2 clock source register

URT2_CLK	URT2 clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	URT2_BR_CKS	URT2_CKO_LCK	URT2_CKO_STA	URT2_BRO_LCK	URT2_BRO_STA	URT2_BR_MDS	URT2_BR_EN
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved		URT2_TX_CKS[1:0]		Reserved		URT2_RX_CKS[1:0]	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
URT2_ECK_CKS	Reserved	URT2_CLK_CKS	URT2_CLK_EN	URT2_CK_SEL[2:0]			Reserved

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	URT2_BR_CKS	UART baud-rate timer clock source select. 0 = PSC : CK_URTx_PSC from clock prescaler output 1 = CK_URTx : CK_URTx from UART internal clock input	0x00
29	rw	URT2_CKO_LCK	UART PSC clock output signal initial state control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	0x00
28	rw	URT2_CKO_STA	UART PSC clock output signal initial state. The bit is written effectively only by written 1 to URTx_CKO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
27	rw	URT2_BRO_LCK	UART baud-rate timer timeout signal initial state control. When	0x00

			locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	
26	rw	URT2_BRO_STA	UART baud-rate timer timeout signal initial state. The bit is written effectively only by written 1 to URTx_BRO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
25	rw	URT2_BR_MDS	UART baud-rate timer mode select. Combined mode is only using for general purpose counter. When SmartCard mode, this bit need set to 'Separated' for SmartCard clock output from PSC output. 0 = Separated : Separated PSC and CNT counters for UART baud-rate generator 1 = Combined : Combine to a linear counter for general using timer	0x00
24	rw	URT2_BR_EN	UART baud-rate timer enable. When enables, the baud-rate timer 0 = Disable 1 = Enable	0x00
23..22	-	Reserved	Reserved	0x00
21..20	rw	URT2_TX_CKS	UART transmission clock source select. 0x0 = Internal : UART internal clock source CK_URTx_INT 0x1 = TM01_TRGO 0x2 = TM10_TRGO 0x3 = EXT_CLK (external clock from URTx_CLK pin)	0x00
19..18	-	Reserved	Reserved	0x00
17..16	rw	URT2_RX_CKS	UART receive clock source select. 0x0 = Internal : UART internal clock source CK_URTx_INT 0x1 = TM01_TRGO 0x2 = TM10_TRGO 0x3 = EXT_CLK (external clock from URTx_CLK pin)	0x00
15..8	-	Reserved	Reserved	0x00
7	rw	URT2_ECK_CKS	UART external clock IO select. When select 'RX', the external clock is connected to the selected signal which is selected from URTx_RX or URTx_TX by URTx_IO_SWAP. 0 = CLK : URTx_CLK pin 1 = RX : receiving signal	0x00
6	-	Reserved	Reserved	0x00
5	rw	URT2_CLK_CKS	UART external clock output source select. 0 = OUT : CK_URTx_OUT from clock output divider 1 = SC : CK_URTx_SC from clock input prescaler	0x00
4	rw	URT2_CLK_EN	URTx_CLK signal output enable. 0 = Disable 1 = Enable	0x00
3..1	rw	URT2_CK_SEL	UART internal clock CK_URTx source select. 0x0 = PROC : CK_URTx_PR process clock from CSC 0x1 = NCO_P0 0x2 = CK_LS 0x3 = TM00_TRGO 0x4 = EXT_CLK (external clock from URTx_ECK signal)	0x00
0	-	Reserved	Reserved	0x00

1.21.4. URT2 status register 2

URT2_STA2	URT2 status register 2		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24

Reserved	URT2_TX_LVL[2:0]			Reserved	URT2_RX_LVL[2:0]		
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	URT2_CTS	Reserved		Reserved	Reserved
7	6	5	4	3	2	1	0
URT2_IR_BUSYF	URT2_BKBF	URT2_NCF	Reserved	Reserved	URT2_ADR	URT2_PAR	URT2_BUSYF

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30..28	r	URT2_TX_LVL	UART data buffer transmission remained level indications. 0x0 = 0 (0-byte,empty) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	0x00
27	-	Reserved	Reserved	0x00
26..24	r	URT2_RX_LVL	UART data buffer received level indications. 0x0 = 0 (0-byte,empty) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	0x00
23..16	-	Reserved	Reserved	0x00
15	-	Reserved	Reserved	0x00
14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	r	URT2_CTS	UART CTS line status bit. This bit reflects the CTS line status which is the watched point behind the CTS input inverter.	0x00
11..10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	r	URT2_IR_BUSYF	UART IrDA data received busy flag. 0 = No (No IrDA signal detect) 1 = Busy (detect some IrDA signal)	0x00
6	r	URT2_BKBF	UART send break busy flag. (set and clear by hardware) 0 = Normal (No break transmitted or transmit finished) 1 = Busy (Event happened)	0x00
5	r	URT2_NCF	UART receive noised character flag. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	-	Reserved	Reserved	0x00
3	-	Reserved	Reserved	0x00
2	r	URT2_ADR	UART data receive slave address bit of shift buffer.	0x00
1	r	URT2_PAR	UART data receive parity bit of shift buffer. When multi-processor mode, the parity value is including of address bit.	0x00
0	r	URT2_BUSYF	UART RX busy flag. (set and clear by hardware) When detect valid start bit, this bit is set and clear after stop bit. 0 = Normal (No event occurred) 1 = Busy (Event happened)	0x00

1.21.5. URT2 control register 0

URT2_CR0	URT2 control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT2_DMA_TXEN	URT2_DMA_RXEN	URT2_DDTX_EN	Reserved	Reserved	Reserved		Reserved
23	22	21	20	19	18	17	16

URT2_LBM_EN	URT2_NCHAR_DIS	URT2_NCHAR_HE	URT2_IDL_MDS	Reserved		URT2_RX_TH[1:0]	
15	14	13	12	11	10	9	8
URT2_DE_GT[1:0]		URT2_DE_INV	URT2_DE_EN	URT2_TX_INV	URT2_RX_INV	URT2_SYNC_MDS	URT2_IO_SWP
7	6	5	4	3	2	1	0
URT2_GSA_EN	URT2_MDS[2:0]			URT2_DAT_LINE	URT2_HDX_EN	URT2_OS_MDS	URT2_EN

Bit	Attr	Bit Name	Description	Reset
31	rw	URT2_DMA_TXEN	Direct memory access enable to transmit. When enables, hardware can receive the data from DMA and transmit to output. This bit is enabled to write if URTx_TX_EN=0. 0 = Disable 1 = Enable	0x00
30	rw	URT2_DMA_RXEN	Direct memory access enable to receive. When enables, hardware can receive the data from input and send to DMA. This bit is enabled to write if URTx_RX_EN=0. 0 = Disable 1 = Enable	0x00
29	rw	URT2_DDTX_EN	Hardware force to disable DMA TX function enable bit when detects a break condition. When enables, hardware will disable the URTx_DMA_TXEN bit if hardware detects a break condition. Also, the URTx_DMA_RXEN bit is disabled in this condition. When disables, hardware will keep to do DMA TX function if hardware detects a break condition. 0 = Disable 1 = Enable	0x00
28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26..25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23	rw	URT2_LBM_EN	UART loop back mode enable bit. When enables, the received input is taken from transmitted output to replace from input pin(RX ->TX ,CTS -> RTS). 0 = Disable 1 = Enable	0x00
22	rw	URT2_NCHAR_DIS	UART receiving noised character disable bit. When disables, the received noised character is skipped and does not assert the URTx_RXF interrupt. Also the noised character will copy to URTx_RCAP data register. When enables, the noised character is accepted for receiving. 0 = Enable (Accept noised character) 1 = Disable (Skip noised character)	0x00
21	rw	URT2_NCHAR_HE	UART receiving hold enable bit if receives a noised character. This bit is no effect when URTx_NCHAR_DIS=0. When enables and URTx_NCHAR_DIS=1, the received data will be hold from shift buffer to shadow buffer and the URTx_RHF will be active after received noised character. Until the URTx_RHF is cleared, chip will release the hold function. 0 = Disable 1 = Enable	0x00
20	rw	URT2_IDL_MDS	UART idle line detect management mode select. When selects 'Load' and detects idle line, chip will load shadow buffer into URTx_RDAT register even though it is not over the receive threshold URTx_RX_TH if shadow buffer is not empty. 0 = No (No operation) 1 = Load (Force to load shadow buffer)	0x00
19..18	-	Reserved	Reserved	0x00
17..16	rw	URT2_RX_TH	UART data buffer high threshold for received access. This register will set to '0' (1byte) and is no effect for register written if URTx_DMA_RXEN is enabled. 0x0 = 1byte (default) 0x1 = 2byte	0x00

			0x2 = 3byte 0x3 = 4byte	
15..14	rw	URT2_DE_GT	URTx_DE signal output guard time select by unit of bit time. The selection set both asserted time before START bit and deasserted time after last STOP bit. 0x0 = 1/4 0x1 = 1/2 0x2 = 1 0x3 = 2	0x00
13	rw	URT2_DE_INV	URTx_DE signal inverse enable. The hardware DE output default is low level. 0 = Disable 1 = Enable	0x00
12	rw	URT2_DE_EN	URTx_DE signal output enable. 0 = Disable 1 = Enable	0x00
11	rw	URT2_TX_INV	URTx_TX output signal inverse enable. 0 = Disable 1 = Enable	0x00
10	rw	URT2_RX_INV	URTx_RX input signal inverse enable. 0 = Disable 1 = Enable	0x00
9	rw	URT2_SYNC_MDS	UART SYNC mode(SPI) select. 0 = Master : SPI Master 1 = Slave : SPI Slave	0x00
8	rw	URT2_IO_SWP	URTx_RX/URTx_TX swap enable bit. 0 = Disable 1 = Enable	0x00
7	rw	URT2_GSA_EN	UART multi-processor global slave address enable.	0x00
6..4	rw	URT2_MDS	UART mode select. The Idle-line and Address-bit modes are using for multi-processor control. When selects IDLE or ADR mode, both URTx_MUTE_AEN0 and URTx_MUTE_AEX0 must be enabled. 0x0 = UART : UART mode 0x1 = SYNC : Synchronous/Shift-Register mode 0x2 = IDLE : Idle-line mode for multi-processor 0x3 = ADR : Address-bit mode for multi-processor	0x00
3	rw	URT2_DAT_LINE	UART communication data line select. 0 = 2 : 2-lines separated ~ URTx_RX , URTx_TX 1 = 1 : 1-line Bidirectional ~URTx_TX only.	0x00
2	rw	URT2_HDX_EN	UART Half-duplex mode enable. When enables and UART is during transmission data, the URTx_RX input is no using and the data does not transfer into shadow buffer. 0 = Disable 1 = Enable	0x00
1	rw	URT2_OS_MDS	UART RX data oversampling majority vote select. 0 = Three : Three sample bits method 1 = One : One sample bit method and noise free	0x00
0	rw	URT2_EN	UART function enable bit. 0 = Disable 1 = Enable	0x00

1.21.6. URT2 control register 1

URT2_CR1	URT2 control register 1		
Offset Address :	0x14	Reset Value :	0x0F400F40

31	30	29	28	27	26	25	24
Reserved	Reserved		URT2_TXOS_NUM[4:0]				
23	22	21	20	19	18	17	16

URT2_TXSTP_LEN[1:0]		URT2_TXMSB_EN	URT2_TXPAR_STK	URT2_TXPAR_POL	URT2_TXPAR_EN	URT2_TXDSIZE[1:0]	
15	14	13	12	11	10	9	8
Reserved			URT2_RXOS_NUM[4:0]				
7	6	5	4	3	2	1	0
URT2_RXSTP_LEN[1:0]		URT2_RXMSB_EN	URT2_RXPAR_STK	URT2_RXPAR_POL	URT2_RXPAR_EN	URT2_RXDSIZE[1:0]	

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30..29	-	Reserved	Reserved	0x00
28..24	rw	URT2_TXOS_NUM	UART TX data oversampling samples select. When selects SYNC Master mode, the valid value is from 1 to 31 for oversampling number from 2 to 32. When selects other modes, the valid value is from 3 to 31 for oversampling samples from 4 to 32. (This register is written no effect if UART_TX_EN set 1.)	0x0F
23..22	rw	URT2_TXSTP_LEN	UART TX stop bit length select. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = 0.5bit 0x1 = 1bit 0x2 = 1.5bit 0x3 = 2bit	0x01
21	rw	URT2_TXMSB_EN	UART TX data order Msb first enable. When disables , the Lsb bit will be the first bit. (This register is written no effect if URTx_TX_EN set 1.) 0 = Disable 1 = Enable	0x00
20	rw	URT2_TXPAR_STK	UART stuck parity bit output enable. When enables and URTx_TXPAR_EN=1, parity bit output fixed value by URTx_TXPAR_POL value setting. 0 = Disable 1 = Enable	0x00
19	rw	URT2_TXPAR_POL	UART TX parity bit polarity. This bit is no effect for SPI and SYNC mods. 0x0 = Even 0x1 = Odd	0x00
18	rw	URT2_TXPAR_EN	UART TX parity bit enable. This bit does not be set for SYNC mods. (This register is written no effect if URTx_TX_EN set 1.) 0 = Disable 1 = Enable	0x00
17..16	rw	URT2_TXDSIZE	UART TX data bit length. It is not including START, STOP, ADR or PARITY bits. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = 8bit 0x1 = 7bit 0x2 = Reserved 0x3 = Reserved	0x00
15..13	-	Reserved	Reserved	0x00
12..8	rw	URT2_RXOS_NUM	UART RX data oversampling samples select. When selects SYNC Master mode, the valid value is from 1 to 31 for oversampling number from 2 to 32. When selects other modes, the valid value is from 3 to 31 for oversampling samples from 4 to 32. (This register is written no effect if UART_RX_EN set 1.)	0x0F
7..6	rw	URT2_RXSTP_LEN	UART RX stop bit length select. (This register is written no effect if URTx_RX_EN set 1.) 0x0 = 0.5bit 0x1 = 1bit 0x2 = 1.5bit 0x3 = 2bit	0x01
5	rw	URT2_RXMSB_EN	UART RX data order Msb first enable. When disables , the Lsb bit will be the first bit. (This register is written no effect if URTx_RX_EN set 1.) 0 = Disable	0x00

			1 = Enable	
4	rw	URT2_RXPAR_STK	UART stuck parity bit input enable. When enables and URTx_RXPAR_EN=1, parity bit input fixed value by URTx_RXPAR_POL value setting. 0 = Disable 1 = Enable	0x00
3	rw	URT2_RXPAR_POL	UART RX parity bit polarity. This bit is no effect for SYNC mods. 0x0 = Even 0x1 = Odd	0x00
2	rw	URT2_RXPAR_EN	UART RX parity bit enable. This bit does not be set for SYNC mods. (This register is written no effect if URTx_RX_EN set 1.) 0 = Disable 1 = Enable	0x00
1..0	rw	URT2_RXDSIZE	UART RX data bit length. It is not including START, STOP, ADR or PARITY bits. This bit is no effect for SPI and SYNC mods. (This register is written no effect if URTx_RX_EN set 1.) 0x0 = 8bit 0x1 = 7bit 0x2 = Reserved 0x3 = Reserved	0x00

1.21.7. URT2 control register 2

URT2_CR2	URT2 control register 2		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT2_DOUT_IDL[1:0]		URT2_DOUT_MDS	Reserved	URT2_NSSI_EN	URT2_NSS_SWEN	URT2_NSS_INV	URT2_NSSI_INV
23	22	21	20	19	18	17	16
Reserved						URT2_NSS_SWI	URT2_NSS_SWO
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			URT2_TX_HALT	URT2_TX_EN	URT2_RX_EN	URT2_ADR_TX	URT2_BK_TX

Bit	Attr	Bit Name	Description	Reset
31..30	rw	URT2_DOUT_IDL	UART SPI mode idle state data output value. When SPI master mode URTx_DOUT_MDS is enabled, the URTx_TX output is with driving during idle state and the output level is set by this bit. 0x0 = LBIT (Last data bit) 0x1 = Reserved 0x2 = 0 (Output 0) 0x3 = 1 (Output 1)	0x00
29	rw	URT2_DOUT_MDS	UART SPI master standard mode idle state data output mode select. When disables and data transfers during idle state, the MOSI will output with tristate for master mode. When enables and data transfers during idle state, the MOSI will output with driving for master mode. 0 = Disable : Output with tristate 1 = Enable : Output with driving	0x00
28	-	Reserved	Reserved	0x00
27	rw	URT2_NSSI_EN	UART NSS signal input function enable when UART configure to synchronous mode SPI Slave. 0 = Disable 1 = Enable	0x00
26	rw	URT2_NSS_SWEN	UART NSS signal output use software control bit enable. 0 = Disable 1 = Enable	0x00
25	rw	URT2_NSS_INV	UART NSS output signal inverse enable. The hardware NSS	0x00

			output default is low active level. 0 = Disable 1 = Enable	
24	rw	URT2_NSSI_INV	UART NSS input signal inverse enable. 0 = Disable 1 = Enable	0x00
23..18	-	Reserved	Reserved	0x00
17	r	URT2_NSS_SWI	UART NSS signal software input status bit.	0x00
16	rw	URT2_NSS_SWO	UART NSS signal software output control bit when URTx_NSS_SWEN is disable.	0x00
15..8	-	Reserved	Reserved	0x00
7..5	-	Reserved	Reserved	0x00
4	rw	URT2_TX_HALT	UART transmitter halt enable. 0 = Disable 1 = Enable	0x00
3	rw	URT2_TX_EN	UART transmitter enable. 0 = Disable 1 = Enable	0x00
2	rw	URT2_RX_EN	UART receiver enable. When URTx_MDS selects SYNC mode and URTx_DAT_LINE sets 1-line, enables this bit is used to set receiver mode only and disables this bit is used to set transmission mode only. 0 = Disable 1 = Enable	0x00
1	rw	URT2_ADR_TX	UART slave address for next data transmitted. This bit will clear by hardware after slave address sending end. If this bit and URTx_BK_TX are both set to 1, only the URTx_BK_TX function is action. Refer the URTx_TXGT_LEN register descriptions for more information. (set by software and clear by hardware) 0 = Normal 1 = Send : Send Address	0x00
0	rw	URT2_BK_TX	UART break condition for next data transmitted. This bit will clear by hardware after break condition sending end. If this bit and URTx_ADR_TX are both set to 1, only the URTx_BK_TX function is action. (set by software and clear by hardware) 0 = Normal 1 = Send : Send Break	0x00

1.21.8. URT2 control register 3

URT2_CR3	URT2 control register 3		
Offset Address :	0x1C	Reset Value :	0x00000A00

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT2_TXGT_LEN[7:0]							
15	14	13	12	11	10	9	8
URT2_DET_IDL[7:0]							
7	6	5	4	3	2	1	0
Reserved			URT2_DET_BK	Reserved	URT2_CPHA	URT2_CPOL	Reserved

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	rw	URT2_TXGT_LEN	UART TX guard time or idle-line length. (1)URTx_MDS=UART,SYNC,ADR modes: This register use as TX guard time between adjacent characters' transmission in the unit of bit time. The time is starting after STOP bit of the last character. Value 0 indicates 0 bit time. (for SmartCard	0x00

			minimum guard-time, counting start at Start bit = 12+{0~254} bit time) (2)URTx_MDS=IDLE mode: This register use as the idle-line length in the unit of bit time.	
15..8	rw	URT2_DET_IDL	UART idle line detect threshold value by using receive bit time. The timeout threshold is starting after STOP bit of the last character and value 1 indicates 2 bit time. The value 0 is invalid.	0x0A
7..5	-	Reserved	Reserved	0x00
4	rw	URT2_DET_BK	UART bit time select for break detection or transmission. For data receiving, the detect time is a character time plus this value after last STOP bit cycle. For data transmission, the break generation guard time is a character time plus this value+3 bit time. 0x0 = 1Bit 0x1 = 3Bit	0x00
3	-	Reserved	Reserved	0x00
2	rw	URT2_CPHA	UART clock phase select. It is used to select the data sampling on leading edge or trailing edge of SPI clock. 0 = Leading edge 1 = Trailing edge	0x00
1	rw	URT2_CPOL	UART clock polarity select. It is used to select the SPI clock level in idle state. 0 = Low 1 = High	0x00
0	-	Reserved	Reserved	0x00

1.21.9. URT2 control register 4

URT2_CR4	URT2 control register 4		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	URT2_TNUM[2:0]			Reserved	URT2_RNUM[2:0]		
7	6	5	4	3	2	1	0
URT2_TDAT_CLR	URT2_RDAT_CLR	URT2_TDAT_INV	URT2_RDAT_INV	Reserved			

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15	-	Reserved	Reserved	0x00
14..12	r	URT2_TNUM	UART remained data byte number in data register. Value 0~4 is valid only. 0x0 = 0 (0-byte) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	0x00
11	-	Reserved	Reserved	0x00
10..8	rw	URT2_RNUM	UART received data byte number when data shadow buffer last transfer to URTx_RDAT register. Firmware can write an initial value for received byte number comparison for URTx_RXDF status bit. Value 0~4 is valid only. 0x0 = 0 (0-byte) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte)	0x00

			0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	
7	w	URT2_TDAT_CLR	UART transmitted data clear enable. When enables, the transmitted data buffer will be flushed and URTx_TXF flag is set. Also URTx_TNUM and URTx_TX_LVL are cleared. It allows discarding the data when data has not been send under NACK error and frame error is active for SmartCard mode. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
6	w	URT2_RDAT_CLR	UART received data clear enable. When enables, the received data buffer will be flushed and URTx_RXF flag is cleared. Also URTx_RNUM and URTx_RX_LVL are cleared. It allows discarding the data without reading it and avoid a data overrun condition. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
5	rw	URT2_TDAT_INV	UART inverse transmitted data enable. When enables, the transmitted data bits are inverted but Start, Stop, Address and Parity bits are not inverted. 0 = Disable 1 = Enable	0x00
4	rw	URT2_RDAT_INV	UART inverse received data enable. When enables, the received data bits are inverted but Start, Stop, Address and Parity bits are not inverted. 0 = Disable 1 = Enable	0x00
3..0	-	Reserved	Reserved	0x00

1.21.10. URT2 baud-rate clock counter reload register

URT2_RLR	URT2 baud-rate clock counter reload register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		URT2_PSR[5:0]					
7	6	5	4	3	2	1	0
URT2_RLR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..8	rw	URT2_PSR	UART baud-rate clock prescaler reload register. Actual value equals the register value plus one.	0x00
7..0	rw	URT2_RLR	UART baud-rate clock counter reload register. Actual value equals the register value plus one.	0x00

1.21.11. URT2 baud-rate clock counter register

URT2_CNT	URT2 baud-rate clock counter register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		URT2_PSC[5:0]					
7	6	5	4	3	2	1	0
URT2_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..8	r	URT2_PSC	UART baud-rate clock prescaler value register.	0x00
7..0	r	URT2_CNT	UART baud-rate clock counter value register.	0x00

1.21.12. URT2 RX data capture register

URT2_RCAP	URT2 RX data capture register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved					URT2_RCAP_ADR	URT2_RCAP_PAR	URT2_RCAP_STP
7	6	5	4	3	2	1	0
URT2_RCAP_DAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..11	-	Reserved	Reserved	0x00
10	rw	URT2_RCAP_ADR	UART capture address bit from RX shift buffer.	0x00
9	rw	URT2_RCAP_PAR	UART capture parity bit from RX shift buffer.	0x00
8	rw	URT2_RCAP_STP	UART capture stop bit from RX shift buffer.	0x00
7..0	rw	URT2_RCAP_DAT	UART capture data from RX shift buffer for Parity error / Frame error / Break detect / Slave-Address detect matched / Calibration Sync Character / Noise Character. The capture function is disabled for synchronous mode. The capture data is affected by data order Msb first setting in URTx_RXMSB_EN. But it not affected by received data inverse setting in URTx_RDAT_INV.	0x00

1.21.13. URT2 RX data register

URT2_RDAT	URT2 RX data register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT2_RDAT[31:24]							
23	22	21	20	19	18	17	16
URT2_RDAT[23:16]							
15	14	13	12	11	10	9	8
URT2_RDAT[15:8]							
7	6	5	4	3	2	1	0
URT2_RDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	URT2_RDAT	UART received data register. Read this register will clear the URTx_RXF. Hardware will force to logic 0 for non-updated byte(s) by URTx_RX_TH setting.	0x00000000

1.21.14. URT2 TX data register

URT2_TDAT	URT2 TX data register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT2_TDAT[31:24]							
23	22	21	20	19	18	17	16
URT2_TDAT[23:16]							
15	14	13	12	11	10	9	8
URT2_TDAT[15:8]							
7	6	5	4	3	2	1	0
URT2_TDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	URT2_TDAT	UART transmitted data register. Write this register will clear the URTx_TXF. When write data by word, half-word or byte operation, chip will transfer 4-byte, 2-byte, or 1-byte data to shadow buffer. (write-only)	0x00000000

1.21.15. URT2 TX data 3-byte register

URT2_TDAT3	URT2 TX data 3-byte register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT2_TDAT3[23:16]							
15	14	13	12	11	10	9	8
URT2_TDAT3[15:8]							
7	6	5	4	3	2	1	0
URT2_TDAT3[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..0	w	URT2_TDAT3	UART transmitted data register for 3-byte data write only. Write this register will clear the URTx_TXF and force to transfer all 24-bit data to shadow buffer. This register is only allowed to access by a 32-bit word instruction.	0x000000

1.21.16. URT2 data shift buffer register

URT2_SBUF	URT2 data shift buffer register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
URT2_TSBUF[7:0]							
7	6	5	4	3	2	1	0
URT2_RSBUF[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	r	URT2_TSBUF	UART TX data shift buffer register.	0x00
7..0	r	URT2_RSBUF	UART RX data shift buffer register.	0x00

1.21.17. URT2 timeout control register

URT2_TMOUT	URT2 timeout control register		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT2_CALTMO_TH[3:0]				URT2_BKTMO_TH[3:0]			
23	22	21	20	19	18	17	16
URT2_RXTMO_TH[7:0]							
15	14	13	12	11	10	9	8
URT2_TMO_LCK	URT2_TMO_STA	Reserved			URT2_TMO_CKS[2:0]		
7	6	5	4	3	2	1	0
URT2_CALTMO_EN	URT2_BKTMO_EN	URT2_RXTMO_EN	URT2_IDTMO_EN	URT2_TMO_MDS[1:0]		URT2_TMO_RST	URT2_TMO_EN

Bit	Attr	Bit Name	Description	Reset
31..28	rw	URT2_CALTMO_TH	UART calibration timeout detect threshold value for TMO counter value comparison. When the TMO counter over the threshold, the calibration timeout is happened. The timeout threshold equals (register value)*BASE. When URT0_BR_MDS sets 'Separated', the BASE value is 0x10 and value 0 indicates counter overflow value 0xFF. When URT0_BR_MDS sets 'Combined', the BASE value is 0x100 and value 0 indicates counter overflow value 0xFFF. When calibration has finished, the TMO counter value will be copied to update the baud-rate generator BRO timer. If calibration timeout is happened, the BRO timer will keep the old baud-rate setting.	0x00
27..24	rw	URT2_BKTMO_TH	UART receive Break timeout detect threshold value by using receive bit time. The timeout threshold is starting after URTx_BKF bit asserting when hardware detect a Break character. Value 0 indicates 1 bit time.	0x00
23..16	rw	URT2_RXTMO_TH	UART RX data buffer timeout detect threshold value by using receive bit time. The timeout threshold is starting after STOP bit of the last character. The timeout threshold equal (register value+1)*8 (receive bit time) and value 0 indicates 8 bits time.	0x00
15	rw	URT2_TMO_LCK	UART timeout timer timeout signal initial state control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	0x00
14	rw	URT2_TMO_STA	UART timeout timer timeout signal initial state. The bit is written effectively only by written 1 to URTx_TMO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
13..11	-	Reserved	Reserved	0x00
10..8	rw	URT2_TMO_CKS	UART timeout timer clock source select. When URTx_TMO_MDS selects 'UART' mode, this register must select CK_URTx_BIT(UART) as TMO timer clock for normal operation. When selects 'Noise' and sets URTx_TMO_EN=1, the number of received noise bit is able to read from URTx_TMO_CNT. 0x0 = UART (CK_URTx_BIT clock) 0x1 = Input (CK_UART clock input) 0x2 = Noise (Noise bit receive event) 0x3 = Reserved	0x00
7	rw	URT2_CALTMO_EN	UART Calibration timeout detection enable bit. When enables and URTx_CAL_AUTO=1 if Break condition has detected, chip will trigger timer-out timer to start counting. After the Calibration timeout detection and the corrected auto-sync-field has not received, UART will assert Calibration timeout flag	0x00

			and do not update the BR counter reload value of calibration result. 0 = Disable 1 = Enable	
6	rw	URT2_BKTMO_EN	UART Break timeout detection enable bit. When enables and Break condition has detected, chip will trigger time-out timer to start counting. After Break timeout detection, UART will assert Break timeout flag. 0 = Disable 1 = Enable	0x00
5	rw	URT2_RXTMO_EN	UART RX timeout enable bit for shadow buffer data loading into URTx_RDAT. When timeout happened and shadow buffer storing data >=1 byte, chip will load shadow buffer into URTx_RDAT register even though it is not over the receive threshold URTx_RX_TH. User can read data to speed process. 0 = Disable 1 = Enable	0x00
4	rw	URT2_IDTMO_EN	UART Idle timeout detection enable bit. When enables and Idle timeout has detected, UART will assert idle timeout flag. The time is starting after STOP bit of the last character. (for SmartCard maximum guard-time) 0 = Disable 1 = Enable	0x00
3..2	rw	URT2_TMO_MDS	UART timeout timer mode select. When selects general timer, the timer auto reload function is enabled and URTx_IDTMO_TH is used as the auto reload register. 0x0 = UART (UART timeout timer) 0x1 = General (general timer)	0x00
1	rw	URT2_TMO_RST	UART timeout timer force reset enable. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
0	rw	URT2_TMO_EN	UART timeout timer enable. 0 = Disable 1 = Enable	0x00

1.21.18. URT2 timeout control register 2

URT2_TMOUT2	URT2 timeout control register 2		
Offset Address :	0x44	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
URT2_TMO_CNT[15:8]							
23	22	21	20	19	18	17	16
URT2_TMO_CNT[7:0]							
15	14	13	12	11	10	9	8
URT2_IDTMO_TH[15:8]							
7	6	5	4	3	2	1	0
URT2_IDTMO_TH[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	rw	URT2_TMO_CNT	UART timeout counter value.	0x0000
15..0	rw	URT2_IDTMO_TH	UART receive idle timeout detect threshold value by using receive bit time. The timeout threshold is starting after STOP bit of the last character and value 1 indicates 1 bit time. When selects general timer in URTx_TMO_MDS, the timer auto reload function is enabled and URTx_IDTMO_TH is used as the auto reload register.	0x0000

1.21.19. URT2 SmartCard control register

URT2_SC	URT2 SmartCard control register		
Offset Address :	0x48	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	URT2_RXE_NUM[2:0]			Reserved	URT2_TXE_NUM[2:0]		
7	6	5	4	3	2	1	0
Reserved			URT2_RXE_LEN	URT2_TXE_MDS[1:0]		URT2_RXE_MDS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	-	Reserved	Reserved	0x00
14..12	rw	URT2_RXE_NUM	UART RX parity error detect and NACK transmission retry maximum number. When the register value >0, chip will retry to pull low on RX line and receive data. This register set the retry maximum number for continuous RX error retry. Value 0 indicates to disable hardware auto retry.	0x00
11	-	Reserved	Reserved	0x00
10..8	rw	URT2_TXE_NUM	UART TX error detect and data resend maximum number. When the register value >0, chip will resend the shift buffer data. This register set the resend maximum number for continuous TX error detection. Value 0 indicates to disable hardware auto resending.	0x00
7..5	-	Reserved	Reserved	0x00
4	rw	URT2_RXE_LEN	UART RX parity error detect and NACK transmission (pull low on RX line) bit time length select. 0x0 = 1Bit 0x1 = 2Bit	0x00
3..2	rw	URT2_TXE_MDS	UART TX error detect mode select. It must be noticed that the URTx_TX pin needs to set open-drain mode when enables the TX error detect function. 0x0 = Disable 0x1 = CHK_Low : check asserted low by RX device (for SmartCard) 0x2 = CHK_TX : check TX data by RX input data (for LIN mode) 0x3 = Reserved	0x00
1..0	rw	URT2_RXE_MDS	UART RX parity error detect control mode select. When enables and detects parity error, chip will pull low on RX line during STOP bit cycle and retry to receive new data but not assert interrupt. It must be noticed that the URTx_RX pin needs to set open-drain mode when enables the parity error detect function. Value 0 indicates to disable hardware auto retry. 0x0 = Disable 0x1 = Enable : hardware RX auto retry number by setting URTx_RXE_NUM 0x2 = Auto : hardware RX auto retry always unless receiving parity correct character	0x00

1.21.20. URT2 slave address detect register

URT2_SADR	URT2 slave address detect register		
Offset Address :	0x4C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
URT2_SA_MSK[7:0]							
7	6	5	4	3	2	1	0
URT2_SA_RX[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..8	rw	URT2_SA_MSK	UART multi-processor slave address mask register. URTx_SA_RX register is combined with URTx_SA_MSK register to form Given/Broadcast Address for automatic address recognition. In fact, URTx_SA_MSK functions as the 'mask' register for URTx_SA_RX register. The slave address is created by taking the logical OR of URTx_SA_RX and URTx_SA_MSK. Zero in this result is considered as 'don't care'. (Value 0x00 indicates to enter multi-processor monitor mode.)	0x00
7..0	rw	URT2_SA_RX	UART multi-processor mode received slave address. When URTx_MDS select multi-processor mode and URTx_SA_MSK=0x00, UART enter multi-processor monitor mode and the input slave address value can be read from URTx_RCAP register.	0x00

1.21.21. URT2 calibration control register

URT2_CAL	URT2 calibration control register		
Offset Address :	0x50	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
URT2_CALC_HE	Reserved			URT2_CAL_MDS[1:0]		URT2_CAL_AUTO	URT2_CAL_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	rw	URT2_CALC_HE	UART auto baud-rate calibration complete data receive hold enable. When enables, the receive data will be hold from shift buffer to shadow buffer after auto baud-rate calibration complete. 0 = Disable 1 = Enable	0x00
6..4	-	Reserved	Reserved	0x00
3..2	rw	URT2_CAL_MDS	UART auto baud-rate calibration mode select. 0x0 = Start : measure the start bit 0x1 = Edge : measure start falling edge to next falling edge 0x2 = Reserved 0x3 = Reserved	0x00
1	rw	URT2_CAL_AUTO	UART Break detection and auto baud-rate calibration enable. When enables, hardware will auto enable baud-rate calibration after detect Break condition. When the calibration is finished and the URTx_CALCF is asserted.	0x00

			0 = Disable 1 = Enable	
0	rw	URT2_CAL_EN	UART baud-rate calibration enable. When enables, calibration will start after receive expected character. This bit will clear by hardware after calibration stop. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00

1.21.22. URT2 IrDA control register

URT2_IRDA	URT2 IrDA control register		
Offset Address :	0x54	Reset Value :	0x00000300

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				URT2_IR_PW[3:0]			
7	6	5	4	3	2	1	0
Reserved						URT2_IR_MDS	URT2_IR_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	-	Reserved	Reserved	0x00
11..8	rw	URT2_IR_PW	UART IrDA output pulse width select. IrDA pulse width = (URTx_IR_PW+1) * T<CK_URTx_TX>. The value needs small than URTx_TXOS_NUM. Note : (1) When URTx_IR_PW value equals URTx_TXOS_NUM value, the output is keep low during data bit cycle. (2) When URTx_IR_PW value is large URTx_TXOS_NUM value, the output is keep high during data bit cycle.	0x03
7..2	-	Reserved	Reserved	0x00
1	rw	URT2_IR_MDS	UART IrDA data received mode select. When selects Normal and over-sampling mode URTx_OS_MDS sets Three, the IrDA sampling sequence value need equal 000 then output bit value 0 and others output 1. When selects Wide and over-sampling mode URTx_OS_MDS sets Three, the IrDA sampling sequence value need equal 000,001,010,100 then output bit value 0 and others output 1. 0 = Normal 1 = Wide	0x00
0	rw	URT2_IR_EN	UART IrDA data format enable. When enables, the IrDA encoder and decoder enable for data stream. 0 = Disable 1 = Enable	0x00

1.21.23. URT2 hardware flow control register

URT2_HFC	URT2 hardware flow control register		
Offset Address :	0x58	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0

Reserved	Reserved	Reserved	URT2_RTS_OUT	URT2_RTS_INV	URT2_CTS_INV	URT2_RTS_EN	URT2_CTS_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	rw	URT2_RTS_OUT	URTx_RTS output control data bit. This bit is no effect when URTx_RTS_EN is set. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
3	rw	URT2_RTS_INV	URTx_RTS output inverse enable. When URTx_EN is disabled and the RTS output is set by URTx_RTS_OUT register, the bit does not affect the RTS output. 0 = Disable 1 = Enable	0x00
2	rw	URT2_CTS_INV	URTx_CTS input inverse enable. 0 = Disable 1 = Enable	0x00
1	rw	URT2_RTS_EN	UART RTS hardware flow control enable. When enables, URTx_RTS signal will output high if RX buffer is full. It will change URTx_RTS to low when RX buffer is not full or under threshold. 0 = Disable 1 = Enable	0x00
0	rw	URT2_CTS_EN	UART CTS hardware flow control enable. When enables, transmitter will hold data transmission and enter idle state if detect URTx_RTS signal high. It will automatically transmit next data when URTx_RTS change to low. 0 = Disable 1 = Enable	0x00

1.21.24. URT2 mute control register

URT2_MUTE	URT2 mute control register		
Offset Address :	0x5C	Reset Value :	0x00010100

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved					URT2_MUTE_AEX2	URT2_MUTE_AEX1	URT2_MUTE_AEX0
15	14	13	12	11	10	9	8
Reserved						URT2_MUTE_AEN1	URT2_MUTE_AEN0
7	6	5	4	3	2	1	0
Reserved							URT2_MUTE_EN

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..19	-	Reserved	Reserved	0x00
18	rw	URT2_MUTE_AEX2	UART auto exit mute mode and receive data by idle line detection enable bit. When UART enters mute mode and this bit enables, it will disable mute condition and exit mute mode if has detected the defined idle-line by setting threshold timer in URTx_DET_IDL. 0 = Disable 1 = Enable	0x00
17	rw	URT2_MUTE_AEX1	UART auto exit mute mode and receive data by Break condition detection enable bit. When UART enters mute mode and this bit enables, it will disable mute condition and exit mute mode if has	0x00

			detected Break condition. 0 = Disable 1 = Enable	
16	rw	**URT2_MUTE_AEX0**	UART auto exit mute mode and receive data by multi-processor slave address matched condition enable bit.. When UART enters mute mode and this bit enables, it will disable mute condition and exit mute mode if has received the defined address in URTx_SADR(URTx_MDS=0x2 or 0x3).(Default 1) 0 = Disable 1 = Enable	0x01
15..10	-	**Reserved**	Reserved	0x00
9	rw	**URT2_MUTE_AEN1**	UART mute mode auto enter by idle line detection enable bit. When enables auto mode, UART will enter mute mode after detect the defined idle-line by setting threshold timer in URTx_DET_IDL. 0 = Disable 1 = Enable	0x00
8	rw	**URT2_MUTE_AEN0**	UART mute mode auto enter by multi-processor slave address unmatched condition enable bit. When enables auto mode, UART will enter mute mode after received the unmatched address in URTx_SADR(URTx_MDS=0x2 or 0x3). 0 = Disable 1 = Enable	0x01
7..1	-	**Reserved**	Reserved	0x00
0	rw	**URT2_MUTE_EN**	UART mute mode enable. When enables, only receives the characters those are idle-line for multi-processor Idle-line mode , data with address bit for multi-processor Address-bit mode or break condition for UART auto calibration mode. Also, the non-address or non-break characters are not received and does not assert the URTx_RXF interrupt. If an address is received, user software can validate the address and reset this bit to continue receiving data. 0 = Disable 1 = Enable	0x00

1.21.25. URT2 Register Map

URT2 Register Map Register Number = 24

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	URT2_STA	Reserved	URT2_CALTMOF	URT2_BKTMOF	URT2_IDTMOF	URT2_RXTMOF	Reserved	URT2_TUDRF	URT2_TXEF	URT2_ROVRF	URT2_NCEF	URT2_FEF	URT2_PEF	Reserved	URT2_CTSF	URT2_IDLF	URT2_BKF	URT2_CALOVF	URT2_CALUDF	URT2_CALCF	URT2_TMOF	URT2_BRTF	URT2_SADRF	Reserved	Reserved	URT2_TXF	URT2_RXF	URT2_RXDF	URT2_LSF	URT2_ERRF	URT2_TCF	URT2_UGF	URT2_RHF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	URT2_INT	Reserved	URT2_CALTMO_IE	URT2_BKTMO_IE	URT2_IDTMO_IE	URT2_RXTMO_IE	Reserved	URT2_TUDR_IE	URT2_TXE_IE	URT2_ROVR_IE	URT2_NCE_IE	URT2_FE_IE	URT2_PE_IE	Reserved	URT2_CTS_IE	URT2_IDL_IE	URT2_BK_IE	Reserved		URT2_CALC_IE	URT2_TMO_IE	URT2_BRT_IE	URT2_SADR_IE	Reserved	Reserved	URT2_TX_IE	URT2_RX_IE	Reserved	URT2_LS_IE	URT2_ERR_IE	URT2_TC_IE	URT2_UG_IE	URT2_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	URT2_CLK	Reserved	URT2_BR_CKS	URT2_CKO_LCK	URT2_CKO_STA	URT2_BRO_LCK	URT2_BRO_STA	URT2_BR_MDS	URT2_BR_EN	Reserved		URT2_TX_CKS [1:0]		Reserved		URT2_RX_CKS [1:0]		Reserved								URT2_ECK_CKS	Reserved	URT2_CLK_CKS	URT2_CLK_EN	URT2_CK_SEL [2:0]			Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	URT2_STA2	Reserved	URT2_TX_LVL [2:0]			Reserved	URT2_RX_LVL [2:0]			Reserved								Reserved	Reserved	Reserved	URT2_CTS	Reserved		Reserved	Reserved	URT2_IR_BUSYF	URT2_BKBF	URT2_NCF	Reserved	Reserved	URT2_ADR	URT2_PAR	URT2_BUSYF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	URT2_CR0	URT2_DMA_TXEN	URT2_DMA_RXEN	URT2_DDTX_EN	Reserved	Reserved	Reserved		Reserved	URT2_LBM_EN	URT2_NCHAR_DIS	URT2_NCHAR_HE	URT2_IDL_MDS	Reserved		URT2_RX_TH[1:0]		URT2_DE_GT[1:0]		URT2_DE_INV	URT2_DE_EN	URT2_TX_INV	URT2_RX_INV	URT2_SYNC_MDS	URT2_IO_SWP	URT2_GSA_EN	URT2_MDS[2:0]			URT2_DAT_LINE	URT2_HDX_EN	URT2_OS_MDS	URT2_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	URT2_CR1	Reserved	Reserved		URT2_TXOS_NUM [4:0]					URT2_TXSTP_LEN [1:0]		URT2_TXMSB_EN	URT2_TXPAR_STK	URT2_TXPAR_POL	URT2_TXPAR_EN	URT2_TXDSIZE [1:0]		Reserved			URT2_RXOS_NUM [4:0]					URT2_RXSTP_LEN [1:0]		URT2_RXMSB_EN	URT2_RXPAR_STK	URT2_RXPAR_POL	URT2_RXPAR_EN	URT2_RXDSIZE [1:0]	
Reset	0x0F400F40	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
0x18	URT2_CR2	URT2_DOUT_IDL [1:0]		URT2_DOUT_MDS	Reserved	URT2_NSSI_EN	URT2_NSS_SWEN	URT2_NSS_INV	URT2_NSSI_INV	Reserved						URT2_NSS_SWI	URT2_NSS_SWO	Reserved								Reserved			URT2_TX_HALT	URT2_TX_EN	URT2_RX_EN	URT2_ADR_TX	URT2_BK_TX
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	URT2_CR3	Reserved								URT2_TXGT_LEN [7:0]								URT2_DET_IDL [7:0]								Reserved			URT2_DET_BK	Reserved	URT2_CPHA	URT2_CPOL	Reserved
Reset	0x00000A00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0

0x20	URT2_CR4	Reserved								Reserved								Reserved	URT2_TNUM[2:0]			Reserved	URT2_RNUM[2:0]			URT2_TDAT_CLR	URT2_RDAT_CLR	URT2_TDAT_INV	URT2_RDAT_INV	Reserved			
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	URT2_RLR	Reserved																Reserved		URT2_PSR[5:0]						URT2_RLR[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	URT2_CNT	Reserved																Reserved		URT2_PSC[5:0]						URT2_CNT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	URT2_RCAP	Reserved																Reserved					URT2_RCAP_ADR	URT2_RCAP_PAR	URT2_RCAP_STP	URT2_RCAP_DAT [7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	URT2_RDAT	URT2_RDAT[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	URT2_TDAT	URT2_TDAT[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	URT2_TDAT3	Reserved								URT2_TDAT3[23:0]																							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	URT2_SBUF	Reserved																URT2_TSBUF[7:0]								URT2_RSBUF[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	URT2_TMOUT	URT2_CALTMO_TH [3:0]				URT2_BKTMO_TH [3:0]				URT2_RXTMO_TH [7:0]								URT2_TMO_LCK	URT2_TMO_STA	Reserved			URT2_TMO_CKS [2:0]			URT2_CALTMO_EN	URT2_BKTMO_EN	URT2_RXTMO_EN	URT2_IDTMO_EN	URT2_TMO_MDS [1:0]		URT2_TMO_RST	URT2_TMO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x44	URT2_TMOUT2	URT2_TMO_CNT[15:0]																URT2_IDTMO_TH[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x48	URT2_SC	Reserved																Reserved	URT2_RXE_NUM[2:0]			Reserved	URT2_TXE_NUM[2:0]			Reserved			URT2_RXE_LEN	URT2_TXE_MDS[1:0]		URT2_RXE_MDS[1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x4C	URT2_SADR	Reserved								Reserved								URT2_SA_MSK[7:0]								URT2_SA_RX[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	URT2_CAL	Reserved																Reserved								URT2_CALC_HE	Reserved			URT2_CAL_MDS[1:0]		URT2_CAL_AUTO	URT2_CAL_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x54	URT2_IRDA	Reserved																Reserved				URT2_IR_PW[3:0]				Reserved						URT2_IR_MDS	URT2_IR_EN
Reset	**0x00000300**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
0x58	URT2_HFC	Reserved																Reserved								Reserved	Reserved	Reserved	URT2_RTS_OUT	URT2_RTS_INV	URT2_CTS_INV	URT2_RTS_EN	URT2_CTS_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x5C	URT2_MUTE	Reserved								Reserved					URT2_MUTE_AEX2	URT2_MUTE_AEX1	URT2_MUTE_AEX0	Reserved						URT2_MUTE_AEN1	URT2_MUTE_AEN0	Reserved							URT2_MUTE_EN
Reset	**0x00010100**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

1.22. URT4 Control Registers

URT4 Control	(URT4) UART Control Module-4
Base Address :	0x52040000

1.22.1. URT4 status register 1

URT4_STA	URT4 status register 1		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved		Reserved
23	22	21	20	19	18	17	16
URT4_ROVRF	Reserved	URT4_FEF	URT4_PEF	Reserved	Reserved	Reserved	Reserved
15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	URT4_BRTF	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0
URT4_TXF	URT4_RXF	Reserved	Reserved	URT4_ERRF	URT4_TCF	URT4_UGF	Reserved

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29	-	Reserved	Reserved	0x00
28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26..25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23	rw	URT4_ROVRF	UART receive overrun error flag. (set by hardware and clear by software writing 1) When receive overrun, hardware will stop to receive next data into data shadow buffer until this flag is cleared. This flag is indicated for following two conditions. (1) When RX shadow buffer is arrived over the RX threshold and the data register has not read out. If shift buffer is filled of next data, this flag is asserted. (2) When Parity error, Frame error, Break detect or Slave-Address detect, has happened and caused RX shadow buffer input holding. If shift buffer is filled of next data, this flag is asserted. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
22	-	Reserved	Reserved	0x00
21	rw	URT4_FEF	UART frame error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
20	rw	URT4_PEF	UART parity error flag. (set by hardware and clear by software writing 1) When multi-processor mode, the parity value is including of address bit. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19	-	Reserved	Reserved	0x00
18	-	Reserved	Reserved	0x00
17	-	Reserved	Reserved	0x00
16	-	Reserved	Reserved	0x00
15	-	Reserved	Reserved	0x00
14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	-	Reserved	Reserved	0x00
11	rw	URT4_BRTF	UART baud-rate generator timer timeout flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00

10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	rw	URT4_TXF	UART transmit data register empty. (set by hardware and clear by hardware or software writing 1) When transmitted shadow buffer is empty and the data register URTx_TDAT will copy to the shadow buffer, this flag is set. This bit is cleared when URTx_TDAT is written or this flag set to 1 by software. The flag is set after UART reset or Idle state. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	rw	URT4_RXF	UART receive data register not empty. (set by hardware and clear by hardware or software writing 1) When received shadow buffer level URTx_RX_LVL is greater than or equal to the shadow buffer threshold URTx_RX_TH setting, this flag is set and the shadow buffer content copy to data register URTx_RDAT. This bit is cleared when URTx_RDAT is read or this flag set to 1 by software. But it does not be cleared when URTx_RDAT is read by SWD debugging. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3	rw	URT4_ERRF	UART error interrupt flag for parity error, frame error, overrun error, receive time out and noise error. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	URT4_TCF	UART transmission complete flag. When both shadow buffer and data register are empty and shift buffer shift out complete, then set this flag. (set by hardware and clear by hardware or software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	rw	URT4_UGF	UART general event flag. It indicates each of URTx_SADRF , URTx_BRTF , URTx_TMOF or URTx_CALCF flag is asserted when this flag is set. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	-	Reserved	Reserved	0x00

1.22.2. URT4 interrupt enable register

URT4_INT	URT4 interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved		Reserved
23	22	21	20	19	18	17	16
URT4_ROVR_IE	Reserved	URT4_FE_IE	URT4_PE_IE	Reserved	Reserved	Reserved	Reserved
15	14	13	12	11	10	9	8
Reserved		Reserved	Reserved	URT4_BRT_IE	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0
URT4_TX_IE	URT4_RX_IE	Reserved	Reserved	URT4_ERR_IE	URT4_TC_IE	URT4_UG_IE	URT4_IEA

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29	-	Reserved	Reserved	0x00

28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26..25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23	rw	URT4_ROVR_IE	UART receive overrun error interrupt enable. Refer to the register descriptions of URTx_ROVRF for the detail. 0 = Disable 1 = Enable	0x00
22	-	Reserved	Reserved	0x00
21	rw	URT4_FE_IE	UART frame error interrupt enable. 0 = Disable 1 = Enable	0x00
20	rw	URT4_PE_IE	UART parity error interrupt enable. 0 = Disable 1 = Enable	0x00
19	-	Reserved	Reserved	0x00
18	-	Reserved	Reserved	0x00
17	-	Reserved	Reserved	0x00
16	-	Reserved	Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	-	Reserved	Reserved	0x00
11	rw	URT4_BRT_IE	UART baud-rate generator timer timeout interrupt enable. 0 = Disable 1 = Enable	0x00
10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	rw	URT4_TX_IE	UART transmit data register empty interrupt enable. Refer to the register descriptions of URTx_TXF for the detail. 0 = Disable 1 = Enable	0x00
6	rw	URT4_RX_IE	UART receive data register not empty interrupt enable. Refer to the register descriptions of URTx_RXF for the detail. 0 = Disable 1 = Enable	0x00
5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3	rw	URT4_ERR_IE	UART error interrupt enable for parity error, frame error, overrun error, receive time out and noise error. 0 = Disable 1 = Enable	0x00
2	rw	URT4_TC_IE	UART transmission complete interrupt enable. (set by hardware and clear by hardware or software writing 1) 0 = Disable 1 = Enable	0x00
1	rw	URT4_UG_IE	UART general event interrupt enable for URTx_SADRF , URTx_TF , URTx_RCNTF or URTx_TCNTF events. 0 = Disable 1 = Enable	0x00
0	rw	URT4_IEA	UART interrupt all enable. When disables, the UART global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.22.3. URT4 clock source register

URT4_CLK	URT4 clock source register		
Offset Address :	0x08	**Reset Value :**	0x00000000

31	30	29	28	27	26	25	24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	URT4_BR_MDS	URT4_BR_EN
23	22	21	20	19	18	17	16
Reserved		Reserved		Reserved		Reserved	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	URT4_CK_SEL[2:0]			Reserved

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29	-	Reserved	Reserved	0x00
28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26	-	Reserved	Reserved	0x00
25	rw	URT4_BR_MDS	UART baud-rate timer mode select. Combined mode is only using for general purpose counter. When SmartCard mode, this bit need set to 'Separated' for SmartCard clock output from PSC output. 0 = Separated : Separated PSC and CNT counters for UART baud-rate generator 1 = Combined : Combine to a linear counter for general using timer	0x00
24	rw	URT4_BR_EN	UART baud-rate timer enable. When enables, the baud-rate timer 0 = Disable 1 = Enable	0x00
23..22	-	Reserved	Reserved	0x00
21..20	-	Reserved	Reserved	0x00
19..18	-	Reserved	Reserved	0x00
17..16	-	Reserved	Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3..1	rw	URT4_CK_SEL	UART internal clock CK_URTx source select. 0x0 = PROC : CK_URTx_PR process clock from CSC 0x1 = NCO_P0 0x2 = CK_LS 0x3 = TM00_TRGO	0x00
0	-	Reserved	Reserved	0x00

1.22.4. URT4 status register 2

URT4_STA2	URT4 status register 2		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	Reserved			Reserved	Reserved		
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved		Reserved	Reserved
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	URT4_PAR	URT4_BUSYF

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30..28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15	-	Reserved	Reserved	0x00
14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	-	Reserved	Reserved	0x00
11..10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	r	URT4_PAR	UART data receive parity bit of shift buffer. When multi-processor mode, the parity value is including of address bit.	0x00
0	r	URT4_BUSYF	UART RX busy flag. (set and clear by hardware) When detect valid start bit, this bit is set and clear after stop bit. 0 = Normal (No event occurred) 1 = Busy (Event happened)	0x00

1.22.5. URT4 control register 0

URT4_CR0	URT4 control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	Reserved	Reserved	Reserved				Reserved
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
URT4_LBM_EN	Reserved	Reserved	Reserved	Reserved		Reserved	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved		Reserved	Reserved	URT4_TX_INV	URT4_RX_INV	Reserved	URT4_IO_SWP
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	Reserved			Reserved	Reserved	Reserved	URT4_EN

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29	-	Reserved	Reserved	0x00
28..25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23	rw	URT4_LBM_EN	UART loop back mode enable bit. When enables, the received input is taken from transmitted output to replace from input pin(RX ->TX). 0 = Disable 1 = Enable	0x00
22	-	Reserved	Reserved	0x00
21	-	Reserved	Reserved	0x00
20	-	Reserved	Reserved	0x00
19..18	-	Reserved	Reserved	0x00
17..16	-	Reserved	Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	-	Reserved	Reserved	0x00

11	rw	URT4_TX_INV	URTx_TX output signal inverse enable. 0 = Disable 1 = Enable	0x00
10	rw	URT4_RX_INV	URTx_RX input signal inverse enable. 0 = Disable 1 = Enable	0x00
9	-	Reserved	Reserved	0x00
8	rw	URT4_IO_SWP	URTx_RX/URTx_TX swap enable bit. 0 = Disable 1 = Enable	0x00
7	-	Reserved	Reserved	0x00
6..4	-	Reserved	Reserved	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	-	Reserved	Reserved	0x00
0	rw	URT4_EN	UART function enable bit. 0 = Disable 1 = Enable	0x00

1.22.6. URT4 control register 1

URT4_CR1	URT4 control register 1		
Offset Address :	0x14	Reset Value :	0x0F400000

31	30	29	28	27	26	25	24
Reserved			URT4_TXOS_NUM[4:0]				
23	22	21	20	19	18	17	16
URT4_TXSTP_LEN[1:0]		Reserved	URT4_TXPAR_STK	URT4_TXPAR_POL	URT4_TXPAR_EN	URT4_TXDSIZE[1:0]	
15	14	13	12	11	10	9	8
Reserved			Reserved				
7	6	5	4	3	2	1	0
Reserved		Reserved	URT4_RXPAR_STK	URT4_RXPAR_POL	Reserved	Reserved	

Bit	Attr	Bit Name	Description	Reset
31..29	-	Reserved	Reserved	0x00
28..24	rw	URT4_TXOS_NUM	UART TX data oversampling samples select. The valid value is from 3 to 31 for oversampling samples from 4 to 32. (This register is written no effect if URTx_TX_EN set 1.)	0x0F
23..22	rw	URT4_TXSTP_LEN	UART TX stop bit length select. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = Reserved 0x1 = 1bit 0x2 = Reserved 0x3 = 2bit	0x01
21	-	Reserved	Reserved	0x00
20	rw	URT4_TXPAR_STK	UART stuck parity bit output enable. When enables and URTx_TXPAR_EN=1, parity bit output fixed value by URTx_TXPAR_POL value setting. 0 = Disable 1 = Enable	0x00
19	rw	URT4_TXPAR_POL	UART TX parity bit polarity. This bit is no effect for SPI and SYNC mods. 0x0 = Even 0x1 = Odd	0x00
18	rw	URT4_TXPAR_EN	UART TX parity bit enable. This bit does not be set for SYNC mods. (This register is written no effect if URTx_TX_EN set 1.) 0 = Disable 1 = Enable	0x00
17..16	rw	URT4_TXDSIZE	UART TX data bit length. It is not including START, STOP, ADR or PARITY bits. (This register is written no effect if	0x00

			URTx_TX_EN set 1.) 0x0 = 8bit 0x1 = 7bit 0x2 = Reserved 0x3 = Reserved	
15..13	-	Reserved	Reserved	0x00
12..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	rw	URT4_RXPAR_STK	UART stuck parity bit input enable. When enables and URTx_RXPAR_EN=1, parity bit input fixed value by URTx_RXPAR_POL value setting. 0 = Disable 1 = Enable	0x00
3	rw	URT4_RXPAR_POL	UART RX parity bit polarity. This bit is no effect for SYNC mods. 0x0 = Even 0x1 = Odd	0x00
2	-	Reserved	Reserved	0x00
1..0	-	Reserved	Reserved	0x00

1.22.7. URT4 control register 2

URT4_CR2	URT4 control register 2		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23	22	21	20	19	18	17	16
Reserved						Reserved	Reserved
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			Reserved	URT4_TX_EN	URT4_RX_EN	Reserved	Reserved

Bit	Attr	Bit Name	Description	Reset
31..30	-	Reserved	Reserved	0x00
29	-	Reserved	Reserved	0x00
28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26	-	Reserved	Reserved	0x00
25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23..18	-	Reserved	Reserved	0x00
17	-	Reserved	Reserved	0x00
16	-	Reserved	Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7..5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3	rw	URT4_TX_EN	UART transmitter enable. 0 = Disable 1 = Enable	0x00
2	rw	URT4_RX_EN	UART receiver enable. 0 = Disable 1 = Enable	0x00
1	-	Reserved	Reserved	0x00
0	-	Reserved	Reserved	0x00

1.22.8. URT4 baud-rate clock counter reload register

URT4_RLR	URT4 baud-rate clock counter reload register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		URT4_PSR[5:0]					
7	6	5	4	3	2	1	0
URT4_RLR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..8	rw	URT4_PSR	UART baud-rate clock prescaler reload register. Actual value equals the register value plus one.	0x00
7..0	rw	URT4_RLR	UART baud-rate clock counter reload register. Actual value equals the register value plus one.	0x00

1.22.9. URT4 baud-rate clock counter register

URT4_CNT	URT4 baud-rate clock counter register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		URT4_PSC[5:0]					
7	6	5	4	3	2	1	0
URT4_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..8	r	URT4_PSC	UART baud-rate clock prescaler value register.	0x00
7..0	r	URT4_CNT	UART baud-rate clock counter value register.	0x00

1.22.10. URT4 RX data register

URT4_RDAT	URT4 RX data register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
URT4_RDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	r	URT4_RDAT	UART received data register. Read this register will clear the URTx_RXF. Hardware will force to logic 0 for non-updated	0x00

			byte(s) by URTx_RX_TH setting.	

1.22.11. URT4 TX data register

URT4_TDAT	URT4 TX data register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
URT4_TDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	URT4_TDAT	UART transmitted data register. Write this register will clear the URTx_TXF. When write data by word, half-word or byte operation, chip will transfer 4-byte, 2-byte, or 1-byte data to shadow buffer. (write-only)	0x00

1.22.12. URT4 data shift buffer register

URT4_SBUF	URT4 data shift buffer register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
URT4_TSBUF[7:0]							
7	6	5	4	3	2	1	0
URT4_RSBUF[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	r	URT4_TSBUF	UART TX data shift buffer register.	0x00
7..0	r	URT4_RSBUF	UART RX data shift buffer register.	0x00

1.22.13. URT4 Register Map

URT4 Register Map Register Number = 12

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	URT4_STA	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved		Reserved	URT4_ROVRF	Reserved	URT4_FEF	URT4_PEF	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	URT4_BRTF	Reserved	Reserved	Reserved	URT4_TXF	URT4_RXF	Reserved	Reserved	URT4_ERRF	URT4_TCF	URT4_UGF	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	URT4_INT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved		Reserved	URT4_ROVR_IE	Reserved	URT4_FE_IE	URT4_PE_IE	Reserved	Reserved	Reserved	Reserved	Reserved		Reserved	Reserved	URT4_BRT_IE	Reserved	Reserved	Reserved	URT4_TX_IE	URT4_RX_IE	Reserved	Reserved	URT4_ERR_IE	URT4_TC_IE	URT4_UG_IE	URT4_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	URT4_CLK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	URT4_BR_MDS	URT4_BR_EN	Reserved		Reserved		Reserved		Reserved		Reserved								Reserved	Reserved	Reserved	Reserved	URT4_CK_SEL [2:0]			Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	URT4_STA2	Reserved	Reserved			Reserved	Reserved			Reserved								Reserved	Reserved	Reserved	Reserved	Reserved		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	URT4_PAR	URT4_BUSYF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	URT4_CR0	Reserved	Reserved	Reserved	Reserved				Reserved	URT4_LBM_EN	Reserved	Reserved	Reserved	Reserved		Reserved		Reserved		Reserved	Reserved	URT4_TX_INV	URT4_RX_INV	Reserved	URT4_IO_SWP	Reserved	Reserved			Reserved	Reserved	Reserved	URT4_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	URT4_CR1	Reserved			URT4_TXOS_NUM [4:0]					URT4_TXSTP_LEN [1:0]		Reserved	URT4_TXPAR_STK	URT4_TXPAR_POL	URT4_TXPAR_EN	URT4_TXDSIZE [1:0]		Reserved			Reserved					Reserved		Reserved	URT4_RXPAR_STK	URT4_RXPAR_POL	Reserved	Reserved	
Reset	**0x0F400000**	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	URT4_CR2	Reserved		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved						Reserved	Reserved	Reserved								Reserved			Reserved	URT4_TX_EN	URT4_RX_EN	Reserved	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	URT4_RLR	Reserved																Reserved		URT4_PSR[5:0]						URT4_RLR[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x28	URT4_CNT	Reserved																Reserved		URT4_PSC[5:0]						URT4_CNT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	URT4_RDAT	Reserved																Reserved								URT4_RDAT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	URT4_TDAT	Reserved																Reserved								URT4_TDAT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	URT4_SBUF	Reserved																URT4_TSBUF[7:0]								URT4_RSBUF[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.23. URT5 Control Registers

URT5 Control	(URT5) UART Control Module-5
Base Address :	0x52050000

1.23.1. URT5 status register 1

URT5_STA	URT5 status register 1		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT5_ROVRF	Reserved	URT5_FEF	URT5_PEF	Reserved			
15	14	13	12	11	10	9	8
Reserved				URT5_BRTF	Reserved		
7	6	5	4	3	2	1	0
URT5_TXF	URT5_RXF	Reserved		URT5_ERRF	URT5_TCF	URT5_UGF	Reserved

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23	rw	URT5_ROVRF	UART receive overrun error flag. (set by hardware and clear by software writing 1) When receive overrun, hardware will stop to receive next data into data shadow buffer until this flag is cleared. This flag is indicated for following two conditions. (1) When RX shadow buffer is arrived over the RX threshold and the data register has not read out. If shift buffer is filled of next data, this flag is asserted. (2) When Parity error, Frame error, Break detect or Slave-Address detect, has happened and caused RX shadow buffer input holding. If shift buffer is filled of next data, this flag is asserted. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
22	-	Reserved	Reserved	0x00
21	rw	URT5_FEF	UART frame error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
20	rw	URT5_PEF	UART parity error flag. (set by hardware and clear by software writing 1) When multi-processor mode, the parity value is including of address bit. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19..16	-	Reserved	Reserved	0x00
15..12	-	Reserved	Reserved	0x00
11	rw	URT5_BRTF	UART baud-rate generator timer timeout flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
10..8	-	Reserved	Reserved	0x00
7	rw	URT5_TXF	UART transmit data register empty. (set by hardware and clear by hardware or software writing 1) When transmitted shadow buffer is empty and the data register URTx_TDAT will copy to the shadow buffer, this flag is set. This bit is cleared when URTx_TDAT is written or this flag set to 1 by software. The flag is set after UART reset or Idle state. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	rw	URT5_RXF	UART receive data register not empty. (set by hardware and clear by hardware or software writing 1) When received shadow buffer level URTx_RX_LVL is greater than or equal to	0x00

			the shadow buffer threshold URTx_RX_TH setting, this flag is set and the shadow buffer content copy to data register URTx_RDAT. This bit is cleared when URTx_RDAT is read or this flag set to 1 by software. But it does not be cleared when URTx_RDAT is read by SWD debugging. 0 = Normal (No event occurred) 1 = Happened (Event happened)	
5..4	-	Reserved	Reserved	0x00
3	rw	URT5_ERRF	UART error interrupt flag for parity error, frame error, overrun error, receive time out and noise error. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	URT5_TCF	UART transmission complete flag. When both shadow buffer and data register are empty and shift buffer shift out complete, then set this flag. (set by hardware and clear by hardware or software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	rw	URT5_UGF	UART general event flag. It indicates each of URTx_SADRF , URTx_BRTF , URTx_TMOF or URTx_CALCF flag is asserted when this flag is set. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	-	Reserved	Reserved	0x00

1.23.2. URT5 interrupt enable register

URT5_INT	URT5 interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT5_ROVR_IE	Reserved	URT5_FE_IE	URT5_PE_IE	Reserved			
15	14	13	12	11	10	9	8
Reserved				URT5_BRT_IE	Reserved		
7	6	5	4	3	2	1	0
URT5_TX_IE	URT5_RX_IE	Reserved		URT5_ERR_IE	URT5_TC_IE	URT5_UG_IE	URT5_IEA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23	rw	URT5_ROVR_IE	UART receive overrun error interrupt enable. Refer to the register descriptions of URTx_ROVRF for the detail. 0 = Disable 1 = Enable	0x00
22	-	Reserved	Reserved	0x00
21	rw	URT5_FE_IE	UART frame error interrupt enable. 0 = Disable 1 = Enable	0x00
20	rw	URT5_PE_IE	UART parity error interrupt enable. 0 = Disable 1 = Enable	0x00
19..16	-	Reserved	Reserved	0x00
15..12	-	Reserved	Reserved	0x00
11	rw	URT5_BRT_IE	UART baud-rate generator timer timeout interrupt enable. 0 = Disable 1 = Enable	0x00
10..8	-	Reserved	Reserved	0x00

7	rw	URT5_TX_IE	UART transmit data register empty interrupt enable. Refer to the register descriptions of URTx_TXF for the detail. 0 = Disable 1 = Enable	0x00
6	rw	URT5_RX_IE	UART receive data register not empty interrupt enable. Refer to the register descriptions of URTx_RXF for the detail. 0 = Disable 1 = Enable	0x00
5..4	-	Reserved	Reserved	0x00
3	rw	URT5_ERR_IE	UART error interrupt enable for parity error, frame error, overrun error, receive time out and noise error. 0 = Disable 1 = Enable	0x00
2	rw	URT5_TC_IE	UART transmission complete interrupt enable. (set by hardware and clear by hardware or software writing 1) 0 = Disable 1 = Enable	0x00
1	rw	URT5_UG_IE	UART general event interrupt enable for URTx_SADRF , URTx_TF , URTx_RCNTF or URTx_TCNTF events. 0 = Disable 1 = Enable	0x00
0	rw	URT5_IEA	UART interrupt all enable. When disables, the UART global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.23.3. URT5 clock source register

URT5_CLK	URT5 clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				Reserved	Reserved	URT5_BR_MDS	URT5_BR_EN
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				URT5_CK_SEL[2:0]			Reserved

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26	-	Reserved	Reserved	0x00
25	rw	URT5_BR_MDS	UART baud-rate timer mode select. Combined mode is only using for general purpose counter. When SmartCard mode, this bit need set to 'Separated' for SmartCard clock output from PSC output. 0 = Separated : Separated PSC and CNT counters for UART baud-rate generator 1 = Combined : Combine to a linear counter for general using timer	0x00
24	rw	URT5_BR_EN	UART baud-rate timer enable. When enables, the baud-rate timer 0 = Disable 1 = Enable	0x00
23..16	-	Reserved	Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00

3..1	rw	URT5_CK_SEL	UART internal clock CK_URTx source select. 0x0 = PROC : CK_URTx_PR process clock from CSC 0x1 = NCO_P0 0x2 = CK_LS 0x3 = TM00_TRGO	0x00
0	-	Reserved	Reserved	0x00

1.23.4. URT5 status register 2

URT5_STA2	URT5 status register 2		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						URT5_PAR	URT5_BUSYF

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..2	-	Reserved	Reserved	0x00
1	r	URT5_PAR	UART data receive parity bit of shift buffer. When multi-processor mode, the parity value is including of address bit.	0x00
0	r	URT5_BUSYF	UART RX busy flag. (set and clear by hardware) When detect valid start bit, this bit is set and clear after stop bit. 0 = Normal (No event occurred) 1 = Busy (Event happened)	0x00

1.23.5. URT5 control register 0

URT5_CR0	URT5 control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT5_LBM_EN	Reserved						
15	14	13	12	11	10	9	8
Reserved				URT5_TX_INV	URT5_RX_INV	Reserved	URT5_IO_SWP
7	6	5	4	3	2	1	0
Reserved							URT5_EN

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23	rw	URT5_LBM_EN	UART loop back mode enable bit. When enables, the received input is taken from transmitted output to replace from input pin(RX ->TX). 0 = Disable 1 = Enable	0x00
22..16	-	Reserved	Reserved	0x00
15..12	-	Reserved	Reserved	0x00
11	rw	URT5_TX_INV	URTx_TX output signal inverse enable. 0 = Disable 1 = Enable	0x00
10	rw	URT5_RX_INV	URTx_RX input signal inverse enable.	0x00

			0 = Disable 1 = Enable	
9	-	Reserved	Reserved	0x00
8	rw	URT5_IO_SWP	URTx_RX/URTx_TX swap enable bit. 0 = Disable 1 = Enable	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	URT5_EN	UART function enable bit. 0 = Disable 1 = Enable	0x00

1.23.6. URT5 control register 1

URT5_CR1	URT5 control register 1		
Offset Address :	0x14	Reset Value :	0x0F400000

31	30	29	28	27	26	25	24
Reserved			URT5_TXOS_NUM[4:0]				
23	22	21	20	19	18	17	16
URT5_TXSTP_LEN[1:0]		Reserved	URT5_TXPAR_STK	URT5_TXPAR_POL	URT5_TXPAR_EN	URT5_TXDSIZE[1:0]	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			URT5_RXPAR_STK	URT5_RXPAR_POL	Reserved		

Bit	Attr	Bit Name	Description	Reset
31..29	-	Reserved	Reserved	0x00
28..24	rw	URT5_TXOS_NUM	UART TX data oversampling samples select. The valid value is from 3 to 31 for oversampling samples from 4 to 32. (This register is written no effect if URTx_TX_EN set 1.)	0x0F
23..22	rw	URT5_TXSTP_LEN	UART TX stop bit length select. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = Reserved 0x1 = 1bit 0x2 = Reserved 0x3 = 2bit	0x01
21	-	Reserved	Reserved	0x00
20	rw	URT5_TXPAR_STK	UART stuck parity bit output enable. When enables and URTx_TXPAR_EN=1, parity bit output fixed value by URTx_TXPAR_POL value setting. 0 = Disable 1 = Enable	0x00
19	rw	URT5_TXPAR_POL	UART TX parity bit polarity. This bit is no effect for SPI and SYNC mods. 0x0 = Even 0x1 = Odd	0x00
18	rw	URT5_TXPAR_EN	UART TX parity bit enable. This bit does not be set for SYNC mods. (This register is written no effect if URTx_TX_EN set 1.) 0 = Disable 1 = Enable	0x00
17..16	rw	URT5_TXDSIZE	UART TX data bit length. It is not including START, STOP, ADR or PARITY bits. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = 8bit 0x1 = 7bit 0x2 = Reserved 0x3 = Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7..5	-	Reserved	Reserved	0x00
4	rw	URT5_RXPAR_STK	UART stuck parity bit input enable. When enables and	0x00

			URTx_RXPAR_EN=1, parity bit input fixed value by URTx_RXPAR_POL value setting. 0 = Disable 1 = Enable	
3	rw	URT5_RXPAR_POL	UART RX parity bit polarity. This bit is no effect for SYNC mods. 0x0 = Even 0x1 = Odd	0x00
2..0	-	Reserved	Reserved	0x00

1.23.7. URT5 control register 2

URT5_CR2	URT5 control register 2		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				URT5_TX_EN	URT5_RX_EN	Reserved	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	URT5_TX_EN	UART transmitter enable. 0 = Disable 1 = Enable	0x00
2	rw	URT5_RX_EN	UART receiver enable. 0 = Disable 1 = Enable	0x00
1..0	-	Reserved	Reserved	0x00

1.23.8. URT5 baud-rate clock counter reload register

URT5_RLR	URT5 baud-rate clock counter reload register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		URT5_PSR[5:0]					
7	6	5	4	3	2	1	0
URT5_RLR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..8	rw	URT5_PSR	UART baud-rate clock prescaler reload register. Actual value equals the register value plus one.	0x00
7..0	rw	URT5_RLR	UART baud-rate clock counter reload register. Actual value equals the register value plus one.	0x00

1.23.9. URT5 baud-rate clock counter register

URT5_CNT	URT5 baud-rate clock counter register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		URT5_PSC[5:0]					
7	6	5	4	3	2	1	0
URT5_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..8	r	URT5_PSC	UART baud-rate clock prescaler value register.	0x00
7..0	r	URT5_CNT	UART baud-rate clock counter value register.	0x00

1.23.10. URT5 RX data register

URT5_RDAT	URT5 RX data register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
URT5_RDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	r	URT5_RDAT	UART received data register. Read this register will clear the URTx_RXF. Hardware will force to logic 0 for non-updated byte(s) by URTx_RX_TH setting.	0x00

1.23.11. URT5 TX data register

URT5_TDAT	URT5 TX data register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
URT5_TDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	URT5_TDAT	UART transmitted data register. Write this register will clear the URTx_TXF. When write data by word, half-word or byte operation, chip will transfer 4-byte, 2-byte, or 1-byte data to	0x00

			shadow buffer. (write-only)	

1.23.12. URT5 data shift buffer register

URT5_SBUF	URT5 data shift buffer register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
URT5_TSBUF[7:0]							
7	6	5	4	3	2	1	0
URT5_RSBUF[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	r	URT5_TSBUF	UART TX data shift buffer register.	0x00
7..0	r	URT5_RSBUF	UART RX data shift buffer register.	0x00

1.23.13. URT5 Register Map

URT5 Register Map Register Number = 12

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	URT5_STA	Reserved								URT5_ROVRF	Reserved	URT5_FEF	URT5_PEF	Reserved				Reserved				URT5_BRTF	Reserved			URT5_TXF	URT5_RXF	Reserved		URT5_ERRF	URT5_TCF	URT5_UGF	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	URT5_INT	Reserved								URT5_ROVR_IE	Reserved	URT5_FE_IE	URT5_PE_IE	Reserved				Reserved				URT5_BRT_IE	Reserved			URT5_TX_IE	URT5_RX_IE	Reserved		URT5_ERR_IE	URT5_TC_IE	URT5_UG_IE	URT5_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	URT5_CLK	Reserved				Reserved	Reserved	URT5_BR_MDS	URT5_BR_EN	Reserved								Reserved								Reserved				URT5_CK_SEL [2:0]			Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	URT5_STA2	Reserved																Reserved								Reserved						URT5_PAR	URT5_BUSYF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	URT5_CR0	Reserved								URT5_LBM_EN	Reserved							Reserved				URT5_TX_INV	URT5_RX_INV	Reserved	URT5_IO_SWP	Reserved							URT5_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	URT5_CR1	Reserved			URT5_TXOS_NUM [4:0]					URT5_TXSTP_LEN [1:0]		Reserved	URT5_TXPAR_STK	URT5_TXPAR_POL	URT5_TXPAR_EN	URT5_TXDSIZE [1:0]		Reserved								Reserved			URT5_RXPAR_STK	URT5_RXPAR_POL	Reserved		
Reset	**0x0F400000**	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	URT5_CR2	Reserved																Reserved								Reserved				URT5_TX_EN	URT5_RX_EN	Reserved	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	URT5_RLR	Reserved																Reserved		URT5_PSR[5:0]						URT5_RLR[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x28	URT5_CNT	Reserved																Reserved		URT5_PSC[5:0]						URT5_CNT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	URT5_RDAT	Reserved																Reserved								URT5_RDAT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	URT5_TDAT	Reserved																Reserved								URT5_TDAT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	URT5_SBUF	Reserved																URT5_TSBUF[7:0]								URT5_RSBUF[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.24. URT6 Control Registers

URT6 Control	(URT6) UART Control Module-6
Base Address :	0x52060000

1.24.1. URT6 status register 1

URT6_STA	URT6 status register 1		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT6_ROVRF	Reserved	URT6_FEF	URT6_PEF	Reserved			
15	14	13	12	11	10	9	8
Reserved				URT6_BRTF	Reserved		
7	6	5	4	3	2	1	0
URT6_TXF	URT6_RXF	Reserved		URT6_ERRF	URT6_TCF	URT6_UGF	Reserved

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23	rw	URT6_ROVRF	UART receive overrun error flag. (set by hardware and clear by software writing 1) When receive overrun, hardware will stop to receive next data into data shadow buffer until this flag is cleared. This flag is indicated for following two conditions. (1) When RX shadow buffer is arrived over the RX threshold and the data register has not read out. If shift buffer is filled of next data, this flag is asserted. (2) When Parity error, Frame error, Break detect or Slave-Address detect, has happened and caused RX shadow buffer input holding. If shift buffer is filled of next data, this flag is asserted. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
22	-	Reserved	Reserved	0x00
21	rw	URT6_FEF	UART frame error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
20	rw	URT6_PEF	UART parity error flag. (set by hardware and clear by software writing 1) When multi-processor mode, the parity value is including of address bit. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19..16	-	Reserved	Reserved	0x00
15..12	-	Reserved	Reserved	0x00
11	rw	URT6_BRTF	UART baud-rate generator timer timeout flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
10..8	-	Reserved	Reserved	0x00
7	rw	URT6_TXF	UART transmit data register empty. (set by hardware and clear by hardware or software writing 1) When transmitted shadow buffer is empty and the data register URTx_TDAT will copy to the shadow buffer, this flag is set. This bit is cleared when URTx_TDAT is written or this flag set to 1 by software. The flag is set after UART reset or Idle state. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	rw	URT6_RXF	UART receive data register not empty. (set by hardware and clear by hardware or software writing 1) When received shadow buffer level URTx_RX_LVL is greater than or equal to	0x00

			the shadow buffer threshold URTx_RX_TH setting, this flag is set and the shadow buffer content copy to data register URTx_RDAT. This bit is cleared when URTx_RDAT is read or this flag set to 1 by software. But it does not be cleared when URTx_RDAT is read by SWD debugging. 0 = Normal (No event occurred) 1 = Happened (Event happened)	
5..4	-	Reserved	Reserved	0x00
3	rw	URT6_ERRF	UART error interrupt flag for parity error, frame error, overrun error, receive time out and noise error. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	URT6_TCF	UART transmission complete flag. When both shadow buffer and data register are empty and shift buffer shift out complete, then set this flag. (set by hardware and clear by hardware or software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	rw	URT6_UGF	UART general event flag. It indicates each of URTx_SADRF , URTx_BRTF , URTx_TMOF or URTx_CALCF flag is asserted when this flag is set. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	-	Reserved	Reserved	0x00

1.24.2. URT6 interrupt enable register

URT6_INT	URT6 interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT6_ROVR_IE	Reserved	URT6_FE_IE	URT6_PE_IE	Reserved			
15	14	13	12	11	10	9	8
Reserved				URT6_BRT_IE	Reserved		
7	6	5	4	3	2	1	0
URT6_TX_IE	URT6_RX_IE	Reserved		URT6_ERR_IE	URT6_TC_IE	URT6_UG_IE	URT6_IEA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23	rw	URT6_ROVR_IE	UART receive overrun error interrupt enable. Refer to the register descriptions of URTx_ROVRF for the detail. 0 = Disable 1 = Enable	0x00
22	-	Reserved	Reserved	0x00
21	rw	URT6_FE_IE	UART frame error interrupt enable. 0 = Disable 1 = Enable	0x00
20	rw	URT6_PE_IE	UART parity error interrupt enable. 0 = Disable 1 = Enable	0x00
19..16	-	Reserved	Reserved	0x00
15..12	-	Reserved	Reserved	0x00
11	rw	URT6_BRT_IE	UART baud-rate generator timer timeout interrupt enable. 0 = Disable 1 = Enable	0x00
10..8	-	Reserved	Reserved	0x00

7	rw	URT6_TX_IE	UART transmit data register empty interrupt enable. Refer to the register descriptions of URTx_TXF for the detail. 0 = Disable 1 = Enable	0x00
6	rw	URT6_RX_IE	UART receive data register not empty interrupt enable. Refer to the register descriptions of URTx_RXF for the detail. 0 = Disable 1 = Enable	0x00
5..4	-	Reserved	Reserved	0x00
3	rw	URT6_ERR_IE	UART error interrupt enable for parity error, frame error, overrun error, receive time out and noise error. 0 = Disable 1 = Enable	0x00
2	rw	URT6_TC_IE	UART transmission complete interrupt enable. (set by hardware and clear by hardware or software writing 1) 0 = Disable 1 = Enable	0x00
1	rw	URT6_UG_IE	UART general event interrupt enable for URTx_SADRF , URTx_TF , URTx_RCNTF or URTx_TCNTF events. 0 = Disable 1 = Enable	0x00
0	rw	URT6_IEA	UART interrupt all enable. When disables, the UART global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.24.3. URT6 clock source register

URT6_CLK	URT6 clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				Reserved	Reserved	URT6_BR_MDS	URT6_BR_EN
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				URT6_CK_SEL[2:0]			Reserved

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26	-	Reserved	Reserved	0x00
25	rw	URT6_BR_MDS	UART baud-rate timer mode select. Combined mode is only using for general purpose counter. When SmartCard mode, this bit need set to 'Separated' for SmartCard clock output from PSC output. 0 = Separated : Separated PSC and CNT counters for UART baud-rate generator 1 = Combined : Combine to a linear counter for general using timer	0x00
24	rw	URT6_BR_EN	UART baud-rate timer enable. When enables, the baud-rate timer 0 = Disable 1 = Enable	0x00
23..16	-	Reserved	Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00

3..1	rw	URT6_CK_SEL	UART internal clock CK_URTx source select. 0x0 = PROC : CK_URTx_PR process clock from CSC 0x1 = NCO_P0 0x2 = CK_LS 0x3 = TM00_TRGO	0x00
0	-	Reserved	Reserved	0x00

1.24.4. URT6 status register 2

URT6_STA2	URT6 status register 2		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						URT6_PAR	URT6_BUSYF

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..2	-	Reserved	Reserved	0x00
1	r	URT6_PAR	UART data receive parity bit of shift buffer. When multi-processor mode, the parity value is including of address bit.	0x00
0	r	URT6_BUSYF	UART RX busy flag. (set and clear by hardware) When detect valid start bit, this bit is set and clear after stop bit. 0 = Normal (No event occurred) 1 = Busy (Event happened)	0x00

1.24.5. URT6 control register 0

URT6_CR0	URT6 control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT6_LBM_EN	Reserved						
15	14	13	12	11	10	9	8
Reserved				URT6_TX_INV	URT6_RX_INV	Reserved	URT6_IO_SWP
7	6	5	4	3	2	1	0
Reserved							URT6_EN

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23	rw	URT6_LBM_EN	UART loop back mode enable bit. When enables, the received input is taken from transmitted output to replace from input pin(RX ->TX). 0 = Disable 1 = Enable	0x00
22..16	-	Reserved	Reserved	0x00
15..12	-	Reserved	Reserved	0x00
11	rw	URT6_TX_INV	URTx_TX output signal inverse enable. 0 = Disable 1 = Enable	0x00
10	rw	URT6_RX_INV	URTx_RX input signal inverse enable.	0x00

			0 = Disable 1 = Enable	
9	-	Reserved	Reserved	0x00
8	rw	URT6_IO_SWP	URTx_RX/URTx_TX swap enable bit. 0 = Disable 1 = Enable	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	URT6_EN	UART function enable bit. 0 = Disable 1 = Enable	0x00

1.24.6. URT6 control register 1

URT6_CR1	URT6 control register 1		
Offset Address :	0x14	Reset Value :	0x0F400000

31	30	29	28	27	26	25	24
Reserved			URT6_TXOS_NUM[4:0]				
23	22	21	20	19	18	17	16
URT6_TXSTP_LEN[1:0]		Reserved	URT6_TXPAR_STK	URT6_TXPAR_POL	URT6_TXPAR_EN	URT6_TXDSIZE[1:0]	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			URT6_RXPAR_STK	URT6_RXPAR_POL	Reserved		

Bit	Attr	Bit Name	Description	Reset
31..29	-	Reserved	Reserved	0x00
28..24	rw	URT6_TXOS_NUM	UART TX data oversampling samples select. The valid value is from 3 to 31 for oversampling samples from 4 to 32. (This register is written no effect if URTx_TX_EN set 1.)	0x0F
23..22	rw	URT6_TXSTP_LEN	UART TX stop bit length select. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = Reserved 0x1 = 1bit 0x2 = Reserved 0x3 = 2bit	0x01
21	-	Reserved	Reserved	0x00
20	rw	URT6_TXPAR_STK	UART stuck parity bit output enable. When enables and URTx_TXPAR_EN=1, parity bit output fixed value by URTx_TXPAR_POL value setting. 0 = Disable 1 = Enable	0x00
19	rw	URT6_TXPAR_POL	UART TX parity bit polarity. This bit is no effect for SPI and SYNC mods. 0x0 = Even 0x1 = Odd	0x00
18	rw	URT6_TXPAR_EN	UART TX parity bit enable. This bit does not be set for SYNC mods. (This register is written no effect if URTx_TX_EN set 1.) 0 = Disable 1 = Enable	0x00
17..16	rw	URT6_TXDSIZE	UART TX data bit length. It is not including START, STOP, ADR or PARITY bits. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = 8bit 0x1 = 7bit 0x2 = Reserved 0x3 = Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7..5	-	Reserved	Reserved	0x00
4	rw	URT6_RXPAR_STK	UART stuck parity bit input enable. When enables and	0x00

Bit	Attr	Bit Name	Description	Reset
			URTx_RXPAR_EN=1, parity bit input fixed value by URTx_RXPAR_POL value setting. 0 = Disable 1 = Enable	
3	rw	URT6_RXPAR_POL	UART RX parity bit polarity. This bit is no effect for SYNC mods. 0x0 = Even 0x1 = Odd	0x00
2..0	-	Reserved	Reserved	0x00

1.24.7. URT6 control register 2

URT6_CR2	URT6 control register 2		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				URT6_TX_EN	URT6_RX_EN	Reserved	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	URT6_TX_EN	UART transmitter enable. 0 = Disable 1 = Enable	0x00
2	rw	URT6_RX_EN	UART receiver enable. 0 = Disable 1 = Enable	0x00
1..0	-	Reserved	Reserved	0x00

1.24.8. URT6 baud-rate clock counter reload register

URT6_RLR	URT6 baud-rate clock counter reload register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		URT6_PSR[5:0]					
7	6	5	4	3	2	1	0
URT6_RLR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..8	rw	URT6_PSR	UART baud-rate clock prescaler reload register. Actual value equals the register value plus one.	0x00
7..0	rw	URT6_RLR	UART baud-rate clock counter reload register. Actual value equals the register value plus one.	0x00

1.24.9. URT6 baud-rate clock counter register

URT6_CNT	URT6 baud-rate clock counter register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		URT6_PSC[5:0]					
7	6	5	4	3	2	1	0
URT6_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..8	r	URT6_PSC	UART baud-rate clock prescaler value register.	0x00
7..0	r	URT6_CNT	UART baud-rate clock counter value register.	0x00

1.24.10. URT6 RX data register

URT6_RDAT	URT6 RX data register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
URT6_RDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	r	URT6_RDAT	UART received data register. Read this register will clear the URTx_RXF. Hardware will force to logic 0 for non-updated byte(s) by URTx_RX_TH setting.	0x00

1.24.11. URT6 TX data register

URT6_TDAT	URT6 TX data register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
URT6_TDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	URT6_TDAT	UART transmitted data register. Write this register will clear the URTx_TXF. When write data by word, half-word or byte operation, chip will transfer 4-byte, 2-byte, or 1-byte data to	0x00

			shadow buffer. (write-only)	

1.24.12. URT6 data shift buffer register

URT6_SBUF	URT6 data shift buffer register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
URT6_TSBUF[7:0]							
7	6	5	4	3	2	1	0
URT6_RSBUF[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	r	URT6_TSBUF	UART TX data shift buffer register.	0x00
7..0	r	URT6_RSBUF	UART RX data shift buffer register.	0x00

1.24.13. URT6 Register Map

URT6 Register Map Register Number = 12

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	URT6_STA	Reserved								URT6_ROVRF	Reserved	URT6_FEF	URT6_PEF	Reserved				Reserved				URT6_BRTF	Reserved			URT6_TXF	URT6_RXF	Reserved		URT6_ERRF	URT6_TCF	URT6_UGF	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	URT6_INT	Reserved								URT6_ROVR_IE	Reserved	URT6_FE_IE	URT6_PE_IE	Reserved				Reserved				URT6_BRT_IE	Reserved			URT6_TX_IE	URT6_RX_IE	Reserved		URT6_ERR_IE	URT6_TC_IE	URT6_UG_IE	URT6_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	URT6_CLK	Reserved				Reserved	Reserved	URT6_BR_MDS	URT6_BR_EN	Reserved								Reserved								Reserved				URT6_CK_SEL [2:0]			Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	URT6_STA2	Reserved																Reserved								Reserved						URT6_PAR	URT6_BUSYF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	URT6_CR0	Reserved								URT6_LBM_EN	Reserved							Reserved				URT6_TX_INV	URT6_RX_INV	Reserved	URT6_IO_SWP	Reserved							URT6_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	URT6_CR1	Reserved			URT6_TXOS_NUM [4:0]					URT6_TXSTP_LEN [1:0]		Reserved	URT6_TXPAR_STK	URT6_TXPAR_POL	URT6_TXPAR_EN	URT6_TXDSIZE [1:0]		Reserved								Reserved			URT6_RXPAR_STK	URT6_RXPAR_POL	Reserved		
Reset	**0x0F400000**	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	URT6_CR2	Reserved																Reserved								Reserved				URT6_TX_EN	URT6_RX_EN	Reserved	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	URT6_RLR	Reserved																Reserved		URT6_PSR[5:0]						URT6_RLR[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x28	URT6_CNT	Reserved																Reserved		URT6_PSC[5:0]						URT6_CNT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	URT6_RDAT	Reserved																Reserved								URT6_RDAT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	URT6_TDAT	Reserved																Reserved								URT6_TDAT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	URT6_SBUF	Reserved																URT6_TSBUF[7:0]								URT6_RSBUF[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.25. URT7 Control Registers

URT7 Control	(URT7) UART Control Module-7
Base Address :	0x52070000

1.25.1. URT7 status register 1

URT7_STA	URT7 status register 1		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT7_ROVRF	Reserved	URT7_FEF	URT7_PEF	Reserved			
15	14	13	12	11	10	9	8
Reserved				URT7_BRTF	Reserved		
7	6	5	4	3	2	1	0
URT7_TXF	URT7_RXF	Reserved		URT7_ERRF	URT7_TCF	URT7_UGF	Reserved

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23	rw	URT7_ROVRF	UART receive overrun error flag. (set by hardware and clear by software writing 1) When receive overrun, hardware will stop to receive next data into data shadow buffer until this flag is cleared. This flag is indicated for following two conditions. (1) When RX shadow buffer is arrived over the RX threshold and the data register has not read out. If shift buffer is filled of next data, this flag is asserted. (2) When Parity error, Frame error, Break detect or Slave-Address detect, has happened and caused RX shadow buffer input holding. If shift buffer is filled of next data, this flag is asserted. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
22	-	Reserved	Reserved	0x00
21	rw	URT7_FEF	UART frame error flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
20	rw	URT7_PEF	UART parity error flag. (set by hardware and clear by software writing 1) When multi-processor mode, the parity value is including of address bit. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19..16	-	Reserved	Reserved	0x00
15..12	-	Reserved	Reserved	0x00
11	rw	URT7_BRTF	UART baud-rate generator timer timeout flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
10..8	-	Reserved	Reserved	0x00
7	rw	URT7_TXF	UART transmit data register empty. (set by hardware and clear by hardware or software writing 1) When transmitted shadow buffer is empty and the data register URTx_TDAT will copy to the shadow buffer, this flag is set. This bit is cleared when URTx_TDAT is written or this flag set to 1 by software. The flag is set after UART reset or Idle state. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	rw	URT7_RXF	UART receive data register not empty. (set by hardware and clear by hardware or software writing 1) When received shadow buffer level URTx_RX_LVL is greater than or equal to	0x00

Bit	Attr	Bit Name	Description	Reset
			the shadow buffer threshold URTx_RX_TH setting, this flag is set and the shadow buffer content copy to data register URTx_RDAT. This bit is cleared when URTx_RDAT is read or this flag set to 1 by software. But it does not be cleared when URTx_RDAT is read by SWD debugging. 0 = Normal (No event occurred) 1 = Happened (Event happened)	
5..4	-	Reserved	Reserved	0x00
3	rw	URT7_ERRF	UART error interrupt flag for parity error, frame error, overrun error, receive time out and noise error. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	URT7_TCF	UART transmission complete flag. When both shadow buffer and data register are empty and shift buffer shift out complete, then set this flag. (set by hardware and clear by hardware or software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	rw	URT7_UGF	UART general event flag. It indicates each of URTx_SADRF , URTx_BRTF , URTx_TMOF or URTx_CALCF flag is asserted when this flag is set. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	-	Reserved	Reserved	0x00

1.25.2. URT7 interrupt enable register

URT7_INT	URT7 interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
URT7_ROVR_IE	Reserved	URT7_FE_IE	URT7_PE_IE	Reserved			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved				URT7_BRT_IE	Reserved		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
URT7_TX_IE	URT7_RX_IE	Reserved		URT7_ERR_IE	URT7_TC_IE	URT7_UG_IE	URT7_IEA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23	rw	URT7_ROVR_IE	UART receive overrun error interrupt enable. Refer to the register descriptions of URTx_ROVRF for the detail. 0 = Disable 1 = Enable	0x00
22	-	Reserved	Reserved	0x00
21	rw	URT7_FE_IE	UART frame error interrupt enable. 0 = Disable 1 = Enable	0x00
20	rw	URT7_PE_IE	UART parity error interrupt enable. 0 = Disable 1 = Enable	0x00
19..16	-	Reserved	Reserved	0x00
15..12	-	Reserved	Reserved	0x00
11	rw	URT7_BRT_IE	UART baud-rate generator timer timeout interrupt enable. 0 = Disable 1 = Enable	0x00
10..8	-	Reserved	Reserved	0x00

7	rw	URT7_TX_IE	UART transmit data register empty interrupt enable. Refer to the register descriptions of URTx_TXF for the detail. 0 = Disable 1 = Enable	0x00
6	rw	URT7_RX_IE	UART receive data register not empty interrupt enable. Refer to the register descriptions of URTx_RXF for the detail. 0 = Disable 1 = Enable	0x00
5..4	-	Reserved	Reserved	0x00
3	rw	URT7_ERR_IE	UART error interrupt enable for parity error, frame error, overrun error, receive time out and noise error. 0 = Disable 1 = Enable	0x00
2	rw	URT7_TC_IE	UART transmission complete interrupt enable. (set by hardware and clear by hardware or software writing 1) 0 = Disable 1 = Enable	0x00
1	rw	URT7_UG_IE	UART general event interrupt enable for URTx_SADRF , URTx_TF , URTx_RCNTF or URTx_TCNTF events. 0 = Disable 1 = Enable	0x00
0	rw	URT7_IEA	UART interrupt all enable. When disables, the UART global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.25.3. URT7 clock source register

URT7_CLK	URT7 clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				Reserved	Reserved	URT7_BR_MDS	URT7_BR_EN
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				URT7_CK_SEL[2:0]			Reserved

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26	-	Reserved	Reserved	0x00
25	rw	URT7_BR_MDS	UART baud-rate timer mode select. Combined mode is only using for general purpose counter. When SmartCard mode, this bit need set to 'Separated' for SmartCard clock output from PSC output. 0 = Separated : Separated PSC and CNT counters for UART baud-rate generator 1 = Combined : Combine to a linear counter for general using timer	0x00
24	rw	URT7_BR_EN	UART baud-rate timer enable. When enables, the baud-rate timer 0 = Disable 1 = Enable	0x00
23..16	-	Reserved	Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00

3..1	rw	URT7_CK_SEL	UART internal clock CK_URTx source select. 0x0 = PROC : CK_URTx_PR process clock from CSC 0x1 = NCO_P0 0x2 = CK_LS 0x3 = TM00_TRGO	0x00
0	-	Reserved	Reserved	0x00

1.25.4. URT7 status register 2

URT7_STA2	URT7 status register 2		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						URT7_PAR	URT7_BUSYF

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..2	-	Reserved	Reserved	0x00
1	r	URT7_PAR	UART data receive parity bit of shift buffer. When multi-processor mode, the parity value is including of address bit.	0x00
0	r	URT7_BUSYF	UART RX busy flag. (set and clear by hardware) When detect valid start bit, this bit is set and clear after stop bit. 0 = Normal (No event occurred) 1 = Busy (Event happened)	0x00

1.25.5. URT7 control register 0

URT7_CR0	URT7 control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
URT7_LBM_EN	Reserved						
15	14	13	12	11	10	9	8
Reserved				URT7_TX_INV	URT7_RX_INV	Reserved	URT7_IO_SWP
7	6	5	4	3	2	1	0
Reserved							URT7_EN

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23	rw	URT7_LBM_EN	UART loop back mode enable bit. When enables, the received input is taken from transmitted output to replace from input pin(RX ->TX). 0 = Disable 1 = Enable	0x00
22..16	-	Reserved	Reserved	0x00
15..12	-	Reserved	Reserved	0x00
11	rw	URT7_TX_INV	URTx_TX output signal inverse enable. 0 = Disable 1 = Enable	0x00
10	rw	URT7_RX_INV	URTx_RX input signal inverse enable.	0x00

			0 = Disable 1 = Enable	
9	-	Reserved	Reserved	0x00
8	rw	URT7_IO_SWP	URTx_RX/URTx_TX swap enable bit. 0 = Disable 1 = Enable	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	URT7_EN	UART function enable bit. 0 = Disable 1 = Enable	0x00

1.25.6. URT7 control register 1

URT7_CR1	URT7 control register 1		
Offset Address :	0x14	Reset Value :	0x0F400000

31	30	29	28	27	26	25	24
Reserved			URT7_TXOS_NUM[4:0]				
23	22	21	20	19	18	17	16
URT7_TXSTP_LEN[1:0]		Reserved	URT7_TXPAR_STK	URT7_TXPAR_POL	URT7_TXPAR_EN	URT7_TXDSIZE[1:0]	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			URT7_RXPAR_STK	URT7_RXPAR_POL	Reserved		

Bit	Attr	Bit Name	Description	Reset
31..29	-	Reserved	Reserved	0x00
28..24	rw	URT7_TXOS_NUM	UART TX data oversampling samples select. The valid value is from 3 to 31 for oversampling samples from 4 to 32. (This register is written no effect if URTx_TX_EN set 1.)	0x0F
23..22	rw	URT7_TXSTP_LEN	UART TX stop bit length select. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = Reserved 0x1 = 1bit 0x2 = Reserved 0x3 = 2bit	0x01
21	-	Reserved	Reserved	0x00
20	rw	URT7_TXPAR_STK	UART stuck parity bit output enable. When enables and URTx_TXPAR_EN=1, parity bit output fixed value by URTx_TXPAR_POL value setting. 0 = Disable 1 = Enable	0x00
19	rw	URT7_TXPAR_POL	UART TX parity bit polarity. This bit is no effect for SPI and SYNC mods. 0x0 = Even 0x1 = Odd	0x00
18	rw	URT7_TXPAR_EN	UART TX parity bit enable. This bit does not be set for SYNC mods. (This register is written no effect if URTx_TX_EN set 1.) 0 = Disable 1 = Enable	0x00
17..16	rw	URT7_TXDSIZE	UART TX data bit length. It is not including START, STOP, ADR or PARITY bits. (This register is written no effect if URTx_TX_EN set 1.) 0x0 = 8bit 0x1 = 7bit 0x2 = Reserved 0x3 = Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7..5	-	Reserved	Reserved	0x00
4	rw	URT7_RXPAR_STK	UART stuck parity bit input enable. When enables and	0x00

			URTx_RXPAR_EN=1, parity bit input fixed value by URTx_RXPAR_POL value setting. 0 = Disable 1 = Enable	
3	rw	URT7_RXPAR_POL	UART RX parity bit polarity. This bit is no effect for SYNC mods. 0x0 = Even 0x1 = Odd	0x00
2..0	-	Reserved	Reserved	0x00

1.25.7. URT7 control register 2

URT7_CR2	URT7 control register 2		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				URT7_TX_EN	URT7_RX_EN	Reserved	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	URT7_TX_EN	UART transmitter enable. 0 = Disable 1 = Enable	0x00
2	rw	URT7_RX_EN	UART receiver enable. 0 = Disable 1 = Enable	0x00
1..0	-	Reserved	Reserved	0x00

1.25.8. URT7 baud-rate clock counter reload register

URT7_RLR	URT7 baud-rate clock counter reload register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		URT7_PSR[5:0]					
7	6	5	4	3	2	1	0
URT7_RLR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..8	rw	URT7_PSR	UART baud-rate clock prescaler reload register. Actual value equals the register value plus one.	0x00
7..0	rw	URT7_RLR	UART baud-rate clock counter reload register. Actual value equals the register value plus one.	0x00

1.25.9. URT7 baud-rate clock counter register

URT7_CNT	URT7 baud-rate clock counter register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		URT7_PSC[5:0]					
7	6	5	4	3	2	1	0
URT7_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..8	r	URT7_PSC	UART baud-rate clock prescaler value register.	0x00
7..0	r	URT7_CNT	UART baud-rate clock counter value register.	0x00

1.25.10. URT7 RX data register

URT7_RDAT	URT7 RX data register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
URT7_RDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	r	URT7_RDAT	UART received data register. Read this register will clear the URTx_RXF. Hardware will force to logic 0 for non-updated byte(s) by URTx_RX_TH setting.	0x00

1.25.11. URT7 TX data register

URT7_TDAT	URT7 TX data register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
URT7_TDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	URT7_TDAT	UART transmitted data register. Write this register will clear the URTx_TXF. When write data by word, half-word or byte operation, chip will transfer 4-byte, 2-byte, or 1-byte data to	0x00

			shadow buffer. (write-only)	

1.25.12. URT7 data shift buffer register

URT7_SBUF	URT7 data shift buffer register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
URT7_TSBUF[7:0]							
7	6	5	4	3	2	1	0
URT7_RSBUF[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	r	URT7_TSBUF	UART TX data shift buffer register.	0x00
7..0	r	URT7_RSBUF	UART RX data shift buffer register.	0x00

1.25.13. URT7 Register Map

URT7 Register Map **Register Number = 12**

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	URT7_STA	Reserved								URT7_ROVRF	Reserved	URT7_FEF	URT7_PEF	Reserved				Reserved				URT7_BRTF	Reserved			URT7_TXF	URT7_RXF	Reserved		URT7_ERRF	URT7_TCF	URT7_UGF	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	URT7_INT	Reserved								URT7_ROVR_IE	Reserved	URT7_FE_IE	URT7_PE_IE	Reserved				Reserved				URT7_BRT_IE	Reserved			URT7_TX_IE	URT7_RX_IE	Reserved		URT7_ERR_IE	URT7_TC_IE	URT7_UG_IE	URT7_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	URT7_CLK	Reserved				Reserved	Reserved	URT7_BR_MDS	URT7_BR_EN	Reserved								Reserved								Reserved				URT7_CK_SEL [2:0]			Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	URT7_STA2	Reserved																Reserved								Reserved						URT7_PAR	URT7_BUSYF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	URT7_CR0	Reserved								URT7_LBM_EN	Reserved							Reserved				URT7_TX_INV	URT7_RX_INV	Reserved	URT7_IO_SWP	Reserved							URT7_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	URT7_CR1	Reserved			URT7_TXOS_NUM [4:0]					URT7_TXSTP_LEN [1:0]		Reserved	URT7_TXPAR_STK	URT7_TXPAR_POL	URT7_TXPAR_EN	URT7_TXDSIZE [1:0]		Reserved								Reserved			URT7_RXPAR_STK	URT7_RXPAR_POL	Reserved		
Reset	**0x0F400000**	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	URT7_CR2	Reserved																Reserved								Reserved				URT7_TX_EN	URT7_RX_EN	Reserved	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	URT7_RLR	Reserved																Reserved		URT7_PSR[5:0]						URT7_RLR[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x28	**URT7_CNT**	Reserved																Reserved		**URT7_PSC[5:0]**						**URT7_CNT[7:0]**							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	**URT7_RDAT**	Reserved																Reserved								**URT7_RDAT[7:0]**							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	**URT7_TDAT**	Reserved																Reserved								**URT7_TDAT[7:0]**							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	**URT7_SBUF**	Reserved																**URT7_TSBUF[7:0]**								**URT7_RSBUF[7:0]**							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.26. SPI0 Control Registers

SPI0 Control	(SPI0) SPI Control Module-0
Base Address :	0x53000000

1.26.1. SPI0 status register

SPI0_STA	SPI0 status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
SPI0_IDL_STA	Reserved				SPI0_RNUM[2:0]		
23	22	21	20	19	18	17	16
Reserved	SPI0_TX_LVL[2:0]			Reserved	SPI0_RX_LVL[2:0]		
15	14	13	12	11	10	9	8
Reserved		Reserved	Reserved	SPI0_TUDRF	SPI0_ROVRF	SPI0_WEF	SPI0_MODF
7	6	5	4	3	2	1	0
SPI0_TXF	SPI0_RXF	SPI0_RXDF	SPI0_TCF	SPI0_IDLF	Reserved		SPI0_BUSYF

Bit	Attr	Bit Name	Description	Reset
31	r	SPI0_IDL_STA	SPI idle state detect status for Slave with NSS mode. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
30..27	-	Reserved	Reserved	0x00
26..24	rw	SPI0_RNUM	SPI received data byte number when data shadow buffer last transfer to SPI0_RDAT register. Firmware can write an initial value for received byte number comparison. See more information in SPI0_RXDF status bit. Value 0~4 is valid only. 0x0 = 0 (0-byte) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	0x00
23	-	Reserved	Reserved	0x00
22..20	r	SPI0_TX_LVL	SPI data buffer transmission remained level indications. 0x0 = 0 (0-byte,empty) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	0x00
19	-	Reserved	Reserved	0x00
18..16	r	SPI0_RX_LVL	SPI data buffer received level indications. 0x0 = 0 (0-byte,empty) 0x1 = 1 (1-byte) 0x2 = 2 (2-byte) 0x3 = 3 (3-byte) 0x4 = 4 (4-byte)	0x00
15..14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	-	Reserved	Reserved	0x00
11	rw	SPI0_TUDRF	SPI slave mode transmit underrun flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
10	rw	SPI0_ROVRF	SPI receive overrun flag. (set by hardware and clear by software writing 1) When receive overrun, hardware will stop to receive next data into data shadow buffer until this flag is cleared. When RX shadow buffer is arrived over the RX threshold and the data register has not read out. If shift buffer is filled of next data, this flag is asserted. 0 = Normal (No event occurred)	0x00

			1 = Happened (Event happened)	
9	rw	SPI0_WEF	SPI slave mode write error flag. It will assert an error when master stop read by setting high on NSS signal before a complete data transaction. The bit size of a data transaction is defined in SPI0_DSIZE. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
8	rw	SPI0_MODF	SPI mode detect fault flag. When master mode SPI0_NSSI_EN enables, this flag will be set if NSS input signal is active. Also it will force SPI0_BDIR_OE to set 'Disable' and SPI0_TX_DIS to set 'Enable'. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
7	rw	SPI0_TXF	SPI transmit data register empty flag (set by hardware and clear by hardware or software writing 1). When transmitted shadow buffer is empty and the data register SPI0_TDAT will copy to the shadow buffer, this flag is set. This bit is cleared when SPI0_TDAT is written or this flag set to 1 by software. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	rw	SPI0_RXF	SPI receive data register not empty. (set by hardware and clear by hardware or software writing 1). When received shadow buffer level SPI0_RX_LVL is greater than or equal to the data buffer threshold SPI0_RX_TH setting, this flag is set and the shadow buffer content copy to data register SPI0_RDAT. This bit is cleared when SPI0_RDAT is read or this flag set to 1 by software. But it does not be cleared when SPI0_RDAT is read by SWD debugging. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	r	SPI0_RXDF	SPI received data byte number is different from previous received data byte number for SPI0_RDAT register. (set and clear by hardware) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	SPI0_TCF	SPI transmission complete flag. When both shadow buffer and data register are empty and shift buffer shift out complete, then set this flag. (set by hardware and clear by hardware or software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	SPI0_IDLF	SPI slave mode NSS idle detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2..1	-	Reserved	Reserved	0x00
0	r	SPI0_BUSYF	SPI data transfer busy flag.	0x00

1.26.2. SPI0 interrupt enable register

SPI0_INT	SPI0 interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		Reserved	Reserved	SPI0_TUDR_IE	SPI0_ROVR_IE	SPI0_WE_IE	SPI0_MODF_IE

7	6	5	4	3	2	1	0
SPI0_TX_IE	SPI0_RX_IE	Reserved	SPI0_TC_IE	SPI0_IDL_IE	Reserved		SPI0_IEA

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	-	Reserved	Reserved	0x00
11	rw	SPI0_TUDR_IE	SPI TX buffer transmit underrun interrupt enable. 0 = Disable 1 = Enable	0x00
10	rw	SPI0_ROVR_IE	SPI RX buffer receive overrun interrupt enable. 0 = Disable 1 = Enable	0x00
9	rw	SPI0_WE_IE	SPI slave mode write error interrupt enable. 0 = Disable 1 = Enable	0x00
8	rw	SPI0_MODF_IE	SPI mode detect fault interrupt enable. 0 = Disable 1 = Enable	0x00
7	rw	SPI0_TX_IE	SPI TX buffer underflow the threshold SPI0_TX_TH Interrupt enable. 0 = Disable 1 = Enable	0x00
6	rw	SPI0_RX_IE	SPI Receive data register not empty interrupt enable. 0 = Disable 1 = Enable	0x00
5	-	Reserved	Reserved	0x00
4	rw	SPI0_TC_IE	SPI transmission complete interrupt enable. (set by hardware and clear by hardware or software writing 1) 0 = Disable 1 = Enable	0x00
3	rw	SPI0_IDL_IE	SPI slave mode NSS idle detect interrupt enable. (set by hardware and clear by software writing 1) 0 = Disable 1 = Enable	0x00
2..1	-	Reserved	Reserved	0x00
0	rw	SPI0_IEA	SPI interrupt all enable. When disables, the SPI0 global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.26.3. SPI0 clock source register

SPI0_CLK	SPI0 clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		SPI0_CK_PDIV[1:0]		Reserved	SPI0_CK_PSC[2:0]		
7	6	5	4	3	2	1	0
Reserved		SPI0_CK_DIV[1:0]		SPI0_CK_SEL[1:0]		Reserved	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00

13..12	rw	SPI0_CK_PDIV	SPI process clock CK_SPI0_PR input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
11	-	Reserved	Reserved	0x00
10..8	rw	SPI0_CK_PSC	SPI internal clock CK_SPI0_INT prescaler. The value range 0~7 is indicated divider 1~8.	0x00
7..6	-	Reserved	Reserved	0x00
5..4	rw	SPI0_CK_DIV	SPI internal clock CK_SPI0_INT input divider. 0x0 = DIV2 : divided by 2 0x1 = DIV4 : divided by 4 0x2 = DIV8 : divided by 8 0x3 = DIV16 : divided by 16	0x00
3..2	rw	SPI0_CK_SEL	SPI internal clock CK_SPI0 source select. 0x0 = PROC : CK_SPI0_PR process clock from CSC 0x1 = Reserved 0x2 = TM00_TRGO 0x3 = Reserved	0x00
1..0	-	Reserved	Reserved	0x00

1.26.4. SPI0 control register 0

SPI0_CR0	SPI0 control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
SPI0_DMA_TXEN	SPI0_DMA_RXEN	SPI0_DMA_MDS	Reserved	Reserved	SPI0_ASYNC_EN	SPI0_HS_EN	SPI0_ADPX_EN
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SPI0_DOUT_IDL[1:0]		SPI0_DOUT_MDS	SPI0_NSSI_SWEN	SPI0_LBM_EN	SPI0_RX_CTL	Reserved	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPI0_MODF_SEL	SPI0_NSS_PEN	SPI0_NSSI_INV	SPI0_NSSO_INV	SPI0_NSS_SWEN	SPI0_NSSI_SEL	SPI0_NSSI_EN	SPI0_NSSO_EN
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPI0_IO_SWP	SPI0_IO_SWP2	SPI0_MDS[1:0]		SPI0_LSB_EN	SPI0_CPHA	SPI0_CPOL	SPI0_EN

Bit	Attr	Bit Name	Description	Reset
31	rw	SPI0_DMA_TXEN	Direct memory access enable to transmit. When enables, hardware can receive the data from DMA and transmit to output. 0 = Disable 1 = Enable	0x00
30	rw	SPI0_DMA_RXEN	Direct memory access enable to receive. When enables, hardware can receive the data from input and send to DMA. 0 = Disable 1 = Enable	0x00
29	rw	SPI0_DMA_MDS	Direct memory access enable to do pre-catch one data for receive mode. 0 = Disable 1 = Enable	0x00
28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26	rw	SPI0_ASYNC_EN	SPI standard slave mode clock input asynchronous function enable. When enables, the SPI shift buffer clock is directly used the SPI clock (SPI0_CLK) input. When disables, the SPI clock (SPI0_CLK) input is synchronized by internal clock. 0 = Disable 1 = Enable	0x00
25	rw	SPI0_HS_EN	SPI slave mode high speed function enable. When this bit is enabled and SPI is slave synchronous mode (SPI0_ASYNC_EN=0), the SPI clock frequency can operate up	0x00

			to 1/3 APB clcok frequency. 0 = Disable 1 = Enable	
24	rw	**SPI0_ADPX_EN**	SPI slave mode auto full duplex data mode enable. This bit is no effect when SPI0_NSSI_EN is disabled. When this bit is enabled and NSS input is changed from inactive to active, the SPI0_DAT_LINE will be auto forced to 0 and change to full duplex standard SPI mode. 0 = Disable 1 = Enable	0x00
23..22	rw	**SPI0_DOUT_IDL**	SPI idle state data output value. When SPI standard master mode SPI0_DOUT_MDS is enabled, the SPI0_MOSI output is with driving during idle state and the output level is set by this bit. 0x0 = LBIT (Last data bit) 0x1 = Reserved 0x2 = 0 (Output 0) 0x3 = 1 (Output 1)	0x00
21	rw	**SPI0_DOUT_MDS**	SPI master standard mode idle state data output mode select. When disables and data transfers during idle state, the SPI0_MOSI will output with tristate for master mode. When enables and data transfers during idle state, the MOSI will output with driving for master mode. 0 = Disable : Output with tristate 1 = Enable : Output with driving	0x00
20	rw	**SPI0_NSSI_SWEN**	SPI NSS input signal use software control bit enable. When enables, the SPI NSS input is coming from the SPI0_NSS_SWI register setting. When disables, the SPI NSS input is coming from external SPI0_NSS or SPI0_NSSI pin. 0 = Disable 1 = Enable	0x00
19	rw	**SPI0_LBM_EN**	Loop back mode enable bit. When enables, the received input is taken from transmitted output to replace from input pin(SPI0_MISO or SPI0_MOSI). 0 = Disable 1 = Enable	0x00
18	rw	**SPI0_RX_CTL**	SPI master mode data receive sampling edge control bit. When selects 'Normal', the SPI data sampling on leading edge or trailing edge of SPI clock is set in SPI0_CPHA register. When selects 'Next', the SPI data sampling at the next half-clock edge of the selected clock edge which is set in SPI0_CPHA register. 0 = Normal : SPI0_CPHA selected clock edge 1 = Next : Next clock edge of SPI0_CPHA selected edge	0x00
17..16	-	**Reserved**	Reserved	0x00
15	rw	**SPI0_MODF_SEL**	SPI function select when master mode fault detect. 0 = SPI disable 1 = Switch to slave	0x00
14	rw	**SPI0_NSS_PEN**	SPI single master mode NSS pulse enable. When enables, NSS will be automatically active between two sequential frame data transferred and the pulse width is set by SPI0_NSS_IDT. 0 = Disable 1 = Enable	0x00
13	rw	**SPI0_NSSI_INV**	SPI NSS input signal inverse enable. 0 = Disable 1 = Enable	0x00
12	rw	**SPI0_NSSO_INV**	SPI NSS output signal inverse enable. The hardware NSS output default is low active level. 0 = Disable 1 = Enable	0x00

11	rw	SPI0_NSS_SWEN	SPI NSS signal output use software control bit enable. When enables, the NSS output is coming from SPI0_NSS_SWO register setting. 0 = Disable 1 = Enable	0x00
10	rw	SPI0_NSSI_SEL	SPI pin select for NSS input signal. 0 = NSS (SPI0_NSS pin) 1 = NSSI (SPI0_NSSI pin)	0x00
9	rw	SPI0_NSSI_EN	SPI_NSS signal input function enable. The input signal is also using for master mode change/fault detection. 0 = Disable 1 = Enable	0x00
8	rw	SPI0_NSSO_EN	SPI_NSS signal output function enable. 0 = Disable 1 = Enable	0x00
7	rw	SPI0_IO_SWP	SPI I/O SPI_MOSI,SPI_MISO signals swap enable. 0 = Disable 1 = Enable	0x00
6	rw	SPI0_IO_SWP2	SPI IO SPI0_D0~3 and SPI0_D4~7 signals swap enable. 0 = Disable 1 = Enable	0x00
5..4	rw	SPI0_MDS	SPI operation mode select. 0x0 = Slave 0x1 = Master 0x2 = Reserved 0x3 = Reserved	0x00
3	rw	SPI0_LSB_EN	SPI data order Lsb first enable. When disables , the Msb bit will be the first bit. 0 = Disable 1 = Enable	0x00
2	rw	SPI0_CPHA	SPI clock phase select. It is used to select the data sampling on leading edge or trailing edge of SPI clock. 0 = Leading edge 1 = Trailing edge	0x00
1	rw	SPI0_CPOL	SPI clock polarity select. It is used to select the SPI clock level in idle state. 0 = Low 1 = High	0x00
0	rw	SPI0_EN	SPI function enable bit. 0 = Disable 1 = Enable	0x00

1.26.5. SPI0 control register 1

SPI0_CR1	SPI0 control register 1		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved						Reserved	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved		Reserved		Reserved			SPI0_NSS_IDT
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved	Reserved			Reserved			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved						SPI0_TDAT_CLR	SPI0_RDAT_CLR

Bit	Attr	Bit Name	Description	Reset
31..26	-	Reserved	Reserved	0x00
25..24	-	Reserved	Reserved	0x00
23..22	-	Reserved	Reserved	0x00

21..20	-	Reserved	Reserved	0x00
19..17	-	Reserved	Reserved	0x00
16	rw	SPI0_NSS_IDT	SPI master mode idle cycle hardware NSS pulse time select. 0x0 = 1T 0x1 = 2T	0x00
15	-	Reserved	Reserved	0x00
14..12	-	Reserved	Reserved	0x00
11..8	-	Reserved	Reserved	0x00
7..2	-	Reserved	Reserved	0x00
1	w	SPI0_TDAT_CLR	SPI transmitted data clear enable. When enables, the transmitted data buffer will be flushed. Also SPI0_TX_LVL is cleared. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
0	w	SPI0_RDAT_CLR	SPI received data clear enable. When enables, the received data buffer will be flushed. Also SPI0_RXF flag and SPI0_RX_LVL is cleared. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00

1.26.6. SPI0 control register 2

SPI0_CR2	SPI0 control register 2		
Offset Address :	0x18	Reset Value :	0x03000100

31	30	29	28	27	26	25	24
Reserved	SPI0_CKO_MUX[2:0]			SPI0_CKO_TOG	SPI0_TXUPD_EN	SPI0_NSS_SWI	SPI0_NSS_SWO
23	22	21	20	19	18	17	16
Reserved			SPI0_DSIZE[4:0]				
15	14	13	12	11	10	9	8
Reserved		Reserved		Reserved		SPI0_RX_TH[1:0]	
7	6	5	4	3	2	1	0
SPI0_TX_DIS	SPI0_DAT_LINE[2:0]			SPI0_COPY_EN	SPI0_BDIR_OE	SPI0_DTR_EN	SPI0_RSB_TRG

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30..28	rw	SPI0_CKO_MUX	SPI0_CLK output signal select. 0x0 = SPI : SPI clock 0x1 = WE : EMB MWE signal 0x2 = OE : EMB MOE signal 0x3 = TM10 : TM10_CKO 0x4 = TM16 : TM16_CKO 0x5 = TM20 : TM20_CKO	0x00
27	rw	SPI0_CKO_TOG	SPI master mode clock output signal toggle enable bit. When enables, the SPI0_CLK signal will be toggled from low to high or high to low. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
26	rw	SPI0_TXUPD_EN	SPI slave mode transmitted data directly update enable. When disables, the SPI data must be updated to TX shift buffer before the previous clock edge of the first sampling clock edge of a frame data. When enables, the SPI data can be delayed updated to TX shift buffer before the first sampling clock edge of a frame data. 0 = Disable 1 = Enable	0x00
25	rw	SPI0_NSS_SWI	SPI NSS signal input control and status bit. When SPI0_NSSI_SWEN is disabled, this bit is used as NSS signal input status bit . When SPI0_NSSI_SWEN is enabled, this bit	0x01

			is used as software input control bit.	
24	rw	SPI0_NSS_SWO	SPI NSS signal software output control bit when SPI0_NSS_SWEN is enable. This bit is no effect for register read or write when SPI0_NSS_SWEN is disable.	0x01
23..21	-	Reserved	Reserved	0x00
20..16	rw	SPI0_DSIZE	SPI transfer data frame bit size from 4-bit to 32-bit. Write 0 indicate actual counter length value 32 and 4 indicate actual counter length value 4.	0x00
15..14	-	Reserved	Reserved	0x00
13..12	-	Reserved	Reserved	0x00
11..10	-	Reserved	Reserved	0x00
9..8	rw	SPI0_RX_TH	SPI received data buffer high threshold for slave mode. This register is no effect for register written if SPI0_DMA_RXEN is enabled. 0x0 = 1-byte 0x1 = 2-byte (default) 0x2 = 3-byte 0x3 = 4-byte	0x01
7	rw	SPI0_TX_DIS	SPI data line output disable. When disables, the data line(s) is/are changed to Hi-Z/GPIO data latch state. 0 = Enable 1 = Disable	0x00
6..4	rw	SPI0_DAT_LINE	SPI data line number select. 0x0 = SPI : 2-lines separated~ standard SPI mode) 0x1 = 1 : 1-line Bidirectional~ SPI0_MOSI 0x2 = 2 : 2-lines Bidirectional~ SPI0_D0(MOSI), SPI0_D1(MISO) 0x3 = 4 : 4-lines Bidirectional~ SPI0_D0 ~ SPI0_D3 0x4 = 4D : 8-lines TX~ SPI0_D0 ~ SPI0_D3 with duplicate SPI0_D4 ~ SPI0_D7 0x5 = 8 : 8-lines Bidirectional~ SPI0_D0 ~ SPI0_D7	0x00
3	rw	SPI0_COPY_EN	SPI data transfer copy mode enable. When enables, the data are the same on all data lines for 2/4 line mode. 0 = Disable 1 = Enable	0x00
2	rw	SPI0_BDIR_OE	SPI data line Bidirectional output enable. When disables, the data line(s) is/are changed to input state only. 0 = Disable 1 = Enable	0x00
1	rw	SPI0_DTR_EN	Dual transfer rate mode enable bit for SPI master mode. When enables, the SPI data will transfer at both rising edge and falling edge of SPI clock only for master clock mode 0. 0 = Disable 1 = Enable	0x00
0	rw	SPI0_RSB_TRG	SPI slave mode data read shadow buffer trigger to upload enable bit. When enables, the chip will force to copy data read shadow buffer content to read data register SPI0_RDAT. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00

1.26.7. SPI0 data receive register

SPI0_RDAT	SPI0 data receive register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
SPI0_RDAT[31:24]							
23	22	21	20	19	18	17	16
SPI0_RDAT[23:16]							

15	14	13	12	11	10	9	8
SPI0_RDAT[15:8]							
7	6	5	4	3	2	1	0
SPI0_RDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	SPI0_RDAT	SPI received data register. Read this register will clear the SPI0_RXF if the received data buffer level SPI0_RX_LVL is smaller than the data buffer threshold SPI0_RX_TH setting.	0x00000000

1.26.8. SPI0 data transmit register

SPI0_TDAT	SPI0 data transmit register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
SPI0_TDAT[31:24]							
23	22	21	20	19	18	17	16
SPI0_TDAT[23:16]							
15	14	13	12	11	10	9	8
SPI0_TDAT[15:8]							
7	6	5	4	3	2	1	0
SPI0_TDAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	SPI0_TDAT	SPI transmitted data register. Write this register will clear the SPI0_TXF if the transmitted data buffer level SPI0_TX_LVL is greater than the data buffer threshold SPI0_TX_TH setting.	0x00000000

1.26.9. SPI0 TX data 3-byte register

SPI0_TDAT3	SPI0 TX data 3-byte register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
SPI0_TDAT3[23:16]							
15	14	13	12	11	10	9	8
SPI0_TDAT3[15:8]							
7	6	5	4	3	2	1	0
SPI0_TDAT3[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..0	w	SPI0_TDAT3	SPI transmitted data register for 3-byte data write only. Write this register will clear the SPI0_TXF and force to transfer all 24-bit data to shadow buffer. This register is only allowed to access by a 32-bit word instruction.	0x000000

1.26.10. SPI0 Register Map

SPI0 Register Map Register Number = 9

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	SPI0_STA	SPI0_IDL_STA	Reserved				SPI0_RNUM[2:0]			Reserved	SPI0_TX_LVL [2:0]			Reserved	SPI0_RX_LVL [2:0]			Reserved		Reserved	Reserved	SPI0_TUDRF	SPI0_ROVRF	SPI0_WEF	SPI0_MODF	SPI0_TXF	SPI0_RXF	SPI0_RXDF	SPI0_TCF	SPI0_IDLF	Reserved		SPI0_BUSYF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	SPI0_INT	Reserved																Reserved		Reserved	Reserved	SPI0_TUDR_IE	SPI0_ROVR_IE	SPI0_WE_IE	SPI0_MODF_IE	SPI0_TX_IE	SPI0_RX_IE	Reserved	SPI0_TC_IE	SPI0_IDL_IE	Reserved		SPI0_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	SPI0_CLK	Reserved																Reserved		SPI0_CK_PDIV [1:0]		Reserved	SPI0_CK_PSC [2:0]			Reserved		SPI0_CK_DIV [1:0]		SPI0_CK_SEL [1:0]		Reserved	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	SPI0_CR0	SPI0_DMA_TXEN	SPI0_DMA_RXEN	SPI0_DMA_MDS	Reserved	Reserved	SPI0_ASYNC_EN	SPI0_HS_EN	SPI0_ADPX_EN	SPI0_DOUT_IDL [1:0]		SPI0_DOUT_MDS	SPI0_NSSI_SWEN	SPI0_LBM_EN	SPI0_RX_CTL	Reserved		SPI0_MODF_SEL	SPI0_NSS_PEN	SPI0_NSSI_INV	SPI0_NSSO_INV	SPI0_NSS_SWEN	SPI0_NSSI_SEL	SPI0_NSSI_EN	SPI0_NSSO_EN	SPI0_IO_SWP	SPI0_IO_SWP2	SPI0_MDS[1:0]		SPI0_LSB_EN	SPI0_CPHA	SPI0_CPOL	SPI0_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	SPI0_CR1	Reserved						Reserved		Reserved		Reserved		Reserved			SPI0_NSS_IDT	Reserved	Reserved			Reserved				Reserved						SPI0_TDAT_CLR	SPI0_RDAT_CLR
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	SPI0_CR2	Reserved	SPI0_CKO_MUX [2:0]			SPI0_CKO_TOG	SPI0_TXUPD_EN	SPI0_NSS_SWI	SPI0_NSS_SWO	Reserved			SPI0_DSIZE[4:0]					Reserved		Reserved		Reserved		SPI0_RX_TH[1:0]		SPI0_TX_DIS	SPI0_DAT_LINE [2:0]			SPI0_COPY_EN	SPI0_BDIR_OE	SPI0_DTR_EN	SPI0_RSB_TRG
Reset	**0x03000100**	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0x30	SPI0_RDAT	SPI0_RDAT[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	SPI0_TDAT	SPI0_TDAT[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x38	SPI0_TDAT3	Reserved								SPI0_TDAT3[23:0]																							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.27. USB Control Registers

USB Control	(USB) USB Control Module
Base Address :	0x54000000

1.27.1. USB status register

USB_STA	USB status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
USB_SE1F	USB_BSUSF[1:0]		Reserved	USB_RWKF	USB_RSTF	USB_RSMF	USB_SUSF
23	22	21	20	19	18	17	16
Reserved	USB_CRCF	USB_BSTF	USB_NORSF	USB_SETUPF	USB_OVRF	Reserved	
15	14	13	12	11	10	9	8
USB_EP7F	USB_EP6F	USB_EP5F	USB_EP4F	USB_EP3F	USB_EP2F	USB_EP1F	USB_EP0F
7	6	5	4	3	2	1	0
USB_LPMF	Reserved	USB_ESOF	USB_SOF	USB_ERRF	Reserved	USB_BUSF	USB_BUSYF

Bit	Attr	Bit Name	Description	Reset
31	rw	USB_SE1F	USB SE1 state detect interrupt flag. Set by hardware when USB bus is kept SE1 state more than 1 USB bit time. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
30..29	r	USB_BSUSF	USB current bus suspend state. 0x0 = Active : USB DPC Active (Device Power Control) 0x1 = Suspend : USB DPC Suspend 0x2 = SendResume : USB DPC Send-Resume (Remote-wakeup) 0x3 = LPMSuspend : USB LPM Suspend	0x00
28	-	Reserved	Reserved	0x00
27	rw	USB_RWKF	USB remote wakeup interrupt flag. During suspend, set by hardware when the function detects the USB bus reset. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
26	rw	USB_RSTF	USB bus reset detected interrupt flag. Set by hardware when the chip detects the reset state on USB bus. It would be cleared by firmware in the USB reset interrupt-service routine. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
25	rw	USB_RSMF	USB bus resume state detected interrupt flag. Set by hardware when the chip detects the resume state on the USB bus. It would be cleared by software in the USB resume interrupt-service routine. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
24	rw	USB_SUSF	USB bus suspend state detected interrupt flag. Set by hardware when the chip detects the suspend state on the USB bus. In the USB suspend interrupt-service routine, software should clear this bit before enter the suspend mode. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
23	-	Reserved	Reserved	0x00
22	rw	USB_CRCF	USB cyclic redundancy check error flag. One of the received CRCs, either in the token or in the data, was wrong. 0 = Normal (No event occurred)	0x00

			1 = Happened (Event happened)	
21	rw	USB_BSTF	USB Bit Stuffing error flag. A bit stuffing error was detected anywhere in the PID, data, and/or CRC. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
20	rw	USB_NORSF	USB host no response error flag. This flag will be asserted if USB host response timeout after data packet is sent. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19	rw	USB_SETUPF	USB wrong Setup data received error flag. This flag will be asserted if the Setup data is not 8-byte or is not DATA0. Normally the Setup DATA0 is received 8-byte. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
18	rw	USB_OVRF	USB packet memory overrun interrupt flag. This bit is set if the hardware has not been able to respond in time to an USB memory request. USB host will retry the transaction if the ACK handshake packet is not sent during reception or the bit-stuff error is happened during transmission. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17..16	-	Reserved	Reserved	0x00
15	r	USB_EP7F	USB endpoint-7 event global interrupt flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
14	r	USB_EP6F	USB endpoint-6 event global interrupt flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
13	r	USB_EP5F	USB endpoint-5 event global interrupt flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
12	r	USB_EP4F	USB endpoint-4 event global interrupt flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
11	r	USB_EP3F	USB endpoint-3 event global interrupt flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
10	r	USB_EP2F	USB endpoint-2 event global interrupt flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
9	r	USB_EP1F	USB endpoint-1 event global interrupt flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
8	r	USB_EP0F	USB endpoint-0 event global interrupt flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
7	rw	USB_LPMF	USB LPM L1 state request interrupt flag. This bit is set by the hardware when LPM command entering the L1 state is successfully received and acknowledged. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	-	Reserved	Reserved	0x00
5	rw	USB_ESOF	USB expected start of frame interrupt flag. This bit is set by hardware when detected an expected SOF. ESOF is a synchronous signal with host SOF that will be generated by hardware expecting to detect a host SOF, even if the real host SOF is missing or corrupted. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred)	0x00

			1 = Happened (Event happened)	
4	rw	USB_SOF	USB host SOF received interrupt flag. This bit is set by hardware when detected a host SOF. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	r	USB_ERRF	USB bus error global interrupt flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	-	Reserved	Reserved	0x00
1	r	USB_BUSF	USB bus event global interrupt flag. When one of USB bus events is happened, this bit is set by hardware. These USB bus events are including of USB bus reset, resume, suspend, SE1 state. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	r	USB_BUSYF	USB data transfer busy flag.	0x00

1.27.2. USB interrupt enable register

USB_INT	USB interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
USB_SE1_IE	Reserved			USB_RWK_IE	USB_RST_IE	USB_RSM_IE	USB_SUS_IE
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved	USB_CRC_IE	USB_BST_IE	USB_NORS_IE	USB_SETUP_IE	USB_OVR_IE	Reserved	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
USB_EP7_IE	USB_EP6_IE	USB_EP5_IE	USB_EP4_IE	USB_EP3_IE	USB_EP2_IE	USB_EP1_IE	USB_EP0_IE
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
USB_LPM_IE	Reserved	USB_ESOF_IE	USB_SOF_IE	USB_ERR_IE	Reserved	USB_BUS_IE	USB_IEA

Bit	Attr	Bit Name	Description	Reset
31	rw	USB_SE1_IE	USB SE1 state detect interrupt enable. 0 = Disable 1 = Enable	0x00
30..28	-	Reserved	Reserved	0x00
27	rw	USB_RWK_IE	USB remote wakeup interrupt enable. 0 = Disable 1 = Enable	0x00
26	rw	USB_RST_IE	USB bus reset detected interrupt enable. 0 = Disable 1 = Enable	0x00
25	rw	USB_RSM_IE	USB bus resume state detected interrupt enable. 0 = Disable 1 = Enable	0x00
24	rw	USB_SUS_IE	USB bus suspend state detected interrupt enable. 0 = Disable 1 = Enable	0x00
23	-	Reserved	Reserved	0x00
22	rw	USB_CRC_IE	USB cyclic redundancy check error interrupt enable. 0 = Disable 1 = Enable	0x00
21	rw	USB_BST_IE	USB Bit Stuffing error interrupt enable. 0 = Disable 1 = Enable	0x00
20	rw	USB_NORS_IE	USB host no ACK response error interrupt enable. 0 = Disable 1 = Enable	0x00
19	rw	USB_SETUP_IE	USB wrong Setup data received error interrupt enable.	0x00

			0 = Disable 1 = Enable	
18	rw	USB_OVR_IE	USB packet memory overrun interrupt enable. 0 = Disable 1 = Enable	0x00
17..16	-	Reserved	Reserved	0x00
15	rw	USB_EP7_IE	USB endpoint-7 event global interrupt enable. 0 = Disable 1 = Enable	0x00
14	rw	USB_EP6_IE	USB endpoint-6 event global interrupt enable. 0 = Disable 1 = Enable	0x00
13	rw	USB_EP5_IE	USB endpoint-5 event global interrupt enable. 0 = Disable 1 = Enable	0x00
12	rw	USB_EP4_IE	USB endpoint-4 event global interrupt enable. 0 = Disable 1 = Enable	0x00
11	rw	USB_EP3_IE	USB endpoint-3 event global interrupt enable. 0 = Disable 1 = Enable	0x00
10	rw	USB_EP2_IE	USB endpoint-2 event global interrupt enable. 0 = Disable 1 = Enable	0x00
9	rw	USB_EP1_IE	USB endpoint-1 event global interrupt enable. 0 = Disable 1 = Enable	0x00
8	rw	USB_EP0_IE	USB endpoint-0 event global interrupt enable. 0 = Disable 1 = Enable	0x00
7	rw	USB_LPM_IE	USB LPM L1 state request interrupt enable. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	USB_ESOF_IE	USB expected start of frame interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	USB_SOF_IE	USB host SOF received interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	USB_ERR_IE	USB bus error global interrupt enable. 0 = Disable 1 = Enable	0x00
2	-	Reserved	Reserved	0x00
1	rw	USB_BUS_IE	USB bus event global interrupt enable. This bit is the global enable bit of USB suspend, resume, reset, remote-wakeup events. 0 = Disable 1 = Enable	0x00
0	rw	USB_IEA	USB interrupt all enable. When disables, the USB global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.27.3. USB clock source register

USB_CLK	USB clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
USB_GPR[7:0]							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

Bit	Attr	Bit Name	Description	Reset
31..24	rw	USB_GPR	General purpose data register bits.	0x00
23..16	-	Reserved	Reserved	0x00
15..0	-	Reserved	Reserved	0x0000

1.27.4. USB status register 2

USB_STA2	USB status register 2		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved					USB_FNUM[10:8]		
23	22	21	20	19	18	17	16
USB_FNUM[7:0]							
15	14	13	12	11	10	9	8
Reserved				Reserved		Reserved	Reserved
7	6	5	4	3	2	1	0
USB_K_STA	USB_J_STA	USB_SE1_STA	USB_SE0_STA	USB_DMI_STA	USB_DPI_STA	Reserved	USB_DI_STA

Bit	Attr	Bit Name	Description	Reset
31..27	-	Reserved	Reserved	0x00
26..16	r	USB_FNUM	USB frame number. The register contains the 11-bits frame number contained in the last received SOF packet. The frame number is incremented for every frame sent by the host.	0x0000
15..12	-	Reserved	Reserved	0x00
11..10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	r	USB_K_STA	USB K state.	0x00
6	r	USB_J_STA	USB J state.	0x00
5	r	USB_SE1_STA	USB SE1 state.	0x00
4	r	USB_SE0_STA	USB SE0 state.	0x00
3	r	USB_DMI_STA	USB bus differential signal minus input line DM status.	0x00
2	r	USB_DPI_STA	USB bus differential signal plus input line DP status.	0x00
1	-	Reserved	Reserved	0x00
0	r	USB_DI_STA	USB differential input state.	0x00

1.27.5. USB control register 0

USB_CR0	USB control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	Reserved	Reserved					
23	22	21	20	19	18	17	16
USB_DP_ODC	USB_DM_ODC	Reserved	USB_DP_PD	USB_DM_PD	Reserved	Reserved	USB_DPU_EN
15	14	13	12	11	10	9	8
Reserved		USB_NORS_EN	Reserved	USB_STP_LVR	USB_RWK_TRG	Reserved	USB_RWK_MDS
7	6	5	4	3	2	1	0
USB_RWK_DSEL[1:0]		Reserved	USB_SUS_MDS	USB_V33_VDD	USB_V33_EN	USB_XTR_EN	USB_EN

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29..24	-	Reserved	Reserved	0x00
23	rw	USB_DP_ODC	USB DP pin output drive strength select. 0 = Level0 : Drive strength normal 1 = Level1 : Drive strength is Level0 * 1.1	0x00
22	rw	USB_DM_ODC	USB DM pin output drive strength select. 0 = Level0 : Drive strength normal 1 = Level1 : Drive strength is Level0 * 1.1	0x00
21	-	Reserved	Reserved	0x00
20	rw	USB_DP_PD	USB DP line with pull-down resistor enable. The resistance is about 750K~1M Ohm. 0 = Disable (disable the pull-down resistors on DP) 1 = Enable (enable the pull-down resistors on DP)	0x00
19	rw	USB_DM_PD	USB DM line with pull-down resistor enable. The resistance is about 750K~1M Ohm. 0 = Disable (disable the pull-down resistors on DM) 1 = Enable (enable the pull-down resistors on DM)	0x00
18	-	Reserved	Reserved	0x00
17	-	Reserved	Reserved	0x00
16	rw	USB_DPU_EN	USB DP line with pull-up resister enable. When enables, the USB DP line will be with the embedded internal pull-up 1.2K ohm resister. User should set 'Enable' to enable connection to upper host/hub. 0 = Disable 1 = Enable	0x00
15..14	-	Reserved	Reserved	0x00
13	rw	USB_NORS_EN	USB No-response enable for endpoint 0 IN/OUT transaction. When disables, the chip (USB device) will send ACK/NAK/STALL packet in IN/OUT transaction. When enables, the chip (USB device) will be just only response ACK packet with SETUP transaction but no response with EP0 IN/OUT transaction. This bit will be clear by hardware when device receive an SETUP token. 0 = Disable 1 = Enable	0x00
12	-	Reserved	Reserved	0x00
11	rw	USB_STP_LVR	LVR disable after enter STOP mode when USB is enabled. When disables and USB_EN=1, hardware will auto disable the LVR after enter STOP mode. When enables, LVR will be always enabled. 0 = Enable 1 = Disable	0x00
10	rw	USB_RWK_TRG	USB remote wakeup trigger. This bit is set by the firmware to initiate a remote wake-up on the USB bus when CPU is wake-up by external trigger. If USB_RWK_MDS=0, this bit will be cleared by hardware when remote-wakeup is completed. If USB_RWK_MDS=1, this bit will be cleared by firmware to stop device driving a remote wake-up on the USB bus. Don't set this bit unless the function is suspended. 0 = Stop (complete or stop) 1 = Start (trigger start)	0x00
9	-	Reserved	Reserved	0x00
8	rw	USB_RWK_MDS	USB remote wakeup control mode select. When selects 'Software', the remote-wakeup length will be controlled by USB_RWK_TRG setting 1 to 0 interval. When selects 'Hardware', the remote-wakeup length will be decided by hardware setting. 0 = Hardware	0x00

			1 = Software	
7..6	rw	USB_RWK_DSEL	USB remote wakeup delay time selection. 0x0 = DT0 (about 6.48ms) 0x1 = DT1 (about 3.24ms) 0x2 = DT2 (about 110us) 0x3 = DT3 (about 55us)	0x00
5	-	Reserved	Reserved	0x00
4	rw	USB_SUS_MDS	USB Suspend signal detect mode select. When selects 'Both', chip will assert USB_SUSF flag if hardware detects J state or SE1 state. When selects 'JS', chip will assert USB_SUSF flag only if hardware detects J state. 0 = JS : Only detect J state 1 = Both : detect J state or SE1 state.	0x00
3	rw	USB_V33_VDD	USB V33 LDO output short to VDD enable. This bit is no effect if USB_V33_EN=1. When enables, the V33 LDO output will be short to VDD power. When disables, the V33 LDO output will be floating. 0 = Disable 1 = Enable	0x00
2	rw	USB_V33_EN	USB V33 LDO power-on enable. When enables, the V33 LDO output is enabled and outputs VDDX voltage level. When disables, the V33 LDO output is disabled and floating. 0 = Disable 1 = Enable	0x00
1	rw	USB_XTR_EN	USB transceiver enable. When disables, it makes USB transceiver and related analog parts into power down mode. The USB peripheral is disconnected from the transceivers. 0 = Disable (Power down) 1 = Enable (Power on)	0x00
0	rw	USB_EN	USB function enable bit. When disables, the USB transceiver, VSS LDO and the pull-up 1.5K ohm resister of DP line are all disabled. 0 = Disable 1 = Enable	0x00

1.27.6. USB control register 1

USB_CR1	USB control register 1		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved		Reserved	USB_LPMNYF	Reserved		Reserved	USB_LPMNY_IE
23	22	21	20	19	18	17	16
USB_LPM_BESL[3:0]				Reserved	USB_LPM_RWK	USB_LPM_ACK	USB_LPM_EN
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	USB_ADR[6:0]						

Bit	Attr	Bit Name	Description	Reset
31..30	-	Reserved	Reserved	0x00
29	-	Reserved	Reserved	0x00
28	rw	USB_LPMNYF	USB LPM L1 state request interrupt flag. This bit is set by the hardware when LPM command entering the L1 state is receiving NYET. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
27..26	-	Reserved	Reserved	0x00
25	-	Reserved	Reserved	0x00

Bit	Attr	Bit Name	Description	Reset
24	rw	USB_LPMNY_IE	USB LPM L1 state receive NYET interrupt enable. 0 = Disable 1 = Enable	0x00
23..20	r	USB_LPM_BESL	USB LPM BESL value. These bits contain the BESL value received with last ACKed LPM Token	0x00
19	-	Reserved	Reserved	0x00
18	r	USB_LPM_RWK	USB LPM bRemoteWake value. This bit contains the bRemoteWake value received with last ACKed LPM Token.	0x00
17	rw	USB_LPM_ACK	USB LPM Token acknowledge enable. 0 = NYET : the valid LPM Token will be NYET 1 = ACK : the valid LPM Token will be ACK.	0x00
16	rw	USB_LPM_EN	USB LPM mode enable. This bit is set to enable to support the LPM transactions. 0 = Disable 1 = Enable	0x00
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6..0	rw	USB_ADR	USB device address. This register holds the address for the USB function. During bus enumeration, it is written with a unique value assigned by the host.	0x00

1.27.7. USB control register 2

USB_CR2	USB control register 2		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	USB_DMA_TXSEL0[2:0]			Reserved	USB_DMA_RXSEL0[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6..4	rw	USB_DMA_TXSEL0	Direct memory access end-point index selection for data transmission. 0x0 = Disable 0x1 = Reserved 0x2 = Reserved 0x3 = EP3 0x4 = EP4	0x00
3	-	Reserved	Reserved	0x00
2..0	rw	USB_DMA_RXSEL0	Direct memory access end-point index selection for data receiving. 0x0 = Disable 0x1 = Reserved 0x2 = Reserved 0x3 = EP3 0x4 = EP4	0x00

1.27.8. USB end-point 0 control register 0

USB_EP0CR0	USB end-point 0 control register 0		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				Reserved	USB_TXSTL0F	USB_TXNAK0F	USB_TXD0F
23	22	21	20	19	18	17	16
Reserved		Reserved		Reserved	USB_RXSTL0F	USB_RXNAK0F	USB_RXD0F
15	14	13	12	11	10	9	8
USB_TXRST0	USB_RXRST0	Reserved			USB_SETUP0F	USB_EDOVW0F	USB_STOVW0F
7	6	5	4	3	2	1	0
Reserved		USB_TXSTL0_IE	USB_TXNAK0_IE	USB_TXD0_IE	USB_RXSTL0_IE	USB_RXNAK0_IE	USB_RXD0_IE

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26	rw	USB_TXSTL0F	USB endpoint transmission STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
25	rw	USB_TXNAK0F	USB endpoint transmission NAK event flag. This bit is set by hardware when detected a transmit done on the NAK packet for IN transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
24	rw	USB_TXD0F	USB endpoint transmission done flag. This bit is set by the hardware when an IN transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
23..22	-	Reserved	Reserved	0x00
21..20	-	Reserved	Reserved	0x00
19	-	Reserved	Reserved	0x00
18	rw	USB_RXSTL0F	USB endpoint receiving STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	rw	USB_RXNAK0F	USB endpoint receiving NAK event flag. This bit is set by hardware when detected a receive done on the NAK packet for OUT transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
16	rw	USB_RXD0F	USB endpoint receiving done flag. This bit is set by the hardware when an OUT/SETUP transaction is successfully completed on this endpoint. The type of occurred transaction, OUT or SETUP, can be determined from the SETUP bit. A transaction ended with a NAK or STALL handshake does not set this bit. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	rw	USB_TXRST0	USB endpoint transmission block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
14	rw	USB_RXRST0	USB endpoint receiving block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'.	0x00

			0 = No : no effect 1 = Enable	
13..11	-	Reserved	Reserved	0x00
10	rw	USB_SETUP0F	USB received setup transaction flag. This bit is set by hardware when a valid SETUP transaction has been received. Clear this bit upon detection of a SETUP transaction or the firmware is ready to handle the data/status stage of control transfer. This bit is only used for control endpoint. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
9	rw	USB_EDOVW0F	USB SETUP end overwrite flag. This flag is set by hardware during the handshake phase of a SETUP transaction. This bit is cleared by firmware to read the FIFO data. This bit is only used for control endpoint. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
8	r	USB_STOVW0F	USB SETUP start overwrite flag. This bit is set by hardware upon receipt of a SETUP token for the control endpoint to indicate that the receive FIFO is being overwritten with new SETUP data. This bit is used only for control endpoint. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	USB_TXSTL0_IE	USB endpoint transmission STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	USB_TXNAK0_IE	USB endpoint transmission NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	USB_TXD0_IE	USB endpoint transmission done interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	USB_RXSTL0_IE	USB endpoint receiving STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
1	rw	USB_RXNAK0_IE	USB endpoint receiving NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	USB_RXD0_IE	USB endpoint receiving done interrupt enable. 0 = Disable 1 = Enable	0x00

1.27.9. USB end-point 0 control register 1

USB_EP0CR1	USB end-point 0 control register 1		
Offset Address :	0x44	Reset Value :	0x01050000

31	30	29	28	27	26	25	24
Reserved	Reserved	USB_TXS_LCK0	USB_TXSEQ0	USB_TXSA_LCK0	USB_TXMC0	USB_TXSTL0	USB_TXEN0
23	22	21	20	19	18	17	16
Reserved	Reserved	USB_RXS_LCK0	USB_RXSEQ0	USB_RXSA_LCK0	USB_RXMC0	USB_RXSTL0	USB_RXEN0
15	14	13	12	11	10	9	8
Reserved	Reserved	USB_BLSIZE0	USB_BLNUM0[4:0]				
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved			

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00

30	-	**Reserved**	Reserved	0x00
29	rw	**USB_TXS_LCK0**	USB transmit data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_TXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_TXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
28	rw	**USB_TXSEQ0**	USB transmit endpoint sequence bit (read, conditional write). The bit will be transmitted in the next PID and toggled on a valid ACK handshake of an IN transaction. This bit can be written by firmware if the USB_TXS_LCKn bit is set when written along with the new USB_TXSEQn value. (n = endpoint index)	0x00
27	rw	**USB_TXSA_LCK0**	USB transmit control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_TXENn, USB_TXSTLn, USB_TXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these transmit control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
26	rw	**USB_TXMC0**	USB transmit memory write complete. Set this bit to release the transmit memory when data write is complete. Hardware clears this bit after the memory release operation has been finished. Firmware should write this bit only after firmware finished writing USB_TXCNTn register. (n = endpoint index) 0 = No : no effect 1 = Complete : write data complete to USB memory	0x00
25	rw	**USB_TXSTL0**	USB transmit endpoint STALL enable. Set this bit to STALL the transmit endpoint. Clear this bit only when the host has intervened through commands sent down endpoint. When this bit is set and USB_SETUPnF is clear, the transmit endpoint will respond with a STALL handshake to a valid IN token. When this bit is set and USB_SETUPnF is set, the transmit endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	0x00
24	rw	**USB_TXEN0**	USB transmit endpoint enable. Set this bit to enable the transmit endpoint. When disabled, the endpoint does not respond to a valid IN token. This bit has the highest priority than USB_En_TXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x01
23	-	**Reserved**	Reserved	0x00
22	-	**Reserved**	Reserved	0x00
21	rw	**USB_RXS_LCK0**	USB receive data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_RXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_RXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
20	rw	**USB_RXSEQ0**	USB receive endpoint sequence bit (read, conditional write). The bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit can be written by firmware if the USB_RXS_LCKn bit is set when written along with the new USB_RXSEQn value. (n = endpoint index)	0x00
19	rw	**USB_RXSA_LCK0**	USB receive control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_RXENn, USB_RXSTLn, USB_RXMCn bits to be overwritten. Set	0x00

			'locked' to this bit makes no effect on these receive control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	
18	rw	USB_RXMC0	USB receive memory read complete. Set this bit to release the receive memory when data read is complete. Hardware clears this bit after the memory release operation has been finished. 0 = No : no effect 1 = Complete : read data complete from USB memory	0x01
17	rw	USB_RXSTL0	USB receive endpoint STALL enable. Set this bit to STALL the receive endpoint. Note: Clear this bit only when the host has intervened through commands sent down endpoint-n. When this bit is set and USB_SETUPnF is clear, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is set and USB_SETUPnF is set, the receive endpoint will NAK. This bit does not affect the reception of SETUP tokens by a control endpoint. (n = endpoint index) 0 = Disable 1 = Enable	0x00
16	rw	USB_RXEN0	USB receive endpoint enable. Set this bit to enable the receive endpoint. When disabled, the endpoint does not respond to a valid OUT or SETUP token. This bit has the highest priority than USB_En_RXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x01
15	-	Reserved	Reserved	0x00
14	-	Reserved	Reserved	0x00
13	rw	USB_BLSIZE0	USB endpoint memory block size select. When selects '2Byte', the memory block is 2-byte large. With this block size the allocated endpoint memory size ranges from 2 to 62 bytes. When selects '32Byte', the memory block is 32-byte. With this block size the allocated endpoint memory size ranges from 32 to 512 bytes. 0 = 2Byte 1 = 32Byte	0x00
12..8	rw	USB_BLNUM0	USB endpoint memory block number. The endpoint memory size is this value multiplied by USB_BLSIZEn for data receiving overflow detect. (n = endpoint index)	0x00
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3..0	-	Reserved	Reserved	0x00

1.27.10. USB end-point 0 receive register

USB_EP0RX	USB end-point 0 receive register		
Offset Address :	0x48	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_RXCNT0
23	22	21	20	19	18	17	16
USB_RXCNT0[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_RXADR0
7	6	5	4	3	2	1	0
USB_RXADR0[7:0]							

Bit	Attr	Bit Name	Description	Reset

31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_RXCNT0	USB endpoint receive byte count. These bits contain the number of bytes received for the endpoint-n for the last OUT/SETUP transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_RXADR0	USB endpoint receive buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for OUT/SETUP transaction. (n = endpoint index)	0x0000

1.27.11. USB end-point 0 transmit register

USB_EP0TX	USB end-point 0 transmit register		
Offset Address :	0x4C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_TXCNT0
23	22	21	20	19	18	17	16
USB_TXCNT0[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_TXADR0
7	6	5	4	3	2	1	0
USB_TXADR0[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_TXCNT0	USB endpoint transmit byte count. These bits contain the number of bytes received for the endpoint-n for the last IN transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_TXADR0	USB endpoint transmit buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for IN transaction. (n = endpoint index)	0x0000

1.27.12. USB end-point 1 control register 0

USB_EP1CR0	USB end-point 1 control register 0		
Offset Address :	0x50	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				USB_ISOTXE1F	USB_TXSTL1F	USB_TXNAK1F	USB_TXD1F
23	22	21	20	19	18	17	16
Reserved		Reserved		USB_ISOOVW1F	USB_RXSTL1F	USB_RXNAK1F	USB_RXD1F
15	14	13	12	11	10	9	8
USB_TXRST1	USB_RXRST1	Reserved			Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0
Reserved		USB_TXSTL1_IE	USB_TXNAK1_IE	USB_TXD1_IE	USB_RXSTL1_IE	USB_RXNAK1_IE	USB_RXD1_IE

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	USB_ISOTXE1F	USB isochronous transmit data empty loss error flag. This bit is set by hardware as a USB memory access empty loss happen when USB host request the next data but firmware has not yet write the data in time. Firmware can use this bit to make sure whether the data had been empty or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00

26	rw	**USB_TXSTL1F**	USB endpoint transmission STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
25	rw	**USB_TXNAK1F**	USB endpoint transmission NAK event flag. This bit is set by hardware when detected a transmit done on the NAK packet for IN transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
24	rw	**USB_TXD1F**	USB endpoint transmission done flag. For single buffer mode, this bit is set when an IN transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-1. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
23..22	-	**Reserved**	Reserved	0x00
21..20	-	**Reserved**	Reserved	0x00
19	rw	**USB_ISOOVW1F**	USB isochronous receive data overwrite error flag. This bit is set by hardware as a USB memory access conflict happen when USB host send the next data but firmware has not yet read out the last data in time. Firmware can use this bit to make sure whether the data had been overwritten or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
18	rw	**USB_RXSTL1F**	USB endpoint receiving STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	rw	**USB_RXNAK1F**	USB endpoint receiving NAK event flag. This bit is set by hardware when detected a receive done on the NAK packet for OUT transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
16	rw	**USB_RXD1F**	USB endpoint receiving done flag. For single buffer mode, this bit is set when an OUT transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-0. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	rw	**USB_TXRST1**	USB endpoint transmission block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
14	rw	**USB_RXRST1**	USB endpoint receiving block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
13..11	-	**Reserved**	Reserved	0x00

10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	USB_TXSTL1_IE	USB endpoint transmission STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	USB_TXNAK1_IE	USB endpoint transmission NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	USB_TXD1_IE	USB endpoint transmission done interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	USB_RXSTL1_IE	USB endpoint receiving STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
1	rw	USB_RXNAK1_IE	USB endpoint receiving NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	USB_RXD1_IE	USB endpoint receiving done interrupt enable. 0 = Disable 1 = Enable	0x00

1.27.13. USB end-point 1 control register 1

USB_EP1CR1	USB end-point 1 control register 1
Offset Address : 0x54	Reset Value : 0x00040000

31	30	29	28	27	26	25	24
Reserved	Reserved	USB_TXS_LCK1	USB_TXSEQ1	USB_TXSA_LCK1	USB_TXMC1	USB_TXSTL1	USB_TXEN1
23	22	21	20	19	18	17	16
Reserved	Reserved	USB_RXS_LCK1	USB_RXSEQ1	USB_RXSA_LCK1	USB_RXMC1	USB_RXSTL1	USB_RXEN1
15	14	13	12	11	10	9	8
Reserved	USB_DBM1	USB_BLSIZE1	USB_BLNUM1[4:0]				
7	6	5	4	3	2	1	0
Reserved	USB_TXTYPE1	Reserved	USB_RXTYPE1	USB_EPADR1[3:0]			

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29	rw	USB_TXS_LCK1	USB transmit data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_TXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_TXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
28	rw	USB_TXSEQ1	USB transmit endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be transmitted in the next PID and toggled on a valid ACK handshake of an IN transaction. This bit can be written by firmware if the USB_TXS_LCKn bit is set when written along with the new USB_TXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an IN transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
27	rw	USB_TXSA_LCK1	USB transmit control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_TXENn, USB_TXSTLn, USB_TXMCn bits to be overwritten. Set 'locked'	0x00

			to this bit makes no effect on these transmit control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	
26	rw	**USB_TXMC1**	USB transmit memory write complete. Set this bit to release the transmit memory when data write is complete. Hardware clears this bit after the memory release operation has been finished. Firmware should write this bit only after firmware finished writing USB_TXCNTn register. (n = endpoint index) 0 = No : no effect 1 = Complete : write data complete to USB memory	0x00
25	rw	**USB_TXSTL1**	USB transmit endpoint STALL enable. Set this bit to STALL the transmit endpoint. Clear this bit only when the host has intervened through commands sent down endpoint. When this bit is set, the transmit endpoint will respond with a STALL handshake to a valid IN token. When this bit is clear, the transmit endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	0x00
24	rw	**USB_TXEN1**	USB transmit endpoint enable. Set this bit to enable the transmit endpoint. When disabled, the endpoint does not respond to a valid IN token. This bit has the highest priority than USB_En_TXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x00
23	-	**Reserved**	Reserved	0x00
22	-	**Reserved**	Reserved	0x00
21	rw	**USB_RXS_LCK1**	USB receive data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_RXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_RXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
20	rw	**USB_RXSEQ1**	USB receive endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit can be written by firmware if the USB_RXS_LCKn bit is set when written along with the new USB_RXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an OUT transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
19	rw	**USB_RXSA_LCK1**	USB receive control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_RXENn, USB_RXSTLn, USB_RXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these receive control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
18	rw	**USB_RXMC1**	USB receive memory read complete. Set this bit to release the receive memory when data read is complete. Hardware clears this bit after the memory release operation has been finished. 0 = No : no effect 1 = Complete : read data complete from USB memory	0x01
17	rw	**USB_RXSTL1**	USB receive endpoint STALL enable. Set this bit to STALL the receive endpoint. Note: Clear this bit only when the host has intervened through commands sent down endpoint-n. When	0x00

			this bit is set, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is clear, the receive endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	
16	rw	**USB_RXEN1**	USB receive endpoint enable. Set this bit to enable the receive endpoint. When disabled, the endpoint does not respond to a valid OUT token. This bit has the highest priority than USB_En_RXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x00
15	-	**Reserved**	Reserved	0x00
14	rw	**USB_DBM1**	USB endpoint double buffer mode enable. This bit is set by the software to enable the double-buffering feature for bulk endpoint. 0 = Disable 1 = Enable	0x00
13	rw	**USB_BLSIZE1**	USB endpoint memory block size select. When selects '2Byte', the memory block is 2-byte large. With this block size the allocated endpoint memory size ranges from 2 to 62 bytes. When selects '32Byte', the memory block is 32-byte. With this block size the allocated endpoint memory size ranges from 32 to 512 bytes. 0 = 2Byte 1 = 32Byte	0x00
12..8	rw	**USB_BLNUM1**	USB endpoint memory block number. The endpoint memory size is this value multiplied by USB_BLSIZEn for data receiving overflow detect. (n = endpoint index)	0x00
7	-	**Reserved**	Reserved	0x00
6	rw	**USB_TXTYPE1**	USB transmit endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
5	-	**Reserved**	Reserved	0x00
4	rw	**USB_RXTYPE1**	USB receive endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
3..0	rw	**USB_EPADR1**	USB endpoint address. The 4-bit address is used to identify the transactions directed to this endpoint. A value must be written before enabling the corresponding endpoint.	0x00

1.27.14. USB end-point 1 receive register

USB_EP1RX	**USB end-point 1 receive register**		
Offset Address :	**0x58**	**Reset Value :**	**0x00000000**

31	30	29	28	27	26	25	24
Reserved							**USB_RXCNT1**
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
USB_RXCNT1[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							**USB_RXADR1**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
USB_RXADR1[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_RXCNT1	USB endpoint receive byte count. These bits contain the number of bytes received for the endpoint-n for the last OUT transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_RXADR1	USB endpoint receive buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for OUT transaction. (n = endpoint index)	0x0000

1.27.15. USB end-point 1 transmit register

USB_EP1TX	USB end-point 1 transmit register		
Offset Address :	0x5C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_TXCNT1
23	22	21	20	19	18	17	16
USB_TXCNT1[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_TXADR1
7	6	5	4	3	2	1	0
USB_TXADR1[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_TXCNT1	USB endpoint transmit byte count. These bits contain the number of bytes received for the endpoint-n for the last IN transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_TXADR1	USB endpoint transmit buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for IN transaction. (n = endpoint index)	0x0000

1.27.16. USB end-point 2 control register 0

USB_EP2CR0	USB end-point 2 control register 0		
Offset Address :	0x60	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				USB_ISOTXE2F	USB_TXSTL2F	USB_TXNAK2F	USB_TXD2F
23	22	21	20	19	18	17	16
Reserved				USB_ISOOVW2F	USB_RXSTL2F	USB_RXNAK2F	USB_RXD2F
15	14	13	12	11	10	9	8
USB_TXRST2	USB_RXRST2	Reserved					
7	6	5	4	3	2	1	0
Reserved		USB_TXSTL2_IE	USB_TXNAK2_IE	USB_TXD2_IE	USB_RXSTL2_IE	USB_RXNAK2_IE	USB_RXD2_IE

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	USB_ISOTXE2F	USB isochronous transmit data empty loss error flag. This bit is set by hardware as a USB memory access empty loss happen when USB host request the next data but firmware has not yet write the data in time. Firmware can use this bit to make sure whether the data had been empty or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred)	0x00

			1 = Happened (Event happened)	
26	rw	USB_TXSTL2F	USB endpoint transmission STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
25	rw	USB_TXNAK2F	USB endpoint transmission NAK event flag. This bit is set by hardware when detected a transmit done on the NAK packet for IN transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
24	rw	USB_TXD2F	USB endpoint transmission done flag. For single buffer mode, this bit is set when an IN transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-1. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
23..20	-	Reserved	Reserved	0x00
19	rw	USB_ISOOVW2F	USB isochronous receive data overwrite error flag. This bit is set by hardware as a USB memory access conflict happen when USB host send the next data but firmware has not yet read out the last data in time. Firmware can use this bit to make sure whether the data had been overwritten or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
18	rw	USB_RXSTL2F	USB endpoint receiving STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	rw	USB_RXNAK2F	USB endpoint receiving NAK event flag. This bit is set by hardware when detected a receive done on the NAK packet for OUT transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
16	rw	USB_RXD2F	USB endpoint receiving done flag. For single buffer mode, this bit is set when an OUT transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-0. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	rw	USB_TXRST2	USB endpoint transmission block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
14	rw	USB_RXRST2	USB endpoint receiving block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
13..8	-	Reserved	Reserved	0x00

7..6	-	Reserved	Reserved	0x00
5	rw	USB_TXSTL2_IE	USB endpoint transmission STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	USB_TXNAK2_IE	USB endpoint transmission NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	USB_TXD2_IE	USB endpoint transmission done interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	USB_RXSTL2_IE	USB endpoint receiving STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
1	rw	USB_RXNAK2_IE	USB endpoint receiving NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	USB_RXD2_IE	USB endpoint receiving done interrupt enable. 0 = Disable 1 = Enable	0x00

1.27.17. USB end-point 2 control register 1

USB_EP2CR1	USB end-point 2 control register 1		
Offset Address :	0x64	Reset Value :	0x00040000

31	30	29	28	27	26	25	24
Reserved	Reserved	USB_TXS_LCK2	USB_TXSEQ2	USB_TXSA_LCK2	USB_TXMC2	USB_TXSTL2	USB_TXEN2
23	22	21	20	19	18	17	16
Reserved	Reserved	USB_RXS_LCK2	USB_RXSEQ2	USB_RXSA_LCK2	USB_RXMC2	USB_RXSTL2	USB_RXEN2
15	14	13	12	11	10	9	8
Reserved	USB_DBM2	USB_BLSIZE2	USB_BLNUM2[4:0]				
7	6	5	4	3	2	1	0
Reserved	USB_TXTYPE2	Reserved	USB_RXTYPE2	USB_EPADR2[3:0]			

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29	rw	USB_TXS_LCK2	USB transmit data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_TXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_TXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
28	rw	USB_TXSEQ2	USB transmit endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be transmitted in the next PID and toggled on a valid ACK handshake of an IN transaction. This bit can be written by firmware if the USB_TXS_LCKn bit is set when written along with the new USB_TXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an IN transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
27	rw	USB_TXSA_LCK2	USB transmit control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_TXENn, USB_TXSTLn, USB_TXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these transmit control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index)	0x00

			0 = Locked 1 = un-Locked	
26	rw	**USB_TXMC2**	USB transmit memory write complete. Set this bit to release the transmit memory when data write is complete. Hardware clears this bit after the memory release operation has been finished. Firmware should write this bit only after firmware finished writing USB_TXCNTn register. (n = endpoint index) 0 = No : no effect 1 = Complete : write data complete to USB memory	0x00
25	rw	**USB_TXSTL2**	USB transmit endpoint STALL enable. Set this bit to STALL the transmit endpoint. Clear this bit only when the host has intervened through commands sent down endpoint. When this bit is set, the transmit endpoint will respond with a STALL handshake to a valid IN token. When this bit is clear, the transmit endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	0x00
24	rw	**USB_TXEN2**	USB transmit endpoint enable. Set this bit to enable the transmit endpoint. When disabled, the endpoint does not respond to a valid IN token. This bit has the highest priority than USB_En_TXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x00
23	-	**Reserved**	Reserved	0x00
22	-	**Reserved**	Reserved	0x00
21	rw	**USB_RXS_LCK2**	USB receive data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_RXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_RXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
20	rw	**USB_RXSEQ2**	USB receive endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit can be written by firmware if the USB_RXS_LCKn bit is set when written along with the new USB_RXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an OUT transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
19	rw	**USB_RXSA_LCK2**	USB receive control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_RXENn, USB_RXSTLn, USB_RXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these receive control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
18	rw	**USB_RXMC2**	USB receive memory read complete. Set this bit to release the receive memory when data read is complete. Hardware clears this bit after the memory release operation has been finished. 0 = No : no effect 1 = Complete : read data complete from USB memory	0x01
17	rw	**USB_RXSTL2**	USB receive endpoint STALL enable. Set this bit to STALL the receive endpoint. Note: Clear this bit only when the host has intervened through commands sent down endpoint-n. When this bit is set, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is clear, the receive endpoint will NAK. (n = endpoint index)	0x00

			0 = Disable 1 = Enable	
16	rw	USB_RXEN2	USB receive endpoint enable. Set this bit to enable the receive endpoint. When disabled, the endpoint does not respond to a valid OUT token. This bit has the highest priority than USB_En_RXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x00
15	-	Reserved	Reserved	0x00
14	rw	USB_DBM2	USB endpoint double buffer mode enable. This bit is set by the software to enable the double-buffering feature for bulk endpoint. 0 = Disable 1 = Enable	0x00
13	rw	USB_BLSIZE2	USB endpoint memory block size select. When selects '2Byte', the memory block is 2-byte large. With this block size the allocated endpoint memory size ranges from 2 to 62 bytes. When selects '32Byte', the memory block is 32-byte. With this block size the allocated endpoint memory size ranges from 32 to 512 bytes. 0 = 2Byte 1 = 32Byte	0x00
12..8	rw	USB_BLNUM2	USB endpoint memory block number. The endpoint memory size is this value multiplied by USB_BLSIZEn for data receiving overflow detect. (n = endpoint index)	0x00
7	-	Reserved	Reserved	0x00
6	rw	USB_TXTYPE2	USB transmit endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
5	-	Reserved	Reserved	0x00
4	rw	USB_RXTYPE2	USB receive endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
3..0	rw	USB_EPADR2	USB endpoint address. The 4-bit address is used to identify the transactions directed to this endpoint. A value must be written before enabling the corresponding endpoint.	0x00

1.27.18. USB end-point 2 receive register

USB_EP2RX	USB end-point 2 receive register		
Offset Address :	0x68	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_RXCNT2
23	22	21	20	19	18	17	16
USB_RXCNT2[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_RXADR2
7	6	5	4	3	2	1	0
USB_RXADR2[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_RXCNT2	USB endpoint receive byte count. These bits contain the	0x0000

			number of bytes received for the endpoint-n for the last OUT transaction. (n = endpoint index)	
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_RXADR2	USB endpoint receive buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for OUT transaction. (n = endpoint index)	0x0000

1.27.19. USB end-point 2 transmit register

USB_EP2TX	USB end-point 2 transmit register		
Offset Address :	0x6C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_TXCNT2
23	22	21	20	19	18	17	16
USB_TXCNT2[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_TXADR2
7	6	5	4	3	2	1	0
USB_TXADR2[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_TXCNT2	USB endpoint transmit byte count. These bits contain the number of bytes received for the endpoint-n for the last IN transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_TXADR2	USB endpoint transmit buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for IN transaction. (n = endpoint index)	0x0000

1.27.20. USB end-point 3 control register 0

USB_EP3CR0	USB end-point 3 control register 0		
Offset Address :	0x70	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				USB_ISOTXE3F	USB_TXSTL3F	USB_TXNAK3F	USB_TXD3F
23	22	21	20	19	18	17	16
Reserved				USB_ISOOVW3F	USB_RXSTL3F	USB_RXNAK3F	USB_RXD3F
15	14	13	12	11	10	9	8
USB_TXRST3	USB_RXRST3	Reserved					
7	6	5	4	3	2	1	0
Reserved		USB_TXSTL3_IE	USB_TXNAK3_IE	USB_TXD3_IE	USB_RXSTL3_IE	USB_RXNAK3_IE	USB_RXD3_IE

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	USB_ISOTXE3F	USB isochronous transmit data empty loss error flag. This bit is set by hardware as a USB memory access empty loss happen when USB host request the next data but firmware has not yet write the data in time. Firmware can use this bit to make sure whether the data had been empty or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
26	rw	USB_TXSTL3F	USB endpoint transmission STALL event flag. (set by hardware and software write 1 to clear)	0x00

			0 = Normal (No event occurred) 1 = Happened (Event happened)	
25	rw	USB_TXNAK3F	USB endpoint transmission NAK event flag. This bit is set by hardware when detected a transmit done on the NAK packet for IN transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
24	rw	USB_TXD3F	USB endpoint transmission done flag. For single buffer mode, this bit is set when an IN transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-1. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
23..20	-	Reserved	Reserved	0x00
19	rw	USB_ISOOVW3F	USB isochronous receive data overwrite error flag. This bit is set by hardware as a USB memory access conflict happen when USB host send the next data but firmware has not yet read out the last data in time. Firmware can use this bit to make sure whether the data had been overwritten or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
18	rw	USB_RXSTL3F	USB endpoint receiving STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	rw	USB_RXNAK3F	USB endpoint receiving NAK event flag. This bit is set by hardware when detected a receive done on the NAK packet for OUT transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
16	rw	USB_RXD3F	USB endpoint receiving done flag. For single buffer mode, this bit is set when an OUT transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-0. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	rw	USB_TXRST3	USB endpoint transmission block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
14	rw	USB_RXRST3	USB endpoint receiving block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
13..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	USB_TXSTL3_IE	USB endpoint transmission STALL event interrupt enable. 0 = Disable	0x00

			1 = Enable	
4	rw	USB_TXNAK3_IE	USB endpoint transmission NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	USB_TXD3_IE	USB endpoint transmission done interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	USB_RXSTL3_IE	USB endpoint receiving STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
1	rw	USB_RXNAK3_IE	USB endpoint receiving NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	USB_RXD3_IE	USB endpoint receiving done interrupt enable. 0 = Disable 1 = Enable	0x00

1.27.21. USB end-point 3 control register 1

USB_EP3CR1	USB end-point 3 control register 1		
Offset Address :	0x74	Reset Value :	0x00040000

31	30	29	28	27	26	25	24
Reserved	Reserved	USB_TXS_LCK3	USB_TXSEQ3	USB_TXSA_LCK3	USB_TXMC3	USB_TXSTL3	USB_TXEN3
23	22	21	20	19	18	17	16
Reserved	Reserved	USB_RXS_LCK3	USB_RXSEQ3	USB_RXSA_LCK3	USB_RXMC3	USB_RXSTL3	USB_RXEN3
15	14	13	12	11	10	9	8
Reserved	USB_DBM3	USB_BLSIZE3	USB_BLNUM3[4:0]				
7	6	5	4	3	2	1	0
Reserved	USB_TXTYPE3	Reserved	USB_RXTYPE3	USB_EPADR3[3:0]			

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29	rw	USB_TXS_LCK3	USB transmit data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_TXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_TXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
28	rw	USB_TXSEQ3	USB transmit endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be transmitted in the next PID and toggled on a valid ACK handshake of an IN transaction. This bit can be written by firmware if the USB_TXS_LCKn bit is set when written along with the new USB_TXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an IN transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
27	rw	USB_TXSA_LCK3	USB transmit control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_TXENn, USB_TXSTLn, USB_TXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these transmit control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
26	rw	USB_TXMC3	USB transmit memory write complete. Set this bit to release	0x00

			the transmit memory when data write is complete. Hardware clears this bit after the memory release operation has been finished. Firmware should write this bit only after firmware finished writing USB_TXCNTn register. (n = endpoint index) 0 = No : no effect 1 = Complete : write data complete to USB memory	
25	rw	**USB_TXSTL3**	USB transmit endpoint STALL enable. Set this bit to STALL the transmit endpoint. Clear this bit only when the host has intervened through commands sent down endpoint. When this bit is set, the transmit endpoint will respond with a STALL handshake to a valid IN token. When this bit is clear, the transmit endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	0x00
24	rw	**USB_TXEN3**	USB transmit endpoint enable. Set this bit to enable the transmit endpoint. When disabled, the endpoint does not respond to a valid IN token. This bit has the highest priority than USB_En_TXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x00
23	-	**Reserved**	Reserved	0x00
22	-	**Reserved**	Reserved	0x00
21	rw	**USB_RXS_LCK3**	USB receive data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_RXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_RXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
20	rw	**USB_RXSEQ3**	USB receive endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit can be written by firmware if the USB_RXS_LCKn bit is set when written along with the new USB_RXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an OUT transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
19	rw	**USB_RXSA_LCK3**	USB receive control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_RXENn, USB_RXSTLn, USB_RXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these receive control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
18	rw	**USB_RXMC3**	USB receive memory read complete. Set this bit to release the receive memory when data read is complete. Hardware clears this bit after the memory release operation has been finished. 0 = No : no effect 1 = Complete : read data complete from USB memory	0x01
17	rw	**USB_RXSTL3**	USB receive endpoint STALL enable. Set this bit to STALL the receive endpoint. Note: Clear this bit only when the host has intervened through commands sent down endpoint-n. When this bit is set, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is clear, the receive endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	0x00
16	rw	**USB_RXEN3**	USB receive endpoint enable. Set this bit to enable the receive	0x00

			endpoint. When disabled, the endpoint does not respond to a valid OUT token. This bit has the highest priority than USB_En_RXSTL. (n = endpoint index) 0 = Disable 1 = Enable	
15	-	**Reserved**	Reserved	0x00
14	rw	**USB_DBM3**	USB endpoint double buffer mode enable. This bit is set by the software to enable the double-buffering feature for bulk endpoint. 0 = Disable 1 = Enable	0x00
13	rw	**USB_BLSIZE3**	USB endpoint memory block size select. When selects '2Byte', the memory block is 2-byte large. With this block size the allocated endpoint memory size ranges from 2 to 62 bytes. When selects '32Byte', the memory block is 32-byte. With this block size the allocated endpoint memory size ranges from 32 to 512 bytes. 0 = 2Byte 1 = 32Byte	0x00
12..8	rw	**USB_BLNUM3**	USB endpoint memory block number. The endpoint memory size is this value multiplied by USB_BLSIZEn for data receiving overflow detect. (n = endpoint index)	0x00
7	-	**Reserved**	Reserved	0x00
6	rw	**USB_TXTYPE3**	USB transmit endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
5	-	**Reserved**	Reserved	0x00
4	rw	**USB_RXTYPE3**	USB receive endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
3..0	rw	**USB_EPADR3**	USB endpoint address. The 4-bit address is used to identify the transactions directed to this endpoint. A value must be written before enabling the corresponding endpoint.	0x00

1.27.22. USB end-point 3 receive register

USB_EP3RX	USB end-point 3 receive register		
Offset Address :	0x78	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_RXCNT3
23	22	21	20	19	18	17	16
USB_RXCNT3[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_RXADR3
7	6	5	4	3	2	1	0
USB_RXADR3[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	**Reserved**	Reserved	0x00
24..16	rw	**USB_RXCNT3**	USB endpoint receive byte count. These bits contain the number of bytes received for the endpoint-n for the last OUT transaction. (n = endpoint index)	0x0000
15..9	-	**Reserved**	Reserved	0x00

8..0	rw	USB_RXADR3	USB endpoint receive buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for OUT transaction. (n = endpoint index)	0x0000

1.27.23. USB end-point 3 transmit register

USB_EP3TX	USB end-point 3 transmit register		
Offset Address :	0x7C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_TXCNT3
23	22	21	20	19	18	17	16
USB_TXCNT3[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_TXADR3
7	6	5	4	3	2	1	0
USB_TXADR3[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_TXCNT3	USB endpoint transmit byte count. These bits contain the number of bytes received for the endpoint-n for the last IN transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_TXADR3	USB endpoint transmit buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for IN transaction. (n = endpoint index)	0x0000

1.27.24. USB end-point 4 control register 0

USB_EP4CR0	USB end-point 4 control register 0		
Offset Address :	0x80	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				USB_ISOTXE4F	USB_TXSTL4F	USB_TXNAK4F	USB_TXD4F
23	22	21	20	19	18	17	16
Reserved				USB_ISOOVW4F	USB_RXSTL4F	USB_RXNAK4F	USB_RXD4F
15	14	13	12	11	10	9	8
USB_TXRST4	USB_RXRST4	Reserved					
7	6	5	4	3	2	1	0
Reserved		USB_TXSTL4_IE	USB_TXNAK4_IE	USB_TXD4_IE	USB_RXSTL4_IE	USB_RXNAK4_IE	USB_RXD4_IE

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	USB_ISOTXE4F	USB isochronous transmit data empty loss error flag. This bit is set by hardware as a USB memory access empty loss happen when USB host request the next data but firmware has not yet write the data in time. Firmware can use this bit to make sure whether the data had been empty or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
26	rw	USB_TXSTL4F	USB endpoint transmission STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
25	rw	USB_TXNAK4F	USB endpoint transmission NAK event flag. This bit is set by hardware when detected a transmit done on the NAK packet	0x00

			for IN transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	
24	rw	**USB_TXD4F**	USB endpoint transmission done flag. For single buffer mode, this bit is set when an IN transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-1. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
23..20	-	**Reserved**	Reserved	0x00
19	rw	**USB_ISOOVW4F**	USB isochronous receive data overwrite error flag. This bit is set by hardware as a USB memory access conflict happen when USB host send the next data but firmware has not yet read out the last data in time. Firmware can use this bit to make sure whether the data had been overwritten or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
18	rw	**USB_RXSTL4F**	USB endpoint receiving STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	rw	**USB_RXNAK4F**	USB endpoint receiving NAK event flag. This bit is set by hardware when detected a receive done on the NAK packet for OUT transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
16	rw	**USB_RXD4F**	USB endpoint receiving done flag. For single buffer mode, this bit is set when an OUT transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-0. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	rw	**USB_TXRST4**	USB endpoint transmission block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
14	rw	**USB_RXRST4**	USB endpoint receiving block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
13..8	-	**Reserved**	Reserved	0x00
7..6	-	**Reserved**	Reserved	0x00
5	rw	**USB_TXSTL4_IE**	USB endpoint transmission STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	**USB_TXNAK4_IE**	USB endpoint transmission NAK event interrupt enable. 0 = Disable 1 = Enable	0x00

3	rw	USB_TXD4_IE	USB endpoint transmission done interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	USB_RXSTL4_IE	USB endpoint receiving STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
1	rw	USB_RXNAK4_IE	USB endpoint receiving NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	USB_RXD4_IE	USB endpoint receiving done interrupt enable. 0 = Disable 1 = Enable	0x00

1.27.25. USB end-point 4 control register 1

USB_EP4CR1	USB end-point 4 control register 1		
Offset Address :	0x84	Reset Value :	0x00040000

31	30	29	28	27	26	25	24
Reserved	Reserved	USB_TXS_LCK4	USB_TXSEQ4	USB_TXSA_LCK4	USB_TXMC4	USB_TXSTL4	USB_TXEN4
23	22	21	20	19	18	17	16
Reserved	Reserved	USB_RXS_LCK4	USB_RXSEQ4	USB_RXSA_LCK4	USB_RXMC4	USB_RXSTL4	USB_RXEN4
15	14	13	12	11	10	9	8
Reserved	USB_DBM4	USB_BLSIZE4	USB_BLNUM4[4:0]				
7	6	5	4	3	2	1	0
Reserved	USB_TXTYPE4	Reserved	USB_RXTYPE4	USB_EPADR4[3:0]			

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29	rw	USB_TXS_LCK4	USB transmit data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_TXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_TXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
28	rw	USB_TXSEQ4	USB transmit endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be transmitted in the next PID and toggled on a valid ACK handshake of an IN transaction. This bit can be written by firmware if the USB_TXS_LCKn bit is set when written along with the new USB_TXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an IN transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
27	rw	USB_TXSA_LCK4	USB transmit control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_TXENn, USB_TXSTLn, USB_TXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these transmit control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
26	rw	USB_TXMC4	USB transmit memory write complete. Set this bit to release the transmit memory when data write is complete. Hardware clears this bit after the memory release operation has been finished. Firmware should write this bit only after firmware finished writing USB_TXCNTn register. (n = endpoint index)	0x00

			0 = No : no effect 1 = Complete : write data complete to USB memory	
25	rw	USB_TXSTL4	USB transmit endpoint STALL enable. Set this bit to STALL the transmit endpoint. Clear this bit only when the host has intervened through commands sent down endpoint. When this bit is set, the transmit endpoint will respond with a STALL handshake to a valid IN token. When this bit is clear, the transmit endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	0x00
24	rw	USB_TXEN4	USB transmit endpoint enable. Set this bit to enable the transmit endpoint. When disabled, the endpoint does not respond to a valid IN token. This bit has the highest priority than USB_En_TXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x00
23	-	Reserved	Reserved	0x00
22	-	Reserved	Reserved	0x00
21	rw	USB_RXS_LCK4	USB receive data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_RXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_RXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
20	rw	USB_RXSEQ4	USB receive endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit can be written by firmware if the USB_RXS_LCKn bit is set when written along with the new USB_RXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an OUT transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
19	rw	USB_RXSA_LCK4	USB receive control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_RXENn, USB_RXSTLn, USB_RXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these receive control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
18	rw	USB_RXMC4	USB receive memory read complete. Set this bit to release the receive memory when data read is complete. Hardware clears this bit after the memory release operation has been finished. 0 = No : no effect 1 = Complete : read data complete from USB memory	0x01
17	rw	USB_RXSTL4	USB receive endpoint STALL enable. Set this bit to STALL the receive endpoint. Note: Clear this bit only when the host has intervened through commands sent down endpoint-n. When this bit is set, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is clear, the receive endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	0x00
16	rw	USB_RXEN4	USB receive endpoint enable. Set this bit to enable the receive endpoint. When disabled, the endpoint does not respond to a valid OUT token. This bit has the highest priority than USB_En_RXSTL. (n = endpoint index) 0 = Disable	0x00

			1 = Enable	
15	-	Reserved	Reserved	0x00
14	rw	USB_DBM4	USB endpoint double buffer mode enable. This bit is set by the software to enable the double-buffering feature for bulk endpoint. 0 = Disable 1 = Enable	0x00
13	rw	USB_BLSIZE4	USB endpoint memory block size select. When selects '2Byte', the memory block is 2-byte large. With this block size the allocated endpoint memory size ranges from 2 to 62 bytes. When selects '32Byte', the memory block is 32-byte. With this block size the allocated endpoint memory size ranges from 32 to 512 bytes. 0 = 2Byte 1 = 32Byte	0x00
12..8	rw	USB_BLNUM4	USB endpoint memory block number. The endpoint memory size is this value multiplied by USB_BLSIZEn for data receiving overflow detect. (n = endpoint index)	0x00
7	-	Reserved	Reserved	0x00
6	rw	USB_TXTYPE4	USB transmit endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
5	-	Reserved	Reserved	0x00
4	rw	USB_RXTYPE4	USB receive endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
3..0	rw	USB_EPADR4	USB endpoint address. The 4-bit address is used to identify the transactions directed to this endpoint. A value must be written before enabling the corresponding endpoint.	0x00

1.27.26. USB end-point 4 receive register

USB_EP4RX	USB end-point 4 receive register		
Offset Address :	0x88	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_RXCNT4
23	22	21	20	19	18	17	16
USB_RXCNT4[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_RXADR4
7	6	5	4	3	2	1	0
USB_RXADR4[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_RXCNT4	USB endpoint receive byte count. These bits contain the number of bytes received for the endpoint-n for the last OUT transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_RXADR4	USB endpoint receive buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for OUT transaction. (n = endpoint index)	0x0000

1.27.27. USB end-point 4 transmit register

USB_EP4TX	USB end-point 4 transmit register		
Offset Address :	0x8C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_TXCNT4
23	22	21	20	19	18	17	16
USB_TXCNT4[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_TXADR4
7	6	5	4	3	2	1	0
USB_TXADR4[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_TXCNT4	USB endpoint transmit byte count. These bits contain the number of bytes received for the endpoint-n for the last IN transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_TXADR4	USB endpoint transmit buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for IN transaction. (n = endpoint index)	0x0000

1.27.28. USB end-point 5 control register 0

USB_EP5CR0	USB end-point 5 control register 0		
Offset Address :	0x90	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				USB_ISOTXE5F	USB_TXSTL5F	USB_TXNAK5F	USB_TXD5F
23	22	21	20	19	18	17	16
Reserved				USB_ISOOVW5F	USB_RXSTL5F	USB_RXNAK5F	USB_RXD5F
15	14	13	12	11	10	9	8
USB_TXRST5	USB_RXRST5	Reserved					
7	6	5	4	3	2	1	0
Reserved		USB_TXSTL5_IE	USB_TXNAK5_IE	USB_TXD5_IE	USB_RXSTL5_IE	USB_RXNAK5_IE	USB_RXD5_IE

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	USB_ISOTXE5F	USB isochronous transmit data empty loss error flag. This bit is set by hardware as a USB memory access empty loss happen when USB host request the next data but firmware has not yet write the data in time. Firmware can use this bit to make sure whether the data had been empty or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
26	rw	USB_TXSTL5F	USB endpoint transmission STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
25	rw	USB_TXNAK5F	USB endpoint transmission NAK event flag. This bit is set by hardware when detected a transmit done on the NAK packet for IN transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred)	0x00

			1 = Happened (Event happened)	
24	rw	USB_TXD5F	USB endpoint transmission done flag. For single buffer mode, this bit is set when an IN transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-1. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
23..20	-	Reserved	Reserved	0x00
19	rw	USB_ISOOVW5F	USB isochronous receive data overwrite error flag. This bit is set by hardware as a USB memory access conflict happen when USB host send the next data but firmware has not yet read out the last data in time. Firmware can use this bit to make sure whether the data had been overwritten or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
18	rw	USB_RXSTL5F	USB endpoint receiving STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	rw	USB_RXNAK5F	USB endpoint receiving NAK event flag. This bit is set by hardware when detected a receive done on the NAK packet for OUT transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
16	rw	USB_RXD5F	USB endpoint receiving done flag. This bit is set by the hardware when an OUT/SETUP transaction is successfully completed on this endpoint. The type of occurred transaction, OUT or SETUP, can be determined from the SETUP bit. A transaction ended with a NAK or STALL handshake does not set this bit. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	rw	USB_TXRST5	USB endpoint transmission block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
14	rw	USB_RXRST5	USB endpoint receiving block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
13..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	USB_TXSTL5_IE	USB endpoint transmission STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	USB_TXNAK5_IE	USB endpoint transmission NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	USB_TXD5_IE	USB endpoint transmission done interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	USB_RXSTL5_IE	USB endpoint receiving STALL event interrupt enable. 0 = Disable	0x00

			1 = Enable	
1	rw	USB_RXNAK5_IE	USB endpoint receiving NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	USB_RXD5_IE	USB endpoint receiving done interrupt enable. 0 = Disable 1 = Enable	0x00

1.27.29. USB end-point 5 control register 1

USB_EP5CR1	USB end-point 5 control register 1		
Offset Address :	0x94	Reset Value :	0x00040000

31	30	29	28	27	26	25	24
Reserved	Reserved	USB_TXS_LCK5	USB_TXSEQ5	USB_TXSA_LCK5	USB_TXMC5	USB_TXSTL5	USB_TXEN5
23	22	21	20	19	18	17	16
Reserved	Reserved	USB_RXS_LCK5	USB_RXSEQ5	USB_RXSA_LCK5	USB_RXMC5	USB_RXSTL5	USB_RXEN5
15	14	13	12	11	10	9	8
Reserved	USB_DBM5	USB_BLSIZE5	USB_BLNUM5[4:0]				
7	6	5	4	3	2	1	0
Reserved	USB_TXTYPE5	Reserved	USB_RXTYPE5	USB_EPADR5[3:0]			

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29	rw	USB_TXS_LCK5	USB transmit data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_TXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_TXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
28	rw	USB_TXSEQ5	USB transmit endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be transmitted in the next PID and toggled on a valid ACK handshake of an IN transaction. This bit can be written by firmware if the USB_TXS_LCKn bit is set when written along with the new USB_TXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an IN transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
27	rw	USB_TXSA_LCK5	USB transmit control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_TXENn, USB_TXSTLn, USB_TXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these transmit control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
26	rw	USB_TXMC5	USB transmit memory write complete. Set this bit to release the transmit memory when data write is complete. Hardware clears this bit after the memory release operation has been finished. Firmware should write this bit only after firmware finished writing USB_TXCNTn register. (n = endpoint index) 0 = No : no effect 1 = Complete : write data complete to USB memory	0x00
25	rw	USB_TXSTL5	USB transmit endpoint STALL enable. Set this bit to STALL the transmit endpoint. Clear this bit only when the host has intervened through commands sent down endpoint. When this	0x00

			bit is set, the transmit endpoint will respond with a STALL handshake to a valid IN token. When this bit is clear, the transmit endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	
24	rw	**USB_TXEN5**	USB transmit endpoint enable. Set this bit to enable the transmit endpoint. When disabled, the endpoint does not respond to a valid IN token. This bit has the highest priority than USB_En_TXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x00
23	-	**Reserved**	Reserved	0x00
22	-	**Reserved**	Reserved	0x00
21	rw	**USB_RXS_LCK5**	USB receive data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_RXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_RXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
20	rw	**USB_RXSEQ5**	USB receive endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit can be written by firmware if the USB_RXS_LCKn bit is set when written along with the new USB_RXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an OUT transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
19	rw	**USB_RXSA_LCK5**	USB receive control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_RXENn, USB_RXSTLn, USB_RXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these receive control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
18	rw	**USB_RXMC5**	USB receive memory read complete. Set this bit to release the receive memory when data read is complete. Hardware clears this bit after the memory release operation has been finished. 0 = No : no effect 1 = Complete : read data complete from USB memory	0x01
17	rw	**USB_RXSTL5**	USB receive endpoint STALL enable. Set this bit to STALL the receive endpoint. Note: Clear this bit only when the host has intervened through commands sent down endpoint-n. When this bit is set, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is clear, the receive endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	0x00
16	rw	**USB_RXEN5**	USB receive endpoint enable. Set this bit to enable the receive endpoint. When disabled, the endpoint does not respond to a valid OUT token. This bit has the highest priority than USB_En_RXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x00
15	-	**Reserved**	Reserved	0x00
14	rw	**USB_DBM5**	USB endpoint double buffer mode enable. This bit is set by the software to enable the double-buffering feature for bulk endpoint.	0x00

			0 = Disable 1 = Enable	
13	rw	USB_BLSIZE5	USB endpoint memory block size select. When selects '2Byte', the memory block is 2-byte large. With this block size the allocated endpoint memory size ranges from 2 to 62 bytes. When selects '32Byte', the memory block is 32-byte. With this block size the allocated endpoint memory size ranges from 32 to 512 bytes. 0 = 2Byte 1 = 32Byte	0x00
12..8	rw	USB_BLNUM5	USB endpoint memory block number. The endpoint memory size is this value multiplied by USB_BLSIZEn for data receiving overflow detect. (n = endpoint index)	0x00
7	-	Reserved	Reserved	0x00
6	rw	USB_TXTYPE5	USB transmit endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
5	-	Reserved	Reserved	0x00
4	rw	USB_RXTYPE5	USB receive endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
3..0	rw	USB_EPADR5	USB endpoint address. The 4-bit address is used to identify the transactions directed to this endpoint. A value must be written before enabling the corresponding endpoint.	0x00

1.27.30. USB end-point 5 receive register

USB_EP5RX	USB end-point 5 receive register		
Offset Address :	0x98	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_RXCNT5
23	22	21	20	19	18	17	16
USB_RXCNT5[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_RXADR5
7	6	5	4	3	2	1	0
USB_RXADR5[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_RXCNT5	USB endpoint receive byte count. These bits contain the number of bytes received for the endpoint-n for the last OUT transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_RXADR5	USB endpoint receive buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for OUT transaction. (n = endpoint index)	0x0000

1.27.31. USB end-point 5 transmit register

USB_EP5TX	USB end-point 5 transmit register		
Offset Address :	0x9C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_TXCNT5
23	22	21	20	19	18	17	16
USB_TXCNT5[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_TXADR5
7	6	5	4	3	2	1	0
USB_TXADR5[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_TXCNT5	USB endpoint transmit byte count. These bits contain the number of bytes received for the endpoint-n for the last IN transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_TXADR5	USB endpoint transmit buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for IN transaction. (n = endpoint index)	0x0000

1.27.32. USB end-point 6 control register 0

USB_EP6CR0	USB end-point 6 control register 0		
Offset Address :	0xA0	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				USB_ISOTXE6F	USB_TXSTL6F	USB_TXNAK6F	USB_TXD6F
23	22	21	20	19	18	17	16
Reserved				USB_ISOOVW6F	USB_RXSTL6F	USB_RXNAK6F	USB_RXD6F
15	14	13	12	11	10	9	8
USB_TXRST6	USB_RXRST6	Reserved					
7	6	5	4	3	2	1	0
Reserved		USB_TXSTL6_IE	USB_TXNAK6_IE	USB_TXD6_IE	USB_RXSTL6_IE	USB_RXNAK6_IE	USB_RXD6_IE

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	USB_ISOTXE6F	USB isochronous transmit data empty loss error flag. This bit is set by hardware as a USB memory access empty loss happen when USB host request the next data but firmware has not yet write the data in time. Firmware can use this bit to make sure whether the data had been empty or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
26	rw	USB_TXSTL6F	USB endpoint transmission STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
25	rw	USB_TXNAK6F	USB endpoint transmission NAK event flag. This bit is set by hardware when detected a transmit done on the NAK packet for IN transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
24	rw	USB_TXD6F	USB endpoint transmission done flag. For single buffer mode, this bit is set when an IN transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this	0x00

			bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-1. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	
23..20	-	**Reserved**	Reserved	0x00
19	rw	**USB_ISOOVW6F**	USB isochronous receive data overwrite error flag. This bit is set by hardware as a USB memory access conflict happen when USB host send the next data but firmware has not yet read out the last data in time. Firmware can use this bit to make sure whether the data had been overwritten or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
18	rw	**USB_RXSTL6F**	USB endpoint receiving STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	rw	**USB_RXNAK6F**	USB endpoint receiving NAK event flag. This bit is set by hardware when detected a receive done on the NAK packet for OUT transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
16	rw	**USB_RXD6F**	USB endpoint receiving done flag. For single buffer mode, this bit is set when an OUT transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-0. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	rw	**USB_TXRST6**	USB endpoint transmission block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
14	rw	**USB_RXRST6**	USB endpoint receiving block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
13..8	-	**Reserved**	Reserved	0x00
7..6	-	**Reserved**	Reserved	0x00
5	rw	**USB_TXSTL6_IE**	USB endpoint transmission STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	**USB_TXNAK6_IE**	USB endpoint transmission NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	**USB_TXD6_IE**	USB endpoint transmission done interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	**USB_RXSTL6_IE**	USB endpoint receiving STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
1	rw	**USB_RXNAK6_IE**	USB endpoint receiving NAK event interrupt enable. 0 = Disable 1 = Enable	0x00

0	rw	USB_RXD6_IE	USB endpoint receiving done interrupt enable. 0 = Disable 1 = Enable	0x00

1.27.33. USB end-point 6 control register 1

USB_EP6CR1	USB end-point 6 control register 1		
Offset Address :	0xA4	Reset Value :	0x00040000

31	30	29	28	27	26	25	24
Reserved	Reserved	USB_TXS_LCK6	USB_TXSEQ6	USB_TXSA_LCK6	USB_TXMC6	USB_TXSTL6	USB_TXEN6
23	22	21	20	19	18	17	16
Reserved	Reserved	USB_RXS_LCK6	USB_RXSEQ6	USB_RXSA_LCK6	USB_RXMC6	USB_RXSTL6	USB_RXEN6
15	14	13	12	11	10	9	8
Reserved	USB_DBM6	USB_BLSIZE6	USB_BLNUM6[4:0]				
7	6	5	4	3	2	1	0
Reserved	USB_TXTYPE6	Reserved	USB_RXTYPE6	USB_EPADR6[3:0]			

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29	rw	USB_TXS_LCK6	USB transmit data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_TXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_TXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
28	rw	USB_TXSEQ6	USB transmit endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be transmitted in the next PID and toggled on a valid ACK handshake of an IN transaction. This bit can be written by firmware if the USB_TXS_LCKn bit is set when written along with the new USB_TXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an IN transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
27	rw	USB_TXSA_LCK6	USB transmit control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_TXENn, USB_TXSTLn, USB_TXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these transmit control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
26	rw	USB_TXMC6	USB transmit memory write complete. Set this bit to release the transmit memory when data write is complete. Hardware clears this bit after the memory release operation has been finished. Firmware should write this bit only after firmware finished writing USB_TXCNTn register. (n = endpoint index) 0 = No : no effect 1 = Complete : write data complete to USB memory	0x00
25	rw	USB_TXSTL6	USB transmit endpoint STALL enable. Set this bit to STALL the transmit endpoint. Clear this bit only when the host has intervened through commands sent down endpoint. When this bit is set, the transmit endpoint will respond with a STALL handshake to a valid IN token. When this bit is clear, the transmit endpoint will NAK. (n = endpoint index) 0 = Disable	0x00

			1 = Enable	
24	rw	USB_TXEN6	USB transmit endpoint enable. Set this bit to enable the transmit endpoint. When disabled, the endpoint does not respond to a valid IN token. This bit has the highest priority than USB_En_TXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x00
23	-	Reserved	Reserved	0x00
22	-	Reserved	Reserved	0x00
21	rw	USB_RXS_LCK6	USB receive data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_RXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_RXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
20	rw	USB_RXSEQ6	USB receive endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit can be written by firmware if the USB_RXS_LCKn bit is set when written along with the new USB_RXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an OUT transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
19	rw	USB_RXSA_LCK6	USB receive control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_RXENn, USB_RXSTLn, USB_RXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these receive control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
18	rw	USB_RXMC6	USB receive memory read complete. Set this bit to release the receive memory when data read is complete. Hardware clears this bit after the memory release operation has been finished. 0 = No : no effect 1 = Complete : read data complete from USB memory	0x01
17	rw	USB_RXSTL6	USB receive endpoint STALL enable. Set this bit to STALL the receive endpoint. Note: Clear this bit only when the host has intervened through commands sent down endpoint-n. When this bit is set, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is clear, the receive endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	0x00
16	rw	USB_RXEN6	USB receive endpoint enable. Set this bit to enable the receive endpoint. When disabled, the endpoint does not respond to a valid OUT token. This bit has the highest priority than USB_En_RXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x00
15	-	Reserved	Reserved	0x00
14	rw	USB_DBM6	USB endpoint double buffer mode enable. This bit is set by the software to enable the double-buffering feature for bulk endpoint. 0 = Disable 1 = Enable	0x00
13	rw	USB_BLSIZE6	USB endpoint memory block size select. When selects '2Byte', the memory block is 2-byte large. With this block size the	0x00

			allocated endpoint memory size ranges from 2 to 62 bytes. When selects '32Byte', the memory block is 32-byte. With this block size the allocated endpoint memory size ranges from 32 to 512 bytes. 0 = 2Byte 1 = 32Byte	
12..8	rw	USB_BLNUM6	USB endpoint memory block number. The endpoint memory size is this value multiplied by USB_BLSIZEn for data receiving overflow detect. (n = endpoint index)	0x00
7	-	Reserved	Reserved	0x00
6	rw	USB_TXTYPE6	USB transmit endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
5	-	Reserved	Reserved	0x00
4	rw	USB_RXTYPE6	USB receive endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
3..0	rw	USB_EPADR6	USB endpoint address. The 4-bit address is used to identify the transactions directed to this endpoint. A value must be written before enabling the corresponding endpoint.	0x00

1.27.34. USB end-point 6 receive register

USB_EP6RX	USB end-point 6 receive register		
Offset Address :	0xA8	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_RXCNT6
23	22	21	20	19	18	17	16
USB_RXCNT6[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_RXADR6
7	6	5	4	3	2	1	0
USB_RXADR6[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_RXCNT6	USB endpoint receive byte count. These bits contain the number of bytes received for the endpoint-n for the last OUT transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_RXADR6	USB endpoint receive buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for OUT transaction. (n = endpoint index)	0x0000

1.27.35. USB end-point 6 transmit register

USB_EP6TX	USB end-point 6 transmit register		
Offset Address :	0xAC	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_TXCNT6
23	22	21	20	19	18	17	16

USB_TXCNT6[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_TXADR6
7	6	5	4	3	2	1	0
USB_TXADR6[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_TXCNT6	USB endpoint transmit byte count. These bits contain the number of bytes received for the endpoint-n for the last IN transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_TXADR6	USB endpoint transmit buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for IN transaction. (n = endpoint index)	0x0000

1.27.36. USB end-point 7 control register 0

USB_EP7CR0	USB end-point 7 control register 0		
Offset Address :	0xB0	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				USB_ISOTXE7F	USB_TXSTL7F	USB_TXNAK7F	USB_TXD7F
23	22	21	20	19	18	17	16
Reserved				USB_ISOOVW7F	USB_RXSTL7F	USB_RXNAK7F	USB_RXD7F
15	14	13	12	11	10	9	8
USB_TXRST7	USB_RXRST7	Reserved					
7	6	5	4	3	2	1	0
Reserved		USB_TXSTL7_IE	USB_TXNAK7_IE	USB_TXD7_IE	USB_RXSTL7_IE	USB_RXNAK7_IE	USB_RXD7_IE

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	USB_ISOTXE7F	USB isochronous transmit data empty loss error flag. This bit is set by hardware as a USB memory access empty loss happen when USB host request the next data but firmware has not yet write the data in time. Firmware can use this bit to make sure whether the data had been empty or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
26	rw	USB_TXSTL7F	USB endpoint transmission STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
25	rw	USB_TXNAK7F	USB endpoint transmission NAK event flag. This bit is set by hardware when detected a transmit done on the NAK packet for IN transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
24	rw	USB_TXD7F	USB endpoint transmission done flag. For single buffer mode, this bit is set when an IN transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-1. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred)	0x00

			1 = Happened (Event happened)	
23..20	-	**Reserved**	Reserved	0x00
19	rw	**USB_ISOOVW7F**	USB isochronous receive data overwrite error flag. This bit is set by hardware as a USB memory access conflict happen when USB host send the next data but firmware has not yet read out the last data in time. Firmware can use this bit to make sure whether the data had been overwritten or not. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
18	rw	**USB_RXSTL7F**	USB endpoint receiving STALL event flag. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	rw	**USB_RXNAK7F**	USB endpoint receiving NAK event flag. This bit is set by hardware when detected a receive done on the NAK packet for OUT transaction of the selected endpoint by USB_NAKEP_SEL. (set by hardware and software write 1 to clear) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
16	rw	**USB_RXD7F**	USB endpoint receiving done flag. For single buffer mode, this bit is set when an OUT transaction is successfully completed on this endpoint. A transaction ended with a NAK or STALL handshake does not set this bit. For double buffer mode, this bit is set when an OUT or IN transaction is successfully completed on the USB Buffer-0. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	rw	**USB_TXRST7**	USB endpoint transmission block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
14	rw	**USB_RXRST7**	USB endpoint receiving block reset and flags clear enable bit. When enables, hardware auto clear after register write access and this bit always returns '0'. 0 = No : no effect 1 = Enable	0x00
13..8	-	**Reserved**	Reserved	0x00
7..6	-	**Reserved**	Reserved	0x00
5	rw	**USB_TXSTL7_IE**	USB endpoint transmission STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	**USB_TXNAK7_IE**	USB endpoint transmission NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	**USB_TXD7_IE**	USB endpoint transmission done interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	**USB_RXSTL7_IE**	USB endpoint receiving STALL event interrupt enable. 0 = Disable 1 = Enable	0x00
1	rw	**USB_RXNAK7_IE**	USB endpoint receiving NAK event interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	**USB_RXD7_IE**	USB endpoint receiving done interrupt enable. 0 = Disable 1 = Enable	0x00

1.27.37. USB end-point 7 control register 1

USB_EP7CR1	USB end-point 7 control register 1		
Offset Address :	0xB4	Reset Value :	0x00040000

31	30	29	28	27	26	25	24
Reserved	Reserved	USB_TXS_LCK7	USB_TXSEQ7	USB_TXSA_LCK7	USB_TXMC7	USB_TXSTL7	USB_TXEN7
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved	Reserved	USB_RXS_LCK7	USB_RXSEQ7	USB_RXSA_LCK7	USB_RXMC7	USB_RXSTL7	USB_RXEN7
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved	USB_DBM7	USB_BLSIZE7	USB_BLNUM7[4:0]				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	USB_TXTYPE7	Reserved	USB_RXTYPE7	USB_EPADR7[3:0]			

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29	rw	USB_TXS_LCK7	USB transmit data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_TXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_TXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
28	rw	USB_TXSEQ7	USB transmit endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be transmitted in the next PID and toggled on a valid ACK handshake of an IN transaction. This bit can be written by firmware if the USB_TXS_LCKn bit is set when written along with the new USB_TXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an IN transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
27	rw	USB_TXSA_LCK7	USB transmit control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_TXENn, USB_TXSTLn, USB_TXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these transmit control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
26	rw	USB_TXMC7	USB transmit memory write complete. Set this bit to release the transmit memory when data write is complete. Hardware clears this bit after the memory release operation has been finished. Firmware should write this bit only after firmware finished writing USB_TXCNTn register. (n = endpoint index) 0 = No : no effect 1 = Complete : write data complete to USB memory	0x00
25	rw	USB_TXSTL7	USB transmit endpoint STALL enable. Set this bit to STALL the transmit endpoint. Clear this bit only when the host has intervened through commands sent down endpoint. When this bit is set, the transmit endpoint will respond with a STALL handshake to a valid IN token. When this bit is clear, the transmit endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	0x00
24	rw	USB_TXEN7	USB transmit endpoint enable. Set this bit to enable the transmit endpoint. When disabled, the endpoint does not respond to a valid IN token. This bit has the highest priority than USB_En_TXSTL. (n = endpoint index)	0x00

			0 = Disable 1 = Enable	
23	-	Reserved	Reserved	0x00
22	-	Reserved	Reserved	0x00
21	rw	USB_RXS_LCK7	USB receive data sequence bit write access un-locked control. Set 'un-locked' to allow the value of the USB_RXSEQn bit to be overwritten. Set 'locked' to this bit makes no effect on USB_RXSEQn. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
20	rw	USB_RXSEQ7	USB receive endpoint sequence bit (read, conditional write). For single buffer mode, this bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit can be written by firmware if the USB_RXS_LCKn bit is set when written along with the new USB_RXSEQn value. For double buffer mode, this bit is used to set the initial USB buffer index for an OUT transaction and read back to indicate which USB buffer is operating by hardware. Value 0 is indicated USB Buffer-0 and value 1 is indicated USB Buffer-1. (n = endpoint index)	0x00
19	rw	USB_RXSA_LCK7	USB receive control register bits write access un-locked control. Set 'un-locked' to allow the value of the USB_RXENn, USB_RXSTLn, USB_RXMCn bits to be overwritten. Set 'locked' to this bit makes no effect on these receive control register bits. Hardware auto clear after register write access and this bit always returns '0' when read. (n = endpoint index) 0 = Locked 1 = un-Locked	0x00
18	rw	USB_RXMC7	USB receive memory read complete. Set this bit to release the receive memory when data read is complete. Hardware clears this bit after the memory release operation has been finished. 0 = No : no effect 1 = Complete : read data complete from USB memory	0x01
17	rw	USB_RXSTL7	USB receive endpoint STALL enable. Set this bit to STALL the receive endpoint. Note: Clear this bit only when the host has intervened through commands sent down endpoint-n. When this bit is set, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is clear, the receive endpoint will NAK. (n = endpoint index) 0 = Disable 1 = Enable	0x00
16	rw	USB_RXEN7	USB receive endpoint enable. Set this bit to enable the receive endpoint. When disabled, the endpoint does not respond to a valid OUT token. This bit has the highest priority than USB_En_RXSTL. (n = endpoint index) 0 = Disable 1 = Enable	0x00
15	-	Reserved	Reserved	0x00
14	rw	USB_DBM7	USB endpoint double buffer mode enable. This bit is set by the software to enable the double-buffering feature for bulk endpoint. 0 = Disable 1 = Enable	0x00
13	rw	USB_BLSIZE7	USB endpoint memory block size select. When selects '2Byte', the memory block is 2-byte large. With this block size the allocated endpoint memory size ranges from 2 to 62 bytes. When selects '32Byte', the memory block is 32-byte. With this block size the allocated endpoint memory size ranges from 32 to 512 bytes. 0 = 2Byte	0x00

			1 = 32Byte	
12..8	rw	USB_BLNUM7	USB endpoint memory block number. The endpoint memory size is this value multiplied by USB_BLSIZEn for data receiving overflow detect. (n = endpoint index)	0x00
7	-	Reserved	Reserved	0x00
6	rw	USB_TXTYPE7	USB transmit endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
5	-	Reserved	Reserved	0x00
4	rw	USB_RXTYPE7	USB receive endpoint type select. When selects 'ISO', configure the endpoint for Isochronous-In transfer type. When selects 'BKINT', the endpoint is for Bulk/Interrupt-In transfer type. 0 = BKINT 1 = ISO	0x00
3..0	rw	USB_EPADR7	USB endpoint address. The 4-bit address is used to identify the transactions directed to this endpoint. A value must be written before enabling the corresponding endpoint.	0x00

1.27.38. USB end-point 7 receive register

USB_EP7RX	USB end-point 7 receive register		
Offset Address :	0xB8	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_RXCNT7
23	22	21	20	19	18	17	16
USB_RXCNT7[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_RXADR7
7	6	5	4	3	2	1	0
USB_RXADR7[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	Reserved	Reserved	0x00
24..16	rw	USB_RXCNT7	USB endpoint receive byte count. These bits contain the number of bytes received for the endpoint-n for the last OUT transaction. (n = endpoint index)	0x0000
15..9	-	Reserved	Reserved	0x00
8..0	rw	USB_RXADR7	USB endpoint receive buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for OUT transaction. (n = endpoint index)	0x0000

1.27.39. USB end-point 7 transmit register

USB_EP7TX	USB end-point 7 transmit register		
Offset Address :	0xBC	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							USB_TXCNT7
23	22	21	20	19	18	17	16
USB_TXCNT7[7:0]							
15	14	13	12	11	10	9	8
Reserved							USB_TXADR7
7	6	5	4	3	2	1	0
USB_TXADR7[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..25	-	**Reserved**	Reserved	0x00
24..16	rw	**USB_TXCNT7**	USB endpoint transmit byte count. These bits contain the number of bytes received for the endpoint-n for the last IN transaction. (n = endpoint index)	0x0000
15..9	-	**Reserved**	Reserved	0x00
8..0	rw	**USB_TXADR7**	USB endpoint transmit buffer start address. These bits point to the starting address of the packet buffer, which will contain the data received for the endpoint-n for IN transaction. (n = endpoint index)	0x0000

1.27.40. USB Register Map

USB Register Map Register Number = 39

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	USB_STA	USB_SE1F	USB_BSUSF[1:0]		Reserved	USB_RWKF	USB_RSTF	USB_RSMF	USB_SUSF	Reserved	USB_CRCF	USB_BSTF	USB_NORSF	USB_SETUPF	USB_OVRF	Reserved		USB_EP7F	USB_EP6F	USB_EP5F	USB_EP4F	USB_EP3F	USB_EP2F	USB_EP1F	USB_EP0F	USB_LPMF	Reserved	USB_ESOF	USB_SOF	USB_ERRF	Reserved	USB_BUSF	USB_BUSYF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	USB_INT	USB_SE1_IE	Reserved			USB_RWK_IE	USB_RST_IE	USB_RSM_IE	USB_SUS_IE	Reserved	USB_CRC_IE	USB_BST_IE	USB_NORS_IE	USB_SETUP_IE	USB_OVR_IE	Reserved		USB_EP7_IE	USB_EP6_IE	USB_EP5_IE	USB_EP4_IE	USB_EP3_IE	USB_EP2_IE	USB_EP1_IE	USB_EP0_IE	USB_LPM_IE	Reserved	USB_ESOF_IE	USB_SOF_IE	USB_ERR_IE	Reserved	USB_BUS_IE	USB_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	USB_CLK	USB_GPR[7:0]								Reserved								Reserved															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	USB_STA2	Reserved					USB_FNUM[10:0]											Reserved				Reserved		Reserved	Reserved	USB_K_STA	USB_J_STA	USB_SE1_STA	USB_SE0_STA	USB_DMI_STA	USB_DPI_STA	Reserved	USB_DI_STA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	USB_CR0	Reserved	Reserved	Reserved						USB_DP_ODC	USB_DM_ODC	Reserved	USB_DP_PD	USB_DM_PD	Reserved	Reserved	USB_DPU_EN	Reserved		USB_NORS_EN	Reserved	USB_STP_LVR	USB_RWK_TRG	Reserved	USB_RWK_MDS	USB_RWK_DSEL [1:0]		Reserved	USB_SUS_MDS	USB_V33_VDD	USB_V33_EN	USB_XTR_EN	USB_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	USB_CR1	Reserved		Reserved	USB_LPMNYF	Reserved		Reserved	USB_LPMNY_IE	USB_LPM_BESL [3:0]				Reserved	USB_LPM_RWK	USB_LPM_ACK	USB_LPM_EN	Reserved								Reserved	USB_ADR[6:0]						
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	USB_CR2	Reserved																Reserved								Reserved	USB_DMA_TXSEL0 [2:0]			Reserved	USB_DMA_RXSEL0 [2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	USB_EP0CR0	Reserved				Reserved	USB_TXSTL0F	USB_TXNAK0F	USB_TXD0F	Reserved		Reserved		Reserved	USB_RXSTL0F	USB_RXNAK0F	USB_RXD0F	USB_TXRST0	USB_RXRST0	Reserved			USB_SETUP0F	USB_EDOVW0F	USB_STOVW0F	Reserved		USB_TXSTL0_IE	USB_TXNAK0_IE	USB_TXD0_IE	USB_RXSTL0_IE	USB_RXNAK0_IE	USB_RXD0_IE
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x44	USB_EP0CR1	Reserved	Reserved	USB_TXS_LCK0	USB_TXSEQ0	USB_TXSA_LCK0	USB_TXMC0	USB_TXSTL0	USB_TXEN0	Reserved	Reserved	USB_RXS_LCK0	USB_RXSEQ0	USB_RXSA_LCK0	USB_RXMC0	USB_RXSTL0	USB_RXEN0	Reserved	Reserved	USB_BLSIZE0	USB_BLNUM0[4:0]					Reserved	Reserved	Reserved	Reserved	Reserved			
Reset	**0x01050000**	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x48	USB_EP0RX	Reserved							USB_RXCNT0[8:0]									Reserved							USB_RXADR0[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x4C	USB_EP0TX	Reserved							USB_TXCNT0[8:0]									Reserved							USB_TXADR0[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	USB_EP1CR0	Reserved				USB_ISOTXE1F	USB_TXSTL1F	USB_TXNAK1F	USB_TXD1F	Reserved		Reserved		USB_ISOOVW1F	USB_RXSTL1F	USB_RXNAK1F	USB_RXD1F	USB_TXRST1	USB_RXRST1	Reserved			Reserved	Reserved	Reserved	Reserved		USB_TXSTL1_IE	USB_TXNAK1_IE	USB_TXD1_IE	USB_RXSTL1_IE	USB_RXNAK1_IE	USB_RXD1_IE
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x54	USB_EP1CR1	Reserved	Reserved	USB_TXS_LCK1	USB_TXSEQ1	USB_TXSA_LCK1	USB_TXMC1	USB_TXSTL1	USB_TXEN1	Reserved	Reserved	USB_RXS_LCK1	USB_RXSEQ1	USB_RXSA_LCK1	USB_RXMC1	USB_RXSTL1	USB_RXEN1	Reserved	USB_DBM1	USB_BLSIZE1	USB_BLNUM1[4:0]					Reserved	USB_TXTYPE1	Reserved	USB_RXTYPE1	USB_EPADR1[3:0]			
Reset	**0x00040000**	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x58	USB_EP1RX	Reserved							USB_RXCNT1[8:0]									Reserved							USB_RXADR1[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x5C	USB_EP1TX	Reserved							USB_TXCNT1[8:0]									Reserved							USB_TXADR1[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x60	USB_EP2CR0	Reserved				USB_ISOTXE2F	USB_TXSTL2F	USB_TXNAK2F	USB_TXD2F	Reserved				USB_ISOOVW2F	USB_RXSTL2F	USB_RXNAK2F	USB_RXD2F	USB_TXRST2	USB_RXRST2	Reserved						Reserved		USB_TXSTL2_IE	USB_TXNAK2_IE	USB_TXD2_IE	USB_RXSTL2_IE	USB_RXNAK2_IE	USB_RXD2_IE
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x64	USB_EP2CR1	Reserved	Reserved	USB_TXS_LCK2	USB_TXSEQ2	USB_TXSA_LCK2	USB_TXMC2	USB_TXSTL2	USB_TXEN2	Reserved	Reserved	USB_RXS_LCK2	USB_RXSEQ2	USB_RXSA_LCK2	USB_RXMC2	USB_RXSTL2	USB_RXEN2	Reserved	USB_DBM2	USB_BLSIZE2	USB_BLNUM2[4:0]					Reserved	USB_TXTYPE2	Reserved	USB_RXTYPE2	USB_EPADR2[3:0]			
Reset	**0x00040000**	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x68	USB_EP2RX	Reserved							USB_RXCNT2[8:0]									Reserved							USB_RXADR2[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x6C	USB_EP2TX	Reserved							USB_TXCNT2[8:0]									Reserved							USB_TXADR2[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x70	USB_EP3CR0	Reserved				USB_ISOTXE3F	USB_TXSTL3F	USB_TXNAK3F	USB_TXD3F	Reserved				USB_ISOOVW3F	USB_RXSTL3F	USB_RXNAK3F	USB_RXD3F	USB_TXRST3	USB_RXRST3	Reserved						Reserved		USB_TXSTL3_IE	USB_TXNAK3_IE	USB_TXD3_IE	USB_RXSTL3_IE	USB_RXNAK3_IE	USB_RXD3_IE
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x74	USB_EP3CR1	Reserved	Reserved	USB_TXS_LCK3	USB_TXSEQ3	USB_TXSA_LCK3	USB_TXMC3	USB_TXSTL3	USB_TXEN3	Reserved	Reserved	USB_RXS_LCK3	USB_RXSEQ3	USB_RXSA_LCK3	USB_RXMC3	USB_RXSTL3	USB_RXEN3	Reserved	USB_DBM3	USB_BLSIZE3	USB_BLNUM3[4:0]					Reserved	USB_TXTYPE3	Reserved	USB_RXTYPE3	USB_EPADR3[3:0]			
Reset	**0x00040000**	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x78	USB_EP3RX	Reserved							USB_RXCNT3[8:0]									Reserved							USB_RXADR3[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x7C	USB_EP3TX	Reserved							USB_TXCNT3[8:0]									Reserved							USB_TXADR3[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x80	USB_EP4CR0	Reserved				USB_ISOTXE4F	USB_TXSTL4F	USB_TXNAK4F	USB_TXD4F	Reserved				USB_ISOOVW4F	USB_RXSTL4F	USB_RXNAK4F	USB_RXD4F	USB_TXRST4	USB_RXRST4	Reserved						Reserved		USB_TXSTL4_IE	USB_TXNAK4_IE	USB_TXD4_IE	USB_RXSTL4_IE	USB_RXNAK4_IE	USB_RXD4_IE
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x84	USB_EP4CR1	Reserved	Reserved	USB_TXS_LCK4	USB_TXSEQ4	USB_TXSA_LCK4	USB_TXMC4	USB_TXSTL4	USB_TXEN4	Reserved	Reserved	USB_RXS_LCK4	USB_RXSEQ4	USB_RXSA_LCK4	USB_RXMC4	USB_RXSTL4	USB_RXEN4	Reserved	USB_DBM4	USB_BLSIZE4	USB_BLNUM4[4:0]					Reserved	USB_TXTYPE4	Reserved	USB_RXTYPE4	USB_EPADR4[3:0]			
Reset	**0x00040000**	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x88	USB_EP4RX	Reserved							USB_RXCNT4[8:0]									Reserved							USB_RXADR4[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x8C	USB_EP4TX	Reserved							USB_TXCNT4[8:0]									Reserved							USB_TXADR4[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x90	USB_EP5CR0	Reserved				USB_ISOTXE5F	USB_TXSTL5F	USB_TXNAK5F	USB_TXD5F	Reserved				USB_ISOOVW5F	USB_RXSTL5F	USB_RXNAK5F	USB_RXD5F	USB_TXRST5	USB_RXRST5	Reserved						Reserved		USB_TXSTL5_IE	USB_TXNAK5_IE	USB_TXD5_IE	USB_RXSTL5_IE	USB_RXNAK5_IE	USB_RXD5_IE
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x94	USB_EP5CR1	Reserved	Reserved	USB_TXS_LCK5	USB_TXSEQ5	USB_TXSA_LCK5	USB_TXMC5	USB_TXSTL5	USB_TXEN5	Reserved	Reserved	USB_RXS_LCK5	USB_RXSEQ5	USB_RXSA_LCK5	USB_RXMC5	USB_RXSTL5	USB_RXEN5	Reserved	USB_DBM5	USB_BLSIZE5	USB_BLNUM5[4:0]					Reserved	USB_TXTYPE5	Reserved	USB_RXTYPE5	USB_EPADR5[3:0]			
Reset	**0x00040000**	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x98	USB_EP5RX	Reserved							USB_RXCNT5[8:0]									Reserved							USB_RXADR5[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x9C	USB_EP5TX	Reserved							USB_TXCNT5[8:0]									Reserved							USB_TXADR5[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xA0	USB_EP6CR0	Reserved				USB_ISOTXE6F	USB_TXSTL6F	USB_TXNAK6F	USB_TXD6F	Reserved				USB_ISOOVW6F	USB_RXSTL6F	USB_RXNAK6F	USB_RXD6F	USB_TXRST6	USB_RXRST6	Reserved						Reserved		USB_TXSTL6_IE	USB_TXNAK6_IE	USB_TXD6_IE	USB_RXSTL6_IE	USB_RXNAK6_IE	USB_RXD6_IE
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xA4	USB_EP6CR1	Reserved	Reserved	USB_TXS_LCK6	USB_TXSEQ6	USB_TXSA_LCK6	USB_TXMC6	USB_TXSTL6	USB_TXEN6	Reserved	Reserved	USB_RXS_LCK6	USB_RXSEQ6	USB_RXSA_LCK6	USB_RXMC6	USB_RXSTL6	USB_RXEN6	Reserved	USB_DBM6	USB_BLSIZE6	USB_BLNUM6[4:0]					Reserved	USB_TXTYPE6	Reserved	USB_RXTYPE6	USB_EPADR6[3:0]			
Reset	**0x00040000**	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xA8	USB_EP6RX	Reserved							USB_RXCNT6[8:0]									Reserved							USB_RXADR6[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xAC	USB_EP6TX	Reserved							USB_TXCNT6[8:0]									Reserved							USB_TXADR6[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Addr	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xB0	USB_EP7CR0	Reserved				USB_ISOTXE7F	USB_TXSTL7F	USB_TXNAK7F	USB_TXD7F	Reserved				USB_ISOOVW7F	USB_RXSTL7F	USB_RXNAK7F	USB_RXD7F	USB_TXRST7	USB_RXRST7	Reserved						Reserved		USB_TXSTL7_IE	USB_TXNAK7_IE	USB_TXD7_IE	USB_RXSTL7_IE	USB_RXNAK7_IE	USB_RXD7_IE
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xB4	USB_EP7CR1	Reserved	Reserved	USB_TXS_LCK7	USB_TXSEQ7	USB_TXSA_LCK7	USB_TXMC7	USB_TXSTL7	USB_TXEN7	Reserved	Reserved	USB_RXS_LCK7	USB_RXSEQ7	USB_RXSA_LCK7	USB_RXMC7	USB_RXSTL7	USB_RXEN7	Reserved	USB_DBM7	USB_BLSIZE7	USB_BLNUM7[4:0]					Reserved	USB_TXTYPE7	Reserved	USB_RXTYPE7	USB_EPADR7[3:0]			
Reset	**0x00040000**	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xB8	USB_EP7RX	Reserved							USB_RXCNT7[8:0]									Reserved							USB_RXADR7[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xBC	USB_EP7TX	Reserved							USB_TXCNT7[8:0]									Reserved							USB_TXADR7[8:0]								
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.28. Timer00 Control Registers

Timer00 Control	(TM00) Timer Control Module-00
Base Address :	0x55000000

1.28.1. TM00 Timer status register

TM00_STA	TM00 Timer status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM00_TUF2	Reserved	TM00_TOF2	TM00_TOF	TM00_EXF	Reserved		Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	rw	TM00_TUF2	2nd Timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	-	Reserved	Reserved	0x00
5	rw	TM00_TOF2	2nd Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	TM00_TOF	Main Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	TM00_EXF	Timer external trigger flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2..1	-	Reserved	Reserved	0x00
0	-	Reserved	Reserved	0x00

1.28.2. TM00 Timer interrupt enable register

TM00_INT	TM00 Timer interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		TM00_TIE2	TM00_TIE	TM00_EXIE	Reserved		TM00_IEA

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00

5	rw	**TM00_TIE2**	2nd Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	**TM00_TIE**	Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	**TM00_EXIE**	Timer external trigger interrupt enable. 0 = Disable 1 = Enable	0x00
2..1	-	**Reserved**	Reserved	0x00
0	rw	**TM00_IEA**	Timer interrupt all enable. When disables, the timer global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.28.3. TM00 Timer clock source register

TM00_CLK	TM00 Timer clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		TM00_CKI_DIV[1:0]		Reserved		TM00_CKI_SEL[1:0]	
7	6	5	4	3	2	1	0
TM00_CKS2_SEL	TM00_CKS_SEL	TM00_CKE_SEL[1:0]		Reserved	Reserved		

Bit	Attr	Bit Name	Description	Reset
31..16	-	**Reserved**	Reserved	0x0000
15..14	-	**Reserved**	Reserved	0x00
13..12	rw	**TM00_CKI_DIV**	Timer internal clock CK_TM00_INT input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
11..10	-	**Reserved**	Reserved	0x00
9..8	rw	**TM00_CKI_SEL**	Timer input clock CK_TM00_INT source select. 0x0 = PROC : CK_TM00_PR process clock from CSC 0x1 = Reserved 0x2 = CK_LS 0x3 = Reserved	0x00
7	rw	**TM00_CKS2_SEL**	Counter/Timer CK_TC2 clock source select. 0 = CK_INT 1 = CK_EXT	0x00
6	rw	**TM00_CKS_SEL**	Counter/Timer CK_TC clock source select. 0 = CK_INT 1 = CK_EXT	0x00
5..4	rw	**TM00_CKE_SEL**	Timer internal clock CK_EXT source select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = Reserved 0x3 = Reserved	0x00
3	-	**Reserved**	Reserved	0x00
2..0	-	**Reserved**	Reserved	0x00

1.28.4. TM00 Timer trigger control register

TM00_TRG	TM00 Timer trigger control register		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
TM00_GT2_SW	TM00_GT_SW	TM00_RST2_SW	TM00_RST_SW	Reserved		TM00_TRGO_INV	TM00_TRGO_SW
23	22	21	20	19	18	17	16
TM00_UEV_SEL[1:0]		Reserved					
15	14	13	12	11	10	9	8
TM00_TRGO_MDS[3:0]				Reserved	TM00_ITR_MUX[2:0]		
7	6	5	4	3	2	1	0
TM00_TRG_MUX[1:0]		TM00_TRGI2_MDS[2:0]			TM00_TRGI_MDS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31	rw	TM00_GT2_SW	2nd Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
30	rw	TM00_GT_SW	Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
29	rw	TM00_RST2_SW	2nd Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
28	rw	TM00_RST_SW	Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
27..26	-	Reserved	Reserved	0x00
25	rw	TM00_TRGO_INV	Timer TRGO output inverse enable bit. 0 = Disable 1 = Enable	0x00
24	rw	TM00_TRGO_SW	Timer TRGO software control data bit. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
23..22	rw	TM00_UEV_SEL	Timer UEV output select bits for TM00_TRGO. When TM00_TRGO_MDS selects UEV as output signal, this bit uses to select output pulse function from Main timer overflow and/or underflow. These bits are no effect when TM00_TRGO_MDS does not select UEV as output. 0x0 = All : output all UEV pulses 0x1 = TOF : output timer overflow pulses 0x2 = UDF : output timer underflow pulses 0x3 = Reserved	0x00
21..16	-	Reserved	Reserved	0x00
15..12	rw	TM00_TRGO_MDS	Timer trigger output mode select 0x0 = RST : TM00_RST (Main Timer Reset) 0x1 = EN : TM00_EN (Main Timer Enable) 0x2 = UEV : TM00_UEV (Main Timer Update event) 0x3 = TOF : TM00_TOF (Main Timer overflow) 0x4 = Reserved 0x5 = EN2 : TM00_EN2 (Timer-2 Enable) 0x6 = TOF2 :TM00_TOF2 (Timer-2 overflow) 0x7 = Reserved 0x8 = UEV2 : TM00_UEV2 (Timer-2 Update event) 0x9 = SW : TM00_TRGO_SW (software control bit) 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = Reserved 0xE = TRGI : TM00_TRGI (internal TRGI signal) 0xF = Reserved	0x00
11	-	Reserved	Reserved	0x00

10..8	rw	TM00_ITR_MUX	Timer internal trigger source select. See the [Timer Internal Trigger and Channel Input Signals Table] for more information. 0x0 = ITR0 (TM00_ITR0) 0x1 = ITR1 (TM00_ITR1) 0x2 = ITR2 (TM00_ITR2) 0x3 = ITR3 (TM00_ITR3) 0x4 = ITR4 (TM00_ITR4) 0x5 = ITR5 (TM00_ITR5) 0x6 = ITR6 (TM00_ITR6) 0x7 = ITR7 (TM00_ITR7)	0x00
7..6	rw	TM00_TRG_MUX	Timer trigger source TRGI select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = Reserved 0x3 = Reserved	0x00
5..3	rw	TM00_TRGI2_MDS	2nd Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00
2..0	rw	TM00_TRGI_MDS	Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00

1.28.5. TM00 Timer control register 0

TM00_CR0	TM00 Timer control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM00_UEX_EN	TM00_USW_EN	Reserved	TM00_UEV_DIS	TM00_EX_INV	TM00_EX_EN	TM00_ACLEAR_EN	TM00_ASTOP_EN
7	6	5	4	3	2	1	0
TM00_DIR2	Reserved	TM00_MDS[1:0]		Reserved	Reserved	TM00_EN2	TM00_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	TM00_UEX_EN	Timer external trigger update event enable. 0 = Disable 1 = Enable	0x00
14	rw	TM00_USW_EN	Timer software update event generation enable. (automatically clear by hardware) 0 = Disable 1 = Enable	0x00
13	-	Reserved	Reserved	0x00
12	rw	TM00_UEV_DIS	Update event generation disable for main Timer. Update event is generation from counter overflow/underflow or software	0x00

			register forced bit. 0 = Enable 1 = Disable	
11	rw	TM00_EX_INV	Timer external trigger input inverted enable. 0 = Normal 1 = Inverted	0x00
10	rw	TM00_EX_EN	Timer external trigger event enable. 0 = Disable 1 = Enable	0x00
9	rw	TM00_ACLEAR_EN	Timer overflow or underflow flag auto-clear enable. This bit is no effect if TMx_ASTOP_EN is disabled. When enables, the timer will auto clear the flag of TMx_TOF or TMx_TUF after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
8	rw	TM00_ASTOP_EN	Timer auto stop mode enable. When enables, the timer will auto stop after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
7	rw	TM00_DIR2	2nd Timer counting direction bit. 0 = Up (Up Counting) 1 = Down (Down Counting)	0x00
6	-	Reserved	Reserved	0x00
5..4	rw	TM00_MDS	Timer operation mode select. When selects 'Cascade', both TMx_EN and TMx_EN2 must set the same setting of Enable or Disable. (x : module index) 0x0 = Cascade : 8-bit counter with 8-bit prescaler Mode 0x1 = Separate : Separated two 8-bit counters Mode 0x2 = Full-Counter : 16-bit counter Mode 0x3 = Reserved	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	rw	TM00_EN2	2nd Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00
0	rw	TM00_EN	Main Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00

1.28.6. TM00 Timer CKO control register

TM00_CKO	TM00 Timer CKO control register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				TM00_CKO_LCK	TM00_CKO_STA	TM00_CKO_SEL	TM00_CKO_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	TM00_CKO_LCK	TM00_CKO_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access.	0x00

			0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	
2	rw	TM00_CKO_STA	Timer CKO output signal initial state. The bit is written effectively only by written 1 to TM00_CKO_LCK simultaneously. 0 = Output 0 1 = Output 1	0x00
1	rw	TM00_CKO_SEL	Timer overflow as CKO output source select. 0 = 2nd : 2nd Timer overflow 1 = Main : Main Timer overflow	0x00
0	rw	TM00_CKO_EN	Timer overflow as CKO output enable. 0 = Disable 1 = Enable	0x00

1.28.7. TM00 Timer main counter register

TM00_CNT	TM00 Timer main counter register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM00_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	TM00_CNT	Main timer/counter register.	0x00

1.28.8. TM00 Timer main counter auto-reload value register

TM00_ARR	TM00 Timer main counter auto-reload value register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM00_ARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	TM00_ARR	Main timer/counter auto-reload value register	0x00

1.28.9. TM00 Timer prescaler register

TM00_PSCNT	TM00 Timer prescaler register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM00_CNTA[7:0]							
7	6	5	4	3	2	1	0
TM00_PSCNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	r	TM00_CNTA	Main timer/counter alias register. This register is the alias of TM00_CNT for read only.	0x00
7..0	rw	TM00_PSCNT	Timer prescaler or 2nd timer/counter register	0x00

1.28.10. TM00 Timer prescaler auto-reload register

TM00_PSARR	TM00 Timer prescaler auto-reload register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM00_PSARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	TM00_PSARR	Timer prescaler or 2nd timer/counter auto-reload value register	0x00

1.28.11. TM00 Register Map

TM00 Register Map Register Number = 10

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	TM00_STA	Reserved																Reserved								TM00_TUF2	Reserved	TM00_TOF2	TM00_TOF	TM00_EXF	Reserved		Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	TM00_INT	Reserved																Reserved								Reserved		TM00_TIE2	TM00_TIE	TM00_EXIE	Reserved		TM00_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	TM00_CLK	Reserved																Reserved		TM00_CKI_DIV [1:0]		Reserved		TM00_CKI_SEL [1:0]		TM00_CKS2_SEL	TM00_CKS_SEL	TM00_CKE_SEL [1:0]		Reserved	Reserved		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	TM00_TRG	TM00_GT2_SW	TM00_GT_SW	TM00_RST2_SW	TM00_RST_SW	Reserved		TM00_TRGO_INV	TM00_TRGO_SW	TM00_UEV_SEL [1:0]		Reserved						TM00_TRGO_MDS [3:0]				Reserved	TM00_ITR_MUX [2:0]			TM00_TRG_MUX [1:0]		TM00_TRGI2_MDS [2:0]			TM00_TRGI_MDS [2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	TM00_CR0	Reserved																TM00_UEX_EN	TM00_USW_EN	Reserved	TM00_UEV_DIS	TM00_EX_INV	TM00_EX_EN	TM00_ACLEAR_EN	TM00_ASTOP_EN	TM00_DIR2	Reserved	TM00_MDS[1:0]		Reserved	Reserved	TM00_EN2	TM00_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	TM00_CKO	Reserved																Reserved								Reserved				TM00_CKO_LCK	TM00_CKO_STA	TM00_CKO_SEL	TM00_CKO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	TM00_CNT	Reserved																Reserved								TM00_CNT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	TM00_ARR	Reserved																Reserved								TM00_ARR[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<table>
<tr><td>0x28</td><td>TM00_PSCNT</td><td colspan="16">Reserved</td><td colspan="8">TM00_CNTA[7:0]</td><td colspan="8">TM00_PSCNT[7:0]</td></tr>
<tr><td>Reset</td><td>0x00000000</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0x2C</td><td>TM00_PSARR</td><td colspan="16">Reserved</td><td colspan="8">Reserved</td><td colspan="8">TM00_PSARR[7:0]</td></tr>
<tr><td>Reset</td><td>0x00000000</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

1.29. Timer01 Control Registers

Timer01 Control	(TM01) Timer Control Module-01
Base Address :	0x55010000

1.29.1. TM01 Timer status register

TM01_STA	TM01 Timer status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM01_TUF2	Reserved	TM01_TOF2	TM01_TOF	TM01_EXF	Reserved		Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	rw	TM01_TUF2	2nd Timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	-	Reserved	Reserved	0x00
5	rw	TM01_TOF2	2nd Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	TM01_TOF	Main Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	TM01_EXF	Timer external trigger flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2..1	-	Reserved	Reserved	0x00
0	-	Reserved	Reserved	0x00

1.29.2. TM01 Timer interrupt enable register

TM01_INT	TM01 Timer interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		TM01_TIE2	TM01_TIE	TM01_EXIE	Reserved		TM01_IEA

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00

5	rw	TM01_TIE2	2nd Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	TM01_TIE	Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	TM01_EXIE	Timer external trigger interrupt enable. 0 = Disable 1 = Enable	0x00
2..1	-	Reserved	Reserved	0x00
0	rw	TM01_IEA	Timer interrupt all enable. When disables, the timer global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.29.3. TM01 Timer clock source register

TM01_CLK	TM01 Timer clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		TM01_CKI_DIV[1:0]		Reserved		TM01_CKI_SEL[1:0]	
7	6	5	4	3	2	1	0
TM01_CKS2_SEL	TM01_CKS_SEL	TM01_CKE_SEL[1:0]		Reserved	Reserved		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13..12	rw	TM01_CKI_DIV	Timer internal clock CK_TM01_INT input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
11..10	-	Reserved	Reserved	0x00
9..8	rw	TM01_CKI_SEL	Timer input clock CK_TM01_INT source select. 0x0 = PROC : CK_TM01_PR process clock from CSC 0x1 = Reserved 0x2 = CK_LS 0x3 = Reserved	0x00
7	rw	TM01_CKS2_SEL	Counter/Timer CK_TC2 clock source select. 0 = CK_INT 1 = CK_EXT	0x00
6	rw	TM01_CKS_SEL	Counter/Timer CK_TC clock source select. 0 = CK_INT 1 = CK_EXT	0x00
5..4	rw	TM01_CKE_SEL	Timer internal clock CK_EXT source select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = Reserved 0x3 = Reserved	0x00
3	-	Reserved	Reserved	0x00
2..0	-	Reserved	Reserved	0x00

1.29.4. TM01 Timer trigger control register

TM01_TRG	TM01 Timer trigger control register		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
TM01_GT2_SW	TM01_GT_SW	TM01_RST2_SW	TM01_RST_SW	Reserved		TM01_TRGO_INV	TM01_TRGO_SW
23	22	21	20	19	18	17	16
TM01_UEV_SEL[1:0]		Reserved					
15	14	13	12	11	10	9	8
TM01_TRGO_MDS[3:0]				Reserved	TM01_ITR_MUX[2:0]		
7	6	5	4	3	2	1	0
TM01_TRG_MUX[1:0]		TM01_TRGI2_MDS[2:0]			TM01_TRGI_MDS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31	rw	TM01_GT2_SW	2nd Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
30	rw	TM01_GT_SW	Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
29	rw	TM01_RST2_SW	2nd Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
28	rw	TM01_RST_SW	Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
27..26	-	Reserved	Reserved	0x00
25	rw	TM01_TRGO_INV	Timer TRGO output inverse enable bit. 0 = Disable 1 = Enable	0x00
24	rw	TM01_TRGO_SW	Timer TRGO software control data bit. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
23..22	rw	TM01_UEV_SEL	Timer UEV output select bits for TM01_TRGO. When TM01_TRGO_MDS selects UEV as output signal, this bit uses to select output pulse function from Main timer overflow and/or underflow. These bits are no effect when TM01_TRGO_MDS does not select UEV as output. 0x0 = All : output all UEV pulses 0x1 = TOF : output timer overflow pulses 0x2 = UDF : output timer underflow pulses 0x3 = Reserved	0x00
21..16	-	Reserved	Reserved	0x00
15..12	rw	TM01_TRGO_MDS	Timer trigger output mode select 0x0 = RST : TM01_RST (Main Timer Reset) 0x1 = EN : TM01_EN (Main Timer Enable) 0x2 = UEV : TM01_UEV (Main Timer Update event) 0x3 = TOF : TM01_TOF (Main Timer overflow) 0x4 = Reserved 0x5 = EN2 : TM01_EN2 (Timer-2 Enable) 0x6 = TOF2 :TM01_TOF2 (Timer-2 overflow) 0x7 = Reserved 0x8 = UEV2 : TM01_UEV2 (Timer-2 Update event) 0x9 = SW : TM01_TRGO_SW (software control bit) 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = Reserved 0xE = TRGI : TM01_TRGI (internal TRGI signal) 0xF = Reserved	0x00
11	-	Reserved	Reserved	0x00

10..8	rw	TM01_ITR_MUX	Timer internal trigger source select. See the [Timer Internal Trigger and Channel Input Signals Table] for more information. 0x0 = ITR0 (TM01_ITR0) 0x1 = ITR1 (TM01_ITR1) 0x2 = ITR2 (TM01_ITR2) 0x3 = ITR3 (TM01_ITR3) 0x4 = ITR4 (TM01_ITR4) 0x5 = ITR5 (TM01_ITR5) 0x6 = ITR6 (TM01_ITR6) 0x7 = ITR7 (TM01_ITR7)	0x00
7..6	rw	TM01_TRG_MUX	Timer trigger source TRGI select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = Reserved 0x3 = Reserved	0x00
5..3	rw	TM01_TRGI2_MDS	2nd Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00
2..0	rw	TM01_TRGI_MDS	Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00

1.29.5. TM01 Timer control register 0

TM01_CR0	TM01 Timer control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM01_UEX_EN	TM01_USW_EN	Reserved	TM01_UEV_DIS	TM01_EX_INV	TM01_EX_EN	TM01_ACLEAR_EN	TM01_ASTOP_EN
7	6	5	4	3	2	1	0
TM01_DIR2	Reserved	TM01_MDS[1:0]		Reserved	Reserved	TM01_EN2	TM01_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	TM01_UEX_EN	Timer external trigger update event enable. 0 = Disable 1 = Enable	0x00
14	rw	TM01_USW_EN	Timer software update event generation enable. (automatically clear by hardware) 0 = Disable 1 = Enable	0x00
13	-	Reserved	Reserved	0x00
12	rw	TM01_UEV_DIS	Update event generation disable for main Timer. Update event is generation from counter overflow/underflow or software	0x00

			register forced bit. 0 = Enable 1 = Disable	
11	rw	TM01_EX_INV	Timer external trigger input inverted enable. 0 = Normal 1 = Inverted	0x00
10	rw	TM01_EX_EN	Timer external trigger event enable. 0 = Disable 1 = Enable	0x00
9	rw	TM01_ACLEAR_EN	Timer overflow or underflow flag auto-clear enable. This bit is no effect if TMx_ASTOP_EN is disabled. When enables, the timer will auto clear the flag of TMx_TOF or TMx_TUF after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
8	rw	TM01_ASTOP_EN	Timer auto stop mode enable. When enables, the timer will auto stop after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
7	rw	TM01_DIR2	2nd Timer counting direction bit. 0 = Up (Up Counting) 1 = Down (Down Counting)	0x00
6	-	Reserved	Reserved	0x00
5..4	rw	TM01_MDS	Timer operation mode select. When selects 'Cascade', both TMx_EN and TMx_EN2 must set the same setting of Enable or Disable. (x : module index) 0x0 = Cascade : 8-bit counter with 8-bit prescaler Mode 0x1 = Separate : Separated two 8-bit counters Mode 0x2 = Full-Counter : 16-bit counter Mode 0x3 = Reserved	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	rw	TM01_EN2	2nd Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00
0	rw	TM01_EN	Main Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00

1.29.6. TM01 Timer CKO control register

TM01_CKO	TM01 Timer CKO control register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				TM01_CKO_LCK	TM01_CKO_STA	TM01_CKO_SEL	TM01_CKO_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	TM01_CKO_LCK	TM01_CKO_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access.	0x00

			0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	
2	rw	TM01_CKO_STA	Timer CKO output signal initial state. The bit is written effectively only by written 1 to TM01_CKO_LCK simultaneously. 0 = Output 0 1 = Output 1	0x00
1	rw	TM01_CKO_SEL	Timer overflow as CKO output source select. 0 = 2nd : 2nd Timer overflow 1 = Main : Main Timer overflow	0x00
0	rw	TM01_CKO_EN	Timer overflow as CKO output enable. 0 = Disable 1 = Enable	0x00

1.29.7. TM01 Timer main counter register

TM01_CNT	TM01 Timer main counter register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM01_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	TM01_CNT	Main timer/counter register.	0x00

1.29.8. TM01 Timer main counter auto-reload value register

TM01_ARR	TM01 Timer main counter auto-reload value register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM01_ARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	TM01_ARR	Main timer/counter auto-reload value register	0x00

1.29.9. TM01 Timer prescaler register

TM01_PSCNT	TM01 Timer prescaler register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM01_CNTA[7:0]							
7	6	5	4	3	2	1	0
TM01_PSCNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	r	TM01_CNTA	Main timer/counter alias register. This register is the alias of TM01_CNT for read only.	0x00
7..0	rw	TM01_PSCNT	Timer prescaler or 2nd timer/counter register	0x00

1.29.10. TM01 Timer prescaler auto-reload register

TM01_PSARR	TM01 Timer prescaler auto-reload register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM01_PSARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	rw	TM01_PSARR	Timer prescaler or 2nd timer/counter auto-reload value register	0x00

1.29.11. TM01 Register Map

TM01 Register Map Register Number = 10

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	TM01_STA	Reserved																Reserved								TM01_TUF2	Reserved	TM01_TOF2	TM01_TOF	TM01_EXF	Reserved		Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	TM01_INT	Reserved																Reserved								Reserved		TM01_TIE2	TM01_TIE	TM01_EXIE	Reserved		TM01_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	TM01_CLK	Reserved																Reserved		TM01_CKI_DIV [1:0]		Reserved		TM01_CKI_SEL [1:0]		TM01_CKS2_SEL	TM01_CKS_SEL	TM01_CKE_SEL [1:0]		Reserved	Reserved		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	TM01_TRG	TM01_GT2_SW	TM01_GT_SW	TM01_RST2_SW	TM01_RST_SW	Reserved		TM01_TRGO_INV	TM01_TRGO_SW	TM01_UEV_SEL [1:0]		Reserved						TM01_TRGO_MDS [3:0]				Reserved	TM01_ITR_MUX [2:0]			TM01_TRG_MUX [1:0]		TM01_TRGI2_MDS [2:0]			TM01_TRGI_MDS [2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	TM01_CR0	Reserved																TM01_UEX_EN	TM01_USW_EN	Reserved	TM01_UEV_DIS	TM01_EX_INV	TM01_EX_EN	TM01_ACLEAR_EN	TM01_ASTOP_EN	TM01_DIR2	Reserved	TM01_MDS[1:0]		Reserved	Reserved	TM01_EN2	TM01_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	TM01_CKO	Reserved																Reserved								Reserved				TM01_CKO_LCK	TM01_CKO_STA	TM01_CKO_SEL	TM01_CKO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	TM01_CNT	Reserved																Reserved								TM01_CNT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	TM01_ARR	Reserved																Reserved								TM01_ARR[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x28	TM01_PSCNT	Reserved																TM01_CNTA[7:0]								TM01_PSCNT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	TM01_PSARR	Reserved																Reserved								TM01_PSARR[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.30. Timer10 Control Registers

Timer10 Control	(TM10) Timer Control Module-10
Base Address :	0x55800000

1.30.1. TM10 Timer status register

TM10_STA	TM10 Timer status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM10_TUF2	Reserved	TM10_TOF2	TM10_TOF	TM10_EXF	Reserved		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	rw	TM10_TUF2	2nd Timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	-	Reserved	Reserved	0x00
5	rw	TM10_TOF2	2nd Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	TM10_TOF	Main Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	TM10_EXF	Timer external trigger flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2..0	-	Reserved	Reserved	0x00

1.30.2. TM10 Timer interrupt enable register

TM10_INT	TM10 Timer interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		TM10_TIE2	TM10_TIE	TM10_EXIE	Reserved		TM10_IEA

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	TM10_TIE2	2nd Timer overflow/underflow interrupt enable.	0x00

			0 = Disable 1 = Enable	
4	rw	TM10_TIE	Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	TM10_EXIE	Timer external trigger interrupt enable. 0 = Disable 1 = Enable	0x00
2..1	-	Reserved	Reserved	0x00
0	rw	TM10_IEA	Timer interrupt all enable. When disables, the timer global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.30.3. TM10 Timer clock source register

TM10_CLK	TM10 Timer clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		TM10_CKI_DIV[1:0]		Reserved		TM10_CKI_SEL[1:0]	
7	6	5	4	3	2	1	0
TM10_CKS2_SEL	TM10_CKS_SEL	TM10_CKE_SEL[1:0]		Reserved			

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13..12	rw	TM10_CKI_DIV	Timer internal clock CK_TM10_INT input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
11..10	-	Reserved	Reserved	0x00
9..8	rw	TM10_CKI_SEL	Timer input clock CK_TM10 source select. 0x0 = PROC : CK_TM10_PR process clock from CSC 0x1 = Reserved 0x2 = CK_LS 0x3 = Reserved	0x00
7	rw	TM10_CKS2_SEL	Counter/Timer CK_TC2 clock source select. 0 = CK_INT 1 = CK_EXT	0x00
6	rw	TM10_CKS_SEL	Counter/Timer CK_TC clock source select. 0 = CK_INT 1 = CK_EXT	0x00
5..4	rw	TM10_CKE_SEL	Timer internal clock CK_EXT source select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = Reserved 0x3 = Reserved	0x00
3..0	-	Reserved	Reserved	0x00

1.30.4. TM10 Timer trigger control register

TM10_TRG	TM10 Timer trigger control register

Offset Address : 0x0C Reset Value : 0x00000000

31	30	29	28	27	26	25	24
TM10_GT2_SW	TM10_GT_SW	TM10_RST2_SW	TM10_RST_SW	Reserved		TM10_TRGO_INV	TM10_TRGO_SW
23	22	21	20	19	18	17	16
TM10_UEV_SEL[1:0]		Reserved					
15	14	13	12	11	10	9	8
TM10_TRGO_MDS[3:0]				Reserved	TM10_ITR_MUX[2:0]		
7	6	5	4	3	2	1	0
TM10_TRG_MUX[1:0]		TM10_TRGI2_MDS[2:0]			TM10_TRGI_MDS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31	rw	TM10_GT2_SW	2nd Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
30	rw	TM10_GT_SW	Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
29	rw	TM10_RST2_SW	2nd Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
28	rw	TM10_RST_SW	Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
27..26	-	Reserved	Reserved	0x00
25	rw	TM10_TRGO_INV	Timer TRGO output inverse enable bit. 0 = Disable 1 = Enable	0x00
24	rw	TM10_TRGO_SW	Timer TRGO software control data bit. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
23..22	rw	TM10_UEV_SEL	Timer UEV output select bits for TM10_TRGO. When TM10_TRGO_MDS selects UEV as output signal, this bit uses to select output pulse function from Main timer overflow and/or underflow. These bits are no effect when TM10_TRGO_MDS does not select UEV as output. 0x0 = All : output all UEV pulses 0x1 = TOF : output timer overflow pulses 0x2 = UDF : output timer underflow pulses 0x3 = Reserved	0x00
21..16	-	Reserved	Reserved	0x00
15..12	rw	TM10_TRGO_MDS	Timer trigger output mode select 0x0 = RST : TM10_RST (Main Timer Reset) 0x1 = EN : TM10_EN (Main Timer Enable) 0x2 = UEV : TM10_UEV (Main Timer Update event) 0x3 = TOF : TM10_TOF (Main Timer overflow) 0x4 = Reserved 0x5 = EN2 : TM10_EN2 (Timer-2 Enable) 0x6 = TOF2 :TM10_TOF2 (Timer-2 overflow) 0x7 = Reserved 0x8 = UEV2 : TM10_UEV2 (Timer-2 Update event) 0x9 = SW : TM10_TRGO_SW (software control bit) 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = Reserved 0xE = TRGI : TM10_TRGI (internal TRGI signal) 0xF = Reserved	0x00
11	-	Reserved	Reserved	0x00
10..8	rw	TM10_ITR_MUX	Timer internal trigger source select. See the [Timer Internal	0x00

			Trigger and Channel Input Signals Table] for more information. 0x0 = ITR0 (TM10_ITR0) 0x1 = ITR1 (TM10_ITR1) 0x2 = ITR2 (TM10_ITR2) 0x3 = ITR3 (TM10_ITR3) 0x4 = ITR4 (TM10_ITR4) 0x5 = ITR5 (TM10_ITR5) 0x6 = ITR6 (TM10_ITR6) 0x7 = ITR7 (TM10_ITR7)	
7..6	rw	TM10_TRG_MUX	Timer trigger source TRGI select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = Reserved 0x3 = Reserved	0x00
5..3	rw	TM10_TRGI2_MDS	2nd Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00
2..0	rw	TM10_TRGI_MDS	Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00

1.30.5. TM10 Timer control register 0

TM10_CR0	TM10 Timer control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM10_UEX_EN	TM10_USW_EN	Reserved	TM10_UEV_DIS	TM10_EX_INV	TM10_EX_EN	TM10_ACLEAR_EN	TM10_ASTOP_EN
7	6	5	4	3	2	1	0
TM10_DIR2	Reserved	TM10_MDS[1:0]		Reserved	Reserved	TM10_EN2	TM10_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	TM10_UEX_EN	Timer external trigger update event enable. 0 = Disable 1 = Enable	0x00
14	rw	TM10_USW_EN	Timer software update event generation enable. (automatically clear by hardware) 0 = Disable 1 = Enable	0x00
13	-	Reserved	Reserved	0x00
12	rw	TM10_UEV_DIS	Update event generation disable for main Timer. Update event is generation from counter overflow/underflow or software register forced bit.	0x00

			0 = Enable 1 = Disable	
11	rw	TM10_EX_INV	Timer external trigger input inverted enable. 0 = Normal 1 = Inverted	0x00
10	rw	TM10_EX_EN	Timer external trigger event enable. 0 = Disable 1 = Enable	0x00
9	rw	TM10_ACLEAR_EN	Timer overflow or underflow flag auto-clear enable. This bit is no effect if TMx_ASTOP_EN is disabled. When enables, the timer will auto clear the flag of TMx_TOF or TMx_TUF after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
8	rw	TM10_ASTOP_EN	Timer auto stop mode enable. When enables, the timer will auto stop after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
7	rw	TM10_DIR2	2nd Timer counting direction bit. 0 = Up (Up Counting) 1 = Down (Down Counting)	0x00
6	-	Reserved	Reserved	0x00
5..4	rw	TM10_MDS	Timer operation mode select. When selects 'Cascade', both TMx_EN and TMx_EN2 must set the same setting of Enable or Disable. (x : module index) 0x0 = Cascade : 16-bit counter with 16-bit prescaler Mode 0x1 = Separate : Separated two 16-bit counters Mode 0x2 = Full-Counter : 32-bit counter Mode 0x3 = Reserved	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	rw	TM10_EN2	2nd Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00
0	rw	TM10_EN	Main Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00

1.30.6. TM10 Timer CKO control register

TM10_CKO	TM10 Timer CKO control register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				TM10_CKO_LCK	TM10_CKO_STA	TM10_CKO_SEL	TM10_CKO_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	TM10_CKO_LCK	TM10_CKO_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked (enable chip hardware control)	0x00

			1 = Un-Locked (disable chip hardware control)	
2	rw	TM10_CKO_STA	Timer CKO output signal initial state. The bit is written effectively only by written 1 to TM10_CKO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
1	rw	TM10_CKO_SEL	Timer overflow as CKO output source select. 0 = 2nd : 2nd Timer overflow 1 = Main : Main Timer overflow	0x00
0	rw	TM10_CKO_EN	Timer overflow as CKO output enable. 0 = Disable 1 = Enable	0x00

1.30.7. TM10 Timer main counter register

TM10_CNT	TM10 Timer main counter register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM10_CNT[15:8]							
7	6	5	4	3	2	1	0
TM10_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM10_CNT	Main timer/counter register.	0x0000

1.30.8. TM10 Timer main counter auto-reload value register

TM10_ARR	TM10 Timer main counter auto-reload value register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM10_ARR[15:8]							
7	6	5	4	3	2	1	0
TM10_ARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM10_ARR	Main timer/counter auto-reload value register	0x0000

1.30.9. TM10 Timer prescaler register

TM10_PSCNT	TM10 Timer prescaler register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
TM10_CNTA[15:8]							
23	22	21	20	19	18	17	16
TM10_CNTA[7:0]							
15	14	13	12	11	10	9	8

TM10_PSCNT[15:8]							
7	6	5	4	3	2	1	0
TM10_PSCNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	r	TM10_CNTA	Main timer/counter alias register. This register is the alias of TM10_CNT for read only.	0x0000
15..0	rw	TM10_PSCNT	Timer prescaler or 2nd timer/counter register	0x0000

1.30.10. TM10 Timer prescaler auto-reload register

TM10_PSARR	TM10 Timer prescaler auto-reload register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM10_PSARR[15:8]							
7	6	5	4	3	2	1	0
TM10_PSARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM10_PSARR	Timer prescaler or 2nd timer/counter auto-reload value register	0x0000

1.30.11. TM10 Register Map

TM10 Register Map Register Number = 10

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	TM10_STA	Reserved																Reserved								TM10_TUF2	Reserved	TM10_TOF2	TM10_TOF	TM10_EXF	Reserved		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	TM10_INT	Reserved																Reserved								Reserved		TM10_TIE2	TM10_TIE	TM10_EXIE	Reserved		TM10_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	TM10_CLK	Reserved								Reserved								Reserved		TM10_CKI_DIV [1:0]		Reserved		TM10_CKI_SEL [1:0]		TM10_CKS2_SEL	TM10_CKS_SEL	TM10_CKE_SEL [1:0]		Reserved			
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	TM10_TRG	TM10_GT2_SW	TM10_GT_SW	TM10_RST2_SW	TM10_RST_SW	Reserved		TM10_TRGO_INV	TM10_TRGO_SW	TM10_UEV_SEL [1:0]		Reserved						TM10_TRGO_MDS [3:0]				Reserved	TM10_ITR_MUX [2:0]			TM10_TRG_MUX [1:0]		TM10_TRGI2_MDS [2:0]			TM10_TRGI_MDS [2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	TM10_CR0	Reserved																TM10_UEX_EN	TM10_USW_EN	Reserved	TM10_UEV_DIS	TM10_EX_INV	TM10_EX_EN	TM10_ACLEAR_EN	TM10_ASTOP_EN	TM10_DIR2	Reserved	TM10_MDS[1:0]		Reserved	Reserved	TM10_EN2	TM10_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	TM10_CKO	Reserved																Reserved								Reserved				TM10_CKO_LCK	TM10_CKO_STA	TM10_CKO_SEL	TM10_CKO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	TM10_CNT	Reserved																TM10_CNT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	TM10_ARR	Reserved																TM10_ARR[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x28	TM10_PSCNT	TM10_CNTA[15:0]																TM10_PSCNT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	TM10_PSARR	Reserved																TM10_PSARR[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.31. Timer16 Control Registers

Timer16 Control	(TM16) Timer Control Module-16
Base Address :	0x55860000

1.31.1. TM16 Timer status register

TM16_STA	TM16 Timer status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM16_TUF2	TM16_TUF	TM16_TOF2	TM16_TOF	TM16_EXF	Reserved		TM16_DIRF

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	rw	TM16_TUF2	2nd Timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	rw	TM16_TUF	Main Timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	rw	TM16_TOF2	2nd Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	TM16_TOF	Main Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	TM16_EXF	Timer external trigger flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2..1	-	Reserved	Reserved	0x00
0	r	TM16_DIRF	Main Timer up/down counting flag. 0 = Up counting 1 = Down counting	0x00

1.31.2. TM16 Timer interrupt enable register

TM16_INT	TM16 Timer interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		TM16_TIE2	TM16_TIE	TM16_EXIE	Reserved		TM16_IEA

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	TM16_TIE2	2nd Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	TM16_TIE	Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	TM16_EXIE	Timer external trigger interrupt enable. 0 = Disable 1 = Enable	0x00
2..1	-	Reserved	Reserved	0x00
0	rw	TM16_IEA	Timer interrupt all enable. When disables, the timer global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.31.3. TM16 Timer clock source register

TM16_CLK	TM16 Timer clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved		TM16_CKI_DIV[1:0]		Reserved		TM16_CKI_SEL[1:0]	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TM16_CKS2_SEL	TM16_CKS_SEL	TM16_CKE_SEL[1:0]		Reserved			

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13..12	rw	TM16_CKI_DIV	Timer internal clock CK_TM16_INT input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
11..10	-	Reserved	Reserved	0x00
9..8	rw	TM16_CKI_SEL	Timer input clock CK_TM16 source select. 0x0 = PROC : CK_TM16_PR process clock from CSC 0x1 = Reserved 0x2 = CK_LS 0x3 = Reserved	0x00
7	rw	TM16_CKS2_SEL	Counter/Timer CK_TC2 clock source select. 0 = CK_INT 1 = CK_EXT	0x00
6	rw	TM16_CKS_SEL	Counter/Timer CK_TC clock source select. 0 = CK_INT 1 = CK_EXT	0x00
5..4	rw	TM16_CKE_SEL	Timer internal clock CK_EXT source select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = Reserved 0x3 = Reserved	0x00

3..0	-	Reserved	Reserved	0x00

1.31.4. TM16 Timer trigger control register

TM16_TRG	TM16 Timer trigger control register
Offset Address : 0x0C	Reset Value : 0x00000000

31	30	29	28	27	26	25	24
TM16_GT2_SW	TM16_GT_SW	TM16_RST2_SW	TM16_RST_SW	Reserved		TM16_TRGO_INV	TM16_TRGO_SW
23	22	21	20	19	18	17	16
TM16_UEV_SEL[1:0]		Reserved					
15	14	13	12	11	10	9	8
TM16_TRGO_MDS[3:0]				Reserved	TM16_ITR_MUX[2:0]		
7	6	5	4	3	2	1	0
TM16_TRG_MUX[1:0]		TM16_TRGI2_MDS[2:0]			TM16_TRGI_MDS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31	rw	TM16_GT2_SW	2nd Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
30	rw	TM16_GT_SW	Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
29	rw	TM16_RST2_SW	2nd Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
28	rw	TM16_RST_SW	Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
27..26	-	Reserved	Reserved	0x00
25	rw	TM16_TRGO_INV	Timer TRGO output inverse enable bit. 0 = Disable 1 = Enable	0x00
24	rw	TM16_TRGO_SW	Timer TRGO software control data bit. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
23..22	rw	TM16_UEV_SEL	Timer UEV output select bits for TM16_TRGO. When TM16_TRGO_MDS selects UEV as output signal, this bit uses to select output pulse function from Main timer overflow and/or underflow. These bits are no effect when TM16_TRGO_MDS does not select UEV as output. 0x0 = All : output all UEV pulses 0x1 = TOF : output timer overflow pulses 0x2 = UDF : output timer underflow pulses 0x3 = Reserved	0x00
21..16	-	Reserved	Reserved	0x00
15..12	rw	TM16_TRGO_MDS	Timer trigger output mode select 0x0 = RST : TM16_RST (Main Timer Reset) 0x1 = EN : TM16_EN (Main Timer Enable) 0x2 = UEV : TM16_UEV (Main Timer Update event) 0x3 = TOF : TM16_TOF (Main Timer overflow) 0x4 = TUF : TM16_TUF (Main Timer underflow) 0x5 = EN2 : TM16_EN2 (Timer-2 Enable) 0x6 = TOF2 :TM16_TOF2 (Timer-2 overflow) 0x7 = DIR : TM16_DIR (Main Timer direction event) 0x8 = UEV2 : TM16_UEV2 (Timer-2 Update event) 0x9 = SW : TM16_TRGO_SW (software control bit) 0xA = Reserved 0xB = Reserved 0xC = Reserved	0x00

			0xD = Reserved 0xE = TRGI : TM16_TRGI (internal TRGI signal) 0xF = Reserved	
11	-	Reserved	Reserved	0x00
10..8	rw	TM16_ITR_MUX	Timer internal trigger source select. See the [Timer Internal Trigger and Channel Input Signals Table] for more information. 0x0 = ITR0 (TM16_ITR0) 0x1 = ITR1 (TM16_ITR1) 0x2 = ITR2 (TM16_ITR2) 0x3 = ITR3 (TM16_ITR3) 0x4 = ITR4 (TM16_ITR4) 0x5 = ITR5 (TM16_ITR5) 0x6 = ITR6 (TM16_ITR6) 0x7 = ITR7 (TM16_ITR7)	0x00
7..6	rw	TM16_TRG_MUX	Timer trigger source TRGI select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = Reserved 0x3 = Reserved	0x00
5..3	rw	TM16_TRGI2_MDS	2nd Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00
2..0	rw	TM16_TRGI_MDS	Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00

1.31.5. TM16 Timer control register 0

TM16_CR0	TM16 Timer control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM16_UEX_EN	TM16_USW_EN	Reserved	TM16_UEV_DIS	TM16_EX_INV	TM16_EX_EN	TM16_ACLEAR_EN	TM16_ASTOP_EN
7	6	5	4	3	2	1	0
TM16_DIR2	TM16_DIR	TM16_MDS[1:0]		Reserved	Reserved	TM16_EN2	TM16_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	TM16_UEX_EN	Timer external trigger update event enable. 0 = Disable 1 = Enable	0x00
14	rw	TM16_USW_EN	Timer software update event generation enable. (automatically clear by hardware) 0 = Disable	0x00

			1 = Enable	
13	-	Reserved	Reserved	0x00
12	rw	TM16_UEV_DIS	Update event generation disable for main Timer. Update event is generation from counter overflow/underflow or software register forced bit. 0 = Enable 1 = Disable	0x00
11	rw	TM16_EX_INV	Timer external trigger input inverted enable. 0 = Normal 1 = Inverted	0x00
10	rw	TM16_EX_EN	Timer external trigger event enable. 0 = Disable 1 = Enable	0x00
9	rw	TM16_ACLEAR_EN	Timer overflow or underflow flag auto-clear enable. This bit is no effect if TMx_ASTOP_EN is disabled. When enables, the timer will auto clear the flag of TMx_TOF or TMx_TUF after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
8	rw	TM16_ASTOP_EN	Timer auto stop mode enable. When enables, the timer will auto stop after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
7	rw	TM16_DIR2	2nd Timer counting direction bit. 0 = Up (Up Counting) 1 = Down (Down Counting)	0x00
6	rw	TM16_DIR	Main Timer counting direction bit. 0 = Up (Up Counting) 1 = Down (Down Counting)	0x00
5..4	rw	TM16_MDS	Timer operation mode select. When selects 'Cascade', both TMx_EN and TMx_EN2 must set the same setting of Enable or Disable. (x : module index) 0x0 = Cascade : 16-bit counter with 16-bit prescaler Mode 0x1 = Separate : Separated two 16-bit counters Mode 0x2 = Full-Counter : 32-bit counter Mode 0x3 = Reserved	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	rw	TM16_EN2	2nd Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00
0	rw	TM16_EN	Main Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00

1.31.6. TM16 Timer CKO control register

TM16_CKO	TM16 Timer CKO control register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				TM16_CKO_LCK	TM16_CKO_STA	TM16_CKO_SEL	TM16_CKO_EN

Bit	Attr	Bit Name	Description	Reset

31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	TM16_CKO_LCK	TM16_CKO_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
2	rw	TM16_CKO_STA	Timer CKO output signal initial state. The bit is written effectively only by written 1 to TM16_CKO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
1	rw	TM16_CKO_SEL	Timer overflow as CKO output source select. 0 = 2nd : 2nd Timer overflow 1 = Main : Main Timer overflow	0x00
0	rw	TM16_CKO_EN	Timer overflow as CKO output enable. 0 = Disable 1 = Enable	0x00

1.31.7. TM16 Timer main counter register

TM16_CNT	TM16 Timer main counter register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM16_CNT[15:8]							
7	6	5	4	3	2	1	0
TM16_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM16_CNT	Main timer/counter register.	0x0000

1.31.8. TM16 Timer main counter auto-reload value register

TM16_ARR	TM16 Timer main counter auto-reload value register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM16_ARR[15:8]							
7	6	5	4	3	2	1	0
TM16_ARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM16_ARR	Main timer/counter auto-reload value register	0x0000

1.31.9. TM16 Timer prescaler register

TM16_PSCNT	TM16 Timer prescaler register

Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
TM16_CNTA[15:8]							
23	22	21	20	19	18	17	16
TM16_CNTA[7:0]							
15	14	13	12	11	10	9	8
TM16_PSCNT[15:8]							
7	6	5	4	3	2	1	0
TM16_PSCNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	r	TM16_CNTA	Main timer/counter alias register. This register is the alias of TM16_CNT for read only.	0x0000
15..0	rw	TM16_PSCNT	Timer prescaler or 2nd timer/counter register	0x0000

1.31.10. TM16 Timer prescaler auto-reload register

TM16_PSARR	TM16 Timer prescaler auto-reload register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM16_PSARR[15:8]							
7	6	5	4	3	2	1	0
TM16_PSARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM16_PSARR	Timer prescaler or 2nd timer/counter auto-reload value register	0x0000

1.31.11. TM16 Register Map

TM16 Register Map Register Number = 10

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	TM16_STA	Reserved																Reserved								TM16_TUF2	TM16_TUF	TM16_TOF2	TM16_TOF	TM16_EXF	Reserved		TM16_DIRF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	TM16_INT	Reserved																Reserved								Reserved		TM16_TIE2	TM16_TIE	TM16_EXIE	Reserved		TM16_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	TM16_CLK	Reserved								Reserved								Reserved		TM16_CKI_DIV [1:0]		Reserved		TM16_CKI_SEL [1:0]		TM16_CKS2_SEL	TM16_CKS_SEL	TM16_CKE_SEL [1:0]		Reserved			
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	TM16_TRG	TM16_GT2_SW	TM16_GT_SW	TM16_RST2_SW	TM16_RST_SW	Reserved		TM16_TRGO_INV	TM16_TRGO_SW	TM16_UEV_SEL [1:0]		Reserved						TM16_TRGO_MDS [3:0]				Reserved	TM16_ITR_MUX [2:0]			TM16_TRG_MUX [1:0]		TM16_TRGI2_MDS [2:0]			TM16_TRGI_MDS [2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	TM16_CR0	Reserved																TM16_UEX_EN	TM16_USW_EN	Reserved	TM16_UEV_DIS	TM16_EX_INV	TM16_EX_EN	TM16_ACLEAR_EN	TM16_ASTOP_EN	TM16_DIR2	TM16_DIR	TM16_MDS[1:0]		Reserved	Reserved	TM16_EN2	TM16_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	TM16_CKO	Reserved																Reserved								Reserved				TM16_CKO_LCK	TM16_CKO_STA	TM16_CKO_SEL	TM16_CKO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	TM16_CNT	Reserved																TM16_CNT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	TM16_ARR	Reserved																TM16_ARR[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x28	TM16_PSCNT	TM16_CNTA[15:0]																TM16_PSCNT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	TM16_PSARR	Reserved																TM16_PSARR[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.32. Timer20 Control Registers

Timer20 Control	(TM20) Timer Control Module-20
Base Address :	0x56000000

1.32.1. TM20 Timer status register

TM20_STA	TM20 Timer status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			TM20_RTUF	Reserved	Reserved	Reserved	Reserved
15	14	13	12	11	10	9	8
Reserved		TM20_CF1B	TM20_CF0B	Reserved		TM20_CF1A	TM20_CF0A
7	6	5	4	3	2	1	0
TM20_TUF2	Reserved	TM20_TOF2	TM20_TOF	TM20_EXF	Reserved		Reserved

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..21	-	Reserved	Reserved	0x00
20	rw	TM20_RTUF	Repetition timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19	-	Reserved	Reserved	0x00
18	-	Reserved	Reserved	0x00
17	-	Reserved	Reserved	0x00
16	-	Reserved	Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13	rw	TM20_CF1B	Timer IC1 falling edge flag/OC1 event sub flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of TM20_CF0B. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
12	rw	TM20_CF0B	Timer IC0 falling edge flag/OC0 event sub flag. (set by hardware and clear by software writing 1) [Capture Mode]: Input capture event sub flag for single edge mode or input capture falling edge event flag for dual edge mode. [16-bit Compare/PWM Mode]: When center-alignment PWM mode, this bit is used as down counting PWM compare flag. It is no using for other 16-bit comparator mode. [8-bit Compare/PWM Mode]: (1) When compare-L is PWM and center-alignment mode, this bit is used as down counting PWM compare-L flag. (2) Others, this bit is used as compare-H event flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
11..10	-	Reserved	Reserved	0x00
9	rw	TM20_CF1A	Timer IC1 rising edge flag/OC1 event main flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of TM20_CF0A. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
8	rw	TM20_CF0A	Timer IC0 rising edge flag/OC0 event main flag. (set by hardware and clear by software writing 1) [Capture Mode]: Input capture event main flag for single edge mode or input capture rising edge event flag for dual edge mode.	0x00

			[16-bit Compare/PWM Mode]: Output compare event flag for 16-bit comparator mode. When center-alignment PWM mode, this bit is used as up counting PWM compare flag. [8-bit Compare/PWM Mode]: Output compare-L event flag. When compare-L is PWM and center-alignment mode, this bit is used as up counting PWM compare-L flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	
7	rw	TM20_TUF2	2nd Timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	-	Reserved	Reserved	0x00
5	rw	TM20_TOF2	2nd Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	TM20_TOF	Main Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	TM20_EXF	Timer external trigger flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2..1	-	Reserved	Reserved	0x00
0	-	Reserved	Reserved	0x00

1.32.2. TM20 Timer interrupt enable register

TM20_INT	TM20 Timer interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			TM20_RTU_IE	Reserved	Reserved	Reserved	Reserved
15	14	13	12	11	10	9	8
Reserved						TM20_CC1_IE	TM20_CC0_IE
7	6	5	4	3	2	1	0
Reserved		TM20_TIE2	TM20_TIE	TM20_EXIE	Reserved		TM20_IEA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..21	-	Reserved	Reserved	0x00
20	rw	TM20_RTU_IE	Repetition timer underflow interrupt enable. 0 = Disable 1 = Enable	0x00
19	-	Reserved	Reserved	0x00
18	-	Reserved	Reserved	0x00
17	-	Reserved	Reserved	0x00
16	-	Reserved	Reserved	0x00
15..10	-	Reserved	Reserved	0x00
9	rw	TM20_CC1_IE	Timer IC1/OC1 interrupt enable. 0 = Disable 1 = Enable	0x00
8	rw	TM20_CC0_IE	Timer IC0/OC0 interrupt enable. 0 = Disable 1 = Enable	0x00
7..6	-	Reserved	Reserved	0x00

5	rw	TM20_TIE2	2nd Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	TM20_TIE	Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	TM20_EXIE	Timer external trigger interrupt enable. 0 = Disable 1 = Enable	0x00
2..1	-	Reserved	Reserved	0x00
0	rw	TM20_IEA	Timer interrupt all enable. When disables, the timer global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.32.3. TM20 Timer clock source register

TM20_CLK	TM20 Timer clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved			TM20_RC_CKS	Reserved			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved		TM20_CKI_DIV[1:0]		Reserved		TM20_CKI_SEL[1:0]	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TM20_CKS2_SEL	TM20_CKS_SEL	TM20_CKE_SEL[1:0]		Reserved			

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..21	-	Reserved	Reserved	0x00
20	rw	TM20_RC_CKS	Repetition Timer/Counter clock source select. 0 = MAIN : clock input from Main timer overflow/underflow 1 = CKO : clock input from CK_CKOM	0x00
19..16	-	Reserved	Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13..12	rw	TM20_CKI_DIV	Timer internal clock CK_TM20_INT input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
11..10	-	Reserved	Reserved	0x00
9..8	rw	TM20_CKI_SEL	Timer input clock CK_TM20 source select. 0x0 = PROC : CK_TM20_PR process clock from CSC 0x1 = Reserved 0x2 = CK_LS 0x3 = Reserved	0x00
7	rw	TM20_CKS2_SEL	Counter/Timer CK_TC2 clock source select. 0 = CK_INT 1 = CK_EXT	0x00
6	rw	TM20_CKS_SEL	Counter/Timer CK_TC clock source select. 0 = CK_INT 1 = CK_EXT	0x00
5..4	rw	TM20_CKE_SEL	Timer internal clock CK_EXT source select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = IN0 (TM20_IN0) 0x3 = IN1 (TM20_IN1)	0x00

3..0	-	Reserved	Reserved	0x00

1.32.4. TM20 Timer trigger control register

TM20_TRG	TM20 Timer trigger control register		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
TM20_GT2_SW	TM20_GT_SW	TM20_RST2_SW	TM20_RST_SW	Reserved		TM20_TRGO_INV	TM20_TRGO_SW
23	22	21	20	19	18	17	16
TM20_UEV_SEL[1:0]		Reserved		Reserved	Reserved		
15	14	13	12	11	10	9	8
TM20_TRGO_MDS[3:0]				Reserved	TM20_ITR_MUX[2:0]		
7	6	5	4	3	2	1	0
TM20_TRG_MUX[1:0]		TM20_TRGI2_MDS[2:0]			TM20_TRGI_MDS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31	rw	TM20_GT2_SW	2nd Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
30	rw	TM20_GT_SW	Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
29	rw	TM20_RST2_SW	2nd Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
28	rw	TM20_RST_SW	Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
27..26	-	Reserved	Reserved	0x00
25	rw	TM20_TRGO_INV	Timer TRGO output inverse enable bit. 0 = Disable 1 = Enable	0x00
24	rw	TM20_TRGO_SW	Timer TRGO software control data bit. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
23..22	rw	TM20_UEV_SEL	Timer UEV output select bits for TM20_TRGO. When TM20_TRGO_MDS selects UEV as output signal, this bit uses to select output pulse function from Main timer overflow and/or underflow. These bits are no effect when TM20_TRGO_MDS does not select UEV as output. 0x0 = All : output all UEV pulses 0x1 = TOF : output timer overflow pulses 0x2 = UDF : output timer underflow pulses 0x3 = Reserved	0x00
21..20	-	Reserved	Reserved	0x00
19	-	Reserved	Reserved	0x00
18..16	-	Reserved	Reserved	0x00
15..12	rw	TM20_TRGO_MDS	Timer trigger output mode select 0x0 = RST : TM20_RST (Main Timer Reset) 0x1 = EN : TM20_EN (Main Timer Enable) 0x2 = UEV : TM20_UEV (Main Timer Update event) 0x3 = TOF : TM20_TOF (Main Timer overflow) 0x4 = Reserved 0x5 = EN2 : TM20_EN2 (Timer-2 Enable) 0x6 = TOF2 :TM20_TOF2 (Timer-2 overflow) 0x7 = Reserved 0x8 = UEV2 : TM20_UEV2 (Timer-2 Update event) 0x9 = SW : TM20_TRGO_SW (software control bit) 0xA = OS0 : TM20_OS0 (channel-0 output state signal)	0x00

			0xB = OS1 : TM20_OS1 (channel-1 output state signal) 0xC = Reserved 0xD = Reserved 0xE = TRGI : TM20_TRGI (internal TRGI signal) 0xF = POE : TM20_POE (Output enable register preload signal)	
11	-	**Reserved**	Reserved	0x00
10..8	rw	**TM20_ITR_MUX**	Timer internal trigger source select. See the [Timer Internal Trigger and Channel Input Signals Table] for more information. 0x0 = ITR0 (TM20_ITR0) 0x1 = ITR1 (TM20_ITR1) 0x2 = ITR2 (TM20_ITR2) 0x3 = ITR3 (TM20_ITR3) 0x4 = ITR4 (TM20_ITR4) 0x5 = ITR5 (TM20_ITR5) 0x6 = ITR6 (TM20_ITR6) 0x7 = ITR7 (TM20_ITR7)	0x00
7..6	rw	**TM20_TRG_MUX**	Timer trigger source TRGI select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = IN0 (TM20_IN0) 0x3 = IN1 (TM20_IN1)	0x00
5..3	rw	**TM20_TRGI2_MDS**	2nd Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00
2..0	rw	**TM20_TRGI_MDS**	Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00

1.32.5. TM20 Timer control register 0

TM20_CR0	TM20 Timer control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						TM20_RC_STP	TM20_RC_EN
15	14	13	12	11	10	9	8
TM20_UEX_EN	TM20_USW_EN	Reserved	TM20_UEV_DIS	TM20_EX_INV	TM20_EX_EN	TM20_ACLEAR_EN	TM20_ASTOP_EN
7	6	5	4	3	2	1	0
TM20_DIR2	Reserved	TM20_MDS[1:0]		Reserved	Reserved	TM20_EN2	TM20_EN

Bit	Attr	Bit Name	Description	Reset
31..24	-	**Reserved**	Reserved	0x00
23..18	-	**Reserved**	Reserved	0x00
17	rw	**TM20_RC_STP**	Main Counter stop enable when repetition counter underflow. 0 = Disable	0x00

			1 = Enable	
16	rw	TM20_RC_EN	Repetition Counter enable bit. 0 = Disable 1 = Enable	0x00
15	rw	TM20_UEX_EN	Timer external trigger update event enable. 0 = Disable 1 = Enable	0x00
14	rw	TM20_USW_EN	Timer software update event generation enable. (automatically clear by hardware) 0 = Disable 1 = Enable	0x00
13	-	Reserved	Reserved	0x00
12	rw	TM20_UEV_DIS	Update event generation disable for main Timer. Update event is generation from counter overflow/underflow or software register forced bit. 0 = Enable 1 = Disable	0x00
11	rw	TM20_EX_INV	Timer external trigger input inverted enable. 0 = Normal 1 = Inverted	0x00
10	rw	TM20_EX_EN	Timer external trigger event enable. 0 = Disable 1 = Enable	0x00
9	rw	TM20_ACLEAR_EN	Timer overflow or underflow flag auto-clear enable. This bit is no effect if TMx_ASTOP_EN is disabled. When enables, the timer will auto clear the flag of TMx_TOF or TMx_TUF after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
8	rw	TM20_ASTOP_EN	Timer auto stop mode enable. When enables, the timer will auto stop after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
7	rw	TM20_DIR2	2nd Timer counting direction bit. 0 = Up (Up Counting) 1 = Down (Down Counting)	0x00
6	-	Reserved	Reserved	0x00
5..4	rw	TM20_MDS	Timer operation mode select. When selects 'Cascade', both TMx_EN and TMx_EN2 must set the same setting of Enable or Disable. (x : module index) 0x0 = Cascade : 16-bit counter with 16-bit prescaler Mode 0x1 = Separate : Separated two 16-bit counters Mode 0x2 = Full-Counter : 32-bit counter Mode 0x3 = Reserved	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	rw	TM20_EN2	2nd Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00
0	rw	TM20_EN	Main Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00

1.32.6. TM20 Timer control register 1

TM20_CR1	TM20 Timer control register 1		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		TM20_CC1B_SEN	TM20_CC0B_SEN	Reserved		TM20_CC1A_SEN	TM20_CC0A_SEN
7	6	5	4	3	2	1	0
Reserved						TM20_OVR1_MDS	TM20_OVR0_MDS

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13	rw	TM20_CC1B_SEN	Timer channel 1 software IC/OC event-B generation enable. When capture mode, this bit is used to trigger falling edge capture event. When PWM mode, this bit is used to set TM20_CF1B flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
12	rw	TM20_CC0B_SEN	Timer channel 0 software IC/OC event-B generation enable. When capture mode, this bit is used to trigger falling edge capture event. When PWM mode, this bit is used to set TM20_CF0B flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
11..10	-	Reserved	Reserved	0x00
9	rw	TM20_CC1A_SEN	Timer channel 1 software IC/OC event-A generation enable. When capture mode, this bit is used to trigger rising edge capture event. When PWM mode, this bit is used to set TM20_CF1A flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
8	rw	TM20_CC0A_SEN	Timer channel 0 software IC/OC event-A generation enable. When capture mode, this bit is used to trigger rising edge capture event. When PWM mode, this bit is used to set TM20_CF0A flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
7..2	-	Reserved	Reserved	0x00
1	rw	TM20_OVR1_MDS	Timer channel 1 capture data buffer overrun mode select 0 = Overwritten (Overwritten by new data) 1 = Keep (Preserved old data)	0x00
0	rw	TM20_OVR0_MDS	Timer channel 0 capture data buffer overrun mode select 0 = Overwritten (Overwritten by new data) 1 = Keep (Preserved old data)	0x00

1.32.7. TM20 Timer CKO control register

TM20_CKO	TM20 Timer CKO control register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				TM20_CKO_LCK	TM20_CKO_STA	TM20_CKO_SEL	TM20_CKO_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00

7..4	-	Reserved	Reserved	0x00
3	rw	TM20_CKO_LCK	TM20_CKO_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
2	rw	TM20_CKO_STA	Timer CKO output signal initial state. The bit is written effectively only by written 1 to TM20_CKO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
1	rw	TM20_CKO_SEL	Timer overflow as CKO output source select. 0 = 2nd : 2nd Timer overflow 1 = Main : Main Timer overflow	0x00
0	rw	TM20_CKO_EN	Timer overflow as CKO output enable. 0 = Disable 1 = Enable	0x00

1.32.8. TM20 repetition counter register

TM20_RCNT	TM20 repetition counter register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
TM20_RARR[7:0]							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM20_RCNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	rw	TM20_RARR	Repetition counter auto-reload value register. This register is used to set the main timer overflow / underflow number or TMx_CKOM pulse number which is as the next updated auto-reload value after the Repetition counter is underflow. When the Repetition counter has been started and counting underflow, the chip will be asserting a RTUF flag.	0x00
15..8	-	Reserved	Reserved	0x00
7..0	rw	TM20_RCNT	Repetition counter register.	0x00

1.32.9. TM20 Timer main counter register

TM20_CNT	TM20 Timer main counter register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM20_CNT[15:8]							
7	6	5	4	3	2	1	0
TM20_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000

15..0	rw	TM20_CNT	Main timer/counter register.	0x0000

1.32.10. TM20 Timer main counter auto-reload value register

TM20_ARR	TM20 Timer main counter auto-reload value register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM20_ARR[15:8]							
7	6	5	4	3	2	1	0
TM20_ARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM20_ARR	Main timer/counter auto-reload value register. [Two 8bit OC/PWM Mode] for all channels: This register value is limited to 0x00ZZ (ZZ={0x00~0xFF}) [Two 8bit OC/PWM,16bit OC/PWM Mode] for mixed channels: This register value is limited to 0xZZFF (ZZ={0x00~0xFF})	0x0000

1.32.11. TM20 Timer prescaler register

TM20_PSCNT	TM20 Timer prescaler register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
TM20_CNTA[15:8]							
23	22	21	20	19	18	17	16
TM20_CNTA[7:0]							
15	14	13	12	11	10	9	8
TM20_PSCNT[15:8]							
7	6	5	4	3	2	1	0
TM20_PSCNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	r	TM20_CNTA	Main timer/counter alias register. This register is the alias of TM20_CNT for read only.	0x0000
15..0	rw	TM20_PSCNT	Timer prescaler or 2nd timer/counter register	0x0000

1.32.12. TM20 Timer prescaler auto-reload register

TM20_PSARR	TM20 Timer prescaler auto-reload register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM20_PSARR[15:8]							
7	6	5	4	3	2	1	0
TM20_PSARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000

15..0	rw	TM20_PSARR	Timer prescaler or 2nd timer/counter auto-reload value register	0x0000

1.32.13. TM20 Timer capture and compare mode select register

TM20_CCMDS	TM20 Timer capture and compare mode select register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							TM20_OC_LCK
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	TM20_CC1_MDS[2:0]			Reserved	TM20_CC0_MDS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	TM20_OC_LCK	Timer output compare reload function lock enable bit for all channel. When enables and timer update event is happened, it is locked that the compare preload registers of TM20_CCnB reload to compare shadow buffer registers of TM20_CCnA. Until this bit is disabled, these compare preload registers will update the compare shadow buffer at next timer update event happened. 0 = un-Locked : enable unlocked 1 = Locked : enable locked	0x00
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6..4	rw	TM20_CC1_MDS	Timer channel 1 capture and compare mode select. 0x0 = NOP (No operation) 0x1 = 16bit_IC (Input capture) 0x2 = 16bit_OC (Output compare) 0x3 = 8bitx2_OC (Two 8-bit compare) 0x4 = 16bit_PWM (16bit PWM) 0x5 = 8bitx2_PWM (Two 8bit PWMs) 0x6 = Reserved 0x7 = Reserved	0x00
3	-	Reserved	Reserved	0x00
2..0	rw	TM20_CC0_MDS	Timer channel 0 capture and compare mode select. 0x0 = NOP (No operation) 0x1 = 16bit_IC (Input capture) 0x2 = 16bit_OC (Output compare) 0x3 = 8bitx2_OC (Two 8-bit compare) 0x4 = 16bit_PWM (16bit PWM) 0x5 = 8bitx2_PWM (Two 8bit PWMs) 0x6 = Reserved 0x7 = Reserved	0x00

1.32.14. TM20 Timer input capture control register

TM20_ICCR	TM20 Timer input capture control register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved				TM20_IC1_TRGS[1:0]		TM20_IC0_TRGS[1:0]	
15	14	13	12	11	10	9	8

Reserved							
7	6	5	4	3	2	1	0
Reserved		TM20_IC1_MUX[1:0]		Reserved		TM20_IC0_MUX[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..20	-	Reserved	Reserved	0x00
19..18	rw	TM20_IC1_TRGS	Timer channel 1 input trigger edge select. 0x0 = Disable : disable capture data 0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	0x00
17..16	rw	TM20_IC0_TRGS	Timer channel 0 input trigger edge select. 0x0 = Disable : disable capture data 0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	0x00
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5..4	rw	TM20_IC1_MUX	Timer channel 1 input Mux select for input capture. 0x0 = IC10 : TM20_IC1 0x1 = IC11 : TM20_ITR 0x2 = IC12 : CMP1_OUT 0x3 = IC13 : Reserved	0x00
3..2	-	Reserved	Reserved	0x00
1..0	rw	TM20_IC0_MUX	Timer channel 0 input Mux select for input capture. 0x0 = IC00 : TM20_IC0 0x1 = IC01 : TM20_ITR 0x2 = IC02 : CMP0_OUT 0x3 = IC03 : Reserved	0x00

1.32.15. TM20 Timer output compare state register

TM20_OSCR	TM20 Timer output compare state register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		TM20_OS1H_LCK	TM20_OS0H_LCK	Reserved		TM20_OS1H_STA	TM20_OS0H_STA
7	6	5	4	3	2	1	0
Reserved		TM20_OS1_LCK	TM20_OS0_LCK	Reserved		TM20_OS1_STA	TM20_OS0_STA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13	rw	TM20_OS1H_LCK	TM20_OS1H_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access.TM20_OS1H_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
12	rw	TM20_OS0H_LCK	TM20_OS0H_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. TM20_OS0H_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control)	0x00

			1 = Un-Locked (disable chip hardware control)	
11..10	-	Reserved	Reserved	0x00
9	rw	TM20_OS1H_STA	Timer channel 1 OC compare-H output signal initial state for two 8-Bit comparator mode 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
8	rw	TM20_OS0H_STA	Timer channel 0 OC compare-H output signal initial state for two 8-Bit comparator mode. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	TM20_OS1_LCK	TM20_OS1_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. TM20_OS1_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
4	rw	TM20_OS0_LCK	TM20_OS0_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. TM20_OS0_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	TM20_OS1_STA	Timer channel 1 OC compare/compare-L output signal initial state. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
0	rw	TM20_OS0_STA	Timer channel 0 OC compare/compare-L output signal initial state. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00

1.32.16. TM20 Timer output compare control register 0

TM20_OCCR0	TM20 Timer output compare control register 0		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			TM20_OC1N_OE	Reserved			TM20_OC0N_OE
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	TM20_OC1_OE2	TM20_OC1_OE1	TM20_OC1_OE0	Reserved	TM20_OC0_OE2	TM20_OC0_OE1	TM20_OC0_OE0

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..21	-	Reserved	Reserved	0x00
20	rw	TM20_OC1N_OE	Timer channel 1 OC1N (complement) line output enable. 0 = Disable (output by TM20_BK1N_STA setting) 1 = Enable	0x00
19..17	-	Reserved	Reserved	0x00
16	rw	TM20_OC0N_OE	Timer channel 0 OC0N (complement) line output enable. 0 = Disable (output by TM20_BK0N_STA setting) 1 = Enable	0x00
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	rw	TM20_OC1_OE2	Timer channel 1 OC line-2 output enable.	0x00

			0 = Disable (output by TM36_BK1_STA setting) 1 = Enable	
5	rw	TM20_OC1_OE1	Timer channel 1 OC line-1 output enable. 0 = Disable (output by TM20_BK1_STA setting) 1 = Enable	0x00
4	rw	TM20_OC1_OE0	Timer channel 1 OC line-0 output enable. 0 = Disable (output by TM20_BK1_STA setting) 1 = Enable	0x00
3	-	Reserved	Reserved	0x00
2	rw	TM20_OC0_OE2	Timer channel 0 OC line-2 output enable. 0 = Disable (output by TM36_BK0_STA setting) 1 = Enable	0x00
1	rw	TM20_OC0_OE1	Timer channel 0 OC line-1 output enable. 0 = Disable (output by TM20_BK0_STA setting) 1 = Enable	0x00
0	rw	TM20_OC0_OE0	Timer channel 0 OC line-0 output enable. 0 = Disable (output by TM20_BK0_STA setting) 1 = Enable	0x00

1.32.17. TM20 Timer output compare control register 1

TM20_OCCR1	TM20 Timer output compare control register 1		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	TM20_ODLY_SEL	Reserved	TM20_POE_SW	Reserved	TM20_POE_EN2	TM20_POE_EN1	TM20_POE_EN0
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved	TM20_OC1_POE2	TM20_OC1_POE1	TM20_OC1_POE0	Reserved	TM20_OC0_POE2	TM20_OC0_POE1	TM20_OC0_POE0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved						TM20_OC1N_INV	TM20_OC0N_INV
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		TM20_OC1H_INV	TM20_OC0H_INV	Reserved		TM20_OC1_INV	TM20_OC0_INV

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	TM20_ODLY_SEL	Timer output delay mode select. When selects '0Step', channel-0,1 output is normal and no delay. When selects '1Step', channel-0,1 output will delay 0,1 step uint delay time. 0x0 = 0Step 0x1 = 1Step	0x00
29	-	Reserved	Reserved	0x00
28	w	TM20_POE_SW	Timer output enable registers preload software enable bit. Refer the TM20_OCn_POE[2:0] (n={0,1}) registers for the output enable registers detail descriptions. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
27	-	Reserved	Reserved	0x00
26	rw	TM20_POE_EN2	Timer OC preload enable bit for output enable preload register control. This bit is used to enable INT_PD input. 0 = Disable 1 = Enable	0x00
25	rw	TM20_POE_EN1	Timer OC preload enable bit for output enable preload register control. This bit is used to enable INT_PB input. 0 = Disable 1 = Enable	0x00
24	rw	TM20_POE_EN0	Timer OC preload enable bit for output enable preload register control. This bit is used to enable 3-line XOR input from TM36. 0 = Disable 1 = Enable	0x00

23	-	**Reserved**	Reserved	0x00
22	rw	**TM20_OC1_POE2**	Timer channel 1 OC line-2 output enable preload register bit. This bit will load into TM20_OC1_OE2 register when the preload event happened. 0 = Disable 1 = Enable	0x00
21	rw	**TM20_OC1_POE1**	Timer channel 1 OC line-1 output enable preload register bit. This bit will load into TM20_OC0_OE1 register when the preload event happened. 0 = Disable 1 = Enable	0x00
20	rw	**TM20_OC1_POE0**	Timer channel 1 OC line-0 output enable preload register bit. This bit will load into TM20_OC0_OE0 register when the preload event happened. 0 = Disable 1 = Enable	0x00
19	-	**Reserved**	Reserved	0x00
18	rw	**TM20_OC0_POE2**	Timer channel 0 OC line-2 output enable preload register bit. This bit will load into TM20_OC0_OE2 register when the preload event happened. 0 = Disable 1 = Enable	0x00
17	rw	**TM20_OC0_POE1**	Timer channel 0 OC line-0 output enable preload register bit. This bit will load into TM20_OC0_OE1 register when the preload event happened. 0 = Disable 1 = Enable	0x00
16	rw	**TM20_OC0_POE0**	Timer channel 0 OC line-1 output enable preload register bit. This bit will load into TM20_OC0_OE0 register when the preload event happened. 0 = Disable 1 = Enable	0x00
15..10	-	**Reserved**	Reserved	0x00
9	rw	**TM20_OC1N_INV**	Timer channel 1 complement output inverse enable. 0 = Disable 1 = Enable	0x00
8	rw	**TM20_OC0N_INV**	Timer channel 0 complement output inverse enable. 0 = Disable 1 = Enable	0x00
7..6	-	**Reserved**	Reserved	0x00
5	rw	**TM20_OC1H_INV**	Timer channel 1 High output inverse enable. 0 = Disable 1 = Enable	0x00
4	rw	**TM20_OC0H_INV**	Timer channel 0 High output inverse enable. 0 = Disable 1 = Enable	0x00
3..2	-	**Reserved**	Reserved	0x00
1	rw	**TM20_OC1_INV**	Timer channel 1 output inverse enable. 0 = Disable 1 = Enable	0x00
0	rw	**TM20_OC0_INV**	Timer channel 0 output inverse enable. 0 = Disable 1 = Enable	0x00

1.32.18. TM20 Timer PWM and DTG control register

TM20_PWM	**TM20 Timer PWM and DTG control register**		
Offset Address :	**0x44**	**Reset Value :**	**0x00000000**

31	30	29	28	27	26	25	24

Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						TM20_PWM_MDS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..2	-	Reserved	Reserved	0x00
1..0	rw	TM20_PWM_MDS	Timer OC0/1/2/3 PWM mode select. 0x0 = Edge Left-aligned 0x1 = Reserved 0x2 = Reserved 0x3 = Reserved	0x00

1.32.19. TM20 Timer stop control register

TM20_BS	TM20 Timer stop control register		
Offset Address :	0x48	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved		TM20_STP1N_STA	TM20_STP0N_STA	Reserved		TM20_STP1_STA	TM20_STP0_STA
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

Bit	Attr	Bit Name	Description	Reset
31..30	-	Reserved	Reserved	0x00
29	rw	TM20_STP1N_STA	Timer BK input active or stop condition output OC1N state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
28	rw	TM20_STP0N_STA	Timer BK input active or stop condition output OC0N state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
27..26	-	Reserved	Reserved	0x00
25	rw	TM20_STP1_STA	Timer BK input active or stop condition output OC1 state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
24	rw	TM20_STP0_STA	Timer BK input active or stop condition output OC0 state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
23..16	-	Reserved	Reserved	0x00
15..0	-	Reserved	Reserved	0x0000

1.32.20. TM20 Timer capture and compare register 0A

TM20_CC0A	TM20 Timer capture and compare register 0A		
Offset Address :	0x50	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM20_CC0A[15:8]							
7	6	5	4	3	2	1	0
TM20_CC0A[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM20_CC0A	TM20 Timer capture and compare register 0A for channel 0. When the channel is configured as input capture mode, this register is used to capture the counter value of input trigger signal : (1) first capture data for single edge (2) rising edge capture data for dual edge. When the channel is configured as output compare/PWM mode, this register is used as the compared shadow register for Timer output compare and will be copied from R_TM20_CC0B when TM20_CC0B was write. When the channel is configured as output two 8-bit compare/PWM mode, this register is separated to low 8-bt compared shadow register for compare-L path and high 8-bt compared shadow register for compare-H path.	0x0000

1.32.21. TM20 Timer capture and compare register 0B

TM20_CC0B	TM20 Timer capture and compare register 0B		
Offset Address :	0x54	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM20_CC0B[15:8]							
7	6	5	4	3	2	1	0
TM20_CC0B[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM20_CC0B	TM20 Timer capture and compare register 0B for channel 0. When the channel is configured as input capture mode, this register is used to capture the counter value of input trigger signal : (1) 2nd capture data for single edge (2) falling edge capture data for dual edge. When the channel is configured as output compare/PWM mode, this register is used as the compared preload register for software setting and will copy the value to TM20_CC0A. When the channel is configured as output two 8-bit compare/PWM mode, this register is separated to low 8-bt compared preload register for compare-L path and high 8-bt compared preload register for compare-H path.	0x0000

1.32.22. TM20 Timer capture and compare register 1A

TM20_CC1A	TM20 Timer capture and compare register 1A		
Offset Address :	0x58	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16

Reserved							
15	14	13	12	11	10	9	8
TM20_CC1A[15:8]							
7	6	5	4	3	2	1	0
TM20_CC1A[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM20_CC1A	TM20 Timer capture and compare register 1A for channel 1. Refer to the register descriptions of TM20_CC0A for detail descriptions.	0x0000

1.32.23. TM20 Timer capture and compare register 1B

TM20_CC1B	TM20 Timer capture and compare register 1B		
Offset Address :	0x5c	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM20_CC1B[15:8]							
7	6	5	4	3	2	1	0
TM20_CC1B[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM20_CC1B	Timer TM20 capture and compare register 1B for channel 1. Refer to the register descriptions of TM20_CC0B for detail descriptions.	0x0000

1.32.24. TM20 Register Map

TM20 Register Map Register Number = 23

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	TM20_STA	Reserved								Reserved			TM20_RTUF	Reserved	Reserved	Reserved	Reserved	Reserved		TM20_CF1B	TM20_CF0B	Reserved		TM20_CF1A	TM20_CF0A	TM20_TUF2	Reserved	TM20_TOF2	TM20_TOF	TM20_EXF	Reserved		Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	TM20_INT	Reserved								Reserved			TM20_RTU_IE	Reserved	Reserved	Reserved	Reserved	Reserved						TM20_CC1_IE	TM20_CC0_IE	Reserved		TM20_TIE2	TM20_TIE	TM20_EXIE	Reserved		TM20_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	TM20_CLK	Reserved								Reserved			TM20_RC_CKS	Reserved				Reserved		TM20_CKI_DIV [1:0]		Reserved		TM20_CKI_SEL [1:0]		TM20_CKS2_SEL	TM20_CKS_SEL	TM20_CKE_SEL [1:0]		Reserved			
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	TM20_TRG	TM20_GT2_SW	TM20_GT_SW	TM20_RST2_SW	TM20_RST_SW	Reserved		TM20_TRGO_INV	TM20_TRGO_SW	TM20_UEV_SEL [1:0]		Reserved		Reserved	Reserved			TM20_TRGO_MDS [3:0]				Reserved	TM20_ITR_MUX [2:0]			TM20_TRG_MUX [1:0]		TM20_TRGI2_MDS [2:0]			TM20_TRGI_MDS [2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	TM20_CR0	Reserved								Reserved						TM20_RC_STP	TM20_RC_EN	TM20_UEX_EN	TM20_USW_EN	Reserved	TM20_UEV_DIS	TM20_EX_INV	TM20_EX_EN	TM20_ACLEAR_EN	TM20_ASTOP_EN	TM20_DIR2	Reserved	TM20_MDS[1:0]		Reserved	Reserved	TM20_EN2	TM20_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	TM20_CR1	Reserved																Reserved		TM20_CC1B_SEN	TM20_CC0B_SEN	Reserved		TM20_CC1A_SEN	TM20_CC0A_SEN	Reserved						TM20_OVR1_MDS	TM20_OVR0_MDS
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	TM20_CKO	Reserved																Reserved								Reserved				TM20_CKO_LCK	TM20_CKO_STA	TM20_CKO_SEL	TM20_CKO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	TM20_RCNT	Reserved								TM20_RARR[7:0]								Reserved								TM20_RCNT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x20	TM20_CNT	Reserved																TM20_CNT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	TM20_ARR	Reserved																TM20_ARR[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	TM20_PSCNT	TM20_CNTA[15:0]																TM20_PSCNT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	TM20_PSARR	Reserved																TM20_PSARR[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	TM20_CCMDS	Reserved								Reserved							TM20_OC_LCK	Reserved								Reserved	TM20_CC1_MDS [2:0]			Reserved	TM20_CC0_MDS [2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	TM20_ICCR	Reserved								Reserved				TM20_IC1_TRGS [1:0]		TM20_IC0_TRGS [1:0]		Reserved								Reserved		TM20_IC1_MUX [1:0]		Reserved		TM20_IC0_MUX [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	TM20_OSCR	Reserved								Reserved								Reserved		TM20_OS1H_LCK	TM20_OS0H_LCK	Reserved		TM20_OS1H_STA	TM20_OS0H_STA	Reserved		TM20_OS1_LCK	TM20_OS0_LCK	Reserved		TM20_OS1_STA	TM20_OS0_STA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	TM20_OCCR0	Reserved								Reserved			TM20_OC1N_OE	Reserved			TM20_OC0N_OE	Reserved								Reserved	TM20_OC1_OE2	TM20_OC1_OE1	TM20_OC1_OE0	Reserved	TM20_OC0_OE2	TM20_OC0_OE1	TM20_OC0_OE0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	TM20_OCCR1	Reserved	TM20_ODLY_SEL	Reserved	TM20_POE_SW	Reserved	TM20_POE_EN2	TM20_POE_EN1	TM20_POE_EN0	Reserved	TM20_OC1_POE2	TM20_OC1_POE1	TM20_OC1_POE0	Reserved	TM20_OC0_POE2	TM20_OC0_POE1	TM20_OC0_POE0	Reserved						TM20_OC1N_INV	TM20_OC0N_INV	Reserved		TM20_OC1H_INV	TM20_OC0H_INV	Reserved		TM20_OC1_INV	TM20_OC0_INV
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x44	TM20_PWM	Reserved																Reserved								Reserved						TM20_PWM_MDS [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x48	TM20_BS	Reserved		TM20_STP1N_STA	TM20_STP0N_STA	Reserved		TM20_STP1_STA	TM20_STP0_STA	Reserved								Reserved															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	TM20_CC0A	Reserved																TM20_CC0A[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x54	TM20_CC0B	Reserved																TM20_CC0B[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x58	TM20_CC1A	Reserved																TM20_CC1A[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x5c	TM20_CC1B	Reserved																TM20_CC1B[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.33. Timer26 Control Registers

Timer26 Control	(TM26) Timer Control Module-26
Base Address :	0x56060000

1.33.1. TM26 Timer status register

TM26_STA	TM26 Timer status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			TM26_RTUF	TM26_QPEF	TM26_IDXF	Reserved	TM26_DIRCF
15	14	13	12	11	10	9	8
Reserved		TM26_CF1B	TM26_CF0B	Reserved		TM26_CF1A	TM26_CF0A
7	6	5	4	3	2	1	0
TM26_TUF2	TM26_TUF	TM26_TOF2	TM26_TOF	TM26_EXF	Reserved		TM26_DIRF

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..21	-	Reserved	Reserved	0x00
20	rw	TM26_RTUF	Repetition timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19	rw	TM26_QPEF	Main Timer QEI phase state transition error detect flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
18	rw	TM26_IDXF	Main Timer QEI external index signal input active detect and internal timer reset flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	-	Reserved	Reserved	0x00
16	rw	TM26_DIRCF	Main Timer up/down counting direction change flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15..14	-	Reserved	Reserved	0x00
13	rw	TM26_CF1B	Timer IC1 falling edge flag/OC1 event sub flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of TM26_CF0B. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
12	rw	TM26_CF0B	Timer IC0 falling edge flag/OC0 event sub flag. (set by hardware and clear by software writing 1) [Capture Mode]: Input capture event sub flag for single edge mode or input capture falling edge event flag for dual edge mode. [16-bit Compare/PWM Mode]: When center-alignment PWM mode, this bit is used as down counting PWM compare flag. It is no using for other 16-bit comparator mode. [8-bit Compare/PWM Mode]: (1) When compare-L is PWM and center-alignment mode, this bit is used as down counting PWM compare-L flag. (2) Others, this bit is used as compare-H event flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
11..10	-	Reserved	Reserved	0x00
9	rw	TM26_CF1A	Timer IC1 rising edge flag/OC1 event main flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of TM26_CF0A.	0x00

			0 = Normal (No event occurred) 1 = Happened (Event happened)	
8	rw	TM26_CF0A	Timer IC0 rising edge flag/OC0 event main flag. (set by hardware and clear by software writing 1) [Capture Mode]: Input capture event main flag for single edge mode or input capture rising edge event flag for dual edge mode. [16-bit Compare/PWM Mode]: Output compare event flag for 16-bit comparator mode. When center-alignment PWM mode, this bit is used as up counting PWM compare flag. [8-bit Compare/PWM Mode]: Output compare-L event flag. When compare-L is PWM and center-alignment mode, this bit is used as up counting PWM compare-L flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
7	rw	TM26_TUF2	2nd Timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	rw	TM26_TUF	Main Timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	rw	TM26_TOF2	2nd Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	TM26_TOF	Main Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	TM26_EXF	Timer external trigger flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2..1	-	Reserved	Reserved	0x00
0	r	TM26_DIRF	Main Timer up/down counting flag. 0 = Up counting 1 = Down counting	0x00

1.33.2. TM26 Timer interrupt enable register

TM26_INT	TM26 Timer interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			TM26_RTU_IE	TM26_QPE_IE	TM26_IDX_IE	Reserved	TM26_DIRC_IE
15	14	13	12	11	10	9	8
Reserved						TM26_CC1_IE	TM26_CC0_IE
7	6	5	4	3	2	1	0
Reserved		TM26_TIE2	TM26_TIE	TM26_EXIE	Reserved		TM26_IEA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..21	-	Reserved	Reserved	0x00
20	rw	TM26_RTU_IE	Repetition timer underflow interrupt enable. 0 = Disable 1 = Enable	0x00

19	rw	TM26_QPE_IE	Main Timer QEI phase state transition error detect interrupt enable. 0 = Disable 1 = Enable	0x00
18	rw	TM26_IDX_IE	Main Timer QEI external index signal input active detect interrupt enable. 0 = Disable 1 = Enable	0x00
17	-	Reserved	Reserved	0x00
16	rw	TM26_DIRC_IE	Main Timer up/down counting direction change interrupt enable. 0 = Disable 1 = Enable	0x00
15..10	-	Reserved	Reserved	0x00
9	rw	TM26_CC1_IE	Timer IC1/OC1 interrupt enable. 0 = Disable 1 = Enable	0x00
8	rw	TM26_CC0_IE	Timer IC0/OC0 interrupt enable. 0 = Disable 1 = Enable	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	TM26_TIE2	2nd Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	TM26_TIE	Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	TM26_EXIE	Timer external trigger interrupt enable. 0 = Disable 1 = Enable	0x00
2..1	-	Reserved	Reserved	0x00
0	rw	TM26_IEA	Timer interrupt all enable. When disables, the timer global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.33.3. TM26 Timer clock source register

TM26_CLK	TM26 Timer clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			TM26_RC_CKS	Reserved			
15	14	13	12	11	10	9	8
Reserved		TM26_CKI_DIV[1:0]		Reserved		TM26_CKI_SEL[1:0]	
7	6	5	4	3	2	1	0
TM26_CKS2_SEL	TM26_CKS_SEL	TM26_CKE_SEL[1:0]		Reserved			

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..21	-	Reserved	Reserved	0x00
20	rw	TM26_RC_CKS	Repetition Timer/Counter clock source select. 0 = MAIN : clock input from Main timer overflow/underflow 1 = CKO : clock input from CK_CKOM	0x00
19..16	-	Reserved	Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13..12	rw	TM26_CKI_DIV	Timer internal clock CK_TM26_INT input divider.	0x00

			0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	
11..10	-	Reserved	Reserved	0x00
9..8	rw	TM26_CKI_SEL	Timer input clock CK_TM26 source select. 0x0 = PROC : CK_TM26_PR process clock from CSC 0x1 = Reserved 0x2 = CK_LS 0x3 = Reserved	0x00
7	rw	TM26_CKS2_SEL	Counter/Timer CK_TC2 clock source select. 0 = CK_INT 1 = CK_EXT	0x00
6	rw	TM26_CKS_SEL	Counter/Timer CK_TC clock source select. 0 = CK_INT 1 = CK_EXT	0x00
5..4	rw	TM26_CKE_SEL	Timer internal clock CK_EXT source select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = IN0 (TM26_IN0) 0x3 = IN1 (TM26_IN1)	0x00
3..0	-	Reserved	Reserved	0x00

1.33.4. TM26 Timer trigger control register

TM26_TRG	TM26 Timer trigger control register		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
TM26_GT2_SW	TM26_GT_SW	TM26_RST2_SW	TM26_RST_SW	Reserved		TM26_TRGO_INV	TM26_TRGO_SW
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TM26_UEV_SEL[1:0]		TM26_IDX_MDS[1:0]		TM26_IDX_EN	TM26_QEI_MDS[2:0]		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TM26_TRGO_MDS[3:0]				Reserved	TM26_ITR_MUX[2:0]		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TM26_TRG_MUX[1:0]		TM26_TRGI2_MDS[2:0]			TM26_TRGI_MDS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31	rw	TM26_GT2_SW	2nd Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
30	rw	TM26_GT_SW	Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
29	rw	TM26_RST2_SW	2nd Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
28	rw	TM26_RST_SW	Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
27..26	-	Reserved	Reserved	0x00
25	rw	TM26_TRGO_INV	Timer TRGO output inverse enable bit. 0 = Disable 1 = Enable	0x00
24	rw	TM26_TRGO_SW	Timer TRGO software control data bit. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
23..22	rw	TM26_UEV_SEL	Timer UEV output select bits for TM26_TRGO. When TM26_TRGO_MDS selects UEV as output signal, this bit uses to select output pulse function from Main timer overflow and/or	0x00

			underflow. These bits are no effect when TM26_TRGO_MDS does not select UEV as output. 0x0 = All : output all UEV pulses 0x1 = TOF : output timer overflow pulses 0x2 = UDF : output timer underflow pulses 0x3 = Reserved	
21..20	rw	**TM26_IDX_MDS**	Main Timer QEI external index signal input reset timer transition state select. 0x0 = 1T2 : State change between 1 and 2 0x1 = 2T3 : State change between 2 and 3 0x2 = 3T4 : State change between 3 and 4 0x3 = 4T1 : State change between 4 and 1	0x00
19	rw	**TM26_IDX_EN**	Main Timer QEI external index signal input enable. When enables and the index signal will input from TM26_ETR, the timer will reset during up counting or reload the auto-reload value during down counting if detect the index signal active pulse. 0 = Disable 1 = Enable	0x00
18..16	rw	**TM26_QEI_MDS**	Main Timer quadrature encoder interface(QEI) or external input timer up/down control mode select. 0x0 = No operation (up/down control by TM26_DIR) 0x1 = IN0POS : TM26_IN0 positive (high level up count, low level down count) 0x2 = IN0NEG : TM26_IN0 negative (low level up count, high level down count) 0x3 = IN0TRG : TM26_IN0 trigger (edge depending on TM26_IN1 level) 0x4 = IN1TRG : TM26_IN1 trigger (edge depending on TM26_IN0 level) 0x5 = BOTH : Both TM26_IN0 and TM26_IN1 edge	0x00
15..12	rw	**TM26_TRGO_MDS**	Timer trigger output mode select 0x0 = RST : TM26_RST (Main Timer Reset) 0x1 = EN : TM26_EN (Main Timer Enable) 0x2 = UEV : TM26_UEV (Main Timer Update event) 0x3 = TOF : TM26_TOF (Main Timer overflow) 0x4 = TUF : TM26_TUF (Main Timer underflow) 0x5 = EN2 : TM26_EN2 (Timer-2 Enable) 0x6 = TOF2 :TM26_TOF2 (Timer-2 overflow) 0x7 = DIR : TM26_DIR (Main Timer direction event) 0x8 = UEV2 : TM26_UEV2 (Timer-2 Update event) 0x9 = SW : TM26_TRGO_SW (software control bit) 0xA = OS0 : TM26_OS0 (channel-0 output state signal) 0xB = OS1 : TM26_OS1 (channel-1 output state signal) 0xC = Reserved 0xD = Reserved 0xE = TRGI : TM26_TRGI (internal TRGI signal) 0xF = POE : TM26_POE (Output enable register preload signal)	0x00
11	-	**Reserved**	Reserved	0x00
10..8	rw	**TM26_ITR_MUX**	Timer internal trigger source select. See the [Timer Internal Trigger and Channel Input Signals Table] for more information. 0x0 = ITR0 (TM26_ITR0) 0x1 = ITR1 (TM26_ITR1) 0x2 = ITR2 (TM26_ITR2) 0x3 = ITR3 (TM26_ITR3) 0x4 = ITR4 (TM26_ITR4) 0x5 = ITR5 (TM26_ITR5) 0x6 = ITR6 (TM26_ITR6) 0x7 = ITR7 (TM26_ITR7)	0x00
7..6	rw	**TM26_TRG_MUX**	Timer trigger source TRGI select.	0x00

Bit	Attr	Bit Name	Description	Reset
			0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = IN0 (TM26_IN0) 0x3 = IN1 (TM26_IN1)	
5..3	rw	TM26_TRGI2_MDS	2nd Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00
2..0	rw	TM26_TRGI_MDS	Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00

1.33.5. TM26 Timer control register 0

TM26_CR0	TM26 Timer control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						TM26_RC_STP	TM26_RC_EN
15	14	13	12	11	10	9	8
TM26_UEX_EN	TM26_USW_EN	TM26_DIR_INV	TM26_UEV_DIS	TM26_EX_INV	TM26_EX_EN	TM26_ACLEAR_EN	TM26_ASTOP_EN
7	6	5	4	3	2	1	0
TM26_DIR2	TM26_DIR	TM26_MDS[1:0]		Reserved	Reserved	TM26_EN2	TM26_EN

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..18	-	Reserved	Reserved	0x00
17	rw	TM26_RC_STP	Main Counter stop enable when repetition counter underflow. 0 = Disable 1 = Enable	0x00
16	rw	TM26_RC_EN	Repetition Counter enable bit. 0 = Disable 1 = Enable	0x00
15	rw	TM26_UEX_EN	Timer external trigger update event enable. 0 = Disable 1 = Enable	0x00
14	rw	TM26_USW_EN	Timer software update event generation enable. (automatically clear by hardware) 0 = Disable 1 = Enable	0x00
13	rw	TM26_DIR_INV	Main Timer counting direction inverted enable. 0 = Normal 1 = Inverted	0x00
12	rw	TM26_UEV_DIS	Update event generation disable for main Timer. Update event is generation from counter overflow/underflow or software register forced bit. 0 = Enable	0x00

			1 = Disable	
11	rw	TM26_EX_INV	Timer external trigger input inverted enable. 0 = Normal 1 = Inverted	0x00
10	rw	TM26_EX_EN	Timer external trigger event enable. 0 = Disable 1 = Enable	0x00
9	rw	TM26_ACLEAR_EN	Timer overflow or underflow flag auto-clear enable. This bit is no effect if TMx_ASTOP_EN is disabled. When enables, the timer will auto clear the flag of TMx_TOF or TMx_TUF after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
8	rw	TM26_ASTOP_EN	Timer auto stop mode enable. When enables, the timer will auto stop after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
7	rw	TM26_DIR2	2nd Timer counting direction bit. 0 = Up (Up Counting) 1 = Down (Down Counting)	0x00
6	rw	TM26_DIR	Main Timer counting direction bit. 0 = Up (Up Counting) 1 = Down (Down Counting)	0x00
5..4	rw	TM26_MDS	Timer operation mode select. When selects 'Cascade', both TMx_EN and TMx_EN2 must set the same setting of Enable or Disable. (x : module index) 0x0 = Cascade : 16-bit counter with 16-bit prescaler Mode 0x1 = Separate : Separated two 16-bit counters Mode 0x2 = Full-Counter : 32-bit counter Mode 0x3 = Reserved	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	rw	TM26_EN2	2nd Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00
0	rw	TM26_EN	Main Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00

1.33.6. TM26 Timer control register 1

TM26_CR1	TM26 Timer control register 1		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved		TM26_CC1B_SEN	TM26_CC0B_SEN	Reserved		TM26_CC1A_SEN	TM26_CC0A_SEN
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved						TM26_OVR1_MDS	TM26_OVR0_MDS

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..14	-	Reserved	Reserved	0x00
13	rw	TM26_CC1B_SEN	Timer channel 1 software IC/OC event-B generation enable. When capture mode, this bit is used to trigger falling edge capture event. When PWM mode, this bit is used to set TM26_CF1B flag only. (set by software and clear by hardware)	0x00

			0 = No-Effect 1 = Enable	
12	rw	TM26_CC0B_SEN	Timer channel 0 software IC/OC event-B generation enable. When capture mode, this bit is used to trigger falling edge capture event. When PWM mode, this bit is used to set TM26_CF0B flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
11..10	-	Reserved	Reserved	0x00
9	rw	TM26_CC1A_SEN	Timer channel 1 software IC/OC event-A generation enable. When capture mode, this bit is used to trigger rising edge capture event. When PWM mode, this bit is used to set TM26_CF1A flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
8	rw	TM26_CC0A_SEN	Timer channel 0 software IC/OC event-A generation enable. When capture mode, this bit is used to trigger rising edge capture event. When PWM mode, this bit is used to set TM26_CF0A flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
7..2	-	Reserved	Reserved	0x00
1	rw	TM26_OVR1_MDS	Timer channel 1 capture data buffer overrun mode select 0 = Overwritten (Overwritten by new data) 1 = Keep (Preserved old data)	0x00
0	rw	TM26_OVR0_MDS	Timer channel 0 capture data buffer overrun mode select 0 = Overwritten (Overwritten by new data) 1 = Keep (Preserved old data)	0x00

1.33.7. TM26 Timer CKO control register

TM26_CKO	TM26 Timer CKO control register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				TM26_CKO_LCK	TM26_CKO_STA	TM26_CKO_SEL	TM26_CKO_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	TM26_CKO_LCK	TM26_CKO_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
2	rw	TM26_CKO_STA	Timer CKO output signal initial state. The bit is written effectively only by written 1 to TM26_CKO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
1	rw	TM26_CKO_SEL	Timer overflow as CKO output source select. 0 = 2nd : 2nd Timer overflow 1 = Main : Main Timer overflow	0x00

0	rw	TM26_CKO_EN	Timer overflow as CKO output enable. 0 = Disable 1 = Enable	0x00

1.33.8. TM26 repetition counter register

TM26_RCNT	TM26 repetition counter register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
TM26_RARR[7:0]							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM26_RCNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	rw	TM26_RARR	Repetition counter auto-reload value register. This register is used to set the main timer overflow / underflow number or TMx_CKOM pulse number which is as the next updated auto-reload value after the Repetition counter is underflow. When the Repetition counter has been started and counting underflow, the chip will be asserting a RTUF flag.	0x00
15..8	-	Reserved	Reserved	0x00
7..0	rw	TM26_RCNT	Repetition counter register.	0x00

1.33.9. TM26 Timer main counter register

TM26_CNT	TM26 Timer main counter register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM26_CNT[15:8]							
7	6	5	4	3	2	1	0
TM26_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM26_CNT	Main timer/counter register.	0x0000

1.33.10. TM26 Timer main counter auto-reload value register

TM26_ARR	TM26 Timer main counter auto-reload value register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM26_ARR[15:8]							
7	6	5	4	3	2	1	0

TM26_ARR[7:0]

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM26_ARR	Main timer/counter auto-reload value register. [Two 8bit OC/PWM Mode] for all channels: This register value is limited to 0x00ZZ (ZZ={0x00~0xFF}) [Two 8bit OC/PWM,16bit OC/PWM Mode] for mixed channels: This register value is limited to 0xZZFF (ZZ={0x00~0xFF})	0x0000

1.33.11. TM26 Timer prescaler register

TM26_PSCNT	TM26 Timer prescaler register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
TM26_CNTA[15:8]							
23	22	21	20	19	18	17	16
TM26_CNTA[7:0]							
15	14	13	12	11	10	9	8
TM26_PSCNT[15:8]							
7	6	5	4	3	2	1	0
TM26_PSCNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	r	TM26_CNTA	Main timer/counter alias register. This register is the alias of TM26_CNT for read only.	0x0000
15..0	rw	TM26_PSCNT	Timer prescaler or 2nd timer/counter register	0x0000

1.33.12. TM26 Timer prescaler auto-reload register

TM26_PSARR	TM26 Timer prescaler auto-reload register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM26_PSARR[15:8]							
7	6	5	4	3	2	1	0
TM26_PSARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM26_PSARR	Timer prescaler or 2nd timer/counter auto-reload value register	0x0000

1.33.13. TM26 Timer capture and compare mode select register

TM26_CCMDS	TM26 Timer capture and compare mode select register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							TM26_OC_LCK
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0

Reserved	TM26_CC1_MDS[2:0]	Reserved	TM26_CC0_MDS[2:0]

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..17	-	Reserved	Reserved	0x00
16	rw	TM26_OC_LCK	Timer output compare reload function lock enable bit for all channel. When enables and timer update event is happened, it is locked that the compare preload registers of TM26_CCnB reload to compare shadow buffer registers of TM26_CCnA. Until this bit is disabled, these compare preload registers will update the compare shadow buffer at next timer update event happened. 0 = un-Locked : enable unlocked 1 = Locked : enable locked	0x00
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6..4	rw	TM26_CC1_MDS	Timer channel 1 capture and compare mode select. 0x0 = NOP (No operation) 0x1 = 16bit_IC (Input capture) 0x2 = 16bit_OC (Output compare) 0x3 = 8bitx2_OC (Two 8-bit compare) 0x4 = 16bit_PWM (16bit PWM) 0x5 = 8bitx2_PWM (Two 8bit PWMs) 0x6 = Reserved 0x7 = Reserved	0x00
3	-	Reserved	Reserved	0x00
2..0	rw	TM26_CC0_MDS	Timer channel 0 capture and compare mode select. 0x0 = NOP (No operation) 0x1 = 16bit_IC (Input capture) 0x2 = 16bit_OC (Output compare) 0x3 = 8bitx2_OC (Two 8-bit compare) 0x4 = 16bit_PWM (16bit PWM) 0x5 = 8bitx2_PWM (Two 8bit PWMs) 0x6 = Reserved 0x7 = Reserved	0x00

1.33.14. TM26 Timer input capture control register

TM26_ICCR	TM26 Timer input capture control register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved				TM26_IC1_TRGS[1:0]		TM26_IC0_TRGS[1:0]	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		TM26_IC1_MUX[1:0]		Reserved		TM26_IC0_MUX[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..20	-	Reserved	Reserved	0x00
19..18	rw	TM26_IC1_TRGS	Timer channel 1 input trigger edge select. 0x0 = Disable : disable capture data 0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	0x00
17..16	rw	TM26_IC0_TRGS	Timer channel 0 input trigger edge select. 0x0 = Disable : disable capture data	0x00

			0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5..4	rw	TM26_IC1_MUX	Timer channel 1 input Mux select for input capture. 0x0 = IC10 : TM26_IC1 0x1 = IC11 : TM26_ITR 0x2 = IC12 : CMP1_OUT 0x3 = IC13 : Reserved	0x00
3..2	-	Reserved	Reserved	0x00
1..0	rw	TM26_IC0_MUX	Timer channel 0 input Mux select for input capture. 0x0 = IC00 : TM26_IC0 0x1 = IC01 : TM26_ITR 0x2 = IC02 : CMP0_OUT 0x3 = IC03 : Reserved	0x00

1.33.15. TM26 Timer output compare state register

TM26_OSCR	TM26 Timer output compare state register
Offset Address : 0x38	Reset Value : 0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved		TM26_OS1H_LCK	TM26_OS0H_LCK	Reserved		TM26_OS1H_STA	TM26_OS0H_STA
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		TM26_OS1_LCK	TM26_OS0_LCK	Reserved		TM26_OS1_STA	TM26_OS0_STA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	-	Reserved	Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13	rw	TM26_OS1H_LCK	TM26_OS1H_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access.TM26_OS1H_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
12	rw	TM26_OS0H_LCK	TM26_OS0H_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. TM26_OS0H_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
11..10	-	Reserved	Reserved	0x00
9	rw	TM26_OS1H_STA	Timer channel 1 OC compare-H output signal initial state for two 8-Bit comparator mode 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
8	rw	TM26_OS0H_STA	Timer channel 0 OC compare-H output signal initial state for two 8-Bit comparator mode. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	TM26_OS1_LCK	TM26_OS1_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. TM26_OS1_STA is written	0x00

			effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	
4	rw	TM26_OS0_LCK	TM26_OS0_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. TM26_OS0_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	TM26_OS1_STA	Timer channel 1 OC compare/compare-L output signal initial state. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
0	rw	TM26_OS0_STA	Timer channel 0 OC compare/compare-L output signal initial state. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00

1.33.16. TM26 Timer output compare control register 0

TM26_OCCR0	TM26 Timer output compare control register 0		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			TM26_OC1N_OE	Reserved			TM26_OC0N_OE
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	TM26_OC1_OE2	TM26_OC1_OE1	TM26_OC1_OE0	Reserved	TM26_OC0_OE2	TM26_OC0_OE1	TM26_OC0_OE0

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..21	-	Reserved	Reserved	0x00
20	rw	TM26_OC1N_OE	Timer channel 1 OC1N (complement) line output enable. 0 = Disable (output by TM26_BK1N_STA setting) 1 = Enable	0x00
19..17	-	Reserved	Reserved	0x00
16	rw	TM26_OC0N_OE	Timer channel 0 OC0N (complement) line output enable. 0 = Disable (output by TM26_BK0N_STA setting) 1 = Enable	0x00
15..8	-	Reserved	Reserved	0x00
7	-	Reserved	Reserved	0x00
6	rw	TM26_OC1_OE2	Timer channel 1 OC line-2 output enable. 0 = Disable (output by TM36_BK1_STA setting) 1 = Enable	0x00
5	rw	TM26_OC1_OE1	Timer channel 1 OC line-1 output enable. 0 = Disable (output by TM26_BK1_STA setting) 1 = Enable	0x00
4	rw	TM26_OC1_OE0	Timer channel 1 OC line-0 output enable. 0 = Disable (output by TM26_BK1_STA setting) 1 = Enable	0x00
3	-	Reserved	Reserved	0x00
2	rw	TM26_OC0_OE2	Timer channel 0 OC line-2 output enable. 0 = Disable (output by TM36_BK0_STA setting) 1 = Enable	0x00
1	rw	TM26_OC0_OE1	Timer channel 0 OC line-1 output enable. 0 = Disable (output by TM26_BK0_STA setting)	0x00

			1 = Enable	
0	rw	TM26_OC0_OE0	Timer channel 0 OC line-0 output enable. 0 = Disable (output by TM26_BK0_STA setting) 1 = Enable	0x00

1.33.17. TM26 Timer output compare control register 1

TM26_OCCR1	TM26 Timer output compare control register 1
Offset Address : 0x40	Reset Value : 0x00000000

31	30	29	28	27	26	25	24
Reserved	TM26_ODLY_SEL	Reserved	TM26_POE_SW	Reserved	TM26_POE_EN2	TM26_POE_EN1	TM26_POE_EN0
23	22	21	20	19	18	17	16
Reserved	TM26_OC1_POE2	TM26_OC1_POE1	TM26_OC1_POE0	Reserved	TM26_OC0_POE2	TM26_OC0_POE1	TM26_OC0_POE0
15	14	13	12	11	10	9	8
Reserved						TM26_OC1N_INV	TM26_OC0N_INV
7	6	5	4	3	2	1	0
Reserved		TM26_OC1H_INV	TM26_OC0H_INV	Reserved		TM26_OC1_INV	TM26_OC0_INV

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	TM26_ODLY_SEL	Timer output delay mode select. When selects '0Step', channel-0,1 output is normal and no delay. When selects '1Step', channel-0,1 output will delay 0,1 step uint delay time. 0x0 = 0Step 0x1 = 1Step	0x00
29	-	Reserved	Reserved	0x00
28	w	TM26_POE_SW	Timer output enable registers preload software enable bit. Refer the TM26_OCn_POE[2:0] (n={0,1}) registers for the output enable registers detail descriptions. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
27	-	Reserved	Reserved	0x00
26	rw	TM26_POE_EN2	Timer OC preload enable bit for output enable preload register control. This bit is used to enable INT_PD input. 0 = Disable 1 = Enable	0x00
25	rw	TM26_POE_EN1	Timer OC preload enable bit for output enable preload register control. This bit is used to enable INT_PB input. 0 = Disable 1 = Enable	0x00
24	rw	TM26_POE_EN0	Timer OC preload enable bit for output enable preload register control. This bit is used to enable 3-line XOR input from TM36. 0 = Disable 1 = Enable	0x00
23	-	Reserved	Reserved	0x00
22	rw	TM26_OC1_POE2	Timer channel 1 OC line-2 output enable preload register bit. This bit will load into TM26_OC1_OE2 register when the preload event happened. 0 = Disable 1 = Enable	0x00
21	rw	TM26_OC1_POE1	Timer channel 1 OC line-1 output enable preload register bit. This bit will load into TM26_OC0_OE1 register when the preload event happened. 0 = Disable 1 = Enable	0x00
20	rw	TM26_OC1_POE0	Timer channel 1 OC line-0 output enable preload register bit. This bit will load into TM26_OC0_OE0 register when the preload event happened.	0x00

			0 = Disable 1 = Enable	
19	-	Reserved	Reserved	0x00
18	rw	TM26_OC0_POE2	Timer channel 0 OC line-2 output enable preload register bit. This bit will load into TM26_OC0_OE2 register when the preload event happened. 0 = Disable 1 = Enable	0x00
17	rw	TM26_OC0_POE1	Timer channel 0 OC line-1 output enable preload register bit. This bit will load into TM26_OC0_OE1 register when the preload event happened. 0 = Disable 1 = Enable	0x00
16	rw	TM26_OC0_POE0	Timer channel 0 OC line-0 output enable preload register bit. This bit will load into TM26_OC0_OE0 register when the preload event happened. 0 = Disable 1 = Enable	0x00
15..10	-	Reserved	Reserved	0x00
9	rw	TM26_OC1N_INV	Timer channel 1 complement output inverse enable. 0 = Disable 1 = Enable	0x00
8	rw	TM26_OC0N_INV	Timer channel 0 complement output inverse enable. 0 = Disable 1 = Enable	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	TM26_OC1H_INV	Timer channel 1 High output inverse enable. 0 = Disable 1 = Enable	0x00
4	rw	TM26_OC0H_INV	Timer channel 0 High output inverse enable. 0 = Disable 1 = Enable	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	TM26_OC1_INV	Timer channel 1 output inverse enable. 0 = Disable 1 = Enable	0x00
0	rw	TM26_OC0_INV	Timer channel 0 output inverse enable. 0 = Disable 1 = Enable	0x00

1.33.18. TM26 Timer PWM and DTG control register

TM26_PWM	TM26 Timer PWM and DTG control register		
Offset Address :	0x44	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						TM26_PWM_MDS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..2	-	Reserved	Reserved	0x00
1..0	rw	TM26_PWM_MDS	Timer OC0/1/2/3 PWM mode select. 0x0 = Edge Left-aligned	0x00

			0x1 = Reserved 0x2 = Reserved 0x3 = Reserved	

1.33.19. TM26 Timer stop control register

TM26_BS	TM26 Timer stop control register		
Offset Address :	0x48	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved		TM26_STP1N_STA	TM26_STP0N_STA	Reserved		TM26_STP1_STA	TM26_STP0_STA
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

Bit	Attr	Bit Name	Description	Reset
31..30	-	Reserved	Reserved	0x00
29	rw	TM26_STP1N_STA	Timer BK input active or stop condition output OC1N state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
28	rw	TM26_STP0N_STA	Timer BK input active or stop condition output OC0N state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
27..26	-	Reserved	Reserved	0x00
25	rw	TM26_STP1_STA	Timer BK input active or stop condition output OC1 state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
24	rw	TM26_STP0_STA	Timer BK input active or stop condition output OC0 state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
23..16	-	Reserved	Reserved	0x00
15..0	-	Reserved	Reserved	0x0000

1.33.20. TM26 Timer capture and compare register 0A

TM26_CC0A	TM26 Timer capture and compare register 0A		
Offset Address :	0x50	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM26_CC0A[15:8]							
7	6	5	4	3	2	1	0
TM26_CC0A[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM26_CC0A	TM26 Timer capture and compare register 0A for channel 0. When the channel is configured as input capture mode, this register is used to capture the counter value of input trigger	0x0000

			signal : (1) first capture data for single edge (2) rising edge capture data for dual edge. When the channel is configured as output compare/PWM mode, this register is used as the compared shadow register for Timer output compare and will be copied from R_TM26_CC0B when TM26_CC0B was write. When the channel is configured as output two 8-bit compare/PWM mode, this register is separated to low 8-bt compared shadow register for compare-L path and high 8-bt compared shadow register for compare-H path.	

1.33.21. TM26 Timer capture and compare register 0B

TM26_CC0B	TM26 Timer capture and compare register 0B		
Offset Address :	0x54	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM26_CC0B[15:8]							
7	6	5	4	3	2	1	0
TM26_CC0B[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM26_CC0B	TM26 Timer capture and compare register 0B for channel 0. When the channel is configured as input capture mode, this register is used to capture the counter value of input trigger signal : (1) 2nd capture data for single edge (2) falling edge capture data for dual edge. When the channel is configured as output compare/PWM mode, this register is used as the compared preload register for software setting and will copy the value to TM26_CC0A. When the channel is configured as output two 8-bit compare/PWM mode, this register is separated to low 8-bt compared preload register for compare-L path and high 8-bt compared preload register for compare-H path.	0x0000

1.33.22. TM26 Timer capture and compare register 1A

TM26_CC1A	TM26 Timer capture and compare register 1A		
Offset Address :	0x58	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM26_CC1A[15:8]							
7	6	5	4	3	2	1	0
TM26_CC1A[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM26_CC1A	TM26 Timer capture and compare register 1A for channel 1. Refer to the register descriptions of TM26_CC0A for detail descriptions.	0x0000

1.33.23. TM26 Timer capture and compare register 1B

TM26_CC1B	TM26 Timer capture and compare register 1B		
Offset Address :	0x5c	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM26_CC1B[15:8]							
7	6	5	4	3	2	1	0
TM26_CC1B[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM26_CC1B	Timer TM26 capture and compare register 1B for channel 1. Refer to the register descriptions of TM26_CC0B for detail descriptions.	0x0000

1.33.24. TM26 Register Map

TM26 Register Map Register Number = 23

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	TM26_STA	Reserved								Reserved			TM26_RTUF	TM26_QPEF	TM26_IDXF	Reserved	TM26_DIRCF	Reserved		TM26_CF1B	TM26_CF0B	Reserved		TM26_CF1A	TM26_CF0A	TM26_TUF2	TM26_TUF	TM26_TOF2	TM26_TOF	TM26_EXF	Reserved		TM26_DIRF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	TM26_INT	Reserved								Reserved			TM26_RTU_IE	TM26_QPE_IE	TM26_IDX_IE	Reserved	TM26_DIRC_IE	Reserved						TM26_CC1_IE	TM26_CC0_IE	Reserved		TM26_TIE2	TM26_TIE	TM26_EXIE	Reserved		TM26_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	TM26_CLK	Reserved								Reserved			TM26_RC_CKS	Reserved				Reserved		TM26_CKI_DIV [1:0]		Reserved		TM26_CKI_SEL [1:0]		TM26_CKS2_SEL	TM26_CKS_SEL	TM26_CKE_SEL [1:0]		Reserved			
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	TM26_TRG	TM26_GT2_SW	TM26_GT_SW	TM26_RST2_SW	TM26_RST_SW	Reserved		TM26_TRGO_INV	TM26_TRGO_SW	TM26_UEV_SEL [1:0]		TM26_IDX_MDS [1:0]		TM26_IDX_EN	TM26_QEI_MDS [2:0]			TM26_TRGO_MDS [3:0]				Reserved	TM26_ITR_MUX [2:0]			TM26_TRG_MUX [1:0]		TM26_TRGI2_MDS [2:0]			TM26_TRGI_MDS [2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	TM26_CR0	Reserved								Reserved						TM26_RC_STP	TM26_RC_EN	TM26_UEX_EN	TM26_USW_EN	TM26_DIR_INV	TM26_UEV_DIS	TM26_EX_INV	TM26_EX_EN	TM26_ACLEAR_EN	TM26_ASTOP_EN	TM26_DIR2	TM26_DIR	TM26_MDS[1:0]		Reserved	Reserved	TM26_EN2	TM26_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	TM26_CR1	Reserved																Reserved		TM26_CC1B_SEN	TM26_CC0B_SEN	Reserved		TM26_CC1A_SEN	TM26_CC0A_SEN	Reserved						TM26_OVR1_MDS	TM26_OVR0_MDS
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	TM26_CKO	Reserved																Reserved								Reserved				TM26_CKO_LCK	TM26_CKO_STA	TM26_CKO_SEL	TM26_CKO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	TM26_RCNT	Reserved								TM26_RARR[7:0]								Reserved								TM26_RCNT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x20	TM26_CNT	Reserved																TM26_CNT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	TM26_ARR	Reserved																TM26_ARR[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	TM26_PSCNT	TM26_CNTA[15:0]																TM26_PSCNT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	TM26_PSARR	Reserved																TM26_PSARR[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	TM26_CCMDS	Reserved								Reserved							TM26_OC_LCK	Reserved								Reserved	TM26_CC1_MDS[2:0]			Reserved	TM26_CC0_MDS[2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	TM26_ICCR	Reserved								Reserved				TM26_IC1_TRGS[1:0]		TM26_IC0_TRGS[1:0]		Reserved								Reserved		TM26_IC1_MUX[1:0]		Reserved		TM26_IC0_MUX[1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	TM26_OSCR	Reserved								Reserved								Reserved		TM26_OS1H_LCK	TM26_OS0H_LCK	Reserved		TM26_OS1H_STA	TM26_OS0H_STA	Reserved		TM26_OS1_LCK	TM26_OS0_LCK	Reserved		TM26_OS1_STA	TM26_OS0_STA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	TM26_OCCR0	Reserved								Reserved			TM26_OC1N_OE	Reserved			TM26_OC0N_OE	Reserved								Reserved	TM26_OC1_OE2	TM26_OC1_OE1	TM26_OC1_OE0	Reserved	TM26_OC0_OE2	TM26_OC0_OE1	TM26_OC0_OE0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	TM26_OCCR1	Reserved	TM26_ODLY_SEL	Reserved	TM26_POE_SW	Reserved	TM26_POE_EN2	TM26_POE_EN1	TM26_POE_EN0	Reserved	TM26_OC1_POE2	TM26_OC1_POE1	TM26_OC1_POE0	Reserved	TM26_OC0_POE2	TM26_OC0_POE1	TM26_OC0_POE0	Reserved						TM26_OC1N_INV	TM26_OC0N_INV	Reserved		TM26_OC1H_INV	TM26_OC0H_INV	Reserved		TM26_OC1_INV	TM26_OC0_INV
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x44	TM26_PWM	Reserved																Reserved								Reserved						TM26_PWM_MDS[1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x48	TM26_BS	Reserved		TM26_STP1N_STA	TM26_STP0N_STA	Reserved		TM26_STP1_STA	TM26_STP0_STA	Reserved								Reserved															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	TM26_CC0A	Reserved																TM26_CC0A[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x54	TM26_CC0B	Reserved																TM26_CC0B[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x58	TM26_CC1A	Reserved																TM26_CC1A[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x5c	TM26_CC1B	Reserved																TM26_CC1B[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.34. Timer36 Control Registers

Timer36 Control	(TM36) Timer Control Module-36
Base Address :	0x56860000

1.34.1. TM36 Timer status register

TM36_STA	TM36 Timer status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			TM36_RTUF	TM36_QPEF	TM36_IDXF	Reserved	TM36_DIRCF
15	14	13	12	11	10	9	8
TM36_CF3B	TM36_CF2B	TM36_CF1B	TM36_CF0B	TM36_CF3A	TM36_CF2A	TM36_CF1A	TM36_CF0A
7	6	5	4	3	2	1	0
TM36_TUF2	TM36_TUF	TM36_TOF2	TM36_TOF	TM36_EXF	TM36_BKF	Reserved	TM36_DIRF

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..21	-	Reserved	Reserved	0x00
20	rw	TM36_RTUF	Repetition timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
19	rw	TM36_QPEF	Main Timer QEI phase state transition error detect flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
18	rw	TM36_IDXF	Main Timer QEI external index signal input active detect and internal timer reset flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	-	Reserved	Reserved	0x00
16	rw	TM36_DIRCF	Main Timer up/down counting direction change flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15	rw	TM36_CF3B	Timer IC3 falling edge flag/OC3 event sub flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of TM36_CF0B. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
14	rw	TM36_CF2B	Timer IC2 falling edge flag/OC2 event sub flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of TM36_CF0B. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
13	rw	TM36_CF1B	Timer IC1 falling edge flag/OC1 event sub flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of TM36_CF0B. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
12	rw	TM36_CF0B	Timer IC0 falling edge flag/OC0 event sub flag. (set by hardware and clear by software writing 1) [Capture Mode]: Input capture event sub flag for single edge mode or input capture falling edge event flag for dual edge mode. [16-bit Compare/PWM Mode]: When center-alignment PWM mode, this bit is used as down counting PWM compare flag. It is no using for other 16-bit comparator mode. [8-bit Compare/PWM Mode]: (1) When compare-L is PWM and center-alignment mode, this bit is used as down counting PWM compare-L flag. (2) Others, this bit is used as compare-H event flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
11	rw	TM36_CF3A	Timer IC3 rising edge flag/OC3 event main flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of TM36_CF0A. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
10	rw	TM36_CF2A	Timer IC2 rising edge flag/OC2 event main flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of TM36_CF0A. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
9	rw	TM36_CF1A	Timer IC1 rising edge flag/OC1 event main flag. (set by hardware and clear by software writing 1) Refer to the register descriptions of TM36_CF0A. 0 = Normal (No event occurred)	0x00

			1 = Happened (Event happened)	
8	rw	TM36_CF0A	Timer IC0 rising edge flag/OC0 event main flag. (set by hardware and clear by software writing 1) [Capture Mode]: Input capture event main flag for single edge mode or input capture rising edge event flag for dual edge mode. [16-bit Compare/PWM Mode]: Output compare event flag for 16-bit comparator mode. When center-alignment PWM mode, this bit is used as up counting PWM compare flag. [8-bit Compare/PWM Mode]: Output compare-L event flag. When compare-L is PWM and center-alignment mode, this bit is used as up counting PWM compare-L flag. 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
7	rw	TM36_TUF2	2nd Timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	rw	TM36_TUF	Main Timer underflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	rw	TM36_TOF2	2nd Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	TM36_TOF	Main Timer overflow flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	TM36_EXF	Timer external trigger flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	TM36_BKF	Timer break input flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	-	Reserved	Reserved	0x00
0	r	TM36_DIRF	Main Timer up/down counting flag. 0 = Up counting 1 = Down counting	0x00

1.34.2. TM36 Timer interrupt enable register

TM36_INT	TM36 Timer interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved			TM36_RTU_IE	TM36_QPE_IE	TM36_IDX_IE	Reserved	TM36_DIRC_IE
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved				TM36_CC3_IE	TM36_CC2_IE	TM36_CC1_IE	TM36_CC0_IE
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		TM36_TIE2	TM36_TIE	TM36_EXIE	TM36_BKIE	Reserved	TM36_IEA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..21	-	Reserved	Reserved	0x00

20	rw	TM36_RTU_IE	Repetition timer underflow interrupt enable. 0 = Disable 1 = Enable	0x00
19	rw	TM36_QPE_IE	Main Timer QEI phase state transition error detect interrupt enable. 0 = Disable 1 = Enable	0x00
18	rw	TM36_IDX_IE	Main Timer QEI external index signal input active detect interrupt enable. 0 = Disable 1 = Enable	0x00
17	-	Reserved	Reserved	0x00
16	rw	TM36_DIRC_IE	Main Timer up/down counting direction change interrupt enable. 0 = Disable 1 = Enable	0x00
15..12	-	Reserved	Reserved	0x00
11	rw	TM36_CC3_IE	Timer IC3/OC3 interrupt enable. 0 = Disable 1 = Enable	0x00
10	rw	TM36_CC2_IE	Timer IC2/OC2 interrupt enable. 0 = Disable 1 = Enable	0x00
9	rw	TM36_CC1_IE	Timer IC1/OC1 interrupt enable. 0 = Disable 1 = Enable	0x00
8	rw	TM36_CC0_IE	Timer IC0/OC0 interrupt enable. 0 = Disable 1 = Enable	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	TM36_TIE2	2nd Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	TM36_TIE	Timer overflow/underflow interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	TM36_EXIE	Timer external trigger interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	TM36_BKIE	Timer break input interrupt enable. 0 = Disable 1 = Enable	0x00
1	-	Reserved	Reserved	0x00
0	rw	TM36_IEA	Timer interrupt all enable. When disables, the timer global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.34.3. TM36 Timer clock source register

TM36_CLK	TM36 Timer clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			TM36_RC_CKS	Reserved		TM36_DTG_DIV[1:0]	
15	14	13	12	11	10	9	8
Reserved		TM36_CKI_DIV[1:0]		Reserved		TM36_CKI_SEL[1:0]	

7	6	5	4	3	2	1	0
TM36_CKS2_SEL	TM36_CKS_SEL	TM36_CKE_SEL[1:0]		Reserved	Reserved	Reserved	

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..21	-	Reserved	Reserved	0x00
20	rw	TM36_RC_CKS	Repetition Timer/Counter clock source select. 0 = MAIN : clock input from Main timer overflow/underflow 1 = CKO : clock input from CK_CKOM	0x00
19..18	-	Reserved	Reserved	0x00
17..16	rw	TM36_DTG_DIV	Timer internal dead time clock CK_DTG divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
15..14	-	Reserved	Reserved	0x00
13..12	rw	TM36_CKI_DIV	Timer internal clock CK_TM36_INT input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
11..10	-	Reserved	Reserved	0x00
9..8	rw	TM36_CKI_SEL	Timer input clock CK_TM36 source select. 0x0 = PROC : CK_TM36_PR process clock from CSC 0x1 = Reserved 0x2 = CK_LS 0x3 = Reserved	0x00
7	rw	TM36_CKS2_SEL	Counter/Timer CK_TC2 clock source select. 0 = CK_INT 1 = CK_EXT	0x00
6	rw	TM36_CKS_SEL	Counter/Timer CK_TC clock source select. 0 = CK_INT 1 = CK_EXT	0x00
5..4	rw	TM36_CKE_SEL	Timer internal clock CK_EXT source select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = IN0 (TM36_IN0) 0x3 = IN1 (TM36_IN1)	0x00
3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1..0	-	Reserved	Reserved	0x00

1.34.4. TM36 Timer trigger control register

TM36_TRG	TM36 Timer trigger control register		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
TM36_GT2_SW	TM36_GT_SW	TM36_RST2_SW	TM36_RST_SW	Reserved		TM36_TRGO_INV	TM36_TRGO_SW
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TM36_UEV_SEL[1:0]		TM36_IDX_MDS[1:0]		TM36_IDX_EN	TM36_QEI_MDS[2:0]		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TM36_TRGO_MDS[3:0]				Reserved	TM36_ITR_MUX[2:0]		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TM36_TRG_MUX[1:0]		TM36_TRGI2_MDS[2:0]			TM36_TRGI_MDS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31	rw	TM36_GT2_SW	2nd Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00

30	rw	**TM36_GT_SW**	Timer clock gating software enable bit. 0 = Disable 1 = Enable	0x00
29	rw	**TM36_RST2_SW**	2nd Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
28	rw	**TM36_RST_SW**	Timer reset software enable bit. 0 = Disable 1 = Enable	0x00
27..26	-	**Reserved**	Reserved	0x00
25	rw	**TM36_TRGO_INV**	Timer TRGO output inverse enable bit. 0 = Disable 1 = Enable	0x00
24	rw	**TM36_TRGO_SW**	Timer TRGO software control data bit. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
23..22	rw	**TM36_UEV_SEL**	Timer UEV output select bits for TM36_TRGO. When TM36_TRGO_MDS selects UEV as output signal, this bit uses to select output pulse function from Main timer overflow and/or underflow. These bits are no effect when TM36_TRGO_MDS does not select UEV as output. 0x0 = All : output all UEV pulses 0x1 = TOF : output timer overflow pulses 0x2 = UDF : output timer underflow pulses 0x3 = Reserved	0x00
21..20	rw	**TM36_IDX_MDS**	Main Timer QEI external index signal input reset timer transition state select. 0x0 = 1T2 : State change between 1 and 2 0x1 = 2T3 : State change between 2 and 3 0x2 = 3T4 : State change between 3 and 4 0x3 = 4T1 : State change between 4 and 1	0x00
19	rw	**TM36_IDX_EN**	Main Timer QEI external index signal input enable. When enables and the index signal will input from TM36_ETR, the timer will reset during up counting or reload the auto-reload value during down counting if detect the index signal active pulse. 0 = Disable 1 = Enable	0x00
18..16	rw	**TM36_QEI_MDS**	Main Timer quadrature encoder interface(QEI) or external input timer up/down control mode select. 0x0 = No operation (up/down control by TM36_DIR) 0x1 = IN0POS : TM36_IN0 positive (high level up count, low level down count) 0x2 = IN0NEG : TM36_IN0 negative (low level up count, high level down count) 0x3 = IN0TRG : TM36_IN0 trigger (edge depending on TM36_IN1 level) 0x4 = IN1TRG : TM36_IN1 trigger (edge depending on TM36_IN0 level) 0x5 = BOTH : Both TM36_IN0 and TM36_IN1 edge	0x00
15..12	rw	**TM36_TRGO_MDS**	Timer trigger output mode select 0x0 = RST : TM36_RST (Main Timer Reset) 0x1 = EN : TM36_EN (Main Timer Enable) 0x2 = UEV : TM36_UEV (Main Timer Update event) 0x3 = TOF : TM36_TOF (Main Timer overflow) 0x4 = TUF : TM36_TUF (Main Timer underflow) 0x5 = EN2 : TM36_EN2 (Timer-2 Enable) 0x6 = TOF2 :TM36_TOF2 (Timer-2 overflow) 0x7 = DIR : TM36_DIR (Main Timer direction event) 0x8 = UEV2 : TM36_UEV2 (Timer-2 Update event) 0x9 = SW : TM36_TRGO_SW (software control bit)	0x00

			0xA = OS0 : TM36_OS0 (channel-0 output state signal) 0xB = OS1 : TM36_OS1 (channel-1 output state signal) 0xC = OS2 : TM36_OS2 (channel-2 output state signal) 0xD = OS3 : TM36_OS3 (channel-3 output state signal) 0xE = TRGI : TM36_TRGI (internal TRGI signal) 0xF = POE : TM36_POE (Output enable register preload signal)	
11	-	Reserved	Reserved	0x00
10..8	rw	TM36_ITR_MUX	Timer internal trigger source select. See the [Timer Internal Trigger and Channel Input Signals Table] for more information. 0x0 = ITR0 (TM36_ITR0) 0x1 = ITR1 (TM36_ITR1) 0x2 = ITR2 (TM36_ITR2) 0x3 = ITR3 (TM36_ITR3) 0x4 = ITR4 (TM36_ITR4) 0x5 = ITR5 (TM36_ITR5) 0x6 = ITR6 (TM36_ITR6) 0x7 = ITR7 (TM36_ITR7)	0x00
7..6	rw	TM36_TRG_MUX	Timer trigger source TRGI select. 0x0 = ETR (CK_ETR) 0x1 = ITR (CK_ITR) 0x2 = IN0 (TM36_IN0) 0x3 = IN1 (TM36_IN1)	0x00
5..3	rw	TM36_TRGI2_MDS	2nd Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00
2..0	rw	TM36_TRGI_MDS	Timer trigger input mode select 0x0 = No operation 0x1 = Trigger-R (TRGI rising) 0x2 = Reset-R (TRGI rising) 0x3 = Gate-H (TRGI high) 0x4 = Reset (TRGI dual edge) 0x5 = Trigger-F (TRGI falling) 0x6 = Reset-F (TRGI falling) 0x7 = Gate-L (TRGI low)	0x00

1.34.5. TM36 Timer control register 0

TM36_CR0	TM36 Timer control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						TM36_RC_STP	TM36_RC_EN
15	14	13	12	11	10	9	8
TM36_UEX_EN	TM36_USW_EN	TM36_DIR_INV	TM36_UEV_DIS	TM36_EX_INV	TM36_EX_EN	TM36_ACLEAR_EN	TM36_ASTOP_EN
7	6	5	4	3	2	1	0
TM36_DIR2	TM36_DIR	TM36_MDS[1:0]		Reserved	Reserved	TM36_EN2	TM36_EN

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..18	-	Reserved	Reserved	0x00
17	rw	TM36_RC_STP	Main Counter stop enable when repetition counter underflow.	0x00

			0 = Disable 1 = Enable	
16	rw	**TM36_RC_EN**	Repetition Counter enable bit. 0 = Disable 1 = Enable	0x00
15	rw	**TM36_UEX_EN**	Timer external trigger update event enable. 0 = Disable 1 = Enable	0x00
14	rw	**TM36_USW_EN**	Timer software update event generation enable. (automatically clear by hardware) 0 = Disable 1 = Enable	0x00
13	rw	**TM36_DIR_INV**	Main Timer counting direction inverted enable. 0 = Normal 1 = Inverted	0x00
12	rw	**TM36_UEV_DIS**	Update event generation disable for main Timer. Update event is generation from counter overflow/underflow or software register forced bit. 0 = Enable 1 = Disable	0x00
11	rw	**TM36_EX_INV**	Timer external trigger input inverted enable. 0 = Normal 1 = Inverted	0x00
10	rw	**TM36_EX_EN**	Timer external trigger event enable. 0 = Disable 1 = Enable	0x00
9	rw	**TM36_ACLEAR_EN**	Timer overflow or underflow flag auto-clear enable. This bit is no effect if TMx_ASTOP_EN is disabled. When enables, the timer will auto clear the flag of TMx_TOF or TMx_TUF after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
8	rw	**TM36_ASTOP_EN**	Timer auto stop mode enable. When enables, the timer will auto stop after timer counting is overflow or underflow. 0 = Disable 1 = Enable	0x00
7	rw	**TM36_DIR2**	2nd Timer counting direction bit. 0 = Up (Up Counting) 1 = Down (Down Counting)	0x00
6	rw	**TM36_DIR**	Main Timer counting direction bit. This bit cannot update if set PWM center-aligned mode and TM36_EN=1. 0 = Up (Up Counting) 1 = Down (Down Counting)	0x00
5..4	rw	**TM36_MDS**	Timer operation mode select. When selects 'Cascade', both TMx_EN and TMx_EN2 must set the same setting of Enable or Disable. (x : module index) 0x0 = Cascade : 16-bit counter with 16-bit prescaler Mode 0x1 = Separate : Separated two 16-bit counters Mode 0x2 = Full-Counter : 32-bit counter Mode 0x3 = Reserved	0x00
3	-	**Reserved**	Reserved	0x00
2	-	**Reserved**	Reserved	0x00
1	rw	**TM36_EN2**	2nd Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00
0	rw	**TM36_EN**	Main Timer/Counter enable bit. 0 = Disable 1 = Enable	0x00

1.34.6. TM36 Timer control register 1

TM36_CR1	TM36 Timer control register 1		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_CC3B_SEN	TM36_CC2B_SEN	TM36_CC1B_SEN	TM36_CC0B_SEN	TM36_CC3A_SEN	TM36_CC2A_SEN	TM36_CC1A_SEN	TM36_CC0A_SEN
7	6	5	4	3	2	1	0
Reserved				TM36_OVR3_MDS	TM36_OVR2_MDS	TM36_OVR1_MDS	TM36_OVR0_MDS

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	TM36_CC3B_SEN	Timer channel 3 software IC/OC event-B generation enable. When capture mode, this bit is used to trigger falling edge capture event. When PWM mode, this bit is used to set TM36_CF3B flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
14	rw	TM36_CC2B_SEN	Timer channel 2 software IC/OC event-B generation enable. When capture mode, this bit is used to trigger falling edge capture event. When PWM mode, this bit is used to set TM36_CF2B flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
13	rw	TM36_CC1B_SEN	Timer channel 1 software IC/OC event-B generation enable. When capture mode, this bit is used to trigger falling edge capture event. When PWM mode, this bit is used to set TM36_CF1B flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
12	rw	TM36_CC0B_SEN	Timer channel 0 software IC/OC event-B generation enable. When capture mode, this bit is used to trigger falling edge capture event. When PWM mode, this bit is used to set TM36_CF0B flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
11	rw	TM36_CC3A_SEN	Timer channel 3 software IC/OC event-A generation enable. When capture mode, this bit is used to trigger rising edge capture event. When PWM mode, this bit is used to set TM36_CF3A flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
10	rw	TM36_CC2A_SEN	Timer channel 2 software IC/OC event-A generation enable. When capture mode, this bit is used to trigger rising edge capture event. When PWM mode, this bit is used to set TM36_CF2A flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
9	rw	TM36_CC1A_SEN	Timer channel 1 software IC/OC event-A generation enable. When capture mode, this bit is used to trigger rising edge capture event. When PWM mode, this bit is used to set TM36_CF1A flag only. (set by software and clear by hardware) 0 = No-Effect 1 = Enable	0x00
8	rw	TM36_CC0A_SEN	Timer channel 0 software IC/OC event-A generation enable. When capture mode, this bit is used to trigger rising edge capture event. When PWM mode, this bit is used to set TM36_CF0A flag only. (set by software and clear by hardware)	0x00

			0 = No-Effect 1 = Enable	
7..4	-	Reserved	Reserved	0x00
3	rw	TM36_OVR3_MDS	Timer channel 3 capture data buffer overrun mode select 0 = Overwritten (Overwritten by new data) 1 = Keep (Preserved old data)	0x00
2	rw	TM36_OVR2_MDS	Timer channel 2 capture data buffer overrun mode select 0 = Overwritten (Overwritten by new data) 1 = Keep (Preserved old data)	0x00
1	rw	TM36_OVR1_MDS	Timer channel 1 capture data buffer overrun mode select 0 = Overwritten (Overwritten by new data) 1 = Keep (Preserved old data)	0x00
0	rw	TM36_OVR0_MDS	Timer channel 0 capture data buffer overrun mode select 0 = Overwritten (Overwritten by new data) 1 = Keep (Preserved old data)	0x00

1.34.7. TM36 Timer CKO control register

TM36_CKO	TM36 Timer CKO control register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				TM36_CKO_LCK	TM36_CKO_STA	TM36_CKO_SEL	TM36_CKO_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	TM36_CKO_LCK	TM36_CKO_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
2	rw	TM36_CKO_STA	Timer CKO output signal initial state. The bit is written effectively only by written 1 to TM36_CKO_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
1	rw	TM36_CKO_SEL	Timer overflow as CKO output source select. 0 = 2nd : 2nd Timer overflow 1 = Main : Main Timer overflow	0x00
0	rw	TM36_CKO_EN	Timer overflow as CKO output enable. 0 = Disable 1 = Enable	0x00

1.34.8. TM36 repetition counter register

TM36_RCNT	TM36 repetition counter register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
TM36_RARR[7:0]							

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
TM36_RCNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	rw	TM36_RARR	Repetition counter auto-reload value register. This register is used to set the main timer overflow / underflow number or TMx_CKOM pulse number which is as the next updated auto-reload value after the Repetition counter is underflow. When the Repetition counter has been started and counting underflow, the chip will be asserting a RTUF flag.	0x00
15..8	-	Reserved	Reserved	0x00
7..0	rw	TM36_RCNT	Repetition counter register.	0x00

1.34.9. TM36 Timer main counter register

TM36_CNT	TM36 Timer main counter register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_CNT[15:8]							
7	6	5	4	3	2	1	0
TM36_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM36_CNT	Main timer/counter register.	0x0000

1.34.10. TM36 Timer main counter auto-reload value register

TM36_ARR	TM36 Timer main counter auto-reload value register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_ARR[15:8]							
7	6	5	4	3	2	1	0
TM36_ARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM36_ARR	Main timer/counter auto-reload value register. [Two 8bit OC/PWM Mode] for all channels: This register value is limited to 0x00ZZ (ZZ={0x00~0xFF}) [Two 8bit OC/PWM,16bit OC/PWM Mode] for mixed channels: This register value is limited to 0xZZFF (ZZ={0x00~0xFF})	0x0000

1.34.11. TM36 Timer prescaler register

TM36_PSCNT	TM36 Timer prescaler register

Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
TM36_CNTA[15:8]							
23	22	21	20	19	18	17	16
TM36_CNTA[7:0]							
15	14	13	12	11	10	9	8
TM36_PSCNT[15:8]							
7	6	5	4	3	2	1	0
TM36_PSCNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	r	TM36_CNTA	Main timer/counter alias register. This register is the alias of TM36_CNT for read only.	0x0000
15..0	rw	TM36_PSCNT	Timer prescaler or 2nd timer/counter register	0x0000

1.34.12. TM36 Timer prescaler auto-reload register

TM36_PSARR	TM36 Timer prescaler auto-reload register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_PSARR[15:8]							
7	6	5	4	3	2	1	0
TM36_PSARR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM36_PSARR	Timer prescaler or 2nd timer/counter auto-reload value register	0x0000

1.34.13. TM36 Timer capture and compare mode select register

TM36_CCMDS	TM36 Timer capture and compare mode select register		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				TM36_DMA_CC3E	TM36_DMA_CC2E	TM36_DMA_CC1E	TM36_DMA_CC0E
23	22	21	20	19	18	17	16
TM36_DMA_OMDS	Reserved						TM36_OC_LCK
15	14	13	12	11	10	9	8
Reserved	TM36_CC3_MDS[2:0]			Reserved	TM36_CC2_MDS[2:0]		
7	6	5	4	3	2	1	0
Reserved	TM36_CC1_MDS[2:0]			Reserved	TM36_CC0_MDS[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	rw	TM36_DMA_CC3E	Direct memory access enable for IC3. 0 = Disable 1 = Enable	0x00
26	rw	TM36_DMA_CC2E	Direct memory access enable for OC2. 0 = Disable 1 = Enable	0x00
25	rw	TM36_DMA_CC1E	Direct memory access enable for OC1. 0 = Disable 1 = Enable	0x00

24	rw	**TM36_DMA_CC0E**	Direct memory access enable for OC0. 0 = Disable 1 = Enable	0x00
23	rw	**TM36_DMA_OMDS**	Timer output DMA request mode select. When selects ITR, the DMA request is asserted at UEV (update event) active and ITR input event has occurred before. That triggers to update the output compare register TM36_CCnB for the channels those DMA enable bit (TM36_DMA_CCnE, n={0,1,2}) is enabled. When selects UEV, the DMA request is asserted at UEV active only. 0 = UEV : UEV update event only 1 = ITR : both UEV and ITR	0x00
22..17	-	**Reserved**	Reserved	0x00
16	rw	**TM36_OC_LCK**	Timer output compare reload function lock enable bit for all channel. When enables and timer update event is happened, it is locked that the compare preload registers of TM36_CCnB reload to compare shadow buffer registers of TM36_CCnA. Until this bit is disabled, these compare preload registers will update the compare shadow buffer at next timer update event happened. 0 = un-Locked : enable unlocked 1 = Locked : enable locked	0x00
15	-	**Reserved**	Reserved	0x00
14..12	rw	**TM36_CC3_MDS**	Timer channel 3 capture and compare mode select. 0x0 = NOP (No operation) 0x1 = 16bit_IC (Input capture) 0x2 = 16bit_OC (Output compare) 0x3 = 8bitx2_OC (Two 8-bit compare) 0x4 = 16bit_PWM (16bit PWM) 0x5 = 8bitx2_PWM (Two 8bit PWMs)	0x00
11	-	**Reserved**	Reserved	0x00
10..8	rw	**TM36_CC2_MDS**	Timer channel 2 capture and compare mode select. 0x0 = NOP (No operation) 0x1 = 16bit_IC (Input capture) 0x2 = 16bit_OC (Output compare) 0x3 = 8bitx2_OC (Two 8-bit compare) 0x4 = 16bit_PWM (16bit PWM) 0x5 = 8bitx2_PWM (Two 8bit PWMs) 0x6 = 16bit_PWM_DTG (16bit PWM with DTG) 0x7 = 8bitx2_PWM_DTG (Two 8bit PWMs with DTG)	0x00
7	-	**Reserved**	Reserved	0x00
6..4	rw	**TM36_CC1_MDS**	Timer channel 1 capture and compare mode select. 0x0 = NOP (No operation) 0x1 = 16bit_IC (Input capture) 0x2 = 16bit_OC (Output compare) 0x3 = 8bitx2_OC (Two 8-bit compare) 0x4 = 16bit_PWM (16bit PWM) 0x5 = 8bitx2_PWM (Two 8bit PWMs) 0x6 = 16bit_PWM_DTG (16bit PWM with DTG) 0x7 = 8bitx2_PWM_DTG (Two 8bit PWMs with DTG)	0x00
3	-	**Reserved**	Reserved	0x00
2..0	rw	**TM36_CC0_MDS**	Timer channel 0 capture and compare mode select. 0x0 = NOP (No operation) 0x1 = 16bit_IC (Input capture) 0x2 = 16bit_OC (Output compare) 0x3 = 8bitx2_OC (Two 8-bit compare) 0x4 = 16bit_PWM (16bit PWM) 0x5 = 8bitx2_PWM (Two 8bit PWMs) 0x6 = 16bit_PWM_DTG (16bit PWM with DTG) 0x7 = 8bitx2_PWM_DTG (Two 8bit PWMs with DTG)	0x00

1.34.14. TM36 Timer input capture control register

TM36_ICCR	TM36 Timer input capture control register		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
TM36_IC3_TRGS[1:0]		TM36_IC2_TRGS[1:0]		TM36_IC1_TRGS[1:0]		TM36_IC0_TRGS[1:0]	
15	14	13	12	11	10	9	8
Reserved		TM36_IC3_MUX[1:0]		Reserved		TM36_IC2_MUX[1:0]	
7	6	5	4	3	2	1	0
Reserved		TM36_IC1_MUX[1:0]		Reserved		TM36_IC0_MUX[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..22	rw	TM36_IC3_TRGS	Timer channel 3 input trigger edge select. 0x0 = Disable : disable capture data 0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	0x00
21..20	rw	TM36_IC2_TRGS	Timer channel 2 input trigger edge select. 0x0 = Disable : disable capture data 0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	0x00
19..18	rw	TM36_IC1_TRGS	Timer channel 1 input trigger edge select. 0x0 = Disable : disable capture data 0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	0x00
17..16	rw	TM36_IC0_TRGS	Timer channel 0 input trigger edge select. 0x0 = Disable : disable capture data 0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	0x00
15..14	-	Reserved	Reserved	0x00
13..12	rw	TM36_IC3_MUX	Timer channel 3 input Mux select for input capture. 0x0 = IC30 : TM36_IC3 0x1 = IC31 : TM36_ITR 0x2 = IC32 : Reserved 0x3 = IC33 : TM36_XOR	0x00
11..10	-	Reserved	Reserved	0x00
9..8	rw	TM36_IC2_MUX	Timer channel 2 input Mux select for input capture. 0x0 = IC20 : TM36_IC2 0x1 = IC21 : TM36_ITR 0x2 = IC22 : Reserved 0x3 = IC23 : Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5..4	rw	TM36_IC1_MUX	Timer channel 1 input Mux select for input capture. 0x0 = IC10 : TM36_IC1 0x1 = IC11 : TM36_ITR 0x2 = IC12 : CMP1_OUT 0x3 = IC13 : Reserved	0x00
3..2	-	Reserved	Reserved	0x00
1..0	rw	TM36_IC0_MUX	Timer channel 0 input Mux select for input capture. 0x0 = IC00 : TM36_IC0 0x1 = IC01 : TM36_ITR 0x2 = IC02 : CMP0_OUT 0x3 = IC03 : TM36_XOR	0x00

1.34.15. TM36 Timer output compare state register

TM36_OSCR	TM36 Timer output compare state register		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved					Reserved	Reserved	Reserved
15	14	13	12	11	10	9	8
TM36_OS3H_LCK	TM36_OS2H_LCK	TM36_OS1H_LCK	TM36_OS0H_LCK	TM36_OS3H_STA	TM36_OS2H_STA	TM36_OS1H_STA	TM36_OS0H_STA
7	6	5	4	3	2	1	0
TM36_OS3_LCK	TM36_OS2_LCK	TM36_OS1_LCK	TM36_OS0_LCK	TM36_OS3_STA	TM36_OS2_STA	TM36_OS1_STA	TM36_OS0_STA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..19	-	Reserved	Reserved	0x00
18	-	Reserved	Reserved	0x00
17	-	Reserved	Reserved	0x00
16	-	Reserved	Reserved	0x00
15	rw	TM36_OS3H_LCK	TM36_OS3H_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. TM36_OS3H_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
14	rw	TM36_OS2H_LCK	TM36_OS2H_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access.TM36_OS2H_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
13	rw	TM36_OS1H_LCK	TM36_OS1H_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access.TM36_OS1H_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
12	rw	TM36_OS0H_LCK	TM36_OS0H_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access.TM36_OS0H_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
11	rw	TM36_OS3H_STA	Timer channel 3 OC compare-H output signal initial state for two 8-Bit comparator mode 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
10	rw	TM36_OS2H_STA	Timer channel 2 OC compare-H output signal initial state for two 8-Bit comparator mode 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
9	rw	TM36_OS1H_STA	Timer channel 1 OC compare-H output signal initial state for two 8-Bit comparator mode 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
8	rw	TM36_OS0H_STA	Timer channel 0 OC compare-H output signal initial state for two 8-Bit comparator mode. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
7	rw	TM36_OS3_LCK	TM36_OS3_STA register write access protected control. When	0x00

			locked, disables the register bit write access. Hardware auto clear after register write access. TM36_OS3_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	
6	rw	**TM36_OS2_LCK**	TM36_OS2_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. TM36_OS2_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
5	rw	**TM36_OS1_LCK**	TM36_OS1_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. TM36_OS1_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
4	rw	**TM36_OS0_LCK**	TM36_OS0_STA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. TM36_OS0_STA is written effectively only by written 1 to this bit simultaneously. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
3	rw	**TM36_OS3_STA**	Timer channel 3 OC compare/compare-L output signal initial state. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
2	rw	**TM36_OS2_STA**	Timer channel 2 OC compare/compare-L output signal initial state. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
1	rw	**TM36_OS1_STA**	Timer channel 1 OC compare/compare-L output signal initial state. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
0	rw	**TM36_OS0_STA**	Timer channel 0 OC compare/compare-L output signal initial state. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00

1.34.16. TM36 Timer output compare control register 0

TM36_OCCR0	TM36 Timer output compare control register 0		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	Reserved	Reserved	Reserved	Reserved			TM36_OC2N_OE
23	22	21	20	19	18	17	16
Reserved			TM36_OC1N_OE	Reserved			TM36_OC0N_OE
15	14	13	12	11	10	9	8
Reserved			TM36_OC3_OE	Reserved			TM36_OC2_OE
7	6	5	4	3	2	1	0
Reserved	TM36_OC1_OE2	TM36_OC1_OE1	TM36_OC1_OE0	Reserved	TM36_OC0_OE2	TM36_OC0_OE1	TM36_OC0_OE0

Bit	Attr	Bit Name	Description	Reset
31	-	**Reserved**	Reserved	0x00
30	-	**Reserved**	Reserved	0x00
29	-	**Reserved**	Reserved	0x00
28	-	**Reserved**	Reserved	0x00
27..25	-	**Reserved**	Reserved	0x00

24	rw	TM36_OC2N_OE	Timer channel 2 OC2N (complement) line output enable. 0 = Disable (output by TM36_BK2N_STA setting) 1 = Enable	0x00
23..21	-	Reserved	Reserved	0x00
20	rw	TM36_OC1N_OE	Timer channel 1 OC1N (complement) line output enable. 0 = Disable (output by TM36_BK1N_STA setting) 1 = Enable	0x00
19..17	-	Reserved	Reserved	0x00
16	rw	TM36_OC0N_OE	Timer channel 0 OC0N (complement) line output enable. 0 = Disable (output by TM36_BK0N_STA setting) 1 = Enable	0x00
15..13	-	Reserved	Reserved	0x00
12	rw	TM36_OC3_OE	Timer channel 3 OC line output enable. 0 = Disable (output by TM36_BK3_STA setting) 1 = Enable	0x00
11..9	-	Reserved	Reserved	0x00
8	rw	TM36_OC2_OE	Timer channel 2 OC line output enable. 0 = Disable (output by TM36_BK2_STA setting) 1 = Enable	0x00
7	-	Reserved	Reserved	0x00
6	rw	TM36_OC1_OE2	Timer channel 1 OC line-2 output enable. 0 = Disable (output by TM36_BK1_STA setting) 1 = Enable	0x00
5	rw	TM36_OC1_OE1	Timer channel 1 OC line-1 output enable. 0 = Disable (output by TM36_BK1_STA setting) 1 = Enable	0x00
4	rw	TM36_OC1_OE0	Timer channel 1 OC line-0 output enable. 0 = Disable (output by TM36_BK1_STA setting) 1 = Enable	0x00
3	-	Reserved	Reserved	0x00
2	rw	TM36_OC0_OE2	Timer channel 0 OC line-2 output enable. 0 = Disable (output by TM36_BK0_STA setting) 1 = Enable	0x00
1	rw	TM36_OC0_OE1	Timer channel 0 OC line-1 output enable. 0 = Disable (output by TM36_BK0_STA setting) 1 = Enable	0x00
0	rw	TM36_OC0_OE0	Timer channel 0 OC line-0 output enable. 0 = Disable (output by TM36_BK0_STA setting) 1 = Enable	0x00

1.34.17. TM36 Timer output compare control register 1

TM36_OCCR1	TM36 Timer output compare control register 1		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	TM36_ODLY_SEL	Reserved	TM36_POE_SW	Reserved	TM36_POE_EN2	TM36_POE_EN1	TM36_POE_EN0
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved	TM36_OC1_POE2	TM36_OC1_POE1	TM36_OC1_POE0	Reserved	TM36_OC0_POE2	TM36_OC0_POE1	TM36_OC0_POE0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved					TM36_OC2N_INV	TM36_OC1N_INV	TM36_OC0N_INV
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TM36_OC3H_INV	TM36_OC2H_INV	TM36_OC1H_INV	TM36_OC0H_INV	TM36_OC3_INV	TM36_OC2_INV	TM36_OC1_INV	TM36_OC0_INV

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	TM36_ODLY_SEL	Timer output delay mode select. When selects '0Step', the channel-0,1,2,3 output are normal and no delay. When selects '1Step', the channel-0,1,2,3 output will be separated delayed 0,1,2,3 step unit delay time.	0x00

			0x0 = 0Step 0x1 = 1Step	
29	-	**Reserved**	Reserved	0x00
28	w	**TM36_POE_SW**	Timer output enable registers preload software enable bit. Refer the TM36_OCn_POE[2:0] (n={0,1}) registers for the output enable registers detail descriptions. (set by software and clear by hardware) 0 = Disable 1 = Enable	0x00
27	-	**Reserved**	Reserved	0x00
26	rw	**TM36_POE_EN2**	Timer OC preload enable bit for output enable preload register control. This bit is used to enable INT_PD input. 0 = Disable 1 = Enable	0x00
25	rw	**TM36_POE_EN1**	Timer OC preload enable bit for output enable preload register control. This bit is used to enable INT_PB input. 0 = Disable 1 = Enable	0x00
24	rw	**TM36_POE_EN0**	Timer OC preload enable bit for output enable preload register control. This bit is used to enable 3-line XOR input. 0 = Disable 1 = Enable	0x00
23	-	**Reserved**	Reserved	0x00
22	rw	**TM36_OC1_POE2**	Timer channel 1 OC line-2 output enable preload register bit. This bit will load into TM36_OC1_OE2 register when the preload event happened. 0 = Disable 1 = Enable	0x00
21	rw	**TM36_OC1_POE1**	Timer channel 1 OC line-1 output enable preload register bit. This bit will load into TM36_OC1_OE1 register when the preload event happened. 0 = Disable 1 = Enable	0x00
20	rw	**TM36_OC1_POE0**	Timer channel 1 OC line-0 output enable preload register bit. This bit will load into TM36_OC1_OE0 register when the preload event happened. 0 = Disable 1 = Enable	0x00
19	-	**Reserved**	Reserved	0x00
18	rw	**TM36_OC0_POE2**	Timer channel 0 OC line-2 output enable preload register bit. This bit will load into TM36_OC0_OE2 register when the preload event happened. 0 = Disable 1 = Enable	0x00
17	rw	**TM36_OC0_POE1**	Timer channel 0 OC line-1 output enable preload register bit. This bit will load into TM36_OC0_OE1 register when the preload event happened. 0 = Disable 1 = Enable	0x00
16	rw	**TM36_OC0_POE0**	Timer channel 0 OC line-0 output enable preload register bit. This bit will load into TM36_OC0_OE0 register when the preload event happened. 0 = Disable 1 = Enable	0x00
15..11	-	**Reserved**	Reserved	0x00
10	rw	**TM36_OC2N_INV**	Timer channel 2 complement output inverse enable. 0 = Disable 1 = Enable	0x00
9	rw	**TM36_OC1N_INV**	Timer channel 1 complement output inverse enable. 0 = Disable 1 = Enable	0x00

8	rw	TM36_OC0N_INV	Timer channel 0 complement output inverse enable. 0 = Disable 1 = Enable	0x00
7	rw	TM36_OC3H_INV	Timer channel 3 High output inverse enable. 0 = Disable 1 = Enable	0x00
6	rw	TM36_OC2H_INV	Timer channel 2 High output inverse enable. 0 = Disable 1 = Enable	0x00
5	rw	TM36_OC1H_INV	Timer channel 1 High output inverse enable. 0 = Disable 1 = Enable	0x00
4	rw	TM36_OC0H_INV	Timer channel 0 High output inverse enable. 0 = Disable 1 = Enable	0x00
3	rw	TM36_OC3_INV	Timer channel 3 output inverse enable. 0 = Disable 1 = Enable	0x00
2	rw	TM36_OC2_INV	Timer channel 2 output inverse enable. 0 = Disable 1 = Enable	0x00
1	rw	TM36_OC1_INV	Timer channel 1 output inverse enable. 0 = Disable 1 = Enable	0x00
0	rw	TM36_OC0_INV	Timer channel 0 output inverse enable. 0 = Disable 1 = Enable	0x00

1.34.18. TM36 Timer PWM and DTG control register

TM36_PWM	TM36 Timer PWM and DTG control register		
Offset Address :	0x44	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_DTG_DY[7:0]							
7	6	5	4	3	2	1	0
Reserved						TM36_PWM_MDS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	rw	TM36_DTG_DY	Timer output DTG dead-time delay(CK_DTG clock time base) for all channels. Value 0 indicates disabled.	0x00
7..2	-	Reserved	Reserved	0x00
1..0	rw	TM36_PWM_MDS	Timer OC0/1/2/3 PWM mode select. 0x0 = Edge Left-aligned 0x1 = Center-aligned 0x2 = Reserved 0x3 = Reserved	0x00

1.34.19. TM36 Timer break and stop control register

TM36_BS	TM36 Timer break and stop control register		
Offset Address :	0x48	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	TM36_STP2N_STA	TM36_STP1N_STA	TM36_STP0N_STA	TM36_STP3_STA	TM36_STP2_STA	TM36_STP1_STA	TM36_STP0_STA

23	22	21	20	19	18	17	16
TM36_BK3_CTL	TM36_BK2_CTL	TM36_BK1_CTL	TM36_BK0_CTL	Reserved	TM36_BKI_EN2	TM36_BKI_EN1	TM36_BKI_EN0
15	14	13	12	11	10	9	8
TM36_BKE_EN7	TM36_BKE_EN6	TM36_BKE_EN5	TM36_BKE_EN4	TM36_BKE_EN3	TM36_BKE_EN2	TM36_BKE_EN1	TM36_BKE_EN0
7	6	5	4	3	2	1	0
TM36_BKSW_EN	Reserved	Reserved	TM36_BK_MDS	TM36_BK_EN3	Reserved		TM36_BK_EN

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	rw	TM36_STP2N_STA	Timer BK input active or stop condition output OC2N state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
29	rw	TM36_STP1N_STA	Timer BK input active or stop condition output OC1N state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
28	rw	TM36_STP0N_STA	Timer BK input active or stop condition output OC0N state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
27	rw	TM36_STP3_STA	Timer BK input active or stop condition output OC3 state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
26	rw	TM36_STP2_STA	Timer BK input active or stop condition output OC2 state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
25	rw	TM36_STP1_STA	Timer BK input active or stop condition output OC1 state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
24	rw	TM36_STP0_STA	Timer BK input active or stop condition output OC0 state select. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
23	rw	TM36_BK3_CTL	Timer OC3 output switch control when break event happened. When selects 'Stop' and the event is happened, the output is switched to the stop state setting in TM36_STP3_STA. 0 = Stop (Switch to stop state register setting) 1 = Hold (hold the output state)	0x00
22	rw	TM36_BK2_CTL	Timer OC2 output switch control when break event happened. When selects 'Stop' and the event is happened, the output is switched to the stop state setting in TM36_STP2_STA and TM36_STP2N_STA. 0 = Stop (Switch to stop state register setting) 1 = Hold (hold the output state)	0x00
21	rw	TM36_BK1_CTL	Timer OC1 output switch control when break event happened. When selects 'Stop' and the event is happened, the output is switched to the stop state setting in TM36_STP1_STA and TM36_STP1N_STA. 0 = Stop (Switch to stop state register setting) 1 = Hold (hold the output state)	0x00
20	rw	TM36_BK0_CTL	Timer OC0 output switch control when break event happened. When selects 'Stop' and the event is happened, the output is switched to the stop state setting in TM36_STP0_STA and TM36_STP0N_STA. 0 = Stop (Switch to stop state register setting) 1 = Hold (hold the output state)	0x00

19	-	Reserved	Reserved	0x00
18	rw	TM36_BKI_EN2	Timer Break internal input channels' enable bit. This bit is using for CPU LOCKUP output event input. 0 = Disable 1 = Enable	0x00
17	rw	TM36_BKI_EN1	Timer Break internal input channels' enable bit. This bit is reserved for future using. 0 = Disable 1 = Enable	0x00
16	rw	TM36_BKI_EN0	Timer Break internal input channels' enable bit. This bit is using for missing clock detect(MCD) event input. 0 = Disable 1 = Enable	0x00
15	rw	TM36_BKE_EN7	Timer Break external input channels' enable bit. This bit is reserved. 0 = Disable 1 = Enable	0x00
14	rw	TM36_BKE_EN6	Timer Break external input channels' enable bit. This bit is reserved. 0 = Disable 1 = Enable	0x00
13	rw	TM36_BKE_EN5	Timer Break external input channels' enable bit. This bit is using for CMP1_OUT signal input. 0 = Disable 1 = Enable	0x00
12	rw	TM36_BKE_EN4	Timer Break external input channels' enable bit. This bit is using for CMP0_OUT signal input. 0 = Disable 1 = Enable	0x00
11	rw	TM36_BKE_EN3	Timer Break external input channels' enable bit. This bit is using for ADC0_OUT signal input. 0 = Disable 1 = Enable	0x00
10	rw	TM36_BKE_EN2	Timer Break external input channels' enable bit. This bit is using for INT_PB signal input. 0 = Disable 1 = Enable	0x00
9	rw	TM36_BKE_EN1	Timer Break external input channels' enable bit. This bit is using for INT_BOD1 signal input. 0 = Disable 1 = Enable	0x00
8	rw	TM36_BKE_EN0	Timer Break external input channels' enable bit. This bit is using for TM36_BK0 signal input. 0 = Disable 1 = Enable	0x00
7	rw	TM36_BKSW_EN	Timer software break input generation enable. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	rw	TM36_BK_MDS	Timer break event input control mode select. 0 = Latch mode 1 = Cycle by cycle	0x00
3	rw	TM36_BK_EN3	Timer Break Input enable for OC3. (output state stop or reset) 0 = Disable 1 = Enable	0x00
2..1	-	Reserved	Reserved	0x00
0	rw	TM36_BK_EN	Timer Break Input enable for OC[2:0]. (output state stop or reset) 0 = Disable 1 = Enable	0x00

1.34.20. TM36 Timer capture and compare register 0A

TM36_CC0A	TM36 Timer capture and compare register 0A		
Offset Address :	0x50	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_CC0A[15:8]							
7	6	5	4	3	2	1	0
TM36_CC0A[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM36_CC0A	TM36 Timer capture and compare register 0A for channel 0. When the channel is configured as input capture mode, this register is used to capture the counter value of input trigger signal : (1) first capture data for single edge (2) rising edge capture data for dual edge. When the channel is configured as output compare/PWM mode, this register is used as the compared shadow register for Timer output compare and will be copied from R_TM36_CC0B when TM36_CC0B was written. When the channel is configured as output two 8-bit compare/PWM mode, this register is separated to low 8-bt compared shadow register for compare-L path and high 8-bt compared shadow register for compare-H path. When both TM36_CC0A and TM36_CC0B value is equal TM36_ARR or 0x0000 in central-align mode, the output high and low width are 0x10000 clocks' width.	0x0000

1.34.21. TM36 Timer capture and compare register 0B

TM36_CC0B	TM36 Timer capture and compare register 0B		
Offset Address :	0x54	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_CC0B[15:8]							
7	6	5	4	3	2	1	0
TM36_CC0B[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM36_CC0B	TM36 Timer capture and compare register 0B for channel 0. When the channel is configured as input capture mode, this register is used to capture the counter value of input trigger signal : (1) 2nd capture data for single edge (2) falling edge capture data for dual edge. When the channel is configured as output compare/PWM mode, this register is used as the compared preload register for software setting and will copy the value to TM36_CC0A. When the channel is configured as output two 8-bit compare/PWM mode, this register is separated to low 8-bt compared preload register for compare-L path and high 8-bt compared preload register for compare-H path.	0x0000

1.34.22. TM36 Timer capture and compare register 1A

TM36_CC1A	TM36 Timer capture and compare register 1A		
Offset Address :	0x58	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_CC1A[15:8]							
7	6	5	4	3	2	1	0
TM36_CC1A[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM36_CC1A	TM36 Timer capture and compare register 1A for channel 1. Refer to the register descriptions of TM36_CC0A for detail descriptions.	0x0000

1.34.23. TM36 Timer capture and compare register 1B

TM36_CC1B	TM36 Timer capture and compare register 1B		
Offset Address :	0x5c	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_CC1B[15:8]							
7	6	5	4	3	2	1	0
TM36_CC1B[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM36_CC1B	TM36 Timer capture and compare register 1B for channel 1. Refer to the register descriptions of TM36_CC0B for detail descriptions.	0x0000

1.34.24. TM36 Timer capture and compare register 2A

TM36_CC2A	TM36 Timer capture and compare register 2A		
Offset Address :	0x60	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_CC2A[15:8]							
7	6	5	4	3	2	1	0
TM36_CC2A[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM36_CC2A	TM36 Timer capture and compare register 2A for channel 2. Refer to the register descriptions of TM36_CC0A for detail	0x0000

			descriptions.	

1.34.25. TM36 Timer capture and compare register 2B

TM36_CC2B	TM36 Timer capture and compare register 2B		
Offset Address :	0x64	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_CC2B[15:8]							
7	6	5	4	3	2	1	0
TM36_CC2B[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM36_CC2B	TM36 Timer capture and compare register 2B for channel 2. Refer to the register descriptions of TM36_CC0B for detail descriptions.	0x0000

1.34.26. TM36 Timer capture and compare register 3A

TM36_CC3A	TM36 Timer capture and compare register 3A		
Offset Address :	0x68	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_CC3A[15:8]							
7	6	5	4	3	2	1	0
TM36_CC3A[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM36_CC3A	TM36 Timer capture and compare register 3A for channel 3. Refer to the register descriptions of TM36_CC0A for detail descriptions.	0x0000

1.34.27. TM36 Timer capture and compare register 3B

TM36_CC3B	TM36 Timer capture and compare register 3B		
Offset Address :	0x6c	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
TM36_CC3B[15:8]							
7	6	5	4	3	2	1	0
TM36_CC3B[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	TM36_CC3B	Timer TM36 capture and compare register 3B for channel 3.	0x0000

			Refer to the register descriptions of TM36_CC0B for detail descriptions.	

1.34.28. TM36 Register Map

TM36 Register Map Register Number = 27

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	TM36_STA	Reserved								Reserved			TM36_RTUF	TM36_QPEF	TM36_IDXF	Reserved	TM36_DIRCF	TM36_CF3B	TM36_CF2B	TM36_CF1B	TM36_CF0B	TM36_CF3A	TM36_CF2A	TM36_CF1A	TM36_CF0A	TM36_TUF2	TM36_TUF	TM36_TOF2	TM36_TOF	TM36_EXF	TM36_BKF	Reserved	TM36_DIRF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	TM36_INT	Reserved								Reserved			TM36_RTU_IE	TM36_QPE_IE	TM36_IDX_IE	Reserved	TM36_DIRC_IE	Reserved				TM36_CC3_IE	TM36_CC2_IE	TM36_CC1_IE	TM36_CC0_IE	Reserved		TM36_TIE2	TM36_TIE	TM36_EXIE	TM36_BKIE	Reserved	TM36_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	TM36_CLK	Reserved								Reserved			TM36_RC_CKS	Reserved		TM36_DTG_DIV [1:0]		Reserved		TM36_CKI_DIV [1:0]		Reserved		TM36_CKI_SEL [1:0]		TM36_CKS2_SEL	TM36_CKS_SEL	TM36_CKE_SEL [1:0]		Reserved	Reserved	Reserved	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	TM36_TRG	TM36_GT2_SW	TM36_GT_SW	TM36_RST2_SW	TM36_RST_SW	Reserved		TM36_TRGO_INV	TM36_TRGO_SW	TM36_UEV_SEL [1:0]		TM36_IDX_MDS [1:0]		TM36_IDX_EN	TM36_QEI_MDS [2:0]			TM36_TRGO_MDS [3:0]				Reserved	TM36_ITR_MUX [2:0]			TM36_TRG_MUX [1:0]		TM36_TRGI2_MDS [2:0]			TM36_TRGI_MDS [2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	TM36_CR0	Reserved								Reserved						TM36_RC_STP	TM36_RC_EN	TM36_UEX_EN	TM36_USW_EN	TM36_DIR_INV	TM36_UEV_DIS	TM36_EX_INV	TM36_EX_EN	TM36_ACLEAR_EN	TM36_ASTOP_EN	TM36_DIR2	TM36_DIR	TM36_MDS[1:0]		Reserved	Reserved	TM36_EN2	TM36_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	TM36_CR1	Reserved																TM36_CC3B_SEN	TM36_CC2B_SEN	TM36_CC1B_SEN	TM36_CC0B_SEN	TM36_CC3A_SEN	TM36_CC2A_SEN	TM36_CC1A_SEN	TM36_CC0A_SEN	Reserved				TM36_OVR3_MDS	TM36_OVR2_MDS	TM36_OVR1_MDS	TM36_OVR0_MDS
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	TM36_CKO	Reserved																Reserved								Reserved				TM36_CKO_LCK	TM36_CKO_STA	TM36_CKO_SEL	TM36_CKO_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	TM36_RCNT	Reserved								TM36_RARR[7:0]								Reserved								TM36_RCNT[7:0]							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x20	TM36_CNT	Reserved																TM36_CNT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	TM36_ARR	Reserved																TM36_ARR[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	TM36_PSCNT	TM36_CNTA[15:0]																TM36_PSCNT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	TM36_PSARR	Reserved																TM36_PSARR[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	TM36_CCMDS	Reserved				TM36_DMA_CC3E	TM36_DMA_CC2E	TM36_DMA_CC1E	TM36_DMA_CC0E	TM36_DMA_OMDS	Reserved						TM36_OC_LCK	Reserved	TM36_CC3_MDS [2:0]			Reserved	TM36_CC2_MDS [2:0]			Reserved	TM36_CC1_MDS [2:0]			Reserved	TM36_CC0_MDS [2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	TM36_ICCR	Reserved								TM36_IC3_TRGS [1:0]		TM36_IC2_TRGS [1:0]		TM36_IC1_TRGS [1:0]		TM36_IC0_TRGS [1:0]		Reserved		TM36_IC3_MUX [1:0]		Reserved		TM36_IC2_MUX [1:0]		Reserved		TM36_IC1_MUX [1:0]		Reserved		TM36_IC0_MUX [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	TM36_OSCR	Reserved								Reserved					Reserved	Reserved	Reserved	TM36_OS3H_LCK	TM36_OS2H_LCK	TM36_OS1H_LCK	TM36_OS0H_LCK	TM36_OS3H_STA	TM36_OS2H_STA	TM36_OS1H_STA	TM36_OS0H_STA	TM36_OS3_LCK	TM36_OS2_LCK	TM36_OS1_LCK	TM36_OS0_LCK	TM36_OS3_STA	TM36_OS2_STA	TM36_OS1_STA	TM36_OS0_STA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	TM36_OCCR0	Reserved	Reserved	Reserved	Reserved	Reserved			TM36_OC2N_OE	Reserved			TM36_OC1N_OE	Reserved			TM36_OC0N_OE	Reserved			TM36_OC3_OE	Reserved			TM36_OC2_OE	Reserved	TM36_OC1_OE2	TM36_OC1_OE1	TM36_OC1_OE0	Reserved	TM36_OC0_OE2	TM36_OC0_OE1	TM36_OC0_OE0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	TM36_OCCR1	Reserved	TM36_ODLY_SEL	Reserved	TM36_POE_SW	Reserved	TM36_POE_EN2	TM36_POE_EN1	TM36_POE_EN0	Reserved	TM36_OC1_POE2	TM36_OC1_POE1	TM36_OC1_POE0	Reserved	TM36_OC0_POE2	TM36_OC0_POE1	TM36_OC0_POE0	Reserved					TM36_OC2N_INV	TM36_OC1N_INV	TM36_OC0N_INV	TM36_OC3H_INV	TM36_OC2H_INV	TM36_OC1H_INV	TM36_OC0H_INV	TM36_OC3_INV	TM36_OC2_INV	TM36_OC1_INV	TM36_OC0_INV
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x44	TM36_PWM	Reserved																TM36_DTG_DY [7:0]								Reserved						TM36_PWM_MDS [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x48	TM36_BS	Reserved	TM36_STP2N_STA	TM36_STP1N_STA	TM36_STP0N_STA	TM36_STP3_STA	TM36_STP2_STA	TM36_STP1_STA	TM36_STP0_STA	TM36_BK3_CTL	TM36_BK2_CTL	TM36_BK1_CTL	TM36_BK0_CTL	Reserved	TM36_BKI_EN2	TM36_BKI_EN1	TM36_BKI_EN0	TM36_BKE_EN7	TM36_BKE_EN6	TM36_BKE_EN5	TM36_BKE_EN4	TM36_BKE_EN3	TM36_BKE_EN2	TM36_BKE_EN1	TM36_BKE_EN0	TM36_BKSW_EN	Reserved	Reserved	TM36_BK_MDS	TM36_BK_EN3	Reserved		TM36_BK_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	TM36_CC0A	Reserved																TM36_CC0A[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x54	TM36_CC0B	Reserved																TM36_CC0B[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x58	TM36_CC1A	Reserved																TM36_CC1A[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x5c	TM36_CC1B	Reserved																TM36_CC1B[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x60	TM36_CC2A	Reserved																TM36_CC2A[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x64	TM36_CC2B	Reserved																TM36_CC2B[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x68	TM36_CC3A	Reserved																TM36_CC3A[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x6c	TM36_CC3B	Reserved																TM36_CC3B[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.35. ADC0 Control Registers

ADC0 Control	(ADC0) Analog-to-Digital Converter Control Module-0
Base Address :	0x5B000000

1.35.1. ADC0 status register

ADC0_STA	ADC0 status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				Reserved	Reserved	Reserved	ADC0_POF
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
ADC0_SUMOVRF	ADC0_SUMCF	ADC0_SUMOF	Reserved	Reserved	ADC0_WDHF	ADC0_WDIF	ADC0_WDLF
7	6	5	4	3	2	1	0
ADC0_OVRF	Reserved	ADC0_ESCNVF	Reserved	ADC0_E1CNVF	ADC0_ESMPF	Reserved	ADC0_SOCF

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27	-	Reserved	Reserved	0x00
26	-	Reserved	Reserved	0x00
25	-	Reserved	Reserved	0x00
24	rw	ADC0_POF	ADC PGA offset calibration status bit.	0x00
23..16	-	Reserved	Reserved	0x00
15	rw	ADC0_SUMOVRF	ADC data sum-0,1,2 register overrun flag. When clears this flag, also it clears all the ADC0_SUMn_OVRF(n=0~3) flags. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
14	rw	ADC0_SUMCF	ADC data sum-0,1,2 accumulation complete flag. When clears this flag, also it clears all the ADC0_SUMn_CF(n=0~3) flags. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
13	rw	ADC0_SUMOF	ADC data sum-0,1,2 accumulation overflow or underflow flag. When clears this flag, also it clears all the ADC0_SUMn_OF (n=0~3) and ADC0_SUMn_UF (n=0~3) flags. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
12	-	Reserved	Reserved	0x00
11	-	Reserved	Reserved	0x00
10	rw	ADC0_WDHF	ADC voltage window detect outside high event flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
9	rw	ADC0_WDIF	ADC voltage window detect inside event flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
8	rw	ADC0_WDLF	ADC voltage window detect outside low event flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
7	rw	ADC0_OVRF	ADC conversion overrun event flag. When clears this flag, also it clears all the ADC0_DATn_OVRF(n=0~3) flags. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred)	0x00

			1 = Happened (Event happened)	
6	-	Reserved	Reserved	0x00
5	rw	ADC0_ESCNVF	ADC channel scan conversion end flag. This bit is set at the end of the conversion of a sequence channel scan. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	-	Reserved	Reserved	0x00
3	rw	ADC0_E1CNVF	ADC one-time conversion end flag. This bit is set at the end of each conversion of a channel and a new data result is available in the ADC0_DAT0. When clears this flag, also it clears the ADC0_DAT0_CF flags and ready to receive next data. (set by hardware and clear by software write 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	ADC0_ESMPF	ADC sampling end flag. This bit is set at the end of the sampling phase. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	-	Reserved	Reserved	0x00
0	r	ADC0_SOCF	ADC conversion status. This bit will be active during ADC start conversion to ADC conversion ready period. (set and clear by hardware)	0x00

1.35.2. ADC0 interrupt enable register

ADC0_INT	ADC0 interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
ADC0_SUMOVR_IE	ADC0_SUMC_IE	ADC0_SUMO_IE	Reserved		ADC0_WDH_IE	ADC0_WDI_IE	ADC0_WDL_IE
7	6	5	4	3	2	1	0
ADC0_OVR_IE	Reserved	ADC0_ESCNV_IE	Reserved	ADC0_E1CNV_IE	ADC0_ESMP_IE	Reserved	ADC0_IEA

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	ADC0_SUMOVR_IE	ADC data sum-0,1,2 overrun event interrupt enable. 0 = Disable 1 = Enable	0x00
14	rw	ADC0_SUMC_IE	ADC data sum-0,1,2 accumulation complete interrupt enable. 0 = Disable 1 = Enable	0x00
13	rw	ADC0_SUMO_IE	ADC data sum-0,1,2 accumulation overflow or underflow interrupt enable. 0 = Disable 1 = Enable	0x00
12..11	-	Reserved	Reserved	0x00
10	rw	ADC0_WDH_IE	ADC voltage window detect outside high event interrupt enable. 0 = Disable 1 = Enable	0x00
9	rw	ADC0_WDI_IE	ADC voltage window detect inside event interrupt enable. 0 = Disable 1 = Enable	0x00
8	rw	ADC0_WDL_IE	ADC voltage window detect outside low event interrupt enable.	0x00

			0 = Disable 1 = Enable	
7	rw	ADC0_OVR_IE	ADC conversion overrun event interrupt enable. 0 = Disable 1 = Enable	0x00
6	-	Reserved	Reserved	0x00
5	rw	ADC0_ESCNV_IE	ADC channel scan conversion end interrupt enable. 0 = Disable 1 = Enable	0x00
4	-	Reserved	Reserved	0x00
3	rw	ADC0_E1CNV_IE	ADC one-time conversion end interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	ADC0_ESMP_IE	ADC sampling end interrupt enable. 0 = Disable 1 = Enable	0x00
1	-	Reserved	Reserved	0x00
0	rw	ADC0_IEA	ADC interrupt all enable. When disables, the ADC global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.35.3. ADC0 clock source register

ADC0_CLK	ADC0 clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
ADC0_SCNT[3:0]				Reserved		ADC0_CK_SDIV[1:0]	
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		ADC0_CK_DLY[1:0]		ADC0_CK_DIV2[1:0]		ADC0_CK_SEL2[1:0]	
7	6	5	4	3	2	1	0
Reserved		ADC0_CK_DIV[1:0]		Reserved		Reserved	Reserved

Bit	Attr	Bit Name	Description	Reset
31..28	rw	ADC0_SCNT	ADC power-on start up counter. This register is only valid when auto power-off mode is enabled (ADC0_AUTOFF_EN=1). The value range 0~15 is indicated counter inital value 0~15.	0x00
27..26	-	Reserved	Reserved	0x00
25..24	rw	ADC0_CK_SDIV	ADC power-on start up counter clock divider. This divider is used to divide the input clock CK_ADCx_PR to output as the start up counter clock. 0x0 = DIV1 : divided by 1 0x1 = DIV4 : divided by 4 0x2 = DIV16 : divided by 16 0x3 = DIV32 : divided by 32	0x00
23..16	-	Reserved	Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13..12	rw	ADC0_CK_DLY	ADC sampling clock phase delay select. 0x0 = No : No delay 0x1 = DLY : One step delay 0x2 = INV : Clock invert 0x3 = IDLY : Clock invert with one step delay	0x00
11..10	rw	ADC0_CK_DIV2	ADC input clock CK_PLL divider. 0x0 = DIV2 : divided by 2 0x1 = DIV4 : divided by 4 0x2 = DIV5 : divided by 5	0x00

			0x3 = DIV6 : divided by 6	
9..8	rw	ADC0_CK_SEL2	ADC internal sampling clock CK_ADC_INT source select. 0x0 = CK_ADC 0x1 = CK_PLL 0x2 = TM00_TRGO (only accept TM00_TRGO_UEV, TM00_TRGO_UEV2) 0x3 = TM01_TRGO (only accept TM01_TRGO_UEV, TM01_TRGO_UEV2)	0x00
7..6	-	Reserved	Reserved	0x00
5..4	rw	ADC0_CK_DIV	ADC internal clock CK_ADC0_INT input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV16 : divided by 16	0x00
3..2	-	Reserved	Reserved	0x00
1	-	Reserved	Reserved	0x00
0	-	Reserved	Reserved	0x00

1.35.4. ADC0 window detect threshold register

ADC0_WINDTH	ADC0 window detect threshold register		
Offset Address :	0x0C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				ADC0_WIND_HT[11:8]			
23	22	21	20	19	18	17	16
ADC0_WIND_HT[7:0]							
15	14	13	12	11	10	9	8
Reserved				ADC0_WIND_LT[11:8]			
7	6	5	4	3	2	1	0
ADC0_WIND_LT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27..16	rw	ADC0_WIND_HT	ADC voltage window detect higher threshold	0x0000
15..12	-	Reserved	Reserved	0x00
11..0	rw	ADC0_WIND_LT	ADC Voltage window detect lower threshold	0x0000

1.35.5. ADC0 control register 0

ADC0_CR0	ADC0 control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
ADC0_DMA_EN	ADC0_DMA_DSIZE	ADC0_DMA_MDS	Reserved				
23	22	21	20	19	18	17	16
ADC0_SMP_SEL[7:0]							
15	14	13	12	11	10	9	8
ADC0_LIM_MDS[1:0]		Reserved		ADC0_CH_CHG	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0
ADC0_RES_SEL[1:0]		Reserved	Reserved	Reserved	ADC0_WAIT_EN	ADC0_AUTOFF_EN	ADC0_EN

Bit	Attr	Bit Name	Description	Reset
31	rw	ADC0_DMA_EN	Direct memory access enable. When enables, hardware can get the ADC sampling data and send to DMA. For normal operation, the ADC sampling clock frequency must be slow under 1/4 ratio of AHB clock frequency. 0 = Disable 1 = Enable	0x00

30	rw	ADC0_DMA_DSIZE	ADC data size for direct memory access. When selects 16Bit, chip will transfer the bit[15:0] of ADC0_DAT0 for DMA transmission. When selects 32Bit, chip will transfer all 32-bit of ADC0_DAT0 for DMA transmission. 0 = 32Bit 1 = 16Bit	0x00
29	rw	ADC0_DMA_MDS	E1CNVF flag asserted mode select for direct memory access. When selects 'Disable', the E1CNVF flag will be masked after ADC conversion end. When selects 'Keep', the E1CNVF flag will be asserted after ADC conversion end. Also the interrupt will be generated if the related interrupt enable bit is enabled. 0 = Disable 1 = Keep	0x00
28..24	-	Reserved	Reserved	0x00
23..16	rw	ADC0_SMP_SEL	ADC sampling time select from 0T clock to 255T clocks. Value 0 indicates 0T clock.	0x00
15..14	rw	ADC0_LIM_MDS	ADC output code spike limit function select 0x0 = No operation 0x1 = Skip 0x2 = Clamp 0x3 = Reserved	0x00
13..12	-	Reserved	Reserved	0x00
11	rw	ADC0_CH_CHG	ADC scan/loop mode channel MUX change source control. 0 = CONV : change channel at ADC conversion end 1 = SMP : change channel at ADC sampling end	0x00
10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7..6	rw	ADC0_RES_SEL	ADC data resolution select. register. 0x0 = 12-bit 0x1 = 10-bit 0x2 = 8-bit 0x3 = Reserved	0x00
5	-	Reserved	Reserved	0x00
4	-	Reserved	Reserved	0x00
3	-	Reserved	Reserved	0x00
2	rw	ADC0_WAIT_EN	Wait conversion mode enable for low CPU frequency . 0 = Disable 1 = Enable	0x00
1	rw	ADC0_AUTOFF_EN	Auto-off mode enable. When is enabled, ADC is automatically powered off except during active conversion phase. 0 = Disable 1 = Enable	0x00
0	rw	ADC0_EN	ADC power-on enable bit. 0 = Disable 1 = Enable	0x00

1.35.6. ADC0 control register 1

ADC0_CR1	ADC0 control register 1		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved			ADC0_DOS_VAL[4:0]				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved	ADC0_SUM_NUM[6:0]						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved					ADC0_SUM_MDS	ADC0_SOVR_MDS	ADC0_OVR_MDS
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	ADC0_OUT_SEL[2:0]			ADC0_ALIGN_SEL	Reserved	ADC0_WIND_MDS	ADC0_WIND_EN

Bit	Attr	Bit Name	Description	Reset
31..29	-	Reserved	Reserved	0x00
28..24	rw	ADC0_DOS_VAL	ADC adjusted 2s complement value of digital offset adjuster.	0x00
23	-	Reserved	Reserved	0x00
22..16	rw	ADC0_SUM_NUM	ADC data sum accumulation data number. Value 0 indicates to disable accumulation and the maximum value 0x40 indicates 64 data to accumulate.	0x00
15..11	-	Reserved	Reserved	0x00
10	rw	ADC0_SUM_MDS	ADC data accumulation sum channel mode select. When selects Single mode for ADC one shot conversion mode, the ADC0_SUM0_MUX selection channel data is accumulated into ADC0_SUM0. When selects All mode, the all selection channel data are accumulated one-by-one into ADC0_SUM0 only. When selects Single mode for ADC channel scan conversion mode, the ADC0_SUM1_MUX/ADC0_SUM2_MUX selection channel data are also separately accumulated into ADC0_SUM1/ADC0_SUM2. 0 = Single (Single channel) 1 = All (All selected scan channels)	0x00
9	rw	ADC0_SOVR_MDS	ADC data sum overrun mode select. 0 = Overwritten (Overwritten by new data) 1 = Keep (Preserved old date)	0x00
8	rw	ADC0_OVR_MDS	ADC data buffer overrun mode select. 0 = Overwritten (Overwritten by new data) 1 = Keep (Preserved old date)	0x00
7	-	Reserved	Reserved	0x00
6..4	rw	ADC0_OUT_SEL	ADC_OUT output signal select. 0x0 = WDL (window detect state for outside low) 0x1 = WDI (window detect state for inside) 0x2 = WDH (window detect state for outside high) 0x3 = RDY (ADC0_RDY internal data ready signal) 0x4 = INTS0 (Internal signal 0) 0x5 = INTS1 (Internal signal 1) 0x6 = INTS2 (Internal signal 2) 0x7 = INTS3 (Internal signal 3)	0x00
3	rw	ADC0_ALIGN_SEL	ADC data alignment select. 0 = Right (Right alignment) 1 = Left (Left alignment)	0x00
2	-	Reserved	Reserved	0x00
1	rw	ADC0_WIND_MDS	ADC Voltage window detect and output code spike limit function channel mode select. 0 = Single (Single channel) 1 = All (All scan channels)	0x00
0	rw	ADC0_WIND_EN	ADC Voltage window detect enable bit. 0 = Disable 1 = Enable	0x00

1.35.7. ADC0 channel mask register

ADC0_MSK	ADC0 channel mask register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				ADC0_SUM2_MUX[3:0]			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADC0_SUM1_MUX[3:0]				ADC0_SUM0_MUX[3:0]			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADC0_CH_MSK15	ADC0_CH_MSK14	ADC0_CH_MSK13	ADC0_CH_MSK12	ADC0_CH_MSK11	ADC0_CH_MSK10	ADC0_CH_MSK9	ADC0_CH_MSK8
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

ADC0_CH_MSK7	ADC0_CH_MSK6	ADC0_CH_MSK5	ADC0_CH_MSK4	ADC0_CH_MSK3	ADC0_CH_MSK2	ADC0_CH_MSK1	ADC0_CH_MSK0

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27..24	rw	ADC0_SUM2_MUX	ADC input channel selection for ADC data sum-2 function.	0x00
23..20	rw	ADC0_SUM1_MUX	ADC input channel selection for ADC data sum-1 function.	0x00
19..16	rw	ADC0_SUM0_MUX	Analog input channel selection for ADC data sum-0 function.	0x00
15	rw	ADC0_CH_MSK15	ADC channel-15 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
14	rw	ADC0_CH_MSK14	ADC channel-14 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
13	rw	ADC0_CH_MSK13	ADC channel-13 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
12	rw	ADC0_CH_MSK12	ADC channel-12 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
11	rw	ADC0_CH_MSK11	ADC channel-11 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
10	rw	ADC0_CH_MSK10	ADC channel-10 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
9	rw	ADC0_CH_MSK9	ADC channel-9 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
8	rw	ADC0_CH_MSK8	ADC channel-8 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
7	rw	ADC0_CH_MSK7	ADC channel-7 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
6	rw	ADC0_CH_MSK6	ADC channel-6 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
5	rw	ADC0_CH_MSK5	ADC channel-5 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable	0x00

			1 = Enable	
4	rw	ADC0_CH_MSK4	ADC channel-4 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
3	rw	ADC0_CH_MSK3	ADC channel-3 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
2	rw	ADC0_CH_MSK2	ADC channel-2 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
1	rw	ADC0_CH_MSK1	ADC channel-1 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00
0	rw	ADC0_CH_MSK0	ADC channel-0 selection mask for sequence channel scan. When selects 'Disable', the related channel is masked and disabled from the sequence channel scan loop. 0 = Disable 1 = Enable	0x00

1.35.8. ADC0 start conversion register

ADC0_START	ADC0 start conversion register		
Offset Address :	0x20	Reset Value :	0x00001000

31	30	29	28	27	26	25	24
Reserved					Reserved	ADC0_CONV_MDS[1:0]	
23	22	21	20	19	18	17	16
Reserved		ADC0_TRG_SEL[1:0]		ADC0_TRG_CONT	ADC0_START_SEL[2:0]		
15	14	13	12	11	10	9	8
Reserved			ADC0_CH_SEL	ADC0_CH_MUX[3:0]			
7	6	5	4	3	2	1	0
Reserved		Reserved		Reserved		ADC0_HOLD	ADC0_START

Bit	Attr	Bit Name	Description	Reset
31..27	-	Reserved	Reserved	0x00
26	-	Reserved	Reserved	0x00
25..24	rw	ADC0_CONV_MDS	ADC conversion mode select. 0x0 = One :One shot (1-time) conversion 0x1 = Scan :Single sequence channel-scan conversion 0x2 = Loop :Continuous loop channel-scan conversion 0x3 = Reserved	0x00
23..22	-	Reserved	Reserved	0x00
21..20	rw	ADC0_TRG_SEL	ADC start trigger selection. When selects Disable, the edge trigger detection is disabled and no start trigger signal output. When ADC0_START_SEL = SW (ADC0_START register setting), this register is no effect. 0x0 = Disable 0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	0x00
19	rw	ADC0_TRG_CONT	ADC start trigger continuous control enable. When disables, the ADC conversion will convert one-time/one-channel for each	0x00

			start trigger. When enables, the ADC will convert one by one until stop it for One shot mode and will convert one-loop channels for Single-Loop mode. 0 = Disable 1 = Enable	
18..16	rw	ADC0_START_SEL	ADC0 start control source select. 0x0 = SW : ADC0_START register setting 0x1 = TM00 : TM00_TRGO 0x2 = PIN : ADC0_TRG : ADC external trigger pin 0x3 = CMP0 : CMP0_OUT 0x4 = CMP1 : CMP1_OUT 0x5 = TM01 : TM01_TRGO 0x6 = TM20 : TM20_TRGO 0x7 = TM36 : TM36_TRGO	0x00
15..13	-	Reserved	Reserved	0x00
12	rw	ADC0_CH_SEL	ADC input channel Mux external or internal channel selection. When selects EXT, the input Mux channel 0~15 are mapping to external channel 0~15 by setting ADC0_CH_MUX. When selects INT, the input Mux channel 0, 2~3, 8~12 are mapping to internal channel 0, 2~3, 8~12 for internal voltage source VSSA, VBUF, DAC_P0, LDO_VR0, TSO, 1/2VDD, VPG, V33 by setting ADC0_CH_MUX. The input Mux will be HiZ if selects channel 1, 4~7, 13~15. 0 = EXT : external channels 1 = INT : internal channels	0x01
11..8	rw	ADC0_CH_MUX	ADC input channel Mux selection. The selected channel is also used to select the channel of voltage window detect channel and data limit. These bits are no effect for Scan/Loop mode. Refer to the register descriptions of ADC0_CH_SEL for the detail. When ADC0_CH_SEL=0, these bits are used to select the external input channel. When ADC0_CH_SEL=1, these bits are used to select the internal input channel.	0x00
7..6	-	Reserved	Reserved	0x00
5..4	-	Reserved	Reserved	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	ADC0_HOLD	ADC hold conversion command. 0 = Disable 1 = Enable	0x00
0	rw	ADC0_START	ADC start conversion command. (set by software and clear by hardware)	0x00

1.35.9. ADC0 analog control register

ADC0_ANA	ADC0 analog control register		
Offset Address :	0x24	Reset Value :	0x00000200

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
ADC0_TS_AUTO	ADC0_CONV_TIME	Reserved	ADC0_BUF_BIAS	Reserved		Reserved	
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	ADC0_IVREF_SEL	ADC0_TS_EN	ADC0_PGA_EN	ADC0_IVR_EN	Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	rw	ADC0_TS_AUTO	ADC internal reference IVR24 auto select. When temperature sensor output voltage is selected in ADC0_CH_MUX internal channel and this bit is set 0, the ADC reference is force to	0x00

			select internal reference IVR24. Also the ADC reference will be set back to ADC0_IVREF_SEL setting when ADC0_CH_MUX is set to other channel. 0 = Normal 1 = Auto	
14	rw	ADC0_CONV_TIME	ADC minimum conversion time select. 0 = 24ADCK : 24 ADC sampleing clock 1 = 30ADCK : 30 ADC sampleing clock	0x00
13	-	Reserved	Reserved	0x00
12	rw	ADC0_BUF_BIAS	ADC input buffer bias current control.	0x00
11..10	-	Reserved	Reserved	0x00
9..8	-	Reserved	Reserved	0x02
7	-	Reserved	Reserved	0x00
6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	rw	ADC0_IVREF_SEL	ADC internal reference top voltage select. When selects 'IVR24', both ADC0_IVR_EN and ADC0_EN must be enabled for normal operation. 0x0 = VREF : external reference pin VREF+ (ADC_VREF) 0x1 = IVR24 : internal reference voltage 2.4 volt	0x00
3	rw	ADC0_TS_EN	ADC temperature sensor enable bit. The ADC needs 100us settle time for ADC conversion after this bit is enabled. 0 = Disable 1 = Enable	0x00
2	rw	ADC0_PGA_EN	ADC input buffer and PGA enable bit. 0 = Disable 1 = Enable	0x00
1	rw	ADC0_IVR_EN	ADC internal reference source IVR24 power on enable. 0 = Disable 1 = Enable	0x00
0	-	Reserved	Reserved	0x00

1.35.10. ADC0 calibration control register

ADC0_CAL	ADC0 calibration control register		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved		Reserved					
23	22	21	20	19	18	17	16
Reserved		Reserved					
15	14	13	12	11	10	9	8
Reserved		Reserved					
7	6	5	4	3	2	1	0
Reserved				ADC0_CAL_POFFT	Reserved	Reserved	Reserved

Bit	Attr	Bit Name	Description	Reset
31..30	-	Reserved	Reserved	0x00
29..24	-	Reserved	Reserved	0x00
23..22	-	Reserved	Reserved	0x00
21..16	-	Reserved	Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	ADC0_CAL_POFFT	ADC PGA offset calibration function enable. 0 = Disable 1 = Enable	0x00
2	-	Reserved	Reserved	0x00
1	-	Reserved	Reserved	0x00

0	-	Reserved	Reserved	0x00

1.35.11. ADC0 gain control register

ADC0_GAIN	ADC0 gain control register		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved			ADC0_OFFT_ADC[4:0]				
23	22	21	20	19	18	17	16
Reserved		ADC0_OFFT_PGA[5:0]					
15	14	13	12	11	10	9	8
Reserved						Reserved	
7	6	5	4	3	2	1	0
Reserved		ADC0_GAIN_PGA[5:0]					

Bit	Attr	Bit Name	Description	Reset
31..29	-	Reserved	Reserved	0x00
28..24	rw	ADC0_OFFT_ADC	ADC offset adjust bits. ADC output code is equal ADC conversion code minus this offset code. Value 0x00,0x01 to 0x0E,0x0F are adjusted offset -31LSB, -29LSB to -3LSB, -1LSB. Value 0x10,0x11 to0x1E, 0x1F are adjusted offset 1LSB, 3LSB to 29LSB, 31LSB. (The default value is loaded from CFG OR after Cold reset)	0x00
23..22	-	Reserved	Reserved	0x00
21..16	rw	ADC0_OFFT_PGA	ADC input PGA offset adjust bits.	0x00
15..10	-	Reserved	Reserved	0x00
9..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5..0	rw	ADC0_GAIN_PGA	ADC input PGA gain adjust bits. Gain range is 1 ~ 4. ADC Gain is equal : (1+(ADC0_GAIN_PGA*3)/(63+(63-ADC0_GAIN_PGA)*3))	0x00

1.35.12. ADC0 accumulator sum result register 0

ADC0_SUM0	ADC0 accumulator sum result register 0		
Offset Address :	0x30	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
ADC0_SUM0_OVRF	ADC0_SUM0_CF	ADC0_SUM0_OF	ADC0_SUM0_UF	Reserved			
15	14	13	12	11	10	9	8
ADC0_SUM0_DAT[15:8]							
7	6	5	4	3	2	1	0
ADC0_SUM0_DAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23	rw	ADC0_SUM0_OVRF	ADC data sum register-0 overwrite/overrun indication status bit. Software need to clear both ADC0_SUM0_OVRF and ADC0_SUM0_CF and avoid getting extra invalid ADC0_SUM0_OVRF. (set by hardware and clear by software writing 1)	0x00
22	rw	ADC0_SUM0_CF	ADC data sum-0 accumulation complete indication status bit. (set by hardware and clear by software writing 1)	0x00
21	rw	ADC0_SUM0_OF	ADC data sum-0 accumulation overflow indication status bit. (set by hardware and clear by software writing 1)	0x00
20	rw	ADC0_SUM0_UF	ADC data sum-0 accumulation underflow indication status bit.	0x00

			(set by hardware and clear by software writing 1)	
19..16	-	Reserved	Reserved	0x00
15..0	rw	ADC0_SUM0_DAT	ADC data accumulator sum-0 result.	0x0000

1.35.13. ADC0 accumulator sum result register 1

ADC0_SUM1	ADC0 accumulator sum result register 1		
Offset Address :	0x34	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
ADC0_SUM1_OVRF	ADC0_SUM1_CF	ADC0_SUM1_OF	ADC0_SUM1_UF	Reserved			
15	14	13	12	11	10	9	8
ADC0_SUM1_DAT[15:8]							
7	6	5	4	3	2	1	0
ADC0_SUM1_DAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23	rw	ADC0_SUM1_OVRF	ADC data sum register-1 overwrite/overrun indication status bit. Software need to clear both ADC0_SUM1_OVRF and ADC0_SUM1_CF and avoid getting extra invalid ADC0_SUM1_OVRF. (set by hardware and clear by software writing 1)	0x00
22	rw	ADC0_SUM1_CF	ADC data sum-1 accumulation complete indication status bit. (set by hardware and clear by software writing 1)	0x00
21	rw	ADC0_SUM1_OF	ADC data sum-1 accumulation overflow indication status bit. (set by hardware and clear by software writing 1)	0x00
20	rw	ADC0_SUM1_UF	ADC data sum-1 accumulation underflow indication status bit. (set by hardware and clear by software writing 1)	0x00
19..16	-	Reserved	Reserved	0x00
15..0	rw	ADC0_SUM1_DAT	ADC data accumulator sum-1 result	0x0000

1.35.14. ADC0 accumulator sum result register 2

ADC0_SUM2	ADC0 accumulator sum result register 2		
Offset Address :	0x38	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
ADC0_SUM2_OVRF	ADC0_SUM2_CF	ADC0_SUM2_OF	ADC0_SUM2_UF	Reserved			
15	14	13	12	11	10	9	8
ADC0_SUM2_DAT[15:8]							
7	6	5	4	3	2	1	0
ADC0_SUM2_DAT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23	rw	ADC0_SUM2_OVRF	ADC data sum register-1 overwrite/overrun indication status bit. Software need to clear both ADC0_SUM2_OVRF and ADC0_SUM2_CF and avoid getting extra invalid ADC0_SUM2_OVRF. (set by hardware and clear by software writing 1)	0x00
22	rw	ADC0_SUM2_CF	ADC data sum-2 accumulation complete indication status bit. (set by hardware and clear by software writing 1)	0x00
21	rw	ADC0_SUM2_OF	ADC data sum-2 accumulation overflow indication status bit. (set by hardware and clear by software writing 1)	0x00

20	rw	ADC0_SUM2_UF	ADC data sum-2 accumulation underflow indication status bit. (set by hardware and clear by software writing 1)	0x00
19..16	-	Reserved	Reserved	0x00
15..0	rw	ADC0_SUM2_DAT	ADC data accumulator sum-2 result	0x0000

1.35.15. ADC0 Temperature Sensor calibration register

ADC0_TCAL	ADC0 Temperature Sensor calibration register		
Offset Address :	0x3C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				ADC0_TCAL1[11:8]			
23	22	21	20	19	18	17	16
ADC0_TCAL1[7:0]							
15	14	13	12	11	10	9	8
Reserved				ADC0_TCAL0[11:8]			
7	6	5	4	3	2	1	0
ADC0_TCAL0[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27..16	r	ADC0_TCAL1	Temperature Sensor calibration ADC value 1.	0x0000
15..12	-	Reserved	Reserved	0x00
11..0	r	ADC0_TCAL0	Temperature Sensor calibration ADC value 0.	0x0000

1.35.16. ADC0 conversion data register 0

ADC0_DAT0	ADC0 conversion data register 0		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
ADC0_DAT0_CH[3:0]				Reserved			
23	22	21	20	19	18	17	16
ADC0_DAT0_OVRF	ADC0_DAT0_CF	Reserved			ADC0_DAT0_WDHF	ADC0_DAT0_WDIF	ADC0_DAT0_WDLF
15	14	13	12	11	10	9	8
ADC0_DAT0[15:8]							
7	6	5	4	3	2	1	0
ADC0_DAT0[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..28	r	ADC0_DAT0_CH	ADC data conversion channel number. These bits are used to indicate the active channel number for the capture ADC data in the register of ADC0_DAT0.	0x00
27..24	-	Reserved	Reserved	0x00
23	rw	ADC0_DAT0_OVRF	ADC conversion data register-0 overwrite/overrun indication status bit. Software need to clear both ADC0_DAT0_OVRF and ADC0_DAT0_CF and avoid getting extra invalid ADC0_DAT0_OVRF. (set by hardware and clear by software writing 1)	0x00
22	rw	ADC0_DAT0_CF	ADC conversion data-0 complete in 1-time and data ready status bit. (set by hardware and clear by software writing 1)	0x00
21..19	-	Reserved	Reserved	0x00
18	rw	ADC0_DAT0_WDHF	ADC voltage window detect outside high event flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
17	rw	ADC0_DAT0_WDIF	ADC voltage window detect inside event flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred)	0x00

			1 = Happened (Event happened)	
16	rw	**ADC0_DAT0_WDLF**	ADC voltage window detect outside low event flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
15..0	r	**ADC0_DAT0**	ADC conversion data-0. User read this data and also clear ADC0_DAT0_CF/ADC0_DAT0_OVRF, then chip is ready to receive next ADC data.	0x0000

1.35.17. ADC0 Register Map

ADC0 Register Map Register Number = 16

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ADC0_STA	Reserved				Reserved	Reserved	Reserved	ADC0_POF	Reserved								ADC0_SUMOVRF	ADC0_SUMCF	ADC0_SUMOF	Reserved	Reserved	ADC0_WDHF	ADC0_WDIF	ADC0_WDLF	ADC0_OVRF	Reserved	ADC0_ESCNVF	Reserved	ADC0_E1CNVF	ADC0_ESMPF	Reserved	ADC0_SOCF
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	ADC0_INT	Reserved																ADC0_SUMOVR_IE	ADC0_SUMC_IE	ADC0_SUMO_IE	Reserved		ADC0_WDH_IE	ADC0_WDI_IE	ADC0_WDL_IE	ADC0_OVR_IE	Reserved	ADC0_ESCNV_IE	Reserved	ADC0_E1CNV_IE	ADC0_ESMP_IE	Reserved	ADC0_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	ADC0_CLK	ADC0_SCNT[3:0]				Reserved		ADC0_CK_SDIV [1:0]		Reserved								Reserved		ADC0_CK_DLY [1:0]		ADC0_CK_DIV2 [1:0]		ADC0_CK_SEL2 [1:0]		Reserved		ADC0_CK_DIV [1:0]		Reserved		Reserved	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	ADC0_WINDTH	Reserved				ADC0_WIND_HT [11:0]												Reserved				ADC0_WIND_LT [11:0]											
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	ADC0_CR0	ADC0_DMA_EN	ADC0_DMA_DSIZE	ADC0_DMA_MDS	Reserved					ADC0_SMP_SEL [7:0]								ADC0_LIM_MDS [1:0]		Reserved		ADC0_CH_CHG	Reserved	Reserved	Reserved	ADC0_RES_SEL [1:0]		Reserved	Reserved	Reserved	ADC0_WAIT_EN	ADC0_AUTOFF_EN	ADC0_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	ADC0_CR1	Reserved			ADC0_DOS_VAL [4:0]					Reserved	ADC0_SUM_NUM [6:0]							Reserved					ADC0_SUM_MDS	ADC0_SOVR_MDS	ADC0_OVR_MDS	Reserved	ADC0_OUT_SEL [2:0]			ADC0_ALIGN_SEL	Reserved	ADC0_WIND_MDS	ADC0_WIND_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	ADC0_MSK	Reserved				ADC0_SUM2_MUX [3:0]				ADC0_SUM1_MUX [3:0]				ADC0_SUM0_MUX [3:0]				ADC0_CH_MSK15	ADC0_CH_MSK14	ADC0_CH_MSK13	ADC0_CH_MSK12	ADC0_CH_MSK11	ADC0_CH_MSK10	ADC0_CH_MSK9	ADC0_CH_MSK8	ADC0_CH_MSK7	ADC0_CH_MSK6	ADC0_CH_MSK5	ADC0_CH_MSK4	ADC0_CH_MSK3	ADC0_CH_MSK2	ADC0_CH_MSK1	ADC0_CH_MSK0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	ADC0_START	Reserved					Reserved	ADC0_CONV_MDS [1:0]		Reserved		ADC0_TRG_SEL [1:0]		ADC0_TRG_CONT	ADC0_START_SEL [2:0]			Reserved			ADC0_CH_SEL	ADC0_CH_MUX [3:0]				Reserved		Reserved		Reserved		ADC0_HOLD	ADC0_START
Reset	**0x00001000**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

0x24	ADC0_ANA	Reserved																ADC0_TS_AUTO	ADC0_CONV_TIME	Reserved	ADC0_BUF_BIAS	Reserved		Reserved		Reserved	Reserved	Reserved	ADC0_IVREF_SEL	ADC0_TS_EN	ADC0_PGA_EN	ADC0_IVR_EN	Reserved
Reset	0x00000200	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0x28	ADC0_CAL	Reserved		Reserved						Reserved		Reserved						Reserved		Reserved						Reserved				ADC0_CAL_POFFT	Reserved	Reserved	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	ADC0_GAIN	Reserved			ADC0_OFFT_ADC[4:0]					Reserved		ADC0_OFFT_PGA[5:0]						Reserved						Reserved		Reserved		ADC0_GAIN_PGA[5:0]					
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	ADC0_SUM0	Reserved								ADC0_SUM0_OVRF	ADC0_SUM0_CF	ADC0_SUM0_OF	ADC0_SUM0_UF	Reserved				ADC0_SUM0_DAT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	ADC0_SUM1	Reserved								ADC0_SUM1_OVRF	ADC0_SUM1_CF	ADC0_SUM1_OF	ADC0_SUM1_UF	Reserved				ADC0_SUM1_DAT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	ADC0_SUM2	Reserved								ADC0_SUM2_OVRF	ADC0_SUM2_CF	ADC0_SUM2_OF	ADC0_SUM2_UF	Reserved				ADC0_SUM2_DAT[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	ADC0_TCAL	Reserved				ADC0_TCAL1[11:0]												Reserved				ADC0_TCAL0[11:0]											
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	ADC0_DAT0	ADC0_DAT0_CH[3:0]				Reserved				ADC0_DAT0_OVRF	ADC0_DAT0_CF	Reserved			ADC0_DAT0_WDHF	ADC0_DAT0_WDIF	ADC0_DAT0_WDLF	ADC0_DAT0[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.36. Analog Comparator Registers

Analog Comparator	(CMP) Analog Comparator Control
Base Address :	0x5C000000

1.36.1. CMP Analog comparator status register

CMP_STA	CMP Analog comparator status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0
CMP_AC1_FF	CMP_AC1_RF	Reserved	CMP_AC1_S	CMP_AC0_FF	CMP_AC0_RF	Reserved	CMP_AC0_S

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	-	Reserved	Reserved	0x00
14	-	Reserved	Reserved	0x00
13	-	Reserved	Reserved	0x00
12	-	Reserved	Reserved	0x00
11	-	Reserved	Reserved	0x00
10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7	rw	CMP_AC1_FF	Analog comparator CMP1 falling edge interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6	rw	CMP_AC1_RF	Analog comparator CMP1 rising edge interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
5	-	Reserved	Reserved	0x00
4	r	CMP_AC1_S	Analog comparator CMP1 result status. When CMP1_INV =0, the result status is 0 if analog comparator input(+) voltage < analog comparator input(-) voltage and the result status is 1 if analog comparator input(+) voltage > analog comparator input(-) voltage. This bit value is inverse when CMP1_INV =1.	0x00
3	rw	CMP_AC0_FF	Analog comparator CMP0 falling edge interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	CMP_AC0_RF	Analog comparator CMP0 rising edge interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	-	Reserved	Reserved	0x00
0	r	CMP_AC0_S	Analog comparator CMP0 result status. When CMP0_INV =0, the result status is 0 if analog comparator input(+) voltage < analog comparator input(-) voltage and the result status is 1 if analog comparator input(+) voltage > analog comparator input(-) voltage. This bit value is inverse when CMP0_INV =1.	0x00

1.36.2. CMP Analog comparator interrupt enable register

CMP_INT	CMP Analog comparator interrupt enable register

Offset Address : 0x04 Reset Value : 0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved		Reserved	Reserved	Reserved	
7	6	5	4	3	2	1	0
CMP_AC1_FIE	CMP_AC1_RIE	Reserved		CMP_AC0_FIE	CMP_AC0_RIE	Reserved	CMP_IEA

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15	-	Reserved	Reserved	0x00
14	-	Reserved	Reserved	0x00
13..12	-	Reserved	Reserved	0x00
11	-	Reserved	Reserved	0x00
10	-	Reserved	Reserved	0x00
9..8	-	Reserved	Reserved	0x00
7	rw	CMP_AC1_FIE	Analog comparator CMP1 falling edge interrupt enable. 0 = Disable 1 = Enable	0x00
6	rw	CMP_AC1_RIE	Analog comparator CMP1 rising edge interrupt enable. 0 = Disable 1 = Enable	0x00
5..4	-	Reserved	Reserved	0x00
3	rw	CMP_AC0_FIE	Analog comparator CMP0 falling edge interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	CMP_AC0_RIE	Analog comparator CMP0 rising edge interrupt enable. 0 = Disable 1 = Enable	0x00
1	-	Reserved	Reserved	0x00
0	rw	CMP_IEA	Analog comparator interrupt all enable. When disables, the Analog comparator global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.36.3. CMP Analog comparator analog control register

CMP_ANA	CMP Analog comparator analog control register

Offset Address : 0x0C Reset Value : 0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
CMP_IVREF2_RS[5:0]						CMP_IVREF2_SEL	CMP_IVREF2_EN
7	6	5	4	3	2	1	0
CMP_IVREF_RS[5:0]						CMP_IVREF_SEL	CMP_IVREF_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..10	rw	CMP_IVREF2_RS	Analog comparator 2nd internal reference (R-ladder) voltage select. The output is equal IVRT*[Register_Value]/63. IVRT is the R-ladder top voltage.	0x00

9	rw	CMP_IVREF2_SEL	Analog comparator 2nd internal reference (R-ladder) top voltage IVRT source select. 0x0 = VDDA (analog power voltage) 0x1 = VR0 (LDO VR0 output)	0x00
8	rw	CMP_IVREF2_EN	Comparator CMP1 power-on enable bit. 0 = Disable 1 = Enable	0x00
7..2	rw	CMP_IVREF_RS	Analog comparator main internal reference (R-ladder) voltage select. The output is equal IVRT*[Register_Value]/63. IVRT is the R-ladder top voltage.	0x00
1	rw	CMP_IVREF_SEL	Analog comparator main internal reference (R-ladder) top voltage IVRT source select. 0x0 = VDDA (analog power voltage) 0x1 = VR0 (LDO VR0 output)	0x00
0	rw	CMP_IVREF_EN	Comparator CMP0 power-on enable bit. 0 = Disable 1 = Enable	0x00

1.36.4. CMP Analog comparator-0 control register

CMP_CR0	CMP Analog comparator-0 control register		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
CMP_AC0_IVROE	Reserved						
23	22	21	20	19	18	17	16
Reserved		CMP_AC0_FDIV[1:0]		CMP_AC0_FSEL[1:0]		CMP_AC0_PINV	CMP_AC0_INV
15	14	13	12	11	10	9	8
Reserved	CMP_AC0_NMUX[2:0]			Reserved	CMP_AC0_PMUX[2:0]		
7	6	5	4	3	2	1	0
Reserved		Reserved	CMP_AC0_HYS	CMP_AC0_RES	Reserved	Reserved	CMP_AC0_EN

Bit	Attr	Bit Name	Description	Reset
31	rw	CMP_AC0_IVROE	IVREF output to CMP0_I0 pin enable bit for positive channel MUX . 0 = Disable 1 = Enable	0x00
30..24	-	Reserved	Reserved	0x00
23..22	-	Reserved	Reserved	0x00
21..20	rw	CMP_AC0_FDIV	CMP0 analog comparator output synchronized filter divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
19..18	rw	CMP_AC0_FSEL	CMP0 analog comparator output signal select with synchronized filter. When selects the signal with 3-clock filter except Bypass selection, the comparator output will filter 3 clocks by the filter clock which is divided by the CMP_AC0_FDIV from the following selection clock source. 0x0 = Bypass 0x1 = CMP_CK : filter with CMP_CLK 0x2 = TM00_TRGO : filter with TM00_TRGO 0x3 = TM01_TRGO : filter with TM01_TRGO	0x00
17	rw	CMP_AC0_PINV	CMP0 output to pins' signal inverse enable. 0 = Disable 1 = Enable	0x00
16	rw	CMP_AC0_INV	CMP0 analog comparator output signal polarity select. 0 = Positive 1 = Negative	0x00
15	-	Reserved	Reserved	0x00

14..12	rw	CMP_AC0_NMUX	CMP0 Analog input negative channel selection. 0x0 = IVREF 0x1 = CMP0_I0 0x2 = CMP0_I1 0x3 = CMP_C0 0x4 = CMP_C1 0x5 = DAC_P0	0x00
11	-	Reserved	Reserved	0x00
10..8	rw	CMP_AC0_PMUX	CMP0 Analog input positive channel selection. 0x0 = IVREF 0x1 = CMP0_I0 0x2 = CMP0_I1 0x3 = CMP_C0 0x4 = CMP_C1 0x5 = DAC_P0	0x00
7..6	-	Reserved	Reserved	0x00
5	-	Reserved	Reserved	0x00
4	rw	CMP_AC0_HYS	CMP0 input hysteresis window select. 0x0 = No : no hysteresis 0x1 = LVL1 : with hysteresis about 10mv	0x00
3	rw	CMP_AC0_RES	CMP0 compare response time select. 0x0 = 200ns 0x1 = 10us (5~10us)	0x00
2	-	Reserved	Reserved	0x00
1	-	Reserved	Reserved	0x00
0	rw	CMP_AC0_EN	Analog comparator CMP0 power-on enable bit. When disables, it will force the analog comparator output low. 0 = Disable 1 = Enable	0x00

1.36.5. CMP Analog comparator-1 control register

CMP_CR1	CMP Analog comparator-1 control register		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
CMP_AC1_IVROE	Reserved						
23	22	21	20	19	18	17	16
Reserved		CMP_AC1_FDIV[1:0]		CMP_AC1_FSEL[1:0]		CMP_AC1_PINV	CMP_AC1_INV
15	14	13	12	11	10	9	8
Reserved	CMP_AC1_NMUX[2:0]			Reserved	CMP_AC1_PMUX[2:0]		
7	6	5	4	3	2	1	0
Reserved			CMP_AC1_HYS	CMP_AC1_RES	Reserved		CMP_AC1_EN

Bit	Attr	Bit Name	Description	Reset
31	rw	CMP_AC1_IVROE	IVREF output to CMP1_I0 pin enable bit for positive channel MUX . 0 = Disable 1 = Enable	0x00
30..24	-	Reserved	Reserved	0x00
23..22	-	Reserved	Reserved	0x00
21..20	rw	CMP_AC1_FDIV	CMP1 analog comparator output synchronized filter divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
19..18	rw	CMP_AC1_FSEL	CMP1 analog comparator output signal select with synchronized filter. When selects the signal with 3-clock filter except Bypass selection, the comparator output will filter 3 clocks by the filter clock which is divided by the	0x00

			CMP_AC1_FDIV from the following selection clock source. 0x0 = Bypass 0x1 = CMP_CK : filter with CMP_CLK 0x2 = TM00_TRGO : filter with TM00_TRGO 0x3 = TM01_TRGO : filter with TM01_TRGO	
17	rw	**CMP_AC1_PINV**	CMP1 output to pins' signal inverse enable. 0 = Disable 1 = Enable	0x00
16	rw	**CMP_AC1_INV**	CMP1 analog comparator output signal polarity select. 0 = Positive 1 = Negative	0x00
15	-	**Reserved**	Reserved	0x00
14..12	rw	**CMP_AC1_NMUX**	CMP1 Analog input negative channel selection. 0x0 = IVREF 0x1 = CMP0_I0 0x2 = CMP0_I1 0x3 = CMP_C0 0x4 = CMP_C1 0x5 = DAC_P0	0x00
11	-	**Reserved**	Reserved	0x00
10..8	rw	**CMP_AC1_PMUX**	CMP1 Analog input positive channel selection. 0x0 = IVREF 0x1 = CMP0_I0 0x2 = CMP0_I1 0x3 = CMP_C0 0x4 = CMP_C1 0x5 = DAC_P0	0x00
7..5	-	**Reserved**	Reserved	0x00
4	rw	**CMP_AC1_HYS**	CMP1 input hysteresis window select. 0x0 = No : no hysteresis 0x1 = LVL1 : with hysteresis about 10mv	0x00
3	rw	**CMP_AC1_RES**	CMP1 compare response time select. 0x0 = 200ns 0x1 = 10us (5~10us)	0x00
2..1	-	**Reserved**	Reserved	0x00
0	rw	**CMP_AC1_EN**	Analog comparator CMP1 power-on enable bit. When disables, it will force the analog comparator output low. 0 = Disable 1 = Enable	0x00

1.36.6. CMP Register Map

CMP Register Map Register Number = 5

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	CMP_STA	Reserved																Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CMP_AC1_FF	CMP_AC1_RF	Reserved	CMP_AC1_S	CMP_AC0_FF	CMP_AC0_RF	Reserved	CMP_AC0_S
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	CMP_INT	Reserved																Reserved	Reserved	Reserved		Reserved	Reserved	Reserved		CMP_AC1_FIE	CMP_AC1_RIE	Reserved		CMP_AC0_FIE	CMP_AC0_RIE	Reserved	CMP_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	CMP_ANA	Reserved																CMP_IVREF2_RS [5:0]						CMP_IVREF2_SEL	CMP_IVREF2_EN	CMP_IVREF_RS [5:0]						CMP_IVREF_SEL	CMP_IVREF_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	CMP_CR0	CMP_AC0_IVROE	Reserved							Reserved		CMP_AC0_FDIV [1:0]		CMP_AC0_FSEL [1:0]		CMP_AC0_PINV	CMP_AC0_INV	Reserved	CMP_AC0_NMUX [2:0]			Reserved	CMP_AC0_PMUX [2:0]			Reserved		Reserved	CMP_AC0_HYS	CMP_AC0_RES	Reserved	Reserved	CMP_AC0_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	CMP_CR1	CMP_AC1_IVROE	Reserved							Reserved		CMP_AC1_FDIV [1:0]		CMP_AC1_FSEL [1:0]		CMP_AC1_PINV	CMP_AC1_INV	Reserved	CMP_AC1_NMUX [2:0]			Reserved	CMP_AC1_PMUX [2:0]			Reserved			CMP_AC1_HYS	CMP_AC1_RES	Reserved		CMP_AC1_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.37. DAC Control Registers

DAC Control	(DAC) Digital-to-Analog Converter Control
Base Address :	0x5C080000

1.37.1. DAC status register

DAC_STA	DAC status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							Reserved
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
DAC_UDR0F	Reserved				Reserved	DAC_RDY0F	Reserved

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..17	-	Reserved	Reserved	0x00
16	-	Reserved	Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7	rw	DAC_UDR0F	DAC-0 conversion underrun event flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
6..3	-	Reserved	Reserved	0x00
2	-	Reserved	Reserved	0x00
1	rw	DAC_RDY0F	DAC-0 ready flag to update new data to data register. It will be set by hardware when DAC power-on. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	-	Reserved	Reserved	0x00

1.37.2. DAC interrupt enable register

DAC_INT	DAC interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							Reserved
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
DAC_UDR0_IE	Reserved				Reserved	DAC_RDY0_IE	DAC_IEA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..17	-	Reserved	Reserved	0x00
16	-	Reserved	Reserved	0x00
15..8	-	Reserved	Reserved	0x00
7	rw	DAC_UDR0_IE	DAC-0 conversion underrun event interrupt enable. 0 = Disable 1 = Enable	0x00
6..3	-	Reserved	Reserved	0x00

2	-	Reserved	Reserved	0x00
1	rw	DAC_RDY0_IE	DAC-0 ready to update new data to data register interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	DAC_IEA	DAC interrupt all enable. When disables, the DAC global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.37.3. DAC control register 0

DAC_CR0	DAC control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
DAC_DMA_EN	Reserved						
23	22	21	20	19	18	17	16
Reserved							Reserved
15	14	13	12	11	10	9	8
Reserved		DAC_TRG0_SEL[1:0]		Reserved	DAC_START0_SEL[2:0]		
7	6	5	4	3	2	1	0
DAC_RES0_SEL[1:0]		Reserved	DAC_ALIGN0_SEL	Reserved		DAC_BUF0_EN	DAC_DA0_EN

Bit	Attr	Bit Name	Description	Reset
31	rw	DAC_DMA_EN	Direct memory access enable to transmit. When enables, hardware can receive the data from DMA and send to DAC output. 0 = Disable 1 = Enable	0x00
30..24	-	Reserved	Reserved	0x00
23..17	-	Reserved	Reserved	0x00
16	-	Reserved	Reserved	0x00
15..14	-	Reserved	Reserved	0x00
13..12	rw	DAC_TRG0_SEL	DAC-0 start trigger selection. When selects Disable, the edge trigger detection is disabled and no start trigger signal output. When DAC_START0_SEL = WDAT (DAC_DAT0 register written), this register is no effect. 0x0 = Disable 0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	0x00
11	-	Reserved	Reserved	0x00
10..8	rw	DAC_START0_SEL	DAC-0 start trigger control source select. When DAC_DMA_EN = Enable, 0x0(WDAT) register written mode is not support. 0x0 = WDAT : DAC_DAT0 register written 0x1 = PIN : DAC_TRG external trigger pin 0x2 = CMP0 : CMP0_OUT 0x3 = TM00 : TM00_TRGO 0x4 = TM01 : TM01_TRGO 0x5 = TM10 : TM10_TRGO 0x6 = ITR6 : APB_ITR6 0x7 = ITR7 : APB_ITR7	0x00
7..6	rw	DAC_RES0_SEL	DAC-0 data resolution select. register. Lower resolution allows faster conversion times for applications. 0x0 = 12-bit 0x1 = 10-bit 0x2 = 8-bit	0x00
5	-	Reserved	Reserved	0x00

4	rw	DAC_ALIGN0_SEL	DAC-0 data alignment select. 0 = Right (Right alignment) 1 = Left (Left alignment)	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	DAC_BUF0_EN	DAC-0 output buffer enable bit. 0 = Disable 1 = Enable	0x00
0	rw	DAC_DA0_EN	DAC-0 power-on enable bit. 0 = Disable 1 = Enable	0x00

1.37.4. DAC conversion data register 0

DAC_DAT0	DAC conversion data register 0		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
DAC_DAT0[15:8]							
7	6	5	4	3	2	1	0
DAC_DAT0[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	DAC_DAT0	DAC-0 conversion data register. This register is the data buffer to copy to the conversion output register DAC_DOR0 when the conversion trigger event is occurred. It will clear the DAC_RDY0F and DAC_UDR0F flag when writes this data register.	0x0000

1.37.5. DAC conversion output register 0

DAC_DOR0	DAC conversion output register 0		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
DAC_DOR0[15:8]							
7	6	5	4	3	2	1	0
DAC_DOR0[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	r	DAC_DOR0	DAC-0 conversion output register. When this register value is changed, the DAC analog output get to the stable state after a minimum settling time.	0x0000

1.37.6. DAC Register Map

DAC Register Map **Register Number = 5**

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	DAC_STA	Reserved								Reserved							Reserved	Reserved								DAC_UDR0F	Reserved				Reserved	DAC_RDY0F	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	DAC_INT	Reserved								Reserved							Reserved	Reserved								DAC_UDR0_IE	Reserved				Reserved	DAC_RDY0_IE	DAC_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	DAC_CR0	DAC_DMA_EN	Reserved							Reserved							Reserved	Reserved		DAC_TRG0_SEL [1:0]		Reserved	DAC_START0_SEL [2:0]			DAC_RES0_SEL [1:0]		Reserved	DAC_ALIGN0_SEL	Reserved		DAC_BUF0_EN	DAC_DA0_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	DAC_DAT0	Reserved																DAC_DAT0[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	DAC_DOR0	Reserved																DAC_DOR0[15:0]															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.38. IWDT Control Registers

IWDT Control	(IWDT) Independent Watch Dog Timer Control
Base Address :	0x5D000000

1.38.1. IWDT status register

IWDT_STA	IWDT status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				IWDT_EW1F	IWDT_EW0F	IWDT_TF	Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	IWDT_EW1F	IWDT early wakeup-1 flag. This bit is set when the counter value reaches to 0x40. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	IWDT_EW0F	IWDT early wakeup-0 flag. This bit is set when the counter value reaches to 0x20. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	rw	IWDT_TF	IWDT timer timeout interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	-	Reserved	Reserved	0x00

1.38.2. IWDT interrupt enable register

IWDT_INT	IWDT interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				IWDT_EW1_IE	IWDT_EW0_IE	IWDT_TIE	Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	IWDT_EW1_IE	IWDT early wakeup-1 interrupt enable. 0 = Disable 1 = Enable	0x00

2	rw	IWDT_EW0_IE	IWDT early wakeup-0 interrupt enable. 0 = Disable 1 = Enable	0x00
1	rw	IWDT_TIE	IWDT timer timeout interrupt enable. 0 = Disable 1 = Enable	0x00
0	-	Reserved	Reserved	0x00

1.38.3. IWDT clock source register

IWDT_CLK	IWDT clock source register		
Offset Address :	0x08	Reset Value :	0x000000C0

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
IWDT_CK_DIV[3:0]				Reserved		Reserved	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	rw	IWDT_CK_DIV	IWDT internal clock CK_IWDT_INT input divider. (The register is loaded from CFG OR only after Cold reset.) 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8 0x4 = DIV16 : divided by 16 0x5 = DIV32 : divided by 32 0x6 = DIV64 : divided by 64 0x7 = DIV128 : divided by 128 0x8 = DIV256 : divided by 256 0x9 = DIV512 : divided by 512 0xA = DIV1024 : divided by 1024 0xB = DIV2048 : divided by 2048 0xC = DIV4096 : divided by 4096 0xD = Reserved 0xE = Reserved 0xF = Reserved	0x0C
3..2	-	Reserved	Reserved	0x00
1..0	-	Reserved	Reserved	0x00

1.38.4. IWDT write protected Key register

IWDT_KEY	IWDT write protected Key register		
Offset Address :	0x0C	Reset Value :	0x00000001

31	30	29	28	27	26	25	24
IWDT_LOCK[15:8]							
23	22	21	20	19	18	17	16
IWDT_LOCK[7:0]							
15	14	13	12	11	10	9	8
IWDT_KEY[15:8]							
7	6	5	4	3	2	1	0
IWDT_KEY[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	rw	IWDT_LOCK	IWDT lock register. Write value 0x712A to lock the register write access except IWDT_STA, IWDT_KEY registers. When locks, the registers cannot change until Cold reset. Write other value except 0x712A is no effect. (The register is loaded from CFG OR only after Cold reset.) For read access : 0 = Unlocked 1 = Locked	0x0000
15..0	rw	IWDT_KEY	IWDT key register and counter reload enable control. Write value 0xA217 to unprotect the register write access. Write value 0x2014 to reload and refresh the counter. Others, write other value except 0xA217 to protect the registers except IWDT_STA, IWDT_KEY registers. For read access : 0 = Unprotected 1 = Protected	0x0001

1.38.5. IWDT control register 0

IWDT_CR0	IWDT control register 0		
Offset Address :	0x10	Reset Value :	0x00000003

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				IWDT_EW1_WPEN	IWDT_EW0_WPEN	Reserved	IWDT_TF_WPEN
7	6	5	4	3	2	1	0
Reserved						Reserved	IWDT_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	-	Reserved	Reserved	0x00
11	rw	IWDT_EW1_WPEN	IWDT detect IWDT_EW1F flag wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
10	rw	IWDT_EW0_WPEN	IWDT detect IWDT_EW0F flag wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
9	-	Reserved	Reserved	0x00
8	rw	IWDT_TF_WPEN	IWDT detect IWDT_TF flag wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
7..2	-	Reserved	Reserved	0x00
1	-	Reserved	Reserved	0x01
0	rw	IWDT_EN	IWDT function enable bit. When disables, IWDT_CNT will reload to default value. (The register is loaded from CFG OR only after Cold reset.) 0 = Disable 1 = Enable	0x01

1.38.6. IWDT counter register

IWDT_CNT	IWDT counter register		
Offset Address :	0x18	Reset Value :	0x000000FF

31	30	29	28	27	26	25	24

Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
IWDT_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..0	r	IWDT_CNT	IWDT counter value register.	0xFF

1.38.7. IWDT Register Map

IWDT Register Map Register Number = 6

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	IWDT_STA	Reserved																Reserved								Reserved				IWDT_EW1F	IWDT_EW0F	IWDT_TF	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	IWDT_INT	Reserved																Reserved								Reserved				IWDT_EW1_IE	IWDT_EW0_IE	IWDT_TIE	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	IWDT_CLK	Reserved																Reserved								IWDT_CK_DIV[3:0]				Reserved		Reserved	
Reset	0x000000C0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
0x0C	IWDT_KEY	IWDT_LOCK[15:0]																IWDT_KEY[15:0]															
Reset	0x00000001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x10	IWDT_CR0	Reserved																Reserved				IWDT_EW1_WPEN	IWDT_EW0_WPEN	Reserved	IWDT_TF_WPEN	Reserved						Reserved	IWDT_EN
Reset	0x00000003	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0x18	IWDT_CNT	Reserved																Reserved								IWDT_CNT[7:0]							
Reset	0x000000FF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

1.39. WWDT Control Registers

WWDT Control	(WWDT) System Window Watch Dog Timer Control
Base Address :	0x5D010000

1.39.1. WWDT status register

WWDT_STA	WWDT status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				WWDT_WRNF	WWDT_WINF	WWDT_TF	Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	WWDT_WRNF	WWDT counter warning flag. It is set when the WWDT counter reaches the value of WWDT_WRN. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	WWDT_WINF	WWDT counter refreshing and value over the window compare threshold condition flag. It is set when the WWDT_KEY is written 0x2014 by firmware and the counter value is over the threshold value of WWDT_WIN in the same time. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	rw	WWDT_TF	WWDT timer timeout interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	-	Reserved	Reserved	0x00

1.39.2. WWDT interrupt enable register

WWDT_INT	WWDT interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				WWDT_WRN_IE	WWDT_WIN_IE	WWDT_TIE	Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3	rw	WWDT_WRN_IE	WWDT counter warning interrupt enable.	0x00

			0 = Disable 1 = Enable	
2	rw	WWDT_WIN_IE	WWDT counter refreshing and value over the window compare threshold condition interrupt enable. 0 = Disable 1 = Enable	0x00
1	rw	WWDT_TIE	WWDT timer timeout interrupt enable. 0 = Disable 1 = Enable	0x00
0	-	Reserved	Reserved	0x00

1.39.3. WWDT clock source register

WWDT_CLK	WWDT clock source register		
Offset Address :	0x08	Reset Value :	0x00000170

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							WWDT_CK_PDIV
7	6	5	4	3	2	1	0
Reserved	WWDT_CK_DIV[2:0]			Reserved	WWDT_CK_SEL	Reserved	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..9	-	Reserved	Reserved	0x00
8	rw	WWDT_CK_PDIV	WWDT internal clock CK_WWDT_INT pre-divider value. 0 = divided by 1 1 = divided by 256	0x01
7	-	Reserved	Reserved	0x00
6..4	rw	WWDT_CK_DIV	WWDT internal clock CK_WWDT_INT input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8 0x4 = DIV16 : divided by 16 0x5 = DIV32 : divided by 32 0x6 = DIV64 : divided by 64 0x7 = DIV128 : divided by 128	0x07
3	-	Reserved	Reserved	0x00
2	rw	WWDT_CK_SEL	WWDT input clock CK_WWDT source select. 0x0 = CK_APB 0x1 = CK_UT	0x00
1..0	-	Reserved	Reserved	0x00

1.39.4. WWDT write protected Key register

WWDT_KEY	WWDT write protected Key register		
Offset Address :	0x0C	Reset Value :	0x00000001

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
WWDT_KEY[15:8]							
7	6	5	4	3	2	1	0

WWDT_KEY[7:0]

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..0	rw	WWDT_KEY	WWDT key register and counter reload enable control. Write value 0xA217 to unprotect the register write access. Write value 0x2014 to reload and refresh the counter. Others, write other value except 0xA217 to protect the register except WWDT_STA, WWDT_KEY registers. For read access : 0 = Unprotected 1 = Protected	0x0001

1.39.5. WWDT control register 0

WWDT_CR0	WWDT control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		WWDT_RSTW_EN	WWDT_RSTF_EN	Reserved			WWDT_EN

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	WWDT_RSTW_EN	WWDT reload counter out of window reset generation enable bit. 0 = Disable 1 = Enable	0x00
4	rw	WWDT_RSTF_EN	WWDT timer underflow reset generation enable bit. 0 = Disable 1 = Enable	0x00
3..1	-	Reserved	Reserved	0x00
0	rw	WWDT_EN	WWDT function enable bit. When disables, WWDT_CNT will keep the counter value. 0 = Disable 1 = Enable	0x00

1.39.6. WWDT counter register

WWDT_CNT	WWDT counter register		
Offset Address :	0x18	Reset Value :	0x000003FF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						WWDT_CNT[9:8]	
7	6	5	4	3	2	1	0
WWDT_CNT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000

15..10	-	Reserved	Reserved	0x00
9..0	r	WWDT_CNT	WWDT counter value register.	0x03FF

1.39.7. WWDT reload register

WWDT_RLR	WWDT reload register		
Offset Address :	0x1C	Reset Value :	0x000003FF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						WWDT_RLR[9:8]	
7	6	5	4	3	2	1	0
WWDT_RLR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..10	-	Reserved	Reserved	0x00
9..0	rw	WWDT_RLR	WWDT counter reload register.	0x03FF

1.39.8. WWDT window compare register

WWDT_WIN	WWDT window compare register		
Offset Address :	0x20	Reset Value :	0x000003FF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						WWDT_WIN[9:8]	
7	6	5	4	3	2	1	0
WWDT_WIN[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..10	-	Reserved	Reserved	0x00
9..0	rw	WWDT_WIN	WWDT window compare threshold register.	0x03FF

1.39.9. WWDT warning compare register

WWDT_WRN	WWDT warning compare register		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						WWDT_WRN[9:8]	
7	6	5	4	3	2	1	0
WWDT_WRN[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..10	-	Reserved	Reserved	0x00
9..0	rw	WWDT_WRN	WWDT warning interrupt compare threshold register.	0x0000

1.39.10. WWDT Register Map

WWDT Register Map Register Number = 9

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	WWDT_STA	Reserved																Reserved								Reserved				WWDT_WRNF	WWDT_WINF	WWDT_TF	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	WWDT_INT	Reserved																Reserved								Reserved				WWDT_WRN_IE	WWDT_WIN_IE	WWDT_TIE	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	WWDT_CLK	Reserved																Reserved							WWDT_CK_PDIV	Reserved	WWDT_CK_DIV[2:0]			Reserved	WWDT_CK_SEL	Reserved	
Reset	0x00000170	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0
0x0C	WWDT_KEY	Reserved																WWDT_KEY[15:0]															
Reset	0x00000001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x10	WWDT_CR0	Reserved																Reserved								Reserved		WWDT_RSTW_EN	WWDT_RSTF_EN	Reserved			WWDT_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	WWDT_CNT	Reserved																Reserved						WWDT_CNT[9:0]									
Reset	0x000003FF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
0x1C	WWDT_RLR	Reserved																Reserved						WWDT_RLR[9:0]									
Reset	0x000003FF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
0x20	WWDT_WIN	Reserved																Reserved						WWDT_WIN[9:0]									
Reset	0x000003FF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

0x24	WWDT_WRN	Reserved																Reserved						WWDT_WRN[9:0]									
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.40. RTC Control Registers

RTC Control	(RTC) Real Time Clock Control
Base Address :	0x5D040000

1.40.1. RTC status register

RTC_STA	RTC status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		RTC_RCRF	RTC_TOF	RTC_TSF	RTC_PCF	RTC_ALMF	Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	RTC_RCRF	RTC reload or capture flag. This flag is active when RTC_RLR register reload finished, RTC_CAP register software capture finished or RTC_ALM register value update allowed flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
4	rw	RTC_TOF	RTC timer overflow interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
3	rw	RTC_TSF	RTC time stamp interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
2	rw	RTC_PCF	RTC periodic interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
1	rw	RTC_ALMF	RTC alarm matched interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (Event happened)	0x00
0	-	Reserved	Reserved	0x00

1.40.2. RTC interrupt enable register

RTC_INT	RTC interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		RTC_RCR_IE	RTC_TIE	RTC_TS_IE	RTC_PC_IE	RTC_ALM_IE	RTC_IEA

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	RTC_RCR_IE	RTC_RCR register reload finished, software capture finished or RTC_ALM register value update allowed interrupt enable. 0 = Disable 1 = Enable	0x00
4	rw	RTC_TIE	RTC timer overflow interrupt enable. 0 = Disable 1 = Enable	0x00
3	rw	RTC_TS_IE	RTC time stamp interrupt enable. 0 = Disable 1 = Enable	0x00
2	rw	RTC_PC_IE	RTC periodic interrupt enable. 0 = Disable 1 = Enable	0x00
1	rw	RTC_ALM_IE	RTC alarm matched interrupt enable. 0 = Disable 1 = Enable	0x00
0	rw	RTC_IEA	RTC interrupt all enable. When disables, the RTC global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.40.3. RTC clock source register

RTC_CLK	RTC clock source register		
Offset Address :	0x08	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
RTC_CK_PDIV	Reserved	RTC_CK_DIV[1:0]		RTC_CK_SEL[1:0]		Reserved	

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7	rw	RTC_CK_PDIV	RTC internal clock CK_RTC_INT input pre-divider 0x0 = DIV4096 : divided by 4096 0x1 = DIV1 : divided by 1	0x00
6	-	Reserved	Reserved	0x00
5..4	rw	RTC_CK_DIV	RTC internal clock CK_RTC_INT input divider 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
3..2	rw	RTC_CK_SEL	RTC input clock CK_RTC source select. 0x0 = CK_LS 0x1 = CK_UT 0x2 = CK_APB 0x3 = TM01_TRGO	0x00
1..0	-	Reserved	Reserved	0x00

1.40.4. RTC write protected Key register

RTC_KEY	RTC write protected Key register		
Offset Address :	0x0C	Reset Value :	0x00000001

31	30	29	28	27	26	25	24
RTC_LOCK[15:8]							
23	22	21	20	19	18	17	16
RTC_LOCK[7:0]							
15	14	13	12	11	10	9	8
RTC_KEY[15:8]							
7	6	5	4	3	2	1	0
RTC_KEY[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..16	rw	RTC_LOCK	RTC lock register. Write value 0x712A to lock the register write access except RTC_STA, RTC_KEY registers. When locks, the registers cannot change until Cold reset. Write other value except 0x712A is no effect. For read access : 0 = Unlocked 1 = Locked	0x0000
15..0	rw	RTC_KEY	RTC key register. Write value 0xA217 to unprotect the register write access. Write other value except 0xA217 to protect the register except RTC_STA, RTC_KEY registers. For read access : 0 = Unprotected 1 = Protected	0x0001

1.40.5. RTC control register 0

RTC_CR0	RTC control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved				RTC_TF_WPEN	Reserved	RTC_PC_WPEN	RTC_ALM_WPEN
15	14	13	12	11	10	9	8
RTC_OUT_LCK	RTC_OUT_STA	RTC_TS_TRGS[1:0]		Reserved	Reserved	RTC_OUT_SEL[1:0]	
7	6	5	4	3	2	1	0
Reserved		RTC_RCR_MDS[1:0]		Reserved		RTC_ALM_EN	RTC_EN

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..20	-	Reserved	Reserved	0x00
19	rw	RTC_TF_WPEN	RTC detect RTC_TOF flag wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
18	-	Reserved	Reserved	0x00
17	rw	RTC_PC_WPEN	RTC detect RTC_PCF flag wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
16	rw	RTC_ALM_WPEN	RTC detect RTC_ALMF flag wakeup from STOP mode enable bit. 0 = Disable 1 = Enable	0x00
15	rw	RTC_OUT_LCK	RTC_OUT output signal initial state control. When locked, disables the RTC_OUT_STA register bit write access.	0x00

			Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	
14	w	RTC_OUT_STA	RTC_OUT output signal initial state. The bit is written effectively only by written 1 to RTC_OUT_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
13..12	rw	RTC_TS_TRGS	RTC time stamp trigger edge select. 0x0 = Disable 0x1 = Rising edge 0x2 = Falling edge 0x3 = Dual-edge	0x00
11	-	Reserved	Reserved	0x00
10	-	Reserved	Reserved	0x00
9..8	rw	RTC_OUT_SEL	RTC output signal select. When selects 'PC', the RTC_CK_DIV and RTC_CK_PDIV cannot set both divided by 1. 0x0 = ALM : Alarm compare output event 0x1 = PC : CK_RTC_INT periodic clock signal 0x2 = TS : Time stamp trigger event 0x3 = TO : Timer overflow signal toggle output	0x00
7..6	-	Reserved	Reserved	0x00
5..4	rw	RTC_RCR_MDS	RTC timer reload or capture control mode select. If selects 'Directly capture' or 'Delayed capture' mode, the RTC timer counter value will capture into the RTC_CAP register when software capture event (RTC_RC_START=1) or hardware time stamp event happened. If selects 'Force reload', the RTC timer counter will be updated by RTC_RLR register value when RTC_RLR has been written. If selects 'Auto reload' mode, the RTC timer counter will be update by RTC_RLR register value when RTC timer is overflow. 0x0 = Directly capture 0x1 = Delayed capture 0x2 = Forced reload 0x3 = Auto reload	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	RTC_ALM_EN	RTC Alarm enable bit. When disables, hardware will assert the RTC_RCRF flag to notify software. Then software can update the RTC_ALM register value. 0 = Disable 1 = Enable	0x00
0	rw	RTC_EN	RTC function enable bit. 0 = Disable 1 = Enable	0x00

1.40.6. RTC control register 1

RTC_CR1	RTC control register 1		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							RTC_RC_START

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000

15..8	-	Reserved	Reserved	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	RTC_RC_START	RTC timer counter reload and software capture start enable. For forced and auto reload mode when this bit enables, the RTC_RLR register value will reload to RTC timer. For capture mode when this bit enables, the RTC start to capture the counter value. When capture is finished, the timer value is captured to RTC_CAP. After reload or capture finished, RTC automatically clear this bit and set the RTC_RCRF flag. 0 = No effect 1 = Enable	0x00

1.40.7. RTC reload register

RTC_RLR	RTC reload register		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
RTC_RLR[31:24]							
23	22	21	20	19	18	17	16
RTC_RLR[23:16]							
15	14	13	12	11	10	9	8
RTC_RLR[15:8]							
7	6	5	4	3	2	1	0
RTC_RLR[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	RTC_RLR	RTC counter reload register. The value 0xFFFFFFFF is invalid.	0x00000000

1.40.8. RTC alarm compare register

RTC_ALM	RTC alarm compare register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
RTC_ALM[31:24]							
23	22	21	20	19	18	17	16
RTC_ALM[23:16]							
15	14	13	12	11	10	9	8
RTC_ALM[15:8]							
7	6	5	4	3	2	1	0
RTC_ALM[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	RTC_ALM	RTC alarm compared value register. This register is able to update under RTC_ALM_EN=0. When RTC_ALM_EN=1, update this register may be quite possible to asserted abnormal RTC flag. Refer the detail information in RTC_ALM_EN register description.	0x00000000

1.40.9. RTC capture register

RTC_CAP	RTC capture register		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
RTC_CAP[31:24]							
23	22	21	20	19	18	17	16
RTC_CAP[23:16]							

15	14	13	12	11	10	9	8
RTC_CAP[15:8]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RTC_CAP[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	r	RTC_CAP	RTC counter capture register. See more detail information in RTC_RCR_MDS register descriptions.	0x00000000

1.40.10. RTC Register Map

RTC Register Map **Register Number = 9**

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	RTC_STA	Reserved																Reserved								Reserved		RTC_RCRF	RTC_TOF	RTC_TSF	RTC_PCF	RTC_ALMF	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	RTC_INT	Reserved																Reserved								Reserved		RTC_RCR_IE	RTC_TIE	RTC_TS_IE	RTC_PC_IE	RTC_ALM_IE	RTC_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	RTC_CLK	Reserved																Reserved								RTC_CK_PDIV	Reserved	RTC_CK_DIV[1:0]		RTC_CK_SEL[1:0]		Reserved	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	RTC_KEY	RTC_LOCK[15:0]																RTC_KEY[15:0]															
Reset	**0x00000001**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x10	RTC_CR0	Reserved								Reserved				RTC_TF_WPEN	Reserved	RTC_PC_WPEN	RTC_ALM_WPEN	RTC_OUT_LCK	RTC_OUT_STA	RTC_TS_TRGS[1:0]		Reserved	Reserved	RTC_OUT_SEL[1:0]		Reserved		RTC_RCR_MDS[1:0]		Reserved		RTC_ALM_EN	RTC_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	RTC_CR1	Reserved																Reserved								Reserved							RTC_RC_START
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	RTC_RLR	RTC_RLR[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	RTC_ALM	RTC_ALM[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x20	**RTC_CAP**	**RTC_CAP[31:0]**																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.41. APB Control Registers

APB Control	(APB) APB Module Global Control
Base Address :	0x5F000000

1.41.1. APB status register

APB_STA	APB status register		
Offset Address :	0x00	Reset Value :	0x03000000

31	30	29	28	27	26	25	24
Reserved				Reserved		APB_OBM1_SW	APB_OBM0_SW
23	22	21	20	19	18	17	16
Reserved			APB_NCO0_OUT	Reserved		APB_OBM1_OUT	APB_OBM0_OUT
15	14	13	12	11	10	9	8
Reserved			APB_NCO0F	Reserved		APB_OBM1F	APB_OBM0F
7	6	5	4	3	2	1	0
Reserved							

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27..26	-	Reserved	Reserved	0x00
25	r	APB_OBM1_SW	OBM-1 break switching signal status.	0x01
24	r	APB_OBM0_SW	OBM-0 break switching signal status.	0x01
23..21	-	Reserved	Reserved	0x00
20	r	APB_NCO0_OUT	NCO-0 output status bit.	0x00
19..18	-	Reserved	Reserved	0x00
17	r	APB_OBM1_OUT	OBM-1 output signal status.	0x00
16	r	APB_OBM0_OUT	OBM-0 output signal status.	0x00
15..13	-	Reserved	Reserved	0x00
12	rw	APB_NCO0F	NCO-0 adder overflow event detect interrupt flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
11..10	-	Reserved	Reserved	0x00
9	rw	APB_OBM1F	OBM-1 break trigger event detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
8	rw	APB_OBM0F	OBM-0 break trigger event detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
7..0	-	Reserved	Reserved	0x00

1.41.2. APB interrupt enable register

APB_INT	APB interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved			APB_NCO0_IE	Reserved		APB_OBM1_IE	APB_OBM0_IE
7	6	5	4	3	2	1	0
Reserved							APB_IEA

Bit	Attr	Bit Name	Description	Reset

31..16	-	Reserved	Reserved	0x0000
15..13	-	Reserved	Reserved	0x00
12	rw	APB_NCO0_IE	NCO-0 adder overflow event detect interrupt enable. 0 = Disable 1 = Enable	0x00
11..10	-	Reserved	Reserved	0x00
9	rw	APB_OBM1_IE	OBM-1 break trigger event detect interrupt enable. 0 = Disable 1 = Enable	0x00
8	rw	APB_OBM0_IE	OBM-0 break trigger event detect interrupt enable. 0 = Disable 1 = Enable	0x00
7..1	-	Reserved	Reserved	0x00
0	rw	APB_IEA	APB interrupt all enable. When disables, the APB global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.41.3. APB global control register 0

APB_CR0	APB global control register 0		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
APB_GPR[7:0]							
15	14	13	12	11	10	9	8
Reserved	APB_IRDAT_MUX[2:0]			Reserved	APB_IRCLK_MUX[2:0]		
7	6	5	4	3	2	1	0
Reserved		APB_IRDAT_INV	APB_IRCLK_INV	Reserved	Reserved		

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..16	rw	APB_GPR	General purpose data register bits.	0x00
15	-	Reserved	Reserved	0x00
14..12	rw	APB_IRDAT_MUX	IR data envelope signal source select. 0x0 = DAT0 : Output 0 0x1 = DAT1 0x2 = DAT2 0x3 = DAT3 0x4 = DAT4 0x5 = DAT5 0x6 = DAT6 0x7 = DAT7	0x00
11	-	Reserved	Reserved	0x00
10..8	rw	APB_IRCLK_MUX	IR carrier clock source select. 0x0 = CLK0 : Output 0 0x1 = CLK1 0x2 = CLK2 0x3 = CLK3 0x4 = CLK4 0x5 = CLK5 0x6 = CLK6 0x7 = CLK7	0x00
7..6	-	Reserved	Reserved	0x00
5	rw	APB_IRDAT_INV	IR data envelope signal inverse enable bit. 0 = Disable 1 = Enable	0x00

4	rw	APB_IRCLK_INV	IR clock signal inverse enable bit. 0 = Disable 1 = Enable	0x00
3	-	Reserved	Reserved	0x00
2..0	-	Reserved	Reserved	0x00

1.41.4. APB global control register 1

APB_CR1	APB global control register 1		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
APB_TM36_EN2	Reserved			APB_TM26_EN2	Reserved	Reserved	APB_TM20_EN2
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
APB_TM16_EN2	Reserved		APB_TM10_EN2	Reserved		APB_TM01_EN2	APB_TM00_EN2
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
APB_TM36_EN	Reserved			APB_TM26_EN	Reserved	Reserved	APB_TM20_EN
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
APB_TM16_EN	Reserved		APB_TM10_EN	Reserved		APB_TM01_EN	APB_TM00_EN

Bit	Attr	Bit Name	Description	Reset
31	w	APB_TM36_EN2	TM36 2nd Timer/Counter enable bit. 0 = No : No effect 1 = Enable	0x00
30..28	-	Reserved	Reserved	0x00
27	w	APB_TM26_EN2	TM26 2nd Timer/Counter enable bit. 0 = No : No effect 1 = Enable	0x00
26	-	Reserved	Reserved	0x00
25	-	Reserved	Reserved	0x00
24	w	APB_TM20_EN2	TM20 2nd Timer/Counter enable bit. 0 = No : No effect 1 = Enable	0x00
23	w	APB_TM16_EN2	TM16 2nd Timer/Counter enable bit. 0 = No : No effect 1 = Enable	0x00
22..21	-	Reserved	Reserved	0x00
20	w	APB_TM10_EN2	TM10 2nd Timer/Counter enable bit. 0 = No : No effect 1 = Enable	0x00
19..18	-	Reserved	Reserved	0x00
17	w	APB_TM01_EN2	TM01 2nd Timer/Counter enable bit. 0 = No : No effect 1 = Enable	0x00
16	w	APB_TM00_EN2	TM00 2nd Timer/Counter enable bit. 0 = No : No effect 1 = Enable	0x00
15	w	APB_TM36_EN	TM36 main Timer/Counter enable bit. 0 = No : No effect 1 = Enable	0x00
14..12	-	Reserved	Reserved	0x00
11	w	APB_TM26_EN	TM26 main Timer/Counter enable bit. 0 =No : No effect 1 = Enable	0x00
10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	w	APB_TM20_EN	TM20 main Timer/Counter enable bit. 0 = No : No effect 1 = Enable	0x00
7	w	APB_TM16_EN	TM16 main Timer/Counter enable bit.	0x00

			0 = No : No effect 1 = Enable	
6..5	-	Reserved	Reserved	0x00
4	w	APB_TM10_EN	TM10 main Timer/Counter enable bit. 0 = No : No effect 1 = Enable	0x00
3..2	-	Reserved	Reserved	0x00
1	w	APB_TM01_EN	TM01 main Timer/Counter enable bit. 0 = No : No effect 1 = Enable	0x00
0	w	APB_TM00_EN	TM00 main Timer/Counter enable bit. 0 = No : No effect 1 = Enable	0x00

1.41.5. APB global control register 2

APB_CR2	APB global control register 2		
Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
APB_ITR7_MUX[3:0]				Reserved	APB_ITR6_MUX[2:0]		

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..8	-	Reserved	Reserved	0x00
7..4	rw	APB_ITR7_MUX	Timer internal common trigger source ITR7 source select. See the [Timer Common ITR6/ITR7 Signals Table] for more information. 0x0 = TRG0 0x1 = TRG1 0x2 = TRG2 0x3 = TRG3 0x4 = TRG4 0x5 = TRG5 0x6 = TRG6 0x7 = TRG7 0x8 = TRG8 0x9 = TRG9 0xA = TRG10 0xB = TRG11	0x00
3	-	Reserved	Reserved	0x00
2..0	rw	APB_ITR6_MUX	Timer internal common trigger source ITR6 source select. See the [Timer Common ITR6/ITR7 Signals Table] for more information. 0x0 = TRG0 0x1 = TRG1 0x2 = TRG2 0x3 = TRG3 0x4 = TRG4 0x5 = TRG5 0x6 = TRG6 0x7 = TRG7	0x00

1.41.6. APB OBM0 control register-0

APB_OBM00	APB OBM0 control register-0		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				APB_OBM0_BKS2[3:0]			
23	22	21	20	19	18	17	16
APB_OBM0_BKS1[3:0]				APB_OBM0_BKS0[3:0]			
15	14	13	12	11	10	9	8
Reserved					APB_OBM0_BKN2	APB_OBM0_BKN1	APB_OBM0_BKN0
7	6	5	4	3	2	1	0
Reserved		APB_OBM0_LCK	APB_OBM0_STA	Reserved		APB_OBM0_MDS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27..24	rw	APB_OBM0_BKS2	OBM0 break signal source channel-2 select. 0x0 = BK0 : Output 1 0x1 = BK1 0x2 = BK2 0x3 = BK3 0x4 = BK4 0x5 = BK5 0x6 = BK6 0x7 = BK7 0x8 = BK8 0x9 = BK9 0xA = BK10 0xB = BK11 0xC = BK12 0xD = BK13 0xE = BK14 0xF = BK15	0x00
23..20	rw	APB_OBM0_BKS1	OBM0 break signal source channel-1 select. 0x0 = BK0 : Output 1 0x1 = BK1 0x2 = BK2 0x3 = BK3 0x4 = BK4 0x5 = BK5 0x6 = BK6 0x7 = BK7 0x8 = BK8 0x9 = BK9 0xA = BK10 0xB = BK11 0xC = BK12 0xD = BK13 0xE = BK14 0xF = BK15	0x00
19..16	rw	APB_OBM0_BKS0	OBM0 break signal source channel-0 select. 0x0 = BK0 : Output 1 0x1 = BK1 0x2 = BK2 0x3 = BK3 0x4 = BK4 0x5 = BK5 0x6 = BK6 0x7 = BK7 0x8 = BK8 0x9 = BK9 0xA = BK10 0xB = BK11	0x00

			0xC = BK12 0xD = BK13 0xE = BK14 0xF = BK15	
15..11	-	**Reserved**	Reserved	0x00
10	rw	**APB_OBM0_BKN2**	OBM0 break source-2 signal inverse enable bit. 0 = Disable 1 = Enable	0x00
9	rw	**APB_OBM0_BKN1**	OBM0 break source-1 signal inverse enable bit. 0 = Disable 1 = Enable	0x00
8	rw	**APB_OBM0_BKN0**	OBM0 break source-0 signal inverse enable bit. 0 = Disable 1 = Enable	0x00
7..6	-	**Reserved**	Reserved	0x00
5	rw	**APB_OBM0_LCK**	OBM0 break switching signal initial state write control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	0x00
4	rw	**APB_OBM0_STA**	OBM0 break switching signal initial state. The bit is written effectively only by written 1 to APB_OBM0_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
3..2	-	**Reserved**	Reserved	0x00
1..0	rw	**APB_OBM0_MDS**	OBM0 break operation mode select. User selects the mode to control the APB_OBM0_SW signal. When selects AND, the APB_OBM0_SW signal is directly controlled by the AND signal of all break channels' output. When selects CLR/SET/TOGGLE, the APB_OBM0_SW signal is controlled by STA(APB_OBM0_STA) bit and can update by firmware. 0x0 = AND : AND signal of all break channels' output 0x1 = CLR : STA bit is cleared by falling edge of OR signal 0x2 = SET : STA bit is set by falling edge of OR signal 0x3 = TOGGLE : STA bit is toggle by falling edge of OR signal	0x00

1.41.7. APB OBM0 control register-1

APB_OBM01	APB OBM0 control register-1		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
APB_OBM0_MUX1[3:0]				APB_OBM0_MUX0[3:0]			
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		APB_OBM0_FCKS[1:0]		Reserved	APB_OBM0_POL	APB_OBM0_INV1	APB_OBM0_INV0

Bit	Attr	Bit Name	Description	Reset
31..24	-	**Reserved**	Reserved	0x00
23..20	rw	**APB_OBM0_MUX1**	OBM0 output source channel-1 signal select. 0x0 = SR0 : Output 0 0x1 = SR1 0x2 = SR2 0x3 = SR3 0x4 = SR4 0x5 = SR5	0x00

			0x6 = SR6 0x7 = SR7 0x8 = SR8 0x9 = SR9 0xA = SR10 0xB = SR11 0xC = SR12 0xD = SR13 0xE = SR14 0xF = SR15	
19..16	rw	APB_OBM0_MUX0	OBM0 output source channel-0 signal select. 0x0 = SR0 : Output 0 0x1 = SR1 0x2 = SR2 0x3 = SR3 0x4 = SR4 0x5 = SR5 0x6 = SR6 0x7 = SR7 0x8 = SR8 0x9 = SR9 0xA = SR10 0xB = SR11 0xC = SR12 0xD = SR13 0xE = SR14 0xF = SR15	0x00
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5..4	rw	APB_OBM0_FCKS	OBM0 output deglitch filter clock source select. The filter is filtering the output signal by sampling 3-times. 0x0 = Disable 0x1 = APB : CLK_APB 0x2 = APB_DIV8 : CLK_APB divide by 8 0x3 = TM00_TRGO	0x00
3	-	Reserved	Reserved	0x00
2	rw	APB_OBM0_POL	OBM0 output signal inverse enable bit. 0 = Disable 1 = Enable	0x00
1	rw	APB_OBM0_INV1	OBM0 source channel-1 signal inverse enable bit. 0 = Disable 1 = Enable	0x00
0	rw	APB_OBM0_INV0	OBM0 source channel-0 signal inverse enable bit. 0 = Disable 1 = Enable	0x00

1.41.8. APB OBM1 control register-0

APB_OBM10	APB OBM1 control register-0		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved				APB_OBM1_BKS2[3:0]			
23	22	21	20	19	18	17	16
APB_OBM1_BKS1[3:0]				APB_OBM1_BKS0[3:0]			
15	14	13	12	11	10	9	8
Reserved					APB_OBM1_BKN2	APB_OBM1_BKN1	APB_OBM1_BKN0
7	6	5	4	3	2	1	0
Reserved		APB_OBM1_LCK	APB_OBM1_STA	Reserved		APB_OBM1_MDS[1:0]	

Bit	Attr	Bit Name	Description	Reset
31..28	-	Reserved	Reserved	0x00
27..24	rw	APB_OBM1_BKS2	OBM1 break signal source channel-2 select. 0x0 = BK0 : Output 1 0x1 = BK1 0x2 = BK2 0x3 = BK3 0x4 = BK4 0x5 = BK5 0x6 = BK6 0x7 = BK7 0x8 = BK8 0x9 = BK9 0xA = BK10 0xB = BK11 0xC = BK12 0xD = BK13 0xE = BK14 0xF = BK15	0x00
23..20	rw	APB_OBM1_BKS1	OBM1 break signal source channel-1 select. 0x0 = BK0 : Output 1 0x1 = BK1 0x2 = BK2 0x3 = BK3 0x4 = BK4 0x5 = BK5 0x6 = BK6 0x7 = BK7 0x8 = BK8 0x9 = BK9 0xA = BK10 0xB = BK11 0xC = BK12 0xD = BK13 0xE = BK14 0xF = BK15	0x00
19..16	rw	APB_OBM1_BKS0	OBM1 break signal source channel-0 select. 0x0 = BK0 : Output 1 0x1 = BK1 0x2 = BK2 0x3 = BK3 0x4 = BK4 0x5 = BK5 0x6 = BK6 0x7 = BK7 0x8 = BK8 0x9 = BK9 0xA = BK10 0xB = BK11 0xC = BK12 0xD = BK13 0xE = BK14 0xF = BK15	0x00
15..11	-	Reserved	Reserved	0x00
10	rw	APB_OBM1_BKN2	OBM1 break source-2 signal inverse enable bit. 0 = Disable 1 = Enable	0x00
9	rw	APB_OBM1_BKN1	OBM1 break source-1 signal inverse enable bit. 0 = Disable 1 = Enable	0x00
8	rw	APB_OBM1_BKN0	OBM1 break source-0 signal inverse enable bit.	0x00

			0 = Disable 1 = Enable	
7..6	-	Reserved	Reserved	0x00
5	rw	APB_OBM1_LCK	OBM1 break switching signal initial state write control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked 1 = Un-Locked	0x00
4	rw	APB_OBM1_STA	OBM1 break switching signal initial state. The bit is written effectively only by written 1 to APB_OBM1_LCK simultaneously. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
3..2	-	Reserved	Reserved	0x00
1..0	rw	APB_OBM1_MDS	OBM1 break operation mode select. User select the mode to control the APB_OBM1_SW signal. When selects AND, the APB_OBM1_SW signal is directly controlled by the AND signal of all break channels' output. When selects CLR/SET/TOGGLE, the APB_OBM1_SW signal is controlled by STA(APB_OBM1_STA) bit and can update by firmware. 0x0 = AND : AND signal of all break channels' output 0x1 = CLR : STA bit is cleared by falling edge of OR signal 0x2 = SET : STA bit is set by falling edge of OR signal 0x3 = TOGGLE : STA bit is toggle by falling edge of OR signal	0x00

1.41.9. APB OBM1 control register-1

APB_OBM11	APB OBM1 control register-1		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
APB_OBM1_MUX1[3:0]				APB_OBM1_MUX0[3:0]			
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		APB_OBM1_FCKS[1:0]		Reserved	APB_OBM1_POL	APB_OBM1_INV1	APB_OBM1_INV0

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..20	rw	APB_OBM1_MUX1	OBM1 output source channel-1 signal select. 0x0 = SR0 : Output 0 0x1 = SR1 0x2 = SR2 0x3 = SR3 0x4 = SR4 0x5 = SR5 0x6 = SR6 0x7 = SR7 0x8 = SR8 0x9 = SR9 0xA = SR10 0xB = SR11 0xC = SR12 0xD = SR13 0xE = SR14 0xF = SR15	0x00
19..16	rw	APB_OBM1_MUX0	OBM1 output source channel-0 signal select. 0x0 = SR0 : Output 0	0x00

			0x1 = SR1 0x2 = SR2 0x3 = SR3 0x4 = SR4 0x5 = SR5 0x6 = SR6 0x7 = SR7 0x8 = SR8 0x9 = SR9 0xA = SR10 0xB = SR11 0xC = SR12 0xD = SR13 0xE = SR14 0xF = SR15	
15..8	-	Reserved	Reserved	0x00
7..6	-	Reserved	Reserved	0x00
5..4	rw	APB_OBM1_FCKS	OBM1 output deglitch filter clock source select. The filter is filtering the output signal by sampling 3-times. 0x0 = Disable 0x1 = APB : CLK_APB 0x2 = APB_DIV8 : CLK_APB divide by 8 0x3 = TM00_TRGO	0x00
3	-	Reserved	Reserved	0x00
2	rw	APB_OBM1_POL	OBM1 output signal inverse enable bit. 0 = Disable 1 = Enable	0x00
1	rw	APB_OBM1_INV1	OBM1 source channel-1 signal inverse enable bit. 0 = Disable 1 = Enable	0x00
0	rw	APB_OBM1_INV0	OBM1 source channel-0 signal inverse enable bit. 0 = Disable 1 = Enable	0x00

1.41.10. APB NCO0 increment register

APB_NCO00	APB NCO0 increment register		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	APB_NCO0_CKS[2:0]			Reserved	APB_NCO0_MDS	APB_NCO0_INV	APB_NCO0_EN
23	22	21	20	19	18	17	16
Reserved				APB_NCO0_INC[19:16]			
15	14	13	12	11	10	9	8
APB_NCO0_INC[15:8]							
7	6	5	4	3	2	1	0
APB_NCO0_INC[7:0]							

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30..28	rw	APB_NCO0_CKS	NCO input clock source select. 0x0 = CK_IHRCO 0x1 = CK_PLL 0x2 = CK_APB 0x3 = CK_LS 0x4 = TM00_TRGO 0x5 = NCO_CK0	0x00
27	-	Reserved	Reserved	0x00
26	rw	APB_NCO0_MDS	NCO output mode select. The NCO output frequency needs to be smaller than 1/4 APB clock frequency.	0x00

			0 = FDC : fixed duty cycle mode 1 = PFM : pulse frequency mode	
25	rw	APB_NCO0_INV	NCO output inverse enable. 0 = Disable 1 = Enable	0x00
24	rw	APB_NCO0_EN	NCO enable bit. 0 = Disable 1 = Enable	0x00
23..20	-	Reserved	Reserved	0x00
19..0	rw	APB_NCO0_INC	NCO adder increment value. The register value needs to be equal or smaller than 2^19.	0x000000

1.41.11. APB NCO0 accumulator register

APB_NCO01	APB NCO0 accumulator register		
Offset Address :	0x44	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved					APB_NCO0_PWS[2:0]		
23	22	21	20	19	18	17	16
Reserved				APB_NCO0_ACC[19:16]			
15	14	13	12	11	10	9	8
APB_NCO0_ACC[15:8]							
7	6	5	4	3	2	1	0
APB_NCO0_ACC[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..27	-	Reserved	Reserved	0x00
26..24	rw	APB_NCO0_PWS	NCO PFM mode output pulse width select. 0x0 = CK1 : 1 CK_NCOn clock period 0x1 = CK2 : 2 CK_NCOn clock period 0x2 = CK4 : 4 CK_NCOn clock period 0x3 = CK8 : 8 CK_NCOn clock period 0x4 = CK16 : 16 CK_NCOn clock period 0x5 = CK32 : 32 CK_NCOn clock period 0x6 = CK64 : 64 CK_NCOn clock period 0x7 = CK128 : 128 CK_NCOn clock period	0x00
23..20	-	Reserved	Reserved	0x00
19..0	rw	APB_NCO0_ACC	NCO adder accumulator store data. The read value will be the transient value of the adder value.　It is strongly suggestion that this register is not to changed by write access during the accumulator working.	0x000000

1.41.12. APB Register Map

APB Register Map Register Number = 11

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	APB_STA	Reserved				Reserved		APB_OBM1_SW	APB_OBM0_SW	Reserved			APB_NCO0_OUT	Reserved		APB_OBM1_OUT	APB_OBM0_OUT	Reserved			APB_NCO0F	Reserved		APB_OBM1F	APB_OBM0F	Reserved							
Reset	0x03000000	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	APB_INT	Reserved																Reserved			APB_NCO0_IE	Reserved		APB_OBM1_IE	APB_OBM0_IE	Reserved							APB_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	APB_CR0	Reserved								APB_GPR[7:0]								Reserved	APB_IRDAT_MUX [2:0]			Reserved	APB_IRCLK_MUX [2:0]			Reserved		APB_IRDAT_INV	APB_IRCLK_INV	Reserved	Reserved		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	APB_CR1	APB_TM36_EN2	Reserved			APB_TM26_EN2	Reserved	Reserved	APB_TM20_EN2	APB_TM16_EN2	Reserved		APB_TM10_EN2	Reserved		APB_TM01_EN2	APB_TM00_EN2	APB_TM36_EN	Reserved			APB_TM26_EN	Reserved	Reserved	APB_TM20_EN	APB_TM16_EN	Reserved		APB_TM10_EN	Reserved		APB_TM01_EN	APB_TM00_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	APB_CR2	Reserved																Reserved								APB_ITR7_MUX [3:0]				Reserved	APB_ITR6_MUX [2:0]		
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	APB_OBM00	Reserved				APB_OBM0_BKS2 [3:0]				APB_OBM0_BKS1 [3:0]				APB_OBM0_BKS0 [3:0]				Reserved					APB_OBM0_BKN2	APB_OBM0_BKN1	APB_OBM0_BKN0	Reserved		APB_OBM0_LCK	APB_OBM0_STA	Reserved		APB_OBM0_MDS [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	APB_OBM01	Reserved								APB_OBM0_MUX1 [3:0]				APB_OBM0_MUX0 [3:0]				Reserved								Reserved		APB_OBM0_FCKS [1:0]		Reserved	APB_OBM0_POL	APB_OBM0_INV1	APB_OBM0_INV0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	APB_OBM10	Reserved				APB_OBM1_BKS2 [3:0]				APB_OBM1_BKS1 [3:0]				APB_OBM1_BKS0 [3:0]				Reserved					APB_OBM1_BKN2	APB_OBM1_BKN1	APB_OBM1_BKN0	Reserved		APB_OBM1_LCK	APB_OBM1_STA	Reserved		APB_OBM1_MDS [1:0]	
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x2C	APB_OBM11	Reserved								APB_OBM1_MUX1 [3:0]				APB_OBM1_MUX0 [3:0]				Reserved								Reserved		APB_OBM1_FCKS [1:0]		Reserved	APB_OBM1_POL	APB_OBM1_INV1	APB_OBM1_INV0
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	APB_NCO00	Reserved	APB_NCO0_CKS [2:0]			Reserved	APB_NCO0_MDS	APB_NCO0_INV	APB_NCO0_EN	Reserved				APB_NCO0_INC [19:0]																			
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x44	APB_NCO01	Reserved					APB_NCO0_PWS [2:0]			Reserved				APB_NCO0_ACC [19:0]																			
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.42. APX Control Registers

APX Control	(APX) APB Module Extended Control
Base Address :	0x5F010000

1.42.1. APB status register

APX_STA	APB status register		
Offset Address :	0x00	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved						APX_CCL1_OUT	APX_CCL0_OUT
23	22	21	20	19	18	17	16
Reserved						APX_CCL1F	APX_CCL0F
15	14	13	12	11	10	9	8
Reserved		APX_SDTF5	APX_SDTF4	Reserved	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0
Reserved							Reserved

Bit	Attr	Bit Name	Description	Reset
31..26	-	Reserved	Reserved	0x00
25	r	APX_CCL1_OUT	CCL-1 output status bit.	0x00
24	r	APX_CCL0_OUT	CCL-0 output status bit.	0x00
23..18	-	Reserved	Reserved	0x00
17	rw	APX_CCL1F	CCL-1 output low-to-high detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
16	rw	APX_CCL0F	CCL-0 output low-to-high detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
15..14	-	Reserved	Reserved	0x00
13	rw	APX_SDTF5	SDT state procedures-5 detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
12	rw	APX_SDTF4	SDT state procedures-4 detect flag. (set by hardware and clear by software writing 1) 0 = Normal (No event occurred) 1 = Happened (reset event happened)	0x00
11	-	Reserved	Reserved	0x00
10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7..1	-	Reserved	Reserved	0x00
0	-	Reserved	Reserved	0x00

1.42.2. APX interrupt enable register

APX_INT	APX interrupt enable register		
Offset Address :	0x04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						APX_CCL1_IE	APX_CCL0_IE
15	14	13	12	11	10	9	8
Reserved		APX_SDT_IE5	APX_SDT_IE4	Reserved	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0

Reserved	Reserved	APX_IEA

Bit	Attr	Bit Name	Description	Reset
31..24	-	Reserved	Reserved	0x00
23..18	-	Reserved	Reserved	0x00
17	rw	APX_CCL1_IE	CCL-1 output low-to-high detect interrupt enable. 0 = Disable 1 = Enable	0x00
16	rw	APX_CCL0_IE	CCL-0 output low-to-high detect interrupt enable. 0 = Disable 1 = Enable	0x00
15..14	-	Reserved	Reserved	0x00
13	rw	APX_SDT_IE5	SDT state procedure-5 detect interrupt enable. (User definition mode procedure) 0 = Disable 1 = Enable	0x00
12	rw	APX_SDT_IE4	SDT state procedure-4 detect interrupt enable. (User definition mode procedure) 0 = Disable 1 = Enable	0x00
11	-	Reserved	Reserved	0x00
10	-	Reserved	Reserved	0x00
9	-	Reserved	Reserved	0x00
8	-	Reserved	Reserved	0x00
7..4	-	Reserved	Reserved	0x00
3..1	-	Reserved	Reserved	0x00
0	rw	APX_IEA	APX interrupt all enable. When disables, the APX global all interrupt event are disabled. When enables, the related event interrupt enable bit is to enable or disable the interrupt. 0 = Disable 1 = Enable	0x00

1.42.3. APX CCL0 control register-0

APX_CCL00	APX CCL0 control register-0		
Offset Address :	0x20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	Reserved	Reserved				APX_CCL0_SQIN[1:0]	
23	22	21	20	19	18	17	16
APX_CCL0_TRUTH[7:0]							
15	14	13	12	11	10	9	8
Reserved		APX_CCL0_DIV[1:0]		APX_CCL0_INV	APX_CCL0_SQSEL[2:0]		
7	6	5	4	3	2	1	0
APX_CCL0_EDSEL[1:0]		APX_CCL0_FTSEL[1:0]		Reserved		APX_CCL0_TEN	APX_CCL0_EN

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29..26	-	Reserved	Reserved	0x00
25..24	rw	APX_CCL0_SQIN	CCL sequential logic input CCL_S0 select. 0x0 = 0 0x1 = 1 0x2 = CCL_S1 0x3 = Reserved	0x00
23..16	rw	APX_CCL0_TRUTH	CCL lookup truth table output value definitions for mapping input states. OUT : IN0, IN1, IN2 [0] : 0, 0, 0 [1] : 0, 0, 1	0x00

			[2] : 0, 1, 0 [3] : 0, 1, 1 [4] : 1, 0, 0 [5] : 1, 0, 1 [6] : 1, 1, 0 [7] : 1, 1, 1	
15..14	-	Reserved	Reserved	0x00
13..12	rw	APX_CCL0_DIV	CCL internal clock input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
11	rw	APX_CCL0_INV	CCL output inverse enable bit. 0 = Disable 1 = Enable	0x00
10..8	rw	APX_CCL0_SQSEL	CCL sequential logic mode select. 0x0 = Disable 0x1 = DFF : D flip flop 0x2 = JK : JK flip flop 0x3 = DLH : D latch 0x4 = RS : RS latch	0x00
7..6	rw	APX_CCL0_EDSEL	CCL edge detector mode select. 0x0 = Disable 0x1 = Rising 0x2 = Falling 0x3 = Dual-edge	0x00
5..4	rw	APX_CCL0_FTSEL	CCL filter select. 0x0 = Disable 0x1 = SYNC : Synchronizer enabled 0x2 = FILTER : Filter enabled 0x3 = Reserved	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	APX_CCL0_TEN	CCL truth table enable bit. 0 = Disable 1 = Enable	0x00
0	rw	APX_CCL0_EN	CCL enable bit. 0 = Disable 1 = Enable	0x00

1.42.4. APX CCL0 control register-1

APX_CCL01	APX CCL0 control register-1		
Offset Address :	0x24	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				APX_CCL0_MUX2[3:0]			
7	6	5	4	3	2	1	0
APX_CCL0_MUX1[3:0]				APX_CCL0_MUX0[3:0]			

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	-	Reserved	Reserved	0x00
11..8	rw	APX_CCL0_MUX2	CCL IN2 input Mux select. 0x0 = Disable : Mask input 0x1 = IN01 : Feedback from CCLn_SEQ signal 0x2 = IN02 : Link from CCLn_AO signal	0x00

			0x3 = IN03 : PC1 0x4 = IN04 : PA10 0x5 = IN05 : PB2 0x6 = IN06 : PB10 0x7 = IN07 : PE2 0x8 = IN08 : ADC0_OUT 0x9 = IN09 : URT4_TX 0xA = IN0A : SPI0_CLK 0xB = IN0B : TM36_OC2 0xC = IN0C : TM20_OC00 0xD = IN0D : SDT_P0 0xE = IN0E : OBM_I1 0xF = IN0F : Reserved	
7..4	rw	**APX_CCL0_MUX1**	CCL IN1 input Mux select. 0x0 = Disable : Mask input 0x1 = IN01 : Feedback from CCLn_SEQ signal 0x2 = IN02 : Link from CCLn_AO signal 0x3 = IN03 : PB3 0x4 = IN04 : PA9 0x5 = IN05 : PB1 0x6 = IN06 : PB9 0x7 = IN07 : PE1 0x8 = IN08 : CMP1_OUT 0x9 = IN09 : URT1_TX 0xA = IN0A : SPI0_MISO (output for SPI slave mode) 0xB = IN0B : TM36_OC10 0xC = IN0C : TM26_OC10 0xD = IN0D : SDT_I1 0xE = IN0E : OBM_I0 0xF = IN0F : Reserved	0x00
3..0	rw	**APX_CCL0_MUX0**	CCL IN0 input Mux select. 0x0 = Disable : Mask input 0x1 = IN01 : Feedback from CCLn_SEQ signal 0x2 = IN02 : Link from CCLn_AO signal 0x3 = IN03 : PB11 0x4 = IN04 : PA8 0x5 = IN05 : PB0 0x6 = IN06 : PB8 0x7 = IN07 : PE0 0x8 = IN08 : CMP0_OUT 0x9 = IN09 : URT0_TX 0xA = IN0A : SPI0_MOSI (output for SPI master mode) 0xB = IN0B : TM36_OC00 0xC = IN0C : TM26_OC00 0xD = IN0D : SDT_I0 0xE = IN0E : OBM_P0 0xF = IN0F : Reserved	0x00

1.42.5. APX CCL1 control register-0

APX_CCL10	APX CCL1 control register-0		
Offset Address :	0x28	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	Reserved	Reserved				APX_CCL1_SQIN[1:0]	
23	22	21	20	19	18	17	16
APX_CCL1_LUT[7:0]							
15	14	13	12	11	10	9	8
Reserved		APX_CCL1_DIV[1:0]		APX_CCL1_INV	APX_CCL1_SQSEL[2:0]		
7	6	5	4	3	2	1	0
APX_CCL1_EDSEL[1:0]		APX_CCL1_FTSEL[1:0]		Reserved		APX_CCL1_TEN	APX_CCL1_EN

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30	-	Reserved	Reserved	0x00
29..26	-	Reserved	Reserved	0x00
25..24	rw	APX_CCL1_SQIN	CCL sequential logic input CCL_S1 select. 0x0 = 0 0x1 = 1 0x2 = Reserved 0x3 = Reserved	0x00
23..16	rw	APX_CCL1_LUT	CCL lookup truth table output value definitions for mapping input states. OUT : IN0, IN1, IN2 [0] : 0, 0, 0 [1] : 0, 0, 1 [2] : 0, 1, 0 [3] : 0, 1, 1 [4] : 1, 0, 0 [5] : 1, 0, 1 [6] : 1, 1, 0 [7] : 1, 1, 1	0x00
15..14	-	Reserved	Reserved	0x00
13..12	rw	APX_CCL1_DIV	CCL internal clock input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
11	rw	APX_CCL1_INV	CCL output inverse enable bit. 0 = Disable 1 = Enable	0x00
10..8	rw	APX_CCL1_SQSEL	CCL sequential logic mode select. 0x0 = Disable 0x1 = DFF : D flip flop 0x2 = JK : JK flip flop 0x3 = DLH : D latch 0x4 = RS : RS latch	0x00
7..6	rw	APX_CCL1_EDSEL	CCL edge detector mode select. 0x0 = Disable 0x1 = Rising 0x2 = Falling 0x3 = Dual-edge	0x00
5..4	rw	APX_CCL1_FTSEL	CCL filter select. 0x0 = Disable 0x1 = SYNC : Synchronizer enabled 0x2 = FILTER : Filter enabled 0x3 = Reserved	0x00
3..2	-	Reserved	Reserved	0x00
1	rw	APX_CCL1_TEN	CCL truth table enable bit. 0 = Disable 1 = Enable	0x00
0	rw	APX_CCL1_EN	CCL enable bit. 0 = Disable 1 = Enable	0x00

1.42.6. APX CCL1 control register-1

APX_CCL11	APX CCL1 control register-1		
Offset Address :	0x2C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24

Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				APX_CCL1_MUX2[3:0]			
7	6	5	4	3	2	1	0
APX_CCL1_MUX1[3:0]				APX_CCL1_MUX0[3:0]			

Bit	Attr	Bit Name	Description	Reset
31..16	-	Reserved	Reserved	0x0000
15..12	-	Reserved	Reserved	0x00
11..8	rw	APX_CCL1_MUX2	CCL IN2 input Mux select. 0x0 = Disable : Mask input 0x1 = IN01 : Feedback from CCLn_SEQ signal 0x2 = IN02 : Link from CCLn_AO signal 0x3 = IN03 : PC1 0x4 = IN04 : PA10 0x5 = IN05 : PB2 0x6 = IN06 : PB10 0x7 = IN07 : PE2 0x8 = IN08 : ADC0_OUT 0x9 = IN09 : URT4_TX 0xA = IN0A : SPI0_CLK 0xB = IN0B : TM36_OC2 0xC = IN0C : TM20_OC00 0xD = IN0D : SDT_P0 0xE = IN0E : OBM_I1 0xF = IN0F : Reserved	0x00
7..4	rw	APX_CCL1_MUX1	CCL IN1 input Mux select. 0x0 = Disable : Mask input 0x1 = IN01 : Feedback from CCLn_SEQ signal 0x2 = IN02 : Link from CCLn_AO signal 0x3 = IN03 : PB3 0x4 = IN04 : PA9 0x5 = IN05 : PB1 0x6 = IN06 : PB9 0x7 = IN07 : PE1 0x8 = IN08 : CMP1_OUT 0x9 = IN09 : URT1_TX 0xA = IN0A : SPI0_MISO (output) 0xB = IN0B : TM36_OC10 0xC = IN0C : TM26_OC10 0xD = IN0D : SDT_I1 0xE = IN0E : OBM_I0 0xF = IN0F : Reserved	0x00
3..0	rw	APX_CCL1_MUX0	CCL IN0 input Mux select. 0x0 = Disable : Mask input 0x1 = IN01 : Feedback from CCLn_SEQ signal 0x2 = IN02 : Link from CCLn_AO signal 0x3 = IN03 : PB11 0x4 = IN04 : PA8 0x5 = IN05 : PB0 0x6 = IN06 : PB8 0x7 = IN07 : PE0 0x8 = IN08 : CMP0_OUT 0x9 = IN09 : URT0_TX 0xA = IN0A : SPI0_MOSI (output) 0xB = IN0B : TM36_OC00 0xC = IN0C : TM26_OC00 0xD = IN0D : SDT_I0 0xE = IN0E : OBM_P0	0x00

			0xF = IN0F : Reserved	

1.42.7. APX SDT control register-0

APX_SDT0	APX SDT control register-0		
Offset Address :	0x40	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
APX_SDT_LCK	APX_SDT_PSTA	Reserved					Reserved
23	22	21	20	19	18	17	16
Reserved	Reserved			Reserved	Reserved		
15	14	13	12	11	10	9	8
Reserved				APX_SDT_PSEL[3:0]			
7	6	5	4	3	2	1	0
APX_SDT_PMDS	Reserved	APX_SDT_DIV[1:0]		Reserved		Reserved	APX_SDT_EN

Bit	Attr	Bit Name	Description	Reset
31	rw	APX_SDT_LCK	APX_SDT_PSTA register write access protected control. When locked, disables the register bit write access. Hardware auto clear after register write access. 0 = Locked (enable chip hardware control) 1 = Un-Locked (disable chip hardware control)	0x00
30	rw	APX_SDT_PSTA	SDT pin SDT_P0 output initial state. The bit is written effectively only by written 1 to APX_SDT_LCK simultaneously. When APX_SDT_PMDS = 'Normal', the bit is no effect and the SDT_P0 output is directly outputted the high active signal. 0 = 0 (Output 0) 1 = 1 (Output 1)	0x00
29..25	-	Reserved	Reserved	0x00
24	-	Reserved	Reserved	0x00
23	-	Reserved	Reserved	0x00
22..20	-	Reserved	Reserved	0x00
19	-	Reserved	Reserved	0x00
18..16	-	Reserved	Reserved	0x00
15..12	-	Reserved	Reserved	0x00
11..8	rw	APX_SDT_PSEL	SDT output pin SDT_P0 source select. 0x0 = Reserved 0x1 = Reserved 0x2 = Reserved 0x3 = Reserved 0x4 = PROC4 : state procedure-4 detect event 0x5 = PROC5 : state procedure-5 detect event 0x6 = Reserved 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved	0x00
7	rw	APX_SDT_PMDS	SDT pin SDT_P0 output mode select. 0 = Normal : signal directly output 1 = Toggle : output toggle by detect event	0x00
6	-	Reserved	Reserved	0x00
5..4	rw	APX_SDT_DIV	SDT internal clock input divider. 0x0 = DIV1 : divided by 1 0x1 = DIV2 : divided by 2 0x2 = DIV4 : divided by 4 0x3 = DIV8 : divided by 8	0x00
3..2	-	Reserved	Reserved	0x00
1	-	Reserved	Reserved	0x00
0	rw	APX_SDT_EN	SDT state detector enable bit. 0 = Disable	0x00

			1 = Enable	

1.42.8. APX SDT control register-1

APX_SDT1	APX SDT control register-1		
Offset Address :	0x44	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved	APX_SDT_P5E[2:0]			Reserved		APX_SDT_P5S[9:8]	
23	22	21	20	19	18	17	16
APX_SDT_P5S[7:0]							
15	14	13	12	11	10	9	8
Reserved	APX_SDT_P4E[2:0]			Reserved		APX_SDT_P4S[9:8]	
7	6	5	4	3	2	1	0
APX_SDT_P4S[7:0]							

Bit	Attr	Bit Name	Description	Reset
31	-	Reserved	Reserved	0x00
30..28	rw	APX_SDT_P5E	SDT state procedure-5 detect end state index. The value 0 to 4 are indicated state index-1 to 5..	0x00
27..26	-	Reserved	Reserved	0x00
25..16	rw	APX_SDT_P5S	SDT state procedure-5 detect input line state setting value. [0,1] : state-1 value of input line-0,1 [2,3] : state-2 value of input line-0,1 [4,5] : state-3 value of input line-0,1 [6,7] : state-4 value of input line-0,1 [8,9] : state-5 value of input line-0,1	0x0000
15	-	Reserved	Reserved	0x00
14..12	rw	APX_SDT_P4E	SDT state procedure-4 detect end state index. The value 0 to 4 are indicated state index-1 to 5..	0x00
11..10	-	Reserved	Reserved	0x00
9..0	rw	APX_SDT_P4S	SDT state procedure-4 detect input line state setting value. [0,1] : state-1 value of input line-0,1 [2,3] : state-2 value of input line-0,1 [4,5] : state-3 value of input line-0,1 [6,7] : state-4 value of input line-0,1 [8,9] : state-5 value of input line-0,1	0x0000

1.42.9. APX Register Map

APX Register Map Register Number = 8

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	APX_STA	Reserved						APX_CCL1_OUT	APX_CCL0_OUT	Reserved						APX_CCL1F	APX_CCL0F	Reserved		APX_SDTF5	APX_SDTF4	Reserved	Reserved	Reserved	Reserved	Reserved							Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	APX_INT	Reserved								Reserved						APX_CCL1_IE	APX_CCL0_IE	Reserved		APX_SDT_IE5	APX_SDT_IE4	Reserved	Reserved	Reserved	Reserved	Reserved				Reserved			APX_IEA
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	APX_CCL00	Reserved	Reserved	Reserved				APX_CCL0_SQIN [1:0]		APX_CCL0_TRUTH [7:0]								Reserved		APX_CCL0_DIV [1:0]		APX_CCL0_INV	APX_CCL0_SQSEL [2:0]			APX_CCL0_EDSEL [1:0]		APX_CCL0_FTSEL [1:0]		Reserved		APX_CCL0_TEN	APX_CCL0_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	APX_CCL01	Reserved																Reserved				APX_CCL0_MUX2 [3:0]				APX_CCL0_MUX1 [3:0]				APX_CCL0_MUX0 [3:0]			
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	APX_CCL10	Reserved	Reserved	Reserved				APX_CCL1_SQIN [1:0]		APX_CCL1_LUT [7:0]								Reserved		APX_CCL1_DIV [1:0]		APX_CCL1_INV	APX_CCL1_SQSEL [2:0]			APX_CCL1_EDSEL [1:0]		APX_CCL1_FTSEL [1:0]		Reserved		APX_CCL1_TEN	APX_CCL1_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	APX_CCL11	Reserved																Reserved				APX_CCL1_MUX2 [3:0]				APX_CCL1_MUX1 [3:0]				APX_CCL1_MUX0 [3:0]			
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	APX_SDT0	APX_SDT_LCK	APX_SDT_PSTA	Reserved					Reserved	Reserved	Reserved			Reserved	Reserved			Reserved				APX_SDT_PSEL [3:0]				APX_SDT_PMDS	Reserved	APX_SDT_DIV [1:0]		Reserved		Reserved	APX_SDT_EN
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x44	APX_SDT1	Reserved	APX_SDT_P5E [2:0]			Reserved		APX_SDT_P5S [9:0]										Reserved	APX_SDT_P4E [2:0]			Reserved		APX_SDT_P4S [9:0]									
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.43. CPU PPB SCS Registers

CPU PPB SCS	(CPU) CPU Private Peripheral Bus Control
Base Address :	0xE000E000

1.43.1. CPU SysTick Control and Status Register

CPU_SYST_CSR	CPU SysTick Control and Status Register		
Offset Address :	0x10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							COUNTFLAG
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					CLKSOURCE	TICKINT	ENCNT

Bit	Attr	Bit Name	Description	Reset
31..17	rw	Reserved	Reserved	0x00
16	r	COUNTFLAG	Returns 1 if timer counted to 0 since the last read of this register.	0x00
15..3	rw	Reserved	Reserved	0x00
2	rw	CLKSOURCE	Selects the SysTick timer clock source. 0 = reference clock (external reference clock) 1 = processor clock If your device does not implement a reference clock, this bit reads-as-one and ignores writes.	0x00
1	rw	TICKINT	Enables SysTick exception request: 0 = NotAssert : counting down to zero does not assert the SysTick exception request 1 = Assert : counting down to zero to asserts the SysTick exception request	0x00
0	rw	ENCNT	Enables the counter: 0 = Disable : counter disabled 1 = Enable : counter enabled.	0x00

1.43.2. CPU SysTick Reload Value Register

CPU_SYST_RVR	CPU SysTick Reload Value Register		
Offset Address :	0x14	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
RELOAD[23:16]							
15	14	13	12	11	10	9	8
RELOAD[15:8]							
7	6	5	4	3	2	1	0
RELOAD[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	rw	Reserved	Reserved	0x00
23..0	rw	RELOAD	Value to load into the SYST_CVR when the counter is enabled and when it reaches 0.	0x000000

1.43.3. CPU SysTick Current Value Register

CPU_SYST_CVR	CPU SysTick Current Value Register

Offset Address :	0x18	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
CURRENT[23:16]							
15	14	13	12	11	10	9	8
CURRENT[15:8]							
7	6	5	4	3	2	1	0
CURRENT[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..24	rw	Reserved	Reserved	0x00
23..0	rw	CURRENT	Reads return the current value of the SysTick counter. A write of any value clears the field to 0, and also clears the SYST_CSR.COUNTFLAG bit to 0.	0x000000

1.43.4. CPU SysTick Calibration Value Register

CPU_SYST_CALIB	CPU SysTick Calibration Value Register		
Offset Address :	0x1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
NOREF	SKEW	Reserved					
23	22	21	20	19	18	17	16
TENMS[23:16]							
15	14	13	12	11	10	9	8
TENMS[15:8]							
7	6	5	4	3	2	1	0
TENMS[7:0]							

Bit	Attr	Bit Name	Description	Reset
31	r	NOREF	Indicates whether the device provides a reference clock to the processor: 0 = Refer : reference clock provided 1 = Proc : processor clock provided. If your device does not provide a reference clock, the SYST_CSR.CLKSOURCE bit reads-as-one and ignores writes.	0x00
30	r	SKEW	Indicates whether the TENMS value is exact: 0 = exact : TENMS value is exact 1 = inexact : TENMS value is inexact, or not given. An inexact TENMS value can affect the suitability of SysTick as a software real time clock.	0x00
29..24	r	Reserved	Reserved	0x00
23..0	r	TENMS	Reload value for 10ms (100Hz) timing, subject to system clock skew errors. If the value reads as zero, the calibration value is not known.	0x000000

1.43.5. CPU Interrupt Set-enable Register

CPU_ISER	CPU Interrupt Set-enable Register		
Offset Address :	0x100	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
SETENA[31:24]							
23	22	21	20	19	18	17	16
SETENA[23:16]							
15	14	13	12	11	10	9	8
SETENA[15:8]							

7	6	5	4	3	2	1	0
SETENA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	SETENA	Interrupt set-enable bits. Write: 0 : no effect 1 : enable interrupt. Read: 0 : interrupt disabled 1 : interrupt enabled.	0x00000000

1.43.6. CPU Interrupt Clear-enable Register

CPU_ICER	CPU Interrupt Clear-enable Register		
Offset Address :	0x180	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
CLRENA[31:24]							
23	22	21	20	19	18	17	16
CLRENA[23:16]							
15	14	13	12	11	10	9	8
CLRENA[15:8]							
7	6	5	4	3	2	1	0
CLRENA[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	CLRENA	Interrupt clear-enable bits. Write: 0 : no effect 1 : disable interrupt. Read: 0 : interrupt disabled 1 : interrupt enabled.	0x00000000

1.43.7. CPU Interrupt Set-pending Register

CPU_ISPR	CPU Interrupt Set-pending Register		
Offset Address :	0x200	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
SETPEND[31:24]							
23	22	21	20	19	18	17	16
SETPEND[23:16]							
15	14	13	12	11	10	9	8
SETPEND[15:8]							
7	6	5	4	3	2	1	0
SETPEND[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	SETPEND	Interrupt set-pending bits. Write: 0 : no effect 1 : changes interrupt state to pending. Read: 0 : interrupt is not pending 1 : interrupt is pending.	0x00000000

1.43.8. CPU Interrupt Clear-pending Register

CPU_ICPR	CPU Interrupt Clear-pending Register		
Offset Address :	0x280	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
CLRPEND[31:24]							
23	22	21	20	19	18	17	16
CLRPEND[23:16]							
15	14	13	12	11	10	9	8
CLRPEND[15:8]							
7	6	5	4	3	2	1	0
CLRPEND[7:0]							

Bit	Attr	Bit Name	Description	Reset
31..0	rw	CLRPEND	Interrupt clear-pending bits. Write: 0 : no effect 1 : removes pending state an interrupt. Read: 0 : interrupt is not pending 1 : interrupt is pending.	0x00000000

1.43.9. CPU Interrupt Priority Registers 0

CPU_IPR0	CPU Interrupt Priority Registers 0		
Offset Address :	0x400	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PRI_3[1:0]		Reserved					
23	22	21	20	19	18	17	16
PRI_2[1:0]		Reserved					
15	14	13	12	11	10	9	8
PRI_1[1:0]		Reserved					
7	6	5	4	3	2	1	0
PRI_0[1:0]		Reserved					

Bit	Attr	Bit Name	Description	Reset
31..30	rw	PRI_3	Refer to the register descriptions of CPU_PRI_0.	0x00
29..24	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
23..22	rw	PRI_2	Refer to the register descriptions of CPU_PRI_0.	0x00
21..16	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
15..14	rw	PRI_1	Refer to the register descriptions of CPU_PRI_0.	0x00
13..8	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
7..6	rw	PRI_0	Each priority field holds a priority value, 0-3. The lower the value, the greater the priority of the corresponding interrupt.	0x00
5..0	rw	Reserved	Reserved (read as zero and ignore writes)	0x00

1.43.10. CPU Interrupt Priority Registers 1

CPU_IPR1	CPU Interrupt Priority Registers 1		
Offset Address :	0x404	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PRI_7[1:0]		Reserved					
23	22	21	20	19	18	17	16
PRI_6[1:0]		Reserved					
15	14	13	12	11	10	9	8
PRI_5[1:0]		Reserved					
7	6	5	4	3	2	1	0
PRI_4[1:0]		Reserved					

Bit	Attr	Bit Name	Description	Reset
31..30	rw	PRI_7	Refer to the register descriptions of CPU_PRI_0.	0x00
29..24	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
23..22	rw	PRI_6	Refer to the register descriptions of CPU_PRI_0.	0x00
21..16	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
15..14	rw	PRI_5	Refer to the register descriptions of CPU_PRI_0.	0x00
13..8	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
7..6	rw	PRI_4	Refer to the register descriptions of CPU_PRI_0.	0x00
5..0	rw	Reserved	Reserved (read as zero and ignore writes)	0x00

1.43.11. CPU Interrupt Priority Registers 2

CPU_IPR2	CPU Interrupt Priority Registers 2		
Offset Address :	0x408	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PRI_11[1:0]		Reserved					
23	22	21	20	19	18	17	16
PRI_10[1:0]		Reserved					
15	14	13	12	11	10	9	8
PRI_9[1:0]		Reserved					
7	6	5	4	3	2	1	0
PRI_8[1:0]		Reserved					

Bit	Attr	Bit Name	Description	Reset
31..30	rw	PRI_11	Refer to the register descriptions of CPU_PRI_0.	0x00
29..24	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
23..22	rw	PRI_10	Refer to the register descriptions of CPU_PRI_0.	0x00
21..16	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
15..14	rw	PRI_9	Refer to the register descriptions of CPU_PRI_0.	0x00
13..8	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
7..6	rw	PRI_8	Refer to the register descriptions of CPU_PRI_0.	0x00
5..0	rw	Reserved	Reserved (read as zero and ignore writes)	0x00

1.43.12. CPU Interrupt Priority Registers 3

CPU_IPR3	CPU Interrupt Priority Registers 3		
Offset Address :	0x40C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PRI_15[1:0]		Reserved					
23	22	21	20	19	18	17	16
PRI_14[1:0]		Reserved					
15	14	13	12	11	10	9	8
PRI_13[1:0]		Reserved					
7	6	5	4	3	2	1	0
PRI_12[1:0]		Reserved					

Bit	Attr	Bit Name	Description	Reset
31..30	rw	PRI_15	Refer to the register descriptions of CPU_PRI_0.	0x00
29..24	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
23..22	rw	PRI_14	Refer to the register descriptions of CPU_PRI_0.	0x00
21..16	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
15..14	rw	PRI_13	Refer to the register descriptions of CPU_PRI_0.	0x00
13..8	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
7..6	rw	PRI_12	Refer to the register descriptions of CPU_PRI_0.	0x00
5..0	rw	Reserved	Reserved (read as zero and ignore writes)	0x00

1.43.13. CPU Interrupt Priority Registers 4

CPU_IPR4	CPU Interrupt Priority Registers 4		
Offset Address :	0x410	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PRI_19[1:0]		Reserved					
23	22	21	20	19	18	17	16
PRI_18[1:0]		Reserved					
15	14	13	12	11	10	9	8
PRI_17[1:0]		Reserved					
7	6	5	4	3	2	1	0
PRI_16[1:0]		Reserved					

Bit	Attr	Bit Name	Description	Reset
31..30	rw	PRI_19	Refer to the register descriptions of CPU_PRI_0.	0x00
29..24	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
23..22	rw	PRI_18	Refer to the register descriptions of CPU_PRI_0.	0x00
21..16	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
15..14	rw	PRI_17	Refer to the register descriptions of CPU_PRI_0.	0x00
13..8	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
7..6	rw	PRI_16	Refer to the register descriptions of CPU_PRI_0.	0x00
5..0	rw	Reserved	Reserved (read as zero and ignore writes)	0x00

1.43.14. CPU Interrupt Priority Registers 5

CPU_IPR5	CPU Interrupt Priority Registers 5		
Offset Address :	0x414	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PRI_23[1:0]		Reserved					
23	22	21	20	19	18	17	16
PRI_22[1:0]		Reserved					
15	14	13	12	11	10	9	8
PRI_21[1:0]		Reserved					
7	6	5	4	3	2	1	0
PRI_20[1:0]		Reserved					

Bit	Attr	Bit Name	Description	Reset
31..30	rw	PRI_23	Refer to the register descriptions of CPU_PRI_0.	0x00
29..24	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
23..22	rw	PRI_22	Refer to the register descriptions of CPU_PRI_0.	0x00
21..16	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
15..14	rw	PRI_21	Refer to the register descriptions of CPU_PRI_0.	0x00
13..8	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
7..6	rw	PRI_20	Refer to the register descriptions of CPU_PRI_0.	0x00
5..0	rw	Reserved	Reserved (read as zero and ignore writes)	0x00

1.43.15. CPU Interrupt Priority Registers 6

CPU_IPR6	CPU Interrupt Priority Registers 6		
Offset Address :	0x418	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PRI_27[1:0]		Reserved					
23	22	21	20	19	18	17	16
PRI_26[1:0]		Reserved					
15	14	13	12	11	10	9	8
PRI_25[1:0]		Reserved					

7	6	5	4	3	2	1	0
PRI_24[1:0]		Reserved					

Bit	Attr	Bit Name	Description	Reset
31..30	rw	PRI_27	Refer to the register descriptions of CPU_PRI_0.	0x00
29..24	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
23..22	rw	PRI_26	Refer to the register descriptions of CPU_PRI_0.	0x00
21..16	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
15..14	rw	PRI_25	Refer to the register descriptions of CPU_PRI_0.	0x00
13..8	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
7..6	rw	PRI_24	Refer to the register descriptions of CPU_PRI_0.	0x00
5..0	rw	Reserved	Reserved (read as zero and ignore writes)	0x00

1.43.16. CPU Interrupt Priority Registers 7

CPU_IPR7	CPU Interrupt Priority Registers 7		
Offset Address :	0x41C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PRI_31[1:0]		Reserved					
23	22	21	20	19	18	17	16
PRI_30[1:0]		Reserved					
15	14	13	12	11	10	9	8
PRI_29[1:0]		Reserved					
7	6	5	4	3	2	1	0
PRI_28[1:0]		Reserved					

Bit	Attr	Bit Name	Description	Reset
31..30	rw	PRI_31	Refer to the register descriptions of CPU_PRI_0.	0x00
29..24	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
23..22	rw	PRI_30	Refer to the register descriptions of CPU_PRI_0.	0x00
21..16	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
15..14	rw	PRI_29	Refer to the register descriptions of CPU_PRI_0.	0x00
13..8	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
7..6	rw	PRI_28	Refer to the register descriptions of CPU_PRI_0.	0x00
5..0	rw	Reserved	Reserved (read as zero and ignore writes)	0x00

1.43.17. CPU ID Register

CPU_CPUID	CPU ID Register		
Offset Address :	0xD00	Reset Value :	0x410CC200

31	30	29	28	27	26	25	24
IMPLEMENTER[7:0]							
23	22	21	20	19	18	17	16
VARIANT[3:0]				CONSTANT[3:0]			
15	14	13	12	11	10	9	8
PARTNO[11:4]							
7	6	5	4	3	2	1	0
PARTNO[3:0]				REVISION[3:0]			

Bit	Attr	Bit Name	Description	Reset
31..24	r	IMPLEMENTER	Implementer code: 0x41 corresponds to ARM	0x41
23..20	r	VARIANT	Variant number, the r value in the rnpn product revision identifier: 0x0 corresponds to revision 0 (r0p0)	0x00
19..16	r	CONSTANT	Constant that defines the architecture of the processor: 0xC corresponds to ARMv6-M architecture	0x0C

15..4	r	PARTNO	Part number of the processor: 0xC20 corresponds to Cortex-M0	0x0C20
3..0	r	REVISION	Revision number, the p value in the rnpn product revision identifier: 0x0 corresponds to patch 0	0x00

1.43.18. CPU Interrupt Control and State Register

CPU_ICSR	CPU Interrupt Control and State Register		
Offset Address :	0xD04	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
NMIPENDSET	Reserved		PENDSVSET	PENDSVCLR	PENDSTSET	PENDSTCLR	Reserved
23	22	21	20	19	18	17	16
Reserved	ISRPENDING	Reserved				VECTPENDING[5:4]	
15	14	13	12	11	10	9	8
VECTPENDING[3:0]				Reserved			
7	6	5	4	3	2	1	0
Reserved		VECTACTIVE[5:0]					

Bit	Attr	Bit Name	Description	Reset
31	rw	NMIPENDSET	NMI set-pending bit. Write: 0 : no effect 1 : changes NMI exception state to pending. Read: 0 : NMI exception is not pending 1 : NMI exception is pending. Because NMI is the highest-priority exception, normally the processor enters the NMI exception handler as soon as it detects a write of 1 to this bit. Entering the handler then clears this bit to 0. This means a read of this bit by the NMI exception handler returns 1 only if the NMI signal is reasserted while the processor is executing that handler.	0x00
30..29	rw	Reserved	Reserved	0x00
28	rw	PENDSVSET	PendSV set-pending bit. Write: 0 : no effect 1 : changes PendSV exception state to pending. Read: 0 : PendSV exception is not pending 1 : PendSV exception is pending. Writing 1 to this bit is the only way to set the PendSV exception state to pending.	0x00
27	w	PENDSVCLR	PendSV clear-pending bit. Write: 0 : no effect 1 : removes the pending state from the PendSV exception.	0x00
26	rw	PENDSTSET	SysTick exception set-pending bit. Write: 0 : no effect 1 : changes SysTick exception state to pending. Read: 0 : SysTick exception is not pending 1 : SysTick exception is pending. If your device does not implement the SysTick timer, this bit is Reserved.	0x00
25	w	PENDSTCLR	SysTick exception clear-pending bit. Write: 0 : no effect	0x00

			1 : removes the pending state from the SysTick exception. This bit is WO. On a register read its value is Unknown. If your device does not implement the SysTick timer, this bit is Reserved.	
24	rw	Reserved	Reserved	0x00
23	rw	Reserved	Reserved	0x00
22	r	ISRPENDING	Interrupt pending flag, excluding NMI and Faults: 0 : interrupt not pending 1 : interrupt pending.	0x00
21..18	rw	Reserved	Reserved	0x00
17..12	r	VECTPENDING	Indicates the exception number of the highest priority pending enabled exception: 0 : no pending exceptions Nonzero : the exception number of the highest priority pending enabled exception.	0x00
11..8	rw	Reserved	Reserved	0x00
7..6	rw	Reserved	Reserved	0x00
5..0	r	VECTACTIVE	Contains the active exception number: 0 : Thread mode Nonzero : The exception number of the currently active exception.	0x00

1.43.19. CPU Application Interrupt and Reset Control Register

CPU_AIRCR	CPU Application Interrupt and Reset Control Register		
Offset Address :	0xD0C	Reset Value :	0xFA050000

31	30	29	28	27	26	25	24
VECTKEY[15:8]							
23	22	21	20	19	18	17	16
VECTKEY[7:0]							
15	14	13	12	11	10	9	8
ENDIANESS	Reserved						
7	6	5	4	3	2	1	0
Reserved					SYSRESETREQ	VECTCLRACTIVE	Reserved

Bit	Attr	Bit Name	Description	Reset
31..16	rw	VECTKEY	Register key: Reads as Unknown On writes, write 0x05FA to VECTKEY, otherwise the write is ignored.	0xFA05
15	r	ENDIANESS	Data endianness implemented: 0 = Little-endian 1 = Big-endian.	0x00
14..8	rw	Reserved	Reserved	0x00
7..3	rw	Reserved	Reserved	0x00
2	w	SYSRESETREQ	System reset request: 0 : no effect 1 : requests a system level reset. This bit reads as 0.	0x00
1	w	VECTCLRACTIVE	Reserved for debug use. This bit reads as 0. When writing to the register you must write 0 to this bit, otherwise behavior is unpredictable.	0x00
0	rw	Reserved	Reserved	0x00

1.43.20. CPU System Control Register

CPU_SCR	CPU System Control Register		
Offset Address :	0xD10	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			SEVONPEND	Reserved	SLEEPDEEP	SLEEPONEXIT	Reserved

Bit	Attr	Bit Name	Description	Reset
31..5	rw	Reserved	Reserved	0x0000000
4	rw	SEVONPEND	Send Event on Pending bit: 0 : only enabled interrupts or events can wakeup the processor, disabled interrupts are excluded 1 : enabled events and all interrupts, including disabled interrupts, can wakeup the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects the next WFE. The processor also wakes up on execution of an SEV instruction or an external event.	0x00
3	rw	Reserved	Reserved	0x00
2	rw	SLEEPDEEP	Controls whether the processor uses sleep or deep sleep as its low power mode: 0 = sleep 1 = deep sleep If your device does not support two sleep modes, the effect of changing the value of this bit is implementation-defined.	0x00
1	rw	SLEEPONEXIT	Indicates sleep-on-exit when returning from Handler mode to Thread mode: 0 : do not sleep when returning to Thread mode. 1 : enter sleep, or deep sleep, on return from an ISR to Thread mode. Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application.	0x00
0	rw	Reserved	Reserved	0x00

1.43.21. CPU Configuration and Control Register

CPU_CCR	CPU Configuration and Control Register		
Offset Address :	0xD14	Reset Value :	0x00000208

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						STKALIGN	Reserved
7	6	5	4	3	2	1	0
Reserved				UNALIGN_TRP	Reserved		

Bit	Attr	Bit Name	Description	Reset
31..10	r	Reserved	Reserved	0x000000
9	r	STKALIGN	Always reads as one, indicates 8-byte stack alignment on exception entry. On exception entry, the processor uses bit[9] of the stacked PSR to indicate the stack alignment. On return from the exception it uses this stacked bit to restore the correct	0x01

			stack alignment.	
8	r	Reserved	Reserved	0x00
7..4	r	Reserved	Reserved	0x00
3	r	UNALIGN_TRP	Always reads as one, indicates that all unaligned accesses generate a HardFault.	0x01
2..0	r	Reserved	Reserved	0x00

1.43.22. CPU System Handler Priority Register 2

CPU_SHPR2	CPU System Handler Priority Register 2		
Offset Address :	0xD1C	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PRI_11[1:0]		Reserved					
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

Bit	Attr	Bit Name	Description	Reset
31..30	rw	PRI_11	Priority of system handler 11, SVCall. Refer to the register descriptions of CPU_PRI_0.	0x00
29..24	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
23..0	rw	Reserved	Reserved	0x000000

1.43.23. CPU System Handler Priority Register 3

CPU_SHPR3	CPU System Handler Priority Register 3		
Offset Address :	0xD20	Reset Value :	0x00000000

31	30	29	28	27	26	25	24
PRI_15[1:0]		Reserved					
23	22	21	20	19	18	17	16
PRI_14[1:0]		Reserved					
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

Bit	Attr	Bit Name	Description	Reset
31..30	rw	PRI_15	Priority of system handler 15, SysTick exception. Refer to the register descriptions of CPU_PRI_0.	0x00
29..24	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
23..22	rw	PRI_14	Priority of system handler 14, PendSV. Refer to the register descriptions of CPU_PRI_0.	0x00
21..16	rw	Reserved	Reserved (read as zero and ignore writes)	0x00
15..0	rw	Reserved	Reserved	0x0000

1.43.24. CPU Register Map

CPU Register Map Register Number = 23

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x10	CPU_SYST_CSR	Reserved															COUNTFLAG	Reserved													CLKSOURCE	TICKINT	ENCNT
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	CPU_SYST_RVR	Reserved								RELOAD[23:0]																							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	CPU_SYST_CVR	Reserved								CURRENT[23:0]																							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	CPU_SYST_CALIB	NOREF	SKEW	Reserved						TENMS[23:0]																							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x100	CPU_ISER	SETENA[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x180	CPU_ICER	CLRENA[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x200	CPU_ISPR	SETPEND[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x280	CPU_ICPR	CLRPEND[31:0]																															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x400	CPU_IPR0	PRI_3[1:0]		Reserved						PRI_2[1:0]		Reserved						PRI_1[1:0]		Reserved						PRI_0[1:0]		Reserved					
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x404	CPU_IPR1	PRI_7[1:0]		Reserved						PRI_6[1:0]		Reserved						PRI_5[1:0]		Reserved						PRI_4[1:0]		Reserved					
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x408	CPU_IPR2	PRI_11[1:0]		Reserved						PRI_10[1:0]		Reserved						PRI_9[1:0]		Reserved						PRI_8[1:0]		Reserved					
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40C	CPU_IPR3	PRI_15[1:0]		Reserved						PRI_14[1:0]		Reserved						PRI_13[1:0]		Reserved						PRI_12[1:0]		Reserved					
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x410	CPU_IPR4	PRI_19[1:0]		Reserved						PRI_18[1:0]		Reserved						PRI_17[1:0]		Reserved						PRI_16[1:0]		Reserved					
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x414	CPU_IPR5	PRI_23[1:0]		Reserved						PRI_22[1:0]		Reserved						PRI_21[1:0]		Reserved						PRI_20[1:0]		Reserved					
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x418	CPU_IPR6	PRI_27[1:0]		Reserved						PRI_26[1:0]		Reserved						PRI_25[1:0]		Reserved						PRI_24[1:0]		Reserved					
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x41C	CPU_IPR7	PRI_31[1:0]		Reserved						PRI_30[1:0]		Reserved						PRI_29[1:0]		Reserved						PRI_28[1:0]		Reserved					
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xD00	CPU_CPUID	IMPLEMENTER [7:0]								VARIANT[3:0]				CONSTANT[3:0]				PARTNO[11:0]												REVISION[3:0]			
Reset	**0x410CC200**	0	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0

0xD04	CPU_ICSR	NMIPENDSET	Reserved		PENDSVSET	PENDSVCLR	PENDSTSET	PENDSTCLR	Reserved	Reserved	ISRPENDING	Reserved				VECTPENDING [5:0]						Reserved				Reserved		VECTACTIVE[5:0]					
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xD0C	CPU_AIRCR	VECTKEY[15:0]																ENDIANESS	Reserved							Reserved					SYSRESETREQ	VECTCLRACTIVE	Reserved
Reset	**0xFA050000**	1	1	1	1	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xD10	CPU_SCR	Reserved																											SEVONPEND	Reserved	SLEEPDEEP	SLEEPONEXIT	Reserved
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xD14	CPU_CCR	Reserved																						STKALIGN	Reserved	Reserved				UNALIGN_TRP	Reserved		
Reset	**0x00000208**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0
0xD1C	CPU_SHPR2	PRI_11[1:0]		Reserved						Reserved																							
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xD20	CPU_SHPR3	PRI_15[1:0]		Reserved						PRI_14[1:0]		Reserved						Reserved															
Reset	0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

2. Revision History

Version 1.25 Register Definitions (2023_1127)	
1	Change default value loaded from CFG OR after Cold reset only for ADC0_OFFT_ADC.
Version 1.24 Register Definitions (2023_1025)	
1	Add descriptions about DMA channel-0 using only for DMA_FGBUS_SEL=1.
2	Remove the descriptions of ADC0_DTEST_EN in ADC0_OFFT_PGA, ADC0_GAIN_PGA.
Version 1.23 Register Definitions (2023_0627)	
1	Rename value definition NCO0_P0 to NCO_P0 in URTx_CK_SEL.
Version 1.22 Register Definitions (2022_1109)	
1	Change the [Attr] from "w" to "rw" for bits of URTx_RDAT_INV and URTx_TDAT_INV.
2	Update register descriptions of USB_TXDnF, USB_RXDnF, USB_TXSEQn, USB_RXSEQn, USB_RXSTLn, USB_RXENn, USB_RXCNTn, USB_RXADRn for End-point register set 1~7.
Version 1.21 Register Definitions (2022_0318)	
1	Change APX_SDT_PSEL value definitions.
Version 1.20 Register Definitions (2022_0314)	
1	Add CFG_OR16, CFG_OR17 and USB_ERRF/ESOF/OVRF/SETUPF/NORSF/BSTF/CRCF registers.
2	Remove URT0_SDT_EN, URT1_SDT_EN, URT2_SDT_EN, SPI0_SDT_EN.
3	Remove APX_SDTF0~3, APX_SDTF0~3, APX_SDT_IE0~3, APX_SDT_E1SEL, APX_SDT_E0NS, APX_SDT_E0AS.
4	Change APX_SDT_PSEL value definitions.
Version 1.13 Register Definitions (2021_1223)	
1	Change PC_SC4/5/6 default value=1.
2	Add new register MEM_HSP_EN.
Version 1.12 Register Definitions (2021_0806)	
1	Update the register value definitions of PW_WKSTP_DSEL.
Version 1.11 Register Definitions (2021_0608)	
1	Update the register descriptions of CFG_IAP_SIZE and CFG_ISP_SIZE.
Version 1.10 Register Definitions (2021_0514)	
1	Released version for register definitions
Version 1.00 Register Definitions (2020_0831)	

1	Initial version for register definitions

3. List of abbreviations for registers

Abbreviations	Definition	Descriptions
Attr	access Attribute	Register read/write access attribute
rw	Read/Writer	Indicate the register can be read or write by software.
r	Read	Indicate the register can be read only by software.
w	Write	Indicate the register can be written only by software.
Reserved	Reserved register	Indicate the register is reserved for internal using or future design.
Reset	Reset value	The register default value after chip warm/cold reset by design default or loaded from OB(option byte flash)
Base Address	absolute address	The Base Address is using as the absolute address of CPU addressing for all the registers of a module. The actual address of a register is the Base Address plus the Offset Address.
Offset Address	related address	The Offset Address is using as the related address for one of the registers of a module. The actual address of a register is the Base Address plus the Offset Address.