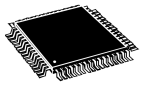
MG32F157xx

32-bit ARM® Cortex™-M3 MCU

Up to 256 KBytes Flash / 64 KBytes SRAM, 11 TIMs, 3 x 12-bit ADC, 2 x 12-bit DAC, 15 communication interfaces



LQFP100 (14 x 14 mm)
LQFP64 (10 x 10 mm)
LQFP48 (7 x 7 mm)

Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 96 MHz maximum frequency
  - Single-cycle multiplication and hardware division
- Memories
  - 256 K-byte Flash memory, 0 wait state from 0 to 48 MHz and 1 wait states above.
  - 64 K-byte SRAM, performance at 0 wait state memory access.
- Reset and supply management
  - VDD:2V
  - Power On Reset(POR),Power Down Reset(PDR), Programmable Voltage Detector (PVD)
- Clock
  - External 4 ~ 24 MHz high speed clock (HSE)
  - Internal 8 MHz high speed clock (HSI)
  - External 32 KHz Low speed clock (LSE)
  - Internal 40 KHz Low speed clock (LSI)
- Operation temperature
  - -40°C~+105°C
- Low power
  - Sleep, Stop and Standby modes
  - VBAT power supply mode (RTC and backup register)
- Up to 80 fast I/O ports
  - All mappable on 16 external interrupt vectors , and most are compatible with 5V
- Debug mode
  - SWD/Trace interface
- 3 x 12-bit, A/D converters , up to 18 channels(Contains built-in temperature sensor and internal reference voltage two channels)
- 2 x 12-bit D/A converters
- Up to 15 communication interfaces
  - Up to 2 I2C interface
  - Up to 5 USARTs (ISO 7816 interface, LIN, IrDA capability, maximum rate is 4.5Mbit/s , MODEM control, low power monitoring function and can wake MCU)
  - 3 SPI interfaces, 1 QSPI interface
  - 1 CAN, 1 USB, 1 SDIO
- Up to 11 timers
  - 4 general timers (32 bit)
  - 2 advanced timer (32-bit)
  - 2 IWDG
  - 1 SysTick timer:
  - 2 basic timers(32-bit)
- CRC calculation unit
- 128-bit unique ID
- Advanced Encryption Standard (AES)
- ESD (±5KV) HBM, Latch-Up (±800mA)
- TRNG generate true Random number
- Built-in ISP Bootloader , supports program upgrade through USART
- 3 high speed rail to rail operational amplifiers

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1 Overview

The MG32F157xx family incorporates the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a 96 MHz frequency, high-speed embedded memories (Flash memory up to 256 Kbytes and SRAM up to 64 Kbytes),

1.1 Product perpherals and characters list

Tab1.1-1 shows an overview of the complete range of peripherals, packages and characters proposed in this family.

Tab 1.1-1 MG32F157xx perpherals and characters

Perpherals		**MG32F157Cxyz**		**MG32F157Rxyz**		**MG32F157Vxyz**	
Flash memory in Kbytes		128	256	128	256	128	256
SRAM in Kbytes		64					
Timer	General	4					
	Advanced	2					
	IWDG	2					
	sys clk	1					
	Basic	2					
Comm	I2C	2					
	QSPI	1					
	SPI(I2S)	3(2)					
	USART	5					
	SDIO	1					
	CAN	1					
	USB	1					
Number of GPIOs		37		51		80	
OPA		1		3		3	
12-bit A/D conversion		3					
channel		16					
12-bit D/A conversion		2					
channel		2					
CPU frequency		96 MHZ					
Operating voltage		2.0v ~ 3.6v					
Operating temperatures		-40°C ~ +105°C					
Packages		LQFP48		LQFP64		LQFP100	

xyz are codes that represent information about different chips. See Fig6.0-1 for details.

x = Flash memory

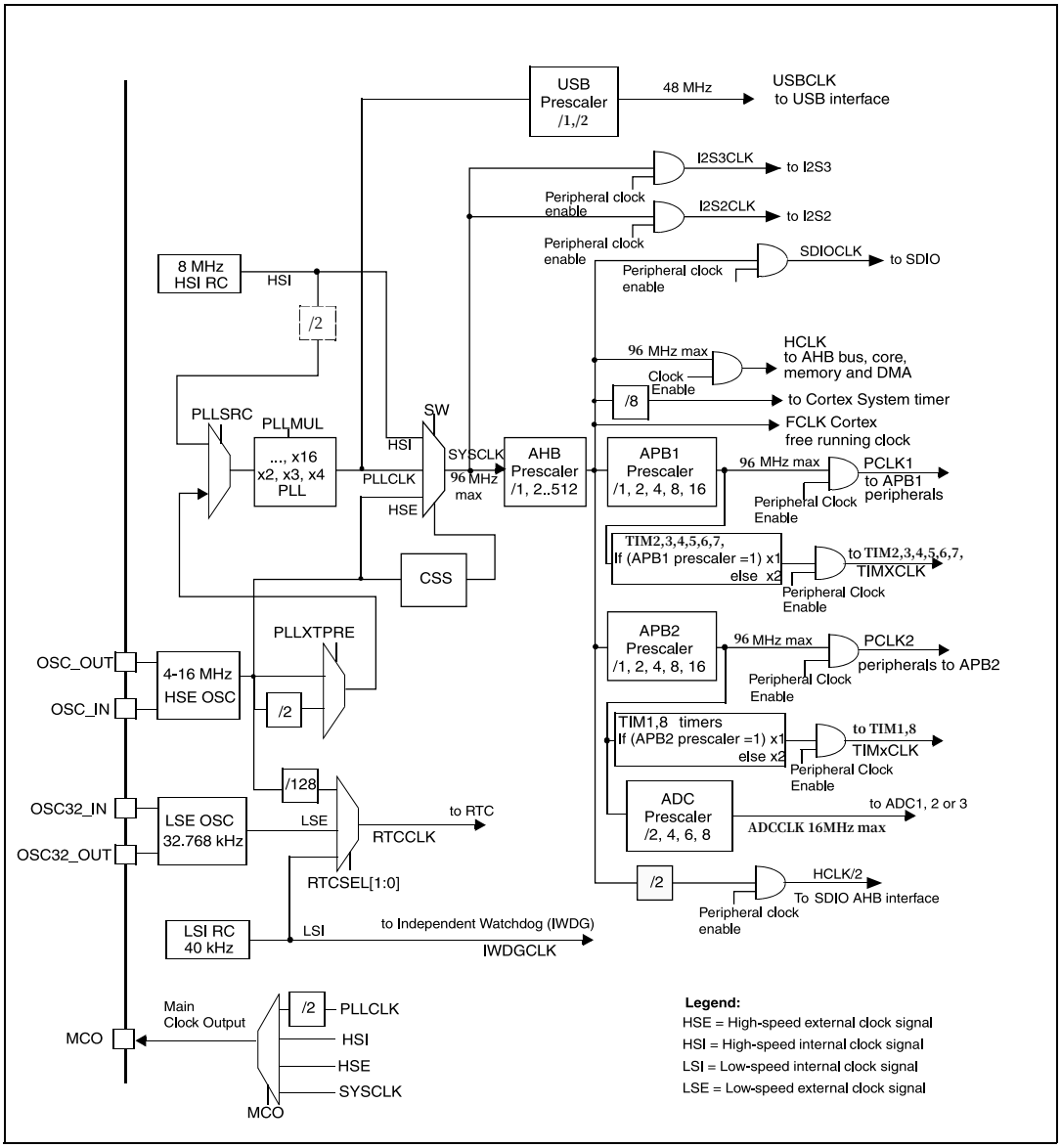
y = package

z = Operating temperatures

1.2 clock tree

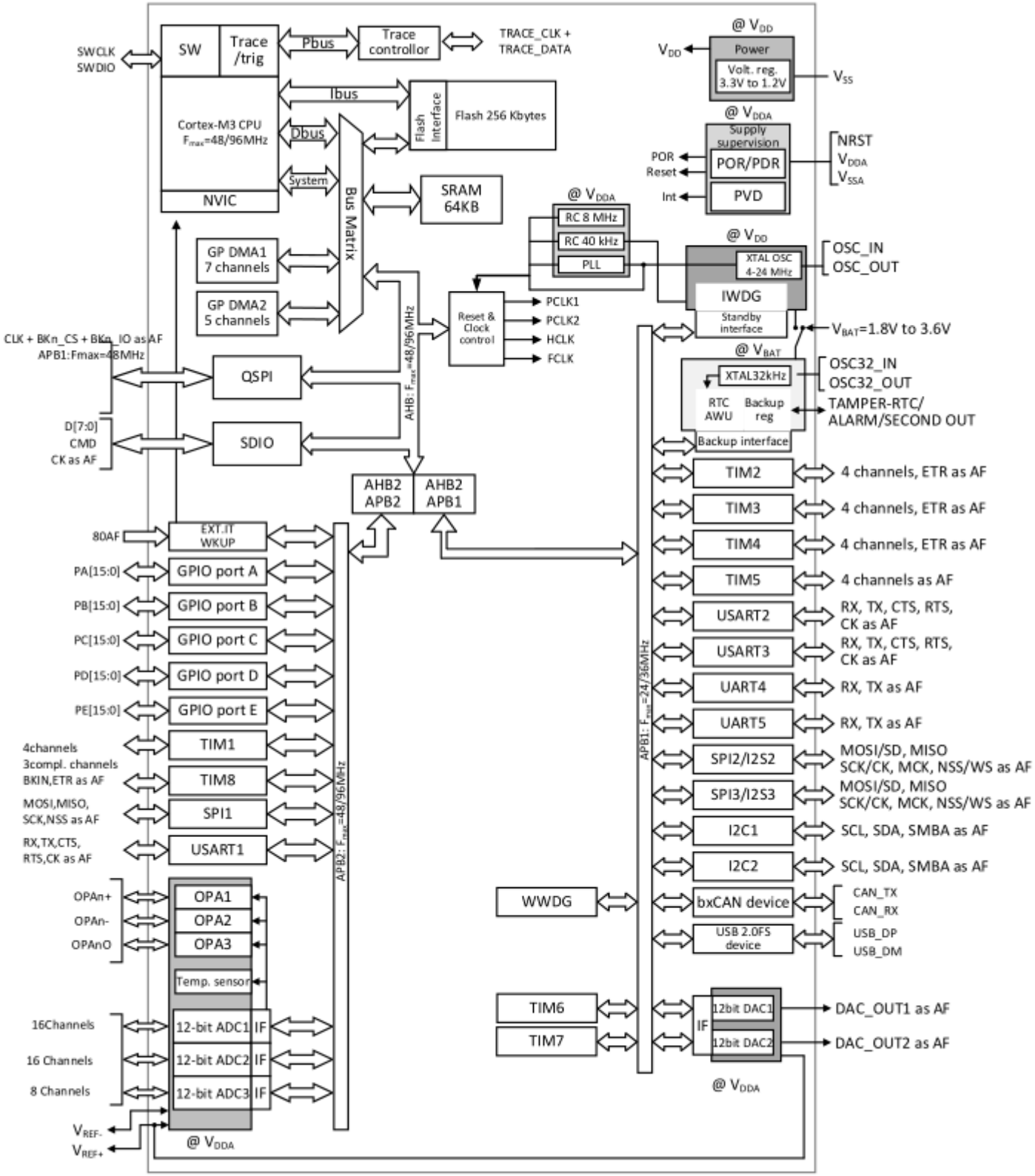
Fig1.2-1 plots the clock relationship for MG32F157xx .

Fig 1.2-1 MG32F157xx clock



1.3 performance line block diagram

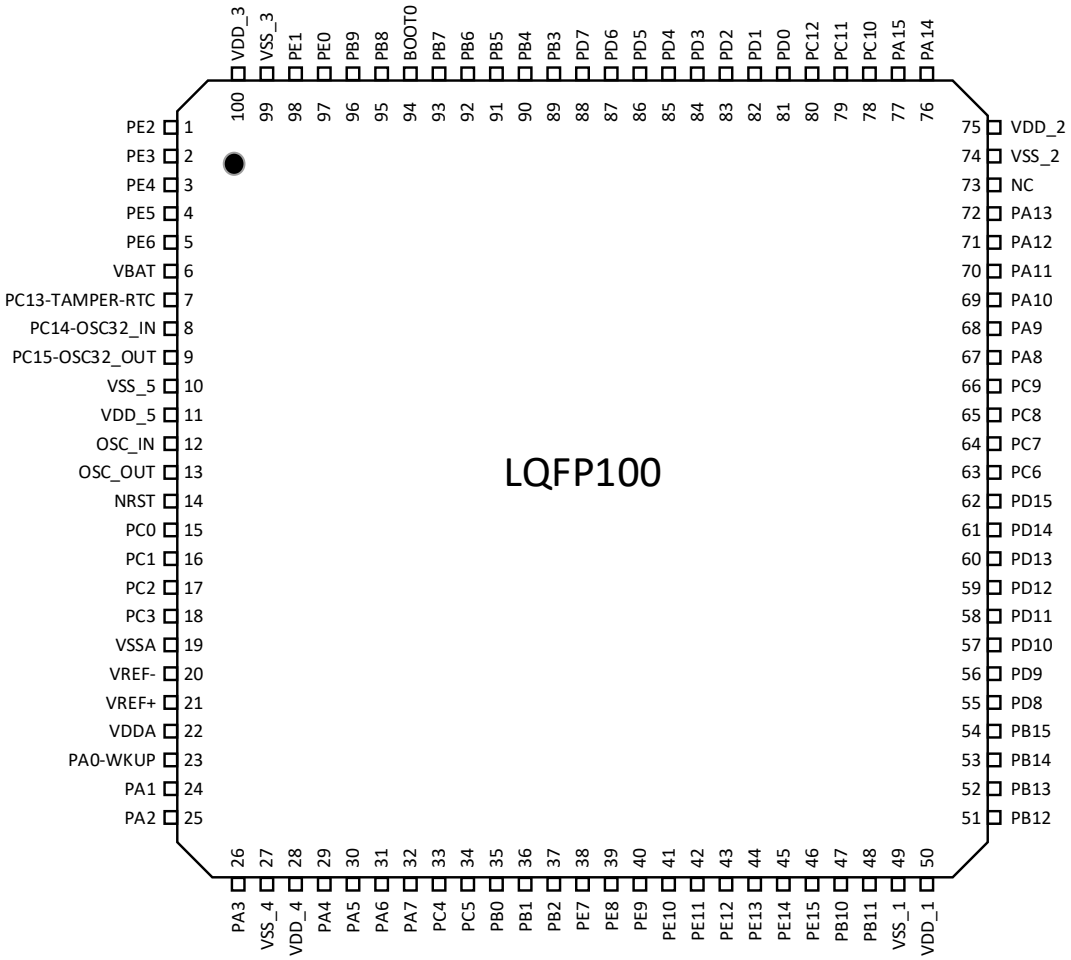
Fig 1.3-1 MG32F157xx performance line block diagram



2 Pinouts and pin descriptions

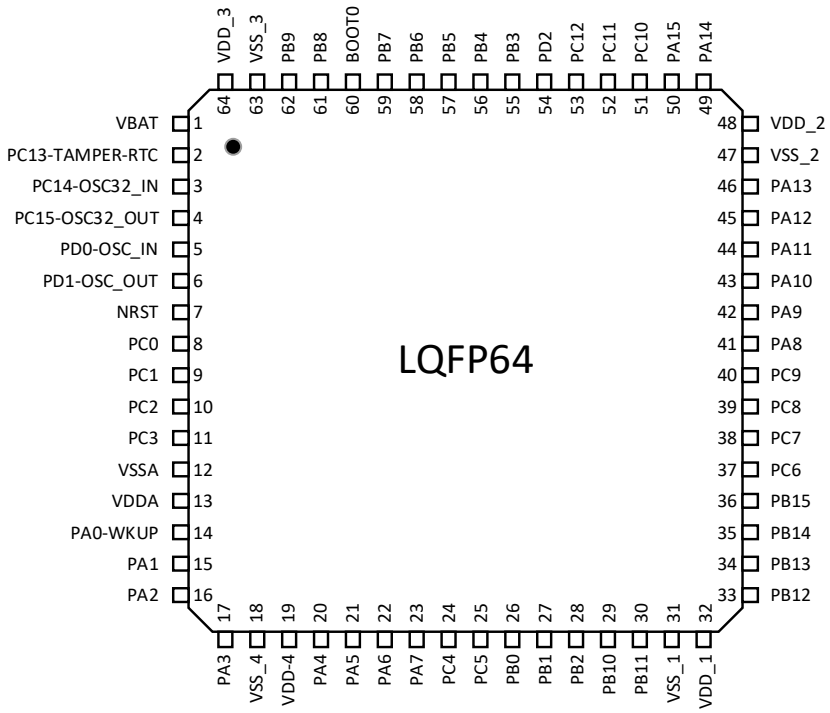
2.1 LQFP100 pinouts

Fig 2.1-1 LQFP100 pinouts



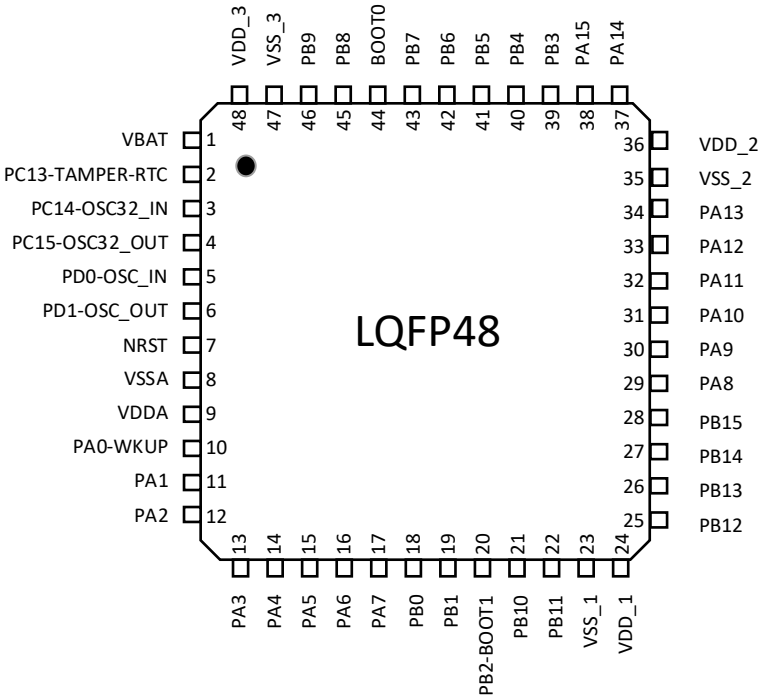
2.2 LQFP64 pinouts

Fig 2.2-1 LQFP64 pinouts



2.3 LQFP48 pinouts

Fig 2.3-1 LQFP48 pinouts



2.4 pin descriptions

Tab 2.4-1 MG32F157xx pin descriptions

Pin No.			Pin Name	Type	I/OLevel[2]	Main Function	AlternateFunction[4]	
LQFP48	LQFP64	LQFP100					Default	Remap
-	-	1	PE2	I/O	FT	PE2	QSPI_BK1_nCS/TRACECK	
-	-	2	PE3	I/O	FT	PE3	QSPI_BK1_IO0/TRACED0	
-	-	3	PE4	I/O	FT	PE4	QSPI_BK1_IO1/TRACED1	
-	-	4	PE5	I/O	FT	PE5	QSPI_BK1_IO2/TRACED2	
-	-	5	PE6	I/O	FT	PE6	QSPI_BK1_IO3/TRACED3	
1	1	6	V_{BAT}	S		VBAT		
2	2	7	TAMPERRTC	I/O		PC13[5]	TAMPERRTC	
3	3	8	PC14 OSC32_IN	I/O		PC14[5]	OSC32_IN	
4	4	9	PC15 OSC32_OUT	I/O		PC15[5]	OSC32_OUT	
-	-	10	V_{SS_5}	S		V_{SS_5}		
-	-	11	V_{DD_5}	S		V_{DD_5}		
5	5	12	OSC_IN	I		OSC_IN		PD0
6	6	13	OSC_OUT	O		OSC_OUT		PD1
7	7	14	NRST	I/O		NRST		
-	8	15	PC0	I/O		PC0	ADC123_IN10	OP3+
-	9	16	PC1	I/O		PC1	ADC123_IN11	OP3-
-	10	17	PC2	I/O		PC2	ADC123_IN12	OP2+
-	11	18	PC3[6]	I/O		PC3	ADC123_IN13	OP2-
8	12	19	V_{SSA}	S		V_{SSA}		
-	-	20	V_{REF}	S		V_{REF}		
-	-	21	V_{REF+}	S		V_{REF+}		
9	13	22	V_{DDA}	S		V_{DDA}		
10	14	23	PA0 WKUP	I/O		PA0	WKUP/USART2_CTS/ADC123_IN0/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR	OP1+
11	15	24	PA1	I/O		PA1	USART2_RTS/ ADC123_IN1/ TIM5_CH2/TIM2_CH2	OP1-
12	16	25	PA2	I/O		PA2	USART2_TX/ TIM5_CH3/ ADC123_IN2/ TIM2_CH3	
13	17	26	PA3	I/O		PA3	USART2_RX/ TIM5_CH4/ ADC123_IN3/ TIM2_CH4	
-	18	27	V_{SS_4}	S		V_{SS_4}		
-	19	28	V_{DD_4}	S		V_{DD_4}		
14	20	29	PA4	I/O		PA4	SPI1_NSS/ USART2_CK/ DAC_OUT1/ ADC12_IN4	OP1O
15	21	30	PA5	I/O		PA5	SPI1_SCK /DAC_OUT2/ ADC12_IN5	
16	22	31	PA6	I/O		PA6	SPI1_MISO/ TIM8_BKIN/ ADC12_IN6/ TIM3_CH1	TIM1_BKIN
17	23	32	PA7	I/O		PA7	SPI1_MOSI/ TIM8_CH1N/ ADC12_IN7/ TIM3_CH2	TIM1_CH1N
-	24	33	PC4	I/O		PC4	ADC12_IN14	OP3O
-	25	34	PC5	I/O		PC5	ADC12_IN15	OP2O
18	26	35	PB0	I/O		PB0	ADC12_IN8/ TIM3_CH3/ TIM8_CH2N	TIM1_CH2N
19	27	36	PB1	I/O		PB1	ADC12_IN9/ TIM3_CH4/ TIM8_CH3N	TIM1_CH3N
20	28	37	PB2	I/O	FT	PB2/BOOT1		
-	-	38	PE7	I/O	FT	PE7		TIM1_ETR
-	-	39	PE8	I/O	FT	PE8		TIM1_CH1N
-	-	40	PE9	I/O	FT	PE9		TIM1_CH1
-	-	41	PE10	I/O	FT	PE10		TIM1_CH2N
-	-	42	PE11	I/O	FT	PE11		TIM1_CH2
-	-	43	PE12	I/O	FT	PE12		TIM1_CH3N
-	-	44	PE13	I/O	FT	PE13		TIM1_CH3
-	-	45	PE14	I/O	FT	PE14		TIM1_CH4
-	-	46	PE15	I/O	FT	PE15		TIM1_BKIN

(continued)

Pin No.			Pin Name	Type	I/OLevel[2]	Main Function	AlternateFunction[4]	
LQFP48	LQFP64	LQFP100					Default	Remap
21	29	47	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX	TIM2_CH3
22	30	48	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX	TIM2_CH4
23	31	49	V_{SS_1}	S		V_{SS_1}		
24	32	50	V_{DD_1}	S		V_{DD_1}		
25	33	51	PB12	I/O	FT	PB12	SPI2_NSS/ I2S2_WS/ I2C2_SMBAI/ USART3_CK/ TIM1_BKIN	
26	34	52	PB13	I/O	FT	PB13	SPI2_SCK/ I2S2_CK /USART3_CTS/ TIM1_CH1N	
27	35	53	PB14	I/O	FT	PB14	SPI2_MISO/ TIM1_CH2N/ USART3_RTS	
28	36	54	PB15	I/O	FT	PB15	SPI2_MOSI/ I2S2_SD/ TIM1_CH3N	
-	-	55	PD8	I/O	FT	PD8		USART3_TX
-	-	56	PD9	I/O	FT	PD9		USART3_RX
-	-	57	PD10	I/O	FT	PD10		USART3_CK
-	-	58	PD11	I/O	FT	PD11		USART3_CTS
-	-	59	PD12	I/O	FT	PD12		USART3_RTS/ TIM4_CH1
-	-	60	PD13	I/O	FT	PD13		TIM4_CH2
-	-	61	PD14	I/O	FT	PD14		TIM4_CH3
-	-	62	PD15	I/O	FT	PD15		TIM4_CH4
-	37	63	PC6	I/O	FT	PC6	I2S2_MCK/ TIM8_CH1/ SDIO_D6/ QSPI_BK2_IO2	TIM3_CH1
-	38	64	PC7	I/O	FT	PC7	I2S3_MCK/ TIM8_CH2/ SDIO_D7/ QSPI_BK2_IO3	TIM3_CH2
-	39	65	PC8	I/O	FT	PC8	TIM8_CH3/ SDIO_D0/ QSPI_BK1_IO0	TIM3_CH3
-	40	66	PC9	I/O	FT	PC9	TIM8_CH4/ SDIO_D1/ QSPI_BK1_IO1	TIM3_CH4
29	41	67	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1/ MCO	
30	42	68	PA9	I/O	FT	PA9	USART1_TX/ TIM1_CH2	
31	43	69	PA10	I/O	FT	PA10	USART1_RX/ TIM1_CH3	
32	44	70	PA11	I/O	FT	PA11	USART1_CTS/ USBDM/ CAN_RX/ TIM1_CH4	
33	45	71	PA12	I/O	FT	PA12	USART1_RTS/ USBDP/ CAN_TX/ TIM1_ETR	
34	46	72	PA13	I/O	FT	SWDIO		PA13
-	-	73	-	-	-	-	-	-
35	47	74	V_{SS_2}	S	FT	V_{SS_2}		
36	48	75	V_{DD_2}	S	FT	V_{DD_2}		
37	49	76	PA14	I/O	FT	SWCLK		PA14
38	50	77	PA15	I/O	FT	PA15	SPI3_NSS/I2S3_WS/QSPI_BK2_nCS	TIM2_CH1_ETR/ SPI1_NSS
-	51	78	PC10	I/O	FT	PC10	UART4_TX/SDIO_D2/QSPI_BK1_IO2	USART3_TX
-	52	79	PC11	I/O	FT	PC11	UART4_RX/SDIO_D3/QSPI_BK1_IO3	USART3_RX
-	53	80	PC12	I/O	FT	PC12	UART5_TX/SDIO_CK/QSPI_CLK	USART3_CK
-	5	81	PD0	I/O	FT	OSC_IN		CAN_RX
-	6	82	PD1	I/O	FT	OSC_OUT		CAN_TX
-	54	83	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX/SDIO_CMD/QSPI_BK1_nCS	
-	-	84	PD3	I/O	FT	PD3		USART2_CTS
-	-	85	PD4	I/O	FT	PD4		USART2_RTS
-	-	86	PD5	I/O	FT	PD5		USART2_TX
-	-	87	PD6	I/O	FT	PD6		USART2_RX
-	-	88	PD7	I/O	FT	PD7		USART2_CK
39	55	89	PB3	I/O	FT	PB3	SPI3_SCK/I2S3_CK	TRACESWO/ TIM2_CH2/ SPI1_SCK
40	56	90	PB4	I/O	FT	PB4	SPI3_MISO	TIM3_CH1/ SPI1_MISO
41	57	91	PB5	I/O	-	PB5	I2C1_SMBAI/SPI3_MOSI/I2S3_SD	TIM3_CH2/ SPI1_MOSI

(continued)

Pin No.			Pin Name	Type	I/OLevel[2]	Main Function	AlternateFunction[4]	
LQFP48	LQFP64	LQFP100					Default	Remap
42	58	92	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
43	59	93	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2	USART1_RX
44	60	94	BOOT0	I	-	BOOT0		
45	61	95	PB8	I/O	FT	PB8	TIM4_CH3/SDIO_D4/QSPI_BK2_IO0	I2C1_SCL/ CAN_RX
46	62	96	PB9	I/O	FT	PB9	TIM4_CH4/SDIO_D5/QSPI_BK2_IO1	I2C1_SDA/ CAN_TX
-	-	97	PE0	I/O	FT	PE0	TIM4_ETR	
-	-	98	PE1	I/O	FT	PE1	QSPI_CLK	
47	63	99	V_{SS_3}	S	-	V_{SS_3}		
48	64	100	V_{DD_3}	S	-	V_{DD_3}		

[1] Symbols: S-supply, I-input, I/O-input/outp

[2]FT = 5 V tolerant.

[3]Function availability depends on the chosen device.

[4]If multiple peripherals share the same I/O pin, you can only enable one peripheral at a time through the peripheral clock enable bit to avoid conflicts between these alternate functions (In the corresponding RCC peripheral clock enable register)

[5]After this reset function is enabled, it is not reset by the master reset signal

[6]The sub-reset function can be remapped by the software to other pin ports (if present in the selected model)

[7]For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins.For the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping.

3 Device description

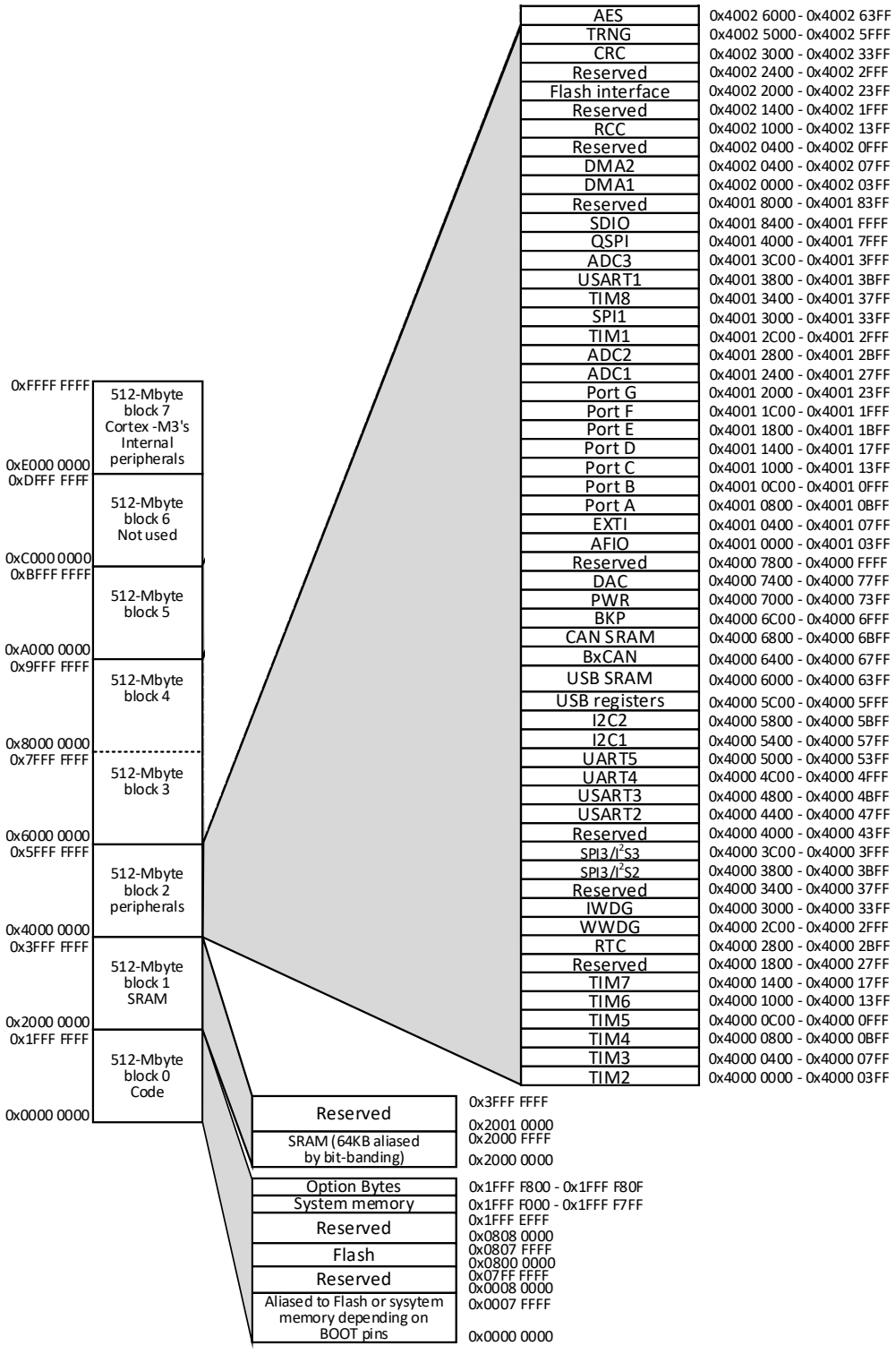
3.1 ARM® Cortex™-M3 core

The 32-bit Arm® Cortex®-M3 core processor is designed for high-performance, real-time processing in cost-constrained applications and can handle complex tasks. Any Arm® Cortex®-M3 microcontroller offers high scalability combined with an optimal trade-off between performance and cost.

3.2 Memory mapping

The memory map is shown in Fig3.2-1.

Fig 3.2-1 MG32F157xx Memory map



The Cortex®-M3 memory map includes two bit-band regions:SRAM area and peripherals area.These regions

map each word in an alias region of memory to a bit in a bit-band region of memory. For specific operation methods, please refer to "Cortex™-M3 Core Manual".

Note: *The unlisted areas are reserved areas or system internal configuration areas and cannot be accessed by users.*

3.3 Embedded Flash memory

Up to 256 Kbytes of embedded Flash is available for storing programs and data. 0 wait state from 0 to 48 MHz and 1 wait states above.

3.4 Embedded SRAM

Up to 64 Kbytes of embedded SRAM at CPU clock with 0 wait states.

3.5 CRC(cyclic redundancy check) calculation unit

CRC-32 polynomials supported by ISO/IEC13239:

$$X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X + 1 \quad (3.1)$$

3.6 Clocks and startup

The system clock has three clock sources: HSI (internal 8MHz), HSE (external 4-24MHz), and PLL (internal 4-96MHz). The system chooses HSI as the default clock during startup and reset, after which the software can optionally configure the system clock to switch between HSI/HSE/PLL.

When HSE is used as the system clock, if an HSE failure is detected, the system automatically switches back to HSI and generates a software interrupt.

Multiple pre-dividers can flexibly configure the clock frequency of AHB/APB1/APB2. The maximum clock frequency of AHB,APB1 and APB2 is 96MHz.

3.7 Boot modes

Can use the boot0/boot1 pins to select the boot mode:

- Boot from the flash memory user area
- Start from the flash system area. After starting, you can program the flash user area through USRAT1
- Boot from SRAM

3.8 Nested vectored interrupt controller (NVIC)

The built-in NVIC can handle up to 64 masked interrupt lines (excluding 16 M3 interrupts) and 16 programmable priorities.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector address passed directly to the core
- Quick response to interrupts
- Handle interrupts of higher priority
- Support for Tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware module provides flexible interrupt management features with minimal interrupt latency.

3.9 External interrupt/event controller (EXTI)

EXTI includes 24 edge detection lines used to generate interrupt/event requests. Each line can be individually configured to trigger events (up edge, falling edge, or both) and can be masked independently. A suspended register maintains the status of all interrupt requests. EXTI can detect pulses less than the internal APB2 clock period, and all GPIOs can be connected to 16 external interrupt lines

3.10 Power supply schemes

- VDD = 2.0V ~ 3.6V: External power supplies all IO and internal voltage regulators through VDD pins.
- VSSA, VDDA = 2.4V ~ 3.6V: external analog power supplies for ADC, DAC, Reset unit, oscillator and PLL (minimum voltage to be applied is 2.4 V when the ADC or DAC is used). VDDA and VSSA must be connected to VDD and VSS , respectively.
- VBTA = 2.0V ~ 3.6V: power supply for RTC, external clock 32.768 kHz oscillator and backup registers when VDD is not present.

3.11 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2.0 V. The device remains in reset mode when VDD is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the VDD power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when VDD drops below the V_{PVD} threshold and/or when VDD is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.12 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run).The regulator provides power to the 1.2V domain (kernel, storage, and digital periphery).
- LPR is used in the Stop modes.The regulator provides a low power supply to the 1.2V domain and retains data from the registers and SRAM
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down(contents of the registers and SRAM are lost).

3.13 Low-power modes

MG32F157xx supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

3.13.1 Sleep mode

In sleep mode, the kernel clock is turned off and all peripherals are still working

3.13.2 Stop mode

The stop mode achieves the lowest power consumption while preserving register and SRAM data. The 1.2V domain clock is turned off, the PLL, the internal high speed oscillator and the external high speed oscillator are turned off. The voltage regulator can be in master mode or low power mode. The product can be awakened through any EXTI wire. EXTI signal sources can be any of 16 external interrupts, PVD output, RTC alarm alarm .

3.13.3 Standby mode

The standby mode provides the lowest power consumption. The internal voltage regulator is turned off, as is the entire 1.2V domain. The phase locked loop, the internal high speed oscillator and the external high speed oscillator are disconnected. After entering standby mode, data of SRAM and registers are lost, and only registers and standby circuits in the backup area remain powered.

Note: *The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

3.14 Direct memory access controller(DMA)

Flexible 12-way universal DMA (7-way for DMA1 and 5-way for DMA2) can manage data transfers from memory to memory, peripherals to memory and memory to peripheral, peripherals to peripheral. The two DMA controllers support the management of the ring buffer, avoiding interrupts when the controller reaches the end of the buffer.

DMA can be used with major peripherals: SPI, I2C, USART, Universal/Basic/Advanced Timer TIMx, DAC, I2S,SDIO, ADC, QSPI, AES.

3.15 Real-time clock (RTC) and backup registers(BKP)

The RTC and back-up registers are powered by a switch that selects VDD power when VDD is active, otherwise it is powered by the VBAT pin. The backup registers are 42 registers(16-bit) used to store 84 bytes of user data when VDD is turned off. This register will not be reset by system or power reset, nor will it be reset by wake up after standby mode.

The real-time clock provides a set of continuously counting counters that can be configured by software to provide clock calendar functions, as well as alarm interrupts and periodic interrupts. Its clock can be provided by an external 32.768kHz oscillator, an internal low speed oscillator, or an external high speed oscillator at 128 FRF. The typical frequency for an internal low speed oscillator is 40kHz. The RTC can be calibrated with an external 512Hz output to compensate for natural frequency deviations. The RTC has a 32-bit programmable counter that can be warned using the comparison register to make long-term measurements. A 20-bit pre-divider is used for a time base clock, configured to generate a 1 second time base from a 32.768 kHz clock by default

3.16 Timers and Watchdog

2 advanced timers, 4 general timers, 2 basic timers, 2 Watchdog timers and 1 System timer

Tab3.16-1 compares the features of the timers.

Tab 3.16-1 High-density timer feature comparison

Timer	Resolution	Type	Prescaler	Capture / compare channels	DMA request generation	Complementary outputs
TIM1/ TIM8	32-bit	Up, down, up/down	Any integer between 1 and 65535	Yes	4	Yes
TIM2/ TIM3/ TIM4/ TIM5	32-bit	Up, down, up/down	Any integer between 1 and 65535	Yes	4	No
TIM6/ TIM7	32-bit	Up	Any integer between 1 and 65535	Yes	0	No

Advanced-control timers (TIM1 and TIM8)

The two advanced-control timers (TIM1 and TIM8) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5). These timers are based on a 32-bit auto-reload up/down counter, a 16 bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Basic timers TIM6 and TIM7

Basic timer is mainly used for triggering generation of digital - to - analog conversion.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The watchdog is disabled in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the watchdog is disabled in debug mode

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.17 I^2C bus

Up to two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave).
They can be served by DMA and they support SMBus 2.0/PMBus.

3.18 Universal synchronous/asynchronous receiver transmitters (USARTs)

three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

3.19 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 24 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8/16 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

3.20 Four-way serial peripheral interface (QSPI)

QSPI interface supports single, dual, and four-way SPI, two groups of interfaces, and supports two external flash memory access at the same time. The operation is 8/16/32 bits:

- Register indirect access
- External flash polling mode
- store mapping mode

3.21 Inter-integrated sound (I2S)

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192kHz are supported. When either or both of the I2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

3.22 SDIO

SDIO interface can communicate with SD , MMC , SDIO and CE-ATA device;
Support SD 2.0 standard, 1/4 bit mode;
Support SDIO 2.0 standard;
Support CE-ATA 1.1 standard;
Support MMC 4.2 standard,1/4/8 bit mode

3.23 Controller area network (CAN)

Support Bosch CAN2.0A/CAN 2.0b, support ISO-11898-1 CAN FD mode

3.24 Universal serial bus (USB)

Embedded one USB controller and physical layer transceiver.

- Comply with USB2.0 full speed device specification
- Can configure 1 to 6 endpoints
- All endpoints dynamically allocate FIFOs
- The FIFO contains a maximum of 1024 bytes
- Supports batch/synchronous transfer with double buffering
- Support control/interrupt transmission
- USB suspend and restore operations are supported
- 4 built-in DMA channels
- Soft connection/disconnection is supported

3.25 General-purpose inputs/outputs(GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high currentcapable. The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.26 Analog to digital converter(ADC)

Three 12-bit analog to digital converters, each with up to 16 external channels and 2 internal sources, complete single, continuous, scanning or non-continuous mode conversion. In scan mode, the selected set of analog inputs is automatically converted.

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.
An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timers (TIM1 and TIM8) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.27 Digital-to-analog converter(DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure consists of an integrated resistor string and an amplifier in a reversed phase configuration

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotone output
- Left/right data alignment in 12-bit mode
- Synchronous update function

- The generation of noise waves
- Triangular wave generation
- Dual DAC channel independent or synchronous conversion
- Each channel DMA capability
- Externally triggered conversion
- Input reference voltage VREF+
- Eight Dacs trigger input sources, supporting DMA interfaces

3.28 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < VDDA < 3.6 V. The temperature sensor is internally connected to the ADC input channel which is used to convert the sensor output voltage into a digital value.

3.29 Serial debugging (SWD/Trace)

Debug Trace interface (SWD/Trace)
The SWD interface can be used to send debugging instructions and receive debugging data
The Trace interface can be used to trace the executed instruction stream in real time

3.30 Operational amplifier(Op-Amp)

3 (Rail to Rail) operational amplifier

3.31 True Random Number Generator (TRNG)

TRNG is a true random number generator that can continuously supply 32-bit true random numbers

3.32 Advanced Encryption Standard (AES)

- supports 128-bit AES hardware encryption and decryption operations.
- Support for DMA interface.
- Support ECB/CBC/CTR modes.

4 Electrical Characteristics

4.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to VSS.

4.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are at ambient temperature of 25 °C and VDD = 3.3V. The characteristic values in the table are based on design simulation, process characteristics and have not been tested in mass production

4.1.2 Typical values

Unless otherwise specified, Typical values are based on ambient temperatures of 25 °C and VDD = 3.3V .

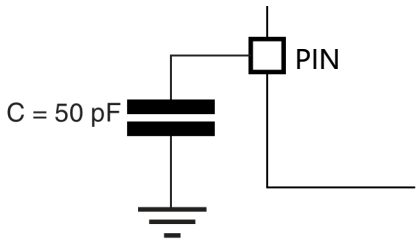
4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in 4.1-1.

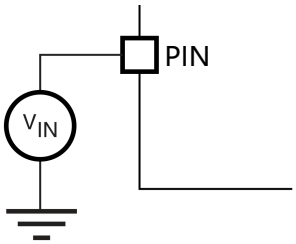
Fig 4.1-1 Pin loading conditions



4.1.5 Pin input voltage

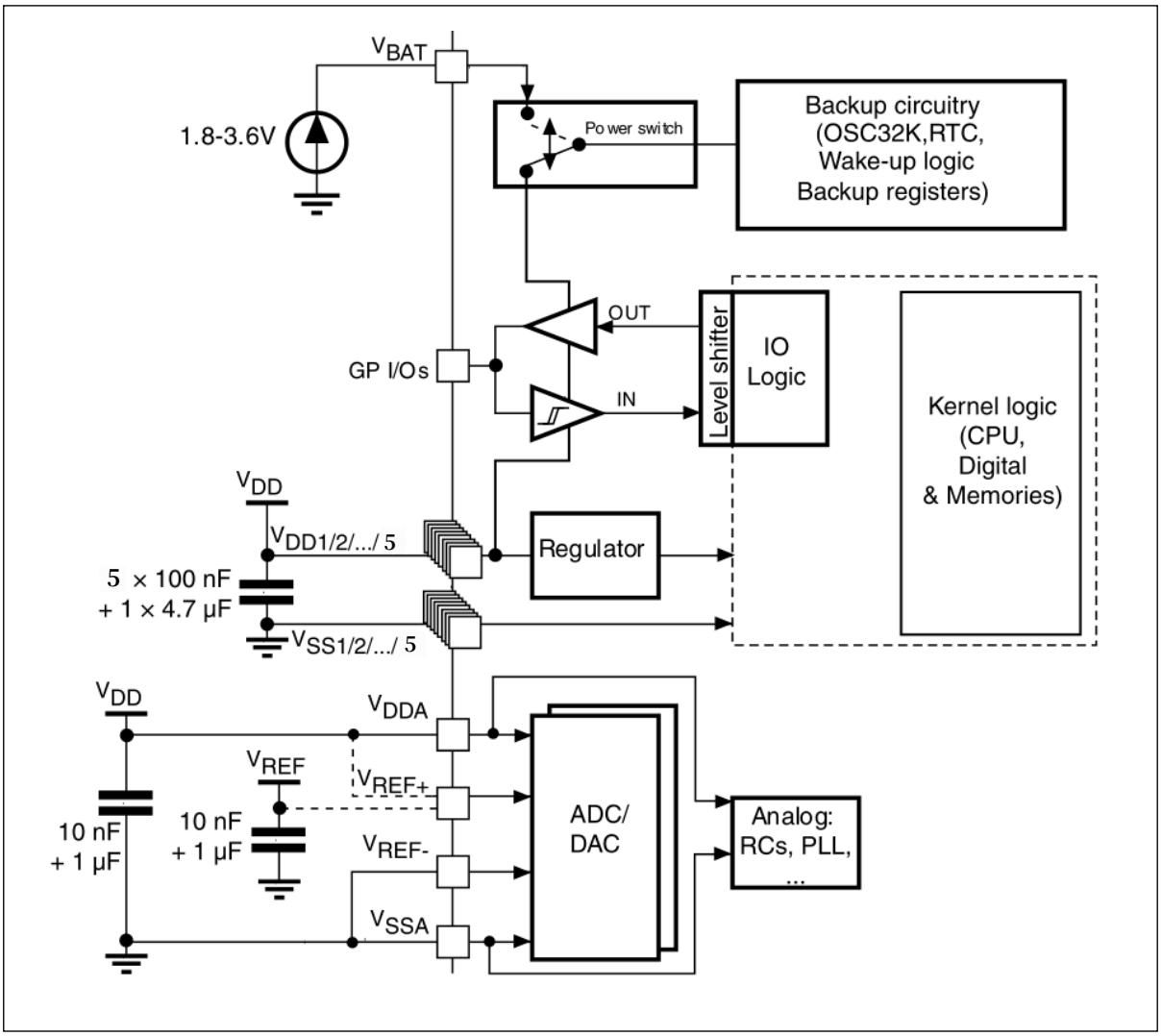
The input voltage measurement on a pin of the device is described in 4.1-2.

Fig 4.1-2 Pin input voltage



4.1.6 Power supply scheme

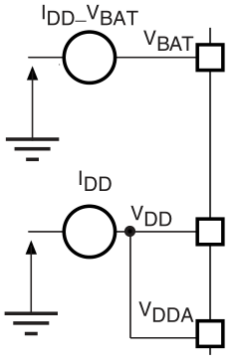
Fig 4.1-3 Pin supply scheme



NOTE: *4.7uF capacitor must be connected to* V_{DD_3}

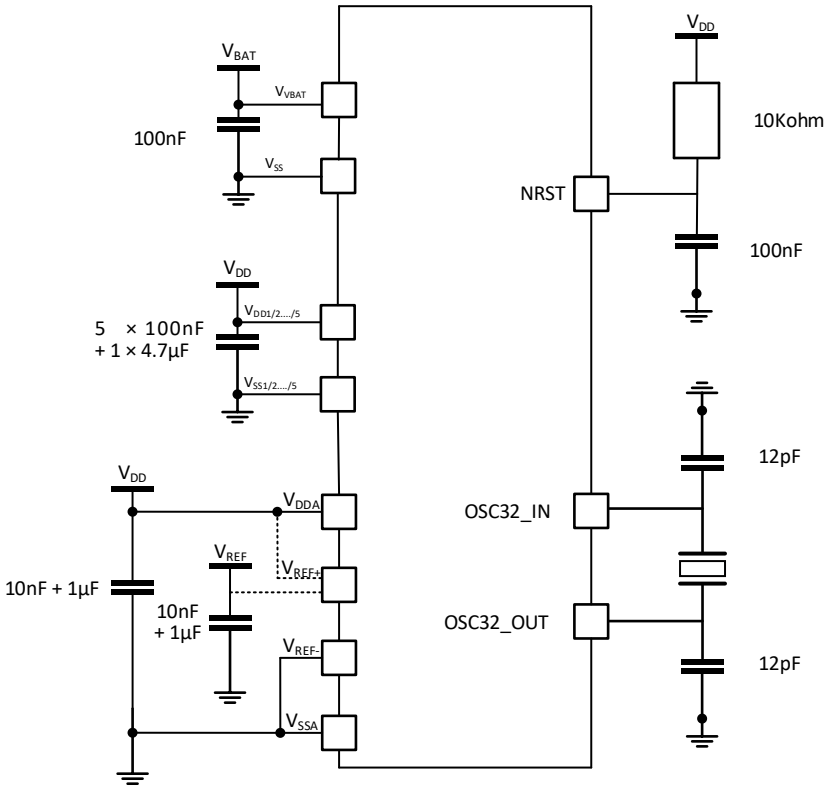
4.1.7 Current consumption measurement

Fig 4.1-4 Current consumption measurement



4.2 Typical application block diagram

Fig 4.2-1 MG32F157 Typical application block diagram



4.3 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

4.3.1 Voltage characteristics

Tab 4.3-1 Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} - V_{SS}	External main supply voltage (including VDDA, VSSA)	-0.3	4.0	V
V_{IN}	Input voltage on five volt tolerant pin	V_{SS} - 0.3	5.5	
	Input voltage on any other pin	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between different ground pins	-	50	

4.3.2 Current characteristics

Tab 4.3-2 Current characteristics

Symbol	Ratings	Max	Unit
I_{VDD}	Total current into VDD power lines (source)	150	mA
I_{VSS}	Total current out of VSS ground lines (sink)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$	Injected current on five-volt tolerant I/O	±5	
	Injected current on any other pin	±5	
$\sum I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)	±25	

4.3.3 Thermal characteristics

Tab 4.3-3 Thermal characteristics

Symbel	Rating	Value	Unit
T_{STG}	Storage temperature range	-65 ~ +150	°C
T_J	Maximum junction temperature	150	

4.4 Operating conditions

4.4.1 General operating conditions

Tab 4.4-1 Power on Reset characteristics

Symbol	Parameter	Conditions	Min	Max	Uint
f_{HCLK}	Internal AHB clock frequency	-	0	96	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	96	
f_{PCLK2}	Internal APB2 clock frequency	-	0	96	
V_{DD}	Standard operating voltage	-	2	3.6	V
VDDA	Analog operating voltage(ADC not used)	Must be the same potential as VDD	2	3.6	
	Analog operating voltage(ADC used)	-	2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	
T_A	Ambient temperature	Maximum power dissipation	-40	85	°C
		Low power dissipation	-40	105	
T_J	Junction temperature range	Basic	-40	105	
		extended	-40	125	

4.4.2 Operating conditions at power-up / power-down

Tab 4.4-2 Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Uint
t_{VDD}	VDD rise time rate	-	0	-	∞	us/V
	VDD fall time rate	-	20	-	∞	-

4.4.3 Embedded reset and power control block characteristics

Tab 4.4-3 PVD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector select (rising edge)	PLS[2:0] = 000	2.1	2.18	2.26	V
		PLS[2:0] = 001	2.19	2.28	2.37	
		PLS[2:0] = 010	2.28	2.38	2.48	
		PLS[2:0] = 011	2.38	2.48	2.58	
		PLS[2:0] = 100	2.47	2.58	2.69	
		PLS[2:0] = 101	2.57	2.68	2.79	
		PLS[2:0] = 110	2.66	2.78	2.90	
		PLS[2:0] = 111	2.76	2.88	3.00	
	Programmable voltage detector select (falling edge)	PLS[2:0] = 000	2.0	2.08	2.16	
		PLS[2:0] = 001	2.09	2.18	2.27	
		PLS[2:0] = 010	2.18	2.28	2.38	
		PLS[2:0] = 011	2.28	2.38	2.48	
		PLS[2:0] = 100	2.37	2.48	2.59	
		PLS[2:0] = 101	2.47	2.58	2.69	
		PLS[2:0] = 110	2.56	2.68	2.80	
		PLS[2:0] = 111	2.66	2.78	2.90	
$V_{PVDhyst}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power off threshold	rising edge	1.80	1.88	1.96	V
		falling edge	1.84	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}$	Reset temporization	-	-	2.5	-	ms

4.4.4 Embedded reference voltage

Tab 4.4-4 Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Uint
V_{REFINT}	Internal reference voltage	-40°C < T_A < +105°C	-	1.0	-	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	-	10	-	us
T_{Coeff}	Temperature coefficient	-	-	-	100	ppm/°C

4.4.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
All current consumption in the running mode is performed in a simplified code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 48 MHz and 1

wait states above)

- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/2}$,$f_{PCLK2} = f_{HCLK}$

Tab 4.4-5 Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Conditions	f_{HCLK}	Max	Uint
			T_A=105°C	
I_{DD}	External clock , all peripherals enabled	96 MHz	58.8	mA
		72 MHz	50.7	
		48 MHz	42.1	
		36 MHz	37.5	
		24 MHz	33.1	
		16 MHz	30.2	
		8 MHz	27.3	
	External clock , all peripherals disabled	96 MHz	12.9	
		72 MHz	10.0	
		48 MHz	7.9	
		36 MHz	5.3	
		24 MHz	4.9	
		16 MHz	3.5	
		8 MHz	2.6	

Tab 4.4-6 Maximum current consumption in Run mode, code with data processing running from SRAM

Symbol	Conditions	f_{HCLK}	Max	Uint
			T_A=105°C	
I_{DD}	External clock , all peripherals enabled	96 MHz	61.8	mA
		72 MHz	53.2	
		48 MHz	44.2	
		36 MHz	39.4	
		24 MHz	34.8	
		16 MHz	31.7	
		8 MHz	28.7	
	External clock , all peripherals disabled	96 MHz	13.5	
		72 MHz	10.5	
		48 MHz	8.3	
		36 MHz	5.5	
		24 MHz	5.2	
		16 MHz	3.7	
		8 MHz	2.7	

Tab 4.4-7 Maximum current consumption in Sleep mode, code with data processing running from flash or SRAM

Symbol	Conditions	f_{HCLK}	Max	Uint
			T_A=105°C	
I_{DD}	External clock , all peripherals enabled	96 MHz	41.2	mA
		72 MHz	35.5	
		48 MHz	29.4	
		36 MHz	26.3	
		24 MHz	23.2	
		16 MHz	21.2	
		8 MHz	19.1	
	External clock , all peripherals disabled	96 MHz	9.0	
		72 MHz	7.0	
		48 MHz	5.6	
		36 MHz	3.7	
		24 MHz	3.4	
		16 MHz	2.4	
		8 MHz	1.8	

Tab 4.4-8 Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ			Max	Uint
			VDD/VBAT = 2.0V	VDD/VBAT = 2.4V	VDD/VBAT = 3.3V	T_A = 105°C	
I_{DD}	upply current in Stop mode	Regulator running mode, low and high speed internal oscillators off, high speed crystal oscillator off (no independent watchdog)	80	85	115	1300	uA
		Regulator low power mode, low and high speed internal oscillators off, high speed crystal oscillator off (no independent watchdog)	85	90	95	1250	
	upply current in Standby mode	Low-speed internal oscillator and independent watchdog ON	1.8	1.9	2.3	-	
		Low-speed internal oscillator ON, independent watchdog OFF	1.6	1.7	2.1	-	
		Low-speed internal oscillator and independent watchdog OFF,Low-speed crystal oscillator and real time clock OFF	1.2	1.3	1.5	4.8	
I_{DD_VBAT}	Backup domain supply current	Low-speed crystal oscillator and real time clock ON	0.8	0.85	0.9	2.3	

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 48 MHz and 1 wait states above).
- Prefetch is ON (reminder: this bit must be set before clock setting and bus prescaling).
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/4}$, $f_{PCLK2} = f_{HCLK/2}$, $f_{ADCCLK} = f_{PLCK2}/4$

Tab 4.4-9 Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Conditions	f_{HCLK}	Typ		Uint
			All peripherals enable	All peripherals disabled	
I_{DD}	External clock	96 MHz	56.7	12.1	mA
		72 MHz	47.4	8.5	
		48 MHz	38.9	6.2	
		36 MHz	34.9	4.4	
		24 MHz	30.4	3.5	
		16 MHz	27.8	2.3	
		8 MHz	25.1	2.0	
		4 MHz	22.2	1.8	
		2 MHz	21.5	1.6	
		1 MHz	21.3	1.3	
		500 KHz	21.0	1.1	
		125 KHz	20.9	1.0	
	Run under an internal high speed oscillator	64 MHz	42.7	7.7	
		48 MHz	38.1	6.0	
		36 MHz	34.2	4.3	
		24 MHz	29.8	3.4	
		16 MHz	27.3	2.3	
		8 MHz	24.6	1.9	
		4 MHz	21.8	1.7	
		2 MHz	21.0	1.5	
		1 MHz	20.9	1.3	
		500 KHz	20.6	1.1	
		125 KHz	20.5	1.0	

Tab 4.4-10 Typical current consumption in Sleep mode, code with data processing running from Flash or SRAM

Symbol	Conditions	f_{HCLK}	Typ		Uint
			All peripherals enable	All peripherals disabled	
I_{DD}	External clock	96 MHz	39.7	8.5	mA
		72 MHz	33.2	6.0	
		48 MHz	27.2	4.3	
		36 MHz	24.4	3.1	
		24 MHz	21.3	2.4	
		16 MHz	19.5	1.6	
		8 MHz	17.6	1.4	
		4 MHz	15.5	1.2	
		2 MHz	15.0	1.1	
		1 MHz	14.9	0.9	
		500 KHz	14.7	0.8	
		125 KHz	14.6	0.7	
	Run under an internal high speed oscillator	64 MHz	29.9	5.4	
		48 MHz	26.7	4.2	
		36 MHz	23.9	3.0	
		24 MHz	20.9	2.4	
		16 MHz	19.1	1.6	
		8 MHz	17.2	1.4	
		4 MHz	15.2	1.2	
		2 MHz	14.7	1.1	
		1 MHz	14.6	0.9	
		500 KHz	14.4	0.8	
		125 KHz	14.3	0.7	

4.4.6 External clock characteristics

The high-speed external user clock is generated by an external clock source

Tab 4.4-11 High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	3	8	26	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7VDD	-	VDD	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{SS}$	
$t_{w(HSE)}$	OSC_IN high or low time		16	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance		-	10	-	pf
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{DD} \leqslant V_{IN} \leqslant V_{SS}$	-	-	±1	uA

Tab 4.4-12 Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	16	32.768	200	KHz
V_{LSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$	OSC_IN high or low time		-	15259	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC_IN rise or fall time		-	1	-	
$C_{in(LSE)}$	OSC_IN input capacitance		-	10	-	pf
$DuCy_{(LSE)}$	Duty cycle		40	50	55	%
I_L	OSC_IN Input leakage current	$V_{DD} \leqslant V_{IN} \leqslant V_{SS}$	-	-	±1	uA

Fig 4.4-1 High-speed external clock source AC timing diagram

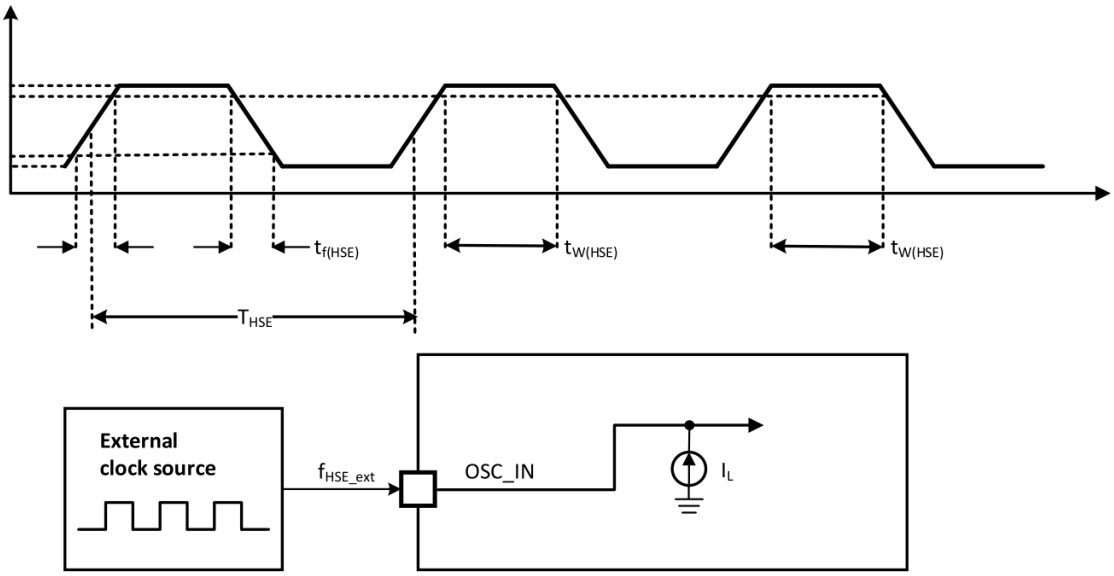
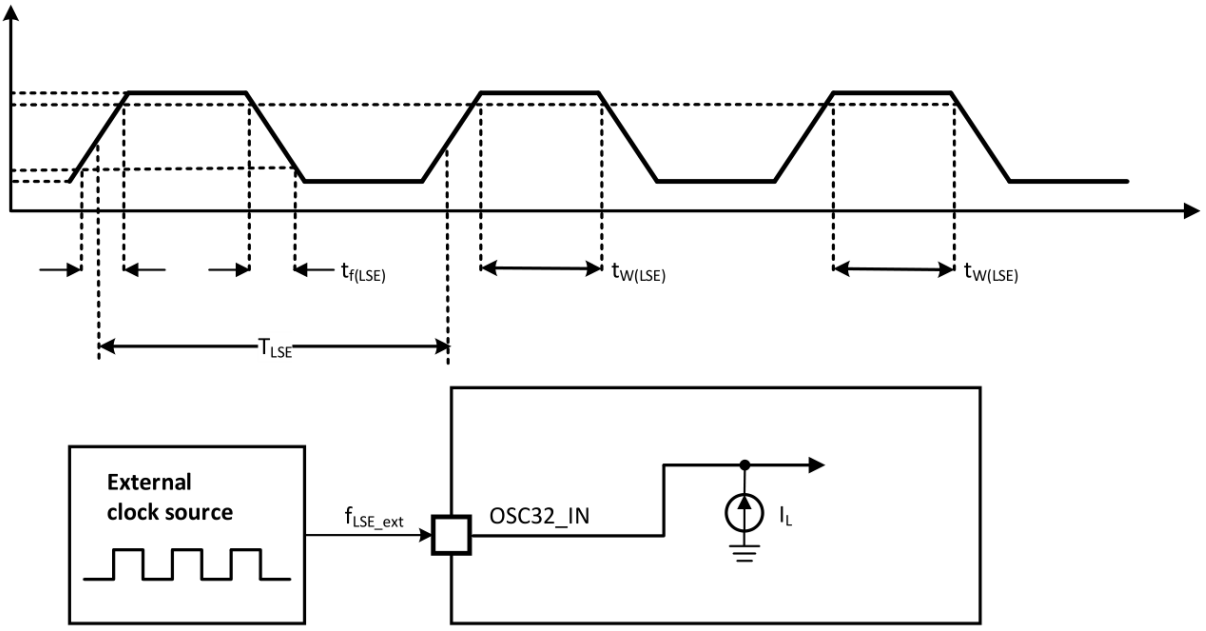


Fig 4.4-2 Low-speed external clock source AC timing diagram



High speed external user clocks are generated by crystal oscillators or ceramic resonators

Tab 4.4-13 HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	3	12	26	MHz
R_F	Feedback resistor	-	-	200	-	Ω
C	Crystal oscillator external load capacitance	-	-	12	-	pF
I_{dd}	HSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS} with 12 pF load	-	0.3	-	mA
$DuCy_{(fclk)}$	Duty cycle	wakeup	40	50	60	%
$t_{SU(HSE)}$	wakeup time	3M ~ 26MHz	-	250	-	us

Low speed user clocks are generated by crystal oscillators or ceramic resonators

Tab 4.4-14 LSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	40	65	85	Ω
C	Crystal oscillator external load capacitance	-	-	12	-	pF
I_{dd}	LSE driving current	ESR = 65kOhm, C_{SCLK} = 12pF	-	250	-	nA
$DuCy_{(fclk)}$	Duty cycle	wakeup	40	50	60	%
$t_{SU(LSE)}$	wakeup time	ESR = 65kOhm, C_{SCLK} = 12pF	-	2	4	s

4.4.7 Internal clock source characteristics

Tab 4.4-15 High-speed internal (HSI) oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
$ACC_{(HSI)}$	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.5	-	2.5	%
		T_A = -10 to 85°C	-2	-	2	%
		T_A = -0 to 70°C	-1.5	-	1.5	%
		T_A = 25°C	-0.8	-	0.8	%
$t_{SU(HSI)}$	HSI oscillator wakeup time	-	-	2	-	us
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	70	-	uA

Tab 4.4-16 Low-speed internal (LSI) oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	38	40	42	kHz
$T_{SU(LSI)}$	LSI oscillator wakeup time	-	-	70	-	us
$I_{DD(LSI)}$	LSI oscillator power consumption	-	0.2	0.25	0.35	uA

Tab 4.4-17 Low-power mode wakeup timings

Symbol	Parameter	Min	Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	4	-	us
t_{WUSTOP}	Wakeup from Stop mode (regulator in run mode)	-	17	-	
t_{WSTDBY}	Wakeup from Standby mode	-	100	-	

Low power mode wakeup time was measured during the wakeup phase using HSI
Wake up time is the time from the wake up event to the first instruction read by the user program

4.4.8 PLL characteristics

Tab 4.4-18 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	4	-	26	MHz
	PLL input clock duty cycle	-	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	-	8	-	96	MHz
T_{LOCK}	PLL lock time	-	-	-	100	us

4.4.9 Memory characteristics

Tab 4.4-19 Memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PROG}	32bit program time	T_A = -40 to +105 °C	-	10	-	us
t_{ERASE}	Page(1 Kbytes) erase time	T_A = -40 to +105 °C	-	4	-	ms
t_{ME}	Mass erase time	T_A = -40 to +105 °C	20	-	40	ms
I_{DD}	Current consumption	f_{HCLK} = 48MHz , Read mode	-	3.5	4.5	mA
		f_{HCLK} = 48MHz , Programming mode	-	-	2	
		f_{HCLK} = 48MHz , Erase mode	-	3	1	
		Standby	-	50/25C	70/25C	
V_{prog}	Programming voltage		2	-	3.6	V
I	Deep sleep		-	0.5/25C	2/25C	uA

Tab 4.4-20 Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 to +105 °C	100	-	-	kcycles
T_{RET}	Data retention	1 kcycle at T_A = 85 °C	30	-	-	year
		1 kcycle at T_A = 105 °C	10	-	-	
		10 kcycle at T_A = 55 °C	20	-	-	

4.4.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

Tab 4.4-21 EMS characteristics

Symbol	Parameter	Conditions	Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturb	VDD = 3.3V, LQFP100, T_A = +25 °C, f_{HCLK} = 96 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturban	VDD = 3.3V, LQFP100, T_A = +25 °C, f_{HCLK} = 96 MHz, conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems
EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations
The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials
Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.
To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring .

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Tab 4.4-22 EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs.[f_{HSE}/f_{HCLK}]		Unit
				8/48 MHz	8/96 MHz	
S_{EMI}	Peak level	VDD = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	12	12	dBuV
			30 to 130 MHz	22	19	
			130MHz to 1GHz	23	29	
			SAE EMI Level	4	4	-

4.4.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size is either 3 parts (cumulative mode) or 3 parts x(n + 1) supply pins (non-cumulative mode). The human body model (HBM) can be simulated. The tests are compliant with JESD22-A114/C101 standard.

Tab 4.4-23 ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	5000	V
$V_{ESD(CMD)}$	Electrostatic discharge voltage (charge device mode)	T_A = +25 °C, conforming to JESD22-C101	2000	

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78A IC latch-up standard.

Tab 4.4-24 Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C,compliant with JESD78A	II level A

4.4.12 IO characteristics

As a general rule, current injection to the I/O pins, due to external voltage below VSS or above VDD (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures. The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

Tab 4.4-25 I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injectio	Positive injectio	
I_{INJ}	5V compatible pin injection current	-5	+5	mA
	Injected current on any other pin	-5	+5	mA

4.4.13 I/O pin electrical characteristics

Tab 4.4-26 I/O pin electrical characteristics

Symbol	Conditions	Parameter	Min	Typ	Max	Unit
V_{IL}		DVDD=3.3V	0	-	0.8	V
		DVDD=2.0V	0	-	0.3*DVDD	
V_{IH}		DVDD=3.3V	2.0	-	DVDD	V
		DVDD=2.0V	0.7*DVDD	-	DVDD	

V_{hys}		DVDD=3.3V	310	310	330	mV
		DVDD=2.0V	300	320	320	
I_{lkg}	Input leakage current (4)	VSS ⩽ Vin ⩽ VDD Standard I/Os	-	-	±1	uA
		V_{IN} = 5 V, 5V compatible I/O port	-	-	3	
R_{PU}	Weak pull-up equivalent resistor (5)	Vin = VSS	30	40	50	KΩ
R_{PD}	Weak pull-down equivalent resistor (5)	Vin = VDD	30	40	50	
C_{IO}	I/O pin capacitance	-	-	10	-	pf

- To maintain a voltage higher than VDD + 0.3, the internal pull-up/pull-down resistance must be disabled.
- The hysteresis between Schmidtt switching levels is guaranteed by characteristic testing.
- Minimum value is 100 mV.
- If reverse current is injected into adjacent pins, the leakage current may be higher than the maximum
- If reverse current is injected into adjacent pins, the leakage current may be higher than the maximum. Pull-up and pull-down resistors are designed to be true resistors in series with switchable PMOS/NMOS. This PMOS/NMOS has the least effect on series resistance (about 10%)

Output drive current

GPIO (General Input/Output) can input and output current.
In user applications, the number of pins that can drive current must be limited to meet the maximum rated current value.

- VDD The sum of the current provided by all I/O in the VDD domain plus the maximum current consumption of products in the VDD domain cannot exceed the maximum IVDD value.
- The sum of the current provided by all I/O in the VSS domain plus the maximum current consumption of products in the VSS domain cannot exceed the maximum value of the IVSS.

Output voltage level

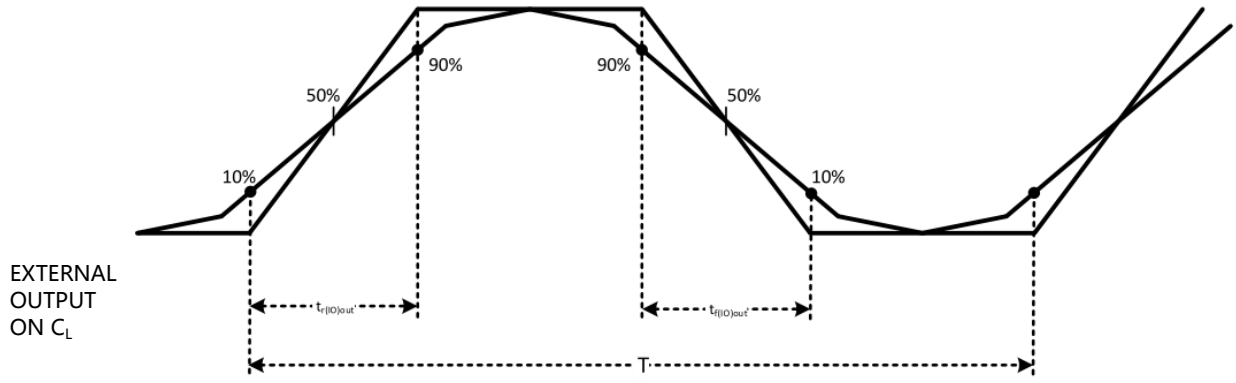
Tab 4.4-27 I/O Output voltage characteristics

Symbol	Parameter	DS[1:0]	Conditions	Min	Max	Unit
V_{OL} (1)	Output low level voltage (When the pin absorbs current)	00	2.7V < VDD < 3.6V, I_{OL} = 5mA	-	0.4	V
			2.0V < VDD < 2.7V, I_{OL} = 3mA	-	0.4	
		01	2.7V < VDD < 3.6V, I_{OL} = 8mA	-	0.4	
			2.0V < VDD < 2.7V, I_{OL} = 5mA	-	0.4	
		10	2.7V < VDD < 3.6V, I_{OL} = 15mA	-	0.4	
			2.0V < VDD < 2.7V, I_{OL} = 10mA	-	0.4	
		11	2.7V < VDD < 3.6V, I_{OL} = 20mA	-	0.4	
			2.0V < VDD < 2.7V, I_{OL} = 14mA	-	0.4	
V_{OL} (2)	Output high level voltage (When the pin provides current)	00	2.7V < VDD < 3.6V, I_{OH} = 7mA	VDD-0.4	-	
			2.0V < VDD < 2.7V, I_{OH} = 3mA	VDD-0.4	-	
		01	2.7V < VDD < 3.6V, I_{OH} = 14mA	VDD-0.4	-	
			2.0V < VDD < 2.7V, I_{OH} = 5mA	VDD-0.4	-	
		10	2.7V < VDD < 3.6V, I_{OH} = 25mA	VDD-0.4	-	
			2.0V < VDD < 2.7V, I_{OH} = 7mA	VDD-0.4	-	
		11	2.7V < VDD < 3.6V, I_{OH} = 40mA	VDD-0.4	-	
			2.0V < VDD < 2.7V, I_{OH} = 15mA	VDD-0.4	-	

- The maximum absorbed current of the pin must always not exceed the maximum absolute value. The sum of current of the IO port and control pin must not exceed the IVSS.
- The maximum value of the current supplied by the pin must always not exceed the maximum absolute value. The sum of the current of the IO port and control pin must not exceed the IVDD.

I/O AC characteristics

Fig 4.4-3 I/O AC characteristics definition



Maximum frequency is achieved if $(t_1+t_2)\leq(2/3)T$ and if the duty cycle is (45-50%) when located by C_L specified in the table "I/O AC characteristics"

Tab 4.4-28 I/O AC characteristics

MODEx[1:0]	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency	C_L = 50pF, VDD = 2V to 3.6V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50pF, VDD = 2V to 3.6V	-	125	ns
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 50pF, VDD = 2V to 3.6V	-	125	
01	$f_{max(IO)out}$	Maximum frequency	C_L = 50pF, VDD = 2V to 3.6V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50pF, VDD = 2V to 3.6V	-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 50pF, VDD = 2V to 3.6V	-	25	
11	$f_{max(IO)out}$	Maximum frequency	C_L = 30pF, VDD = 2.7V to 3.6V	-	50	MHz
			C_L = 50pF, VDD = 2.7V to 3.6V	-	30	
			C_L = 50pF, VDD = 2V to 2.7V	-	30	
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30pF, VDD = 2.7V to 3.6V	-	5	ns
			C_L = 50pF, VDD = 2.7V to 3.6V	-	8	
			C_L = 50pF, VDD = 2V to 2.7V	-	12	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30pF, VDD = 2.7V to 3.6V	-	5	
			C_L = 50pF, VDD = 2.7V to 3.6V	-	8	
			C_L = 50pF, VDD = 2V to 2.7V	-	12	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

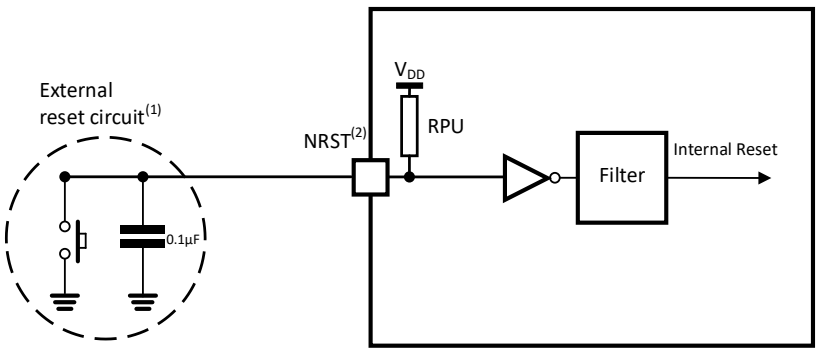
4.4.14 NRST pin define

Tab 4.4-29 I/O pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST Input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$ (1)	NRST Input high level voltage	-	-2	-	V_{DD} +0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	40	50	60	KΩ
$V_{F(NRST)}$ (1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$ (1)	NRST Input not filtered pulse	-	300	-	-	ns

1. Design guarantee
2. The pull-up is designed to be a true resistor in series with the switchable PMOS. The effect of this PMOS on the series resistance Minimum (about 10%).

Fig 4.4-4 NRST Pin protection



1. The reset system prevents the product from being parasitic reset
2. The user needs to ensure that the NRST pin level is below the $V_{IL(NRST)}$ maximum

4.4.15 TIM characteristics

Tab 4.4-30 TIM characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{res(TIM)}$	Timer resolution	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96 MHz	10.4	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 96 MHz	0	48	MHz
Res_{TIM}	Timer resolution	-	-	20	bit
$t_{COUNTER}$	20-bit counter clock period when internal clock is selected	-	1	1048575	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96 MHz	10.4	10905180	ns
t_{MAX_COUNT}	Maximum possible output	-	1	1048575 x 1048575	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 96 MHz	-	11443.2	s

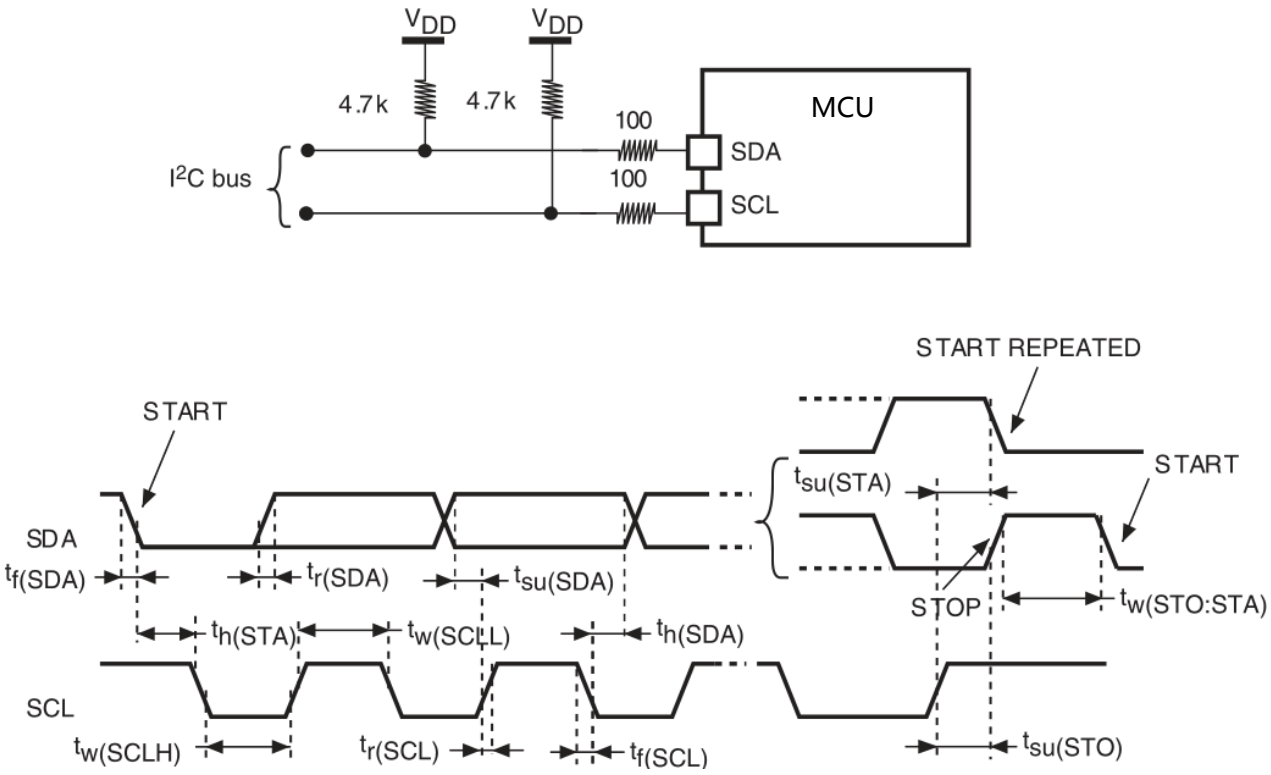
4.4.16 Communications interfaces

Tab 4.4-31 I2C interface characteristics

Symbol	Parameter	Standard mode(1)(2)		Fast mode(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	us
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	us
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	ns
$t_{h(STA)}$	Start condition establishment time	4.0	-	0.6	-	us
$t_{su(STA)}$	Repeated Start condition establishment time	4.7	-	0.6	-	us
$t_{su(STO)}$	Stop condition establishment time	4.0	-	0.6	-	us
$t_{w(STO:STA)}$	Stop to Start condition time(bus free)	4.7	-	1.3	-	us
C_b	Capacitance load per bus	-	400	0	400	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filte	0	50(4)	0	50(4)	ns

1. Design guarantee
2. $_{PCLK1}$ must be at least 2MHz to meet the standard I2C frequency requirement, at least 4MHz to meet the fast I2C frequency requirement, and must be a multiple of 10MHz to meet the fast I2C mode maximum clock speed of 400KHz
3. At least 300ns of hold time must be provided for the SDA signal within the product to connect the undefined region of the SCL's falling edge
4. The minimum width of the peak filtered by the analog filter is greater than the maximum t_{SP}

Fig 4.4-5 I2C bus AC waveforms and measurement circuit



1. Measurement point in CMOS level: 0.3VDD and 0.7VDD
2. Rs: serial protection resistor
3. Rp: pull-up resistor
4. V_{DD_I2C}: I2C bus power supply

Tab 4.4-32 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Typ
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	36	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK}=36 MHz, presc=4	50	60	ns
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5	-	ns
		Slave mode	5	-	
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master mode	5	-	ns
		Slave mode	4	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK}=20 MHz	0	$3t_{PCLK}$	ns
$t_{dis(SO)}$ (1)(3)	Data input disable time	Slave mode	2	10	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$ (1) $t_{h(MO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15	-	ns
		Master mode (after enable edge)	2	-	

1. Characteristic test guarantee
2. The minimum time is the minimum time for driving output, and the maximum time is the maximum time for validating data
3. The minimum time is the minimum time when the output is invalid, and the maximum time is the maximum time when the data is high resistance

Fig 4.4-6 SPI timing diagram - slave mode and CPHA = 0

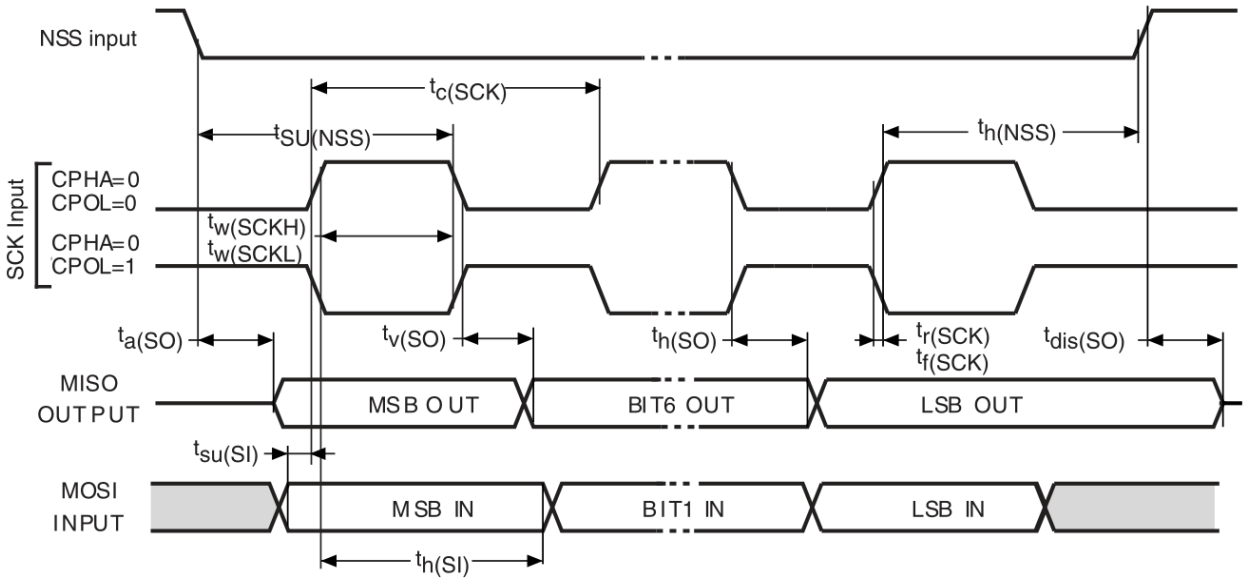


Fig 4.4-7 SPI timing diagram - slave mode and CPHA = 1

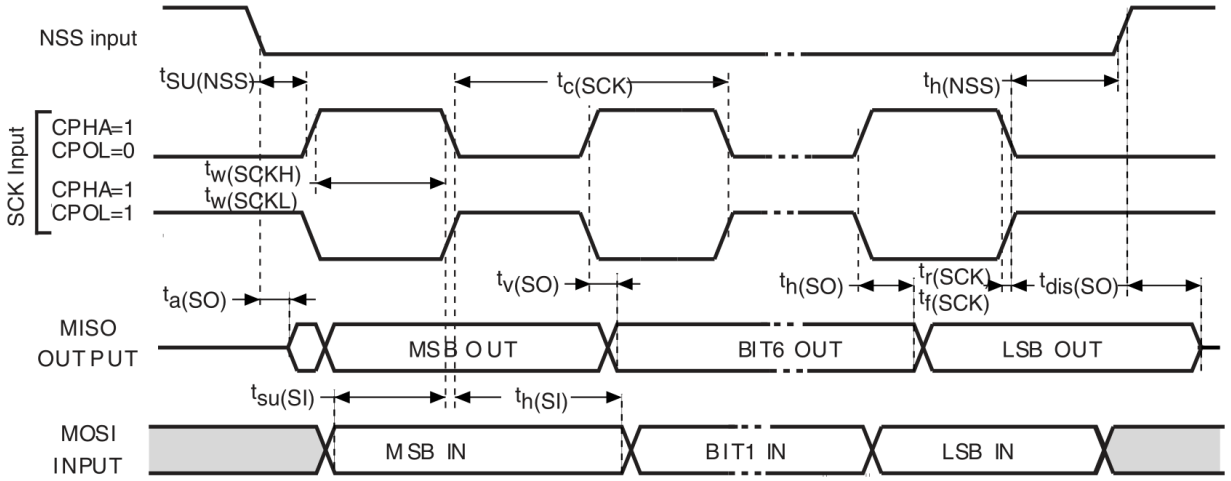
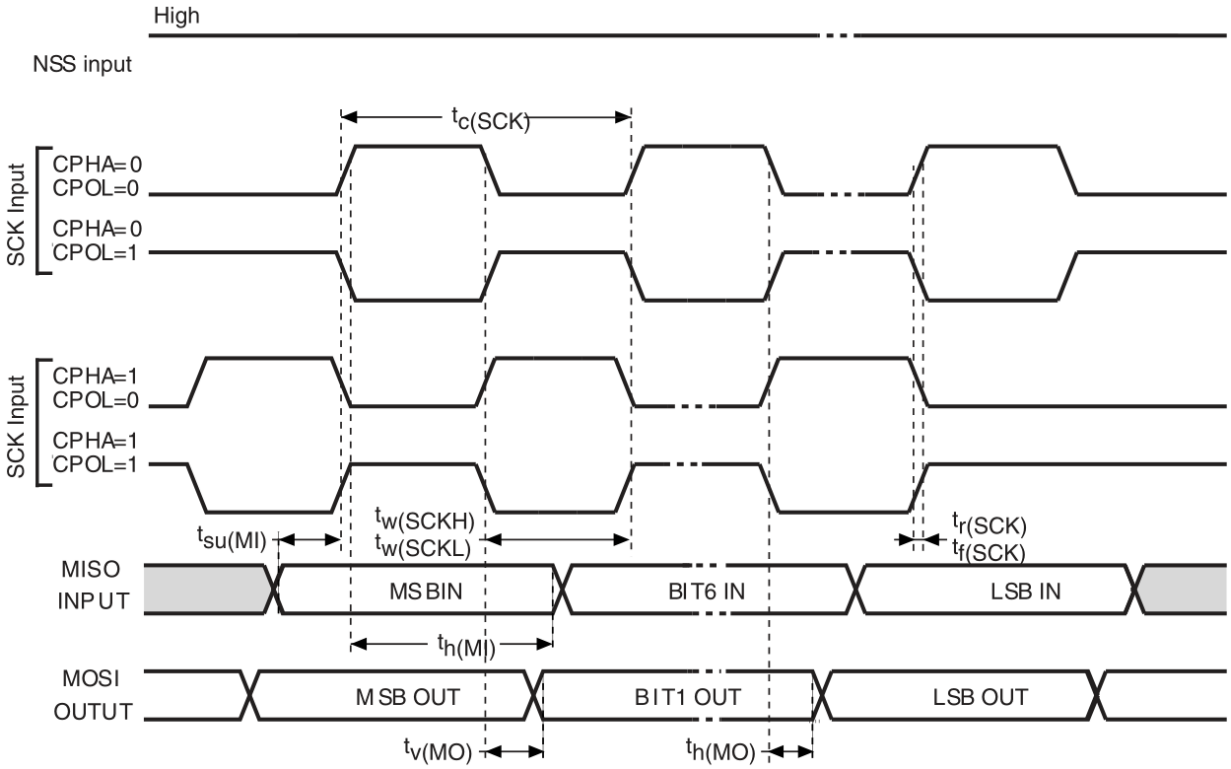


Fig 4.4-8 SPI timing diagram - master mode



Tab 4.4-33 I2S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
f_{CK} $1/t_{c(CK)}$	I2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.522	1.525	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I2S clock rise and fall time	Capacitive load: C_L = 50 pF	-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode	3	-	ns
$t_{h(WS)}$ (1)	WS hold time	I2S2 Master mode	2	-	ns
		I2S3 Master mode	0	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	4	-	ns
$t_{h(WS)}$ (1)	WS hold time	Slave mode	0	-	ns
$t_{w(CKH)}$ (1)	CK high and low time	Master f_{PCLK}=16 MHz, audio frequency=48 kHz	312.5	-	ns
$t_{w(CKL)}$ (1)			345	-	
$t_{su(SD\_MR)}$ (1)	Data input setup time	I2S2 Master receiver	2	-	ns
		I2S3 Master receiver	6.5	-	
$t_{su(SD\_SR)}$ (1)	Data input setup time	Slave receiver	1.5	-	ns
$t_{h(SD\_MR)}$ (1)(2)	Data input hold time	Master receiver	0	-	ns
$t_{h(SD\_SR)}$ (1)(2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$ (1)(2)	Data output valid time	Slave transmitter (after enable edge)	-	18	ns
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)	11	-	ns
$t_{v(SD\_MT)}$ (1)(2)	Data output valid time	Master transmitter (after enable edge)	-	3	ns
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)	0	-	ns

1. Feature test or design assurance
2. Depends onf_{PCLK}. For example, if f_{PCLK} = 8MHz, $T_{pclk} = 1/f_{PCLK}$ = 125ns

Fig 4.4-9 I2S Slave Waveform Diagram

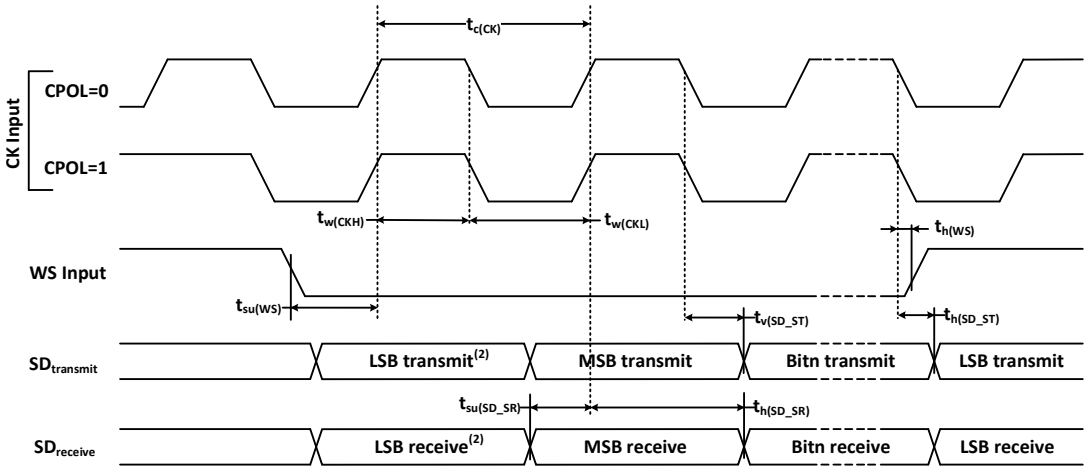
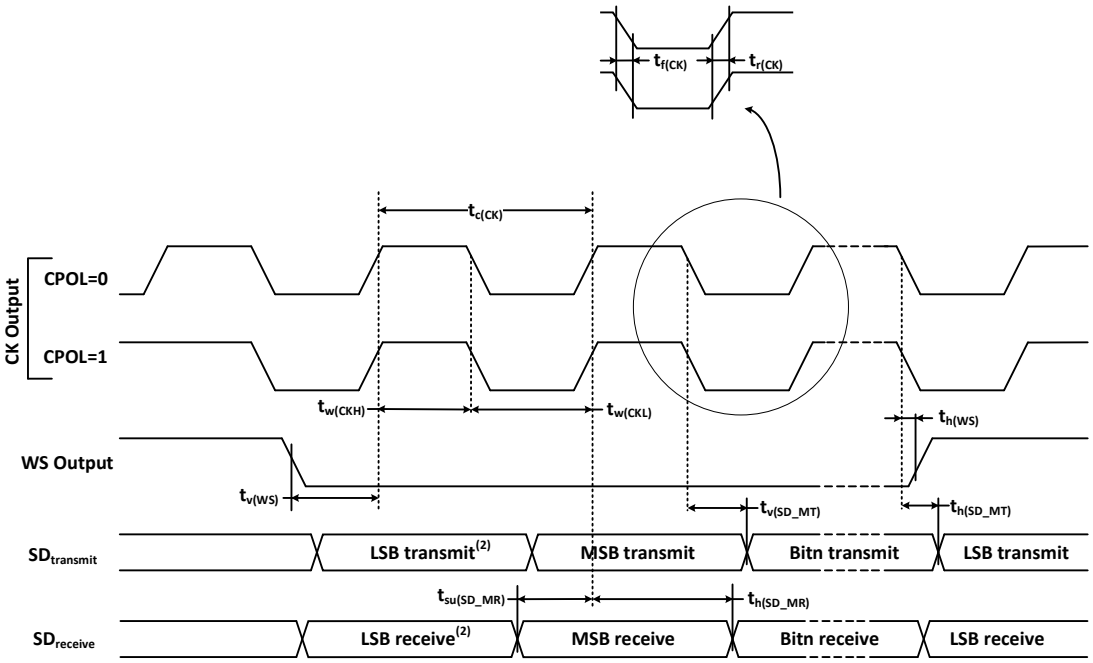


Fig 4.4-10 I2S Master Waveform Diagram



SD/SDIO MMC master interface （SDIO）characteristics

Fig 4.4-11 SDIO High speed mode

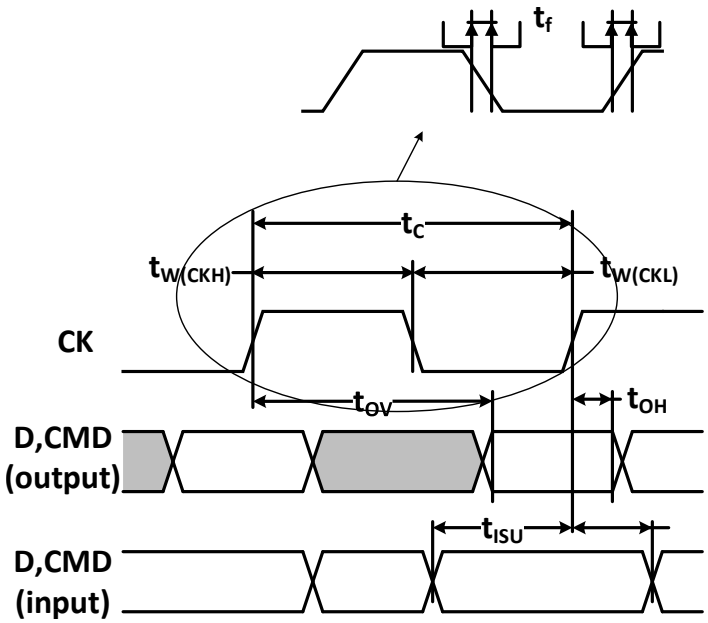
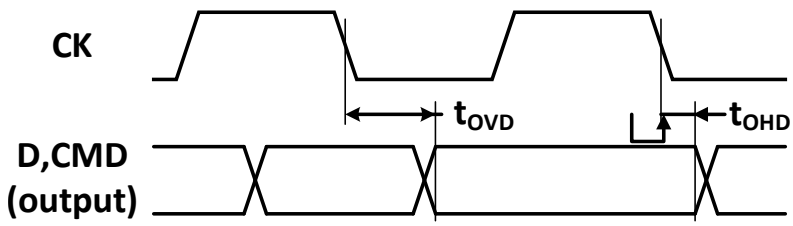


Fig 4.4-12 SDIO Default mode



Tab 4.4-34 SDSD/MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \leqslant 30pF$	0	48	MHz
$t_{W}CKL$	Clock low time, f_{PP} = 16 MHz	$C_L \leqslant 30pF$	32	-	ns
$t_{W}CKH$	Clock high time, f_{PP} = 16 MHz	$C_L \leqslant 30pF$	30	-	
t_r	Clock rise time	$C_L \leqslant 30pF$	-	4	
t_f	Clock fall time	$C_L \leqslant 30pF$	-	5	
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \leqslant 30pF$	2	-	ns
t_{IH}	Input hold time	$C_L \leqslant 30pF$	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \leqslant 30pF$	-	6	ns
t_{OH}	Output hold time	$C_L \leqslant 30pF$	0	-	
CMD, D outputs (referenced to CK) in SD default mode					
t_{OVD}	Output valid default time	$C_L \leqslant 30pF$	-	7	ns
t_{OHD}	Output hold default time	$C_L \leqslant 30pF$	0.5	-	

1. referenced SDIO_CLKCR,SDI clock control register controls the CK output

Tab 4.4-35 SD characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \leqslant 30pF$	0	48	MHz
$t_{W}CKL$	Clock low time, f_{PP} = 16 MHz	$C_L \leqslant 30pF$	32	-	ns
$t_{W}CKH$	Clock low time, f_{PP} = 16 MHz	$C_L \leqslant 30pF$	30	-	
t_r	Clock rise time	$C_L \leqslant 30pF$	-	4	
t_f	Clock fall time	$C_L \leqslant 30pF$	-	5	
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \leqslant 30pF$	2	-	ns
t_{IH}	Input hold time	$C_L \leqslant 30pF$	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \leqslant 30pF$	-	6	ns
t_{OH}	Output hold time	$C_L \leqslant 30pF$	0	-	
CMD, D outputs (referenced to CK) in SD default mode					
t_{OVD}	Output valid default time	$C_L \leqslant 30pF$	-	7	ns
t_{OHD}	Output hold default time	$C_L \leqslant 30pF$	0.5	-	

4.4.17 USB characteristics

Tab 4.4-36 USB characteristics

Symbol	Parameter	Max	Unit
$t_{STARTUP}$	USB transceiver startup time	1	µs

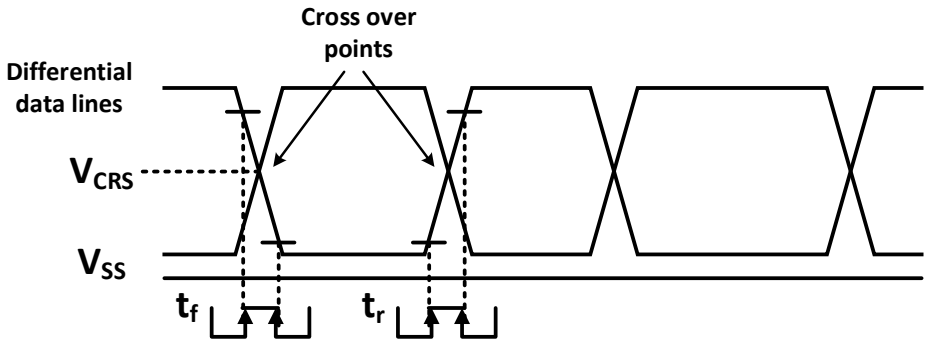
Tab 4.4-37 USB DC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	USB operating voltage	-	3.0	3.6	V
V_{DI}	Differential input sensitivity	I(USBDP, USBDM)	0.2	-	V
V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	2.5	V
V_{SE}	Single ended receiver threshold	-	1.3	2.0	V
V_{OL}	Static output level low	1.5K resistor to 3.6V	-	0.3	V
V_{OH}	Static output level high	1.5K resistor to VSS	2.8	3.6	V

[1] To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range

1. All voltages are measured locally
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range
3. USB function can work at 2.7V, but full speed USB feature will decay between 2.7V and 3V
4. Feature test guarantee
5. RL is the load connected to the USB driver

Fig 4.4-13 USB timings: definition of data signal rise and fall time



Tab 4.4-38 USB full-speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time	C_L = 50pf	4	20	ns
t_f	Fall time	C_L = 50pf	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
t_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

4.4.18 12-bit ADC characteristics

Tab 4.4-39 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	VDDA	V
V_{REF-}	Negative reference voltage	-	0			V
I_{ADC}	ADC working current	-	0.65	0.9	1.23	mA
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_s	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 16MHz	-	-	1	MHz

			-	-	16	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0 (VSSA or VREF-tied to ground)	-	V_{REF+}	V
C_{ADC}	Internal sample and hold capacitor	-	-	12	-	pF
t_{lat}	Injection trigger conversion latency	f_{ADC} = 16MHz	-	-	0.5	µs
		-	-	-	8	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 16MHz	-	-	0.44	µs
		-	-	-	7	$1/f_{ADC}$
t_S	Sampling time	f_{ADC} = 16MHz	-	-	15	µs
		-	-	-	239.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	-	1	-	µs
t_{CONV}	Total conversion time(including sampling time)	f_{ADC} = 16MHz	1.0625	-	15.75	µs
		-	17 to 252 (t_S for sampling +12.5 for successive approximation			$1/f_{ADC}$

$$R_{AIN} < \frac{T_S}{f_{ADC} X C_{ADC} X ln(2^{N+2})} - R_{ADC}$$

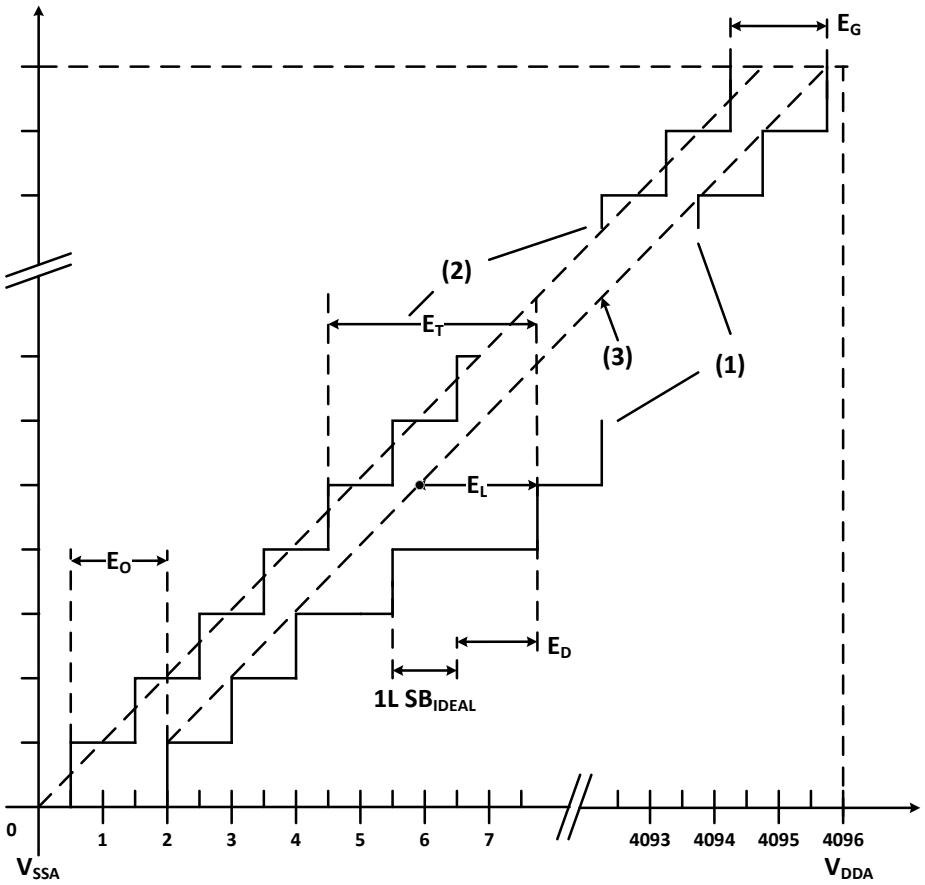
The formula above is used to determine the maximum external impedanceallowed for an error below 1/4 of LSB. Here N = 12 , RAIN max for f_{ADC} = 16MHz

T_s**(cycles)**	T_s**(µs)**	R_{AIN} **MAX (KΩ)**
4	0.25	2.14
8	0.5	4.29
16	1	8.58
32	2	17.17
64	4	34.34
128	8	68.69
256	16	137.39

Tab 4.4-40 ADC accuracy

Symbol	Parameter	Conditions	Typ	Max(4)	Unit
ET	Is calibration error	f_{PCLK2} = 56 MHz, f_{ADC} = 16 MHz, R_{AIN} < 10 KΩ, V_{DDA} = 3 V ∼ 3.6 V	±1.3	±2	LSB
EO	Displacement error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Difference line error		±0.7	±1	
EL	Integral linear error		±0.8	±1.5	

Fig 4.4-14 ADC accuracy characteristic



1. Actual conversion curve
2. Ideal transition curve
3. Terminal correlation line
4. ET = Total unadjusted error, maximum error between actual and ideal conversion curves
   EO = offset error, the difference between the first actual conversion and the first ideal conversion
   EG = Gain error, the difference between the last actual conversion and the last ideal conversion
   EL = Integral linear error, the maximum error of any actual transformation and end point correlation line

4.4.19 DAC characteristics

Tab 4.4-41 DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V_{REF+}	Reference supply voltage	2.4	-	V_{DDA}	V	V_{REF+} must always be below V_{DDA}
V_{SSA+}	ground	0	-	0	V	-
R_{LOAD} (1)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O (2)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and VSS to have a 1% accuracy is 1.5 MΩ
R_{LOAD} (1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).

DAC_OUT buf_on (1)	output voltage with buffer ON	0.15	-	V_{DDA}-0.15	V	It gives the maximum output excursion of the DAC. It corresponds to input code(0x0E0) to (0xF1C) at VREF+ = 3.6 V and (0x155) to (0xEAB) at VREF+ = 2.4 V
DAC_OUT buf_off (1)	output voltage with buffer OFF	0	-	V_{REF}	V	
I_{DDA_off}	Standby power consumption	-	-	1	uA	-
I_{DDA}	Operating power consumption	-	0.35	-	mA	-
T_{STB}	Output voltage stabilization time	-	-	50	us	-
DNL(2)	Differential non linearity	-	-	±2	LSB	Given for the DAC in 12-bit configuration
INL(3)	Integral non linearity	-	-	±2	LSB	Given for the DAC in 12-bit configuration
F_{SCR}	Sampling frequency	-	-	1	MS/s	-
Offset error(3)		-	-	±2	LSB	buffer is off
Gain error(3)	Gain error	-	-	±1.25	FSR	-

1. Design guarantee
2. Characteristic test guarantee
3. The static mode corresponds to a state in which the DAC maintains a stable output level to ensure that no dynamic power consumption occurs

4.4.20 Temperature sensor characteristics

Tab 4.4-42 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	-	±2	-	°C
Avg_Slope	Average slope	-	4.3	-	mV/°C
V_{25}	Voltage at 25 °C	-	1.4	-	V
t_{START}	wakeup time	4	6	10	us
T_{S_temp}	ADC sampling time when reading the temperature	-	-	17.1	us

4.4.21 Operational amplifier characteristics

Tab 4.4-43 Operational amplifier characteristics

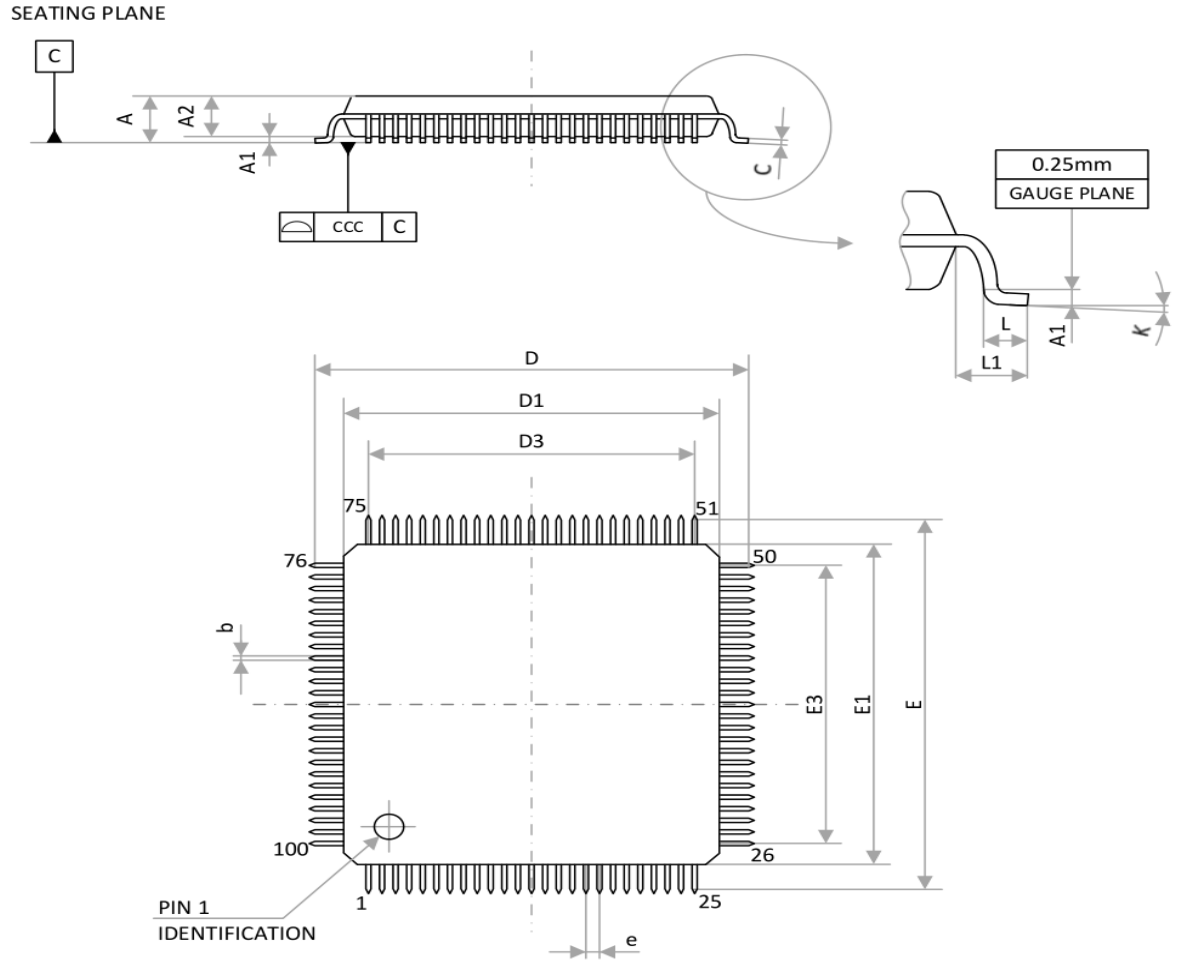
Symbol	Parameter	Min	Typ	Max	Unit	Comments
I_q	current	-	600	-	uA	-
GBW	Unit-gain bandwidth	-	20	-	MHz	Cload=100pF
Vos	Offset voltage	-	-	5	mV	-
e_n	Equivalent input noise voltage	-	18.3	-	nV/$\sqrt{}$Hz	f=10kHz
PSR	Power supply rejection ratio	-	103	-	dB	-
Gain	open-loop gain	-	106	-	dB	-
PM	Unit-gain phase margin	-	60	-	deg	Cload=100pF
SR	Conversion rate	-	11.5	-	V/us	-
Tset	Set up the time	-	85	-	ns	Vstep=500mV, Cload=100pF

1. Design guarantee
2. The minimum sampling time can be determined by several iterations in the application

5 Package characteristics

5.1 LQFP100 14x14mm

Fig 5.1-1 LQFP100 14 x 14mm, 100 pins package parameters



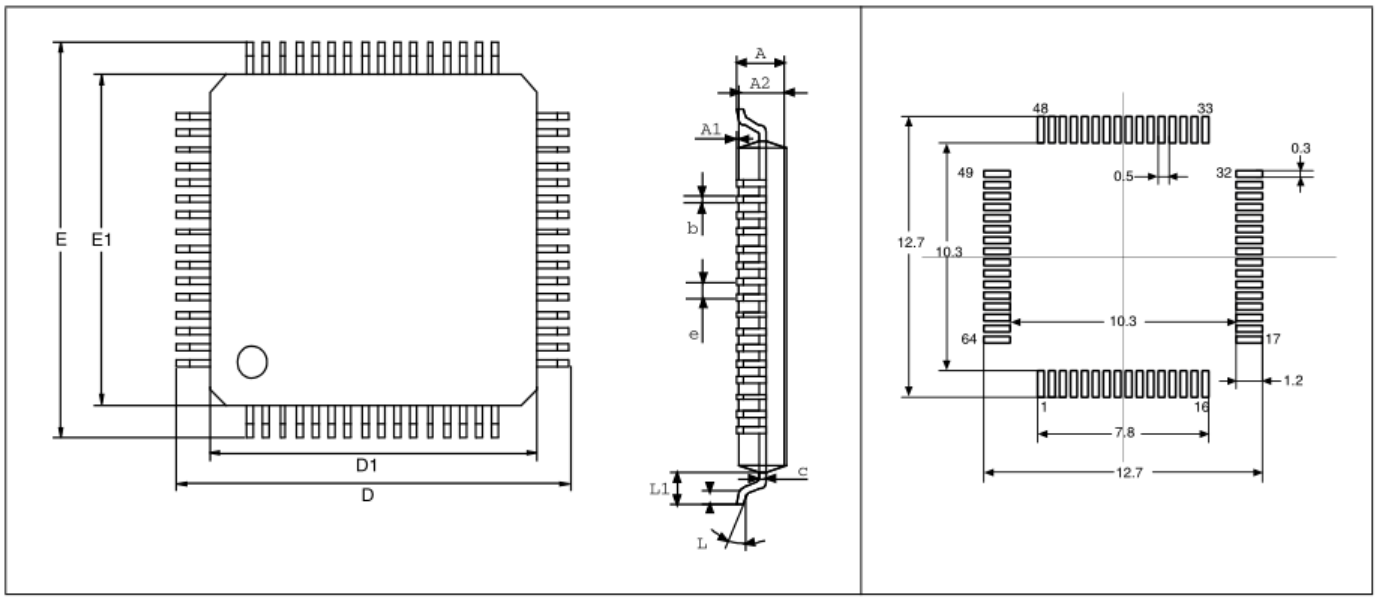
Note: *Drawing is not to scale.*

Tab 5.1-1 LQFP100 14 x 14mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			Symbol	millimeters		
	Min	Typ	Max		Min	Typ	Max
A	-	-	1.60	E	15.80	16.00	16.20
A_1	0.05	-	0.15	E_1	13.80	14.00	14.20
A_2	1.35	1.40	1.45	E_3		12.00	
b	0.17	0.22	0.27	e		0.50	
c	0.09	-	0.20	L	0.45	0.60	0.75
D	15.80	16.00	16.20	L_1		1.00	
D_1	13.80	14.00	14.20	K	0°	3.5°	7°
D_3	-	12.00	-	ccc	-	-	0.08

5.2 LQFP64 10x10mm

Fig 5.2-1 LQFP64 10 x 10mm, 64 pin package parameters



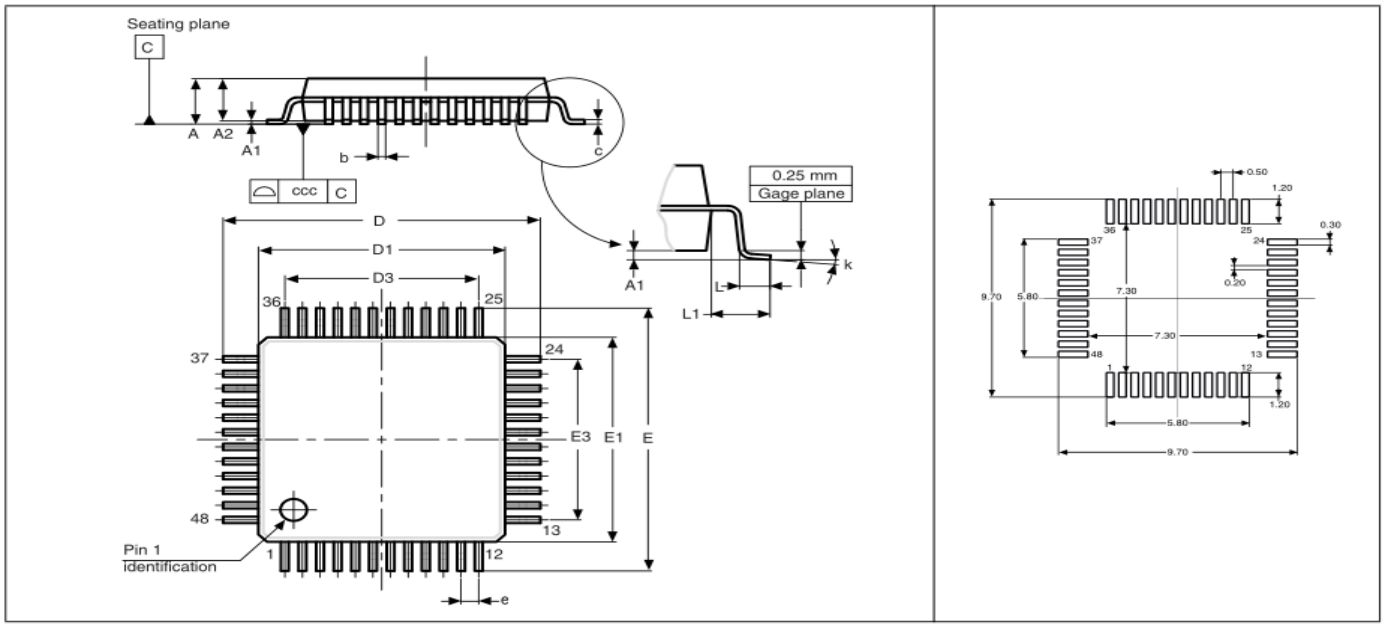
Note: *Drawing is not to scale.*

Tab 5.2-1 LQFP64, 10x10 mm, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	-	-	1.60
A_1	0.05	-	0.15
A_2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	-	12.00	-
D_1	-	10.00	-
E	-	12.00	-
E_1	-	10.00	-
e	0.50		
L	0.45	0.60	0.75
L_1	1.00		
θ	0°	3.5°	7°

5.3 LQFP48 7x7mm

Fig 5.3-1 LQFP48 7 x 7mm, 48 pin package parameters



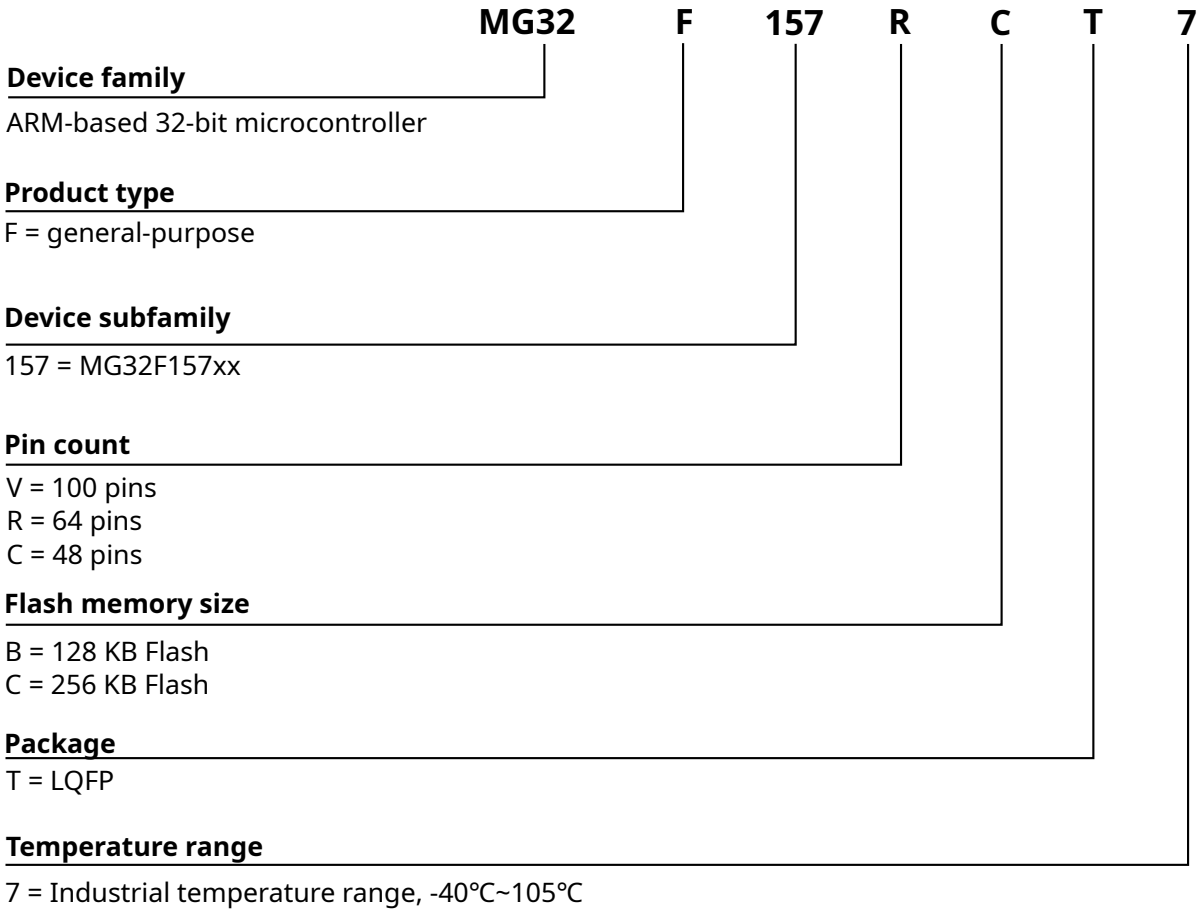
Note: *Drawing is not to scale.*

Tab 5.3-1 LQFP48, 7x7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	-	-	1.60
A_1	0.05	-	0.15
A_2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	8.80	9.00	9.20
D_1	6.80	7.00	7.20
D_3	-	5.50	-
E	8.80	9.00	9.20
E_1	6.90	7.00	7.20
E_3	-	5.50	-
e	0.50		
L	0.45	0.60	0.75
L_1	1.00		
K	0°	3.5°	7°
ccc	0.08		

6 Ordering information

Fig 6.0-1 Ordering code information



7 Revision history

Revision	Data	Changes
00.00	2022/10/10	Draft version
00.01	2022/11/12	Update TIM data
00.02	2022/11/18	Update clock tree
00.03	2023/09/26	Update RAIN formula
00.04	2023/11/26	Update LQFP48/QFN48
00.05	2024/06/04	Remove QFN48

IMPORTANT EXPLANATION

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