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M0 Cost-Efficient MCU

MG32F04A016

Arm® Cortex®-M0 based 32-bit Microcontrollers

Data Sheet

Version: 1.2

Features

- Core 32-bit Arm® Cortex®-M0, frequency up to 48MHz.
- Memory
  - **16KB** embedded Flash storage.
  - **2KB** SRAM.
- Operating voltage range is from 2.0V to 5.5V.
- Power-on and Power-down reset (POR/PDR), Programmable voltage detector (PVD).
- Built-in **40KHz** LSI low-speed oscillator.
- Built-in **48MHz** HSI high-speed oscillator.
- External clock input frequency is up to 48MHz (HSE, through OSCIN pin).
- Multiple low power modes including Sleep mode, Stop mode and Deep Stop mode.
- **5 timers**:
  - One 16-bit 4-channel advanced timer (TIM1), capable of generating four PWM outputs or three complementary PWM pairs, support center- or edge-aligned PWM mode, support hardware dead time insertion and fault brake, support PWM phase-shift output mode.
  - One 16-bit 4-channel general purpose timer (TIM3), capable of generating four PWM outputs or capture four channel input signals, support decode of hall sensor and quadrature encoder, support infrared decode.
  - One 16-bit basic timer (TIM14), capable of generating one PWM output or capture one channel input signal.
  - One watchdog timer equipped with independent clock source (IWDG).
  - One 24-bit Systick timer.
- Up to **18** fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts.
  - All I/O ports can accept input or generate output signal voltage level is not higher than V_{DD}.
- Two USART (support SPI mode).
- One I2C.
- One SPI.
- One **12-bit** ADC (Analog-to-Digital converter) supports **1M** SPS conversion rate, with 8 external inputs and 1 internal input that can sample on-chip voltage sensor.
- Embedded CRC engine
- 96bit unique chip ID (UID)
- Serial Wire Debug (SWD) for debug function.
- Operating temperature range includes -40°C ~ 105°C industrial tier.
- Available in QFN20 and TSSOP20 packages

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1 Introduction

1.1 Overview

The MG32F04A016 microcontrollers are based on Arm® Cortex®-M0 core. These devices have a maximum clocked frequency of 48MHz, built-in 16KB Flash storage, and contain an extensive range of peripherals and I/O ports. These devices contain one 12-bit ADC, one 16-bit advanced timer, one 16-bit general purpose timer and one 16-bit basic timer, as well as communication interfaces including two USART, one SPI and one I2C.

The operating voltage of this product series is 2.0V to 5.5V, and the operating temperature range (ambient temperature) is -40°C to 105°C extended industrial tier. Multiple sets of power-saving modes make the design of low-power applications possible.

The target applications of this product series include:

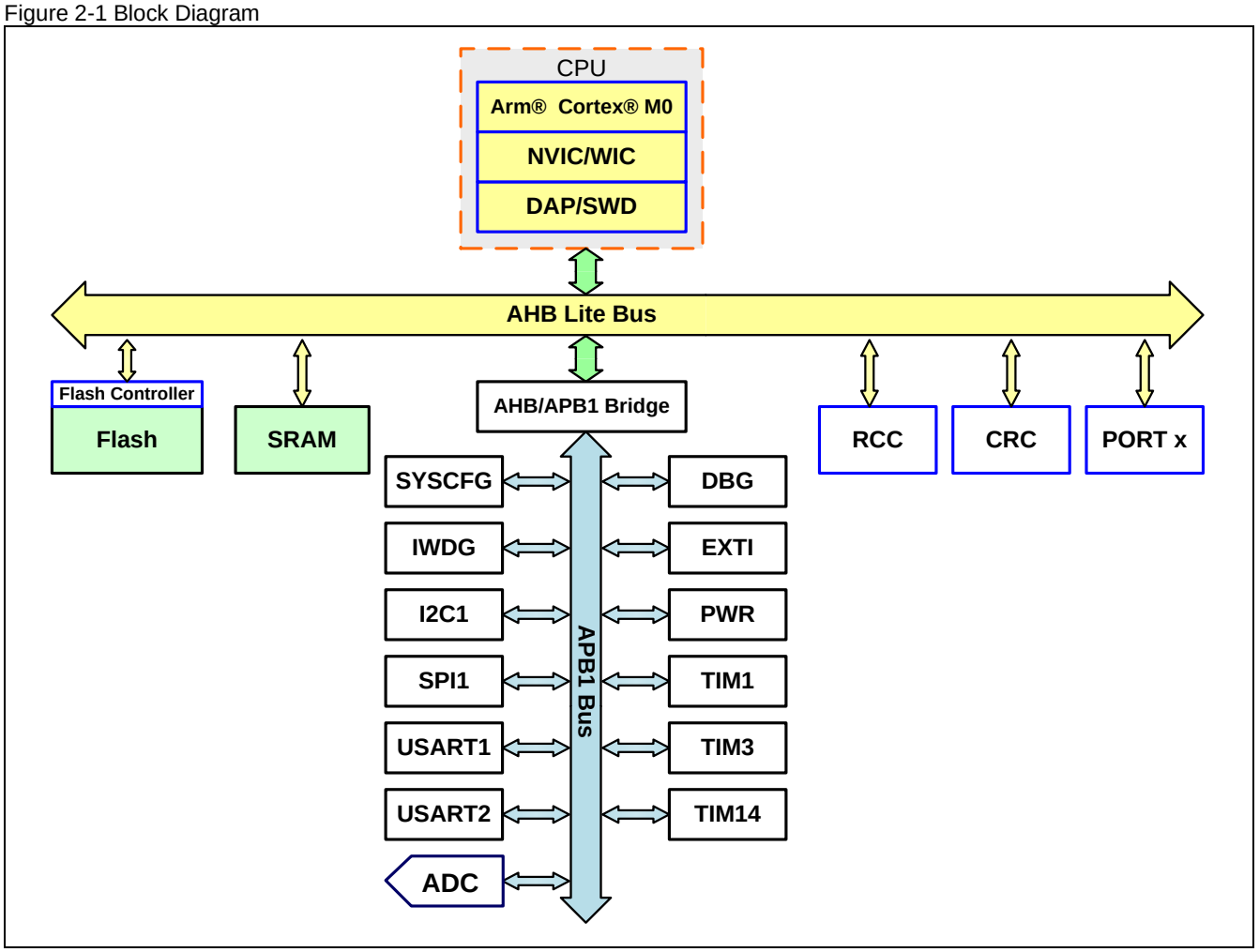
- Wireless charging
- Motor control
- Node control
- Toys
- Lighting circuit
- Fire-fighting devices

These devices are available in QFN20 and TSSOP20 packages.

2 Function Introduction

2.1 Block diagram

Figure 2-1 Block Diagram



2.2 Core introduction

The Arm® Cortex®-M0 processor provides real-time processing and advanced interrupt handling system, which is perfect for cost-effective and low-pin-count microcontrollers targeting real-time control and low power applications.

The Arm® Cortex®-M0 is a 32-bit RISC processor, provides state-of-the-art code efficiency, which is extremely suitable for small memory size microcontrollers and small code size applications.

With its embedded Arm core, this product is compatible with all the tools and software for Arm-based products.

2.3 Bus introduction

The bus matrix includes one AHB inter-connection bus matrix, one AHB bus and two AHB-to-APB bridges. The peripherals on the AHB bus (e.g., RCC, GPIO, CRC) are connected to the system bus through the inter-connection matrix. The data are transferred between AHB and APB bus using an AHB-to-APB bridge. When there's 8-bit or 16-bit access to APB registers, the APB bus will extend the access to 32-bit automatically.

2.4 Memory map

Table 2-1 Memory map

Bus	Address range	Size	Peripheral
Flash	0x00000000 - 0x00003FFF	16 KB	Mapped to Main Flash memory
	0x00004000 - 0x07FFFFFF	~127 MB	Reserved
	0x08000000 - 0x08003FFF	16 KB	Main Flash memory
	0x08000000 - 0x1FFDFFFF	~383 MB	Reserved
	0x1FFE0000 - 0x1FFE01FF	0.5 KB	Reserved
	0x1FFE0200 - 0x1FFE0FFF	3 KB	Reserved
	0x1FFE1000 - 0x1FFE1BFF	3 KB	Reserved
	0x1FFE1C00 - 0x1FFFF3FF	~256 MB	Reserved
	0x1FFFF400 - 0x1FFFF7FF	1 KB	System memory
	0x1FFFF800 - 0x1FFFF80F	16 B	Option bytes
	0x1FFFF810 - 0x1FFFFFFF	~2 KB	Reserved
SRAM	0x20000000 - 0x200007FF	2 KB	SRAM
	0x20000700 - 0x2FFFFFFF	~255 MB	Reserved
APB1	0x40000000 - 0x400003FF	1 KB	Reserved
	0x40000400 - 0x400007FF	1 KB	TIM3
	0x40000800 - 0x40000BFF	8 KB	Reserved
	0x40002800 - 0x40002BFF	1 KB	Reserved
	0x40002C00 - 0x40002FFF	1 KB	Reserved
	0x40003000 - 0x400033FF	1 KB	IWDG
	0x40003400 - 0x400037FF	1 KB	Reserved
	0x40003800 - 0x40003BFF	1 KB	Reserved
	0x40004000 - 0x400043FF	1 KB	Reserved
	0x40004400 - 0x400047FF	1 KB	USART2

Bus	Address range	Size	Peripheral
	0x40004800 - 0x40004BFF	3 KB	Reserved
	0x40005400 - 0x400057FF	1 KB	I2C1
	0x40005800 - 0x40006BFF	5 KB	Reserved
	0x40006C00 - 0x40006FFF	1 KB	Reserved
	0x40007000 - 0x400073FF	1 KB	PWR
	0x40007400 - 0x4000FFFF	35 KB	Reserved
	0x40010000 - 0x400103FF	1 KB	SYSCFG
	0x40010400 - 0x400107FF	1 KB	EXTI
	0x40010800 - 0x400123FF	7 KB	Reserved
	0x40012400 - 0x400127FF	1 KB	ADC1
	0x40012800 - 0x40012BFF	1 KB	Reserved
	0x40012C00 - 0x40012FFF	1 KB	TIM1
	0x40013000 - 0x400133FF	1 KB	SPI1
	0x40013400 - 0x400137FF	1 KB	DBGMCU
	0x40013800 - 0x40013BFF	1 KB	USART1
	0x40013C00 - 0x40013FFF	1 KB	Reserved
	0x40014000 - 0x400143FF	1 KB	TIM14
	0x40014400 - 0x400147FF	1 KB	Reserved
	0x40014800 - 0x40014BFF	1 KB	Reserved
	0x40014C00 - 0x40017FFF	13 KB	Reserved
AHB	0x40020000 - 0x400203FF	1 KB	Reserved
	0x40020400 - 0x40020FFF	3 KB	Reserved
	0x40021000 - 0x400213FF	1 KB	RCC
	0x40021400 - 0x40021FFF	3 KB	Reserved
	0x40022000 - 0x400223FF	1 KB	Flash Interface
	0x40022400 - 0x40022FFF	3 KB	Reserved
	0x40023000 - 0x400233FF	1 KB	CRC
	0x40023400 - 0x47FFFFFF	~127 MB	Reserved
	0x48000000 - 0x480003FF	1 KB	GPIOA
	0x48000400 - 0x480007FF	1 KB	GPIOB
	0x48000800 - 0x48000BFF	1 KB	Reserved
	0x48000C00 - 0x48000FFF	1 KB	Reserved
	0x48001000 - 0x5FFFFFFF	~384 MB	Reserved

2.1 Flash

This product provides up to 16KB embedded Flash memory available for storing code and data.

2.2 SRAM

This product provides up to 2KB embedded SRAM.

2.3 NVIC

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Cortex®-M0) and manage 4 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Allow early processing of interrupts.
- Support high priority interrupt preemption.
- Support interrupt tail-chaining.
- Automatically save processor status.
- Automatic restoration when the interrupt returns with no instruction overhead.

This module provides flexible interrupt management with minimal interrupt latency.

2.4 EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

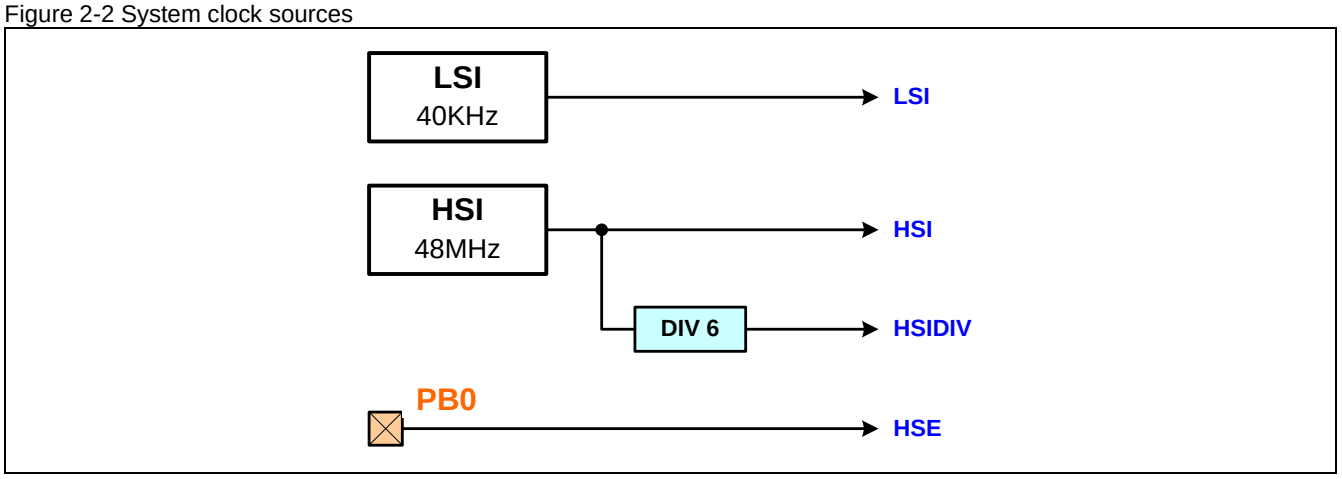
The EXTI can detect a pulse width shorter than the internal APB clock period.

2.5 Clock and boot

As shown in Figure 2-2, this product contains the following internal or external clock sources:

- HSI 48MHz
- LSI 40KHz
- HSE

Figure 2-2 System clock sources



The system clock can be selected from the following internal or external clocks:

- HSI – HSI 48MHz output
- HSIDIV – HSI 48MHz divide-by-6 output, i.e., 8MHz output
- LSI – LSI 40KHz output
- HSE – external clock input externally sourced from the OSC_IN (PB0) pin

The system clock is divided into CPU and AHB bus clocks, which operate at a maximum frequency of 48MHz. The maximum operating frequency of the APB bus is the same as that of the AHB bus.

After reset, HSIDIV (8MHz) is first used as the default system clock, followed by the option to use HSI, LSI, or HSE as the clock source. When an invalid external clock is detected, the system automatically masks the external clock source and uses the internal oscillator instead. In this case, if the relevant interrupt monitoring switch is enabled, a corresponding interrupt request is also generated.

2.6 Boot modes

Boot from embedded Flash.

2.7 Power supply schemes

- Power the I/O ports and internal voltage regulator via VDD pin, V_{DD} operates from 2.0V to 5.5V.
- There is no separate VDDA pin for this product, VDDA and VDD are connected inside the chip, VDDA powers the analog part of the ADC, reset module, oscillator and PLL, please refer to the Electrical Characteristics section for the specific operating voltage range of the analog modules.

2.8 Voltage regulator

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that used by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

2.9 Power supply supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enabled.

2.10 Low power mode

This product supports multiple low power modes, user can select the low power modes according to their application to achieve a balance between power consumption, wakeup time and wakeup source.

Sleep mode

In sleep mode, only the CPU clock is gated off. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

In stop mode, low power consumption can be achieved with all RAM and registers content in retention. In stop mode, HSI and HSE are powered off. The microcontroller can be woken up by the EXTI signals. EXTI signals can come from the 16 external I/O ports or PVD output.

Deep Stop mode

Similar as stop mode, but with lower power consumption.

The peripheral status in each low-power mode is shown in Table 2-2, please note:

- Power Down indicates that the module is powered off and all data except Flash is lost.
- Optional indicates that the peripheral can be turned on or off through software configuration.
- ON means work.
- OFF indicates that the function is turned off.
- Retention indicates that data is retained but not operational.

Table 2-2 Peripheral status in different power modes

Module/Mode	Run	Sleep	Stop	Deep Stop
Max. Freq.	48MHz	48MHz	40KHz	40KHz
PVD	Optional	Optional	Optional	Optional
POR	ON	ON	ON	ON
CPU	ON	OFF	OFF	OFF
SRAM	ON	ON	Retention	Retention
Flash	ON	Standby	Standby	Deep Standby
HSI	Optional	Optional	OFF	Power Down
LSI	Optional	Optional	Optional	Optional
IWDG	Optional	Optional	Optional	Optional
ADC	Optional	Optional	OFF	OFF
Other Peripherals	Optional	Optional	OFF	OFF
I/O	Optional	Optional	Retention	Retention

2.11 Timers and watchdogs

This product has one advanced timer, one general purpose timer, one basic timer, one watchdog timer and one Systick timer. The table below compares the features of advanced, general purpose and basic timers.

Table 2-3 Feature summary of advanced, general purpose and basic timers

Type	Instance	Resolution	Counter direction	pre-divider	DMA request	Capture/compare channels	Complementary output
Advanced	TIM1	16-bit	up, down, up/down	1 to 65536	No	4 (no capture)	3
General purpose	TIM3	16-bit	up, down, up/down	1 to 65536	No	4	No
Basic	TIM14	16-bit	up	1 to 65536	No	1	No

Advanced timer (TIM1)

The advanced timer includes a 16-bit counter, four capture/compare channels and three phases complementary PWM generator. This timer supports hardware dead-time insertion when using as complementary PWM generator. This timer can also be used as a full-function general purpose timer. This timer has four independent channels, each channel can be used for:

- Output compare
- PWM generator (center- or edge-aligned)
- Single pulse output

When this timer is used as a general-purpose timer, it has the same function as the TIM2. When this timer is used as a 16-bit PWM generator, it can be configured to a broad duty cycle range from 0% to 100%.

In debug mode, the counter can be frozen.

The advanced timer has lots of identical features and internal structures as the general-purpose timer, in this way the advanced timer can work together with the general-purpose timer through the link function, to provide synchronization and event trigger function.

General-purpose timer (TIM3)

This product has one general-purpose timer (TIM3). The timer has a 16-bit counter, support both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output. These general-purpose timers can also work together through the timer link function, to provide synchronization between timers and event trigger function.

These timers can also be used to decode incremental encoder signals and can also be used to decode one to four Hall sensors' digital output. Any general-purpose timer can be used to generate PWM output or work as basic timer.

In debug mode, the counter can be frozen.

Basic timer (TIM14)

This product has one 16-bit basic timer (TIM14). Each timer has one 16-bit counter, supporting only up counting, with automatically reload. The timer also has one 16-bit frequency pre-divider and one independent channel. Each channel can be used as input capture, output compare, PWM or one pulse mode output.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 40KHz oscillator. As it is independent of the main clock, it can run in shutdown and standby modes. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter can be frozen.

System tick timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a general down counter. It has the following features:

- 24-bit down counter
- Auto-reload capability
- A maskable interrupt can be generated when counter value is 0
- Programmable clock source

2.12 GPIO

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripherals function port. Most GPIO pins are shared with digital or analog functions.

If necessary, the peripheral functions of the I/O pins can be locked by specific operation to avoid accidental writing to the I/O register.

2.13 USART

This product has two Universal Synchronous/Asynchronous Receiver/Transmitter (USART) interfaces. The USART provides flexibility for full-duplex data exchange with peripherals using the industry standard NRZ asynchronous serial data format. This module can support a wide range of baud rates through the integrated baud rate generator (including integer and fraction settings). Support LSB or MSB receive/transmit mode.

Support 8- or 9-bit programmable data length. Support 0.5-/1-/1.5-/2-bit stop bit configuration. The USART can support synchronous or asynchronous one-way communication and half-duplex single-wire communication. Support maximum 6Mbps baud rate.

2.14 I2C

This product has one I2C interface. The I2C bus interface can work in multi-master mode or slave mode and supports standard mode (100Kbps) and fast mode (400Kbps). The I2C interface supports 7-bit or 10-bit addressing.

2.15 SPI

This product has one SPI interfaces. The SPI interface can be configured as 1 to 32 bits per frame in master or slave mode, allowing up to 24 Mbps in master mode and 12 Mbps in slave mode.

2.16 ADC

This product has one 12-bit analog/digital converter (ADC), support up to 1Msps conversion rate, with up to eight external channels and one internal channel available. Support single-shot single-cycle and continuous scan conversion. Support any sequence sampling mode, the sampling channels can be sequenced in any order. One internal channel is used to sample the built-in voltage reference, and in application the voltage level of the chip power supply can be derived from the sampled conversion value.

The analog watchdog function allows the application to monitor one or all selected channels. When the monitored signal exceeds a preset threshold, an interrupt will be generated.

The triggers generated by the general-purpose timers and the advanced timers can be selected to trigger the ADC sampling, in this way the ADC sampling can be synchronized with the timer.

2.17 CRC

The cyclic redundancy check (CRC) module uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. Among many applications, CRC is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a method to detect flash memory errors. The CRC module can be used to calculate the signature of the software package in real time and compare it with the signature generated when the software is linked and generated.

2.18 SWD

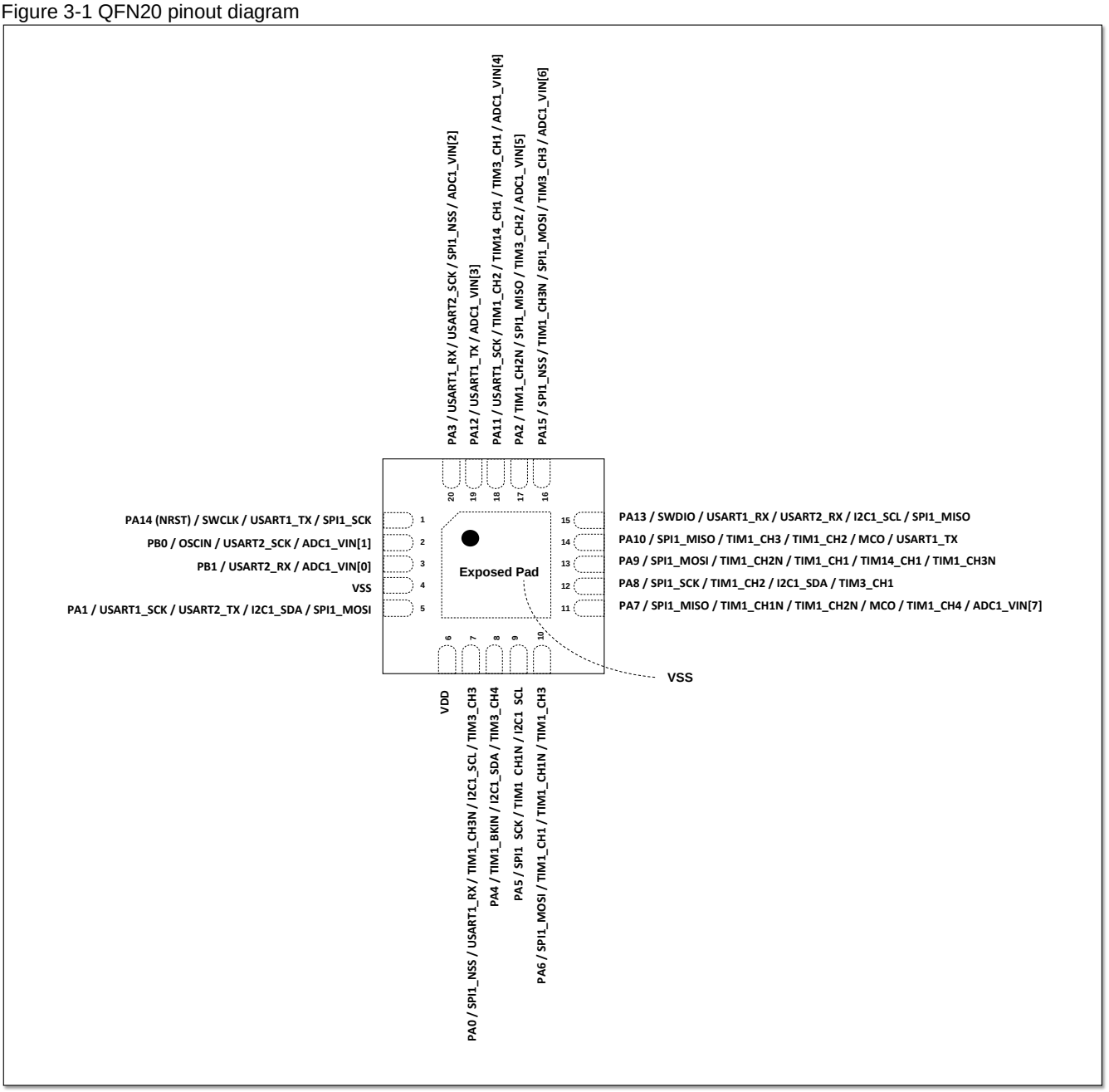
This product equips Arm standard Serial Wire Debug (SWD).

3 Pinout and assignment

3.1 Pinout diagram

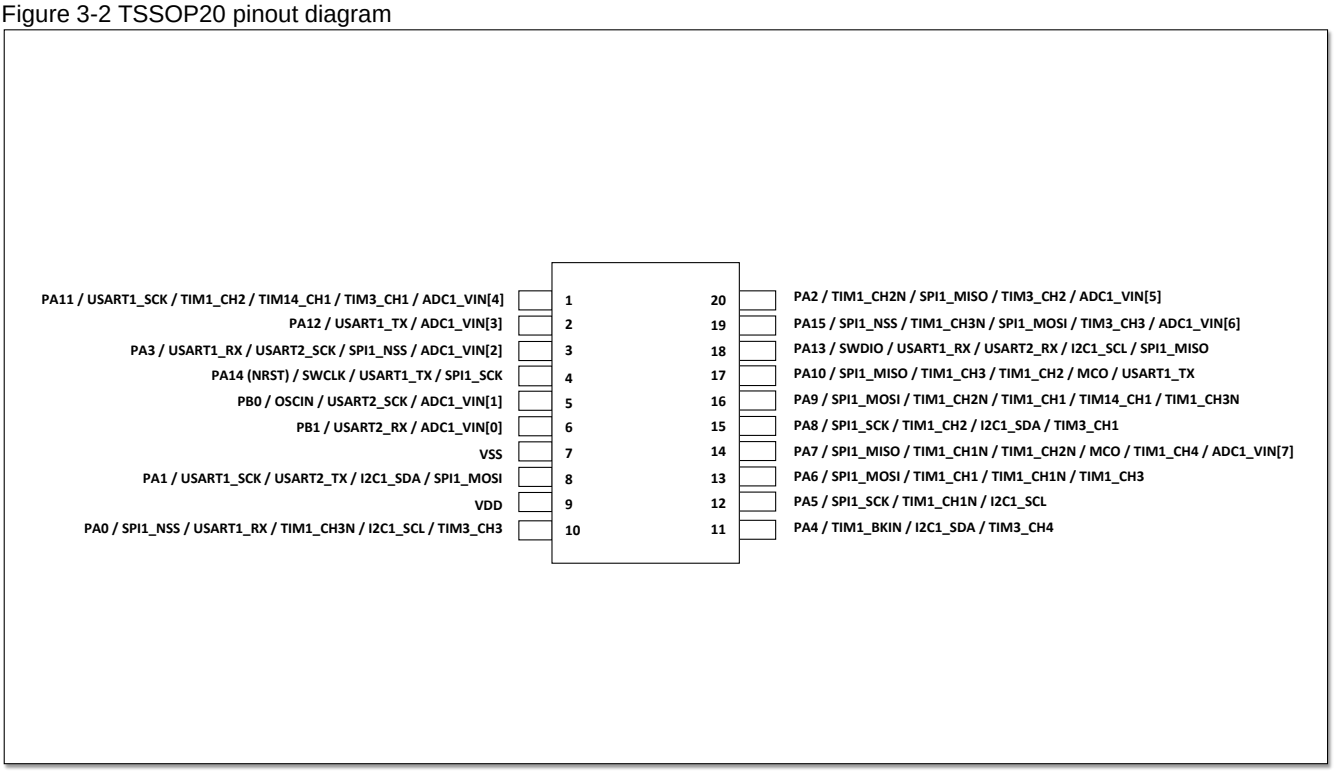
3.1.1 QFN20 pinout

Figure 3-1 QFN20 pinout diagram



3.1.1 TSSOP20 pinout

Figure 3-2 TSSOP20 pinout diagram



3.2 Pin assignment

Table 3-1 Pin assignment table

QFN20	TSSOP20	Name	Type (1)	I/O level (2)	Main function	Multiplex function	Additional function
1	4	PA14 (NRST) (3)	I/O	TC	PA14	SWCLK USART1_TX SPI1_SCK	-
2	5	PB0 OSCIN	I/O	TC	PB0	USART2_SCK	ADC1_VIN[1]
3	6	PB1	I/O	TC	PB1	USART2_RX	ADC1_VIN[0]
4	7	VSS	S	-	VSS	-	-
5	8	PA1	I/O	TC	PA1	USART1_SCK USART2_TX I2C1_SDA SPI1_MOSI	-
6	9	VDD	S	-	VDD	-	-
7	10	PA0	I/O	-	PA0	SPI1_NSS USART1_RX TIM1_CH3N I2C1_SCL TIM3_CH3	-
8	11	PA4	I/O	-	PA4	TIM1_BKIN I2C1_SDA TIM3_CH4	-
9	12	PA5	I/O	-	PA5	SPI1_SCK TIM1_CH1N I2C1_SCL	-
10	13	PA6	I/O	TC	PA6	SPI1_MOSI TIM1_CH1 TIM1_CH1N TIM1_CH3	-
11	14	PA7	I/O	TC	PA7	SPI1_MISO TIM1_CH1N TIM1_CH2N MCO TIM1_CH4	ADC1_VIN[7]
12	15	PA8	I/O	TC	PA8	SPI1_SCK TIM1_CH2 I2C1_SDA TIM3_CH1	-
13	16	PA9	I/O	TC	PA9	SPI1_MOSI TIM1_CH2N TIM1_CH1 TIM14_CH1 TIM1_CH3N	-
14	17	PA10	I/O	TC	PA10	SPI1_MISO TIM1_CH3 TIM1_CH2 MCO USART1_TX	-
15	18	PA13	I/O	TC	PA13	SWDIO USART1_RX USART2_RX I2C1_SCL SPI1_MISO	-
16	19	PA15	I/O	TC	PA15	SPI1_NSS TIM1_CH3N SPI1_MOSI TIM3_CH3	ADC1_VIN[6]
17	20	PA2	I/O	TC	PA2	TIM1_CH2N SPI1_MISO TIM3_CH2	ADC1_VIN[5]
18	1	PA11	I/O	TC	PA11	USART1_SCK TIM1_CH2 TIM14_CH1 TIM3_CH1	ADC1_VIN[4]

QFN20	TSSOP20	Name	Type (1)	I/O level (2)	Main function	Multiplex function	Additional function
19	2	PA12	I/O	TC	PA12	USART1_TX	ADC1_VIN[3]
20	3	PA3	I/O	TC	PA3	USART1_RX USART2_SCK SPI1_NSS	ADC1_VIN[2]

1. I = input, O = output, S = power pins, HiZ = high resistance state.
2. TC: standard IO. Input signal level should not exceed VDD.
3. When SFT_NRST_RMP bit of RCC_SYSCFG is set to 1, PA14 is mapped as an NRST external reset and should be held low for at least 4us for reliable reset.

3.3 Pin multiplexing

Table 3-2 PA port multiplexing AF0-AF4

Pin	AF0	AF1	AF2	AF3	AF4
PA0	SPI1_NSS	USART1_RX	TIM1_CH3N	I2C1_SCL	TIM3_CH3
PA1	-	USART1_SCK	USART2_TX	I2C1_SDA	SPI1_MOSI
PA2	-	-	TIM1_CH2N	SPI1_MISO	TIM3_CH2
PA3	-	USART1_RX	USART2_SCK	-	SPI1_NSS
PA4	-	-	TIM1_BKIN	I2C1_SDA	TIM3_CH4
PA5	SPI1_SCK	TIM1_CH1N	-	I2C1_SCL	-
PA6	SPI1_MOSI	TIM1_CH1	TIM1_CH1N	-	TIM1_CH3
PA7	SPI1_MISO	TIM1_CH1N	TIM1_CH2N	MCO	TIM1_CH4
PA8	SPI1_SCK	TIM1_CH2	-	I2C1_SDA	TIM3_CH1
PA9	SPI1_MOSI	TIM1_CH2N	TIM1_CH1	TIM14_CH1	TIM1_CH3N
PA10	SPI1_MISO	TIM1_CH3	TIM1_CH2	MCO	USART1_TX
PA11	-	USART1_SCK	TIM1_CH2	TIM14_CH1	TIM3_CH1
PA12	-	USART1_TX	-	-	-
PA13	SWDIO	USART1_RX	USART2_RX	I2C1_SCL	SPI1_MISO
PA14	SWCLK	USART1_TX	-	-	SPI1_SCK
PA15	SPI1_NSS	TIM1_CH3N	-	SPI1_MOSI	TIM3_CH3

Table 3-3 PB port multiplexing AF0-AF4

Pin	AF0	AF1	AF2	AF3	AF4
PB0	-	USART2_SCK	-	-	-
PB1	-	-	USART2_RX	-	-

4 Electrical Characteristics

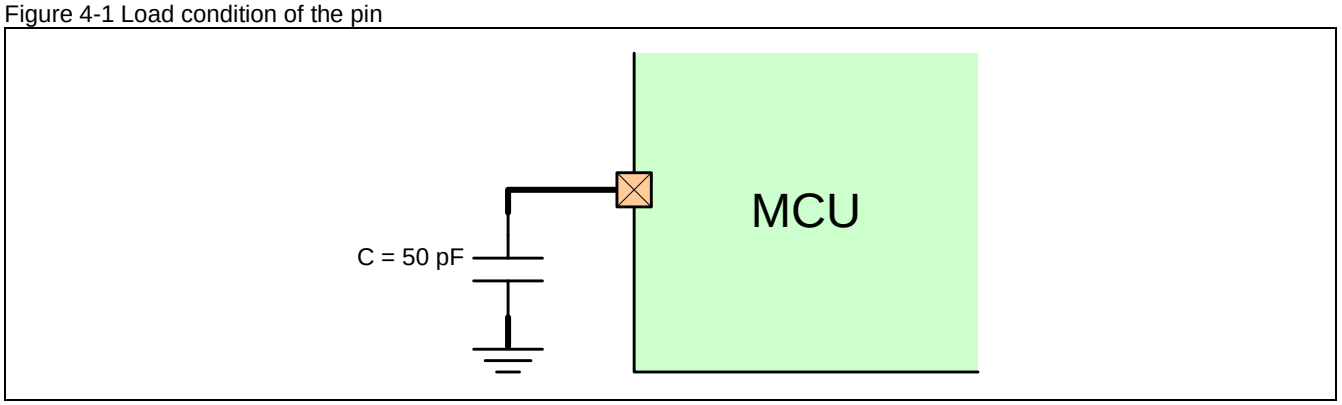
4.1 Test condition

All voltages are referenced to V_{SS} unless otherwise stated.

4.1.1 Load capacitance

The load conditions for pin parameters measurement are shown in the Figure 4-1.

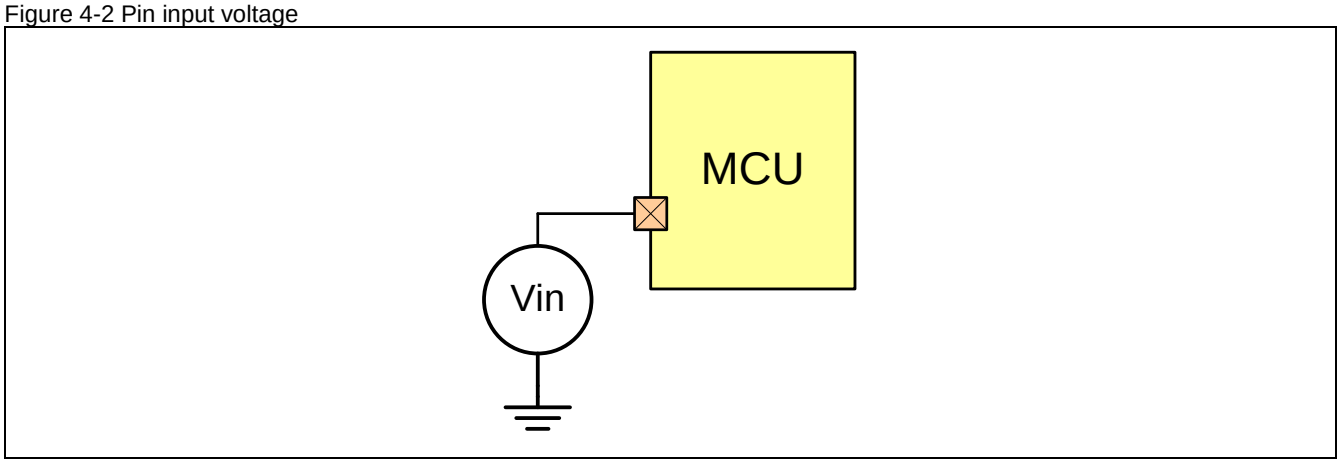
Figure 4-1 Load condition of the pin



4.1.2 I/O input voltage

The measurement of the input voltage on the pin is shown in Figure 4-2.

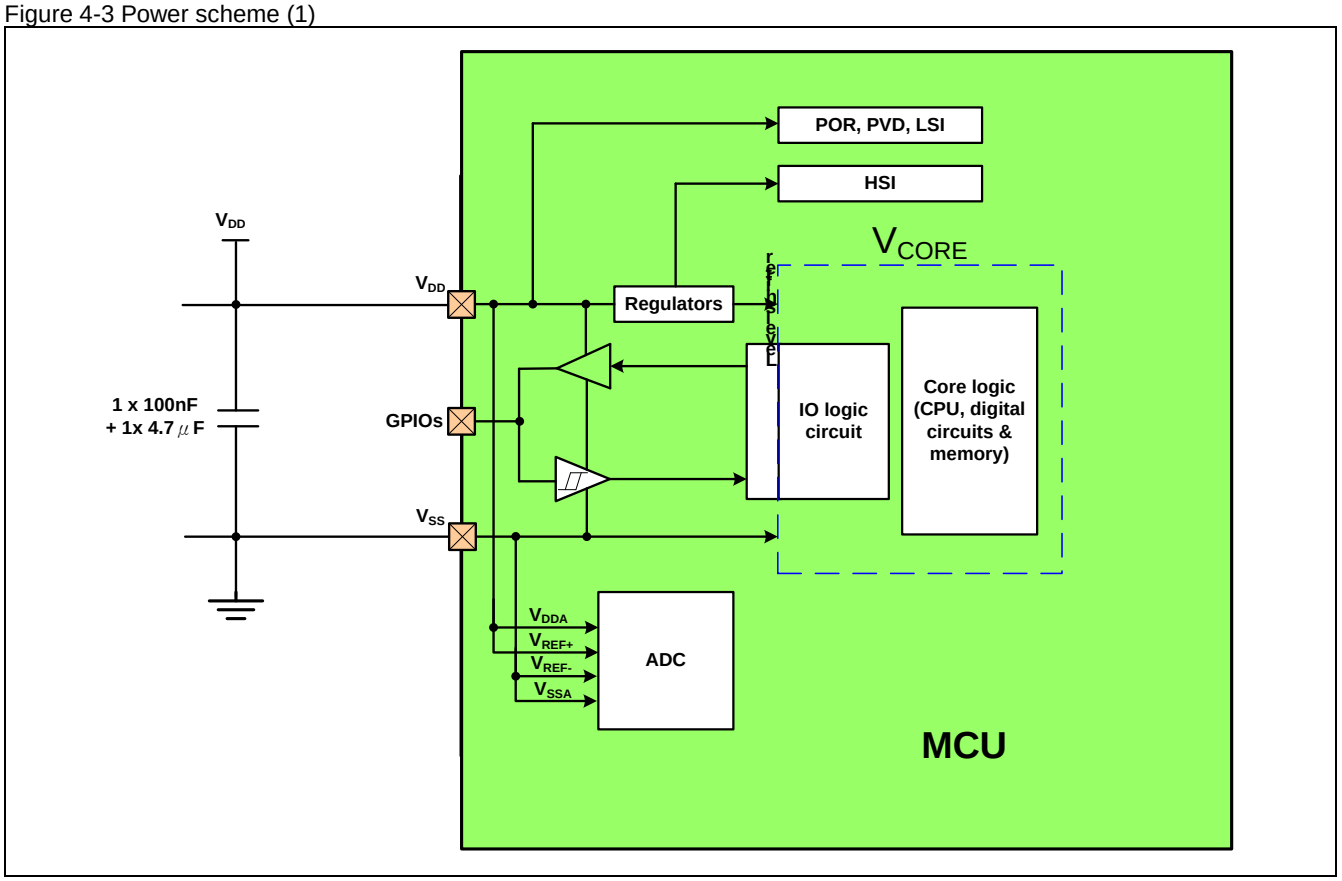
Figure 4-2 Pin input voltage



4.1.3 Power scheme

The power supply design scheme is shown in Figure 4-3.

Figure 4-3 Power scheme (1)



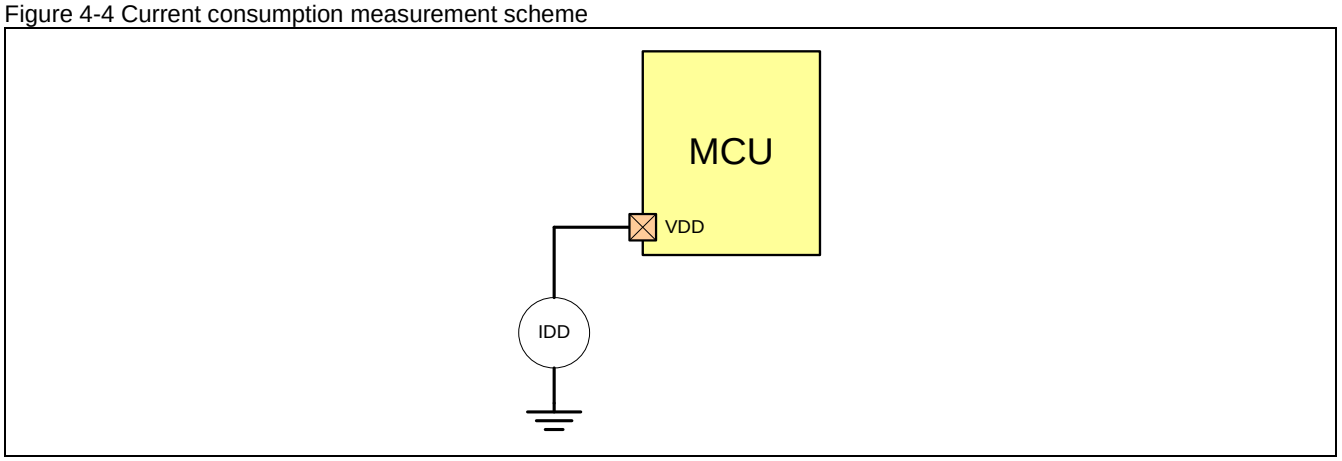
Notes:

1. For optimal chip performance, it is recommended to use the filtering ceramic capacitors shown in the figure above for decoupling between power pair (VDD, VSS)
2. For this product, the V_{DD}, V_{DDA}, and V_{REF+} are all connected to the VDD pin inside the chip, and V_{SS}, V_{SSA}, and V_{REF-} are all connected to the VSS pin inside the chip.

4.1.4 Current consumption measurement

The measurement of the current consumption on the pin is shown in Figure 4-4.

Figure 4-4 Current consumption measurement scheme



4.2 Absolute maximum rating

Stresses above the absolute maximum ratings given in "Absolute Group Maximum Ratings" list (Table 4-1, Table 4-2) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Voltage characteristics

Symbol	Description	Minimum	Maximum	Unit
V_{DDx}-V_{SSx}	External main supply voltage (including V_{DDA} and V_{SSA}) (1)	-0.3	5.8	V
V_{IN} (2)	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	

1. All power (VDD) and ground (VSS) pins must always be connected to the external power supply system within the permitted range.
2. The maximum value of V_{IN} must be respected. Refer to the table below for the maximum allowed injected current values.

Table 4-2 Current characteristics

Symbol	Description	Maximum	Unit
$I_{VDD/VDDA}$ (1)	Total current through V_{DD}/V_{DDA} power pins (supply current) (1)	+60	mA
$I_{VSS/VSSA}$ (1)	Total current through V_{SS}/V_{SSA} ground pins (outflow current) (1)	-60	
I_{IO}	Output sink current on any I/O and control pins, V_{DD} = 5.0V	+20	
	Output source current on any I/O and control pins, V_{DD} = 5.0V	-20	
	Output sink current on any I/O and control pins, V_{DD} = 3.3V	+15	
	Output source current on any I/O and control pins, V_{DD} = 3.3V	-15	
	Output sink current on any I/O and control pins, V_{DD} = 2.0V	+6	
	Output source current on any I/O and control pins, V_{DD} = 2.0V	-6	
$I_{INJ(PIN)}$ (2)(3)	NRST pin injection current	±5	
	HSE OSC_IN pin injection current	±5	
$\sum I_{INJ(PIN)}$ (5)	Other pins injection current (4)	±25	

1. All main power (V_{DD}) and ground (V_{SS}) pins must always be connected to an external power supply in the permitted range.
2. This current consumption must be correctly distributed to all I/O and control pins.
3. The reverse injection current can interfere with the analog performance of the device.
4. When $V_{IN} > V_{DDA}$, a positive injected current is generated; when $V_{IN} < V_{SS}$, a reverse injected current is generated. Do not exceed $I_{INJ(PIN)}$.
5. When there is simultaneous injection current for multiple inputs, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse injection current (instantaneous value).

4.3 Operating conditions

4.3.1 General operating conditions

Table 4-3 General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	-	48	
V_{DD}	Digital circuit operating voltage	All power modes except Standby mode	1.8	3.3	5.5	V
V_{DD}	Digital circuit operating voltage	Standby mode	2.0	3.3	5.5	
V_{DDA}	Analog circuit operating voltage (Performance is guaranteed)	Must be the same as V_{DD} (1)	2.5	3.3	5.5	
	Analog circuit operating voltage (Performance is not guaranteed)		1.8	-	2.5	
P_D	Power dissipation (2)	QFN20	-	-	196	mW
T_A	Ambient temperature (Extended industrial level)	-	-40	-	105	
T_J	Junction temperature (3) (Extended industrial level)	-	-40	-	125	

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}, the maximum permissible difference between V_{DD} and V_{DDA} is 300mV during power up and normal operation.
2. If T_A is low, higher P_D values are allowed if T_J does not exceed T_{Jmax}.
3. In low power dissipation state, T_A can be extended to this range if T_J does not exceed T_{Jmax}.

4.3.2 Operating conditions at power-up/power-down

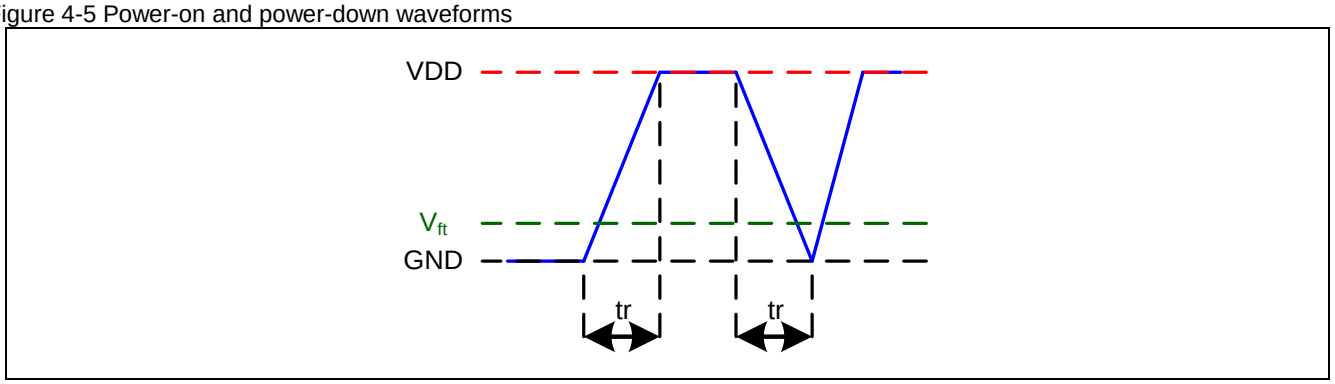
The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 4-3.

Table 4-4 Operating conditions at power-up/power-down

Symbol	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time t_r	0.2	-	∞	us/V
	V_{DD} fall time t_f	60	-	∞	
V_{ft} (3)	Power-down threshold voltage	-	0	-	mV

1. Data based on characterization results, not tested in production.
2. The V_{DD} waveforms of chip power-on and power-down must strictly follow the t_r and t_f phased in the following waveform diagram, and no power-down is allowed during power-on process.
3. Note: To ensure the reliability of chip power-on, all power-on should start from 0V.

Figure 4-5 Power-on and power-down waveforms



4.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 4-3.

Table 4-5 Embedded reset and power control block characteristics

Symbol	Parameter	Condition	Min. (3)	Typ.	Max. (3)	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3:0]=0000 (Rising edge)	-	1.8	-	V
		PLS[3:0]=0000 (Falling edge)	-	1.7	-	
		PLS[3:0]=0001 (Rising edge)	-	2.1	-	
		PLS[3:0]=0001 (Falling edge)	-	2.0	-	
		PLS[3:0]=0010 (Rising edge)	-	2.4	-	
		PLS[3:0]=0010 (Falling edge)	-	2.3	-	
		PLS[3:0]=0011 (Rising edge)	-	2.7	-	
		PLS[3:0]=0011 (Falling edge)	-	2.6	-	
		PLS[3:0]=0100 (Rising edge)	-	3.0	-	
		PLS[3:0]=0100 (Falling edge)	-	2.9	-	
		PLS[3:0]=0101 (Rising edge)	-	3.3	-	
		PLS[3:0]=0101 (Falling edge)	-	3.2	-	
		PLS[3:0]=0110 (Rising edge)	-	3.6	-	
		PLS[3:0]=0110 (Falling edge)	-	3.5	-	
		PLS[3:0]=0111 (Rising edge)	-	3.9	-	
		PLS[3:0]=0111 (Falling edge)	-	3.8	-	
		PLS[3:0]=1000 (Rising edge)	-	4.2	-	
		PLS[3:0]=1000 (Falling edge)	-	4.1	-	
		PLS[3:0]=1001 (Rising edge)	-	4.5	-	
		PLS[3:0]=1001 (Falling edge)	-	4.4	-	
		PLS[3:0]=1010 (Rising edge)	-	4.8	-	
		PLS[3:0]=1010 (Falling edge)	-	4.7	-	
$V_{POR/PDR}$ (1)	Power-on reset threshold	-	-	1.65	-	V
V_{hyst_PDR}	PDR hysteresis	-	-	50	-	mV
$T_{RSTTEMPO}$ (2)	Reset duration	-	-	4.7	-	ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.
3. Drawn from comprehensive evaluation.

Note: The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction

4.3.4 Built-in voltage reference

The parameters given in the table below are provided under the ambient temperature and the V_{DD} supply voltage listed in Table 4-3.

Table 4-6 Build-in voltage reference

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Built-in voltage reference	-40°C < T_A < 105°C	-	1.2	-	V
$T_{s\_vrefint}$ (1)	ADC sampling time when readout build-in voltage reference	-	-	11.8	-	us

1. The sampling time is obtained through multiple tests

4.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and connected to a static level - V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting cycle, 24 ~ 48 MHz is 1 waiting cycle).
- The instruction prefetching function is on. When the peripherals are enabled: f_{PCLK1} = f_{HCLK}.

Note: The instruction prefetching function must be set before setting the clock and bus divider.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 4-3.

Table 4-7 Typical current consumption in Run mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled						Typical All peripherals disabled						Unit
				-40°C	0°C	25°C	55°C	85°C	105°C	-40℃	0℃	25℃	55℃	85℃	105℃	
I_{DD}	Supply current in Run mode	HSI is clock source	48M	4.22	4.36	4.43	4.54	4.63	4.70	3.06	3.19	3.25	3.35	3.44	3.51	mA
			24M	3.05	3.16	3.23	3.31	3.39	3.44	2.34	2.45	2.50	2.58	2.66	-	
			12M	2.15	2.27	2.32	2.40	2.46	2.49	1.81	1.91	1.96	2.04	2.09	-	
			6M	1.70	1.79	1.85	1.92	2.00	2.04	1.53	1.62	1.67	1.74	1.82	1.87	
			3M	1.22	1.30	1.35	1.42	1.48	1.52	1.13	1.21	1.26	1.33	1.39	1.43	
			750K	0.87	0.94	0.98	1.04	1.10	1.13	0.84	0.91	0.95	1.01	1.07	1.10	
			375K	0.80	0.87	0.91	0.97	1.03	1.06	0.79	0.86	0.90	0.96	1.02	1.05	
			187.5K	0.77	0.84	0.88	0.94	1.00	1.03	0.77	0.84	0.88	0.93	0.99	1.02	

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled						Typical All peripherals disabled						Unit
				-40°C	0°C	25°C	55°C	85°C	105°C	-40°C	0°C	25°C	55°C	85°C	105°C	
			93.75K	0.76	0.83	0.87	0.92	0.98	1.01	0.75	0.83	0.86	0.92	0.98	1.01	
		HSIDIV is clock source	8M	1.83	1.92	1.70	1.78	1.84	1.88	1.63	1.73	1.50	1.57	1.64	1.68	
			4M	1.68	1.76	1.79	1.51	1.57	1.61	1.56	1.65	1.65	1.39	1.45	1.49	
			2M	1.19	1.28	1.32	1.39	1.46	1.50	1.13	1.22	1.27	1.33	1.40	1.44	
			1M	0.95	1.03	1.07	1.13	1.19	1.23	0.92	1.00	1.04	1.10	1.16	1.20	
			500K	0.83	0.90	0.94	1.00	1.06	1.09	0.81	0.89	0.93	0.99	1.04	1.08	
			125K	0.74	0.81	0.85	0.91	0.96	0.99	0.73	0.80	0.84	0.90	0.96	0.99	
			62.5K	0.72	0.79	0.83	0.89	0.94	0.97	0.72	0.79	0.83	0.89	0.94	0.97	
			31.25K	0.71	0.78	0.82	0.88	0.93	0.97	0.71	0.78	0.82	0.88	0.93	0.96	
		LSI is clock source	40K	0.19	0.21	0.21	0.22	0.23	0.24	0.19	0.20	0.21	0.22	0.23	0.23	

Table 4-8 Typical current consumption in Sleep mode

Symbol	Parameters	Condition	f_{HCLK} (Hz)	Typical All peripherals enabled						Typical All peripherals disabled						Unit
				-40°C	0°C	25°C	55°C	85°C	105°C	-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DD}	Supply current in Sleep mode	HSI is clock source	48M	3.24	3.35	3.41	3.50	3.58	3.61	2.09	2.18	2.24	2.32	2.40	2.43	mA
			24M	2.18	2.27	2.33	2.40	2.48	2.52	1.49	1.57	1.62	1.69	1.76	1.80	
			12M	1.51	1.59	1.64	1.71	1.78	1.81	1.16	1.24	1.29	1.35	1.42	1.46	
			6M	1.67	1.76	1.81	1.89	1.97	2.01	1.50	1.58	1.64	1.71	1.78	1.82	
			3M	1.20	1.29	1.33	1.39	1.46	1.50	1.12	1.20	1.24	1.31	1.37	1.41	
			750K	0.86	0.94	0.98	1.04	1.10	1.13	0.84	0.91	0.95	1.01	1.07	1.10	
			375K	0.80	0.87	0.91	0.97	1.03	1.06	0.79	0.86	0.90	0.96	1.02	1.05	
			187.5K	0.77	0.84	0.88	0.94	0.99	1.03	0.76	0.84	0.88	0.93	0.99	1.02	
			93.75K	0.76	0.83	0.87	0.92	0.98	1.01	0.75	0.82	0.86	0.92	0.98	1.01	
		HSIDIV is clock source	8M	1.30	1.39	1.44	1.51	1.58	1.61	1.11	1.20	1.24	1.31	1.38	1.42	
			4M	1.75	1.81	1.26	1.26	1.33	1.36	1.63	1.69	1.11	1.15	1.21	1.24	
			2M	1.23	1.32	1.37	1.44	1.50	1.54	1.18	1.26	1.31	1.39	1.44	1.48	
			1M	0.97	1.05	1.09	1.15	1.21	1.25	0.94	1.02	1.06	1.12	1.19	1.23	
			500K	0.84	0.91	0.95	1.01	1.07	1.11	0.82	0.89	0.94	1.00	1.06	1.09	
			125K	0.74	0.81	0.85	0.91	0.96	0.99	0.73	0.80	0.84	0.90	0.96	0.99	
			62.5K	0.72	0.79	0.83	0.89	0.94	0.98	0.72	0.79	0.83	0.89	0.94	0.97	
			31.25K	0.71	0.78	0.82	0.88	0.93	0.97	0.71	0.78	0.82	0.88	0.93	0.97	
		LSI is clock source	40K	0.19	0.21	0.21	0.22	0.23	0.24	0.19	0.20	0.21	0.22	0.23	0.24	

Table 4-9 Typical current consumption in stop mode (1)

Symbol	Parameter	Conditions	Typical						Unit
			-40°C	0°C	25°C	55°C	85°C	105°C	
I_{DD}	Supply current in Stop mode	Enter Stop mode after reset, V_{DD}=3.3V	110.19	117.98	121.73	125.54	113.52	118.95	μA

Symbol	Parameter	Conditions	Typical						Unit
			-40℃	0℃	25℃	55℃	85℃	105℃	
	Supply current in Deep Stop mode	Enter Deep Stop mode after reset, V_{DD}=3.3V	5.75	6.20	6.44	6.79	7.76	9.31	

1. The I/O state is an analog input.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode and connected to a static level - V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise specified.
- The given value is calculated by measuring the current consumption.
  - When all peripherals are clocked off
  - When only one peripheral is clocked on
- Ambient operating temperature and V_{DD} supply voltage conditions are listed in Table 4-3.

Table 4-10 On-chip peripheral current consumption (1)

Symbol	Parameter	Bus	Typical	Unit
I_{DD}	CRC	AHB	0.67	uA/MHz
	GPIOA		0.32	
	GPIOB		0.27	
	TIM1	APB1	5.11	
	I2C1		4.95	
	SPI1		3.38	
	TIM3		3.13	
	USART1		1.96	
	USART2		1.93	
	TIM14		1.50	
	ADC1		0.73	
	PWR		0.10	
	EXTI		0.09	
	SYSCFG		0.09	
	DBG		0.04	
	WWDG		0.03	

1. f_{HCLK} = 48MHz，f_{APB1} = f_{HCLK}, the prescale coefficient of each peripheral is the default value.

Wake up time from low power mode

The wake-up time listed in the table below is measured during the wake-up process of the internal clock HSI. The clock source used to wake up the chip depends on the current operating mode:

Stop or Standby mode: the clock source is the oscillator

Sleep mode: the clock source is the clock used when entering the Sleep mode.

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 4-3.

Table 4-11 Wake up time from low power mode

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wake up from Sleep mode	System clock is HSIDIV	3.22	μs
t_{WUSTOP}	Wake up from Stop mode	System clock is HSIDIV	26.65	μs
$t_{WUDEEPSTOP}$	Wake up from Deep Stop mode	System clock is HSIDIV	28.88	μs

4.3.6 External clock source characteristics

High-speed external user clock generated from an external source

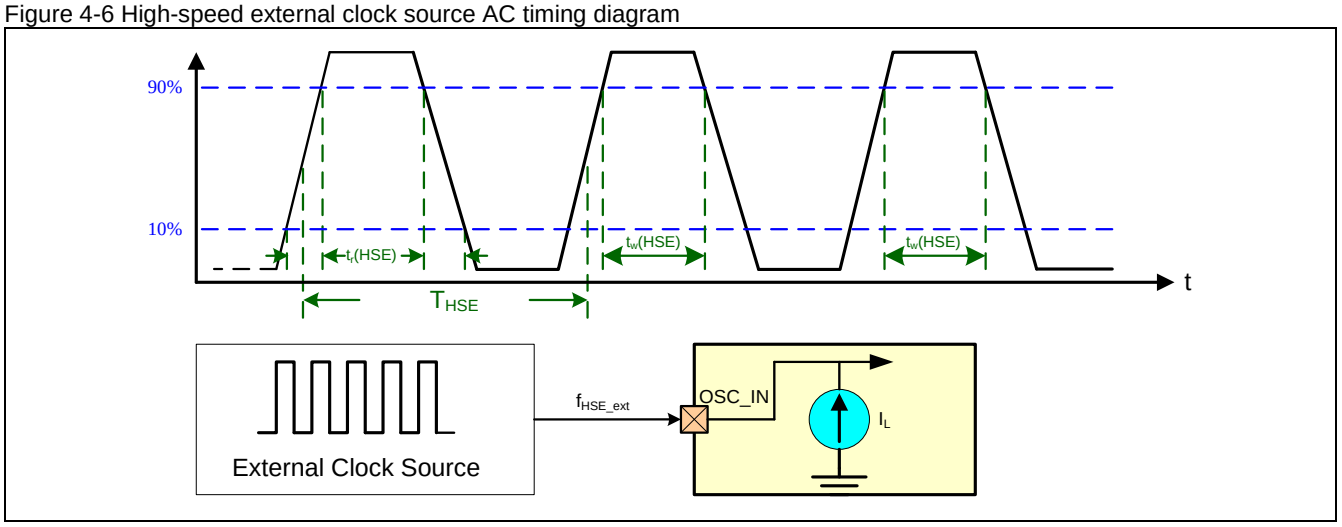
The characteristic parameters given in the following table are measured by a high-speed external clock source, and the ambient temperature and power supply voltage meet General operating conditions.

Table 4-12 High-speed external user clock characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock source frequency (1)	-	-	8	48	MHz
V_{HSEH}	OSC_IN input high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time (1)	-	20	-	-	ns

1. Guaranteed by design, not tested in production

Figure 4-6 High-speed external clock source AC timing diagram



4.3.7 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 4-13 HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
ACC_{HSI} (3)	HSI oscillator deviation	T_A = 0°C ~ 55°C	-1	-	1	%
		T_A = -40°C ~ 105°C	-2	-	2	%
$T_{stab(HSI)}$ (2)	HSI oscillator startup time	-	-	-	20	μs
$I_{DD(HSI)}$ (2)	HSI oscillator power consumption	-	-	480	-	μA

1. V_{DD} = 3.3V, TA = - 40°C ~ 105°C, unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Drawn from comprehensive evaluation.

Low-speed internal (LSI) oscillator

Table 4-14 LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	-	-	40	-	KHz
ACC_{LSI} (3)	LSI oscillator deviation	T_A = 0°C ~ 55°C	-15	-	15	%
		T_A = -40°C ~ 105°C	-20	-	20	%
$T_{stab(LSI)}$ (2)	LSI oscillator startup time	-	-	-	100	μs
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	-	-	1	-	μA

1. V_{DD} = 3.3V, T_A = -40°C ~ 105°C, unless otherwise stated.
2. Guaranteed by design, not tested in production.
3. Drawn from comprehensive evaluation.

4.3.8 Memory characteristics

Table 4-15 Flash memory characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{prog}	16-bit programming time	-	-	37.24	-	μs
t_{ERASE}	Page (1024 bytes) erase time	-	4	-	6	ms
t_{ME}	Mass erase time	-	30	-	40	ms
I_{DD}	Supply current	Read mode	-	-	1.5	mA
		Write mode	-	-	2	mA
		Erase mode	-	-	1	mA

Table 4-16 Flash memory endurance and data retention (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{END}	Endurance	T_A = 105°C	100000	-	-	Cycles
T_{DR}	Data retention	T_A = 25°C	25	-	-	Years

4.3.9 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the following table.

Table 4-17 EMS characteristics

Symbol	Parameter	Conditions	Level/Type
V_{FESD}	Voltage limit applied to any I/O pin, resulting in malfunction	V_{DD} = 3.3V, T_A = +25℃, f_{HCLK} = 48MHz. Conforming to IEC61000-4-2	2A
V_{FEFT}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	V_{DD} = 3.3V， T_A = +25℃, f_{HCLK} = 48MHz. Conforming to IEC61000-4-4	2A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software.

Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for this application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

4.3.10 Functional EMS (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Static latch-up

Two complementary static latch-up tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output, and configurable I/O pin

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 4-18 ESD & LU characteristics

Symbol	Parameter	Conditions	Class	Maximum	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to ESDA/JEDEC JS-001-2017	3A	±5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = 25°C, conforming to ESDA/JEDEC JS-002-2018	C3	±2000	V
I_{LU}	Latch-up current	T_A = 105°C, conforming to JESD78E	II, A	±300	mA

4.3.11 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 4-3 are used for tests. All I/O ports are CMOS compatible.

Table 4-19 I/O static characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low level input voltage	-	-	-	0.3 * V_{DD}	V
V_{IH}	High level input voltage	-	0.7 * V_{DD}	-	-	V
V_{hy}	Schmitt trigger hysteresis (1)	-	0.1 * V_{DD}	-	-	V
I_{lkg}	Input leakage current (2)	-	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor (3)	V_{IN} = V_{SS}	-	60	-	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)	V_{IN} = V_{DD}	-	60	-	kΩ
C_{IO}	I/O pin capacitance	-	-	-	10	pF

1. Drawn from comprehensive evaluation, not tested in production.
2. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are poly resistors.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

In the user application, the number of I/O pins must ensure that the drive current must be limited to respect the absolute maximum rating specified in Table 4-1:

- The sum of the currents sourced by all the I/O pins on V_{DD}, plus the maximum operating current that the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are provided under the ambient temperature and VDD supply voltage in accordance with the conditions summarized in Table 4-3. All I/O ports are CMOS compatible.

Table 4-20 Output voltage static characteristics

Symbol	Parameter	Conditions	Typical	Unit
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA，V_{DD}=2.0V	0.36	V
V_{OH} (2)	Output high voltage		1.56	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA，V_{DD}=3.3V	0.2	
V_{OH} (2)	Output high voltage		3.01	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 8mA，V_{DD} =3.3V	0.27	
V_{OH} (2)	Output high voltage		2.91	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 6mA，V_{DD}=5.0V	0.15	
V_{OH} (2)	Output high voltage		4.75	
V_{OL} (1)	Output low voltage	$\|I_{IO}\|$= 8mA，V_{DD} =5.0V	0.2	
V_{OH} (2)	Output high voltage		4.67	
V_{OL} (2)	Output low voltage	$\|I_{IO}\|$=20mA，V_{DD} =5.0V	0.54	
V_{OH} (2)	Output high voltage		4.18	

1. The current I_{IO} drawn by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VSS}.
2. The current I_{IO} output by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VDD}.
3. Resulted from comprehensive evaluation.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in the following figure and table, respectively.

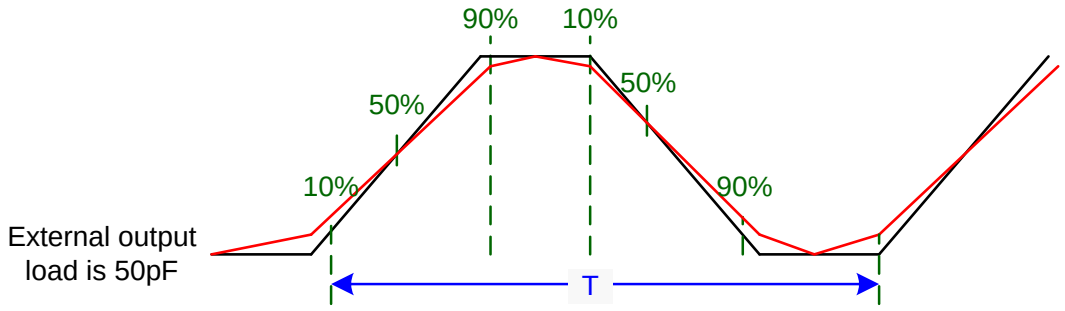
Unless otherwise stated, the parameters listed in the following table are provided under the ambient temperature and supply voltage in accordance with the condition Table 4-3.

Table 4-21 I/O AC characteristics (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
$t_{f(IO)out}$	Output fall time	C_L = 50pF V_{DD}=3.3V	5.8	ns
$t_{r(IO)out}$	Output rise time		5.6	ns

1. The maximum frequency is defined in Figure 4-7.
2. Guaranteed by design, not tested in production.

Figure 4-7 I/O AC characteristics



If ((tr+tf)≦2/3)T, and duty cycle is (45 ~ 55%)
when load is 50pF, can achieve maximum efficiency

4.3.12 Timer characteristics

The parameters listed in the following table are guaranteed by design.

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see section 4.3.6 I/O port characteristics.

Table 4-22 TIMx (1) characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{res(TIM)}$	Timer resolution	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	20.8	-	ns
f_{EXT}	External clock frequency of channel 1 to 4	-	0	-	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0208	1365.3	us
t_{MAX_COUNT}	Maximum possible counter value (TIM_PSC adjustable)	-	-	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	-	1365.3	us
t_{MAX_IN}	TIM maximum input frequency	-	-	48	MHz

1. Guaranteed by design, not tested in production.

4.3.13 I2C interface characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and supply voltage conditions summarized in Table 4-3.

The I2C interface conforms to the standard I2C communication protocol but has the following limitations: SDA and SCL are not true open-drain pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} is disabled, but still present.

The I2C characteristics are listed in the following table. Refer to section 4.3.6 I/O port characteristics for details on the characteristics of input/output alternate function pins (SDA and SCL).

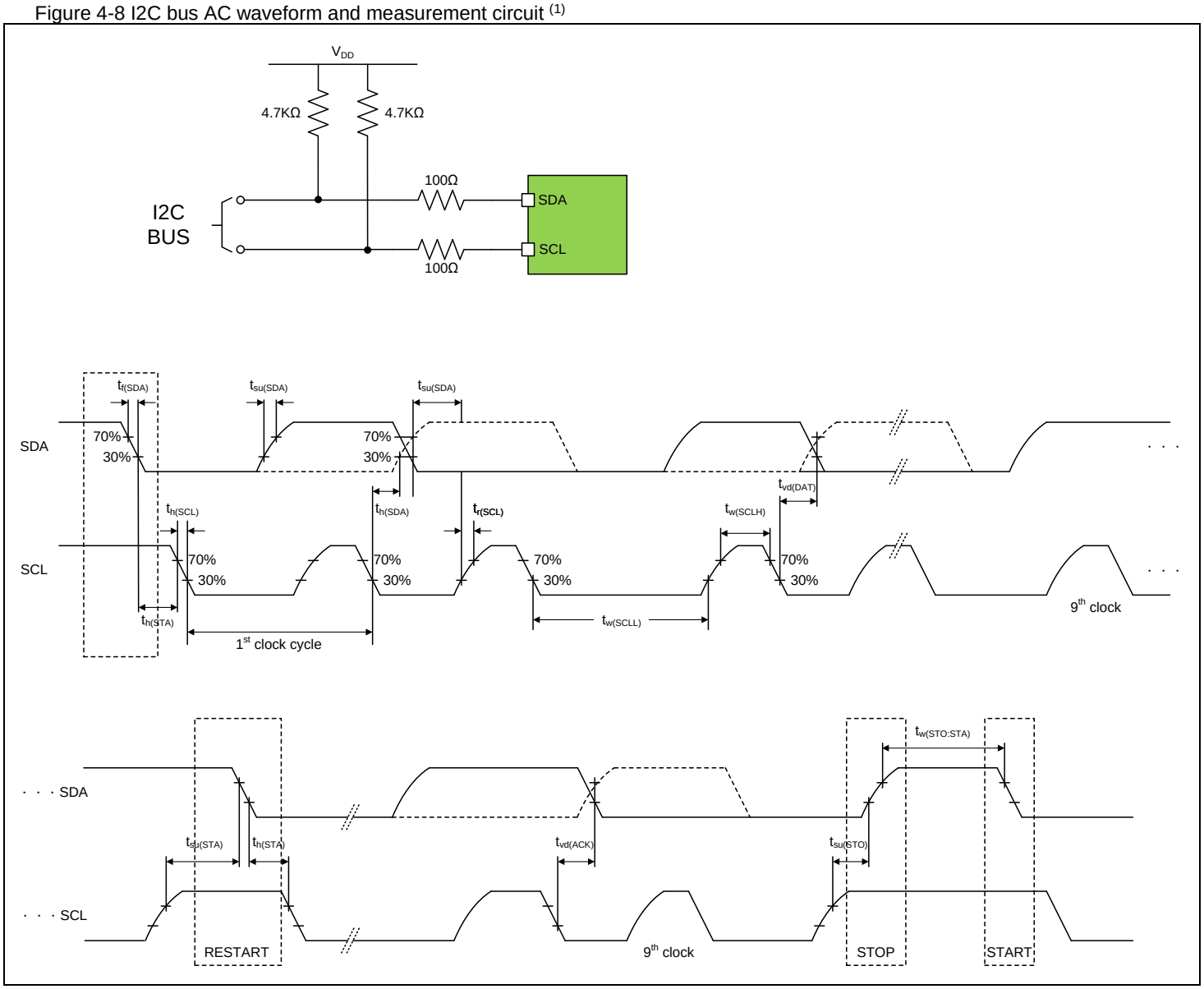
Table 4-23 I2C characteristics

Symbol	Parameter	Standard I2C (1)		Fast mode I2C (1)		Unit
		Minimum	Maximum	Minimum	Maximum	
$t_{w(SCLL)}$	SCL clock low time	9*t_{PCLK}	-	9*t_{PCLK}	-	us
$t_{w(SCLH)}$	SCL clock high time	18*t_{PCLK}	-	18*t_{PCLK}	-	us
$t_{su(SDA)}$	SDA setup time	1*t_{PCLK}	-	1*t_{PCLK}	-	ns
$t_{h(SDA)}$	SDA data retention time	0 (3)	- (4)	0 (3)	- (4)	ns
$t_{r(SDA)}$/ $t_{r(SCL)}$	SDA and SCL rising time	-	1000	20	300	ns
$t_{f(SDA)}$ /$t_{f(SCL)}$	SDA and SCL fall time	-	300	20×(V_{DD}/5.5V)	300	ns
$t_{vd(DAT)}$ (5)	Data valid time	-	8*t_{PCLK} – 1 (4)	-	8*t_{PCLK} - 0.3 (4)	us
$t_{vd(ACK)}$ (6)	Data valid acknowledge time	-	8*t_{PCLK} – 1 (4)	-	8*t_{PCLK} - 0.3 (4)	us
$t_{h(STA)}$	Start condition hold time	8*t_{PCLK}	-	8*t_{PCLK}	-	us

Symbol	Parameter	Standard I2C (1)		Fast mode I2C (1)		Unit
		Minimum	Maximum	Minimum	Maximum	
$t_{su(STA)}$	Start condition setup time	19*t_{PCLK}	-	17*t_{PCLK}	-	us
$t_{su(STO)}$	Stop condition setup time	17*t_{PCLK}	-	17*t_{PCLK}	-	us
$t_{w(STO:STA)}$	Time from Stop condition to Start condition (bus idle)	484*t_{PCLK}	-	144*t_{PCLK}	-	us
C_b	Capacitive load of each bus	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.
3. Ensure SCL drops below $0.3V_{DD}$ on falling edge before SDA crosses into the indeterminate range of $0.3V_{DD}$ to $0.7V_{DD}$.
   NOTE: For controllers that cannot observe the SCL falling edge then independent measurement of the time for the SCL transition from static high (V_{DD}) to $0.3V_{DD}$ should be used to insert a delay of the SDA transition with respect to SCL.
4. The maximum $t_{h(SDA)}$ could be 3.45 us and 0.9 us for Standard mode and Fast mode, but must be less than the maximum of $t_{vd(DAT)}$ or $t_{vd(ACK)}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{w(SCLL)}$)of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.
5. $t_{vd(DAT)}$ = time for data signal from SCL LOW to SDA output.
6. $t_{vd(ACK)}$ = time for Acknowledgement signal from SCL LOW to SDA output.

Figure 4-8 I2C bus AC waveform and measurement circuit (1)



1. Measurement point is set to the CMOS level： $0.3V_{DD}$ and $0.7V_{DD}$.

4.3.14 SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 4-3.

Refer to section 4.3.6 I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 4-24 SPI characteristics (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode, T_A = 25°C	-	24 (4)	MHz
		Slave mode, T_A = 25°C	-	12	
$t_{r(SCK)}$	SPI clock rise time	Load capacitance: C = 15pF	-	6	ns
$t_{f(SCK)}$	SPI clock fall time	Load capacitance: C = 15pF	-	6	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	10	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	10	-	ns
$t_{w(SCKH)}$ (1)	SCK high time	-	$t_{c(SCK)}/2$ - 6	$t_{c(SCK)}/2$ + 6	ns
$t_{w(SCKL)}$ (1)	SCK low time	-	$t_{c(SCK)}/2$ - 6	$t_{c(SCK)}/2$ + 6	ns
$t_{su(MI)}$ (1)	Data input setup time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	15	-	ns
$t_{su(SI)}$ (1)		Slave mode	5	-	ns
$t_{h(MI)}$ (1)	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler = 2, high speed mode	0	-	ns
$t_{h(SI)}$ (1)		Slave mode	5	-	ns
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	15	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	15	ns

1. Data based on characterization results. Not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 4-9 SPI timing diagram-slave mode and CPHA = 0, CPHASEL = 1

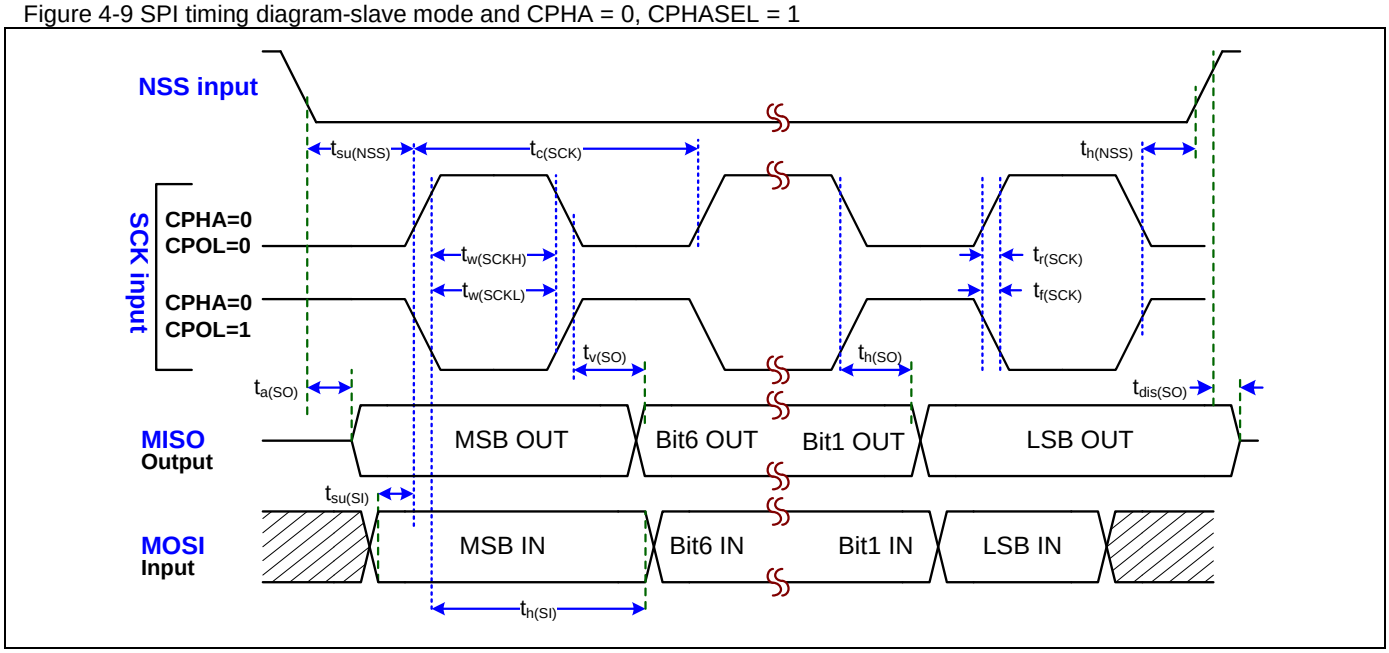
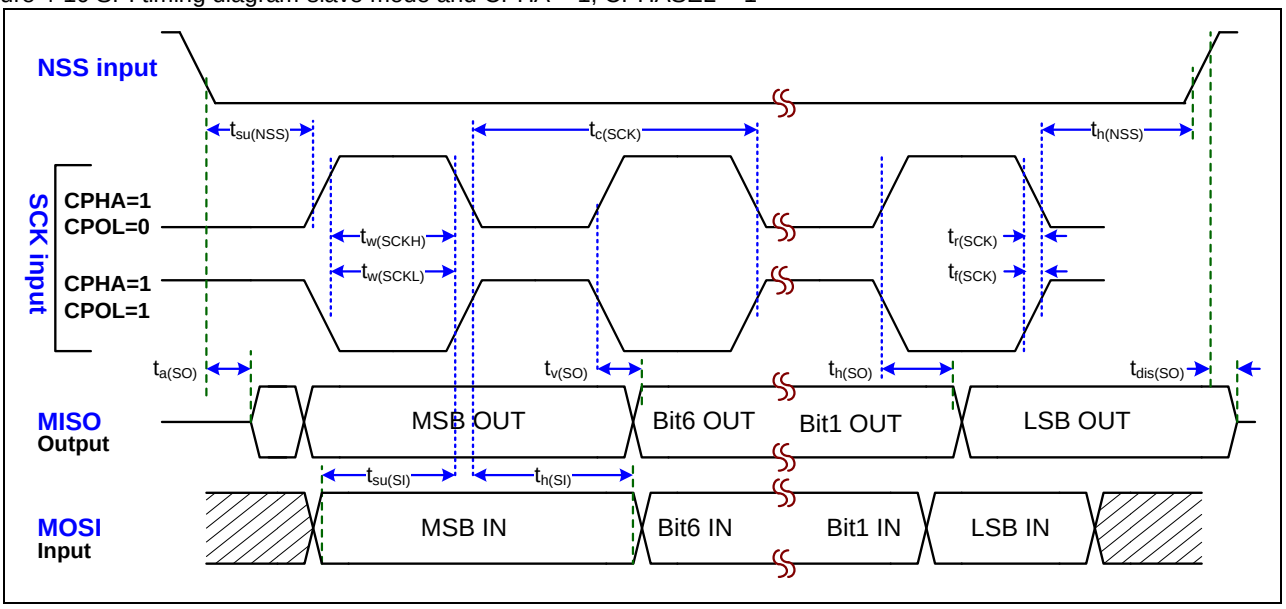
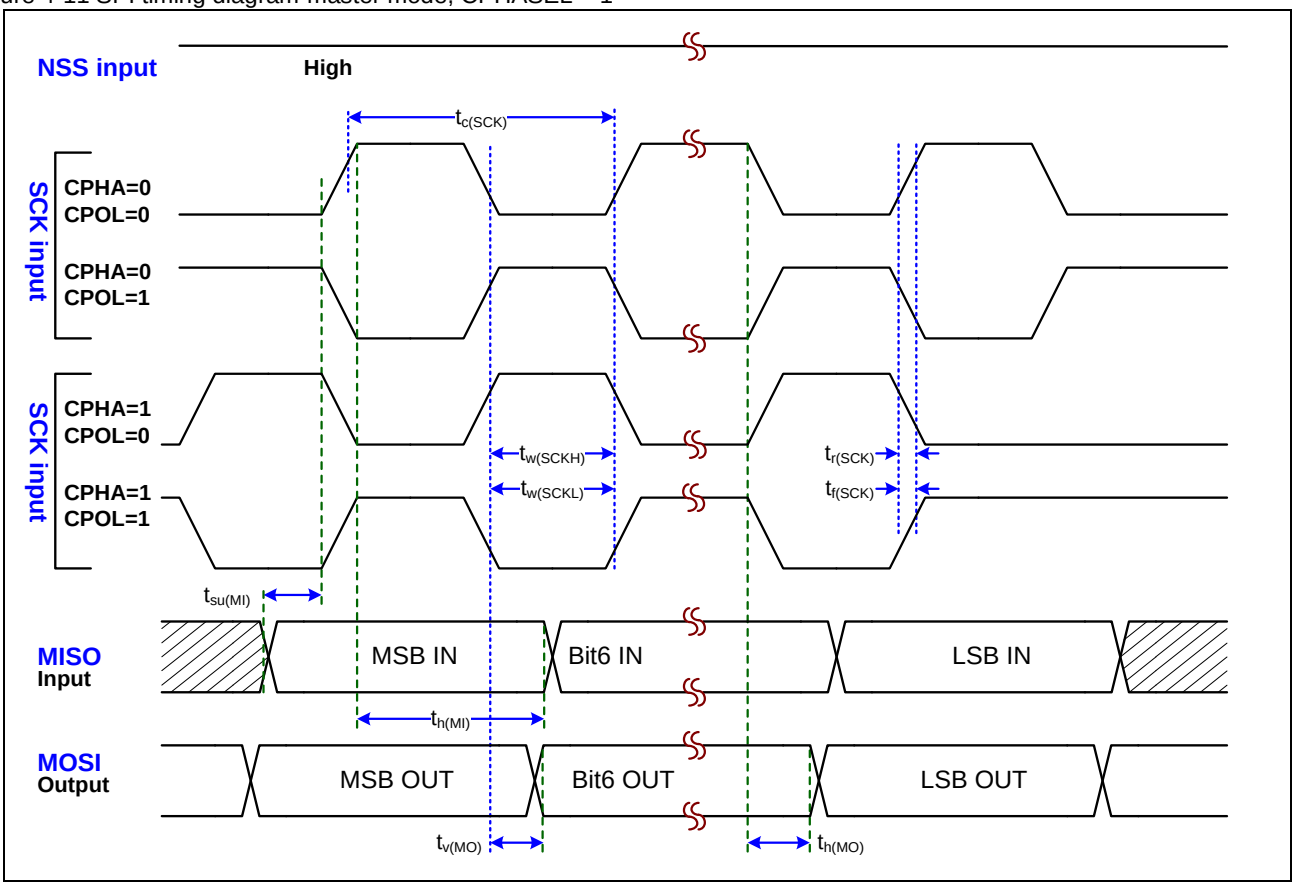


Figure 4-10 SPI timing diagram-slave mode and CPHA = 1, CPHASEL = 1 (1)



1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$

Figure 4-11 SPI timing diagram-master mode, CPHASEL = 1 (1)



1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

4.3.15 USART characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 4-3.

Refer to section 4.3.6 I/O port characteristics for more details on the input/output alternate function characteristics (SCLK, TX, RX).

Table 4-25 USART characteristics (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
f_{SCLK} $1/t_{c(SCLK)}$	USART clock frequency	Master mode, T_A = 25°C	-	6	MHz
		Slave mode, T_A = 25°C	-	6	
$t_{r(SCLK)}$	SCLK clock rise time	Load capacitance: C = 15pF	-	6	ns
$t_{f(SCLK)}$	SCLK clock fall time	Load capacitance: C = 15pF	-	6	ns
$t_{w(SCLKH)}$ (1)	SCLK high time	-	$t_{c(SCLK)}/2$ - 6	$t_{c(SCLK)}/2$ + 6	ns
$t_{w(SCLKL)}$ (1)	SCLK low time	-	$t_{c(SCLK)}/2$ - 6	$t_{c(SCLK)}/2$ + 6	ns
$t_{su(MI)}$ (1)	Data input setup time	Master mode, f_{PCLK} = 48MHz, prescaler = 8	5	-	ns
$t_{su(SI)}$ (1)		Slave mode	5	-	ns
$t_{h(MI)}$ (1)	Data input hold time	Master mode, f_{PCLK} = 48MHz, prescaler = 8	5	-	ns
$t_{h(SI)}$ (1)		Slave mode	5	-	ns
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	10	ns
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	26	ns

1. Guaranteed by design, not tested in production.

4.3.16 ADC characteristics

Unless otherwise specified, the parameters in the table below are measured under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions summarized in Table 4-3.

Table 4-26 ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	-	2.5	3.3	5.5	V
f_{ADC}	ADC clock frequency	-	-	-	16	MHz
f_S (1)	Sampling frequency	VDD > 2.8V			1	MHz
		VDD <=2.8V	-	-	400	KHz
f_{TRIG} (1)	External trigger frequency (3)	f_{ADC} = 16MHz	-	-	1	MHz
		-	-	-	16	$1/f_{ADC}$
V_{AIN} (2)	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN} (1)	External input impedance	-	See equation 2			kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	1.5	kΩ
C_{ADC} (1)	Internal sample and hold capacitance	-	-	-	10	pF
t_{STAB} (1)	Stabilization time	-	-	-	10	μs
t_{latr} (1)	Delay between trigger and conversion start	-	-	-	-	$1/f_{ADC}$
t_S (1)	Sampling time	f_{ADC} = 16MHz	0.156	-	15.031	μs
		-	2.5	-	240.5	$1/f_{ADC}$
t_{CONV} (1)	Total conversion time (including sampling time)	f_{ADC} = 16MHz	0.9375	-	15.8125	μs
		-	15 ~ 253 (sampling t_S + successive approximation 12.5)			$1/f_{ADC}$
ENOB	Effective number of bits	-	-	10.5	-	bit

1. Guaranteed based on test during characterization. Not tested in production.
2. Guaranteed by design, not tested in production.
3. In this product, VREF+ is internally connected to VDDA， VREF− is internally connected to VSSA.
4. Guaranteed by design, not tested in production.
5. For external trigger, a delay of $1/f_{ADC}$ must be added.

AIN Input impedance

Equation 2

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{n+2})} - R_{ADC}$$

The formula above is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (12-bit resolution), is derived from tests under f_{ADC} = 15MHz.

Table 4-27 Maximum R_{AIN} at f_{ADC} = 15MHz (1)

T_S (cycles)	t_S (μs)	Maximum R_{AIN} (kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

1. Guaranteed by design. Not tested in production.

Table 4-28 ADC static parameters (1)(2)

Symbol	Parameter	Conditions	Typical	Unit
ET	Comprehensive error	f_{PCLK1} = 48MHz, f_{ADC} = 16MHz, R_{AIN} < 0.1 kΩ, V_{DDA} = 3.3V, T_A = 25°C	-2.1 ~ 3.8	LSB
EO	Offset error		-2.4 ~ 1.1	
EG	Gain error		-0.6 ~ 1.0	
ED	Differential linearity error		-0.8 ~ 1.0	
EL	Integral linearity error		-2.8 ~ 1.5	

1. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in section 4.2 Absolute maximum rating does not affect the ADC accuracy.
2. Guaranteed based on characterization. Not tested in production.

The implications of the ADC static parameters are seen below, and the corresponding schematic diagram is shown in Figure 4-12.

- ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.
- EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.
- EG = Gain error: The deviation between the last ideal transition and the last actual transition.
- ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.
- EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

Figure 4-12 Schematic diagram of ADC static parameters

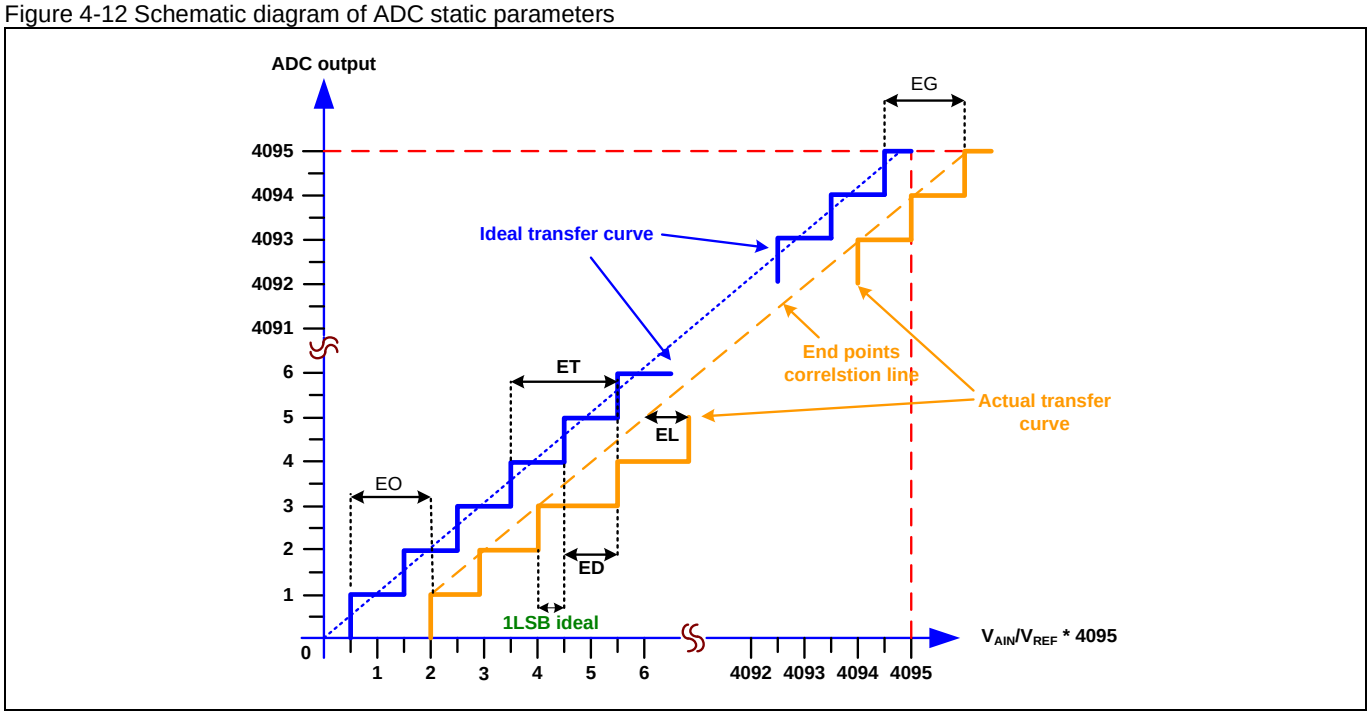
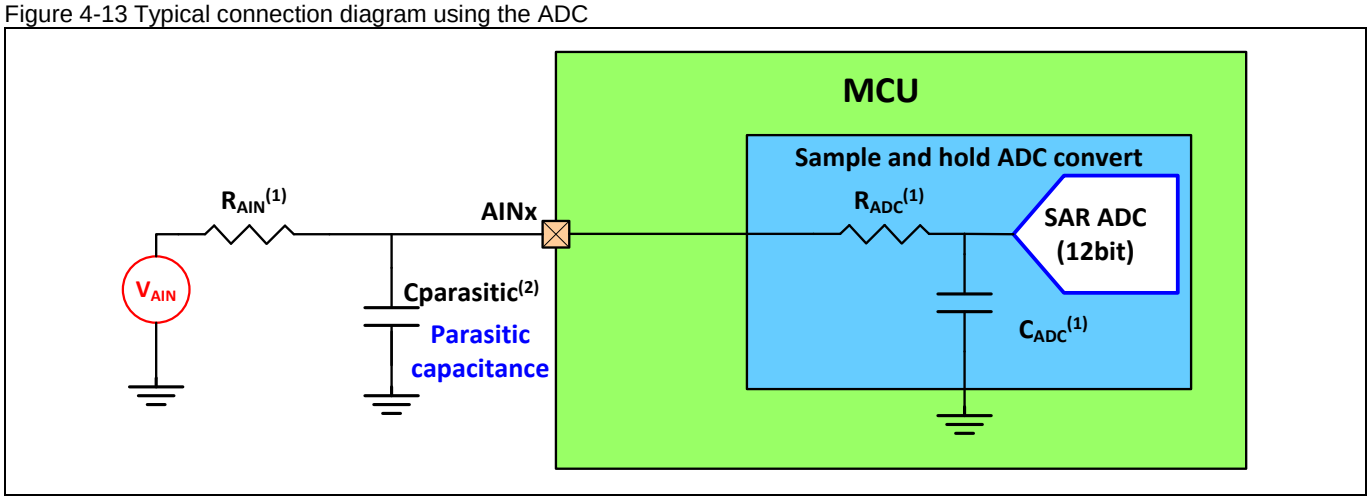


Figure 4-13 Typical connection diagram using the ADC

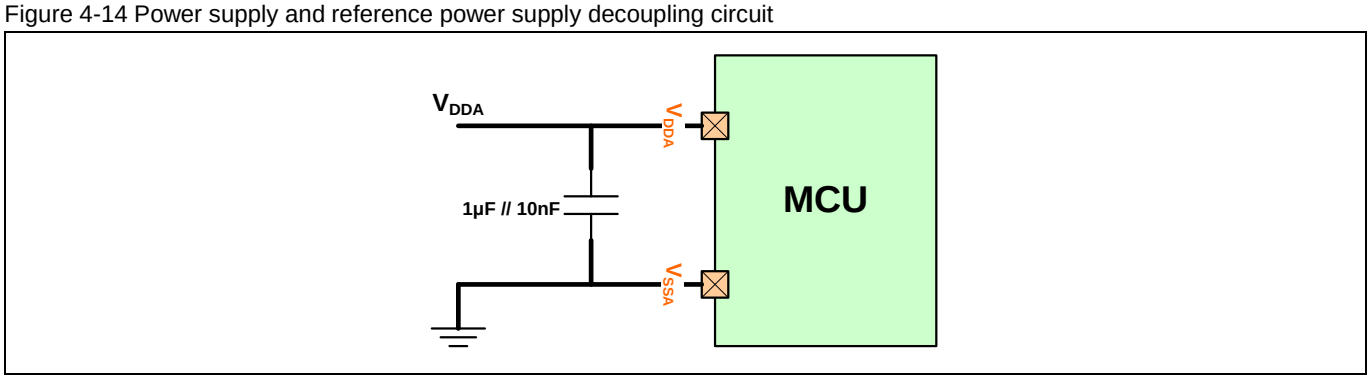


1. See Table 4-26 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply must be connected as shown below. The 10nF capacitor in the figure must be a ceramic capacitor (good quality) , and they should be as close as possible to the MCU chip.

Figure 4-14 Power supply and reference power supply decoupling circuit



5 Package dimensions

5.1 QFN20 (3x3x0.55mm)

Figure 5-1 QFN20 package dimension

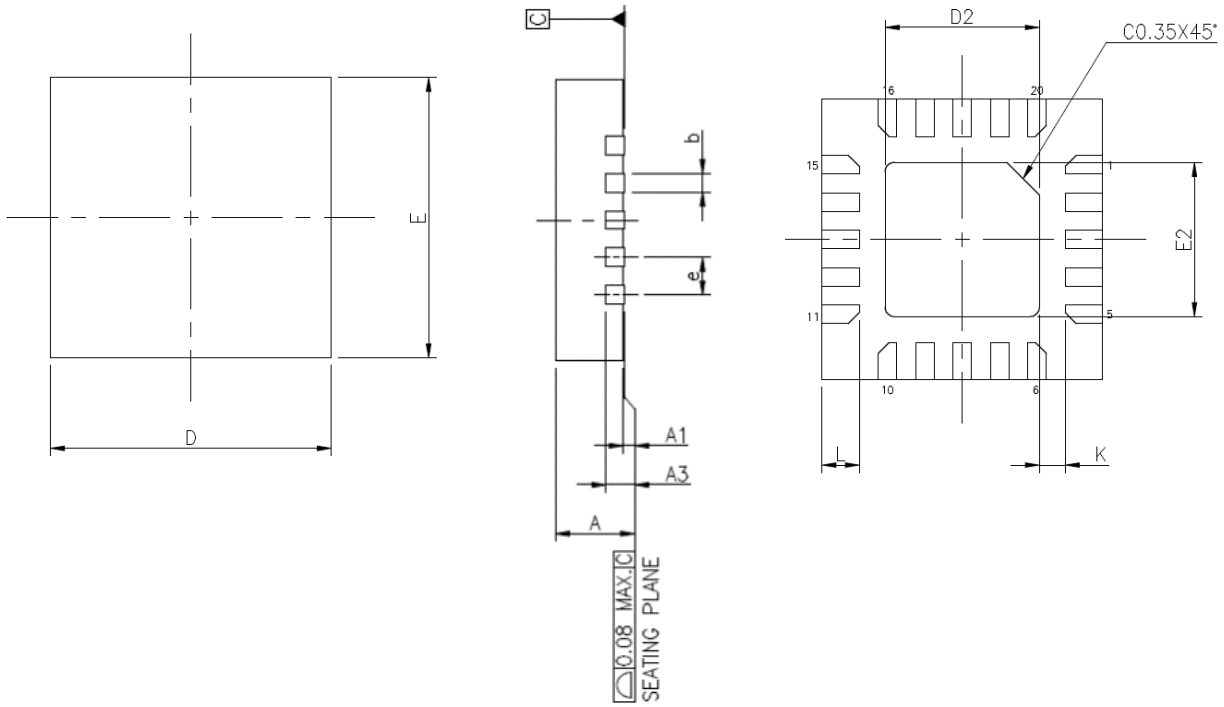


Table 5-1 QFN20 Dimension

Unit	mm			inch		
JEDEC	MO-220			MO-220		
PKG	WQFN(X319)			WQFN(X319)		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.50	0.55	0.60	0.019	0.021	0.023
A1	0.00	0.02	0.05	0.000	0.000	0.001
A3	0.150 REF.			0.005 REF.		
b	0.15	0.20	0.25	0.005	0.007	0.009
D	3.00 BSC			0.11 BSC		
E	3.00 BSC			0.11 BSC		
e	0.40 BSC			0.015 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
K	0.20	---	---	0.007	---	---
D2	1.60	1.65	1.70	0.062	0.064	0.066
E2	1.60	1.65	1.70	0.062	0.064	0.066

5.2 TSSOP20 (173mil) package dimension

Figure 5-2 QFN20 package dimension

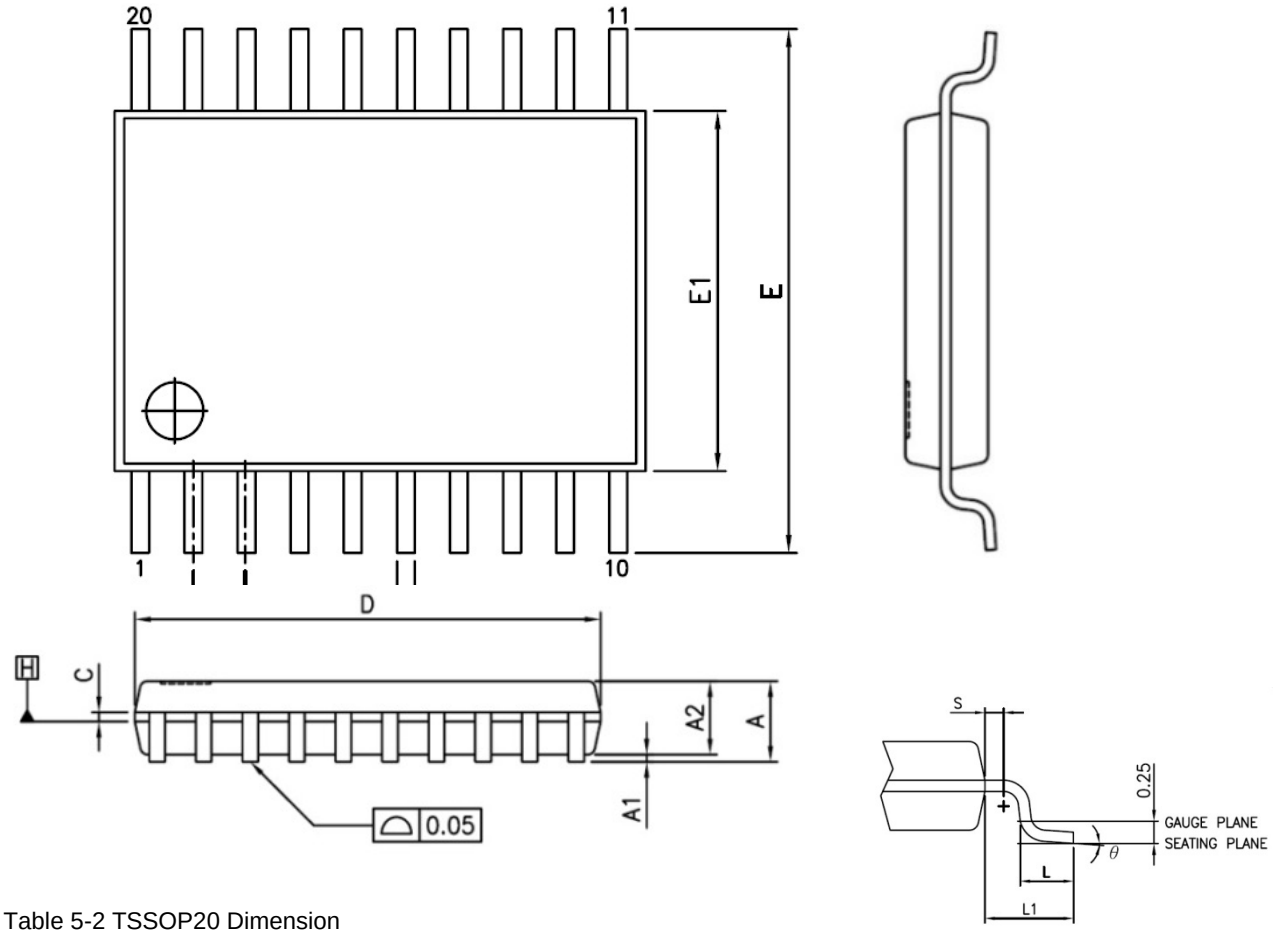


Table 5-2 TSSOP20 Dimension

Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	----	----	1.20	----	----	0.047
A1	0.05	----	0.15	0.001	----	0.005
A2	0.80	0.90	1.05	0.031	0.035	0.041
b	0.19	----	0.30	0.007	----	0.011
C	0.09	-----	0.20	0.003	-----	0.007
D	6.40	6.50	6.60	0.251	0.255	0.259
E1	4.30	4.40	4.50	0.169	0.173	0.177
E	6.40 BSC			0.251 BSC		
e	0.65 BSC			0.025 BSC		
L1	1.00 REF			0.039 REF		
L	0.50	0.60	0.75	0.019	0.023	0.029
S	0.20	----	----	0.007	----	----
θ	0°	----	8°	0°	----	8°

6 Revision history

Table 6-1 Revision history

Rev	Descriptions	Date
V1.1	1. Initial Version	2024/09/06
V1.2	1. Modify Diagrams	2024/11/17

7 Disclaimers

Herein, Megawin stands for "***Megawin Technology Co., Ltd.***"

Life Support — This product is not designed for use in medical, life-saving or life-sustaining applications, or systems where malfunction of this product can reasonably be expected to result in personal injury. Customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify Megawin for any damages resulting from such improper use or sale.

Right to Make Changes — Megawin reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in mass production, relevant changes will be communicated via an Engineering Change Notification (ECN).