CR2105

LDO

Data Sheet

100V 50mA Very High Voltage Linear Regulator

Version: V1.3

1. General Description

The CR2105 device is a very high voltage-tolerant linear regulator that offers the benefits of a thermally-enhanced package, and is able to withstand continuous DC or transient input voltages of up to 100 V. The CR2105 device is stable with output capacitance greater than 2.2μF and any input capacitance greater than 0.47μF. Therefore, implementations of this device require minimal board space because of its miniaturized packaging (PSOP8) and a potentially small output capacitor. In addition, the CR2105 device offers an enable pin (EN) compatible with standard CMOS logic to enable a low-current shutdown mode.

The CR2105 device has an internal thermal shutdown and current limiting to protect the system during fault conditions. The SOP8-EP packages have an operating temperature range of TJ = - 40°C to 125°C. In addition, the CR2105 device is ideal for generating a low-voltage supply from intermediate voltage rails in telecom and industrial applications; not only can it supply a well-regulated voltage rail, but it can also withstand and maintain regulation during very high and fast voltage transients. These features translate to simpler and more cost-effective electrical surge-protection circuitry for a wide range of applications, including PoE, bias supply, and LED lighting.

2. Ordering Information

Part Number	Marking	Package
CR2105_ES8	2105 YYWW	SOP8-EP
CR2105_235	TYYWW	SOT23-5

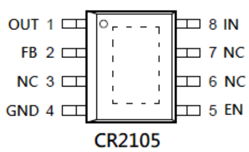
3. Features

- VIN Range 7 to 100V
- Output Voltage Tolerances of ±1.5%
- Output Current of 50 mA
- Low Quiescent Current 23μA
- Quiescent Current at Shutdown 8μA
- Dropout Voltage 2.8V at IOUT = 50 mA
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limit
- Adjustable Output Voltage from 1.2 to 90V

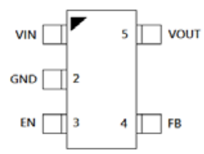
4. Applications

- Microprocessors, Microcontrollers Powered by Industrial Busses With High Voltage Transients
- Industrial Automation
- Telecom Infrastructure
- Automotive
- Power over Ethernet(PoE)
- LED Lighting

5. Pin Configuration

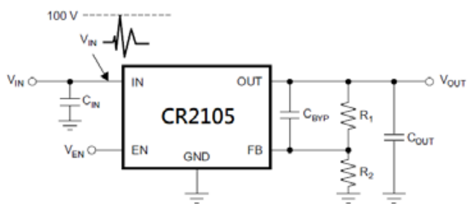


SOP8-EP



SOT23-5

6. Typical Application Circuit



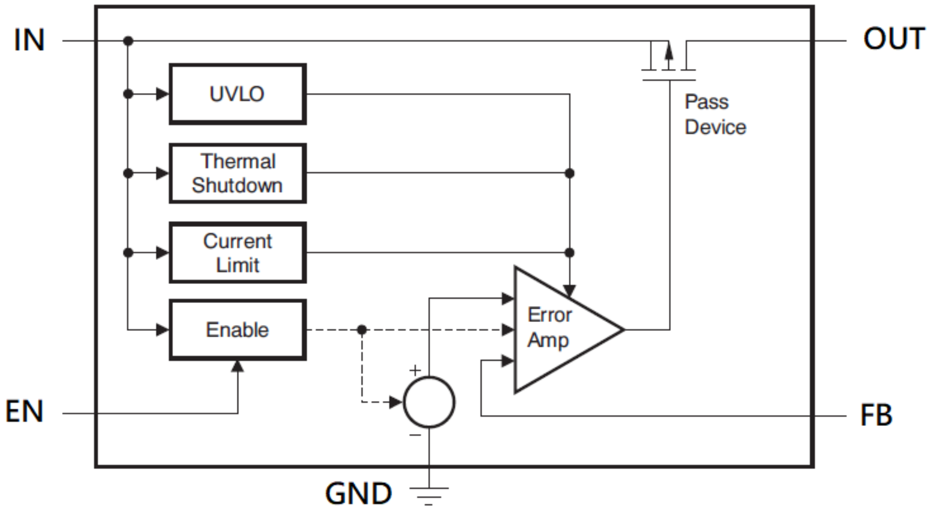
Stable with ceramic capacitor

7. List of Contents

8. Pin Assignment

Pin Name	SOP8-EP Pin No	SOT235 Pin No	Pin Function
OUT	1	5	Output Voltage Pin
FB	2	4	Feedback
NC	3,6,7	-	Non Connect
GND	4,EP	2	Ground
EN	5	3	Enable
IN	8	1	Input Voltage pin.

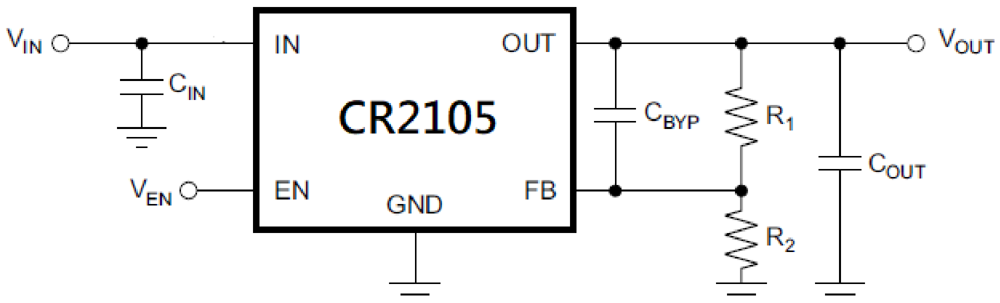
9. Function Block Diagram



10. Design Parameters

Vout (V)	Cin (uF)	Cout(uF)	*Cbypass(nF)	R1 (Kohm)	R2 (Kohm)
12	10	10	10	698	49.9
5	10	10	10	262	49.9
3.3	10	10	10	156	49.9
1.8	10	10	10	62.5	49.9

*Cbypass is for Maximum AC Performance, not requested.



1. Vout = 0.8V * (R1+R2) / R2
2. 10uA < Vout / (R1+R2) < 30uA

11. Absolute Maximum Ratings (Note1)

- V_{IN} -- -0.3V to 110V
- V_{OUT} -- -0.3V to 110V
- FB -- -0.3V to 5.5V
- EN -- -0.3V to 110V
- Power Dissipation, PD@T_A=25°C, PSOP-8---1.8W
- Thermal Resistance, θ_{JA}, PSOP-8---55°C/W
- Thermal Resistance, θ_{JC}, PSOP-8---20°C/W
- Power Dissipation, PD@T_A=25°C, SOT23-5--0.4W
- Thermal Resistance, θ_{JA}, SOT23-5--250°C /W
- Junction Temperature-- 125°C
- Lead Temperature (Soldering, 10 sec.)--- 300°C
- Storage Temperature --- –65°C to 150°C

12. Recommended Operating Conditions

- Input Voltage, V_{IN} --- 7V to 100V
- Output Voltage, V_{OUT} --- 1.2V to 90V
- Enable Voltage, V_{EN} --- 0V to 100V
- Output Current, I_{OUT} --- 0mA to 50mA
- Junction Temperature --- -40°C to 125°C
- Ambient Temperature --- -40°C to 85°C

13. Electrical Characteristics

V_{IN}=V_{OUT} + 4V or V_{IN}=7V(whichever is greater), I_{OUT}=100uA, C_{IN}=1uF, C_{OUT}=4.7uF, T_J=25℃, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}		7		100	V
Internal Reference	V_{REF}		0.784	0.8	0.816	V
Line Regulation	$\triangle V_{LINE}$	V_{IN}=7V to 100V, V_{OUT}=1.6V		0.18	1.25	%
Load Regulation	$\triangle V_{LOAD}$	100uA < I_{OUT} < 50mA, V_{OUT}=1.6V		1.25	3.12	%
Dropout Voltage	V_{DROP}	I_{OUT}=20mA		1000		mV
		I_{OUT}=50mA		2800		mV
Quiescent Current	I_Q	I_{OUT} = 0mA		23	40	uA
Shutdown Current	I_{SD}	V_{EN} = 0V		8	15	uA
Current Limit	I_{CL}	V_{OUT} = 90% $V_{OUT(NOM)}$	55	120	200	mA
Enable High Low Level	V_{ENHI}		1.5			V
	V_{ENLO}				0.4	V
Enable Pin Current	I_{EN}	7V<V_{IN}<100V, V_{IN}=V_{EN}		0.02	1	uA
Feedback Pin Current	I_{FB}			0.01	0.11	uA
Thermal Shutdown	T_{SD}	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		°C

14. Typical Characteristics

V_{IN}=12V, V_{OUT}=5V I_{OUT}=1mA, C_{IN}=0.47uF, C_{OUT}=2.2uF, T_J=25℃, unless otherwise specified

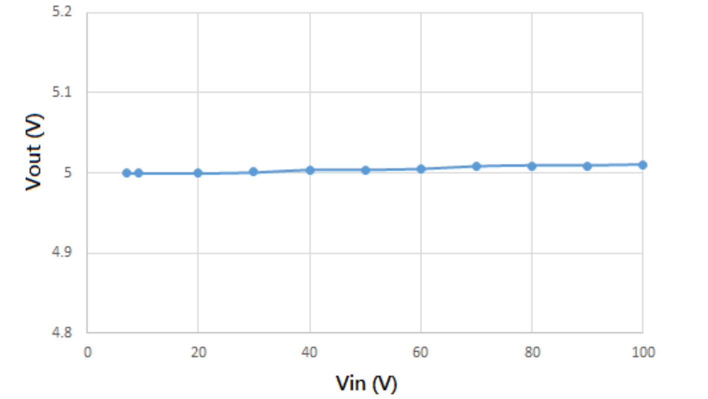


Fig1. Vout vs Vin

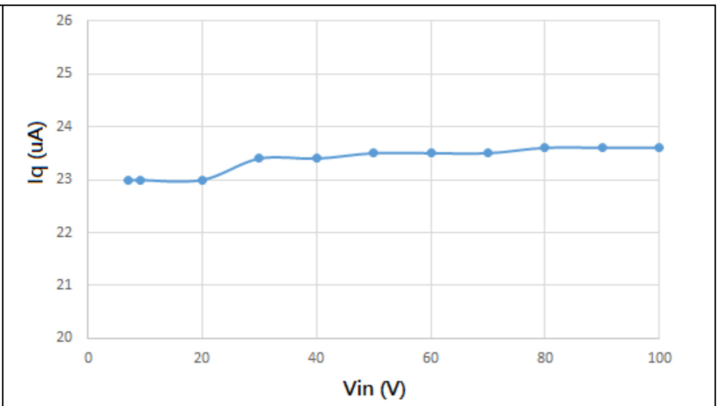
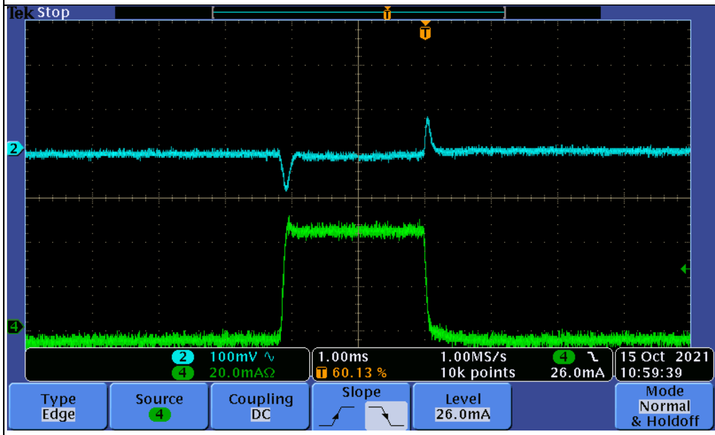
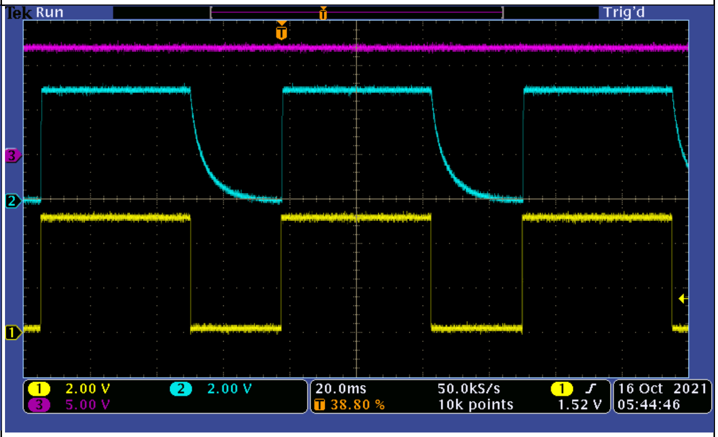


Fig2. Iq vs Vin



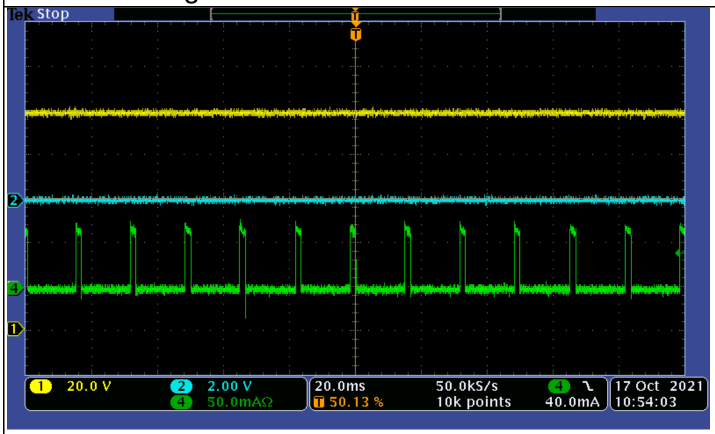
CH2: V_{OUT}, CH4: I_{OUT}

Fig3. Load transient 0 to 50mA



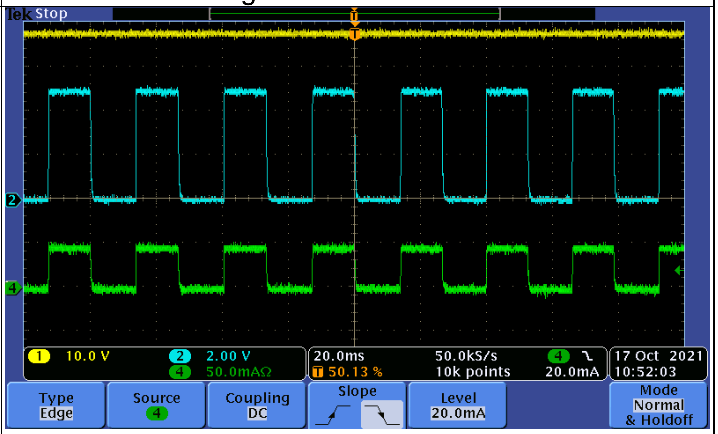
CH1: EN, CH2: V_{OUT}, CH3: V_{IN}

Fig4. Enable ON/OFF



CH1: V_{IN}, CH2: V_{OUT}, CH4: I_{OUT}

Fig5. V_{IN}=100V, V_{OUT} short to GND



CH1: V_{IN}, CH2: V_{OUT}, CH4: I_{OUT}

Fig6. V_{IN}=36V, V_{OUT}=5V, R_{LOAD}=100ohm, thermal protect

15. IC Operation Information

15.1. Basic Operation

The CR2105 device belongs to a new generation of linear regulators that use an innovative BCD process technology to achieve very high maximum input and output voltages.

This process not only allows the CR2105 device to maintain regulation during very fast high-voltage transients up to 105 V, but it also allows the CR2105 device to regulate from a continuous high-voltage input rail. Unlike other regulators created using bipolar technology, the ground current of the CR2105 device is also constant over its output current range, resulting in increased efficiency and lower power consumption.

These features, combined with a high thermal performance SOP8EP Power PAD package, make this device ideal for industrial and telecom applications.

15.2. Over-Temperature Protection (OTP)

The over-temperature protection function will turn off the P-MOSFET when the junction temperature exceeds 160℃ (typ.). Once the junction temperature cools down by approximately 20℃(typ.), the regulator will automatically resume operation.

15.3. Current-limit Protection

The CR2105 provides current limit function to prevent the device from damages during overload or shorted-circuit condition. This current is detected by an internal sensing transistor.

15.4. Error Amplifier

The Error Amplifier compares the internal reference voltage with the output feedback voltage from the internal divider, and controls the Gate voltage of P-MOSFET to support good line regulation and load regulation at output voltage.

15.5. Enable Function

The CR2105 device provides an enable pin (EN) feature that turns on the regulator when VEN > 1.5V, and disables the regulator when VEN < 0.4V.

16. IC Application Information

Like any low dropout linear regulator, the CR2105's external input and output capacitors must be properly selected for stability and performance. Use a 10μF (X5R or X7R) or larger input capacitor and place it close to the IC's VIN and GND pins. Any output capacitor meeting the minimum 1mΩ ESR (Equivalent Series Resistance) and effective capacitance larger than 10μF (X5R or X7R) requirement may be used. Place the output capacitor close to the IC's VOUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

16.1. Current Limit

The CR2105 contains an independent current limiter, which monitors and controls the pass transistor's gate voltage, limiting the output current to 0.12A (typ.). The output can be shorted to ground indefinitely without damaging the part.

16.2. Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage V_{DROP} can also be expressed as the voltage drop on the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance $R_{DS(ON)}$. Thus the dropout voltage can be defined as ($V_{DROP} = V_{VIN} - V_{VOUT} = R_{DS(ON)} \times I_{RATED}$). For normal operation, the suggested LDO operating range is ($V_{VIN} > V_{VOUT} + 4V$) for good transient response and PSRR ability. Conversely, operating at the ohmic region will degrade these performance severely.

16.3. Minimum Operating Input Voltage (VIN)

The CR2105 does not include any dedicated UVLO circuitry. The CR2105 at least 7V. The output voltage is not regulated until VIN has reached at least the greater of 7 V or (VOUT + 4V)

16.4. Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$ and

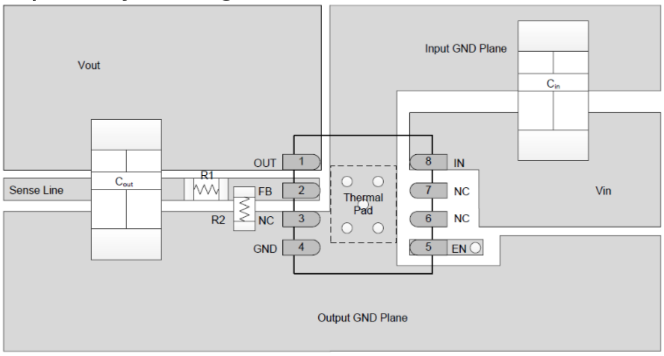
$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance. For recommended operating condition specifications the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP8 (Exposed PAD) package, the thermal resistance, θ_{JA}, is 40°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOT235 package, the thermal resistance, θ_{JA}, is 243.3°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)} = (125°C - 25°C) / (55°C/W) = 1.81W$ for SOP8 (Exposed Pad) package

$P_{D(MAX)} = (125°C - 25°C) / (250°C/W) = 0.4W$ for SOT235 package The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure(below) allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

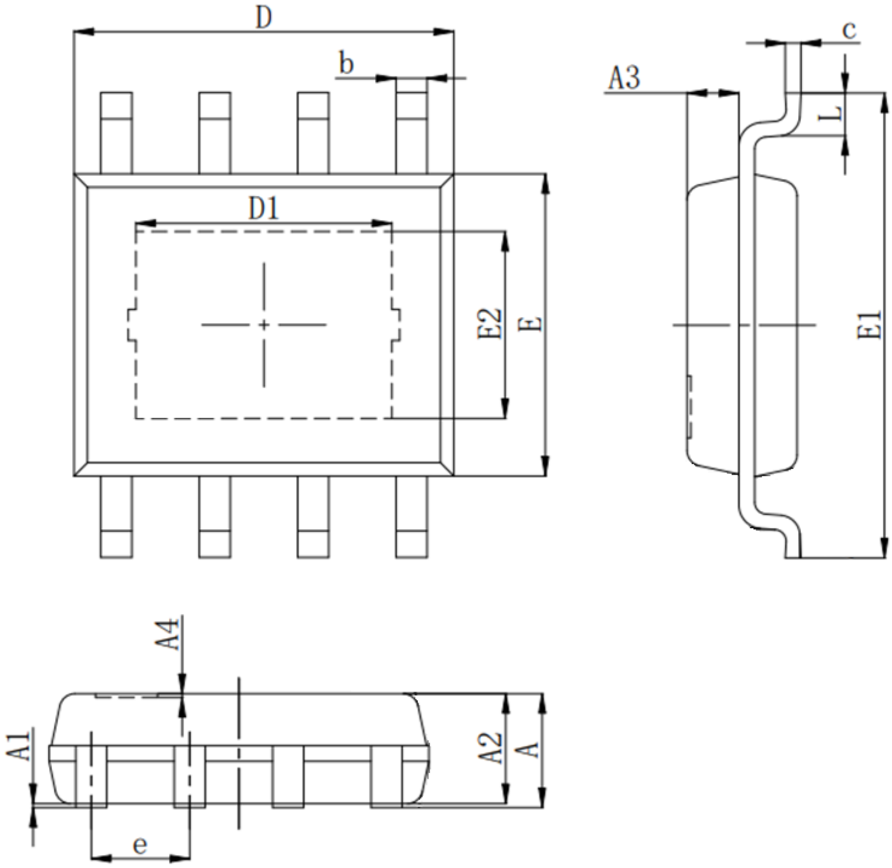
16.5. Layout Considerations

The dynamic performance of the CR2105 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the CR2105. Best performance is achieved by placing CIN and COUT on the same side of the PCB as the CR2105, and as close to the package as possible is practical. The ground connections for C_{IN} and C_{OUT} must be back to the CR2105 ground pin using a copper trace as wide and short as possible. Connections using long trace lengths, narrow trace widths, and/or connections through vias must be avoided. These added parasitic inductances and resistance may result in inferior performance especially during transient conditions.



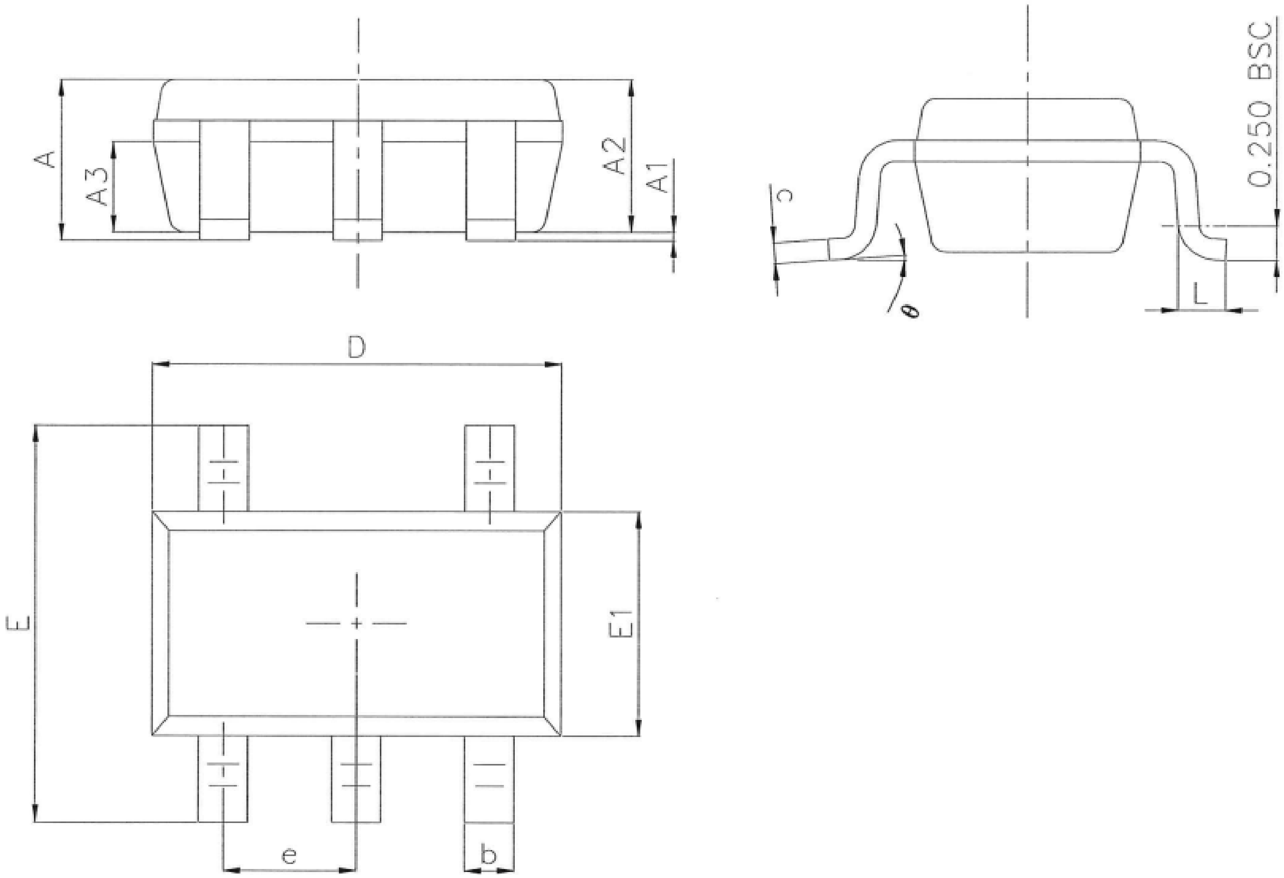
17. Package Information

17.1. SOP8-EP



Symbol	Dimension in mm			Dimension in inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.300	1.300	1.500	0.051	0.051	0.059
A1	0.000	0.000	0.100	0.000	0.000	0.004
A2	1.350	1.350	1.420	0.053	0.053	0.056
A3	0.645	0.645	0.670	0.025	0.025	0.026
A4	0.020	0.020	-	0.001	0.001	-
c	0.170	0.170	0.203	0.007	0.007	0.008
E	3.800	3.800	3.900	0.150	0.150	0.154
E1	5.800	5.800	6.000	0.228	0.228	0.236
E2	2.183	2.183	2.283	0.086	0.086	0.090
L	0.450	0.450	0.600	0.018	0.018	0.024
b	0.330	0.330	0.400	0.013	0.013	0.016
D	4.800	4.800	4.900	0.189	0.189	0.193
D1	3.272	3.272	3.372	0.129	0.129	0.133
e	-	1.270	-	-	0.050	-

17.2. SOT23-5



Symbol	Dimension in mm			Dimension in inch		
	Min.	Min.	Nom.	Max.	Min.	Nom.
A	1.050	1.150	1.250	0.041	0.045	0.049
A1	0.000	0.060	0.100	0.000	0.002	0.004
A2	1.000	1.100	1.200	0.039	0.043	0.047
A3	0.550	0.650	0.750	0.022	0.026	0.030
D	2.820	2.920	3.020	0.111	0.115	0.119
E	2.650	2.800	2.950	0.104	0.110	0.116
E1	1.510	1.610	1.700	0.059	0.063	0.067
b	0.300	0.400	0.500	0.012	0.016	0.020
e	0.95BSC			0.037BSC		
θ	0°	4°	8°	0°	4°	8°
L	0.300	0.420	0.570	0.012	0.017	0.022
c	0.100	0.152	0.200	0.004	0.006	0.008

18. Revision History

Rev	Descriptions	Date
V1.1	Initial version preliminary released	2024/08/26
V1.2	1. Add Revision History table 2. Modify the errors in the minimum, maximum, and nominal dimensions. 3. Modify the part number for the SOP-EP package is **CR2105_ES8**. 4. Correct the order errors of dimensions **E1** and **E**.	2024/11/08
V1.3	Update document Layout Configuration	2024/11/27

19. Disclaimers

Herein, Megawin stands for "***Megawin Technology Co., Ltd.***"

Life Support — This product is not designed for use in medical, life-saving or life-sustaining applications, or systems where malfunction of this product can reasonably be expected to result in personal injury. Customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify Megawin for any damages resulting from such improper use or sale.

Right to Make Changes — Megawin reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in mass production, relevant changes will be communicated via an Engineering Change Notification (ECN).