MSE03GM1

Data Sheet

Version: 0.1

Features

- **CPU Core**
  - ARM 32-bit Cortex-M0 CPU
  - Operation frequency up to 48MHz
  - Built-in one NVIC for 32 external interrupt inputs with 4-level priority
  - Built-in one 24-bit system tick timer
  - Built-in one single-cycle 32-bit multiplier
  - Built-in one SWD serial wire debugger with 2 watch points and 4 breakpoints
- **Reset**
  - Built-in embedded POR (power-on reset) circuit
  - Built-in one reset source controller
    - Programmable chip cold reset and warm reset for reset source
    - Independent software reset control for internal modules
- **Clock**
  - Built-in embedded ILRCO (internal low frequency RC oscillator) by 32KHz
  - Built-in embedded IHRCO (internal high frequency RC oscillator)
    - Trimmed to 11.059 or 12MHz ±1% at +25℃
  - Built-in embedded PLL clock output for system clock
  - Built-in a clock source controller with independent clock enable control for modules
- **GPIO**
  - Support general purpose IO pins for application
    - Maximum 44 GPIO pins for LQFP48 package
  - Provide selectable IO modes by pin independent
    - Push-Pull output
    - Quasi bidirectional (PC pins only)
    - Open-drain output
    - Digital Input with high impedance
- **I2C**
  - Provide I2c modules : I2C0
  - I2C module common functions
    - Support master and slave mode
    - Support programmable clock rate control and clock rate up to 1 MHz
    - Support programmable high/low period control for master mode
    - Support clock stretching for slave mode
    - Support general call function
    - Support multi-master processing capability
    - Support both Byte mode and Buffer mode flow control
    - Support Byte mode bus event code for simplex firmware control
    - Support Buffer mode 4-byte data buffer and 32-bit data register for high speed communication
    - Received and transmitted data are buffered with DMA capability
    - Support slave address hardware detection wakeup from STOP mode
    - Support SMBus timeout detection
- **ADC**
  - 12-bit SAR ADC with 1.5Msps
    - Configurable resolution : 12/10/8-bit
    - Configurable sampling time
  - Provide external 16 channels and internal 7 channels input
    - Internal extra channel source : VBUF, VSSA , LDO VR0, DAC out, 1/2VDD, VPG, TS out

- Support auto-sampling and trigger by external pin, internal events and software bit
- Data alignment for output code left/right justify
- Built-in input buffer stage with bypass option
  - PGA with programmable gain : 1~4
- Optional ADC top voltage reference from external VREF+ or internal IVR24
- Interrupt generation at the end of sampling, end of conversion, end of sequence conversion
- Support voltage window detection and output code limitation
- Built-in three channel independent hardware accumulators for ADC output code
- Support one-shot/channel scan/loop scan

❖ Operating

- Operating voltage range 1.8V ~ 5.5V
- Operating temperature range -40℃ ~ 105℃ (**1)
- Operating frequency range up to 48MHz

❖ Package Types

- LQFP48

Contents

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1 General Description

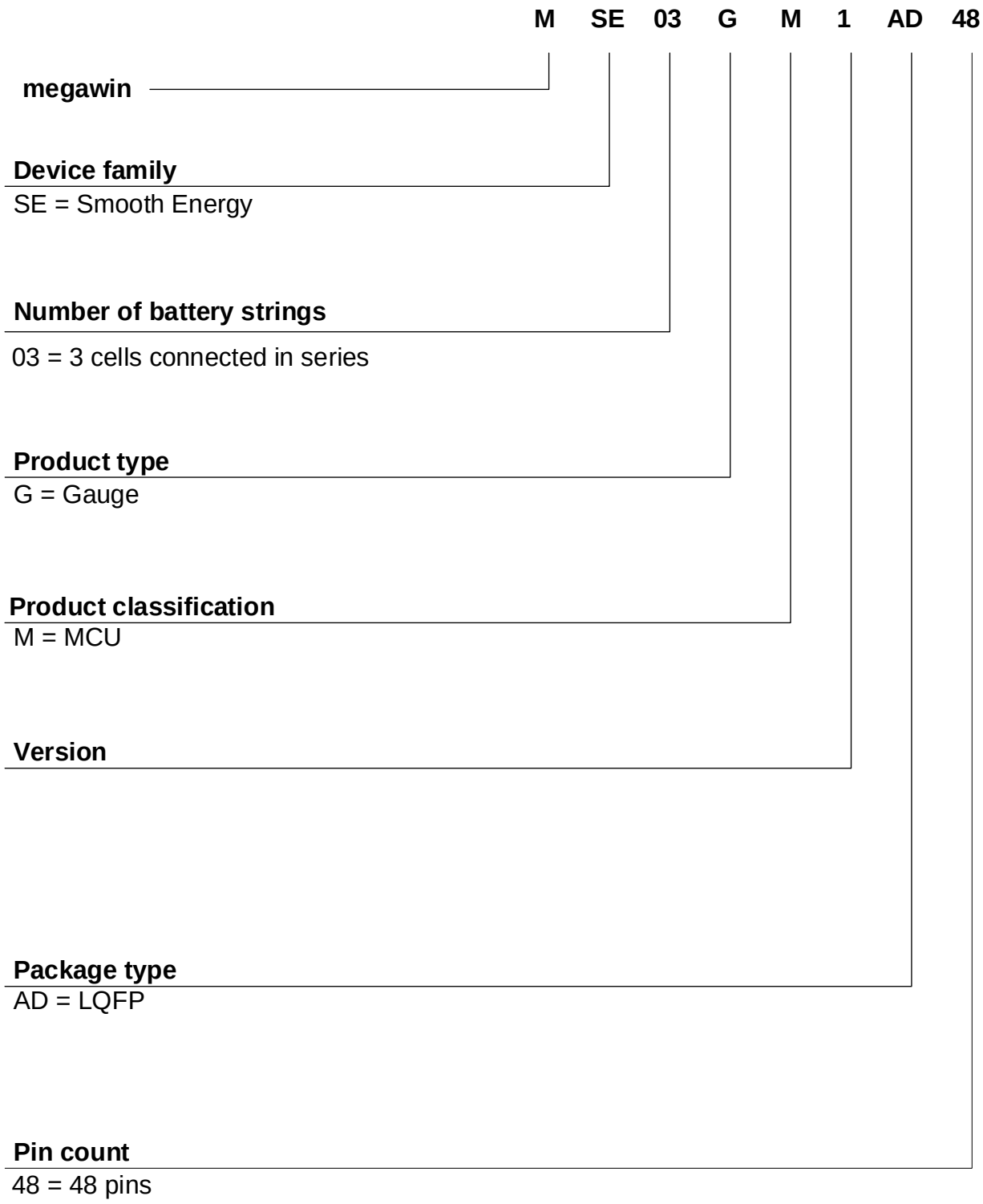
The **MSE03GM1** is a BMS MCU based on a high performance Core ARM® 32-bit Cortex®-M0 CPU with embedded Nested Vectored Interrupt Controller (NVIC).

The **MSE03GM1** has a built-in battery gas gauge algorithm. Suitable for 3-4 cells of lithium-ion and lithium-polymer batteries connected in series. This device also contains a set of ADCs that monitor each cell's voltage as well as current and temperature measurements.

2 Order Information

Please contact the megawin sales for available options (memory size, package …) and more information about this device.

Figure 2-1. Part Numbering

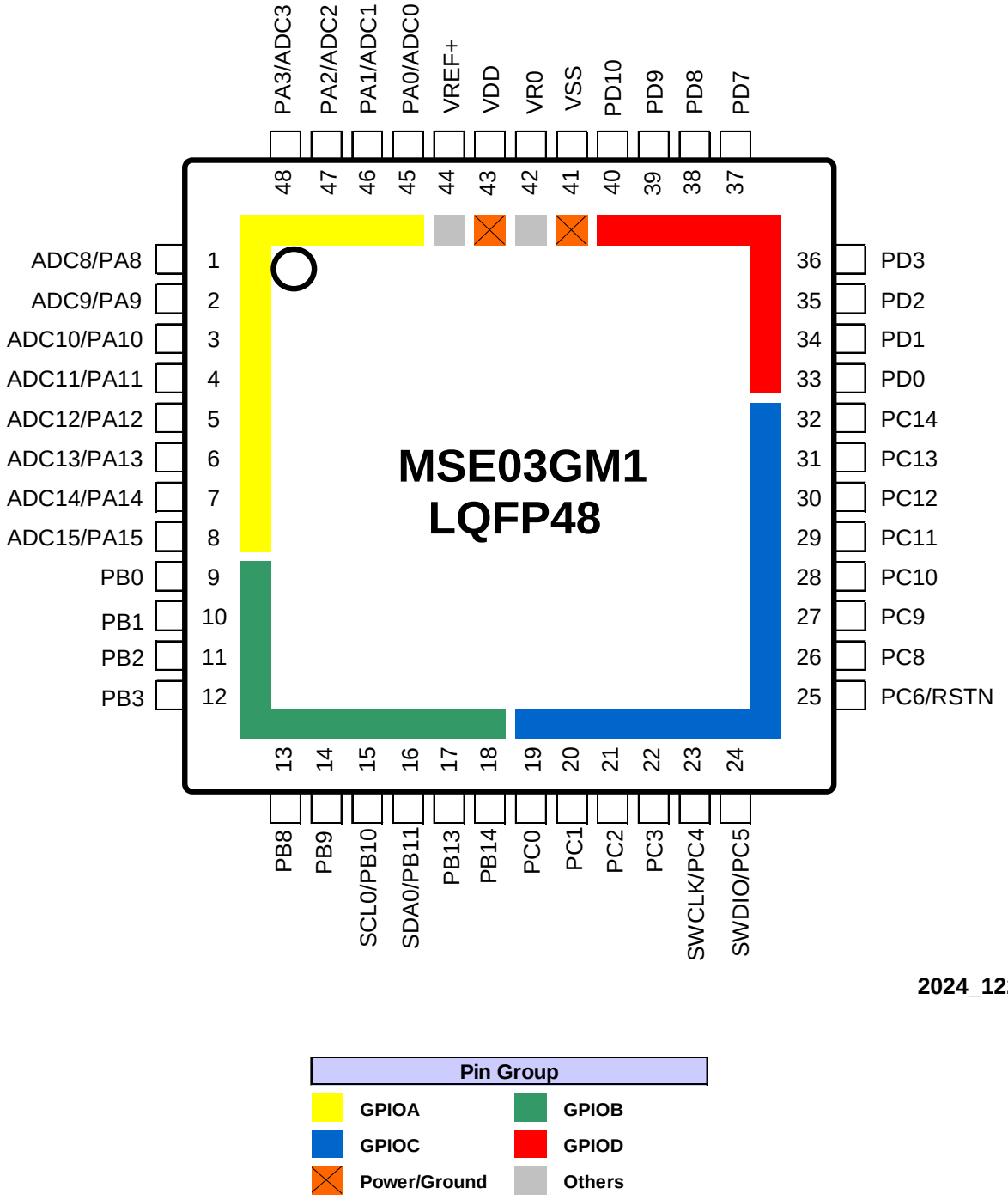


3 Pin Description

3.1. Pin Outline

3.1.1. LQFP48 Package Pinout

Figure 3-1. LQFP48 Package Pinout



4 Functional Descriptions

4.1. ADC

4.1.1. Introduction

The chip builds in one ADC0 module which embeds one 12-bit successive approximation ADC (analog-to-digital converter), one PGA (programmable gain amplifier) with gain 1~4 and digital logic for output code control. It supports the configurable multiplexed channels those include 16 external and 4 internal sources. The analog-to-digital conversion can be performed in one-shot, continuous, one-loop scan or continuous loop scan modes.

The ADC is embedded one temperature sensor to measure the internal thermal of chip for product application.

4.1.2. Features

- **12-bit SAR ADC with 1.5Msps**
  - **Configurable resolution : 12/10/8-bit**
  - **Configurable sampling time**
- **Provide external 16 channels**
- **Support auto-sampling and trigger by external pin , internal events and software bit**
- **Data alignment for output code left/right justify**
- **Built-in input buffer stage with bypass option**
- **PGA with programmable gain : 1~4**
- **Provide internal voltage source VBUF 1.4V**
- **Optional ADC top voltage reference from external VREF+ or internal IVR24**
- **Interrupt generation at the end of sampling, end of conversion, end of sequence conversion**
- **Support voltage window detect and output code limitation**
  - **Two level programmable window threshold**
- **Built-in three channel independent hardware accumulator for ADC output code**
- **Support one-shot/channel scan/loop scan**
- **ADC data are buffered with DMA capability**
- **Support wait mode**
  - **Prevents ADC overrun in application with low frequency**
- **Support auto off mode**
  - **ADC auto power off except during the active conversion phase**
- **Built-in a temperature sensor**
  - **Temperature resolution : +/- 2 °C (Typical)**
  - **Temperature operation range : -40°C ~ 125°C**

4.1.3. ADC Control Block

The ADC control block consists of an analog multiplexer (AMUX) with 16 input channels, a **1.5M**sps/**12**-bit SAR (successive-approximation-register) ADC, reference voltage circuit, ADC conversion trigger start control block and change scan control block.

ADC Input Channels

The analog multiplexer (AMUX) selects the inputs to the ADC, allowing any of the input pins to be measured in single-ended mode.

The analog input pins used for the A/D converters also have its I/O pins for digital input and output function. In order to give the proper analog performance, a pin that is being used with the ADC should have its digital output as disabled. It is done by putting the port pin into the input-only mode. And when an analog signal is applied to the **ADC_In** pin and the digital input from this pin is not needed, software could set the corresponding pin to AIO mode to turn off the digital input buffer to reduce current consumption.

Single-End Mode

The ADC supports single-end operation modes. The ADC can convert the ADC output to unsigned code for single-end mode.

ADC Sampling Time

For input signal quality and conversion speedy issue, user can adjust the ADC sampling time. Usually increase the ADC sampling time to get more stable voltage and better ADC performance if the conversion rate and signal bandwidth are reasonable and valid for actual application.

ADC Conversion Mode

The ADC is supported three conversion modes of One Shot, Channel Scan and Loop Scan.

ADC Output Control

When an ADC conversion is complete, the ADC raw code is generated and sends to the ADC output control blocks those are including of Digital Offset Adjuster, Signed Code Converter, Digital Resolution Adjuster, Voltage Window Detector, Code Limiter and Data Alignment Adjuster.

The ADC output code will be adjusted by the ADC output control blocks and store the conversion result date to the ADC data register.

Voltage Window Detect and Code Limit

The ADC can compare the input voltage by a threshold window. Also the ADC output code can be compared by a code limit area to skip or clamp the code by the same threshold window.

ADC Data Sum Accumulate

The ADC built-in one hardware accumulator for ADC output code. The accumulator is used to accumulate the sequential ADC data with programmable data number and records the sum to the summary registers. User can set the accumulated ADC data number. The ADC is supported three sum data registers and user can get the accumulated sum from these registers.

ADC Wait and Auto-Off

The ADC supports a wait mode function to prevent ADC overrun in application with low frequency ADC sampling clock. Also ADC supports an auto off mode function to force the ADC auto entering power-off except during the active conversion phase.

4.2 I2C

4.2.1. Introduction

The I2C interface is a two-wire, bi-directional serial bus. It is ideally suited for typical microcontroller applications. The I2C protocol allows the systems designer to interconnect up to 128 different devices using only two bi-directional bus lines, one for clock (SCL) and one for data (SDA). The I2C bus provides control of SDA, SCL generation and synchronization, arbitration logic, and START/STOP control and generation. The only external hardware needed to implement this bus is a single pull-up resistor for each of the I2C bus lines. All devices connected to the bus have individual addresses, and mechanisms for resolving bus contention are inherent in the I2C protocol.

The I2C module builds in the shadow buffer and data register to improve transmit and receive communication performance.

4.2.2. Features

- **Provide I2c modules : I2C0**
- **Support master and slave mode**
- **Support programmable clock rate control and clock rate up to 1 MHz**
- **Support programmable high/low period control for master mode**
- **Support clock stretching for slave mode**
- **Support general call function**
- **Support multi-master processing capability**
- **Support both Byte mode and Buffer mode flow control**
- **Support Byte mode bus event code for simplex firmware control**
- **Support Buffer mode 4-byte data buffer and 32-bit data register for high speed communication**
- **Received and transmitted data are buffered with DMA capability**

- **Support slave address hardware detection wakeup from STOP mode**
- **Support SMBus timeout detection**

4.2.3. I2C Control

- **I2C Data Byte Mode Control**

  The module is provides one bus event register to get the I2C Event Code for software byte-mode simplex control. An 8-bit shift buffer and an 8-bit data register are using for the I2C data Byte mode.

- **I2C Data Buffer Mode Control**

  The module implements an 8-bit shift buffer, a 32-bit shadow buffer and a 32-bit data register for data flow control of data Buffer mode..

- **I2C Master Timing Control**

  Two timing control registers are simply used to configure the I2C timing of high and low cycle time.

- **I2C Timeout Timer Control**

  The module is provides one 8-bit timeout timer (TMO) for I2C access time-out control.

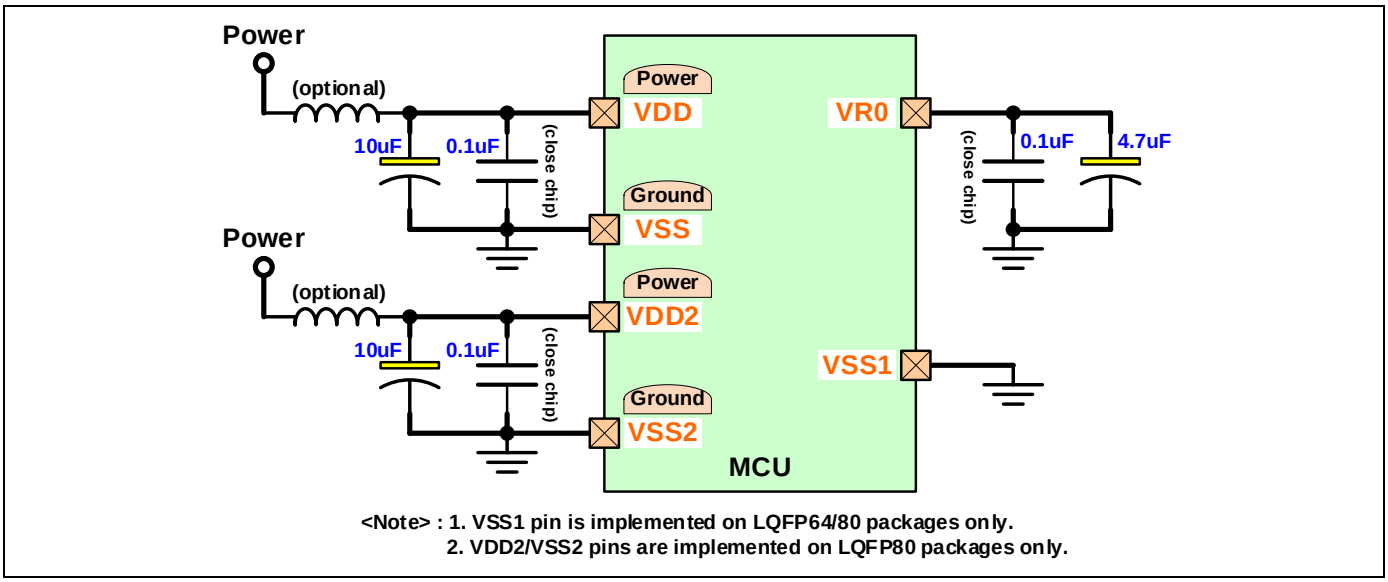
5 Application Notes

5.1. Power Supply Circuit

To have the chip work with power supply varying from 1.8V to 5.5V, adding some external decoupling and bypass capacitors is necessary on **VDD/VSS** power pins, as shown in following figure. Also the same application suggestion on **VDD2/VSS2** power pins for LQFP80 package. The **VR0** pin is the embedded LDO voltage output as internal core logic power supply. It needs to place one 0.1uF capacitor and one 4.7uF capacitor to be closed the pin.

The following figure is showing the power supply suggestion circuit.

Figure 5-2. Power Supply Circuit



<Note> : 1. VSS1 pin is implemented on LQFP64/80 packages only.
2. VDD2/VSS2 pins are implemented on LQFP80 packages only.

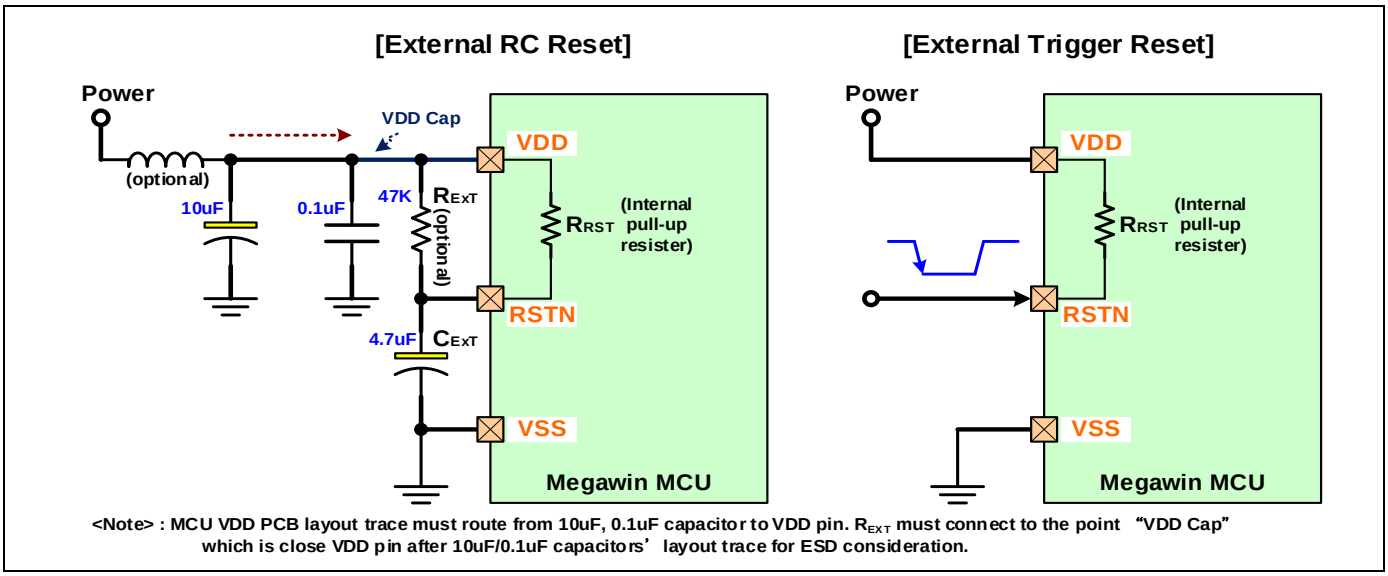
5.2. Reset Circuit

Normally, the power-on reset can be successfully generated during power-up. However, to further ensure the MCU a reliable reset during power-up, the external reset is necessary. The following figure shows the external reset circuit, which consists of a capacitor C_{EXT} connected to **VSS** (ground) and a resistor R_{EXT} connected to **VDD** (power supply).

In general, R_{EXT} is optional because the **RSTN** pin has an internal pull-high resistor (R_{RST}). This internal diffused resistor to **VDD** permits a power-up reset using only an external capacitor C_{EXT} to **VSS**.

Strongly suggestion, the **RSTN** pin must set to output mode if it is used to do as both chip reset and GPIO functions in application. In this condition, the pin input low may make chip reset locked error if it set to GPIO input mode.

Figure 5-3. Reset Circuit



<Note> : MCU VDD PCB layout trace must route from 10uF, 0.1uF capacitor to VDD pin. R_{EXT} must connect to the point "VDD Cap" which is close VDD pin after 10uF/0.1uF capacitors' layout trace for ESD consideration.

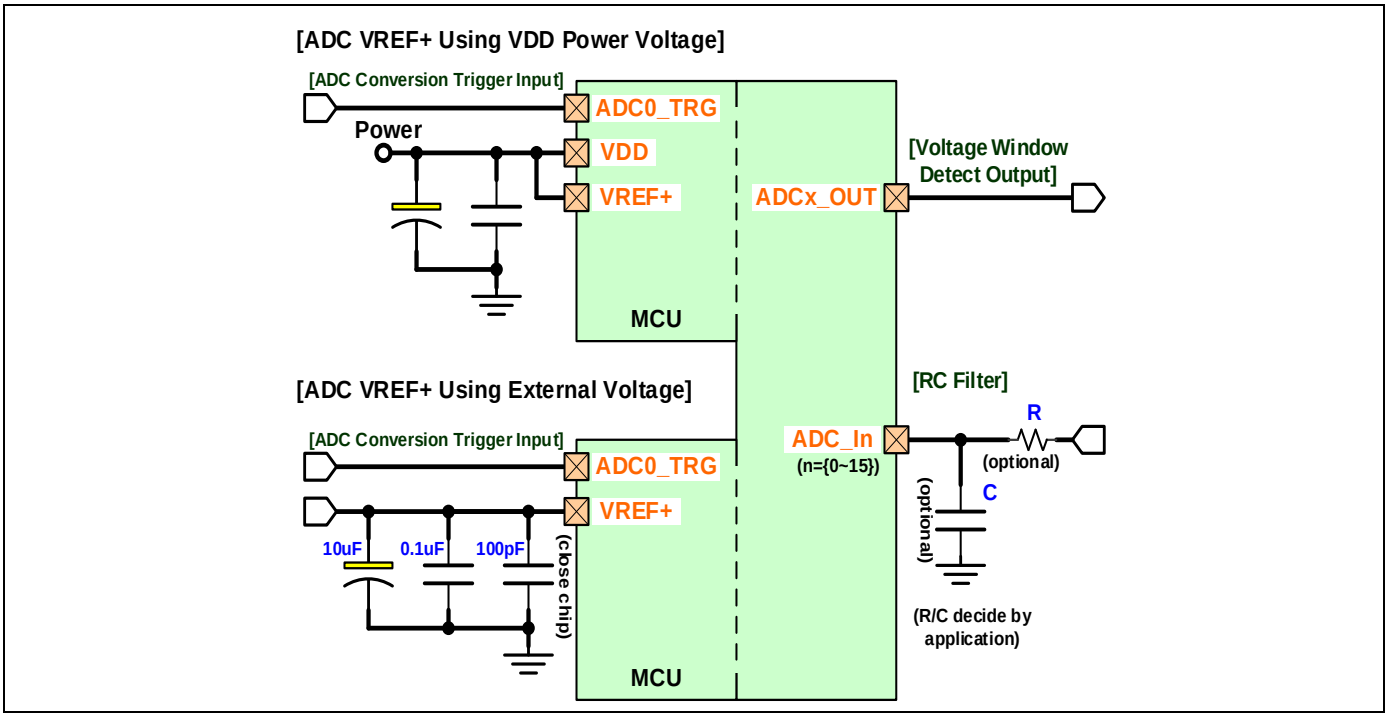
5.3. ADC Application Circuit

The ADC reference voltage source can be from (1) VDD power by connecting **+VREF** pin to **VDD** pin directly (2) external quiet reference voltage source.

When uses the VDD power as the ADC reference voltage, it must connect **+VREF** pin trace to the point which is at current flow behind the power capacitor(s). When uses the external reference voltage source as the ADC reference voltage, it must add some decoupling and bypass capacitors, as shown in following figure.

An optional **ADCx_TRG** pin is able to input the trigger signal for ADC input conversion and an optional **ADCx_OUT** pin is used to output the internal ADC window detection status.

Figure 5-3. ADC Application Circuit



6 Electrical Characteristics

6.1. Parameter Glossary

Table 6-1. Parameter Glossary

Symbol	Definition	Descriptions
Abbreviations for electrical characteristics		
Min	Minimum value	Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value.
Max	Maximum value	Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value.
Typ	Typical value	Unless otherwise specified, the value is based on TA=25 °C, VDD=5V.
VDD	Power supply voltage	The voltage range is specified in characteristics table or conditions column.
VSS	Power reference voltage	Unless otherwise specified, all voltages are referred to VSS.
TA	Ambient temperature	The temperature range is specified in characteristics table or conditions column.
T_{PC}	Peripheral clock cycle time	The peripheral input clock source may select APB, SYS or other clock. This clock frequency needs lower than 1/2 of the module process clock frequency.

6.2. Absolute Maximum Rating

Table 6-2. Absolute Maximum Rating

Parameter	Rating	Unit
Ambient temperature under bias	-40 ~ +105	**°C**
Storage temperature	-65 ~ + 150	**°C**
Voltage on any Port I/O Pin or RST with respect to VSS	-0.5 ~ VDD + 0.5	**Volt**
Voltage on VDD with respect to VSS	-0.5 ~ +6.0	**Volt**
Maximum total current through VDD and VSS	200	**mA**
Maximum output current sunk by any I/O pin	40	**mA**

Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

6.3. IO Characteristics

Table 6-3. IO Characteristics

VSS=0V, TA = 25 °C and execute NOP for each CPU cycle (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	Input High voltage	Except RSTN,XIN/XOUT pins	0.6			VDD
V_{IH_XOSC}	Input High voltage (XIN)	XIN pin GPIO mode	0.75			VDD
V_{IH_RST}	Input High voltage (RSTN)	RSTN pin reset/GPIO mode	0.75			VDD
V_{IL}	Input Low voltage	Except RSTN,XIN/XOUT pins			0.15	VDD
V_{IL_XOSC}	Input Low voltage (XIN)	XIN pin GPIO mode			0.2	VDD
V_{IL_RST}	Input Low voltage (RSTN)	RSTN pin reset/GPIO mode			0.2	VDD
	VDD=5.0V					
I_{IH}	Input High Leakage current	V_{PIN} = VDD		0.02	0.1	uA
I_{IL}	Input Low Leakage current	V_{PIN} = 0.4V		0.01	0.1	uA
I_{H2L}	Logic 1 to 0 input transition current (quasi-bidirectional or input mode with on-chip pull-up resistor)	V_{PIN} = 2.2V (V_{IH} voltage)		250	500	uA
I_{OH1}	Output High current (push-pull output mode & Full level)	VDD=5.0V, V_{PIN} = 2.4V		38.5		mA
I_{OH2}	Output High current (push-pull output mode & 1/2 level)	VDD=5.0V, V_{PIN} = 2.4V		19.8		mA
I_{OH3}	Output High current (push-pull output mode & 1/4 level)	VDD=5.0V, V_{PIN} = 2.4V		10.1		mA
I_{OH4}	Output High current (push-pull output mode & 1/8 level)	VDD=5.0V, V_{PIN} = 2.4V		5.2		mA
I_{OL1}	Output Low current(Full level)	VDD=5.0V, V_{PIN} = 0.4V		30.4		mA
I_{OL2}	Output Low current(1/2 level)	VDD=5.0V, V_{PIN} = 0.4V		15.7		mA
I_{OL3}	Output Low current(1/4 level)	VDD=5.0V, V_{PIN} = 0.4V		8.0		mA
I_{OL4}	Output Low current(1/8 level)	VDD=5.0V, V_{PIN} = 0.4V		4.0		mA
R_{PU}	IO pin pull-high resistance	Except RSTN		13.3		Kohm
R_{RST}	Internal reset pull-high resistance	RSTN pin		250		Kohm
TR1	IO rising time (Normal mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		13.7		ns
TR2	IO rising time (Normal mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		28.9		ns
TR3	IO rising time (High speed mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		5.58		ns
TR4	IO rising time (High speed mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		26.8		ns
TR5	IO rising time (XOUT GPIO mode)	C load=30pF		5.60		ns
TR6	IO rising time (XIN GPIO mode)	C load=30pF		5.29		ns
TR7	IO rising time (RSTIN GPIO mode)	C load=30pF		7.36		ns
TF1	IO falling time (Normal mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		13.7		ns
TF2	IO falling time (Normal mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		16.45		ns
TF3	IO falling time (High speed mode	Except RSTN,XIN/XOUT pins		3.2		ns

	and IO output drive strength is Full level)	C load=30pF				
TF4	IO falling time (High speed mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**9.65**		**ns**
TF5	IO falling time (XOUT GPIO mode)	C load=30pF		**3.1**		**ns**
TF6	IO falling time (XIN GPIO mode)	C load=30pF		**2.6**		**ns**
TF7	IO falling time (RSTIN GPIO mode)	C load=30pF		**3.0**		**ns**
	VDD=3.3V					
I_{IH}	Input High Leakage current	V_{PIN} = VDD		**0.02**	**0.1**	**uA**
I_{IL}	Input Low Leakage current	V_{PIN} = 0.4V		**0.01**	**0.1**	**uA**
I_{H2L}	Logic 1 to 0 input transition current (quasi-bidirectional or input mode with on-chip pull-up resistor)	V_{PIN} = 1.6V (V_{IH} voltage)		**115**	**150**	**uA**
I_{OH1}	Output High current (push-pull output mode & Full level)	VDD=3.3V, V_{PIN} = 2.4V		**13**		**mA**
I_{OH2}	Output High current (push-pull output mode & 1/2 level)	VDD=3.3V, V_{PIN} = 2.4V		**6.5**		**mA**
I_{OH3}	Output High current (push-pull output mode & 1/4 level)	VDD=3.3V, V_{PIN} = 2.4V		**3.5**		**mA**
I_{OH4}	Output High current (push-pull output mode & 1/8 level)	VDD=3.3V, V_{PIN} = 2.4V		**1.7**		**mA**
I_{OL1}	Output Low current(Full level)	VDD=3.3V, V_{PIN} = 0.4V		**22**		**mA**
I_{OL2}	Output Low current(1/2 level)	VDD=3.3V, V_{PIN} = 0.4V		**11.3**		**mA**
I_{OL3}	Output Low current(1/4 level)	VDD=3.3V, V_{PIN} = 0.4V		**5.6**		**mA**
I_{OL4}	Output Low current(1/8 level)	VDD=3.3V, V_{PIN} = 0.4V		**2.8**		**mA**
R_{PU}	IO pin pull-high resistance	Except RSTN		**19.5**		**Kohm**
R_{RST}	Internal reset pull-high resistance	RSTN pin		**426**		**Kohm**
TR1	IO rising time (Normal mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		**19.4**		**ns**
TR2	IO rising time (Normal mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**38.4**		**ns**
TR3	IO rising time (High speed mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		**7.7**		**ns**
TR4	IO rising time (High speed mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**35.5**		**ns**
TR5	IO rising time (XOUT GPIO mode)	C load=30pF		**7.0**		**ns**
TR6	IO rising time (XIN GPIO mode)	C load=30pF		**7.3**		**ns**
TR7	IO rising time (RSTIN GPIO mode)	C load=30pF		**11.3**		**ns**
TF1	IO falling time (Normal mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		**19.9**		**ns**
TF2	IO falling time (Normal mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**21.8**		**ns**
TF3	IO falling time (High speed mode and IO output drive strength is Full level)	Except RSTN,XIN/XOUT pins C load=30pF		**3.66**		**ns**
TF4	IO falling time (High speed mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		**12.76**		**ns**
TF5	IO falling time (XOUT GPIO mode)	C load=30pF		**4.2**		**ns**
TF6	IO falling time (XIN GPIO mode)	C load=30pF		**3.1**		**ns**
TF7	IO falling time (RSTIN GPIO mode)	C load=30pF		**3.8**		**ns**

6.4. ADC Characteristics

Table 6-4. ADC Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C, C_{LOAD}=10pF, Gain=x1 (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
VDDA	Analog Supply Voltage		2.4	5.0	5.5	Volt
I_{ADC_ON}	Operation Current - normal			1200		uA
I_{ADC_OFF}	Operation Current - power-down			0.1		uA
ADC Static Parameters						
Bits	Resolution				12	bits
INL	Integral nonlinearity (INL)	VREF = 5V, VDD = 5V, 1.5Msps Conversion Rate (sampling clock = 36 MHz/24 clocks)		±7		LSB
INL	Integral nonlinearity (INL)	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 24 MHz/24 clocks)		±6		LSB
INL	Integral nonlinearity (INL)	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 30 MHz/30 clocks)		±6		LSB
DNL	Differential nonlinearity (DNL)	VREF = 5V, VDD = 5V, 1.5Msps Conversion Rate (sampling clock = 36 MHz/24 clocks)	-1	2.5		LSB
DNL	Differential nonlinearity (DNL)	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 36 MHz/24 clocks)	-1	2.5		LSB
DNL	Differential nonlinearity (DNL)	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 48 MHz/30 clocks)	-1	2.5		LSB
E_{OFFSET}	Offset error	VREF = 5V, VDD = 5V, 1.5Msps Conversion Rate (sampling clock = 36 MHz/24 clocks)		±4		LSB
E_{OFFSET}	Offset error	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 24 MHz/24 clocks)		±4		LSB
E_{OFFSET}	Offset error	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 30 MHz/30 clocks)		±4		LSB

E_{FS}	Full scale error	VREF = 5V, VDD = 5V, 1.5Msps Conversion Rate (sampling clock = 36 MHz/24 clocks)		±14		LSB
E_{FS}	Full scale error	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 24 MHz/24 clocks)		±10		LSB
E_{FS}	Full scale error	VREF = 5V, VDD = 5V, 1Msps Conversion Rate (sampling clock = 30 MHz/30 clocks)		±10		LSB
	ADC Input and DC Characters					
V_{AIN}	ADC input voltage range (Single Ended)	gain = 1.0	0		Vref	Volt
C_{LOAD}	Input capacitance			5		pF
V_{XREF}	External ADC reference voltage		2.4		VDDA	Volt
VDD_{IREF}	Supply Voltage range for V_{IREF}		2.7		5.5	Volt
V_{IREF}	Internal ADC reference voltage	-40 °C < < 105 °C		2.40		Volt
	Internal ADC reference voltage spread over the temperature range	-40 °C < < 105 °C V_{IREF} =2.40V at 25°C		40		mV
V_{BUF}	Internal VBUF reference voltage	-40 °C < < 105 °C	1.38	1.40	1.42	Volt
	Internal VBUF reference voltage spread over the temperature range	-40 °C < < 105 °C V_{BUF} =1.40V at 25°C		30		mV
TADEN	ADC enable time			5		us
	ADC Conversion Parameters					
Fs	Sampling clock				48	MHz
F_{Conv}	Conversion rate	VDDA = 5.5 ~ 4.0 V			1500	Ksps
		VDDA = 4.0 ~ 2.4 V			1000	Ksps
T_{Conv}	Conversion time in conversion clock (not including acquisition time)	ADC0_CONV_TIME=0		24		clocks
		ADC0_CONV_TIME=1		30		clocks

6.5. ADC PGA Characteristics

Table 6-5. ADC PGA Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
	Supply Range					
VDDA	Analog Supply Voltage		2.4	5.0	5.5	Volt
	DC Characteristics					
V_{OS2}	input offset voltage	With Calibration Gain=x1	-6		10	mV
V_{CM_IN}	Input Common-mode Voltage	VDDA>3.0V,Gain=x1,as a unit gain buffer	0.03		VDDA/2+0.5	V
		VDDA<3.0V,Gain=x1,as a unit gain buffer	0.03		VDDA/2	V
IQ	Ground Current	VDDA=5.0V, VIN= VDDA/2; VOUT=VDDA/2, Gain=x1 (RFB=120KΩ current Not included when Gain=x1)		1150		uA
	AC Characteristics					

SR	Slew rate (*1)	Normal Operation		**3.5**		**V/us**
UGF	PGA Bandwidth Frequency (*2)	Normal Operation		**10**		**MHz**

(*1) Data guaranteed by design, not tested in production.

(*2) The UGF will be divided by the GAIN setting. (ex: Ideal UGF will be 10MHz/4 when PGA gain=4)

6.6. I2C Characteristics

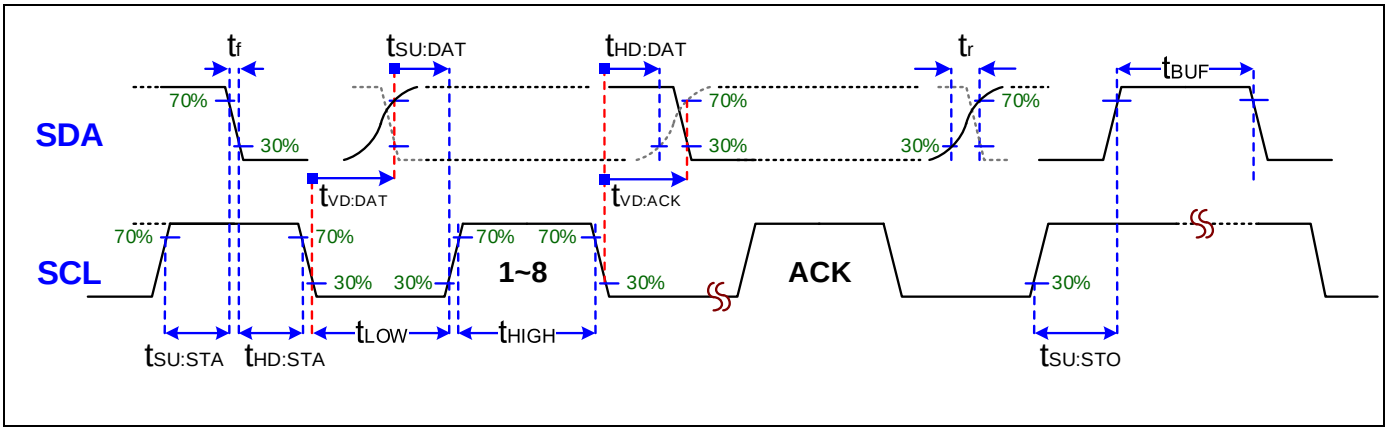
Table 6-6. I2C Characteristics

VDD=5.0V±10%, VSS=0V, TA = -40°C ~ +105°C (unless otherwise specified)

Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100	0	400	0	1000	KHz
t_{Low}	Low period of the SCL clock		4.7		1.3		0.5		us
t_{Low_M}	Low period of the SCL clock (Master Mode)		2		2		2		T_{PC}
t_{Low_S}	Low period of the SCL clock (Slave Mode)		4		4		4		T_{PC}
t_{High}	High period of the SCL clock		4.0		0.6		0.26		us
t_{High_M}	High period of the SCL clock (Master Mode)		3		3		3		T_{PC}
t_{High_S}	High period of the SCL clock (Slave Mode)		5		5		5		T_{PC}
$t_{HD;STA}$	Hold time for START condition		4.0		0.6		0.26		us
$t_{SU;STA}$	Setup time for START condition		4.7		0.6		0.26		us
$t_{HD;DAT}$	Data hold time		0		0		0		us
$t_{SU;DAT}$	Data setup time		250		100		50		ns
$t_{SU;STO}$	Setup time for STOP condition		4.0		0.6		0.26		us
t_{BUF}	Bus free time between a STOP and START		4.7		1.3		0.5		us
$t_{VD;DAT}$	Data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	Data valid acknowledge time			3.45		0.9		0.45	us
t_r	Rise time of both SDA and SCL signals			1000		300		120	ns
t_f	Fall time of both SDA and SCL signals			300	20x (VDD/5.5V)	300	20x (VDD/5.5V)	120	ns
C_i	Capacitive load for each IO pin			10		10		10	pF

T_{PC} : APB clock or SYS clock cycle time

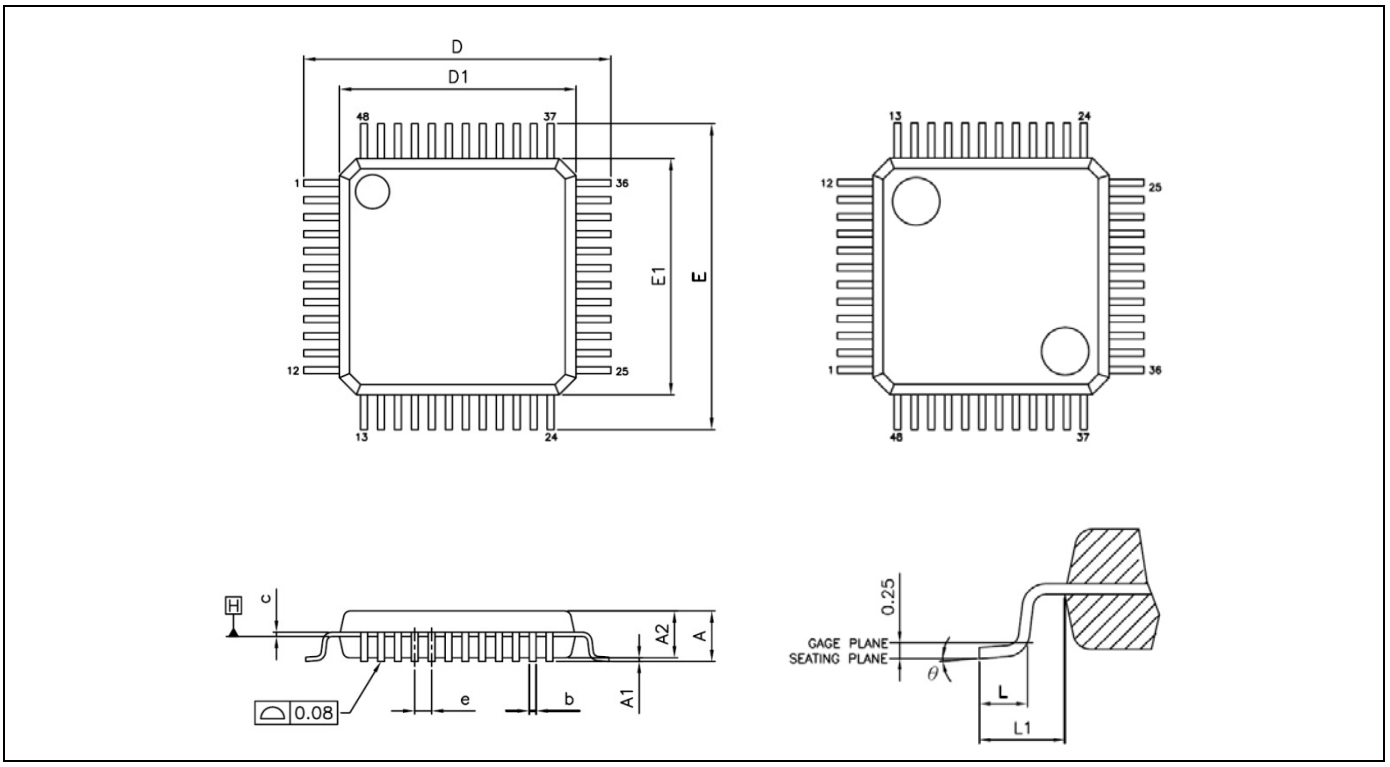
Figure 6-1. I2C Timing Waveform



7 Package Dimension

7.1. LQFP-48

Figure 7-1. LQFP-48 (7mm X 7mm) ~ AD48



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	1.60	---	---	0.062
A1	0.05	---	0.15	0.001	---	0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.006	0.008	0.010
c	0.09	---	0.20	0.003	---	0.007
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.275 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.275 BSC		
e	0.50 BSC			0.019 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

8 Revision Histories

Revision V0.10 (2024_1223)		Chapter
1	Preliminary version	