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M0-Based MCU

MG32F02A032
Data Sheet

Version: 1.81

Features

❖ CPU Core

- ARM 32-bit Cortex-M0 CPU
- Operation frequency up to 48MHz
- Built-in one NVIC for 32 external interrupt inputs with 4-level priority
- Built-in one 24-bit system tick timer
- Built-in one single-cycle 32-bit multiplier
- Built-in one SWD serial wire debugger with 2 watch points and 4 breakpoints

❖ Flash Memory

- Built-in embedded 32K bytes flash memory for application code
- Support ICP (In-circuit program) for ISP boot code update through SWD interface
- Support ISP (In-system program) for application code update
  - Support programmable ISP flash memory size for ISP boot code
- Support IAP (In-application program) for application data update
  - Support programmable IAP flash memory size

❖ SRAM Memory

- Built-in embedded 4K bytes SRAM

❖ Power

- Built-in two brown-out detectors
  - BOD0 detect 1.7V
  - BOD1 detect by selected level 4.2V/3.7V/2.4V/2.0V
- Built-in a power management controller with power-down and wakeup control
- Support three power operation modes
  - ON(Normal) mode and SLEEP , STOP power down modes
- Support wake-up from SLEEP/STOP modes via multiple sources

❖ Reset

- Built-in embedded POR(power-on reset) circuit
- Built-in one reset source controller
  - Programmable chip cold reset and warm reset for reset source
  - Independent software reset control for internal modules
- Provide multiple reset source
  - POR/BOD0/BOD1/External reset pin input/Software force reset
  - IWDT/WWDT/ADC/Analog Comparator
  - Illegal address error reset/Flash access protect error reset
  - Missing clock detect (MCD) reset

❖ Clock

- Built-in embedded ILRCO (internal low frequency RC oscillator) by 32KHz
- Built-in embedded IHRCO (internal high frequency RC oscillator)
  - Trimmed to 11.059 or 12MHz ±1% at +25℃
- Built-in embedded PLL clock output for system clock
- Built-in embedded XOSC oscillator with MCD for external 32KHz and 4 ~ 25MHz Xtal
- Support external clock input up to 36MHz
- Built-in a clock source controller with independent clock enable control for modules
- Support internal XOSC oscillator and internal ILRCO/IHRCO clock output

❖ DMA (Direct Memory Access)

- One configurable channels with dedicated hardware DMA requests
  - Access to Memory, APB and AHB Peripherals as source and destination
  - Support SRAM/Flash as memory source and SRAM as memory destination
  - Peripherals are including of ADC0, I2Cx, URTx, SPIx, TM36 and GPL modules

- DMA transfer management type
  - memory-to-memory
  - peripheral-to-memory
  - memory-to-peripheral
  - peripheral-to-peripheral
- Programmable transfer number of data and up to 65536
- Programmable burst length 1,2,4
- Support transfer loop mode and start address auto reload control
- Provide single/block/demand mode for external pin trigger request

❖ GPIO

- Support general purpose IO pins for application
  - Maximum 44 GPIO pins for LQFP48 package
  - Maximum 29 GPIO pins for QFN32 package
  - Maximum 17 GPIO pins for TSSOP20 package
- Provide selectable IO modes by pin independent
  - Push-Pull output
  - Quasi bidirectional
  - Open-drain output
  - Digital Input with high impedance
  - Analog IO
- Flexible pin alternate function selection
- Support programmable drive strength by pin independent
- Support IO deglitch filter by pin independent
- Support input inverse selection by pin independent
- Support pull-high option by pin independent
- Support high speed option by pin independent except RSTN,XIN
- GPIO pin state and IO mode setting keep optional after reset

❖ Interrupt Support

- Built-in one EXIC (external interrupt controller) for NVIC connection
  - Independent high/low level and rising/falling edge trigger selection
- Built-in one WIC (wakeup interrupt controller) for wakeup event control
- All PA/PB/PC/PD pins can be configured as interrupt source and key pad input
  - Support port OR logic for interrupt function
  - Support port AND logic for KBI function
- Support external pins for CPU NMI/RXEV/TXEV function

❖ Timer

- Provide five timers/counters : TM00,TM01,TM10,TM16,TM36
- Support multi-level timer modules for different application
- Timer module common functions
  - Selectable Full-counter, Cascade, Separate timer operation modes
  - Multiple internal and external signals as timer clock source or trigger source
  - Support timer reset, trigger start and clock gating for trigger source function
  - Timer overflow as clock output to external pin output
  - Auto-stop mode by main counter counting
- Provide TM36 timer module
  - 32-bit timer/counter
  - 4 CCP (input Capture/output Compare/PWM) channels
  - 3 CCP channels with OCN (complementary output compare)
  - PWM function with center/edge-align, dead time control and break control
  - QEI(Quadrature Encoder Interface) support

- One IC and three OC with DMA capability
- External input timer up/down control(TM36 only)

- **Provide TM1x timer modules (TM10,TM16)**
  - 32-bit timer/counter
- **Provide TM0x timer modules (TM00,TM01)**
  - 16-bit timer/counter

❖ RTC

- **Built-in 32-bit counter with selectable clock source**
- **Support alarm function and time-stamp function**
  - Support alarm function with 32-bit programmable compare register
- **Support wakeup from STOP mode**
- **Support periodic timer tick interrupt or wakeup**

❖ Watchdog Timer

- **Built-in one IWDT (Independent Watch Dog Timer)**
  - 8-bit down counter with 12-bit prescaler and clocked by ILRCO clock
  - Operating capability in SLEEP and STOP modes
  - Selectable reset or interrupt when the counter underflow
  - Support two early wakeup comparators with interrupt
- **Built-in one WWDT (Window Watch Dog Timer)**
  - 10-bit counter with 1 or 256 divider , 1/2/4~/128 divider
  - Configurable time-window to detect abnormally late or early application behavior
  - Selectable reset or interrupt when the counter is underflow or reloaded outside the window
  - Support warning interrupt

❖ I2C

- **Provide one I2c module : I2C0**
- **I2C module common functions**
  - Support master and slave mode
  - Support programmable clock rate control and clock rate up to 1 MHz
  - Support programmable high/low period control for master mode
  - Support clock stretching for slave mode
  - Support general call function
  - Support multi-master processing capability
  - Support both Byte mode and Buffer mode flow control
  - Support Byte mode bus event code for simplex firmware control
  - Support Buffer mode 4-byte data buffer and 32-bit data register for high speed communication
  - Received and transmitted data are buffered with DMA capability
  - Support slave address hardware detection wakeup from STOP mode
  - Support SMBus timeout detection

❖ UART

- **Provide two identical UART modules : URT0,URT1**
- **UART module common functions**
  - Support UART, Synchronous, SPI master, SmartCard, LIN, Multi-processor modes
  - Provide precise UART baud-rate control by programmable oversampling rate
  - Support baud rate up to 6 Mbit/s
  - Programmable data word length - 7 or 8 bits
  - Selectable MSB or LSB first data order
  - Configurable stop bits - 0.5,1,1.5 or 2 stop bits
  - Hardware parity checking and parity generation
  - Programmable 4~32 oversampling rate
  - Swappable TX/RX pin configuration

- Separate signal polarity control for transmission and reception
- Support a timeout timer for Idle/RX/Break/Calibration timeout detection
- Support 4-byte data buffer and 32-bit data register for high speed communication
- Received and transmitted data are buffered with DMA capability
- Support auto baud-rate detection and calibration
- Support multiprocessor communication for master and slave mode - Idle-Line , Address-Bit
- Support low speed UART-like frame format IrDA
- Support transceiver hardware flow control by CTS/RTS signals only
- Provide driver enable signal to activate the transmission for bidirectional communication
- Support transmission-error hardware detection and auto resent control for Smart-card application
- Support receiving parity error hardware detection and auto retry control for Smart-card application

❖ SPI

- **Provide three modules for SPI communication: SPI0, URT0, URT1**
  - Provide one advanced SPI module: SPI0
  - Provide two configurable SPI modules: URT0, URT1 (Refer to UART features)
- **Support master and slave mode**
  - Support full duplex , half duplex or simplex communication mode
  - Support data communication without NSS(slave select signal)
- **Support programmable clock rate control**
  - Support clock rate up to 24 MHz for master, 16MHz for slave
- **Selectable 4~32-bit frame size**
  - Support 4-byte data buffer and 32-bit data register for high speed communication
- **Received and transmitted data are buffered with DMA capability**
- **Support multi-master processing capability**
- **Selectable clock polarity and phase**
- **Selectable MSB or LSB first data order**
- **NSS line management by hardware or software for master mode**
- **Configurable data transfer modes**
  - Standard SPI mode (separated transmit and receive line)
  - Single SPI mode with bidirectional data transfer
  - Dual SPI mode with bidirectional data transfer
  - Quad SPI mode with bidirectional data transfer
- **Data transmit/receive overrun detect**

❖ ADC

- **12-bit SAR ADC with 800Ksps**
  - Configurable resolution : 12/10/8-bit
  - Configurable sampling time
- **Provide external 12 channels and internal 4 channels input**
  - Internal extra channel source : VBUF , VSSA , LDO VR0 output , VREF+
- **Support auto-sampling and trigger by external pin, internal events and software bit**
- **Data alignment for output code left/right justify**
- **PGA with programmable gain : 1~4**
- **Interrupt generation at the end of sampling, end of conversion, end of sequence conversion**
- **Support voltage window detection and output code limitation**
- **Built-in three channel independent hardware accumulators for ADC output code**
- **Support one-shot/channel scan/loop scan**
- **ADC data are buffered with DMA capability**
- **Support wait mode to prevent ADC overrun**

❖ Analog Comparator

- **Provide 2 fast Rail-to-rail comparators**

- Programmable 64-step threshold of internal voltage reference
- Provide external total 6 channels input for all comparators
- Programmable input hysteresis voltage
- Programmable response time for optimal current consumption
- Selectable compare output polarity
- Support wakeup from SLEEP and STOP modes
- Support analog watch dog as a reset source

❖ GPL (General Purpose Logic)

- Support data inverse, bit order change, byte order change and parity check
  - Data bit order change for 8/16/32-bit reverse
  - Data byte order change between Little endian and Big endian for 16/32-bit range
  - Parity Check for 8/16/32 bit range
- Support CRC (Cyclic Redundancy Check) calculation
  - Programmable CRC initial value
  - CRC output bit order change
- CRC with fixed common polynomial
  - CRC8 polynomial 0x07
  - CRC16 polynomial 0x8005
  - CCITT16 polynomial 0x1021
  - CRC32(IEEE 802.3) polynomial 0x4C11DB7
- Input data are buffered with DMA capability

❖ Misc.

- Timer synchronous enable global control
- OBM(Output Signal Break and Modulation) control
  - Support two sets of OBM for output signal break and modulation control
- 32-bit non-reset backup register
- Provide on chip 16 bytes Unique ID code

❖ Operating

- Operating voltage range 1.8V ~ 5.5V
- Operating temperature range -40℃ ~ 125℃ (**1)
- Operating frequency range up to 48MHz

❖ Package Types

- LQFP48 / QFN32 / TSSOP20

(1): Tested by sampling.**

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1. General Description

The **MG32F02A** is a single-chip 32-bit microcontroller based on a high performance Core ARM® 32-bit Cortex®-M0 CPU with embedded Nested Vectored Interrupt Controller (NVIC).

The **MG32F02A** has up to **32K** bytes of embedded main flash memory for code and data, programmable memory size of embedded system flash memory for boot load code and 64 bytes of embedded option-byte flash memory for chip configuration. The all flash memory can be programmed either in serial writer mode (ICP, In-Circuit-Programming). Also, the main flash memory can be programmed in ISP (In-System Programming) mode or SRAM (Boot on SRAM) mode. ICP and ISP allow the user to download new code without removing the microcontroller from the actual end product; IAP means that the device can write non-volatile data in the flash memory while the application program is running. There needs no external high voltage for programming due to its built-in charge-pumping circuitry.

The **MG32F02A** retains all features of the ARM® 32-bit Cortex®-M0 with **4K** bytes of SRAM, **4** I/O ports, **32** external interrupts source with 4-level interrupt controller and seven 8/16-bits timer/counters. In addition, the **MG32F02A** has a System Tick Timer, two Watchdog Timers, three advance timer modules with IC/OC, four Basic timer modules for universal using, on-chip crystal oscillator for 32.768 KHz to 25MHz, two high precision internal oscillators IHRCO for 11.059/12MHz and ILRCO for 32 KHz, one 12-bit ADC and two analog comparators with programmable threshold.

Also, the **MG32F02A** support multiple and flexible communicate interface for production application. It provides alternate function pins those are including of GPIO, I2C, SPI, KBI, UART, SmartCard, LIN and SWD(on chip debug). It has maximum **44** GPIO pins and provides programmable IO type - quasi-bidirectional , push-pull output , open-drain output , input only(Hi-z) with optional pull-high. In addition, it is built-in internal de-bounce circuit to deglitch noise for worse signals.

One direct memory access (DMA) controller is used to improve data transfer between peripherals and memory and memory to memory. The data can be transfer by DMA controller and does not cost any CPU time.

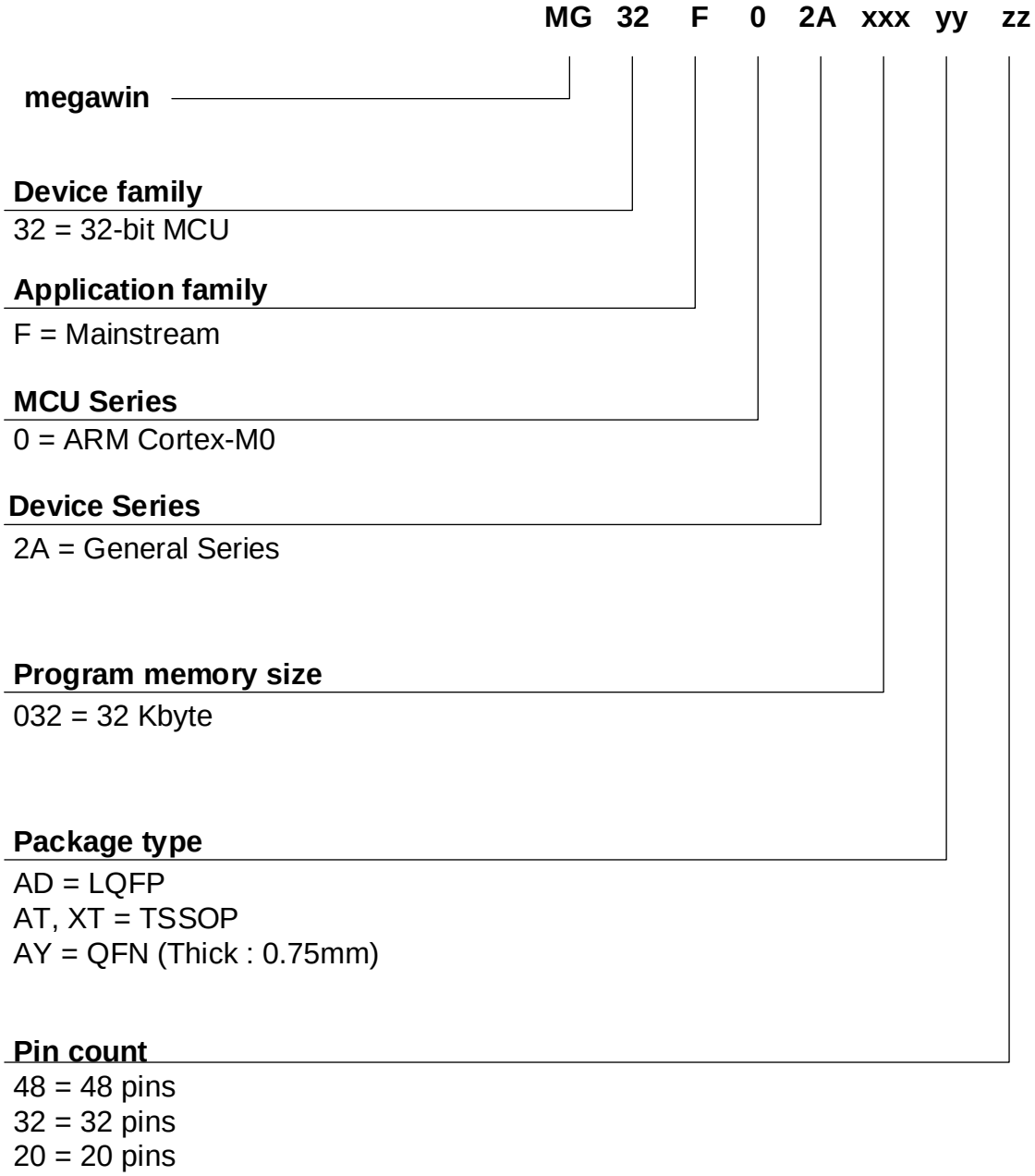
For power management and reset control, the **MG32F02A** is built-in a power supervisor including of a Low Voltage Detector(LVD), two Brown-out Detectors(BOD0/BOD1), a Power-On Reset(POR) , a Low-voltage Reset(LVR). The **MG32F02A** has multiple power-down modes to reduce the power consumption: Sleep mode and Stop mode.

In the Sleep mode the CPU is frozen while the peripherals and the interrupt system are still operating. In the Stop mode the RAM and SFRs' value are saved and all other functions are inoperative; most importantly, in the Sleep mode the chip can be waked up by many interrupt or reset sources(POR/LVR/BOD0/BOD1).

2. Order Information

Please contact the megawin sales for available options (memory size, package …) and more information about this device.

Figure 2-1. Part Numbering



- **Chip Selection**

Table 2-1. Chip Selection Table

Chip Number	MG32F02A032	Comment
Flash ROM	32KB	memory space of AP+IAP+ISP
SRAM	4KB	
Max. CPU Frequency	48MHz	
Internal Clock Source	ILRCO+IHRCO	12MHz(default) & 11.059MHz option for IHRCO
Voltage Detector	LVR+BOD0/1	
IO Number	44/29/17	
Timers	16-bit*2 + 32-bit*3	support Full-Counter, Cascade , Separate modes
IC/OC/PWM	4-CH	OC support (normal + complement output)
WDT	IWDT + WWDT	
RTC	yes	
ADC	12-Bit , 12-CH	embedded one input buffer with PGA
Analog Comparator	2	embedded two R-ladder voltage reference
UART	2	support SPI master,Multi-processor,IrDa,LIN,ISO-7816 (SmartCard),Hardware flow control
SPI	1	Support 1/2/4/8 data line modes
I2C	1	optional Byte/Buffer mode
ISO-7816-3	2 (*1)	included and shared in UART module (SmartCard)
LIN	2 (*1)	included and shared in UART module
DMA	1-CH	memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
CRC	yes	
Package	LQFP48 QFN32 TSSOP20	
Operation Voltage	1.8~5.5V	-40°C ~ 125°C
ICP	yes	In-Chip-Programming
ISP	yes	In-System-Programming ISP flash memory is included in the same space of embedded flash memory
IAP	yes	In-Application-Programming IAP flash memory is included in the same space of embedded flash memory

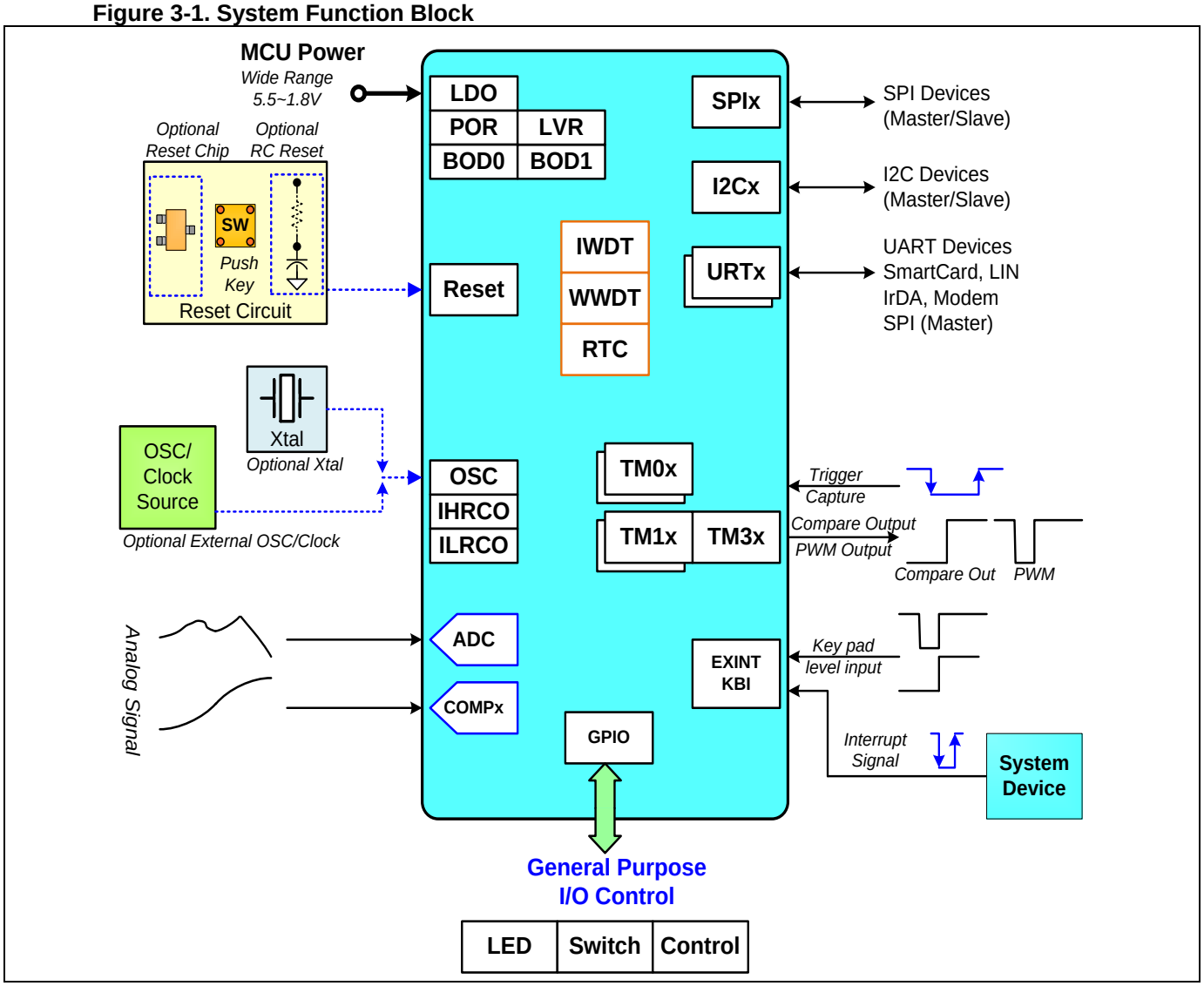
- **Part Number List**
  - **MG32F02A032AD48 : LQFP48 (7mm x 7mm), 32KB Flash, -40°C ~ 105°C**
  - **MG32F02A032AY32 : QFN32 (5mm x 5mm), 32KB Flash, -40°C ~ 105°C**
  - **MG32F02A032AT20 : TSSOP20 (6.5 x 4.4 x1.0 mm), 32KB Flash, -40°C ~ 105°C**
  - **MG32F02A032XT20 : TSSOP20 (6.5 x 4.4 x1.0 mm), 32KB Flash, -40°C ~ 125°C**

3. Block Diagram

3.1. System Function Block

The following diagram is showing the system function block for application.

Figure 3-1. System Function Block

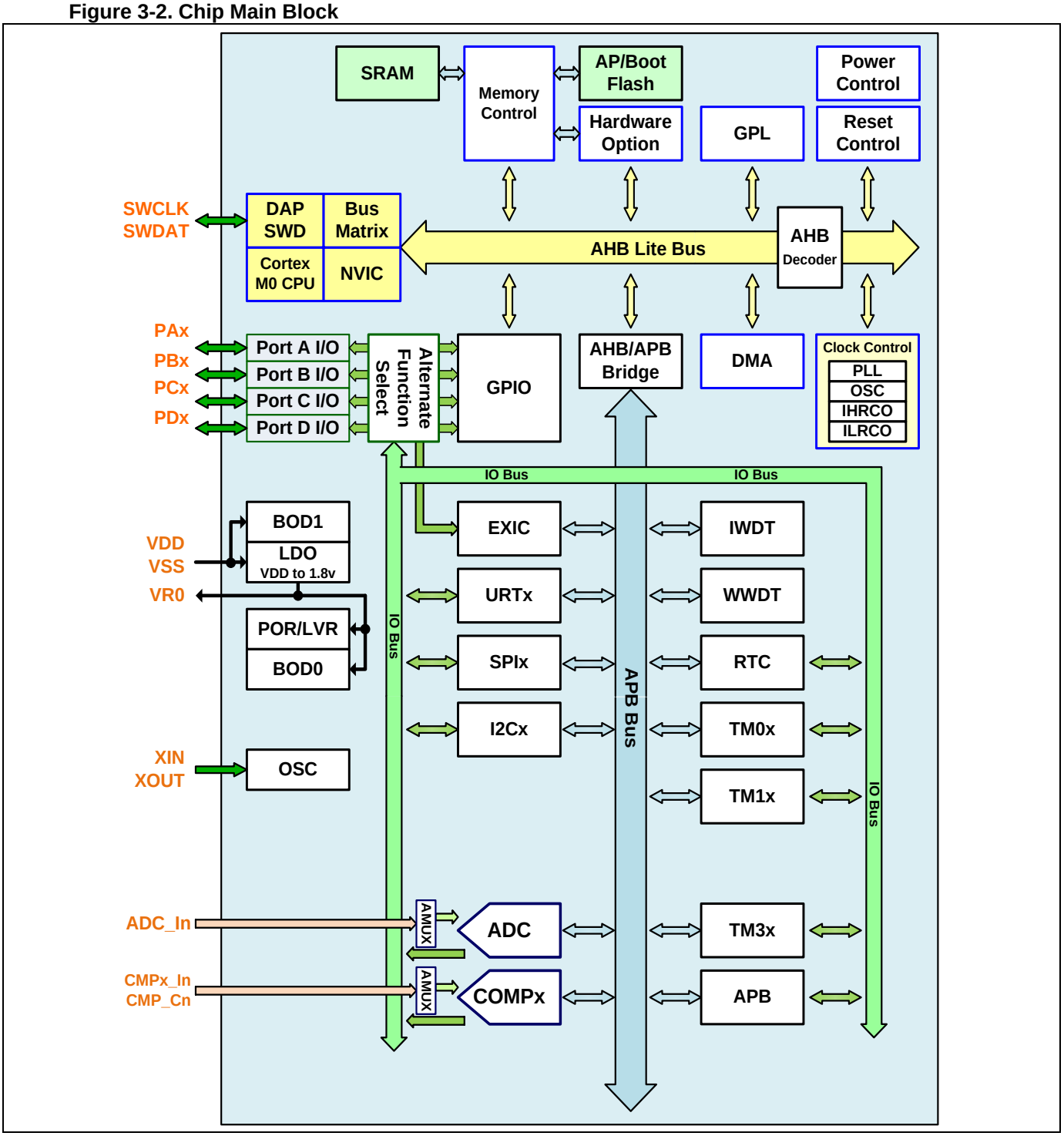


3.2. Chip Main Block

The following diagram is showing the block of internal devices in the chip.

There are one embedded ARM® Cortex®-M0 processor with NVIC (Nested Vectored Interrupt Controller) and DAP (Debug Access Port); AHB lite bus with SRAM/Flash memory, Power/Reset/Clock system controllers, GPIO control blocks and GPL (General Purpose Logic); APB bus with UART/SPI/I2C communication controllers, timers of general timer / IWDT / WWDT / RTC and analog control block of ADC / analog comparators; analog devices of POR (power on reset), BOD0/BOD1 (Brown-Out Detectors), ILRCO (Internal Low-frequency RC Oscillator)/IHRCO Internal High-frequency RC Oscillator)/PLL.

Figure 3-2. Chip Main Block



4. Pin Description

4.1. Pin Outline

4.1.1. LQFP48 Package Pinout

Figure 4-1. LQFP48 Package Pinout

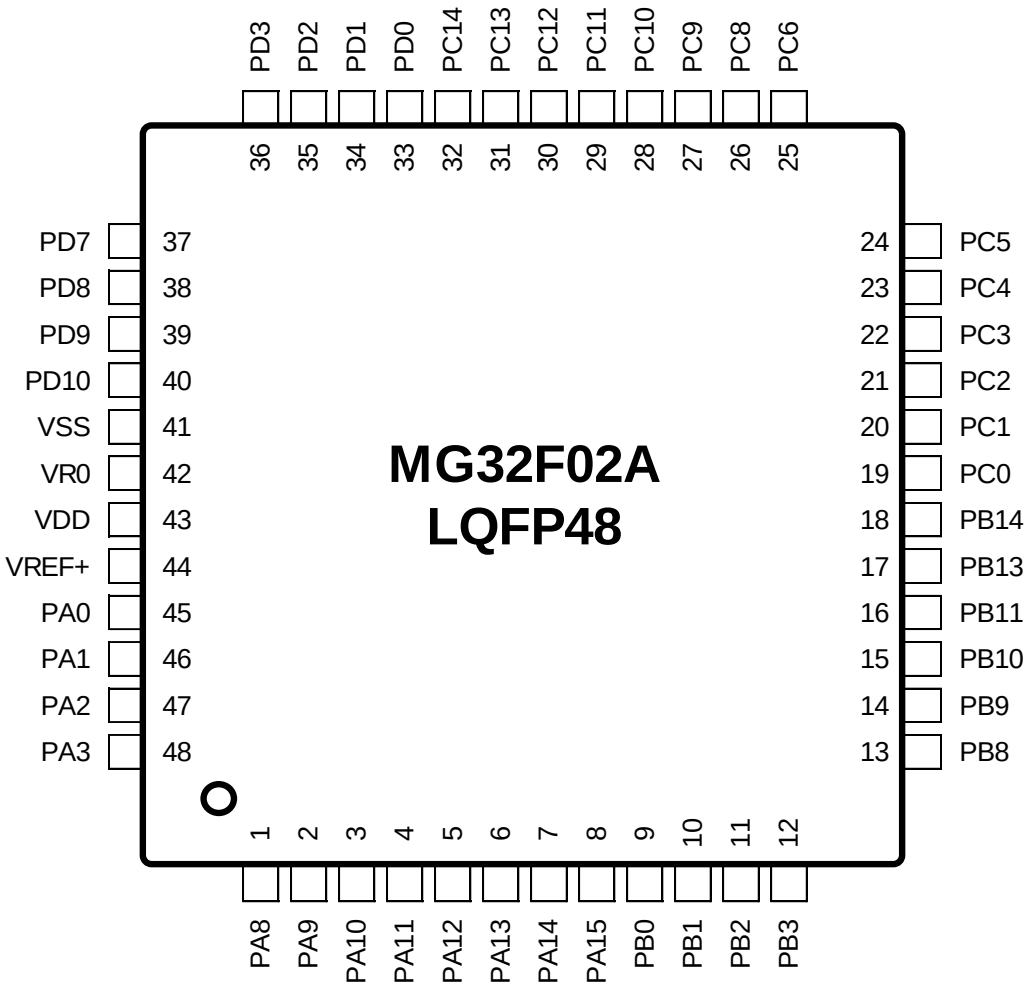


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Table 4-1. LQFP48 Pin AFS List

Pin	Name	Pin AFS List	Analog Function
1	PA8	GPA8	ADC_I8, CMP0_I0, VBG_OUT
2	PA9	GPA9	ADC_I9, CMP0_I1
3	PA10	GPA10	ADC_I10, CMP1_I0, ADC_PGA
4	PA11	GPA11	ADC_I11, CMP1_I1
5	PA12	GPA12, URT1_BRO, TM10_ETR, TM36_IC0	ADC_I12
6	PA13	GPA13, CPU_TXEV, URT0_BRO, URT1_TMO, TM10_TRGO, TM36_IC1	ADC_I13
7	PA14	GPA14, CPU_RXEV, OBM_I0, URT0_TMO, URT1_CTS, TM16_ETR, TM36_IC2	ADC_I14
8	PA15	GPA15, CPU_NMI, OBM_I1, URT0_DE, URT1_RTS, TM16_TRGO, TM36_IC3	ADC_I15
9	PB0	GPB0, SPI0_NSS, TM01_ETR, TM00_CKO, TM16_ETR, TM36_ETR	CMP_C0
10	PB1	GPB1, SPI0_MISO, TM01_TRGO, TM10_CKO, TM16_TRGO, TM36_TRGO	CMP_C1
11	PB2	GPB2, ADC0_TRG, SPI0_CLK, TM01_CKO, TM16_CKO, I2C0_SDA, URT0_TX	
12	PB3	GPB3, ADC0_OUT, SPI0_MOSI, TM36_CKO, I2C0_SCL, URT0_RX	
13	PB8	GPB8, CMP0_P0, RTC_OUT, URT0_TX, TM36_OC01, SPI0_D3, OBM_P0	
14	PB9	GPB9, CMP1_P0, RTC_TS, URT0_RX, TM36_OC02, SPI0_D2, OBM_P1	
15	PB10	GPB10, I2C0_SCL, URT0_NSS, TM36_OC11, URT1_TX, SPI0_NSSI	
16	PB11	GPB11, I2C0_SDA, URT0_DE, IR_OUT, TM36_OC12, URT1_RX, DMA_TRG0	
17	PB13	GPB13, TM00_ETR, URT0_CTS, TM36_ETR	
18	PB14	GPB14, DMA_TRG0, TM00_TRGO, URT0_RTS, TM36_BK0	
19	PC0	GPC0, ICKO, TM00_CKO, URT0_CLK, TM36_OC00, I2C0_SCL, URT0_TX	
20	PC1	GPC1, ADC0_TRG, TM01_CKO, TM36_IC0, URT1_CLK, TM36_OC0N, I2C0_SDA, URT0_RX	
21	PC2	GPC2, ADC0_OUT, TM10_CKO, OBM_P0, TM36_OC10	
22	PC3	GPC3, OBM_P1, TM16_CKO, URT0_CLK, URT1_CLK, TM36_OC1N	
23	PC4	GPC4, SWCLK, I2C0_SCL, URT0_RX, URT1_RX, TM36_OC2	
24	PC5	GPC5, SWDIO, I2C0_SDA, URT0_TX, URT1_TX, TM36_OC3	
25	PC6	GPC6, RSTN, RTC_TS, URT0_NSS, URT1_NSS	
26	PC8	GPC8, ADC0_OUT, I2C0_SCL, URT0_BRO, URT1_TX, TM36_OC0H, TM36_OC0N	
27	PC9	GPC9, CMP0_P0, I2C0_SDA, URT0_TMO, URT1_RX, TM36_OC1H, TM36_OC1N	
28	PC10	GPC10, CMP1_P0, URT0_TX, URT1_TX, TM36_OC2H, TM36_OC2N	
29	PC11	GPC11, URT0_RX, URT1_RX, TM36_OC3H	
30	PC12	GPC12, IR_OUT, URT1_DE, TM10_TRGO, TM36_OC3	
31	PC13	GPC13, XIN, URT1_NSS, URT0_CTS, TM10_ETR, TM36_OC00	
32	PC14	GPC14, XOUT, URT1_TMO, URT0_RTS, TM10_CKO, TM36_OC10	
33	PD0	GPD0, OBM_I0, TM10_CKO, URT0_CLK, TM36_OC2, SPI0_NSS	
34	PD1	GPD1, OBM_I1, TM16_CKO, URT0_CLK, TM36_OC2N, SPI0_CLK	
35	PD2	GPD2, TM00_CKO, URT1_CLK, TM36_CKO, SPI0_MOSI	
36	PD3	GPD3, TM01_CKO, URT1_CLK, SPI0_D3, TM36_TRGO	
37	PD7	GPD7, TM00_CKO, TM01_ETR, URT1_DE, SPI0_MISO, TM36_IC0	
38	PD8	GPD8, CPU_TXEV, TM01_TRGO, URT1_RTS, SPI0_D2, TM36_IC1	
39	PD9	GPD9, CPU_RXEV, TM00_TRGO, URT1_CTS, SPI0_NSSI, TM36_IC2	
40	PD10	GPD10, CPU_NMI, TM00_ETR, URT1_BRO, RTC_OUT, TM36_IC3	
41	VSS		
42	VR0		
43	VDD		
44	VREF+		
45	PA0	GPA0	ADC_I0
46	PA1	GPA1	ADC_I1
47	PA2	GPA2	ADC_I2
48	PA3	GPA3	ADC_I3

4.1.2. QFN32 Package Pinout

Figure 4-2. QFN32 Package Pinout

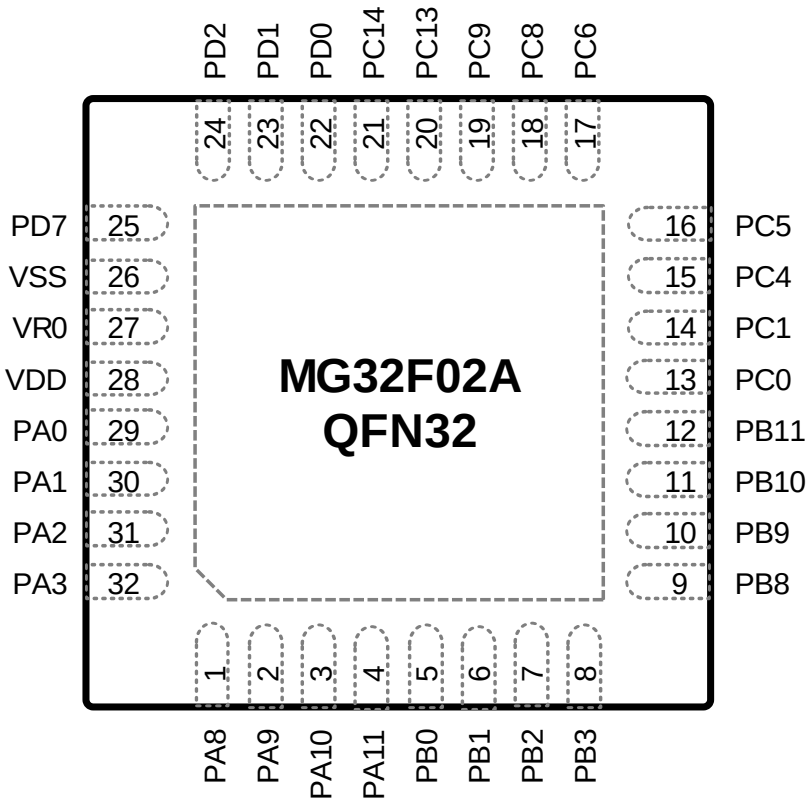

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Table 4-2. QFN32 Pin AFS List

Pin	Name	Pin AFS List	Analog Function
1	**PA8**	GPA8	ADC_I8, CMP0_I0, VBG_OUT
2	**PA9**	GPA9	ADC_I9, CMP0_I1
3	**PA10**	GPA10	ADC_I10, CMP1_I0, ADC_PGA
4	**PA11**	GPA11	ADC_I11, CMP1_I1
5	**PB0**	GPB0, SPI0_NSS, TM01_ETR, TM00_CKO, TM16_ETR, TM36_ETR	CMP_C0
6	**PB1**	GPB1, SPI0_MISO, TM01_TRGO, TM10_CKO, TM16_TRGO, TM36_TRGO	CMP_C1
7	**PB2**	GPB2, ADC0_TRG, SPI0_CLK, TM01_CKO, TM16_CKO, I2C0_SDA, URT0_TX	
8	**PB3**	GPB3, ADC0_OUT, SPI0_MOSI, TM36_CKO, I2C0_SCL, URT0_RX	
9	**PB8**	GPB8, CMP0_P0, RTC_OUT, URT0_TX, TM36_OC01, SPI0_D3, OBM_P0	
10	**PB9**	GPB9, CMP1_P0, RTC_TS, URT0_RX, TM36_OC02, SPI0_D2, OBM_P1	
11	**PB10**	GPB10, I2C0_SCL, URT0_NSS, TM36_OC11, URT1_TX, SPI0_NSSI	
12	**PB11**	GPB11, I2C0_SDA, URT0_DE, IR_OUT, TM36_OC12, URT1_RX, DMA_TRG0	
13	**PC0**	GPC0, ICKO, TM00_CKO, URT0_CLK, TM36_OC00, I2C0_SCL, URT0_TX	
14	**PC1**	GPC1, ADC0_TRG, TM01_CKO, TM36_IC0, URT1_CLK, TM36_OC0N, I2C0_SDA, URT0_RX	
15	**PC4**	GPC4, SWCLK, I2C0_SCL, URT0_RX, URT1_RX, TM36_OC2	
16	**PC5**	GPC5, SWDIO, I2C0_SDA, URT0_TX, URT1_TX, TM36_OC3	
17	**PC6**	GPC6, RSTN, RTC_TS, URT0_NSS, URT1_NSS	
18	**PC8**	GPC8, ADC0_OUT, I2C0_SCL, URT0_BRO, URT1_TX, TM36_OC0H, TM36_OC0N	
19	**PC9**	GPC9, CMP0_P0, I2C0_SDA, URT0_TMO, URT1_RX, TM36_OC1H, TM36_OC1N	
20	**PC13**	GPC13, XIN, URT1_NSS, URT0_CTS, TM10_ETR, TM36_OC00	
21	**PC14**	GPC14, XOUT, URT1_TMO, URT0_RTS, TM10_CKO, TM36_OC10	
22	**PD0**	GPD0, OBM_I0, TM10_CKO, URT0_CLK, TM36_OC2, SPI0_NSS	
23	**PD1**	GPD1, OBM_I1, TM16_CKO, URT0_CLK, TM36_OC2N, SPI0_CLK	
24	**PD2**	GPD2, TM00_CKO, URT1_CLK, TM36_CKO, SPI0_MOSI	
25	**PD7**	GPD7, TM00_CKO, TM01_ETR, URT1_DE, SPI0_MISO, TM36_IC0	

26	VSS		
27	VR0		
28	VDD		
29	PA0	GPA0	ADC_I0
30	PA1	GPA1	ADC_I1
31	PA2	GPA2	ADC_I2
32	PA3	GPA3	ADC_I3

4.1.3. TSSOP20 Package Pinout

Figure 4-3. TSSOP20 Package Pinout

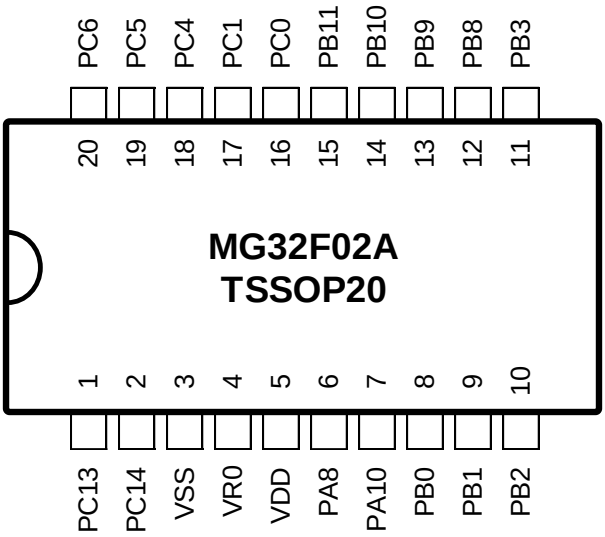

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Table 4-3. TSSOP20 Pin AFS List

Pin	Name	Pin AFS List	Analog Function
1	PC13	GPC13, XIN, URT1_NSS, URT0_CTS, TM10_ETR, TM36_OC00	
2	PC14	GPC14, XOUT, URT1_TMO, URT0_RTS, TM10_CKO, TM36_OC10	
3	VSS		
4	VR0		
5	VDD		
6	PA8	GPA8	ADC_I8, CMP0_I0, VBG_OUT
7	PA10	GPA10	ADC_I10, CMP1_I0, ADC_PGA
8	PB0	GPB0, SPI0_NSS, TM01_ETR, TM00_CKO, TM16_ETR, TM36_ETR	CMP_C0
9	PB1	GPB1, SPI0_MISO, TM01_TRGO, TM10_CKO, TM16_TRGO, TM36_TRGO	CMP_C1
10	PB2	GPB2, ADC0_TRG, SPI0_CLK, TM01_CKO, TM16_CKO, I2C0_SDA, URT0_TX	
11	PB3	GPB3, ADC0_OUT, SPI0_MOSI, TM36_CKO, I2C0_SCL, URT0_RX	
12	PB8	GPB8, CMP0_P0, RTC_OUT, URT0_TX, TM36_OC01, SPI0_D3, OBM_P0	
13	PB9	GPB9, CMP1_P0, RTC_TS, URT0_RX, TM36_OC02, SPI0_D2, OBM_P1	
14	PB10	GPB10, I2C0_SCL, URT0_NSS, TM36_OC11, URT1_TX, SPI0_NSSI	
15	PB11	GPB11, I2C0_SDA, URT0_DE, IR_OUT, TM36_OC12, URT1_RX, DMA_TRG0	
16	PC0	GPC0, ICKO, TM00_CKO, URT0_CLK, TM36_OC00, I2C0_SCL, URT0_TX	
17	PC1	GPC1, ADC0_TRG, TM01_CKO, TM36_IC0, URT1_CLK, TM36_OC0N, I2C0_SDA, URT0_RX	
18	PC4	GPC4, SWCLK, I2C0_SCL, URT0_RX, URT1_RX, TM36_OC2	
19	PC5	GPC5, SWDIO, I2C0_SDA, URT0_TX, URT1_TX, TM36_OC3	
20	PC6	GPC6, RSTN, RTC_TS, URT0_NSS, URT1_NSS	

4.2. Pin Definition

Table 4-4. Abbreviations for pin definition

IO Type		IO Structure	
P	Power/Ground pin	I	Digital Input
B	Bidirection	P	Output Push-pull capability
I	Input	O	Output Open drain capability
O	Output	Q	Quasi-bidirectional
A	Analog I/O	A	Analog I/O (Digital I/O disable)
AO	Analog output only	U	Internal pull-up
AI	Analog input only	H	High Speed
-		C2	Programmable 2-level driving strength
-		C4	Programmable 4-level driving strength
-		CF	Fixed driving strength(GPIO mode)

Table 4-5. Pin Descriptions

Pin Name	Pin Number			IO Type	Default		IO Structure	Alternate Functions	Description
	LQFP48	QFN32	TSSOP20		Type	Value			
PA0	45	29		B	A		A,I,P,O,U,H,C2	GPA0	GPIO/Interrupt/KBI Port-A function pin--0
								ADC_I0	ADC analog single-end input channel 0
PA1	46	30		B	A		A,I,P,O,U,H,C2	GPA1	GPIO/Interrupt/KBI Port-A function pin-1
								ADC_I1	ADC analog single-end input channel 1
PA2	47	31		B	A		A,I,P,O,U,H,C2	GPA2	GPIO/Interrupt/KBI Port-A function pin-2
								ADC_I2	ADC analog single-end input channel 2
PA3	48	32		B	A		A,I,P,O,U,H,C2	GPA3	GPIO/Interrupt/KBI Port-A function pin-3
								ADC_I3	ADC analog single-end input channel 3
PA8	1	1	6	B	A		A,I,P,O,U,H,C2	GPA8	GPIO/Interrupt/KBI Port-A function pin-8
								ADC_I8	ADC analog single-end input channel 8
								CMP0_I0	Comparator-0 analog input channel 0
								VBG_OUT	Bandgap voltage output
PA9	2	2		B	A		A,I,P,O,U,H,C2	GPA9	GPIO/Interrupt/KBI Port-A function pin-9
								ADC_I9	ADC analog single-end input channel 9
								CMP0_I1	Comparator-0 analog input channel 1
PA10	3	3	7	B	A		A,I,P,O,U,H,C2	GPA10	GPIO/Interrupt/KBI Port-A function pin-10
								ADC_I10	ADC analog single-end input channel 10
								CMP1_I0	Comparator-1 analog input channel 0
								ADC_PGA	ADC PGA voltage output
PA11	4	4		B	A		A,I,P,O,U,H,C2	GPA11	GPIO/Interrupt/KBI Port-A function pin-11
								ADC_I11	ADC analog single-end input channel 11
								CMP1_I1	Comparator-1 analog input channel 1
PA12	5			B	A		A,I,P,O,U,H,C2	GPA12	GPIO/Interrupt/KBI Port-A function pin-12
								URT1_BRO	URT1 baud-rate timer overflow output signal
								TM10_ETR	TM10 external trigger/clock input signal

								TM36_IC0	TM36 input capture channel-0
								ADC_I12	ADC analog single-end input channel 12
PA13	6			B	A		A,I,P,O,U,H,C2	GPA13	GPIO/Interrupt/KBI Port-A function pin-13
								CPU_TXEV	CPU wakeup event output
								URT0_BRO	URT0 baud-rate timer overflow output signal
								URT1_TMO	URT1 timeout timer overflow output signal
								TM10_TRGO	TM10 trigger output signal
								TM36_IC1	TM36 input capture channel-1
								ADC_I13	ADC analog single-end input channel 13
PA14	7			B	A		A,I,P,O,U,H,C2	GPA14	GPIO/Interrupt/KBI Port-A function pin-14
								CPU_RXEV	CPU wakeup event input
								OBM_I0	Output signal break control input signal-0
								URT0_TMO	URT0 timeout timer overflow output signal
								URT1_CTS	URT1 CTS input control signal
								TM16_ETR	TM16 external trigger/clock input signal
								TM36_IC2	TM36 input capture channel-2
								ADC_I14	ADC analog single-end input channel 14
PA15	8			B	A		A,I,P,O,U,H,C2	GPA15	GPIO/Interrupt/KBI Port-A function pin-15
								CPU_NMI	CPU NMI external pin input
								OBM_I1	Output signal break control input signal-1
								URT0_DE	URT0 external drive enable output signal
								URT1_RTS	URT1 RTS output control signal
								TM16_TRGO	TM16 trigger output signal
								TM36_IC3	TM36 input capture channel-3
								ADC_I15	ADC analog single-end input channel 15
PB0	9	5	8	B	A		A,I,P,O,U,H,C4	GPB0	GPIO/Interrupt/KBI Port-B function pin-0
								SPI0_NSS	SPI0 slave select input/output signal
								TM01_ETR	TM01 external trigger/clock input signal
								TM00_CKO	TM00 timer overflow output signal
								TM16_ETR	TM16 external trigger/clock input signal
								TM36_ETR	TM36 external trigger/clock input signal
								CMP_C0	Comparator analog input common channel 0
PB1	10	6	9	B	A		A,I,P,O,U,H,C4	GPB1	GPIO/Interrupt/KBI Port-B function pin-1
								SPI0_MISO	SPI0 master input / slave output signal or data-1 signal for 4-I/O mode
								TM01_TRGO	TM01 trigger output signal
								TM10_CKO	TM10 timer overflow output signal
								TM16_TRGO	TM16 trigger output signal
								TM36_TRGO	TM36 trigger output signal
								CMP_C1	Comparator analog input common channel 1
PB2	11	7	10	B	A		A,I,P,O,U,H,C4	GPB2	GPIO/Interrupt/KBI Port-B function pin-2
								ADC0_TRG	ADC trigger start input
								SPI0_CLK	SPI0 clock signal
								TM01_CKO	TM01 timer overflow output signal
								TM16_CKO	TM16 timer overflow output signal
								I2C0_SDA	I2C0 SDA signal

								URT0_TX	URT0 transmit TX signal, SPI MOSI signal
PB3	12	8	11	B	A		A,I,P,O,U,H,C4	GPB3	GPIO/Interrupt/KBI Port-B function pin-3
								ADC0_OUT	ADC threshold window compare output
								SPI0_MOSI	SPI0 master output / slave input signal or data-0 signal for 4-I/O mode
								TM36_CKO	TM36 timer overflow output signal
								I2C0_SCL	I2C0 SCL signal
								URT0_RX	URT0 receive RX signal, SPI MISO signal
PB8	13	9	12	B	A		A,I,P,O,U,H,C4	GPB8	GPIO/Interrupt/KBI Port-B function pin-8
								CMP0_P0	Comparator-0 data output
								RTC_OUT	RTC selection output signal
								URT0_TX	URT0 transmit TX signal, SPI MOSI signal
								TM36_OC01	TM36 output compare/PWM channel-01
								SPI0_D3	SPI0 data-3 signal for 4-I/O mode
								OBM_P0	Output signal break control output signal-0
PB9	14	10	13	B	A		A,I,P,O,U,H,C4	GPB9	GPIO/Interrupt/KBI Port-B function pin-9
								CMP1_P0	Comparator-1 data output
								RTC_TS	RTC time stamp input signal
								URT0_RX	URT0 receive RX signal, SPI MISO signal
								TM36_OC02	TM36 output compare/PWM channel-02
								SPI0_D2	SPI0 data-2 signal for 4-I/O mode
								OBM_P1	Output signal break control output signal-1
PB10	15	11	14	B	A		A,I,P,O,U,H,C2	GPB10	GPIO/Interrupt/KBI Port-B function pin-10
								I2C0_SCL	I2C0 SCL signal
								URT0_NSS	URT0 SPI NSS output signal
								TM36_OC11	TM36 output compare/PWM channel-11
								URT1_TX	URT1 transmit TX signal, SPI MOSI signal
								SPI0_NSSI	SPI0 slave select input only signal
PB11	16	12	15	B	A		A,I,P,O,U,H,C2	GPB11	GPIO/Interrupt/KBI Port-B function pin-11
								I2C0_SDA	I2C0 SDA signal
								URT0_DE	URT0 external drive enable output signal
								IR_OUT	IR output signal
								TM36_OC12	TM36 output compare/PWM channel-12
								URT1_RX	URT1 receive RX signal, SPI MISO signal
								DMA_TRG0	DMA external trigger pin-0 input
PB13	17			B	A		A,I,P,O,U,H,C2	GPB13	GPIO/Interrupt/KBI Port-B function pin-13
								TM00_ETR	TM00 external trigger/clock input signal
								URT0_CTS	URT0 CTS input control signal
								TM36_ETR	TM36 external trigger/clock input signal
PB14	18			B	A		A,I,P,O,U,H,C2	GPB14	GPIO/Interrupt/KBI Port-B function pin-14
								DMA_TRG0	DMA external trigger pin-0 input
								TM00_TRGO	TM00 trigger output signal
								URT0_RTS	URT0 RTS output control signal
								TM36_BK0	TM36 break input signal
PC0	19	13	16	B	Q	H	A,I,P,O,Q,U,H,C2	GPC0	GPIO/Interrupt/KBI Port-C function pin-0
								ICKO	Internal clock source clock output
								TM00_CKO	TM00 timer overflow output signal
								URT0_CLK	URT0 clock signal
								TM36_OC00	TM36 output compare/PWM channel-00

								I2C0_SCL	I2C0 SCL signal
								URT0_TX	URT0 transmit TX signal, SPI MOSI signal
PC1	20	14	17	B	Q	H	A,I,P,O,Q,U,H,C2	GPC1	GPIO/Interrupt/KBI Port-C function pin-1
								ADC0_TRG	ADC trigger start input
								TM01_CKO	TM01 timer overflow output signal
								TM36_IC0	TM36 input capture channel-0
								URT1_CLK	URT1 clock signal
								TM36_OC0N	TM36 output compare/PWM complement channel-0
								I2C0_SDA	I2C0 SDA signal
								URT0_RX	URT0 receive RX signal, SPI MISO signal
PC2	21			B	Q	H	A,I,P,O,Q,U,H,C2	GPC2	GPIO/Interrupt/KBI Port-C function pin-2
								ADC0_OUT	ADC threshold window compare output
								TM10_CKO	TM10 timer overflow output signal
								OBM_P0	Output signal break control output signal-0
								TM36_OC10	TM36 output compare/PWM channel-10
PC3	22			B	Q	H	A,I,P,O,Q,U,H,C2	GPC3	GPIO/Interrupt/KBI Port-C function pin-3
								OBM_P1	Output signal break control output signal-1
								TM16_CKO	TM16 timer overflow output signal
								URT0_CLK	URT0 clock signal
								URT1_CLK	URT1 clock signal
								TM36_OC1N	TM36 output compare/PWM complement channel-1
PC4	23	15	18	B	Q	H	A,I,P,O,Q,U,H,C2	GPC4	GPIO/Interrupt/KBI Port-C function pin-4
								SWCLK	Serial wire debug clock signal
								I2C0_SCL	I2C0 SCL signal
								URT0_RX	URT0 receive RX signal, SPI MISO signal
								URT1_RX	URT1 receive RX signal, SPI MISO signal
								TM36_OC2	TM36 output compare/PWM channel-2
PC5	24	16	19	B	Q	H	A,I,P,O,Q,U,H,C2	GPC5	GPIO/Interrupt/KBI Port-C function pin-5
								SWDIO	Serial wire debug data signal
								I2C0_SDA	I2C0 SDA signal
								URT0_TX	URT0 transmit TX signal, SPI MOSI signal
								URT1_TX	URT1 transmit TX signal, SPI MOSI signal
								TM36_OC3	TM36 output compare/PWM channel-3
PC6	25	17	20	B	Q	H	A,I,P,O,Q,U,CF	GPC6	GPIO/Interrupt/KBI Port-C function pin-6
								RSTN	External hardware reset input
								RTC_TS	RTC time stamp input signal
								URT0_NSS	URT0 SPI NSS output signal
								URT1_NSS	URT1 SPI NSS output signal
PC8	26	18		B	Q	H	A,I,P,O,Q,U,H,C2	GPC8	GPIO/Interrupt/KBI Port-C function pin-8
								ADC0_OUT	ADC threshold window compare output
								I2C0_SCL	I2C0 SCL signal
								URT0_BRO	URT0 baud-rate timer overflow output signal
								URT1_TX	URT1 transmit TX signal, SPI MOSI signal
								TM36_OC0H	TM36 output compare/PWM high channel-0
								TM36_OC0N	TM36 output compare/PWM complement channel-0
PC9	27	19		B	Q	H	A,I,P,O,Q,U,H,C	GPC9	GPIO/Interrupt/KBI Port-C function pin-9

							2	CMP0_P0	Comparator-0 data output
								I2C0_SDA	I2C0 SDA signal
								URT0_TMO	URT0 timeout timer overflow output signal
								URT1_RX	URT1 receive RX signal, SPI MISO signal
								TM36_OC1H	TM36 output compare/PWM high channel-1
								TM36_OC1N	TM36 output compare/PWM complement channel-1
PC10	28			B	Q	H	A,I,P,O,Q,U,H,C2	GPC10	GPIO/Interrupt/KBI Port-C function pin-10
								CMP1_P0	Comparator-1 data output
								URT0_TX	URT0 transmit TX signal, SPI MOSI signal
								URT1_TX	URT1 transmit TX signal, SPI MOSI signal
								TM36_OC2H	TM36 output compare/PWM high channel-2
								TM36_OC2N	TM36 output compare/PWM complement channel-2
PC11	29			B	Q	H	A,I,P,O,Q,U,H,C2	GPC11	GPIO/Interrupt/KBI Port-C function pin-11
								URT0_RX	URT0 receive RX signal, SPI MISO signal
								URT1_RX	URT1 receive RX signal, SPI MISO signal
								TM36_OC3H	TM36 output compare/PWM high channel-3
PC12	30			B	Q	H	A,I,P,O,Q,U,H,C2	GPC12	GPIO/Interrupt/KBI Port-C function pin-12
								IR_OUT	IR output signal
								URT1_DE	URT1 external drive enable output signal
								TM10_TRGO	TM10 trigger output signal
								TM36_OC3	TM36 output compare/PWM channel-3
PC13	31	20	1	B	Q	H	A,I,P,O,Q,U,CF	GPC13	GPIO/Interrupt/KBI Port-C function pin-13
								XIN	External Xtal/OSC input
								URT1_NSS	URT1 SPI NSS output signal
								URT0_CTS	URT0 CTS input control signal
								TM10_ETR	TM10 external trigger/clock input signal
								TM36_OC00	TM36 output compare/PWM channel-00
PC14	32	21	2	B	Q	H	A,I,P,O,Q,U,H,CF	GPC14	GPIO/Interrupt/KBI Port-C function pin-14
								XOUT	External Xtal output
								URT1_TMO	URT1 timeout timer overflow output signal
								URT0_RTS	URT0 RTS output control signal
								TM10_CKO	TM10 timer overflow output signal
								TM36_OC10	TM36 output compare/PWM channel-10
PD0	33	22		B	A		A,I,P,O,U,H,C4	GPD0	GPIO/Interrupt/KBI Port-D function pin-0
								OBM_I0	Output signal break control input signal-0
								TM10_CKO	TM10 timer overflow output signal
								URT0_CLK	URT0 clock signal
								TM36_OC2	TM36 output compare/PWM channel-2
								SPI0_NSS	SPI0 slave select input/output signal
PD1	34	23		B	A		A,I,P,O,U,H,C4	GPD1	GPIO/Interrupt/KBI Port-D function pin-1
								OBM_I1	Output signal break control input signal-1
								TM16_CKO	TM16 timer overflow output signal
								URT0_CLK	URT0 clock signal
								TM36_OC2N	TM36 output compare/PWM complement channel-2
								SPI0_CLK	SPI0 clock signal
PD2	35	24		B	A		A,I,P,O,U,H,C4	GPD2	GPIO/Interrupt/KBI Port-D function pin-2

								TM00_CKO	TM00 timer overflow output signal
								URT1_CLK	URT1 clock signal
								TM36_CKO	TM36 timer overflow output signal
								SPI0_MOSI	SPI0 master output / slave input signal or data-0 signal for 4-I/O mode
PD3	36			B	A		A,I,P,O,U,H,C4	GPD3	GPIO/Interrupt/KBI Port-D function pin-3
								TM01_CKO	TM01 timer overflow output signal
								URT1_CLK	URT1 clock signal
								SPI0_D3	SPI0 data-3 signal for 4-I/O mode
								TM36_TRGO	TM36 trigger output signal
PD7	37	25		B	A		A,I,P,O,U,H,C4	GPD7	GPIO/Interrupt/KBI Port-D function pin-7
								TM00_CKO	TM00 timer overflow output signal
								TM01_ETR	TM01 external trigger/clock input signal
								URT1_DE	URT1 external drive enable output signal
								SPI0_MISO	SPI0 master input / slave output signal or data-1 signal for 4-I/O mode
								TM36_IC0	TM36 input capture channel-0
PD8	38			B	A		A,I,P,O,U,H,C4	GPD8	GPIO/Interrupt/KBI Port-D function pin-8
								CPU_TXEV	CPU wakeup event output
								TM01_TRGO	TM01 trigger output signal
								URT1_RTS	URT1 RTS output control signal
								SPI0_D2	SPI0 data-2 signal for 4-I/O mode
								TM36_IC1	TM36 input capture channel-1
PD9	39			B	A		A,I,P,O,U,H,C2	GPD9	GPIO/Interrupt/KBI Port-D function pin-9
								CPU_RXEV	CPU wakeup event input
								TM00_TRGO	TM00 trigger output signal
								URT1_CTS	URT1 CTS input control signal
								SPI0_NSSI	SPI0 slave select input only signal
								TM36_IC2	TM36 input capture channel-2
PD10	40			B	A		A,I,P,O,U,H,C2	GPD10	GPIO/Interrupt/KBI Port-D function pin-10
								CPU_NMI	CPU NMI external pin input
								TM00_ETR	TM00 external trigger/clock input signal
								URT1_BRO	URT1 baud-rate timer overflow output signal
								RTC_OUT	RTC selection output signal
								TM36_IC3	TM36 input capture channel-3
VSS	41	26	3	P					IO/Core/ADC ground
VR0	42	27	4	AO	AO				Core power supply/LDO output (place 0.1uF+4.7uF capacitors and close pin)
VDD	43	28	5	P					IO power supply/LDO input (place 0.1uF+10uF capacitors and close pin)
VREF+	44			AI	AI				ADC voltage reference (place 0.1uF+4.7uF capacitors and close pin)

4.3. Pin AFS Summary Table

The following table is the AFS signal list of the related IO pin for all pins' summary. (AFS=n, n: I/O pin AFS setting value)

Table 4-6. Pin AFS Summary Table

Pin Name	AFS=0	AFS=1	AFS=2	AFS=3	AFS=4	AFS=5	AFS=6	AFS=7	AFS=10
PA0	GPA0								
PA1	GPA1								
PA2	GPA2								
PA3	GPA3								
PA8	GPA8								
PA9	GPA9								
PA10	GPA10								
PA11	GPA11								
PA12	GPA12				URT1_BRO	TM10_ETR	TM36_IC0		
PA13	GPA13	CPU_TXEV		URT0_BRO	URT1_TMO	TM10_TRGO	TM36_IC1		
PA14	GPA14	CPU_RXEV	OBM_I0	URT0_TMO	URT1_CTS	TM16_ETR	TM36_IC2		
PA15	GPA15	CPU_NMI	OBM_I1	URT0_DE	URT1_RTS	TM16_TRGO	TM36_IC3		
PB0	GPB0		SPI0_NSS	TM01_ETR	TM00_CKO	TM16_ETR		TM36_ETR	
PB1	GPB1		SPI0_MISO	TM01_TRGO	TM10_CKO	TM16_TRGO		TM36_TRGO	
PB2	GPB2	ADC0_TRG	SPI0_CLK	TM01_CKO		TM16_CKO		I2C0_SDA	URT0_TX
PB3	GPB3	ADC0_OUT	SPI0_MOSI			TM36_CKO		I2C0_SCL	URT0_RX
PB8	GPB8	CMP0_P0	RTC_OUT	URT0_TX			TM36_OC01	SPI0_D3	OBM_P0
PB9	GPB9	CMP1_P0	RTC_TS	URT0_RX			TM36_OC02	SPI0_D2	OBM_P1
PB10	GPB10		I2C0_SCL	URT0_NSS			TM36_OC11	URT1_TX	SPI0_NSSI
PB11	GPB11		I2C0_SDA	URT0_DE	IR_OUT		TM36_OC12	URT1_RX	DMA_TRG0
PB13	GPB13		TM00_ETR	URT0_CTS			TM36_ETR		
PB14	GPB14	DMA_TRG0	TM00_TRGO	URT0_RTS			TM36_BK0		
PC0	GPC0	ICKO	TM00_CKO	URT0_CLK			TM36_OC00	I2C0_SCL	URT0_TX
PC1	GPC1	ADC0_TRG	TM01_CKO	TM36_IC0	URT1_CLK		TM36_OC0N	I2C0_SDA	URT0_RX
PC2	GPC2	ADC0_OUT	TM10_CKO	OBM_P0			TM36_OC10		
PC3	GPC3	OBM_P1	TM16_CKO	URT0_CLK	URT1_CLK		TM36_OC1N		
PC4	GPC4	SWCLK	I2C0_SCL	URT0_RX	URT1_RX		TM36_OC2		
PC5	GPC5	SWDIO	I2C0_SDA	URT0_TX	URT1_TX		TM36_OC3		
PC6	GPC6	RSTN	RTC_TS	URT0_NSS	URT1_NSS				
PC8	GPC8	ADC0_OUT	I2C0_SCL	URT0_BRO	URT1_TX		TM36_OC0H	TM36_OC0N	
PC9	GPC9	CMP0_P0	I2C0_SDA	URT0_TMO	URT1_RX		TM36_OC1H	TM36_OC1N	
PC10	GPC10	CMP1_P0		URT0_TX		URT1_TX	TM36_OC2H	TM36_OC2N	
PC11	GPC11			URT0_RX		URT1_RX	TM36_OC3H		
PC12	GPC12		IR_OUT		URT1_DE	TM10_TRGO	TM36_OC3		
PC13	GPC13	XIN	URT1_NSS	URT0_CTS		TM10_ETR		TM36_OC00	
PC14	GPC14	XOUT	URT1_TMO	URT0_RTS		TM10_CKO		TM36_OC10	
PD0	GPD0	OBM_I0	TM10_CKO	URT0_CLK			TM36_OC2	SPI0_NSS	
PD1	GPD1	OBM_I1	TM16_CKO	URT0_CLK			TM36_OC2N	SPI0_CLK	
PD2	GPD2		TM00_CKO	URT1_CLK			TM36_CKO	SPI0_MOSI	
PD3	GPD3		TM01_CKO	URT1_CLK				SPI0_D3	TM36_TRGO
PD7	GPD7	TM00_CKO	TM01_ETR	URT1_DE		SPI0_MISO			TM36_IC0

PD8	GPD8	CPU_TXEV	TM01_TRGO	URT1_RTS		SPI0_D2			TM36_IC1
PD9	GPD9	CPU_RXEV	TM00_TRGO	URT1_CTS		SPI0_NSSI			TM36_IC2
PD10	GPD10	CPU_NMI	TM00_ETR	URT1_BRO		RTC_OUT			TM36_IC3

4.4. Analog Function Pin Table

The following table is the analog signal pin list for all the analog function.

Table 4-7. Analog Function Pin Table

Pin Name	ADC	CMP	Others
PA0	ADC_I0		
PA1	ADC_I1		
PA2	ADC_I2		
PA3	ADC_I3		
PA8	ADC_I8	CMP0_I0	VBG_OUT
PA9	ADC_I9	CMP0_I1	
PA10	ADC_I10	CMP1_I0	ADC_PGA
PA11	ADC_I11	CMP1_I1	
PA12	ADC_I12		
PA13	ADC_I13		
PA14	ADC_I14		
PA15	ADC_I15		
PB0		CMP_C0	
PB1		CMP_C1	

4.5. Alternate Functions Pin List

The following table is the pin list of the related AFS IO signal for all AFS signals' summary.

Table 4-8. Alternate Functions Pin List

No.	AFS List		Pin List for the AFS IO ([ ] : AFS setting value)				
	Group	AFS Name	Pin-1 Name	Pin-2 Name	Pin-3 Name	Pin-4 Name	Pin-5 Name
1	GPA	GPA0	PA0 [0]				
2		GPA1	PA1 [0]				
3		GPA2	PA2 [0]				
4		GPA3	PA3 [0]				
5		GPA8	PA8 [0]				
6		GPA9	PA9 [0]				
7		GPA10	PA10 [0]				
8		GPA11	PA11 [0]				
9		GPA12	PA12 [0]				
10		GPA13	PA13 [0]				
11		GPA14	PA14 [0]				
12		GPA15	PA15 [0]				
13	GPB	GPB0	PB0 [0]				
14		GPB1	PB1 [0]				
15		GPB2	PB2 [0]				
16		GPB3	PB3 [0]				
17		GPB8	PB8 [0]				
18		GPB9	PB9 [0]				
19		GPB10	PB10 [0]				
20		GPB11	PB11 [0]				
21		GPB13	PB13 [0]				
22		GPB14	PB14 [0]				
23	GPC	GPC0	PC0 [0]				
24		GPC1	PC1 [0]				
25		GPC2	PC2 [0]				
26		GPC3	PC3 [0]				
27		GPC4	PC4 [0]				
28		GPC5	PC5 [0]				
29		GPC6	PC6 [0]				
30		GPC8	PC8 [0]				
31		GPC9	PC9 [0]				
32		GPC10	PC10 [0]				
33		GPC11	PC11 [0]				
34		GPC12	PC12 [0]				
35		GPC13	PC13 [0]				
36		GPC14	PC14 [0]				
37	GPD	GPD0	PD0 [0]				
38		GPD1	PD1 [0]				
39		GPD2	PD2 [0]				
40		GPD3	PD3 [0]				
41		GPD7	PD7 [0]				

42		GPD8	PD8 [0]				
43		GPD9	PD9 [0]				
44		GPD10	PD10 [0]				
45	Reset	RSTN	PC6 [1]				
46	SWD	SWCLK	PC4 [1]				
47		SWDIO	PC5 [1]				
48	Clock	ICKO	PC0 [1]				
49		XIN	PC13 [1]				
50		XOUT	PC14 [1]				
51	ADC0	ADC0_TRG	PB2 [1]	PC1 [1]			
52		ADC0_OUT	PB3 [1]	PC2 [1]	PC8 [1]		
53	CMP	CMP0_P0	PB8 [1]	PC9 [1]			
54		CMP1_P0	PB9 [1]	PC10 [1]			
55	I2C0	I2C0_SCL	PB3 [7]	PB10 [2]	PC0 [7]	PC4 [2]	PC8 [2]
56		I2C0_SDA	PB2 [7]	PB11 [2]	PC1 [7]	PC5 [2]	PC9 [2]
57	URT0	URT0_TX	PB2 [10]	PB8 [3]	PC5 [3]	PC10 [3]	PC0 [10]
58		URT0_RX	PB3 [10]	PB9 [3]	PC4 [3]	PC11 [3]	PC1 [10]
59		URT0_CLK	PC0 [3]	PC3 [3]	PD0 [3]	PD1 [3]	
60		URT0_BRO	PA13 [3]	PC8 [3]			
61		URT0_TMO	PA14 [3]	PC9 [3]			
62		URT0_DE	PA15 [3]	PB11 [3]			
63		URT0_CTS	PB13 [3]	PC13 [3]			
64		URT0_RTS	PB14 [3]	PC14 [3]			
65		URT0_NSS	PB10 [3]	PC6 [3]			
66	URT1	URT1_TX	PB10 [7]	PC5 [4]	PC8 [4]	PC10 [5]	
67		URT1_RX	PB11 [7]	PC4 [4]	PC9 [4]	PC11 [5]	
68		URT1_CLK	PC1 [4]	PC3 [4]	PD2 [3]	PD3 [3]	
69		URT1_BRO	PA12 [4]	PD10 [3]			
70		URT1_TMO	PA13 [4]	PC14 [2]			
71		URT1_DE	PC12 [4]	PD7 [3]			
72		URT1_CTS	PA14 [4]	PD9 [3]			
73		URT1_RTS	PA15 [4]	PD8 [3]			
74		URT1_NSS	PC6 [4]	PC13 [2]			
75	SPI0	SPI0_CLK	PB2 [2]	PD1 [7]			
76		SPI0_MOSI	PB3 [2]	PD2 [7]			
77		SPI0_MISO	PB1 [2]	PD7 [5]			
78		SPI0_NSS	PB0 [2]	PD0 [7]			
79		SPI0_D2	PB9 [7]	PD8 [5]			
80		SPI0_D3	PB8 [7]	PD3 [7]			
81		SPI0_NSSI	PB10 [10]	PD9 [5]			
82	TM00	TM00_CKO	PB0 [4]	PC0 [2]	PD2 [2]	PD7 [1]	
83		TM00_TRGO	PB14 [2]	PD9 [2]			
84		TM00_ETR	PB13 [2]	PD10 [2]			
85	TM01	TM01_CKO	PB2 [3]	PC1 [2]	PD3 [2]		
86		TM01_TRGO	PB1 [3]	PD8 [2]			
87		TM01_ETR	PB0 [3]	PD7 [2]			
88	TM10	TM10_CKO	PB1 [4]	PC2 [2]	PC14 [5]	PD0 [2]	
89		TM10_TRGO	PA13 [5]	PC12 [5]			
90		TM10_ETR	PA12 [5]	PC13 [5]			

91	TM16	TM16_CKO	PB2 [5]	PC3 [2]	PD1 [2]		
92		TM16_TRGO	PA15 [5]	PB1 [5]			
93		TM16_ETR	PA14 [5]	PB0 [5]			
94	TM36	TM36_CKO	PB3 [5]	PD2 [6]			
95		TM36_TRGO	PB1 [7]	PD3 [10]			
96		TM36_ETR	PB0 [7]	PB13 [6]			
97		TM36_IC0	PA12 [6]	PD7 [10]	PC1 [3]		
98		TM36_IC1	PA13 [6]	PD8 [10]			
99		TM36_IC2	PA14 [6]	PD9 [10]			
100		TM36_IC3	PA15 [6]	PD10 [10]			
101		TM36_OC00	PC0 [6]	PC13 [7]			
102		TM36_OC01	PB8 [6]				
103		TM36_OC02	PB9 [6]				
104		TM36_OC0N	PC1 [6]	PC8 [7]			
105		TM36_OC10	PC2 [6]	PC14 [7]			
106		TM36_OC11	PB10 [6]				
107		TM36_OC12	PB11 [6]				
108		TM36_OC1N	PC3 [6]	PC9 [7]			
109		TM36_OC2	PC4 [6]	PD0 [6]			
110		TM36_OC2N	PD1 [6]	PC10 [7]			
111		TM36_OC3	PC5 [6]	PC12 [6]			
112		TM36_OC0H	PC8 [6]				
113		TM36_OC1H	PC9 [6]				
114		TM36_OC2H	PC10 [6]				
115		TM36_OC3H	PC11 [6]				
116		TM36_BK0	PB14 [6]				
117	RTC	RTC_OUT	PB8 [2]	PD10 [5]			
118		RTC_TS	PB9 [2]	PC6 [2]			
119	OBM	OBM_I0	PA14 [2]	PD0 [1]			
120		OBM_I1	PA15 [2]	PD1 [1]			
121		OBM_P0	PB8 [10]	PC2 [3]			
122		OBM_P1	PB9 [10]	PC3 [1]			
123	Other	DMA_TRG0	PB11 [10]	PB14 [1]			
124		CPU_TXEV	PA13 [1]	PD8 [1]			
125		CPU_RXEV	PA14 [1]	PD9 [1]			
126		CPU_NMI	PA15 [1]	PD10 [1]			
127		IR_OUT	PB11 [4]	PC12 [2]			

5. Memory Map

5.1. Memory Organization

There are ***4K*** bytes of SRAM built in the chip. The chip has up to ***32K*** bytes of embedded main flash memory for code and data, programmable memory size of embedded system flash memory for boot load code and 64 bytes of embedded option-byte (***OB***) flash memory for chip configuration. Others, there are many module independent hardware control registers and locate at the memory space of AHB/APB devices.

User can configure the whole flash to store for his Application Program (AP) code, In-System-Program (ISP) code and In-Application-Program (IAP) memory. User can adjust the size for the three flash memories.

5.2. CPU Memory Map

The following diagram is showing the memory map of CPU. There are separated eight memory blocks and the memory size is 512M-byte for each block. The block is signed “XN” which is not able to execute code.

Figure 5-1. CPU Memory Map

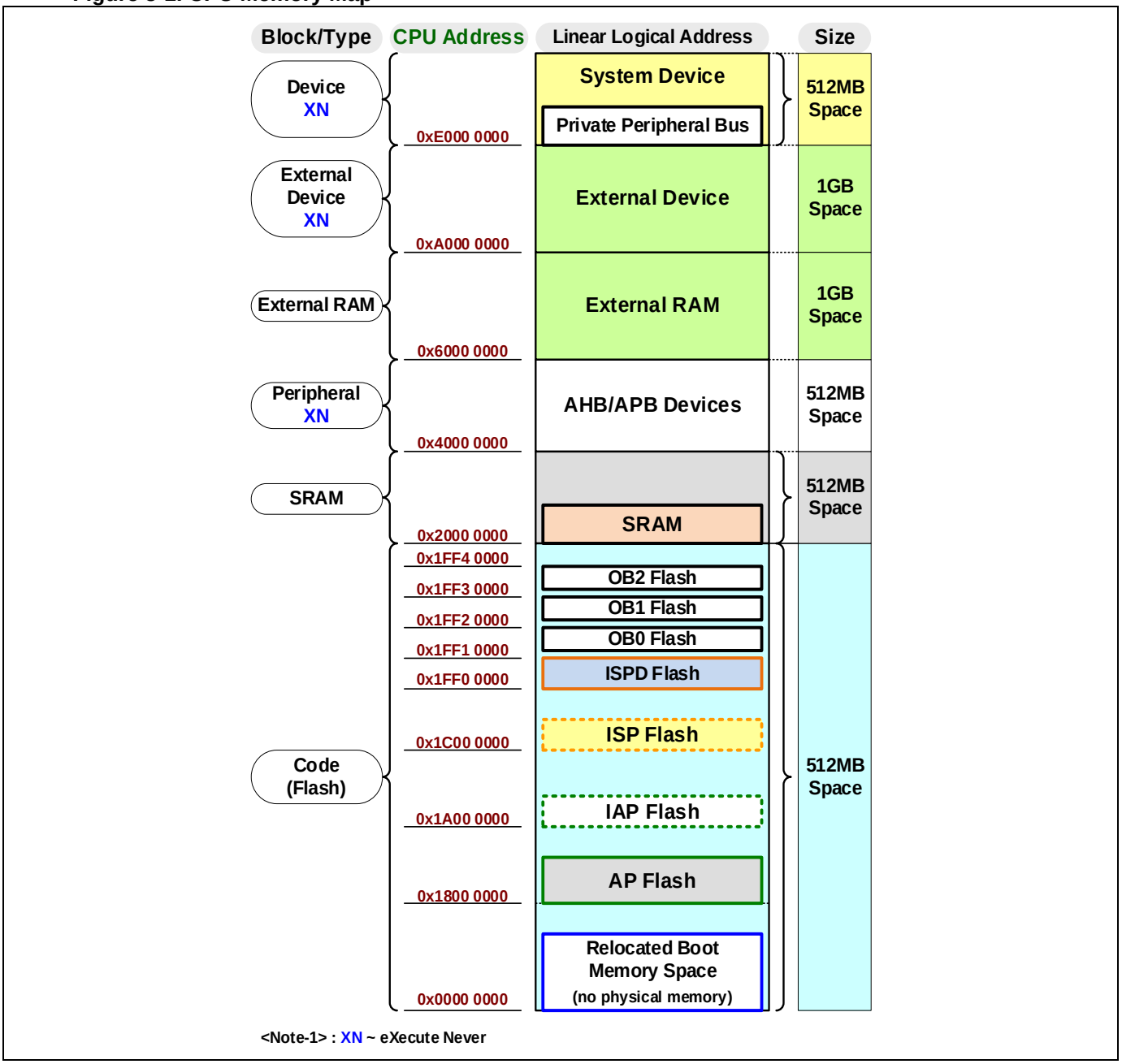


Table 5-1. CPU Memory Address Map

Block Index	Block Name	XN	Boundary address		Size	Address Space	Note
			Start address	End address			
7	System Device	XN	0xE010 0000	0xFFFF FFFF	511MB	VENDOR_SYS	
			0xE000 0000	0xE00F FFFF	1MB	Private Peripheral Bus(PPB)	M0 Reserved Cortex M0 internal peripherals
6	External Device	XN	0xC000 0000	0xDFFF FFFF	512MB	Reserved	External memory (SRAM, Flash)
5	External Device	XN	0xA000 0000	0xBFFF FFFF	512MB	Reserved	External memory (SRAM, Flash)
4	External RAM		0x8000 0000	0x9FFF FFFF	512MB	Reserved	External memory (SRAM, Flash)
3	External RAM		0x6000 0000	0x7FFF FFFF	512MB	Reserved	External memory (SRAM, Flash)
2	Peripheral	XN	0x4000 0000	0x5FFF FFFF	512MB	APB/AHB	APB/AHB modules
1			0x2000 1000	0x3FFF FFFF	512MB	Reserved	
			0x2000 0000	0x2000 0FFF	4KB	**SRAM**	
0	Code		0x1FF4 0000	0x1FFF FFFF	768KB	Reserved	
			0x1FF3 0400	0x1FF3 FFFF	63KB	Reserved	
			0x1FF3 0040	0x1FF3 03FF	960B	**OB Flash-2**	
			0x1FF3 0000	0x1FF3 003F	64B		Hardware Option byte-2 (64-byte)
			0x1FF2 0400	0x1FF2 FFFF	63KB	Reserved	
			0x1FF2 0050	0x1FF2 03FF	944B	**OB Flash-1**	
			0x1FF2 0040	0x1FF2 004F	16B		Random ID (16-byte)
			0x1FF2 0000	0x1FF2 003F	64B		Hardware Option byte-1 (64-byte)
			0x1FF1 0400	0x1FF1 FFFF	63KB	Reserved	
			0x1FF1 0040	0x1FF1 03FF	960B	**OB Flash-0**	
			0x1FF1 0000	0x1FF1 003F	64B		Hardware Option byte-0 (64-byte)
			0x1FF0 0400	0x1FF0 FFFF	63KB	Reserved	
			0x1FF0 0000	0x1FF0 03FF	1KB	**ISPD Flash**	ISP data flash
			0x1C00 8000	0x1FEF FFFF	63MB	Reserved	
			0x1C00 0000	0x1C00 7FFF	32KB	**ISP Flash**	Boot Flash memory (configurable size)
			0x1A00 8000	0x1BFF FFFF	32MB	Reserved	
			0x1A00 0000	0x1A00 7FFF	32KB	**IAP Flash**	Data Flash memory (configurable size)
			0x1800 8000	0x19FF FFFF	32MB	Reserved	
			0x1800 0000	0x1800 7FFF	32KB	**AP Flash**	Application Flash memory (configurable size by chip option)
			0x0000 8000	0x17FF FFFF	384MB	Reserved	
			0x0000 0000	0x0000 7FFF	32KB	Relocated memory space	Interrupt Vector 0x0000 00C0~0x0000 0000

XN : eXecute Never , 1 Block = 512MB

Relocated memory space : Main flash memory, Boot flash memory or SRAM depending on BOOT configuration

5.3. Peripheral Memory Boundary

Table 5-2. Peripheral Memory Boundary Address

Address Type	Boundary address		Size	Sections / Groups Peripheral	Module	Note
	Start address	End address				
APB	0x5F00 0100	0x5FFF FFFF	16MB	APB	Reserved	
	0x5F00 0000	0x5F00 00FF	256B		**APB**	APB module global control
	0x5E00 0000	0x5EFF FFFF	16MB	Reserved	Reserved	
	0x5D04 0100	0x5DFF FFFF	16MB	WDT/RTC	Reserved	
	0x5D04 0000	0x5D04 00FF	256B		**RTC**	Real Time Clock
	0x5D01 0100	0x5D03 FFFF	192KB		Reserved	
	0x5D01 0000	0x5D01 00FF	256B		**WWDT**	Window WatchDog Timer
	0x5D00 0100	0x5D00 FFFF	64KB		Reserved	
	0x5D00 0000	0x5D00 00FF	256B		**IWDT**	Independent WatchDog Timer

	0x5C00 0100	0x5CFF FFFF	16MB	CMP/DAC	Reserved	
	0x5C00 0000	0x5C00 00FF	256B		**CMP**	Analog Comparator 0,1
	0x5B00 0100	0x5BFF FFFF	16MB	ADC	Reserved	
	0x5B00 0000	0x5B00 00FF	256B		**ADC**	Analog-to-Digital controller
	0x5700 0000	0x5AFF FFFF	64MB	Reserved	Reserved	
	0x5686 0100	0x56FF FFFF	8MB	TM2x/3x	Reserved	
	0x5686 0000	0x5686 00FF	256B		**TM36**	32-bit Timer with 4 IC/OC/PWM
	0x5600 0000	0x5685 FFFF	8MB		Reserved	
	0x5586 0100	0x55FF FFFF	8MB	TM0x/1x	Reserved	
	0x5586 0000	0x5586 00FF	256B		**TM16**	Basic32-bit Timer/Counter
	0x5580 0100	0x5585 FFFF	384KB		Reserved	
	0x5580 0000	0x5580 00FF	256B		**TM10**	Basic32-bit Timer/Counter
	0x5501 0100	0x557F FFFF	8MB		Reserved	
	0x5501 0000	0x5501 00FF	256B		**TM01**	Basic 16-bit Timer/Counter
	0x5500 0100	0x5500 FFFF	64KB		Reserved	
	0x5500 0000	0x5500 00FF	256B		**TM00**	Basic 16-bit Timer/Counter
	0x5400 0000	0x54FF FFFF	16MB	Reserved	Reserved	
	0x5300 0100	0x53FF FFFF	16MB	SPI	Reserved	
	0x5300 0000	0x5300 00FF	256B		**SPI0**	SPI bus controller with data buffer
	0x5201 0100	0x52FF FFFF	16MB	UART	Reserved	
	0x5201 0000	0x5201 00FF	256B		**URT1**	Advance UART bus controller
	0x5200 0100	0x5200 FFFF	64KB		Reserved	
	0x5200 0000	0x5200 00FF	256B		**URT0**	Advance UART bus controller
	0x5100 0100	0x51FF FFFF	16MB	I2C	Reserved	
	0x5100 0000	0x5100 00FF	256B		**I2C0**	I2C bus controller
	0x5000 0100	0x50FF FFFF	16MB	EXT Interrupt	Reserved	
	0x5000 0000	0x5000 00FF	256B		**EXIC**	External Interrupt Controller
AHB	0x4FF0 0100	0x4FFF FFFF	1024KB	Chip	Reserved	
	0x4FF0 0000	0x4FF0 00FF	256B		**CFG**	Hardware option (NVR0/1/2)
	0x4F00 0100	0x4FEF FFFF	15MB		Reserved	
	0x4F00 0000	0x4F00 00FF	256B		**WRI**	Writer Interface Control
	0x4E00 0000	0x4EFF FFFF	16MB	Reserved	Reserved	
	0x4D00 0100	0x4DFF FFFF	16MB	Memory	Reserved	
	0x4D00 0000	0x4D00 00FF	256B		**MEM**	Internal Memory Controller
	0x4C03 0100	0x4CFF FFFF	16MB	System	Reserved	
	0x4C03 0000	0x4C03 00FF	256B		**SYS**	System and Chip Control
	0x4C02 0100	0x4C02 FFFF	64KB		Reserved	
	0x4C02 0000	0x4C02 00FF	256B		**PW**	Power Management Controller
	0x4C01 0100	0x4C01 FFFF	64KB		Reserved	
	0x4C01 0000	0x4C01 00FF	256B		**CSC**	Clock Source Controller
	0x4C00 0100	0x4C00 FFFF	64KB		Reserved	
	0x4C00 0000	0x4C00 00FF	256B		**RST**	Reset Source Controller
	0x4BF0 0100	0x4BFF FFFF	1024KB	General Purpose	Reserved	
	0x4BF0 0000	0x4BF0 00FF	256B		**DMA**	Direct memory access
	0x4B00 0100	0x4BEF FFFF	15MB		Reserved	
	0x4B00 0000	0x4B00 00FF	256B		**GPL**	General Purpose Logic
	0x4500 0000	0x4AFF FFFF	96MB	Reserved	Reserved	Reserved for future design
	0x4403 0100	0x44FF FFFF	16MB	IO Configure	Reserved	
	0x4403 0000	0x4403 00FF	256B		**PD**	
	0x4402 0100	0x4402 FFFF	64KB		Reserved	
	0x4402 0000	0x4402 00FF	256B		**PC**	
	0x4401 0100	0x4401 FFFF	64KB		Reserved	
	0x4401 0000	0x4401 00FF	256B		**PB**	
	0x4400 0100	0x4400 FFFF	64KB		Reserved	
	0x4400 0000	0x4400 00FF	256B		**PA**	
	0x4100 0200	0x43FF FFFF	48MB	Reserved		Reserved for future design
	0x4100 0000	0x4100 01FF	512B	GPIO	**IOP**	IO Port Input/Output

	0x4000 0000	0x40FF FFFF	16MB	Reserved		Reserved for future design

5.4. Boot Modes

During chip startup, the hardware configuration option-byte (***OB***) is used to select one of the three boot options:

- **Boot from User Application Program (AP) Flash**
- **Boot from In-System-Program (ISP)**
- **Boot from embedded SRAM**

6. Functional Description

6.1. CPU Core

6.1.1. Introduction

The chip is embedded a CPU core of Cortex®-M0 processor. The processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional DAP hardware debug functionality.

The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

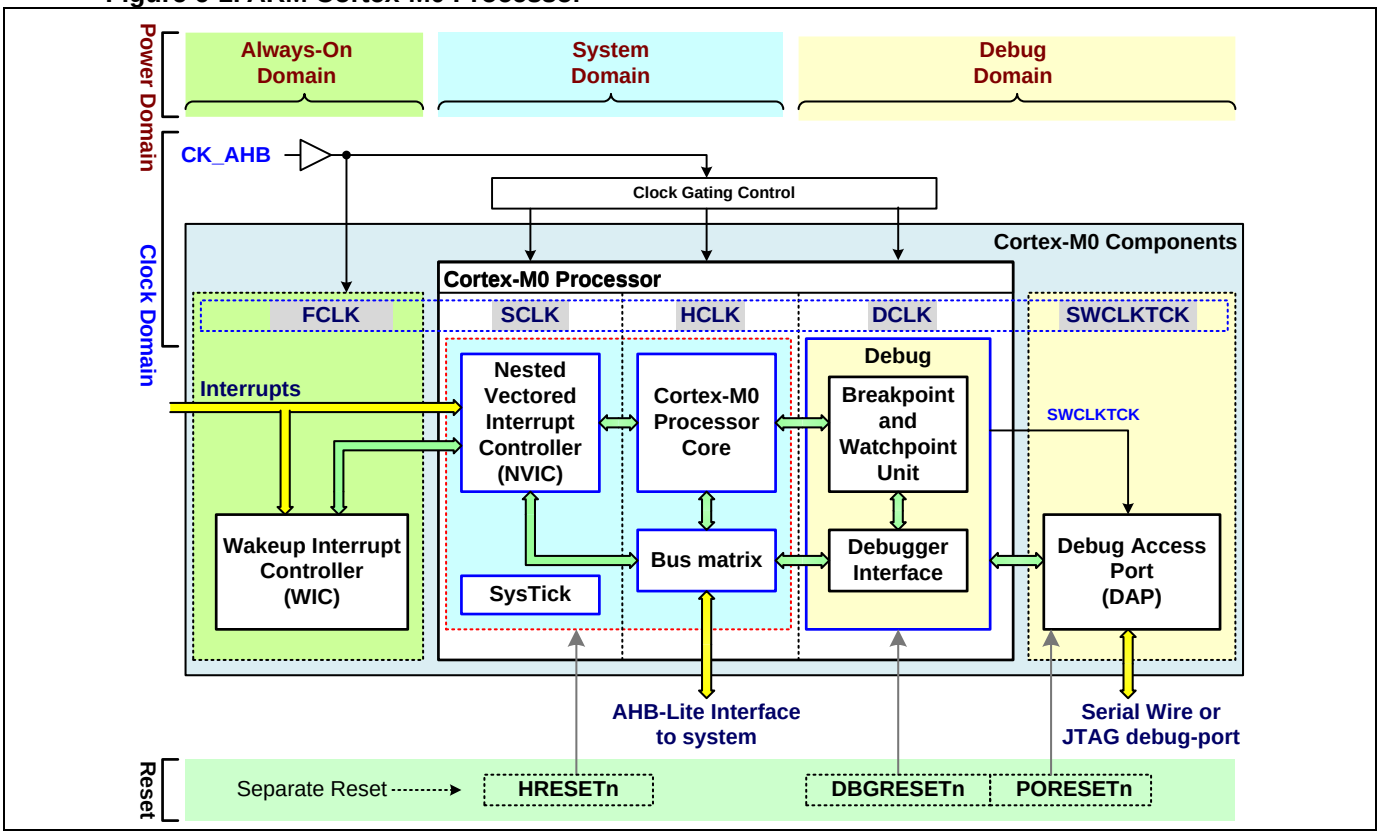
6.1.2. CPU Features

- **ARM® 32-bit Cortex®-M0 CPU**
- **Operation frequency up to 48MHz**
- **Built-in one NVIC for 32 external interrupt inputs with 4-level priority**
- **Built-in one 24-bit system tick timer**
- **Built-in one single-cycle 32-bit multiplier**
- **Built-in one SWD serial wire debugger with 2 watch points and 4 breakpoint**
- **The ARMv6-M Thumb® instruction set**

6.1.3. ARM Cortex-M0 Processor

The following diagram is showing the block of ARM® Cortex®-M0 Processor.

Figure 6-1. ARM Cortex-M0 Processor



6.2. Power Management

6.2.1. Introduction

The chip power is implemented only by single power supply input and embedded one LDO to supply the internal core logic power. The chip supports one power controller (PW) to manage Power-on reset (POR) circuit, Low-voltage reset (LVR) circuit, Brown-Out Detectors (BOD0/1), power down control and wakeup control.

It supports power-down modes: ***SLEEP*** mode and ***STOP*** modes. The power-down modes reduce chip power and provide the different power-saving scheme for chip application.

6.2.2. Chip Power Features

- **Built-in one 1.8V output regulator for core logic power**
- **Built-in two brown-out detectors**
  - **BOD0 detect 1.7V**
  - **BOD1 detect by selected level 4.2V/3.7V/2.4V/2.0V**
- **Built-in a power management controller with power-down and wakeup control**
- **Support three power operation modes**
  - **On(Normal) mode and SLEEP , STOP power down modes**

6.2.3. Power Operation Mode

There are three power operation modes of ***ON***, ***SLEEP***, ***STOP*** to be supported in the power controller.

- **ON mode**

In ***ON*** mode, the CPU is able running in full speed. All peripheral modules can use full power to do normally full function operation. These modules can enable or disable independent to save power consumption.

- **SLEEP mode**

In ***SLEEP*** mode, only the CPU is stopped and entering CPU sleep mode. All peripheral modules can be configurable to continue to operate or sleep.

In this mode, the chip can be waked up by the related interrupt or event occurs.

- **STOP mode**

The ***STOP*** mode provides the lowest power consumption. The different from SLEEP mode is that CPU is entering CPU deep-sleep mode and all peripheral modules are disabled except some special modules or devices. These modules or devices can be configurable to continue to operate in STOP mode or not. They include of IWDT, RTC, CMP modules and LVR, BOD0, BOD1 devices. The internal voltage regulator is also running in low power mode.

In this mode, the chip can be waked up by some of the external input lines (GPIO) and some events detection.

6.2.4. Power Supply

The chip power is implemented only by single power supply input for easy application PCB design. It is embedded one internal low dropout linear regulator (LDO) to generate the +1.8 volt voltage power VDDC for core logic power supply.

The **VDD** pin(s) is/are using for IO power supply input and internal LDO input. The **VSS** pin(s) is/are used to connect the external ground for internal reference ground of internal LDO, hard macros and digital logic. The **VR0** pin is the LDO output and it needs to connect bypass capacitors for normal operation. The **+VREFF** pin is the input of ADC reference voltage which can connect to **VDD** pin for general application.

6.2.5. CPU Power Down

For chip entering power down mode, the firmware must execute WFI or WFE instruction to force the CPU enters sleep mode or deep sleep mode. Then the chip will enter the power down mode of ***SLEEP*** or ***STOP***. User can configure the CPU sleep mode by setting CPU register of SLEEPDEEP after firmware executes WFI or WFE instruction.

Table 6-1. Power-Down Mode Selection

CPU	System	CPU Register
		SLEEPDEEP
Run	ON	x
sleep	SLEEP	0
deep sleep	STOP	1

6.3. System Reset

6.3.1. Introduction

During reset, all Registers are set to their initial values, and the program starts execution from the Reset Vector. The chip includes a reset source controller (RST) to manage multiple sources of reset and generates Warm reset and Cold reset signals to chip system and internal modules. This controller also provides the reset event flags for firmware, which are used to recognize the reset occurred source.

6.3.2. Chip Reset Features

- **Built-in embedded POR(power-on reset)/LVR(low-voltage reset) circuit**
- **Built-in one reset source controller**
  - **Programmable chip cold reset and warm reset for reset source**
  - **Independent software reset control for internal modules**
- **Provide multiple reset sources**
  - **POR/LVR/BOD0/BOD1/External reset pin input/Software force reset**
  - **IWDT/WWDT/ADC/Comparator**
  - **IAR(Illegal address error reset)/Flash access protect error reset**
  - **Missing clock detect (MCD) reset**

6.3.3. Chip Reset Levels

The chip provides three reset levels – POR reset, Cold reset and Warm reset. POR reset is the highest priority reset and is generated by chip hardware. Cold reset is the 2nd priority and Warm reset is the lowest priority reset.

When POR reset occurred, it will cause to generate Cold reset to chip. Also when Cold reset occurred, it will cause to generate Warm reset to chip.

- **Power-On Reset**

Power-on reset (***POR***) is used to internally reset the chip and also the CPU during power-up. The chip will keep in reset state and will not start to work until the VDD power rises above the voltage of Power-On Reset. And, the reset state is activated again whenever the VDD power falls below the POR threshold voltage. During a power off cycle, VDD must fall below the POR threshold voltage before power is reapplied in order to ensure a power-on reset.

- **Cold Reset**

Cold reset is the 2nd priority reset. The Cold reset is also generated and caused by POR reset occurred. It sends to some modules like as IWDT, WWDT … to do deep level module reset. It will cause to reload all hardware configurations ***OB*** and disable the register lock function for the modules which are support the register lock function.

- **Warm Reset**

Warm reset is the lowest priority reset. The Warm reset is also generated and caused by Cold reset occurred. It sends to all modules to clear flags and hardware circuit. It will cause to reload some hardware configuration ***OB*** and reset the registers of module to default value if the module is unlocked or not supported lock function. It will clear Warm reset source enable bits in RST controller if the RST controller is unlocked.

6.3.4. External Reset

The chip provides an external hardware reset input from **RSTN** pin, which is accomplished by holding low level for the **RSTN** pin. The **RSTN** pin is configured to as external reset pin or others (GPIO …) by hardware configuration ***OB***. To ensure a reliable power-up reset, then the hardware reset from **RSTN** pin is necessary.

6.3.5. Module Reset

For each AHB or APB control module, it can receive the system Warm reset signal to reset the module's control flags, registers and logical circuit. For some modules of IWDT, WWDT, RTC, PW, CSC and MEM, they can receive the Cold reset to unlock the register locked function and reset the module.

6.4. System Clock

6.4.1. Introduction

The chip builds in a clock source controller (CSC) for system clock source management. There are four clock sources for the system application: Internal High-frequency RC Oscillator (***IHRCO***), Internal crystal oscillator (***XOSC***), Internal Low-frequency RC Oscillator (***ILRCO***) and External Clock Input (***EXTCK***).

One ***XOSC*** oscillator is embedded for external Xtal circuit. One PLL is embedded to multiply the frequency of clock source and output clock for CPU and other peripheral modules. One missing clock detector (***MCD***) is built-in to monitor the clock of external Xtal or external clock source.

6.4.2. Chip Clock Features

- **Built-in embedded ILRCO (internal low frequency RC oscillator) by 32KHz**
- **Built-in embedded IHRCO (internal high frequency RC oscillator)**
  - **Trimmed to 11.059 or 12MHz ±1% at +25℃**
- **Built-in embedded PLL up to 48MHz output for system clock**
- **Built-in embedded XOSC oscillator with MCD for external 32KHz or 4 to 25MHz Xtal**
- **Support external clock input up to 36MHz**
- **Built-in a clock source controller with clock enable control for modules**
- **Support internal XOSC oscillator and internal ILRCO/IHRCO clock output**

6.4.3. System Clock Source

There are four clock sources for the system application: Internal High-frequency RC Oscillator (***IHRCO***), Internal crystal oscillator (***XOSC***), Internal Low-frequency RC Oscillator (***ILRCO***) and External Clock Input (***EXTCK***). Software can select the one of the four clock sources by application required and switches them on the fly. But software needs to settle the clock source stably before clock switching.

6.4.4. PLL Clock

One PLL is embedded to multiply the frequency of system clock source from ***IHRCO***, ***ILRCO***, ***XOSC*** and ***EXTCK***. The PLL input frequency range is 5~7 MHz and output clock frequency is up to 96-MHz or 144-MHz.

6.4.5. Module Process Clock Control

The CSC module is able to do the process clock enable setting and select the process clock source for internal modules. User must select the module process clock and enable the module process clock before configure the module for operation normal.

6.5. System Common Control

6.5.1. Introduction

The chip embeds one system control (SYS) module for system common control. It is including of one system event interrupt global enable control, chip manufacture identification code.

6.5.2. Features

- **System interrupt global enable control for system interrupt source**
- **Chip manufacture identification code - Device ID, Product ID, User ID, Module Options**
- **32-bit non-reset backup register**

6.6. Memory Access

6.6.1. Introduction

The chip has separate address spaces for program and data memory. The logical separation of program and data memory allows the memory to be accessed by 32bit addresses, which can be quickly stored and manipulated by the CPU. The chip supports one memory controller (MEM) to manage the internal flash memory and SRAM access operation.

6.6.2. Features

❖ **Embedded Memory**

- **Built-in embedded 32K bytes flash memory for application code**
- **Built-in embedded 4K bytes SRAM**

❖ **Memory Controller Features**

- **Support ICP (In-circuit program) for ISP boot code update through SWD interface**
- **Support ISP (In-system program) for application code update**
  - **Support programmable ISP flash memory size for ISP boot code**
  - **Provide fixed 1K bytes ISPD flash memory as ISP private data**
- **Support IAP (In-application program) for application data update**
  - **Support programmable 1M bytes address low boundary**
- **Support flash memory page erase in 1K bytes**

6.6.3. Memory Controller

A memory controller is supported to access on chip flash memory, SRAM on AHB bus. It includes ***ICP*** (In-Circuit Programming)/ ***ISP*** (In-System Programming)/ ***IAP*** (In-Application Programming) circuits for flash memory accessing, option byte loader for hardware option registers loading.

The chip has up to 32K bytes of embedded main flash memory for code and data, programmable memory size of embedded system flash memory for boot load code and 64 bytes of embedded option-byte flash memory for chip configuration.

The memory controller (MEM) supports to Read/ Program (Write)/ Erase the flash memory. User can directly read the data from flash memory by CPU read instruction commands and do not need through any register. For “Program” mode, MEM provides the 32-bit data write operation into flash memory for new data updated. For “Erase” mode, the Erase address is only valid at low 10-bit CPU address=0 (X..X00 0000 0000B) and is addressing 1K-byte alignment.

6.6.4. ICP/ISP/IAP for Flash Memory

There are 3 flash access modes are provided in chip for ICP, ISP and IAP application: program mode and read mode. ICP is allowed to update the entire contents of the flash memory by using the hardware SWD interface and no any firmware request. Others, User can use these two modes of ISP and IAP to update new data into flash storage and get flash content by a firmware flash memory access handler.

6.6.5. Hardware Option Byte Flash Memory

There can be up to **64** bytes of on-chip Option Bytes Flash memory. It is used to store the hardware option configuration setting.

The embedded option-byte (***OB***) flash memory will load into the hardware configuration option-byte register (***OR***) after power-on reset. The hardware configuration ***OR*** are designed to configure the clock source from internal RC oscillator or crystal oscillator; the booted memory selection from AP, ISP flash memory or SRAM; the memory size of IAP flash memory; other chip configurations … etc.

6.7. GPIO

6.7.1. Introduction

The chip has following I/O ports: **PA[0:3][8:15]**, **PB[0:3][8:11][13:14]**, **PC [0:6][8:14]**, **PD[0:3][7:10]**. Support maximum 44 GPIO pins for LQFP48 package. **RSTN** pin is an alternated function pin on **PC6**. If select external crystal oscillator as system clock input, **PC13** and **PC14** are configured to **XIN** and **XOUT**. The exact

number of I/O pins available depends upon the package types.

The chip has built in several IO mode control **(PA/PB/PC/PD)** modules for each GPIO port. These modules are used for GPIO pin IO mode control, alternated function selection, driver strength setting, input inverse selection, pull-high enable, deglitch filter setting and high speed enable. Also one IO Port access control **(IOP)** module is built-in to control the input and output state of GPIO mode for all GPIO ports.

6.7.2. Features

- **Support general purpose IO pins for application**
  - **Maximum 44 GPIO pins for LQFP48 package**
- **Provide selectable IO modes by pin independent**
  - **Push-Pull output**
  - **Quasi bidirectional**
  - **Open-drain output**
  - **Input only with high impedance**
  - **Analog IO**
- **Flexible pin alternate function selection**
- **Support programmable drive strength by pin independent**
- **Support IO deglitch filter by pin independent**
- **Support input inverse selection by pin independent**
- **Support pull-high option by pin independent**
- **Support high speed option by pin independent**
- **GPIO pin state and IO mode setting keep optional after reset**

6.7.3. GPIO Control Block

The GPIO Control block includes IOM (IO pad Mode control), IOP (IO Port access control) and AFS (Alternate Function Select) blocks.

- **IO Operation Mode**

The IO operating modes are supported analog IO, digital input, push-pull output, and open-drain output, quasi-bidirectional. Provide selectable IO modes by pin independent.

The IO mode control block supports programmable IO operation modes, output high speed option, pull-high option, output drive strength, IO deglitch filter and input inverse selection by pin independent.

- **IO Port Access**

When the AFS setting is set GPIO function mode for any IO pin, user can directly set the logical output or get the logical input for the IO pin. There is one independent data out register bit to store the output logic value for each GPIO pin. Also user can directly read the input data register bit to get the GPIO pin logical state for each GPIO pin.

For firmware control, there are one set control bit to set the data out register bit and one clear control bit to clear the data out register bit for each GPIO pin.

The chip provides one set-or-clear register control bit to set, clear the data out register bit or read pin status for each GPIO pin. The register bit is written 1 to set data bit and written 0 to clear data. Read the register bit to get the GPIO pin status. As this register bit is cost eight bit memory space, firmware is easy to control single GPIO pin by CPU byte-access instruction command. It is like the bit access IO control of 8051 MCU.

- **Alternate Function Select Control**

User can configure the alternate function between module function IO and IO pins through the AFS matrix for each GPIO pin independently. Usually the AFS default setting is GPIO function for each GPIO pin except the **XIN**/**XOUT**, **SWCLK**/**SWDIO** and **RSTN** function pins. These pins may be changed by hardware configuration ***OB***.

6.8. Interrupt

6.8.1. Introduction

After reset, the CPU begins execution from the location of reset interrupt vector (0x00000004) addressing, where should be the starting of the user's application code. To service the interrupts, the interrupt service locations (called interrupt vectors) should be located in the address 0x000000BF~0x00000000.

The chip is built-in ARM® Cortex® M0 CPU and is embedded a NVIC (Nested Vectored Interrupt Controller) for 32 external interrupt inputs with 4-level priority. Also builds in an EXIC (External Interrupt Controller) module and connects to NVIC.

6.8.2. Interrupt Features

- **Built-in one NVIC for 32 external interrupt inputs with 4-level priority**
- **Built-in one EXIC (external interrupt controller) for NVIC connection**
  - **Independent high/low level and rising/falling edge trigger selection**
- **Built-in one WIC (wakeup interrupt controller) for wakeup event control**
- **All GPIO pins can be configured as interrupt source and key pad input**
  - **Support port OR logic for interrupt function**
  - **Support port AND logic for KBI function**
- **Support external pins for CPU NMI/RXEV/TXEV function**
  - **Configurable pin for CPU NMI input function**
  - **Configurable pin for CPU RXEV input function**
  - **Configurable pin for CPU TXEV output function**

6.8.3. Interrupt Structure

Each interrupt is assigned a fixed location in the program memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. NMI interrupt, for example, is assigned to location 0x00000008. If NMI is going to be used, its service routine must begin at location 0x00000008.

The interrupt service locations are spaced at an interval of 4 bytes: 0x00000004 for Reset Interrupt, 0x00000008 for ***NMI***, 0x0000000C for ***Hard-Fault***, 0x0000002C for ***SVCall***, 0x00000038 for ***PendSV***, 0x0000003C for ***SysTick***, etc.

- **Exception types**

The NVIC has 7 exception types: ***Reset***, ***NMI***, ***HardFault***, ***SVCall***, ***PendSV***, ***SysTick*** and Interrupt (IRQ). The NVIC supports 32 external interrupt input. An interrupt is an exception signaled by a peripheral or generated by a software request. The four priority level interrupt structure allows great flexibility in handling these interrupt sources.

- **Interrupt Sources**

The ‘Pending Bits’ are the interrupt flags that will generate an interrupt if it is enabled by setting the ‘Set Enable Bit’. The ‘Pending Bits’ can be set or cleared by software, with the same result as though it had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled in software. The ‘Priority Bits’ determine the priority level for each interrupt. The ‘Priority within Level’ is the polling sequence used to resolve simultaneous requests of the same priority level. The ‘Vector Address’ is the entry point of an interrupt service routine in the program memory.

Table 6-2. Interrupt Source Table

NVIC						Comment
Exception No.	IRQ No.	Interrupt Name	Priority	Activation	Exception handlers	
0	-	Initial	-			
1	-	Reset	-3	Asynchronous		Reset exception
2	-14	NMI	-2	Asynchronous	System handlers	Non Maskable Interrupt
3	-13	HardFault	-1	Synchronous	Fault handler	Cortex-M0 Hard Fault Interrupt
4~10	-	Reserved	-			
11	-5	SVC	Configurable	Synchronous	System handlers	Cortex-M0 SV Call Interrupt
12~13	-	Reserved	-			
14	-2	PendSV	Configurable	Asynchronous	System handlers	Cortex-M0 Pend SV Interrupt
15	-1	SysTick	Configurable	Asynchronous	System handlers	Cortex-M0 System Tick Interrupt
16~47	0~31	-	Configurable	Asynchronous	ISRs	Peripheral Interrupts
Configurable : Programmable priority level 0~3						

- **Interrupt Priority**

The priority scheme for servicing the interrupts has four interrupt levels. The priority bits in CPU registers, IPR0-7, SHPR2 and SHPR3, determine the priority level of each interrupt.

The interrupt priority registers provide an 8-bit priority field for each interrupt and each register holds four priority fields. The processor implements only bits [7:6] of each field, bits [5:0] read as zero and ignore writes.

Higher-priority interrupt will be not interrupted by lower-priority interrupt request. If two interrupt requests of different priority levels are received simultaneously, the request of higher priority is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determine which request is serviced. The table of “interrupt sources” shows the internal polling sequence in the same priority level and the interrupt vector address. The lower exception number gets the higher priority.

6.8.4. Nested Vectored Interrupt Controller

The Cortex®-M0 processor integrates a configurable Nested Vectored Interrupt Controller (NVIC) that supports low latency interrupt processing and includes a non-mask interrupt (***NMI***). The NVIC provides a zero-jitter interrupt option and four interrupt priority levels.

Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with sleep mode. Optionally, sleep mode support can include a deep sleep function that enables the entire device to be rapidly powered down.

6.8.5. Wakeup Interrupt Controller

The chip includes a Wakeup Interrupt Controller (WIC) which can detect an interrupt or wakeup event from EXIC and wake the processor from deep sleep mode. The WIC is enabled only when the DEEPSLEEP bit in the CPU register of SCR is set to 1. The WIC is not programmable, and does not have any registers or user interface. It operates entirely from hardware signals.

6.8.6. External Interrupt Controller

The External Interrupt Controller (EXIC) includes four external port interrupt blocks (EXINT) to manage the external pin input interrupt events, one wakeup control block for wakeup event control and control the NMI/RXEV events. The EXIC also do as the interface controller between internal modules and NVIC for the interrupt and wakeup events management

6.9. General Purpose Logic

6.9.1. Introduction

The chip builds in one general purpose logic (GPL) module. It provides the combined functions of Data Order Change, Parity Check, Data Inverse and CRC.

6.9.2. Features

- **Support data inverse, bit order change, byte order change and parity check**
  - **Data bit order change for 8/16/32-bit reverse**
  - **Data byte order change between Little endian and Big endian for 32-bit range**
  - **Parity Check for 8/16/32 bit range**
- **Support CRC (Cyclic Redundancy Check) calculation**
  - **Programmable CRC initial value**
  - **CRC output bit order change**
  - **CRC computation done in 4/2/1 AHB clock cycles for 32/16/8-bit data**
- **CRC with fixed common polynomial**
  - **CRC8 polynomial 0x07**
  - **CRC16 polynomial 0x8005**
  - **CCITT16 polynomial 0x1021**
  - **CRC32(IEEE 802.3) polynomial 0x4C11DB7**
- **Input data are buffered with DMA capability**

6.10. APB Common Control

6.10.1. Introduction

The chip builds in one APB (APB bus common control) module for the common control of APB devices.

6.10.2. Features

- **Timer synchronous enable global control for TMx timer modules**
- **Timer internal trigger/clock source selection for TMx timer modules**
- **OBM(Output Signal Break and Modulation) control**
  - **Support two sets of OBM for output signal break and modulation control**
- **Infrared Remote Modulation Output**

6.11. Direct Memory Access

The chip is built-in a direct memory access controller (DMA) which is used to improve the performance of data transfer between peripheral and memory, memory to memory and peripheral to peripheral. Data can be quickly transfer by through DMA without costing any CPU resources.

Notify: The sign of (n= DMA channel index number) is using for Registers, Signals and Pins/Ports in the descriptions of this chapter.

6.11.1. Features

- **One configurable channels with dedicated hardware DMA requests**
  - **Access to Memory, APB and AHB Peripherals as source and destination**
  - **Support SRAM/Flash as memory source and SRAM as memory destination**
  - **Peripherals are including of ADC0, I2Cx, URTx, SPIx, TM36 and GPL modules**
- **DMA transfer management type**
  - **memory-to-memory**
  - **peripheral-to-memory**
  - **memory-to-peripheral**
  - **peripheral-to-peripheral**
- **Programmable transfer number of data and up to 65535**

- **Programmable burst length 1,2,4**
- **Support transfer loop mode and start address auto reload control**
- **Provide single/block/demand mode for external pin trigger request**

6.11.2. DMA Control Block

The DMA controller (DMA) is used to transfer data between these sources and destinations of AHB peripheral, APB peripheral, SRAM and internal Flash. One external pin of DMA_TRG0 is able to input as the trigger signal of DMA data transfer.

6.12. ADC

6.12.1. Introduction

The chip builds in one ADC0 module which embeds one 12-bit successive approximation ADC (analog-to-digital converter), one PGA (programmable gain amplifier) with gain 1~4 and digital logic for output code control. It supports the configurable multiplexed channels those include 12 external and 4 internal sources. The analog-to-digital conversion can be performed in one-shot, continuous, one-loop scan or continuous loop scan modes.

6.12.2. Features

- **12-bit SAR ADC with 800Ksps**
  - **Configurable resolution : 12/10/8-bit**
  - **Configurable sampling time**
- **Provide external 12 channels and internal 4 channels input**
  - **Internal channel source : VBUF, VSSA, LDO VR0 output, ADC Reference Voltage**
- **Support auto-sampling and trigger by external pin , internal events and software bit**
- **Data alignment for output code left/right justify**
- **Built-in input buffer stage with bypass option**
- **Programmable offset**
- **Programmable gain : 1~4**
- **Interrupt generation at the end of sampling, end of conversion, end of scan conversion**
- **Support voltage window detect**
  - **Two level programmable window threshold**
- **Built-in one hardware accumulator for ADC output code**
- **Support one-shot/channel scan/loop scan**
- **ADC data are buffered with DMA capability**
- **Support wait mode**
  - **Prevents ADC overrun in application with low frequency**

6.12.3. ADC Control Block

The ADC control block consists of an analog multiplexer (AMUX) with 16 input channels, an **800K**sps/**12**-bit SAR (successive-approximation-register) ADC, reference voltage circuit, ADC conversion trigger start control block and change scan control block.

- **ADC Input Channels**

The analog multiplexer (AMUX) selects the inputs to the ADC, allowing any of the input pins to be measured in single-ended mode.

The analog input pins used for the A/D converters also have its I/O pins for digital input and output function. In order to give the proper analog performance, a pin that is being used with the ADC should have its digital output as disabled. It is done by putting the port pin into the input-only mode. And when an analog signal is applied to the **ADC_I[15:8][3:0]** pin and the digital input from this pin is not needed, software could set the corresponding pin to AIO mode to turn off the digital input buffer to reduce power consumption.

- **Single-End Input Mode**

The ADC supports single-end input operation modes. The ADC can convert the ADC output to unsigned code.

- **ADC Sampling Time**

For input signal quality and conversion speedy issue, user can adjust the ADC sampling time. Usually increase the ADC sampling time to get more stable voltage and better ADC performance if the conversion rate and signal bandwidth are reasonable and valid for actual application.

- **ADC Conversion Mode**

  The ADC is supported three conversion modes of One Shot, Channel Scan and Loop Scan.

- **ADC Output Control**

  When an ADC conversion is complete, the ADC raw code is generated and sends to the ADC output control blocks those are including of Digital Offset Adjuster, Signed Code Converter, Digital Resolution Adjuster, Voltage Window Detector, Code Limiter and Data Alignment Adjuster.

  The ADC output code will be adjusted by the ADC output control blocks and store the conversion result date to the ADC data register.

- **Voltage Window Detect and Code Limit**

  The ADC can compare the input voltage by a threshold window. Also the ADC output code can be compared by a code limit area to skip or clamp the code by the same threshold window.

- **ADC Data Sum Accumulate**

  The ADC built-in one hardware accumulator for ADC output code. The accumulator is used to accumulate the sequential ADC data with programmable data number and records the sum to the summary registers. User can set the accumulated ADC data number. The ADC is supported three sum data registers and user can get the accumulated sum from these registers.

- **ADC Wait**

  The ADC supports a wait mode function to prevent ADC overrun in application with low frequency ADC sampling clock.

6.13. Analog Comparator

6.13.1. Introduction

The chip builds in one CMP module which embeds two general purpose analog comparators with flexible input multiplexer, two internal voltage references of R-ladder and independent digital synchronized filter for each analog comparator. These analog comparators can be configured to four standalone comparators or a combined window comparator. The module provides the comparator output result status bit and the interrupt flags of rising edge or falling edge change. Also the output result can be output to external pin or internal other modules for trigger event.

6.13.2. Features

- **Provide 2 fast Rail-to-rail comparators**
- **Programmable 64-step threshold of internal voltage reference**
- **Provide external total 6 channels input for all comparators**
- **Provide flexible 6 channels input for each +/- input path selection**
- **Programmable response time for optimal current consumption**
- **Combined window comparator from two comparators**
- **Selectable compare output polarity**
- **Support power-down wakeup**
- **Compare output to I/O , interrupt or as internal module trigger event**
  - **Timer internal trigger, Capture events, or Break events**
- **Support analog watch dog as a reset source**

6.13.3. CMP Control Block

The CMP module includes four general purpose analog comparators CMP0~1 by the same design structure and two internal voltage references ***IVREF***/***IVREF2*** by R-ladder structure. Each one is with the independent input multiplexer, digital synchronized filter and digital output circuit. The ***IVREF*** is using for CMP0 and the ***IVREF2*** is using for CMP1.

The analog comparator is built-in two internal voltage references – ***IVREF*** and ***IVREF2*** with 64-steps R-ladder structure. They can use as one of the analog comparator input and compare with another input from external source.

The analog multiplexers (AMUX) select the inputs of **CMPn_I0**, **CMPn_I1** to each analog comparator and CMP_**C0**, **CMP_C1** to all analog comparator CMP0/1. It allows any of the input pins to CMP0/1/2/3 to be compared between positive input and negative input.

The analog input pins used for the comparators also have its I/O port's digital input and output function. In order to give the proper analog performance, a pin that is being used should have its digital output as disabled. It is done by putting the port pin into the digital input mode. And when an analog signal is applied to the analog input pin and the digital input from this pin is not needed, software could set the corresponding pin to AIO mode to reduce power consumption in the digital input buffer.

6.14. IWDT

6.14.1. Introduction

The chip has one independent Watch-dog timer to use as a recovery method in situations where the CPU may be subjected to software upset. It will trigger system reset when the counter reaches a given timeout value.

6.14.2. Features

- **8-bit down counter with 12-bit prescaler and clocked by its own CK_ILRCO**
- **Operating capability in SLEEP and STOP modes**
- **Selectable reset or interrupt when the counter underflow**
- **Support two early wakeup comparators with interrupt**
- **Support register key-protected and reset-locked functions**

6.14.3. IWDT Control

The IWDT watch-dog timer consists of a 12-bit prescaler and an 8-bit timer. When the watch-dog timer is enabled, software should always reset the timer before the timer is timeout. When the watch-dog timer is reset, the timer will be reloaded 0xFF value to restart counting.

If the chip is out of control by any disturbance, the firmware may miss to reset the timer and the timer timeout will be coming. It makes the IWDT generating a reset event and sends it to Reset Source Controller (RST) to do as the warm reset events or cold reset events.

The IWDT is able to record default initialized value in hardware option byte (***OB***) about IWDT on/off, input clock divider value, IWDT registers write protection.

The IWDT is able to operate in ***STOP*** mode and the APB clock is stopped and the module is asynchronous control for all logic.

The IWDT supports to wakeup chip in ***STOP*** mode by the events of watch-dog timer underflow and early wakeup-0/1 detection. When the chip is entering ***STOP*** mode and any of these IWDT wakeup events is happened, the IWDT will send the wakeup event to Power Controller (PW) to do as the system wakeup events.

6.15. WWDT

6.15.1. Introduction

The system window watchdog is used to detect the occurrence of a software fault which causes the application program abnormal. The watchdog circuit generates a system reset when the counter reaches a given timeout value.

The WWDT has a configurable time-window that can be programmed to detect abnormally late or early application behavior.

6.15.2. Features

- **10-bit counter with 1 or 256 divider , 1/2/4~/128 divider**
- **Configurable time-window to detect abnormally late or early application behavior**
- **Selectable reset or interrupt when the counter is underflow or reloaded outside the window**
- **Support warning interrupt**
- **Support register key-protected and reset-locked functions**

6.15.3. WWDT Control

The WWDT watch-dog timer consists of one /1 or /256 clock prescaler, one 7-bit clock divider and one 10-

bit timer. When the watch-dog timer is enabled, software should always reset the timer before the timer is timeout. When the watch-dog timer is reset, the timer will reload the value to restart counting.

When the firmware is out of control, which may miss to reset the timer and the timer timeout will be coming. It makes the WWDT generating a reset event and sends it to Reset Source Controller (RST) to do as the warm reset events or cold reset events. If the firmware reset the timer and the counter value is over the threshold value of window compare threshold in the same time, it also makes the WWDT generating a reset event.

6.16. RTC

6.16.1. Introduction

The real-time clock is an independent 32-bit timer. The RTC provides a time clock with programmable alarm interrupt. User can use as a calendar with software programmable alarm seconds, minutes, hours, day, and date.

The RTC provides a wakeup flag to perform auto wakeup from power down mode with interrupt.

6.16.2. Features

- **Built-in 32-bit counter with selectable clock source**
- **Support alarm function with 32-bit programmable compare register**
- **Support time-stamp function for event saving**
- **Support wakeup from Stop mode**
- **Support register key-protected and reset-locked functions**

6.16.3. RTC Control

The RTC supports an alarm function and one register to sets the RTC alarm compare value. When the RTC timer value is matched with RTC alarm compare value, the RTC alarm flag is asserted and generates an interrupt. Also the RTC can capture from the 32-bit timer value or reload value to the 32-bit timer.

The RTC supports a time stamp function by external input. User can select input trigger edge of rising edge, falling edge or dual-edge. When an external input signal is matched, the RTC time stamp flag is asserted and generates an interrupt.

One **RTC_OUT** output is able to output the RTC internal signals to internal modules or external pin. There are four signals of timer overflow signal toggle output, time stamp trigger event, timer input periodic clock signal and alarm compare output event which can be selected and sent from **RTC_OUT** output.

The RTC is able to operate in ***STOP*** mode and the APB clock is stopped and the module is asynchronous control for all logic.

The RTC supports to wakeup chip in ***STOP*** mode by the events of timer overflow, timer input periodic clock and alarm compare output. When the chip is entering ***STOP*** mode and any of these RTC wakeup events is happened, the RTC will send the wakeup event to Power Controller (PW) to do as the system wakeup events.

6.17. Timer

6.17.1. Introduction

The chip has five Timer/Counter modules: TM00, TM01, TM10, TM16 and TM36. All of them can be configured as timers or event counters.

TM0x has an 8-bit timer/counter with 8-bit prescaler. TM1x has a 16-bit timer/counter with 16-bit prescaler. TM36 has a 16-bit timer/counter with 16-bit prescaler and embeds four input capture/output compare channels.

6.17.2. Features

- **Provide five timers/counters : TM00,TM01,TM10,TM16,TM36**
- **Timer module common functions**
  - **Selectable Full-counter , Cascade , Separate modes**
  - **Multiple internal and external signals as timer clock source or trigger source**
  - **Internal timer events output to pin or other modules as input trigger event**
  - **Support timer reset , trigger start and clock gating for trigger source function**
  - **Timer overflow as clock output to external pin output**
  - **Programmable counter auto-stop mode**

- Main counter support up/down control (TM16 /TM36 only)
- 2nd counter support up/down control (Separate mode)

- Provide TM36 timer module
  - 32-bit timer/counter
  - 4 CCP (input Capture/output Compare/PWM) channels
  - 3 CCP channels with OCN (complementary output compare)
  - PWM function with center-align, dead time control and break control
  - Support OC comparator split to two separated comparators mode
  - Programmable dead time control
  - QEI(Quadrature Encoder Interface) support
  - External input timer up/down control
  - One IC and three OC with DMA capability
- Provide TM1x timer modules
  - 32-bit timer/counter
  - External input timer up/down control (TM16 only)
- Provide TM0x timer modules
  - 16-bit timer/counter

6.17.3. Timer Modules' Function Table

The following table is showing the implemented functions of Timer modules.

Table 6-3. Timer Modules' Function Table

Module Functions	TM00	TM01	TM10	TM16	TM36
Timer/Counter total bits	16	16	32	32	32
Timer Cascade Mode	yes	yes	yes	yes	yes
Timer Separate Mode	yes	yes	yes	yes	yes
Timer Full-Counter Mode	yes	yes	yes	yes	yes
Independent channels					4
Internal TRGI lines	8	8	8	8	8
External TRGI lines	1	1	1	1	1
Output TRGO lines	1	1	1	1	1
Output CKO lines	1	1	1	1	1
Input Capture IC lines					4
Output OC lines					4
Output OCN lines					3
Output OCH lines					4
Input Break lines					1
PWM separated two					yes
PWM edge-align					yes
PWM center-align					yes
Dead-time generator					yes
Up/Down of 1st Timer	U	U	U	U/D	U/D
Up/Down of 2nd Timer	U/D	U/D	U/D	U/D	U/D
Timer auto Stop	yes	yes	yes	yes	yes
QEI timer U/D control					yes
3-input XOR to CH-0					yes
DMA request capability					yes

Note 1. Timer Cascade Mode ~ 16-bit_counter+16-bit_prescaler or 8-bit_counter+8-bit_prescaler
2. Timer Separate Mode ~ two 16-bit_counter or 8-bit_counter
3. Timer Full-Counter Mode ~ 32-bit_counter or 16-bit counter

6.17.4. Timer Control Block

The TMx module is including of a Trigger/Clock control block, a Counter Stage, an Capture/Compare control block and Input/Output Stages of channel I/O control (TM3x only) and a Break control block (TM36 only). TMx support three timer operation modes: (1) Cascade Mode (2) Separate Mode (3) Full-Counter Mode.

- **Trigger Control Block**

The Trigger Control block has two functions, one is to control the timer trigger input events and another is to control the timer trigger output events.

The timer trigger input events are including of Reset Timer, Gated Clock and Timer-Start Trigger for Main Timer and 2nd Timer. The input source of the timer trigger input events is selected from external trigger signal, internal trigger signals or external channel input signal of **TMx_IN0**/**TMx_IN1**.

The source of the timer trigger output events are able to come from many internal events or signals of this timer module. Also user can use the software register to set the trigger output directly. This source of output event can select and invert the output signal by registers.

- **Timer Input/Output Channels**

The following table is showing the channel input signals for each timer module. TM0x and TM1x modules are no channel input selection function as the input capture/output compare is not support. Each channel has four input lines.

- **Timer Input Capture and Output Compare**

The input capture (IC) and output compare (OC) functions are only supported for TM3x module. TM0x and TM1x modules are no the functions of the input capture/output compare.

User can configure each of the timer IC/OC channel independently as input capture, output compare or PWM mode.

- **PWM Dead-Time Control**

The Dead Time Generator (DTG) is only support for TM36 module. User can use with the DTG function and configure the timer channel as 16bit PWM mode or Two 8bit PWMs mode.

- **Break Control Block**

The break control block is only support for TM36 module. The module can input the break events from internal events, external events or software register to break the timer output signals.

- **QEI Control Block**

The QEI (Quadrature Encoder Interface) control block is only support for TM26 and TM36 modules. The QEI block can input from two external signals to control the Main Timer up or down counting. The QEI block provides five control modes and user can enable QEI control and configure the QEI control mode by register.

When the QEI control block is enabled, the timer will reset during up counting or reload the auto-reload value during down counting if detect the index signal active pulse.

6.18. I2C

6.18.1. Introduction

The I2C interface is a two-wire, bi-directional serial bus. It is ideally suited for typical microcontroller applications. The I2C protocol allows the systems designer to interconnect up to 128 different devices using only two bi-directional bus lines, one for clock (SCL) and one for data (SDA). The I2C bus provides control of SDA, SCL generation and synchronization, arbitration logic, and START/STOP control and generation. The only external hardware needed to implement this bus is a single pull-up resistor for each of the I2C bus lines. All devices connected to the bus have individual addresses, and mechanisms for resolving bus contention are inherent in the I2C protocol.

The I2C module builds in the shadow buffer and data register to improve transmit and receive communication performance.

6.18.2. Features

- **Provide one I2c module : I2C0**
- **I2C module common functions**
  - **Support master and slave mode**
  - **Support programmable clock rate control and clock rate up to 1 MHz**
  - **Support programmable high/low period control for master mode**

- **Support clock stretching for slave mode**
- **Support general call function**
- **Support multi-master processing capability**
- **Support both Byte mode and Buffer mode flow control**
- **Support Byte mode bus event code for simplex firmware control**
- **Support Buffer mode 4-byte data buffer and 32-bit data register for high speed communication**
- **Received and transmitted data are buffered with DMA capability**
- **Support slave address hardware detection wakeup from STOP mode**
- **Support SMBus timeout detection**

6.18.3. I2C Control

- **I2C Data Byte Mode Control**

  The module is provides one bus event register to get the I2C Event Code for software byte-mode simplex control. An 8-bit shift buffer and an 8-bit data register are using for the I2C data Byte mode.

- **I2C Data Buffer Mode Control**

  The module implements an 8-bit shift buffer, a 32-bit shadow buffer and a 32-bit data register for data flow control of data Buffer mode. The following diagram is showing the I2C Data Buffer mode control block.

- **I2C Master Timing Control**

  Two timing control registers are simply used to configure the I2C timing of high and low cycle time.

- **I2C Timeout Timer Control**

  The module is provides one 8-bit timeout timer (TMO) for I2C access time-out control.

6.19. UART

6.19.1. Introduction

The UART module support full-duplex transmission, meaning it can transmit and receive simultaneously. The module builds in the shadow buffer and data register by transmit and receive independently to improve transmit and receive communication performance. It can commence reception of a second byte before a previously received byte has been read from the register. However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.

The module can operate in multiple modes: asynchronous communication, synchronous communication, SPI master, ***SmartCard***, ***LIN***, multi-processor mode. The asynchronous communication operates as a full-duplex Universal Asynchronous Receiver and Transmitter (UART), which can transmit and receive simultaneously and at different baud rates.

6.19.2. Features

- **Provide two identical UART modules : URT0,URT1**
- **UART module common functions**
  - **Support UART , Synchronous , SPI master , SmartCard , LIN , Multi-processor mode**
  - **Provide precise UART baud-rate control by programmable oversampling rate**
  - **Support baud rate up to 6 Mbit/s**
  - **Programmable data word length - 7 or 8 bits**
  - **Selectable MSB or LSB first data order**
  - **Configurable stop bits - 0.5,1,1.5 or 2 stop bits**
  - **Hardware parity checking and parity generation**
  - **Programmable 4~32 oversampling rate**
  - **Swappable TX/RX pin configuration**
  - **Separate signal polarity control for transmission and reception**
  - **Support a timeout timer for Idle/RX/Break/Calibration timeout detection**
  - **Support 4-byte data buffer and 32-bit data register for high speed communication**
  - **Received and transmitted data are buffered with DMA capability**
  - **Support auto baud-rate detection and calibration**
  - **Support Multiprocessor communication for master and slave mode - Idle-Line , Address-Bit**

- **Support Low speed UART-like frame format IrDA**
- **Support transceiver hardware flow control by CTS/RTS signals only**
- **Provide driver enable signal to activate the transmission for one line communication**
- **Support transmission-error hardware detection and auto resent control for Smart-card**
- **Support receiving parity error hardware detection and auto retry control for Smart-card**

6.19.3. UART Control

The UART module is able to configure the control mode from one of UART (asynchronous mode), SYNC (synchronous mode), IDLE (multi-processor idle mode) and ADR (multi-processor address-bit mode).

The UART module implements two operation modes of Idle-Line mode or Address-Bit mode for multi-processor communication.

- **UART Data Buffer**

The UART module implements two 8-bit shift buffers, two 32-bit shadow buffer and two 32-bit data register for data flow control and reduce the CPU overhead.

- **UART Data Character Format Setting**

The UART character is defined as the data unit for UART transaction. Generally, the character is including of one Start bit, 8-bit or 7-bit data bits and one Stop bit. Others, it also can insert one parity bit (PAR) and one address bit (ADR) for multi-processor mode.

- **UART TMO Timeout Control**

The module is provides one 16-bit timeout timer (TMO) for UART access time-out control. It can configure as an UART timeout timer or a general using timer by register. When the TMO timer is configured as a general using timer, there is one reload register for the timer.

The TMO timer can use to detect Idle Line condition, Break Timeout, RX Timeout, Idle Timeout and Baud-Rate Calibration Timeout.

- **UART Baud-Rate Control**

The Baud-Rate timer (BR) can configure as an UART Baud-Rate generator or a general using timer. The Baud-Rate timer generator is able to output the internal clock for UART communication Baud-Rate control.

- **UART Mute Mode Control**

The UART module is support a mute mode to disable receiving data character but the shift buffer is still operation for status detection. When the UART is entering mute mode, the RX shadow buffer is never load into data from shift buffer. The mute mode is useful for multi-processor communication.

The mute mode can be automatic by hardware detection to enter or exit by register configuration. Also it can be directly forced to enter or exit by register setting and user can manual to control the mute mode entering and exiting.

- **UART IrDA Control**

The UART module is built an IrDA encoder and an IrDA decoder in the data interface for IrDA communication.

- **UART DE Control**

The UART module provides one data enable signal of **URTx_DE**. This signal is used to indicate the data transmitted period and can output to external signal drive device. The external signal drive device can receive the UART TX signal and drive it with a signal enhanced buffer to the target of UART receiver for long distance communication.

- **UART Hardware Flow Control**

The UART supports a hardware flow control function for data transaction and provides two control signals of **URTx_CTS** (Clear to Send) and **URTx_RTS** (Request to Send) for the hardware flow control.

6.20. SPI

6.20.1. Introduction

The chip provides a high-speed serial peripheral interface (SPI). SPI is a full-duplex, high-speed and synchronous communication bus with two operation modes: Master mode and Slave mode. SPI clock rate can be supported up to 24 MHz in Master mode or up to 16 MHz in Slave mode under a 48MHz system clock.

The SPI module builds in the shadow buffer and data register by transmit and receive independently to improve transmit and receive communication performance.

6.20.2. Features

- **Support one SPI module – SPI0**
- **Support master and slave mode**
  - **Support full duplex , half duplex or simplex communication mode**
  - **Support no NSS(slave select signal) communication mode**
- **Support programmable clock rate control**
  - **Support clock rate up to 24 MHz for master and 16 MHz for slave**
- **Selectable 4~32-bit frame size**
  - **Support 4-byte data buffer and 32-bit data register for high speed communication**
- **Received and transmitted data are buffered with DMA capability**
- **Support multi-master processing capability**
- **Selectable clock polarity and phase**
- **Selectable MSB or LSB first data order**
- **NSS line management by hardware or software for both master and slave**
- **Configurable data transfer modes**
  - **Standard SPI mode (separated transmit and receive line)**
  - **Single SPI mode with bidirectional data transfer**
  - **Dual SPI mode with bidirectional data transfer**
  - **Quad SPI mode with bidirectional data transfer**
- **Data transmit/receive overrun detect**
- **Support hardware master mode failure detection and auto slave mode change**

6.20.3. SPI Control

- **SPI Data Buffer Mode Control**

  The module implements two 32-bit shift buffers, two 32-bit shadow buffer and two 32-bit data register for data flow control and reduce the CPU overhead.

- **SPI Data Frame**

  User can set the data frame bit size from 4-bit to 32-bit by register. Also user can configure the frame data order by Lsb first or Msb first.

- **SPI Data Modes**

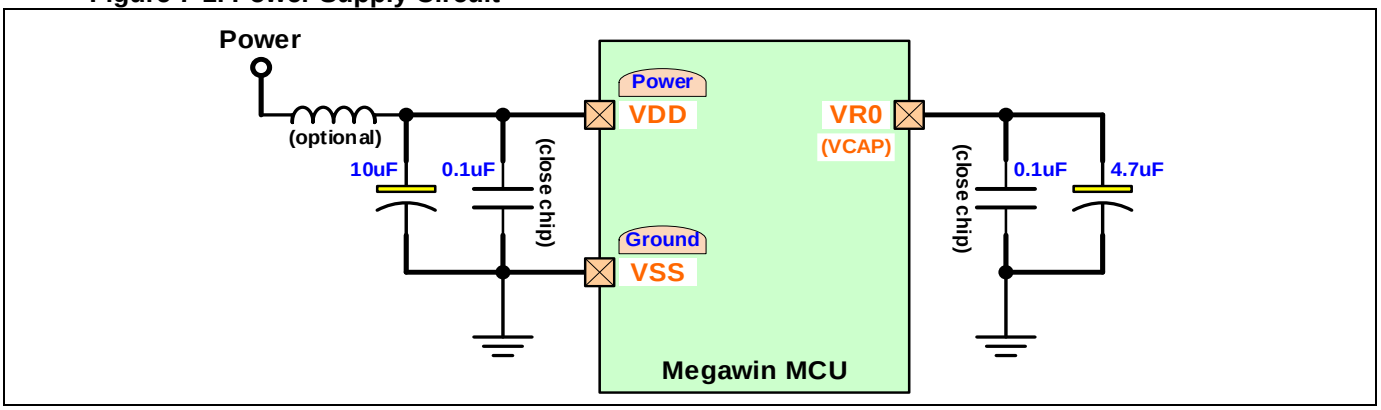
  The SPI module provides several data modes and can be configured to one of the modes of standard SPI, 1-Line SPI, 2-Line SPI, 4-Line SPI for flexible SPI application.

7. Application Notes

7.1. Power Supply Circuit

To have the chip work with power supply varying from 1.8V to 5.5V, adding some external decoupling and bypass capacitors is necessary on **VDD/VSS** power pins, as shown in following figure. The **VR0** pin is the embedded LDO voltage output as internal core logic power supply. It needs to place one 0.1uF capacitor and one 4.7uF capacitor to be closed the pin.

Figure 7-1. Power Supply Circuit



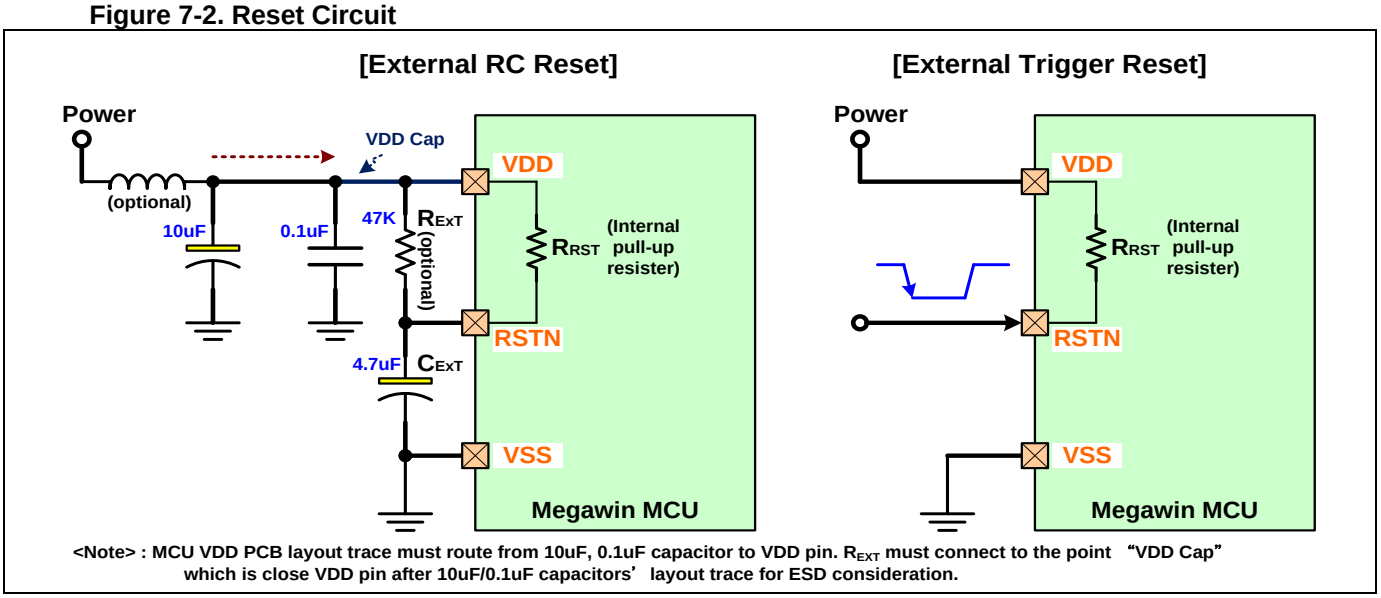
7.2. Reset Circuit

Normally, the power-on reset can be successfully generated during power-up. However, to further ensure the MCU a reliable reset during power-up, the external reset is necessary. The following figure shows the external reset circuit, which consists of a capacitor ***C_{EXT}*** connected to **VSS** (ground) and a resistor ***R_{EXT}*** connected to **VDD** (power supply).

In general, ***R_{EXT}*** is optional because the **RSTN** pin has an internal pull-high resistor (***R_{RST}***). This internal diffused resistor to **VDD** permits a power-up reset using only an external capacitor ***C_{EXT}*** to **VSS**.

Strongly suggestion, the **RSTN** pin must set to output mode if it is used to do as both chip reset and GPIO functions in application. In this condition, the pin input low may make chip reset locked error if it set to GPIO input mode.

Figure 7-2. Reset Circuit

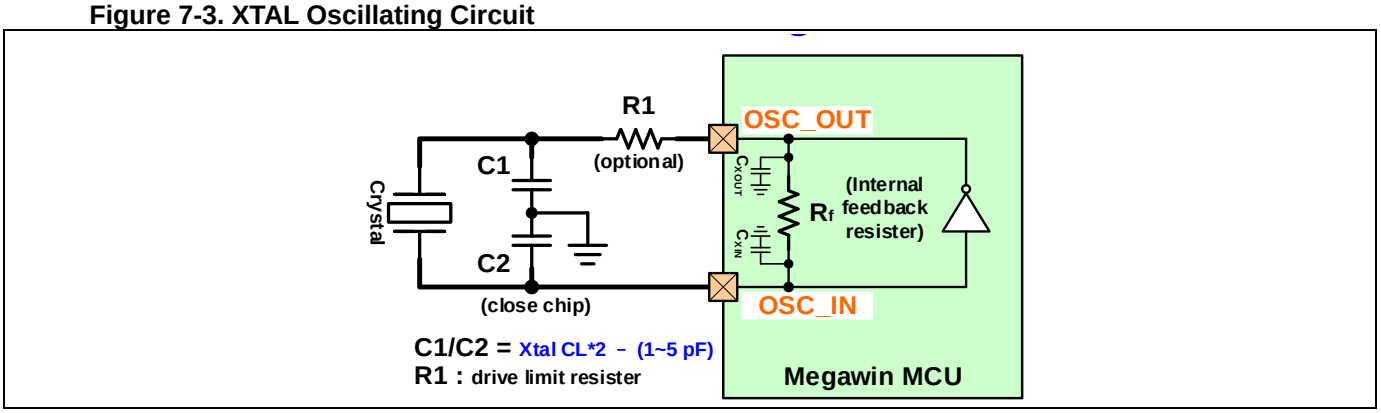


<Note> : MCU VDD PCB layout trace must route from 10uF, 0.1uF capacitor to VDD pin. R_{EXT} must connect to the point "VDD Cap" which is close VDD pin after 10uF/0.1uF capacitors' layout trace for ESD consideration.

7.3. Xtal Oscillating Circuit

To achieve successful and exact oscillating (up to 25MHz), the capacitors ***C1*** and ***C2*** are necessary, as shown in following figure. Normally, ***C1*** and ***C2*** have the same value. Refer the capacitor load (**CL**) value in Xtal manufacture specification for the final matching capacitor of ***C1*** & ***C2***.

Figure 7-3. XTAL Oscillating Circuit



❖ **Xtal Capacitor Selection**

C_{XIN} / C_{XOUT}: Chip internal total equivalent capacitance of internal oscillator circuit, bounding pad, bounding wire, lead frame.

Table 7-1. Internal Total Equivalent Capacitance for XOSC circuit

Component	Capacitance Value
C_{XOUT}	1.3pF (0.8~1.8pF)
C_{XIN}	2.0pF (1.8~2.2pF)

The XTAL Load Capacitance CL = C11 // C22 + Cp

$C11 = C1 + C_{XOUT}$

$C22 = C2 + C_{XIN}$

Cp: the distribution/stray capacitance that is generated by PCB layout path

= 1.18 pF/in for 2-layer FR4 PCB (Trace width=12mil, PCB height= 1.6mm)

= 3.16 pF/in for 4-layer FR4 PCB (Trace width=10mil, Subtract height=6mil)

The following table lists the suggested ***C1*** & ***C2*** value for the different capacitor load (**CL**) crystal application.

Table 7-2. Reference Capacitance of C1 & C2 for crystal oscillating circuit

Crystal C Load	C1, C2 Capacitance
12.5pF	19pF (16~22pF)
20pF	34pF (31~37pF)
32pF	58pF (55~61pF)

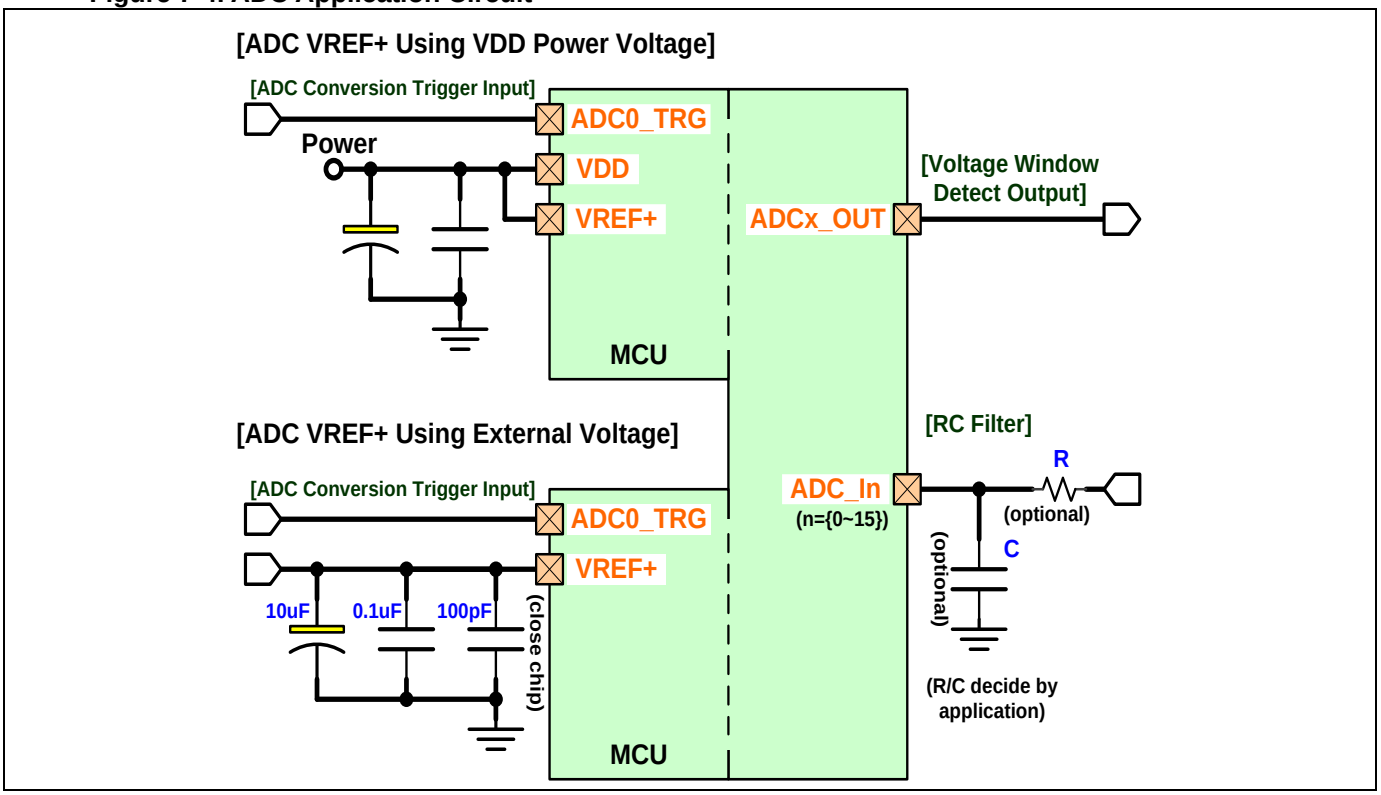
7.4. ADC Application Circuit

The ADC reference voltage source can be from (1) VDD power by connecting **+VREF** pin to **VDD** pin directly (2) external quiet reference voltage source.

When uses the VDD power as the ADC reference voltage, it must connect **+VREF** pin trace to the point which is at current flow behind the power capacitor(s). When uses the external reference voltage source as the ADC reference voltage, it must add some decoupling and bypass capacitors, as shown in following figure.

An optional **ADCx_TRG** pin is able to input the trigger signal for ADC input conversion and an optional **ADCx_OUT** pin is used to output the internal ADC window detection status.

Figure 7-4. ADC Application Circuit



8. Electrical Characteristics

8.1. Parameter Glossary

Table 8-1. Parameter Glossary

Symbol	Definition	Descriptions
Abbreviations for electrical characteristics		
Min	Minimum value	Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value.
Max	Maximum value	Unless otherwise specified, the value is guaranteed in worst conditions of ambient temperature, supply voltage by referring sample testing mean value.
Typ	Typical value	Unless otherwise specified, the value is based on TA=25 °C, VDD=5V.
VDD	Power supply voltage	The voltage range is specified in characteristics table or conditions column.
VSS	Power reference voltage	Unless otherwise specified, all voltages are referred to VSS.
TA	Ambient temperature	The temperature range is specified in characteristics table or conditions column.
T_{PC}	Peripheral clock cycle time	The peripheral input clock source may select APB, SYS or other clock. This clock frequency needs lower than 1/2 of the module process clock frequency.

8.2. Absolute Maximum Rating

Table 8-2. Absolute Maximum Rating

Parameter	Rating	Unit
Ambient temperature under bias	-40 ~ +125	**°C**
Storage temperature	-65 ~ + 150	**°C**
Voltage on any Port I/O Pin or RST with respect to VSS	-0.5 ~ VDD + 0.5	**Volt**
Voltage on VDD with respect to VSS	-0.5 ~ +6.0	**Volt**
Maximum total current through VDD and VSS	200	**mA**
Maximum output current sunk by any I/O pin	40	**mA**

Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

8.3. DC Characteristics

Table 8-3. DC Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25 °C and execute NOP for each CPU cycle (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Input/Output Characteristics						
V_{IH}	Input High voltage	Except RSTN,XIN/XOUT pins	**0.6**			**VDD**
V_{IH_XOSC}	Input High voltage (XIN)	XIN pin GPIO mode	**0.75**			**VDD**
V_{IH_RST}	Input High voltage (RSTN)	RSTN pin reset/GPIO mode	**0.75**			**VDD**
V_{IL}	Input Low voltage	Except RSTN,XIN/XOUT pins			**0.15**	**VDD**
V_{IL_XOSC}	Input Low voltage (XIN)	XIN pin GPIO mode			**0.2**	**VDD**
V_{IL_RST}	Input Low voltage (RSTN)	RSTN pin reset/GPIO mode			**0.2**	**VDD**
I_{IH}	Input High Leakage current	V_{PIN} = VDD		**0**	**0.1**	**uA**

I_{IL1}	Logic 0 input current (quasi-bidirectional mode or input mode with on-chip pull-up resistor)			0	0.001	uA
I_{IL2}	Logic 0 input current (input mode or open-drain mode)			0	0.001	uA
I_{H2L}	Logic 1 to 0 input transition current (quasi-bidirectional or input mode with on-chip pull-up resistor)	V_{PIN} = 1.8V		320	500	uA
I_{OH1}	Output High current (push-pull output mode & full level)	V_{PIN} = 2.4V		32.1		mA
I_{OH2}	Output High current (push-pull output mode & 1/2 level)	V_{PIN} = 2.4V		16.5		mA
I_{OH3}	Output High current (push-pull output mode & 1/4 level)	V_{PIN} = 2.4V		8.5		mA
I_{OH4}	Output High current (push-pull output mode & 1/8 level)	V_{PIN} = 2.4V		4.4		mA
I_{OL1}	Output Low current(full level)	V_{PIN} = 0.4V		23.7		mA
I_{OL2}	Output Low current(1/2 level)	V_{PIN} = 0.4V		12.3		mA
I_{OL3}	Output Low current(1/4 level)	V_{PIN} = 0.4V		6.3		mA
I_{OL4}	Output Low current(1/8 level)	V_{PIN} = 0.4V		3.2		mA
R_{PU}	IO pin pull-high resistance	Except RSTN		12.5		Kohm
R_{RST}	Internal reset pull-high resistance			250		Kohm
TR1	IO rising time(Normal mode and IO output drive strength is full level)	Except RSTN,XIN/XOUT pins C load=30pF		11.7		ns
TR2	IO rising time(Normal mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		34.6		ns
TR3	IO rising time(High speed mode and IO output drive strength is full level)	Except RSTN,XIN/XOUT pins C load=30pF		7.1		ns
TR4	IO rising time(High speed mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		33.3		ns
TR5	IO rising time(XOUT)	C load=30pF		9.5		ns
TR6	IO rising time(XIN)	C load=30pF		7.4		ns
TR7	IO rising time(RSTIN)	C load=30pF		11.1		ns
TF1	IO falling time(Normal mode and IO output drive strength is full level)	Except RSTN,XIN/XOUT pins C load=30pF		10.6		ns
TF2	IO falling time(Normal mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		15.7		ns
TF3	IO falling time(High speed mode and IO output drive strength is full level)	Except RSTN,XIN/XOUT pins C load=30pF		4.1		ns
TF4	IO falling time(High speed mode and IO output drive strength is 1/4 level)	Except RSTN,XIN/XOUT pins C load=30pF		11.6		ns
TF5	IO falling time(XOUT)	C load=30pF		12.7		ns
TF6	IO falling time(XIN)	C load=30pF		3.1		ns
TF7	IO falling time(RSTIN)	C load=30pF		9.7		ns
	Power Consumption					
I_{OP1}	ON(normal) mode operating current	TL1 (APB=AHB=32KHz) dhrystone		0.88		mA
I_{OP2}		TL2 (APB=AHB=12MHz) dhrystone		3.7		mA
I_{OP3}		TL3 (APB=AHB=24MHz) dhrystone + IP		11.4		mA

I_{OP4}		TL4 (APB=AHB=24MHz - XTAL) dhrystone + IP		8.0		mA
I_{OP5}		TL5 (APB=AHB=24MHz - EXTCK) dhrystone + IP		8.0		mA
I_{OP6}		TL6 (APB=AHB=48MHz) dhrystone + all IP		15.4		mA
I_{SLP0}	SLEEP mode operating current (IWDT Enable)	SL0 (ILRCO on: IWDT Disable, APB=AHB=32KHz)		46.6		uA
I_{SLP1}		SL1 (IHRCO on: APB=6MHz,AHB=3MHz)		842		uA
I_{SLP2}		SL2 (IHRCO on: APB=AHB=12MHz)		1156		uA
I_{SLP3}		SL3 (XTAL=12MHz: APB/AHB=6MHz/3MHz)		1560		uA
I_{STP0}	STOP mode operating current (LVR/BOD0/BOD1 Disabled)	ST0 (ILRCO off)		5.5		uA
I_{STP1}		ST1 (IWDT Enable, ILRCO=32KHz)		7		uA
I_{STP2}		ST2 (RTC Enable, ILRCO=32KHz)		6.9		uA
Wakeup Time						
t_{WK_SLP0}	Wakeup from SLEEP mode	IHRCO/ILRCO on, wakeup by RTC event (APB Clock= IHRCO clock)		5	6	T_{PC}
t_{WK_STP0}	Wakeup from STOP mode	ILRCO on, wakeup by RTC event	20			us
BOD Characteristics						
V_{LVR}	LVR detection level (VR0)	TA = -40℃ to +125℃	1.45	1.57	1.65	Volt
V_{BOD0}	BOD0 detection level (VR0)	TA = -40℃ to +125℃	1.6	1.65	1.7	Volt
$I_{BOD0+LVR}$	BOD0 and LVR Power Consumption	TA = 25℃			5	
V_{BOD10}	BOD1 detection level for 2.0V	TA = -40℃ to +125℃	1.8(*1)	2.0	2.2(*1)	Volt
V_{BOD11}	BOD1 detection level for 2.4V	TA = -40℃ to +125℃	2.22(*1)	2.4	2.62(*1)	Volt
V_{BOD12}	BOD1 detection level for 3.7V	TA = -40℃ to +125℃	3.50(*1)	3.7	3.90(*1)	Volt
V_{BOD13}	BOD1 detection level for 4.2V	TA = -40℃ to +125℃	3.89(*1)	4.2	4.59(*1)	Volt
I_{BOD1}	BOD1 Power Consumption	TA = 25℃	4.5		8.3	uA
Operating Condition						
V_{PSR}	Power-on Slope Rate	TA = -40℃ to +125℃	0.05			V/ms
V_{OP1}	CPU Operating Speed 0–48MHz	TA = -40℃ to +125℃	2.7		5.5	Volt
V_{OP2}	CPU Operating Speed 0–12MHz	TA = -40℃ to +125℃	1.8		5.5	Volt

(*1) Data based on characterization results, not tested in production.

T_{PC}: APB clock cycle time, **IP**: internal peripheral modules, **all IP**: all test modules

TL3 ~ TL6: Measure current with IO toggle

Table 8-4. Current Measurement Condition Level Definition Table

Chip Power State	ON Mode						SLEEP Mode				STOP Mode		
Test Level	TL1	TL2	TL3	TL4	TL5	TL6	SL0	SL1	SL2	SL3	ST0	ST1	ST2
Symbol	I_{OP1}	I_{OP2}	I_{OP3}	I_{OP4}	I_{OP5}	I_{OP6}	I_{SLP0}	I_{SLP1}	I_{SLP2}	I_{SLP3}	I_{stp0}	I_{stp1}	I_{stp2}
CPU State	Normal						Sleep				Deep Sleep		
CPU Code (*1)	dhrystone	dhrystone	dhrystone+ normal code			dhrystone+ heavy code	-	-	-	-	-	-	-
APB Clock	32KHz ILRCO	12MHz IHRCO	24MHz PLL/4	24MHz PLL/4	24MHz PLL/4	48MHz PLL/2	32KHz ILRCO	6MHz IHRCO/2	12MHz IHRCO	6MHz XTAL/2	-	32KHz ILRCO	32KHz ILRCO
AHB/CPU Clock	32KHz APB	12MHz APB	24MHz APB	24MHz APB	24MHz APB	48MHz APB	32KHz APB	3MHz APB/2	12MHz APB	3MHz APB/2	-	32KHz APB	32KHz APB
ILRCO (32KHz)	V	V	V	V	V	V	V	V	V	V		V	V
IHRCO (12MHz)		V	V			V		V	V				

XTAL (12MHz)				Medium						Medium			
EXTCK (12MHz)					V								
PLL			V	V	V	V							
LDO (*2)	**Normal**						**Normal**			**Low Power**			
LVR	V	V	V	V	V	V	V	V	V	V			
BOD0	V	V	V	V	V	V	V	V	V	V			
BOD1			V	V	V	V							
ADC0			CK_APB	CK_APB	CK_APB	CK_APB							
CMP			CK_APB	CK_APB	CK_APB	CK_APB		CK_APB	CK_APB	CK_APB			
RTC			CK_UT	CK_UT	CK_UT	CK_UT							CK_UT
IWDT	CK_ILRCO	CK_ILRCO	CK_ILRCO	CK_ILRCO	CK_ILRCO	CK_ILRCO		CK_ILRCO	CK_ILRCO	CK_ILRCO		CK_ILRCO	
WWDT			CK_APB	CK_APB	CK_APB	CK_APB							
TM00	CK_APB	CK_APB	CK_APB	CK_APB	CK_APB	CK_APB		CK_APB	CK_APB	CK_APB			
TM01						CK_APB							
TM10			CK_APB	CK_APB	CK_APB	CK_APB							
TM16						CK_APB							
TM36			CK_APB	CK_APB	CK_APB	CK_APB							
I2C0			CK_APB	CK_APB	CK_APB	CK_APB							
URT0			CK_APB	CK_APB	CK_APB	CK_APB							
URT1						CK_APB							
SPI0						CK_APB							
IO Pins	all Push-Pull Low		IO Toggle				all Push-Pull Low				all Push-Pull Low		

Note: (*1) **[CPU Code]**
dhrystone: CPU runs "Dhrystone" benchmarks code.
normal code: Set CK_APB and CK_AHB frequency by table. The module clock divider can be /4, /8 or others.
heavy code: 1. Set CK_APB and CK_AHB frequency by table. The module clock set the highest frequency (module clock DIV=/2).
2. Let the module operates as busy as possible and fills full data through the buffer. (EX: transfer 4 bytes for one transaction)

(*2) Normal: PW_LDO_ON=0, Low Power: PW_LDO_STP=1

(*3) Normal: PW_WKSLP_MDS=0, Low Power: PW_WKSLP_MDS=1

8.4. External Clock Characteristics

Table 8-5. External Clock Characteristics

VDD=1.8V ~ 5.5V, VSS=0V, TA = -40°C ~ +125°C (unless otherwise specified)

Symbol	Parameter	Conditions	Crystal		External Clock		Unit
			Min	Max	Min	Max	
f_{XOSC}	Oscillator Frequency	VDD = 1.8V ~ 5.5V	4	25	0	36	MHz
t_{XOSC}	Clock Period		40		27.7		ns
t_{H_XOSC}	High Time		0.4T	0.6T	0.4T	0.6T	t_{XOSC}
t_{L_XOSC}	Low Time		0.4T	0.6T	0.4T	0.6T	t_{XOSC}
t_{r_XOSC}	Rise Time			20		7	ns
t_{f_XOSC}	Fall Time			20		7	ns

8.5. PLL Characteristics

Table 8-6. PLL Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25°C (unless otherwise specified)

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Voltage		1.8	5.0	5.5	Volt
Input Clock Frequency Range	TA = -40℃ to +125℃	5 (*1)		7 (*1)	MHz
PLL Locking Time	TA = -40℃ to +125℃		4 (*2)		us
PLL Power Consumption			0.45		mA

Period Jitter (Peak-to-Peak)			500	1000	pS

(*1) Data guaranteed by design, not tested in production.

(*2) Data based on characterization results, not tested in production.

8.6. IHRCO Characteristics

Table 8-7. IHRCO Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25°C (unless otherwise specified)

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Voltage		1.8	5.0	5.5	Volt
IHRCO0 Frequency			12		MHz
IHRCO1 Frequency			11.0592		MHz
IHRCO0 Frequency Deviation	TA = +25℃	-1.0		+1.0	%
(factory calibrated)	TA = -40℃ to +125℃	-2.0(*1)		+2.0(*1)	%
IHRCO1 Frequency Deviation	TA = +25℃	-1.0		+1.0	%
(factory calibrated)	TA = -40℃ to +125℃	-2.0(*1)		+2.0(*1)	%
IHRCO Start-up Time				6(*1)	us
IHRCO Power Consumption			0.35		mA

(*1) Data based on characterization results, not tested in production.

8.7. ILRCO Characteristics

Table 8-8. ILRCO Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25°C (unless otherwise specified)

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Voltage		1.8	5.0	5.5	Volt
ILRCO Frequency			32		KHz
ILRCO Frequency Deviation	TA = +25℃, VDD=5.0V	-8		+8	%
(factory calibrated)	TA = -40℃ to +125℃	-15(*1)		+15(*1)	%
ILRCO Power Consumption				5	uA

(1) Data based on characterization results, not tested in production.

8.8. LDO Characteristics

Table 8-9. LDO Characteristics

VDD=5.0V±10%, VSS=0V, TA = -40℃~ +125 °C

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
VDD	Supply Voltage	Normal Mode	2.6	—	5.5	V
General						
VR0	LDO Output Voltage (VR0 pin)	ON(Normal) mode		1.83		Volt
		Low power mode (VDD=2.6V~5.5V)		1.75		Volt
IQ	Current	VDD=2.6V~5.5V, TA = 25℃		50		uA
		VDD=2.6V~5.5V, TA = -40℃~ +125℃		50(*1)		uA
VDROP	Dropout Voltage (VDD-VDD18)	IOUT=50mA, VDD=2.6V~5.5V		700		mV
IOUT	Max output current	VDD=5.0V	50			mA

		VDD=3.6V	50			mA
		VDD=2.6V	40			mA

(1) Data based on characterization results, not tested in production.

8.9. Flash Characteristics

Table 8-10. Flash Characteristics

VDD=5.0V±10%, VSS=0V, TA = -40℃~ +125 ℃

Parameter	Conditions	Limits			Unit
		Min	Typ	Max	
Supply Voltage		2.0		5.5	Volt
Flash Write (Erase/Program) Voltage		2.2		5.5	Volt
Flash Erase/Program Cycle		10000			Times
Flash Data Retention	TA = +25℃	100			Year

8.10. ADC Characteristics

Table 8-11. ADC Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C, C_{LOAD}=10pF, Gain=x1 (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
VDDA	Analog Supply Voltage		2.7	5.0	5.5	Volt
I_{ADC_ON}	Operation Current - normal			2.2		mA
I_{ADC_OFF}	Operation Current - power-down			0.1		uA
ADC Static Parameters						
Bits	Resolution				12	bits
INL	Integral nonlinearity (INL)	VREF = 5V, VDD = 5V, 800Ksps Conversion Rate (sampling clock = 24 MHz)		±3		LSB
DNL	Differential nonlinearity (DNL)	VREF = 5V, VDD = 5V, 800Ksps Conversion Rate (sampling clock = 24 MHz)		1.5		LSB
E_{OFFSET}	Offset error	VREF = 5V, VDD = 5V, 800Ksps Conversion Rate (sampling clock = 24 MHz)		-15		LSB
E_{FS}	Full scale error	VREF = 5V, VDD = 5V,800Ksps Conversion Rate(sampling clock = 24 MHz)		-15		LSB
	ADC Input and DC Characters					
V_{AIN}	ADC input voltage range (Single Ended)	gain = 1.0	0		Vref	Volt
C_{LOAD}	Input Capacitance				8	pF
V_{XREF}	External ADC reference voltage		2.7		VDDA	Volt
V_{BUF}	Internal VBUF reference voltage	-40 °C < < 125 °C	1.38	1.4	1.42	Volt
	Internal VBUF reference voltage spread over the temperature range	-40 °C < < 125 °C V_{BUF} =1.402V at 25°C			15	mV
ADC Conversion Parameters						
Fs	Sampling clock				24	MHz
	Conversion rate	VDDA = 5.5 ~ 4.0 V			800	Ksps

		VDDA = 4.0 ~ 2.7 V			640	Ksps
	Conversion time in conversion clock (not including acquisition time)			30		clocks
	ADC Other Characters and Definitions					
TADEN	ADC enable time		5			uS

(*1) The UG_{BW} will be divided by the GAIN setting. (ex: Ideal UGF will be 1MHz/4 when PGA gain=4)

8.11. ADC PGA Characteristics

Table 8-12. ADC PGA Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
VDDA	Analog Supply Voltage		2.7	5.0	5.5	Volt
	DC Characteristics					
V_{CM_IN}	Input Common-mode Voltage	VDDA>3.0V,Gain=x1,as a unit gain buffer	0.03		VDDA/2+0.5	V
		VDDA<3.0V,Gain=x1,as a unit gain buffer	0.03		VDDA/2	V
IQ	Ground Current	VDDA=5.0V, VIN= VDDA/2; VOUT=VDDA/2, Gain=x1 (RFB=120KΩ current Not included when Gain=x1)		1050		uA
AC Characteristics						
SR	Slew rate (*1)	Normal Operation		3.5		V/us
UGF	PGA Bandwidth Frequency (*2)	Normal Operation		10		MHz

(*1) Data guaranteed by design, not tested in production.

(*2) The UGF will be divided by the GAIN setting. (ex: Ideal UGF will be 10MHz/4 when PGA gain=4)

8.12. Analog Comparator Characteristics

Table 8-13. Analog Comparator Characteristics

VDDA=VDD=5.0V±10%, VSS=0V, TA = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Supply Range						
VDDA	Analog Supply Voltage		2.0	5.0	5.5	Volt
I_{COMP0}	Operation Current - CMP0	High response time without IVREF (*1)		10		uA
		High response time with IVREF (*1)		210		uA
		Low response time		1.2		uA
I_{COMP1}	Operation Current - CMP1	High response time without IVREF (*1)		10		uA
		High response time with IVREF (*1)		210		uA
		Low response time		1.2		uA
	Analog Comparator Core					
V_{OS}	Input Offset Voltage			20		mV
V_{CM}	Input Common Mode Voltage		50		VDD-50	mV
	Comparator hysteresis	Disable Hysteresis		0		mV
	Input voltage range 50mV~VDD-50mV	High response time		10		mV
		Low response time		10		mV
T_{RT}	Response time	High response time - Falling		230		ns

		High response time - Rising		200		ns
		Low response time - Falling		1.2		us
		Low response time – Rising		1		us
t_{PWON}	Power on Time (from power-down)	High response time	0.5		1.5	us
		Low response time		16.2		us
RU	Unit Resistance			309		ohm

(*1) IVREF : Internal voltage reference circuit

8.13. UART Characteristics

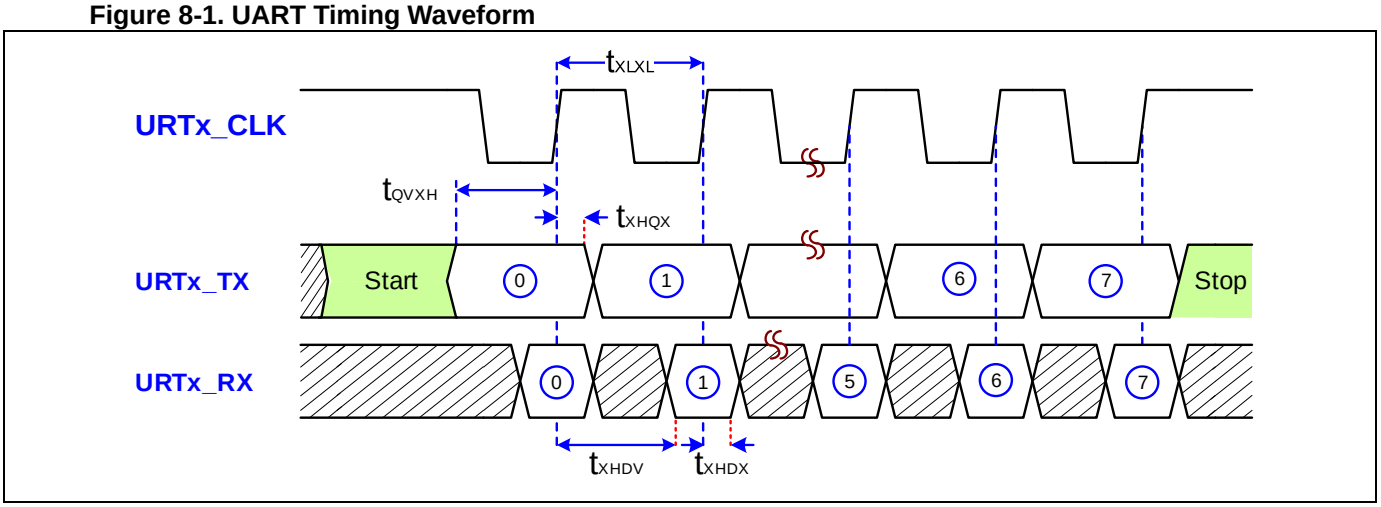
Table 8-14. UART Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
UART Mode						
f_{CK}	Serial Port Clock Frequency				6	MHz
t_{XLXL}	Serial Port Clock Cycle Time		4			T_{PC}
t_{QVXH}	Output Data Setup to Clock Rising Edge		T_{PC} -20			ns
t_{XHQX}	Output Data Hold after Clock Rising Edge		T_{PC} -10			ns
t_{XHDX}	Input Data Hold after Clock Rising Edge		0			ns
t_{XHDV}	Clock Rising Edge to Input Data Valid				T_{PC} -20	ns
SPI Master Mode (Synchronous Mode)						
f_{MCK}	SPI Output Clock Frequency	VDD=3.3V ~ 5.5V			16	MHz
		VDD=1.8V ~ 3.3V			12	MHz
t_{MCKH}	SPI Clock High Time		3			T_{PC}
t_{MCKL}	SPI Clock Low Time		3			T_{PC}

T_{PC} : APB clock or SYS clock cycle time

Figure 8-1. UART Timing Waveform



8.14. SPI Characteristics

Table 8-15. SPI Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Master Mode						
f_{MCK}	SPI Clock Frequency	VDD=3.3V ~ 5.5V			24	MHz
		VDD=1.8V ~ 3.3V			16	MHz
t_{MCKH}	SPI Clock High Time		2			T_{PC}
t_{MCKL}	SPI Clock Low Time		2			T_{PC}
t_{MIS}	D_{IN} Valid to SPI Clock Shift Edge		$2T_{PC}+20$			ns
t_{MIH}	SPI Clock Shift Edge to D_{IN} Change		0			ns
t_{MOH}	SPI Clock Shift Edge to D_{OUT} Change				10	ns
Slave Mode						
f_{SCK}	SPI Clock Frequency	VDD=3.3V ~ 5.5V			16	MHz
		VDD=1.8V ~ 3.3V			12	MHz
t_{SE}	NSS Falling to First SPI Clock Edge		2			T_{PC}
t_{SD}	Last SPI Clock Edge to NSS Rising		2			T_{PC}
t_{SEZ}	NSS Falling to D_{OUT} Valid				4	T_{PC}
t_{SDZ}	NSS Rising to D_{OUT} High-Z				4	T_{PC}
t_{CKH}	SPI Clock High Time		3			T_{PC}
t_{CKL}	SPI Clock Low Time		3			T_{PC}
t_{SIS}	D_{IN} Valid to SPI Clock Sample Edge		2			T_{PC}
t_{SIH}	SPI Clock Sample Edge to D_{IN} Change		2			T_{PC}
t_{SOH}	SPI Clock Shift Edge to D_{OUT} Change				4	T_{PC}
t_{SLH}	Last SPI Clock Edge to D_{OUT} Change (CPHA = 1 only)		1		2	T_{PC}

T_{PC} : APB clock or SYS clock cycle time

D_{IN} : SPI input data signal

D_{OUT} : SPI output data signal

Figure 8-2. SPI Master Timing Waveform

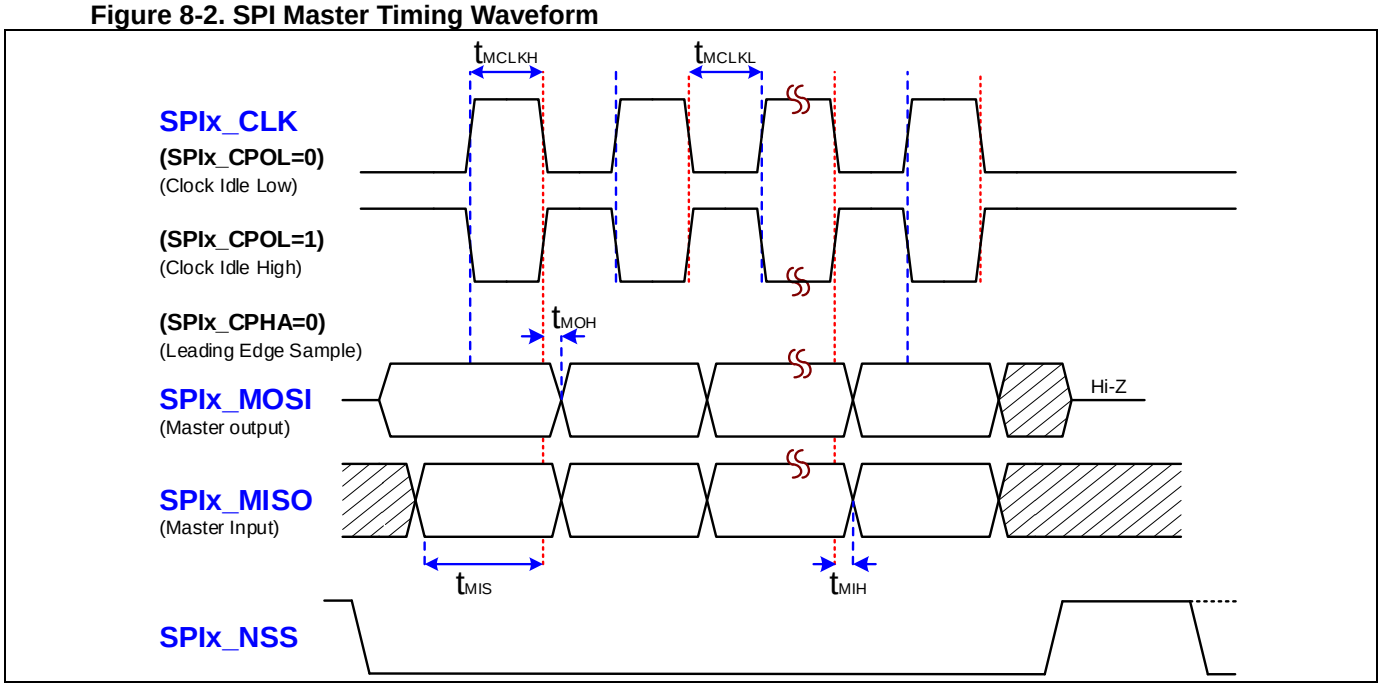
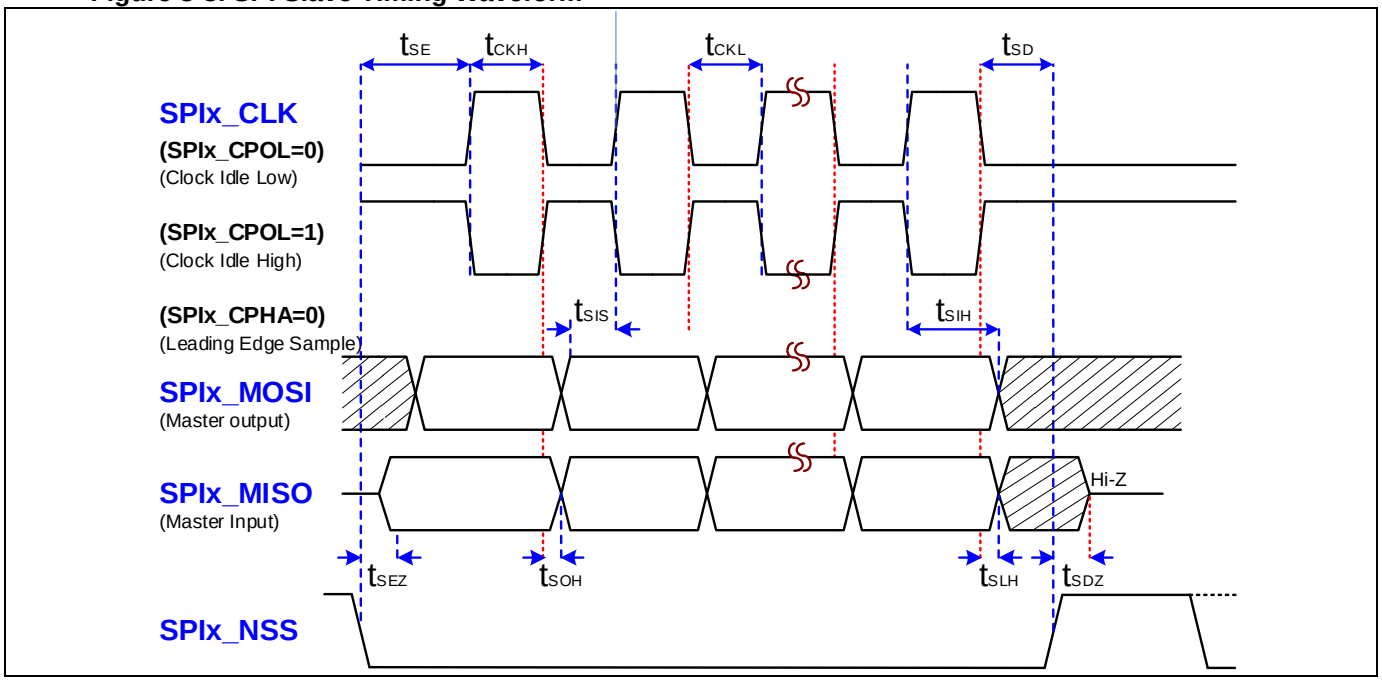


Figure 8-3. SPI Slave Timing Waveform



8.15. I2C Characteristics

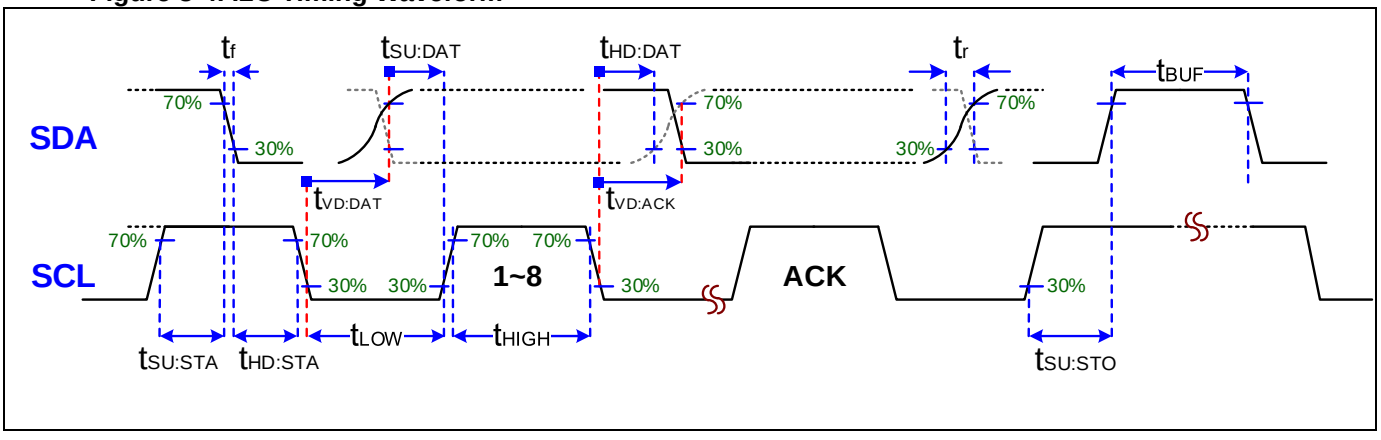
Table 8-16. I2C Characteristics

VDD=5.0V±10%, VSS=0V, TA = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100	0	400	0	1000	KHz
t_{Low}	Low period of the SCL clock		4.7		1.3		0.5		us
t_{Low_M}	Low period of the SCL clock (Master Mode)		2		2		2		T_{PC}
t_{Low_S}	Low period of the SCL clock (Slave Mode)		4		4		4		T_{PC}
t_{High}	High period of the SCL clock		4.0		0.6		0.26		us
t_{High_M}	High period of the SCL clock (Master Mode)		3		3		3		T_{PC}
t_{High_S}	High period of the SCL clock (Slave Mode)		5		5		5		T_{PC}
$t_{HD;STA}$	Hold time for START condition		4.0		0.6		0.26		us
$t_{SU;STA}$	Setup time for START condition		4.7		0.6		0.26		us
$t_{HD;DAT}$	Data hold time		0		0		0		us
$t_{SU;DAT}$	Data setup time		250		100		50		ns
$t_{SU;STO}$	Setup time for STOP condition		4.0		0.6		0.26		us
t_{BUF}	Bus free time between a STOP and START		4.7		1.3		0.5		us
$t_{VD;DAT}$	Data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	Data valid acknowledge time			3.45		0.9		0.45	us
t_r	Rise time of both SDA and SCL signals			1000		300		120	ns
t_f	Fall time of both SDA and SCL signals			300	20x (VDD/5.5V)	300	20x (VDD/5.5V)	120	ns
C_i	Capacitive load for each IO pin			10		10		10	pF

T_{PC} : APB clock or SYS clock cycle time

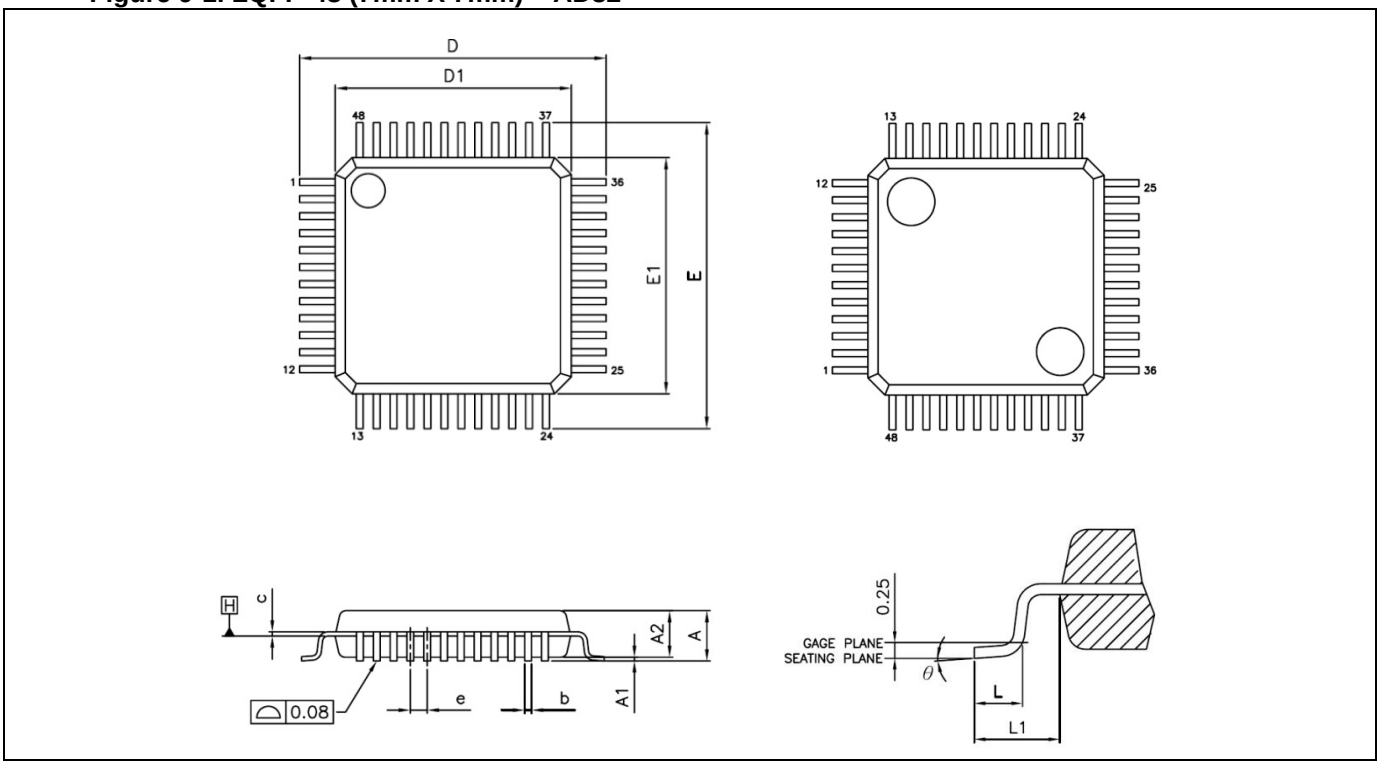
Figure 8-4. I2C Timing Waveform



9. Package Dimension

9.1. LQFP-48

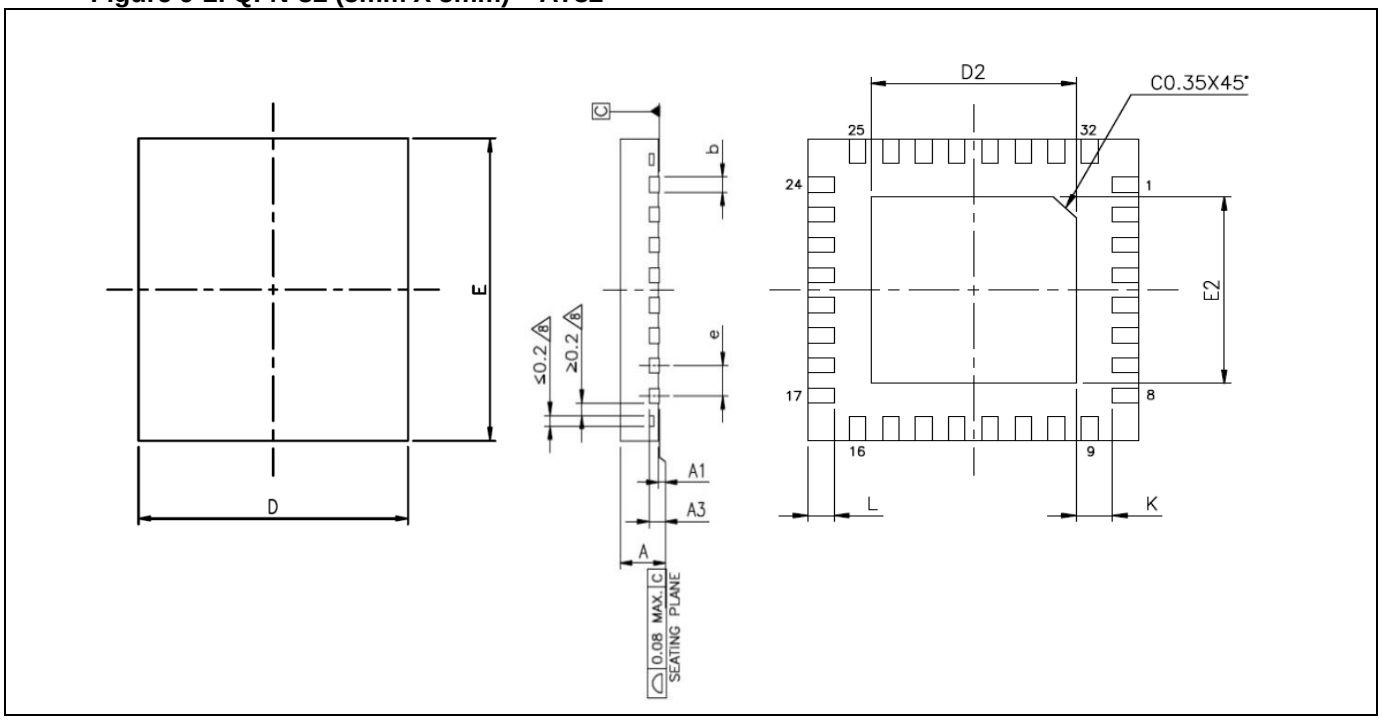
Figure 9-1. LQFP-48 (7mm X 7mm) ~ AD32



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	1.60	---	---	0.062
A1	0.05	---	0.15	0.001	---	0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.006	0.008	0.010
c	0.09	---	0.20	0.003	---	0.007
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.275 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.275 BSC		
e	0.50 BSC			0.019 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
ɵ	0˚	3.5˚	7˚	0˚	3.5˚	7˚

9.2. QFN-32

Figure 9-2. QFN-32 (5mm X 5mm) ~ AY32

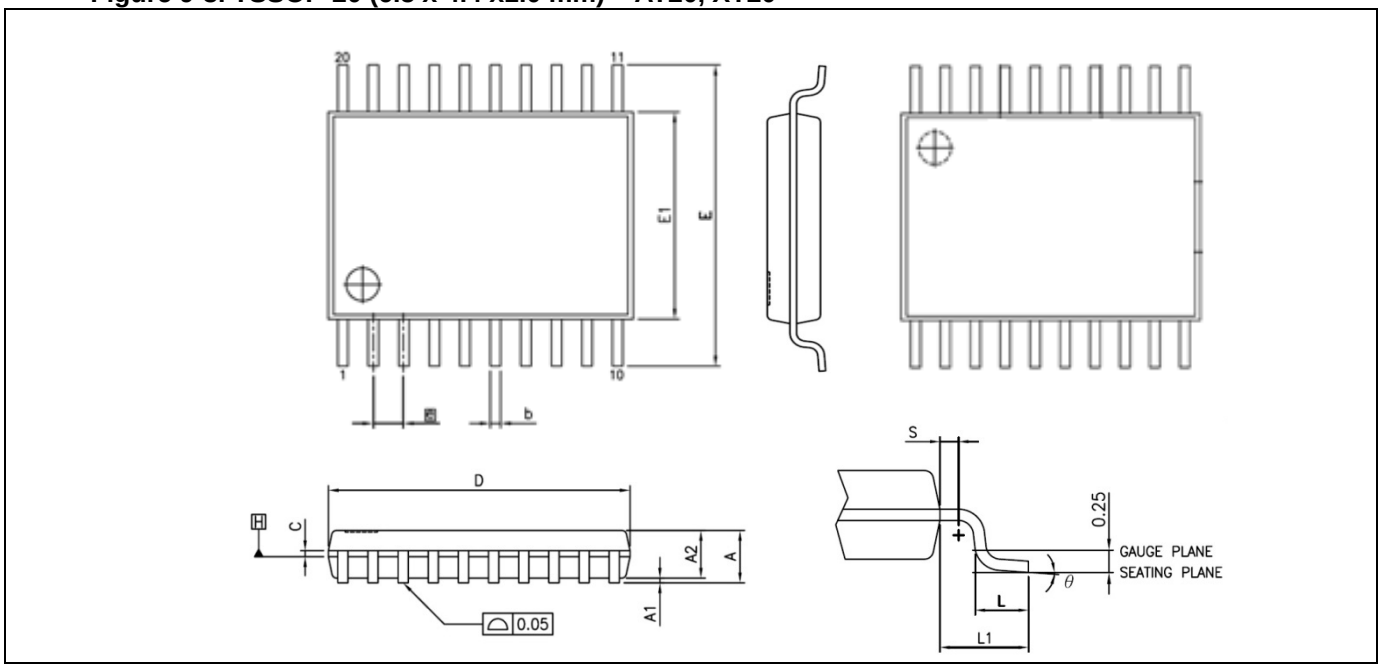


Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	0.02	0.05	0.000	0.000	0.001
A3	0.203 REF.			0.007 REF.		
b	0.18	0.25	0.30	0.007	0.009	0.011
D	5.00 BSC			0.196 BSC		
E	5.00 BSC			0.196 BSC		
e	0.50 BSC			0.019 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
K	0.20	----	----	0.007	----	----

PAD SIZE	E2			D2			LEAD FINISH		JEDEC CODE
	Min.	Nom.	Max.	Min.	Nom.	Max.	Pure Tin	PPF	
114x114MIL	2.60	2.70	2.75	2.60	2.70	2.75	X	V	W(V)HHD-2
134x134MIL	3.10	3.20	3.25	3.10	3.20	3.25	V	V	W(V)HHD-2
153x153MIL	3.15	3.25	3.30	3.15	3.25	3.30	V	V	W(V)HHD-5

9.3. TSSOP-20

Figure 9-3. TSSOP-20 (6.5 x 4.4 x1.0 mm) ~ AT20, XT20



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	----	----	1.20	----	----	0.047
A1	0.05	----	0.15	0.001	----	0.005
A2	0.80	0.90	1.05	0.031	0.035	0.041
b	0.19	----	0.30	0.007	----	0.011
C	0.09	-----	0.20	0.003	-----	0.007
D	6.40	6.50	6.60	0.251	0.255	0.259
E1	4.30	4.40	4.50	0.169	0.173	0.177
E	6.40 BSC			0.251 BSC		
e	0.65 BSC			0.026 BSC		
L1	1.00 REF			0.039 REF		
L	0.50	0.60	0.75	0.019	0.023	0.029
S	0.20	----	----	0.007	----	----
θ	0˚	----	8˚	0˚	----	8˚

10. Revision History

Revision V1.81 (2024_1008)		Chapter
1	Add parameters of I_{OP4}, I_{OP5}, I_{SLP3} parameters in the section of “8.3. DC Characteristics”.	8.3
Revision V1.80 (2024_0424)		**Chapter**
1	Add related data of 125°C temperature support chip in the chapters of Features and Order Information.	Features, 2
2	Change the orientation of package view in the figures of “Figure 4-1. LQFP48 Package Pinout”, “Figure 4-2. QFN32 Package Pinout” and “Figure 4-3. TSSOP20 Package Pinout”.	4.1.1 4.1.2 4.1.3
3	Add the descriptions of VR0 pin in the section of “7.1. Power Supply Circuit".	7.1
4	Update condition and parameter data of 125°C temperature in the chapter of Electrical Characteristics.	8
5	Update the table of “Table 8-6. External Clock Characteristics” about f_{XOSC} parameter.	8.5
Revision V1.70 (2022_0621)		**Chapter**
1	Change the string of “AFS=8” to “AFS=10” in the table of “Table 4-6. Pin AFS Summary Table”.	4.3
2	Add the figure of “Figure 8-1. UART Timing Waveform” and add “Symbol” column in the table of “Table 8-14. UART Characteristics” in the section of “8.13. UART Characteristics”.	8.13
3	Add the figures of “Figure 8-2. SPI Master Timing Waveform” and “Figure 8-3. SPI Slave Timing Waveform” in the section of “8.14. SPI Characteristics”. Add “Symbol” column in the table of “Table 8-15. I2C Characteristics”.	8.14
4	Add the figure of “Figure 8-4. I2C Timing Waveform” in the section of “8.15. I2C Characteristics”.	8.15
Revision V1.60 (2022_0224)		**Chapter**
1	Update the “SPI” descriptions in Features chapter.	
2	Update the **“**TR1~TR7**”** and **“**TF1~TF7**”** parameters in the table of “Table 8-3. DC Characteristics”.	8.3
3	Add the table of “Table 8 4. Current Measurement Condition Level Definition Table”.	8.3
Revision V1.52 (2021_1215)		**Chapter**
1	Update the LQFP48 and QFN32 package size of “Part Number List” in Order Information chapter.	2
2	Change “Peak-Peak Jitter” to “Period Jitter (Peak-to-Peak)” in the table of “Table 8 6. PLL Characteristics”.	8.6
3	Update the diagram of package dimension for each package in Package Dimension chapter.	9
Revision V1.51 (2021_1018)		**Chapter**
1	Correct the wrong word “Code” to “Cold” in the descriptions of the section “6.3.3. Chip Reset Levels”.	6.3.3
2	Update the description “Provide seven timers/counters” to “Provide five timers/counters” in the section “6.17.2. Features”.	6.17.2
3	Correct the wrong word “Slop” to “Slope” in the table of “Table 8-3. DC Characteristics” of the section “8.3.DC Characteristics”.	8.3
Revision V1.50 (2021_0603)		**Chapter**
1	Update the Conditions description of “Current Consumption” in the table of “Table 8-3. DC Characteristics”.	8.3
2	Add the I_{SLP0} parameter in the table of “Table 8-3. DC Characteristics”.	8.3

3	Update ‘Internal VBUF reference voltage’ parameter in the table “Table 8-10. ADC Characteristics”.	8.10
Revision V1.40 (2021_0322)		**Chapter**
1	Update the “Clock” and “Timer” descriptions in Features chapter.	
2	Remove ADC differential input function in the section of “Pin Definition”.	4.2
3	Update the descriptions of the section “7.2. Reset Circuit” in Application Notes chapter.	7.2
4	Update the diagram and tables of the section “7.3. Xtal Oscillating Circuit” in Application Notes chapter.	7.3
5	Update ‘Input High voltage’ and ‘Input Low voltage’ characteristics in the table of “Table 8-3. DC Characteristics”.	8.3
6	Add ‘Wakeup Time’ characteristics in the table of “Table 8-3. DC Characteristics”.	8.3
7	Merge the table of “8.4.External Reset Pin Characteristic” to the table of “Table 8-3. DC Characteristics”.	8.3
Revision V1.33 (2021_0108)		**Chapter**
1	Update the ‘Symbol’ of ‘BOD Characteristics’ in the table of “Table 8-3. DC Characteristics”.	8.3
2	Add the parameters of ‘Input Common-mode Voltage’ and ‘Slew rate’ in the table of “Table 8-12. ADC PGA Characteristics”.	8.12
Revision V1.32 (2020_1214)		**Chapter**
1	Update the ‘Conditions’ description of ‘PLL Peak-Peak Jitter’ parameter in the table of “Table 8-6. PLL Characteristics”.	8.6
2	Add the information of ‘Dimensions in inch’ for each package in Package Dimension chapter.	9
Revision V1.31 (2020_0928)		**Chapter**
1	Add the “Misc.” and update “Operating” descriptions in Features chapter.	
2	Update the I_{OP1} parameter in the table of “Table 8-3. DC Characteristics”.	8.3
Revision V1.30 (2020_0323)		**Chapter**
1	Add the independent pin AFS table for each package in the section of “4.1. Pin Outline”.	4.1
2	Add the sections of “Analog Function Pin Table” and “Alternate Functions Pin List”.	4.4, 4.5
3	Update the I_{OL3} parameter in the table of “Table 8-3. DC Characteristics”.	8.3
4	Update the TR2~5 and the TF1~6 parameters in the table of “Table 8-3. DC Characteristics”.	8.3
Revision V1.21 (2019_1115)		**Chapter**
1	Correct the text “SPI (Slave)” to “SPI (Master)” on the diagram of “Figure 3 1. System Function Block”.	3.1
2	Update the ILRCO Frequency Deviation parameters in the table of “Table 8-8. ILRCO Characteristics”.	8.8
Revision V1.20 (2019_1106)		**Chapter**
1	Update the SRAM size to 4KB and the AP/IAP/ISP flash to 32KB in the table of “Table 5 1. CPU Memory Address Map”.	5.2
2	Update the ADC Offset error and Full scale error parameters in the table of “Table 8-11. ADC Characteristics”.	8.11
3	Update the analog comparator hysteresis parameters in the table of “Table 8-13. Analog Comparator Characteristics”.	8.13
Revision V1.10 (2019_0712)		**Chapter**

1	Modify ADC conversion rate from 1Msps to 800Ksps in Features chapter.	
2	Update the table of “Table 2-1. Chip Selection Table”.	2
3	Remove “Auto-Off” function in 6.12 ADC section.	6.12.3
4	Remove “Octal SPI mode with bidirectional data transfer” function for SPI module.	6.20.2
5	Add UART synchronous mode (SPI master mode) timing electrical in “Table 8-14. UART Characteristics”.	8.14
Revision V1.00 (2019_0614)		**Chapter**
1	Released version.	
2	Update the parameters’ value in Electrical Characteristics chapter.	8
Revision V0.10 (2019_0403)		**Chapter**
1	Initial version	

11. Disclaimers

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