

Megawin

8051 ISP Programmer

&

8051 ISP Writer U2

User Manual

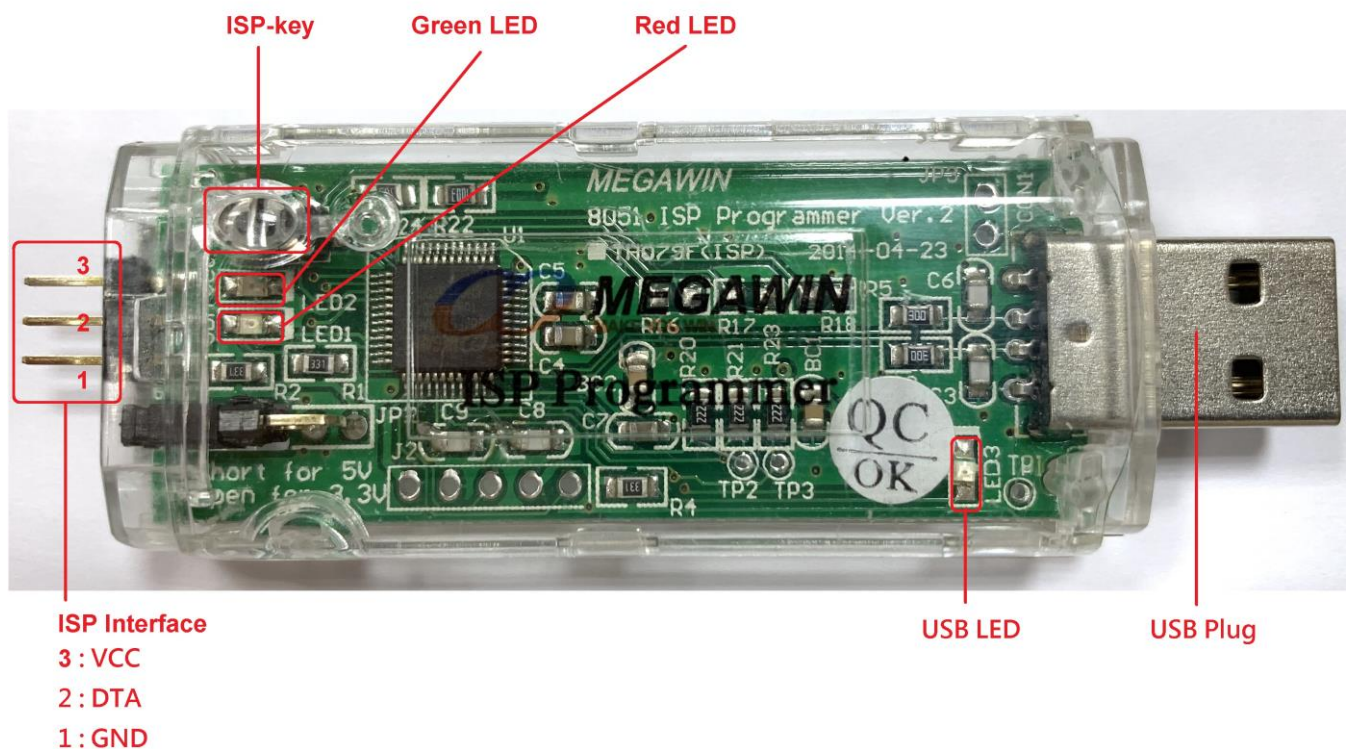
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1 Introduction

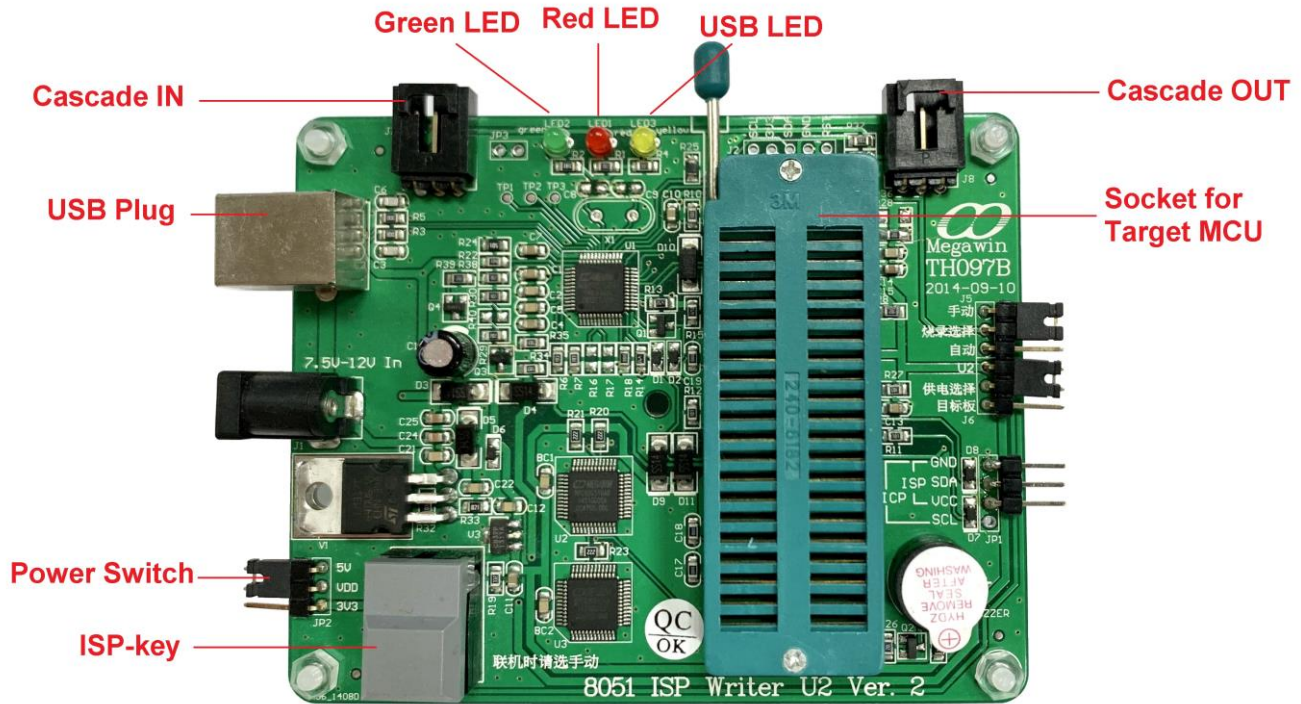
ISP is the acronym of **In-System Programming**. This programming methods make it possible that the user can update the application code under the software control without removing the mounted MCU chip from the actual end product. The tool “Megawin 8051 ISP Programmer”, see the following picture. That is it can function as an ISP Programmer. In addition, because the programming data to be programmed to the target can be saved in the programmer’s non-volatile storage, this programmer is able to work stand-alone without host (PC) intervention. This feature is especially useful in the field without a PC.

Picture of the ISP Programmer



The tool of “Megawin 8051 ISP Writer U2”, see the following picture, can be treated as an ISP Programmer with Target System. It is used for mass production (Cascade to Gang4 or Gang8 mode) to update the MCU chip application code before mount to the end product.

Picture of the ISP Writer U2



1.1 ISP Functions

When acting as an ISP Programmer, it functions as a bridge between the host and the target MCU, which has the loader program running inside. The loader program is the so-called “ISP-code” and should be pre-programmed in the ISP-memory of the target MCU. When powered on, the target boots from the ISP-memory and executes the ISP-code to check if the ISP operation is requested. If the ISP is requested, the target MCU receives the programming data from the Programmer and programs into the AP-memory by in-system programming method. After ISP processing is completed, the target will re-boot from the AP-memory to run the new application code when the Programmer is plugged out of the target; If the ISP is not requested, the target will directly re-boot from the AP-memory for normal running of the application code.

2 Chip Configuration for ISP

To use the ISP function, the user should configure the target MCU by use the “Insert ISP-code” function in “Megawin 8051 Writer” or “Megawin 8051 Writer U1”. And set the **ISP-memory** with 1K bytes (or 1.5K bytes for MPC82L(E)54) and make **HWBS** or **HWBS2** option enabled.

Note:

To let users easily use the ISP function, the Megawin 8051 products will have the following factory setting:

- (1) ISP-memory is configured with 1K (or 1.5K) bytes and “HWBS” option is enabled.*
- (2) The Megawin-provided standard ISP-code is pre-programmed.*
- (3) The “Lock” option is enabled to prevent customize code copy by others. Although, the “Lock” option has been enabled, user still can use ISP Programmer to download the code into the target chip. But after the code downloaded, it can’t be read out by any tools (for example, Megawin U1 writer, Megawin ICP Programmer).*

So, the user has no need to do the chip configuration before using the ISP function.

**** Contact Megawin for detailed product information.*

3 Install the ISP Programmer

3.1 Install the Driver

Plug the ISP Programmer into the PC's USB port, and do as follows when the monitor shows a prompt about new hardware found.

- 1) Select **No, not this time**, click **Next**.
- 2) Select **Install from a list or specific location**, click **Next**.
- 3) Select **Search for the best driver in these locations** and **Include this location in the search**, click **Browse**.
- 4) Locate the driver folder [\[PC-site Driver\]](#), click **OK**.
- 5) Click **Next**. The driver installation starts.
- 6) Click **Finish** when the installation completes.

To check if the Programmer was correctly installed, follow the listed steps:

- 1) Open the **My Computer** folder.
- 2) Open the **Control Panel** folder.
- 3) Open the **System**.
- 4) Click on the **Hardware** tab at the top of the dialog box, then click on the **Device Manager**.
- 5) Click on the plus sign in front of the **Universal Serial Bus Controllers** to check the device listing.

If the installation was completed successfully, you may find an entry, **Megawin 8051 ISP (U2) Programmer**, in the listing.

4 Use the ISP Programmer / ISP Writer U2

As the introduction in previous sections, there have two tools to support ISP download, “ISP Programmer” and “ISP Writer U2”.

When using “ISP Writer U2” to download the code for the DIP package ICs in the following list can be used without a socket board:

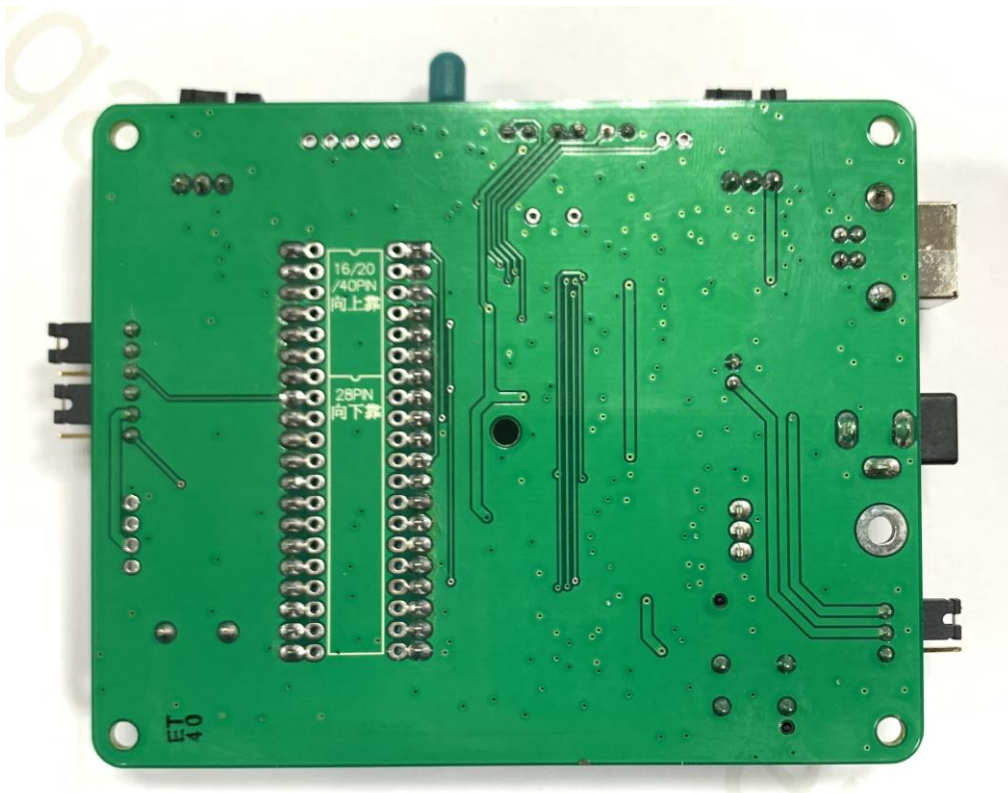
MPC89X52/53/54/58/515

MPC82X52/54

MG87FE52

MG87FX2051/4051/6051

MG86FX508



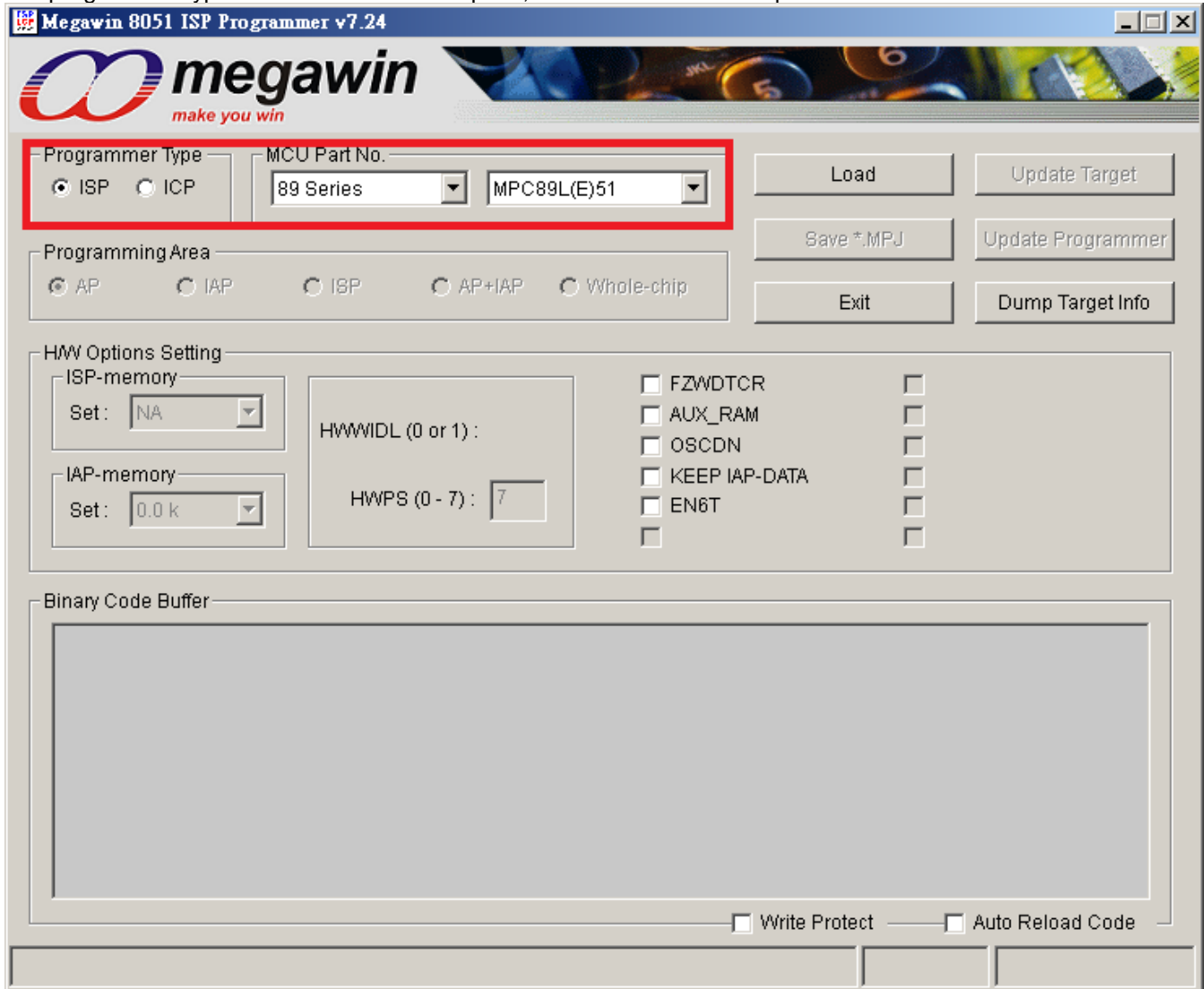
Note that the DIP16/20/40 pins should be aligned up and the DIP 28 Pins should be aligned downwards, as shown on the back of the U2 Writer.

For the latest IC serials, it is needed a transfer socket board between U2 and chip. Please contact Megawin or your agent for detail.

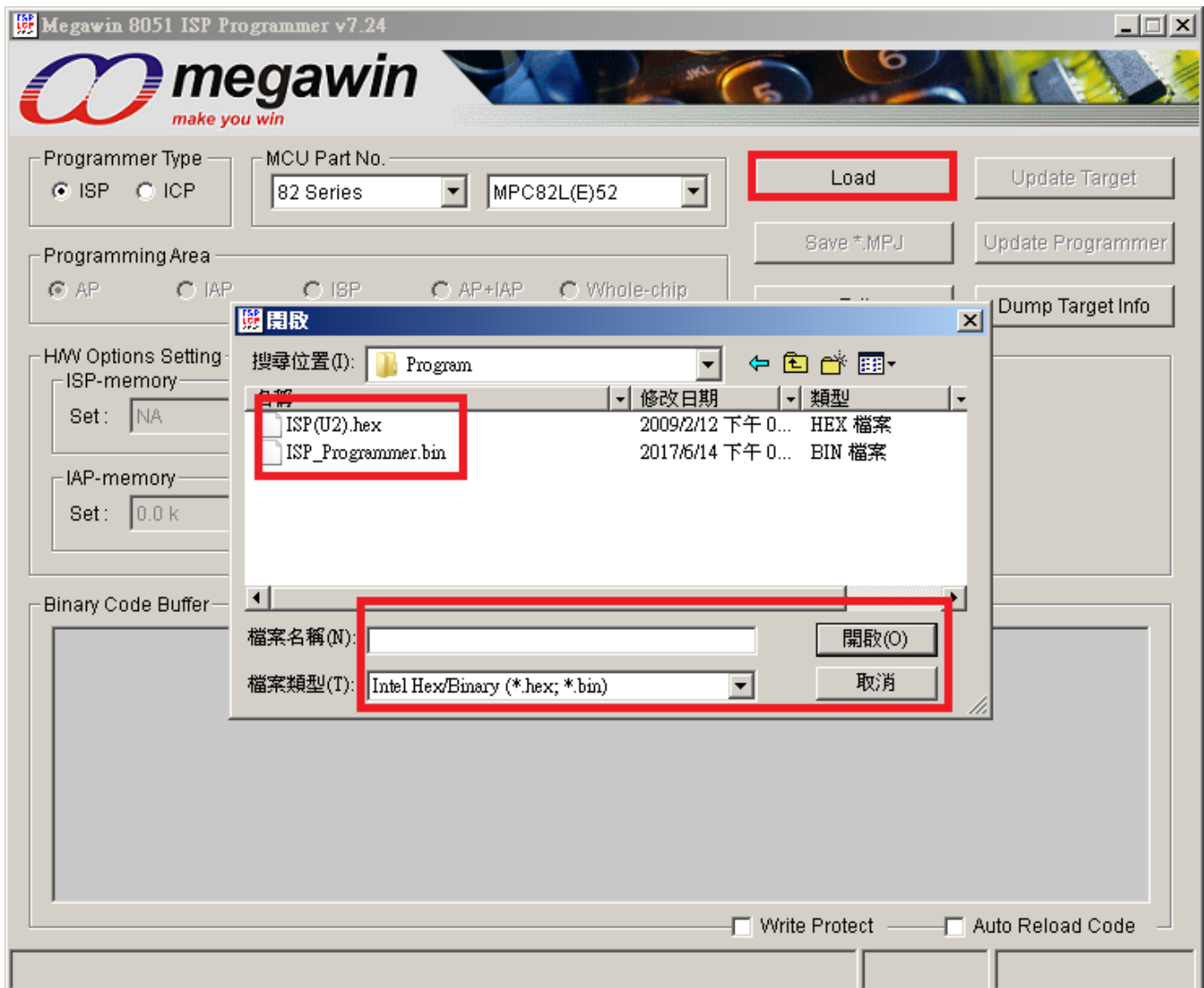
4.1 Download the target code to ISP Programmer or ISP Writer U2

4.1.1 Step 1: Choose the chip model number

The PC-site software AP (Application Program) integrates functions of the ISP Programmer. The first thing the user needs to do is to select the "Programmer Type" when the AP is opened. See the following figures for these two programmer types. After choose "ISP" option, and then select the chip model number.

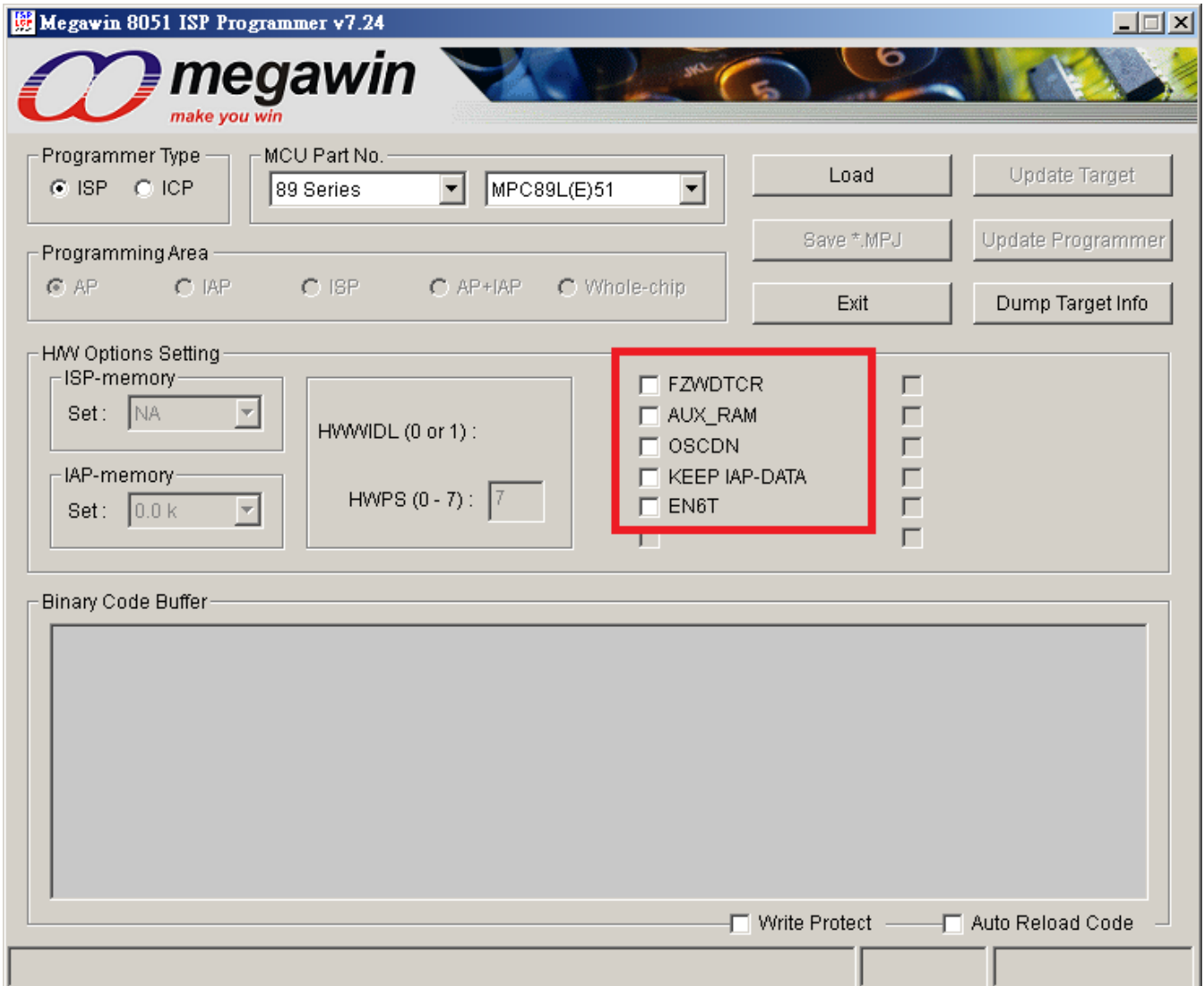


4.1.2 Step 2: Click on “Load” to select HEX or BIN



4.1.3 Step 3: Hardware Options (Only for MPC89/ few of MG82 Serials)

4.1.3.1 MPC89-series



About the H/W Option Setting

The user should always configure proper H/W Option before clicking “Update Target” or “Update Programmer”.

FZWDTCR:

[enabled]: The WDTCR register will be initialized to its reset value (0x00) *only by power-on reset.*
 (For example, if WDTCR=0x2D, it still keeps at 0x2D rather than 0x00 after RST-pin, S/W or WDT reset.)

[disabled]: The WDTCR register will be initialized to its reset value (0x00) by all reset (including power-on, RST-pin, S/W and WDT reset).

OSCDN:

[enabled]: If the XTAL frequency is less than 25MHz, this option can be enabled to reduce the internal oscillating gain for lower EMI.

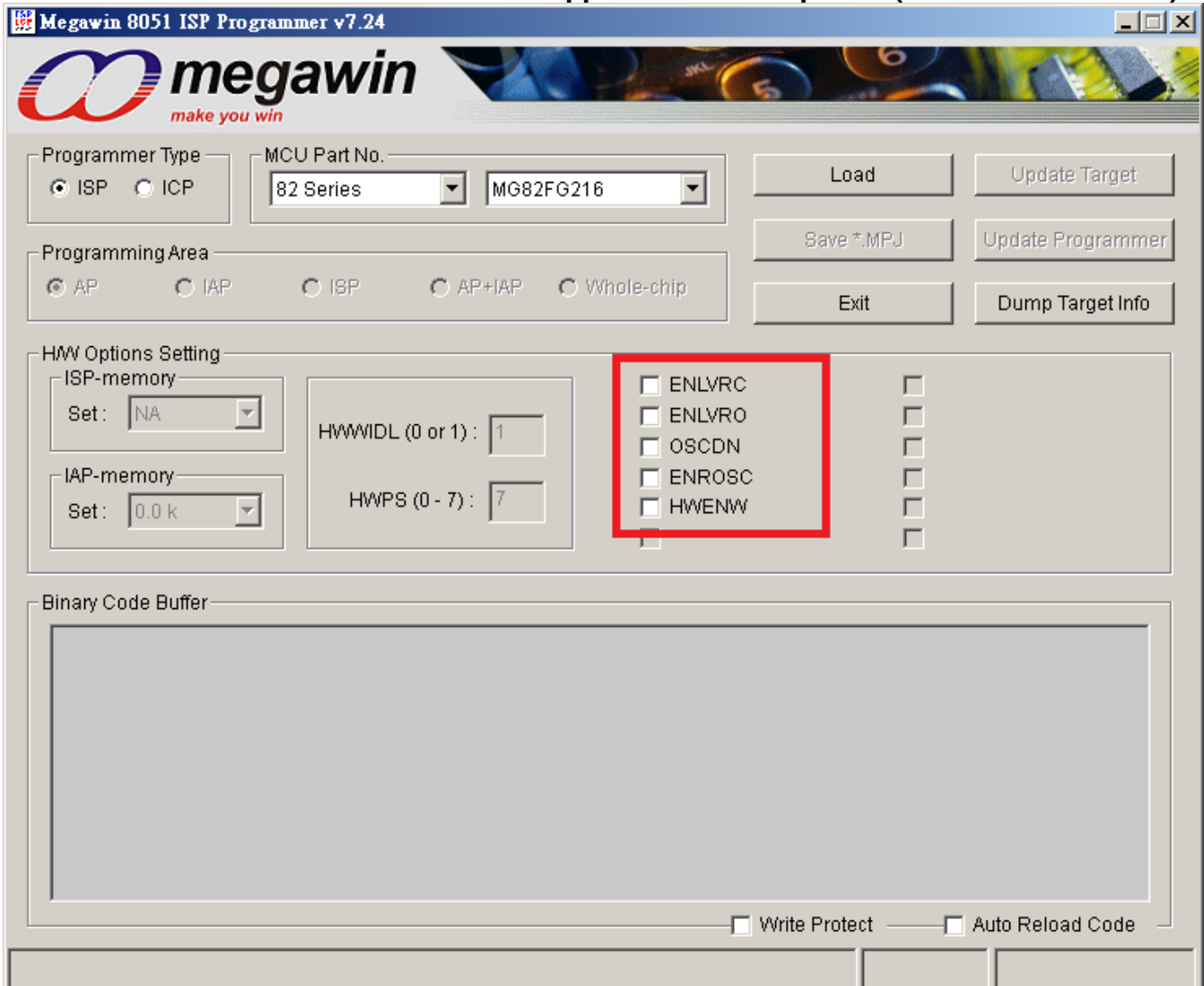
[disabled]: Normal oscillating gain.

EN6T:

[enabled]: MCU runs at 6T mode (6 clocks per machine-cycle, double speed compared to a traditional 8051)

[disabled]: MCU runs at 12T mode (12 clocks per machine-cycle, like a traditional 8051)

4.1.3.2 Partial models of MG82 series support hardware options (MG82FG2XX Series)



The screenshot shows the Megawin 8051 ISP Programmer v7.24 interface. The 'HW Options Setting' section is highlighted with a red box, containing the following options:

- ☐ ENLVRC
- ☐ ENLVRO
- ☐ OSCDN
- ☐ ENROSC
- ☐ HWENW

Other visible settings include:

- Programmer Type:** ISP (selected), ICP
- MCU Part No.:** 82 Series, MG82FG216
- Programming Area:** AP (selected), IAP, ISP, AP+IAP, Whole-chip
- ISP-memory Set:** NA
- IAP-memory Set:** 0.0 k
- HWWIDL (0 or 1):** 1
- HWPS (0 - 7):** 7
- Binary Code Buffer:** (Empty text area)
- Write Protect:** ☐ (unchecked)
- Auto Reload Code:** ☐ (unchecked)

About the H/W Option Setting

MPC82/MG84/MG87-series, the user can not update the H/W Option by ISP.

Users should set hardware options before clicking "Update Target" or "Update Programmer (For off-line mode)"

ENLVRC:

[Enable]: When the V30 pin voltage drops to 2.4V, the hardware will generate a low voltage reset.

[disabled]: Low voltage reset is disabled

ENLVRO:

[Enable]: When the VDD pin voltage drops to 3.7V, the hardware will generate a low voltage reset.

[disabled]: Low voltage reset is disabled

OSCDN:

[Enable]: If the frequency is less than 25MHz, this option can be used to reduce internal gain to reduce EMI

[disabled]: Normal gain.

ENROSC:

[Enable]: Enable internal RC oscillation

[disabled]: Disable internal RC oscillation

HWENW: (with HWWIDL, HWPS [2:0])

[Enable]: When the MCU is powered on, the watchdog is automatically enabled.
 it means the WDTCSR register is automatically set by hardware as follows:

- 1) Set the ENW
- 2) Assign the HWWIDL to the WIDL
- 3) Assign the HWPS [2:0] to the PS [2:0]

E.g.:

If HWWIDL and HWPS [2:0] are set to 1 and 5, respectively, the WDTCSR will be initially 0x2D after the MCU is powered up. As follows:

WDTCSR (Watchdog Register)

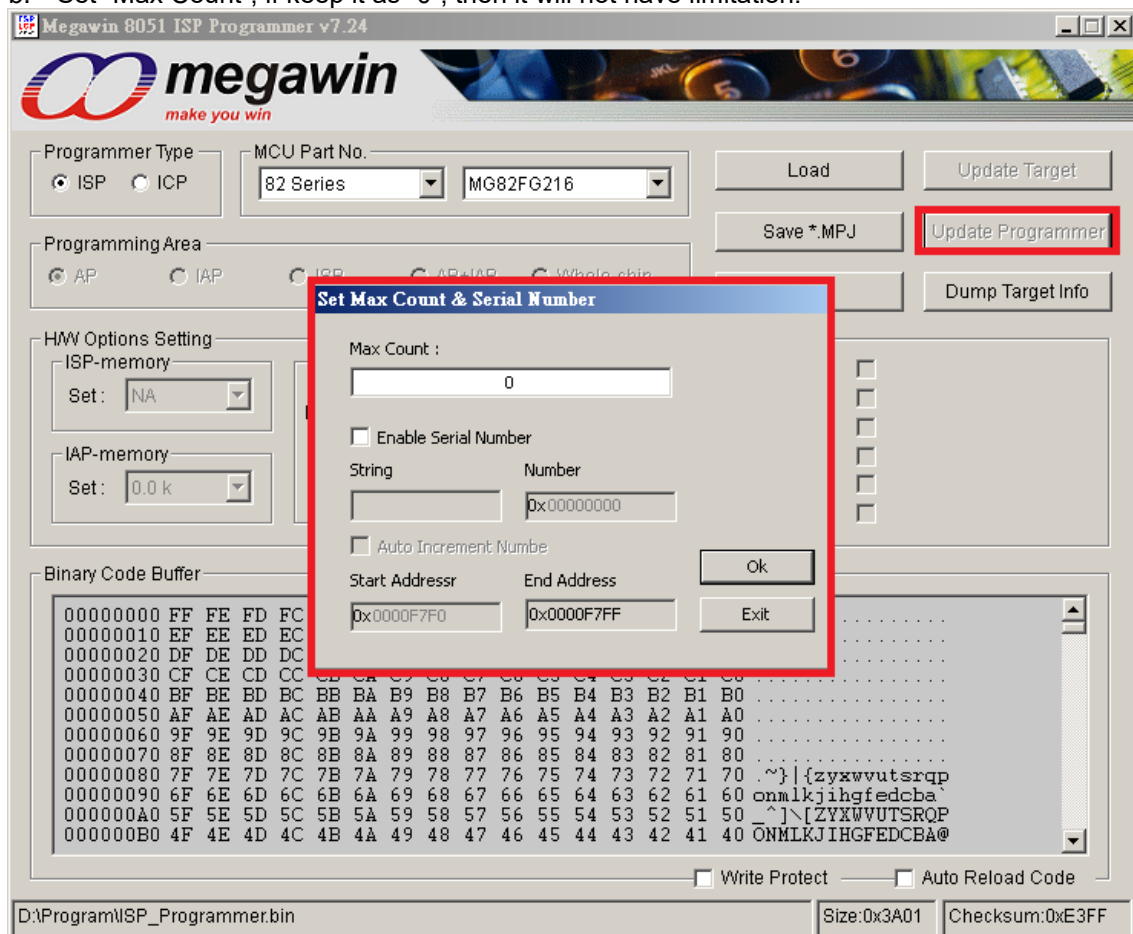
7	6	5	4	3	2	1	0
WRF	-	ENW	CLRW	WIDL	PS2	PS1	PS0
		↑ set		↑ load		↑ load	
		1		HWWIDL		HWPS[2:0]	

Prohibited: Do not access the watchdog at power-on

4.1.4 Step 4: Update Programmer/ Off Line Mode

The ISP Programmer and ISP Writer U2 support “Off Line Mode” download. Before using this function, it needs to save the code into the buffer of “ISP Programmer” or ISP Writer U2”. And it also can set the maximum download device or chip by set the number in the “Max Count”. Once the download numbers is reached, it will stop for further downloads.

- a. Press “Update Programmer”
- b. Set “Max Count”, if keep it as “0”, then it will not have limitation.



4.1.5 Dump the Contents in the Information Zone

How to dump the 256 bytes of target “Information Data”? (Please refer to [Section 5](#))

Step 1: Select “Programmer Type” as an *ISP Programmer*.

Step 2: Click “Dump Target Info”.

4-2 Operation Modes

There are three operation modes for the ISP Programmer based on its connection conditions.

4.2.1 Mode-1: Connected between host and target system

In this condition, the ISP Programmer works with the PC-site AP being executed. Three main buttons can be clicked: (1) The **“Update Programmer”** button, which is used to download the programming data (including Part No., user’s application code and H/W option) into the non-volatile storage of the Programmer. (2) The **“Update Target”** button, which further programs the new application code and H/W option into the Target MCU in addition to those the “Update Programmer” button does. (3) The **“Dump Target Info”** button, which dumps the Target Information Data described in [Section 5](#).

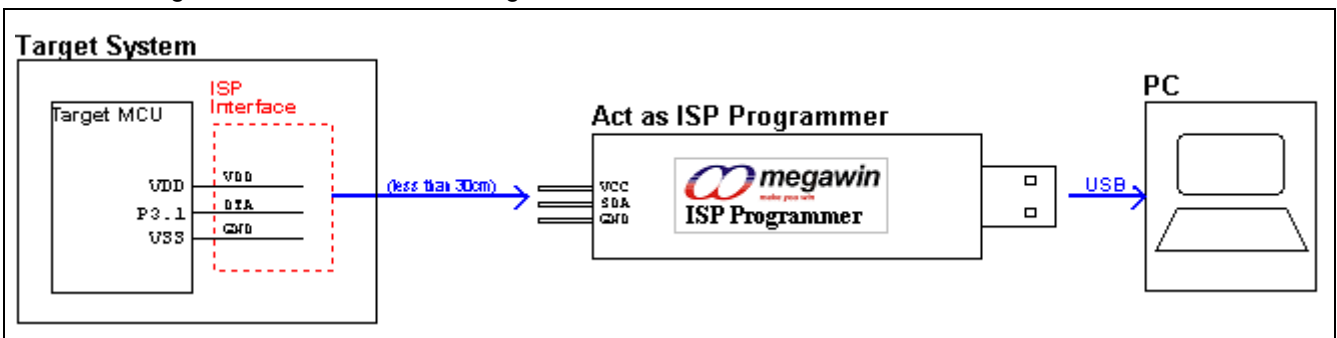
The user should select correct **“Part No.”**, then click **“Load File”** to load the new application code, and configure the H/W options (if have) before clicking the “Update Programmer” or “Update Target” button. The ISP-key can also be used to start the ISP processing after the “Update Programmer” is completed.

The following figures show the connection diagram:

When the Programmer acts as an ISP Programmer, *don’t power on the target system before connection is ready*. After connection has been done, then the user’s system can be powered on. After power up, the target MCU keeps running in the ISP-memory for ISP processing. When ISP processing is finished, it needs to disconnect this Programmer from the target system to let the target MCU run the new application code.

The LEDs show the result. If ISP processing succeeds, the green LED will be turned on, otherwise the red LED will be turned on.

When the Programmer acts as an ISP Programmer:



4.2.2 Mode-2: Connected to host only

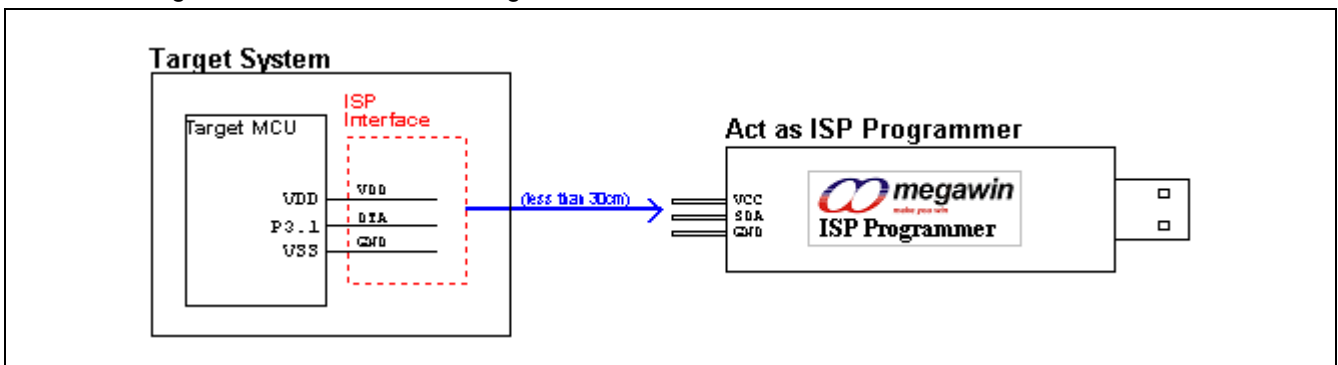
In this condition, the ISP-ICP Programmer works with the PC-site AP being executed and only the “**Update Programmer**” button can be clicked. User can download the programming data into the non-volatile storage in the Programmer for later stand-alone operation.

4.2.3 Mode-3: Connected to target system only

In this condition, the Programmer works stand-alone without the AP’s intervention.

When acting as an ISP Programmer, connect the Programmer to the target system before the system is powered up. Then, power on the system, and press the **ISP-key** to start ISP processing. The green and red LEDs show the processing result. Now, the user can disconnect the Programmer to let the system start running the new application code.

When the Programmer acts as an ISP Programmer:

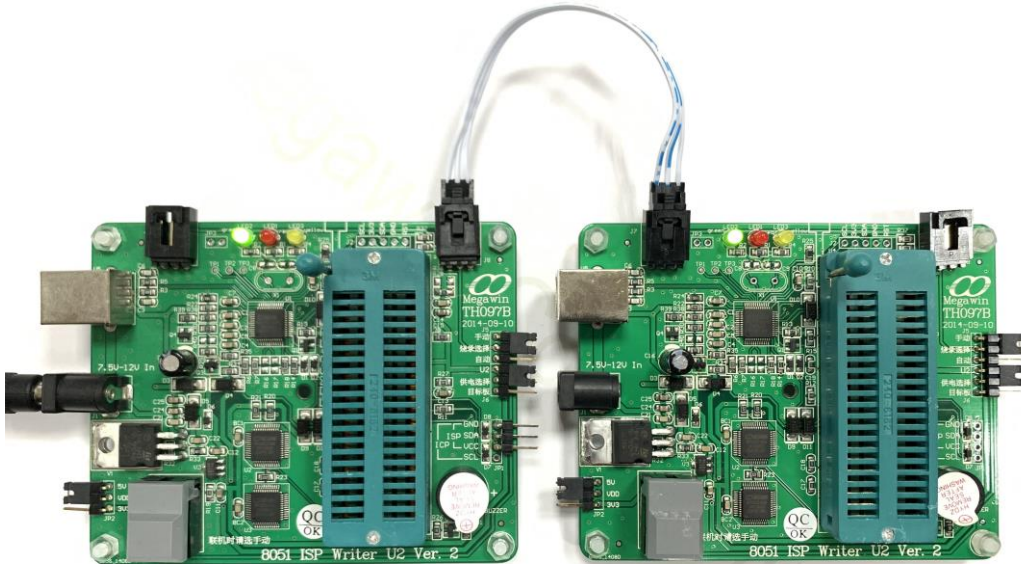


4.3 ISP Writer U2 Cascade Mode

ISP Writer U2 supports cascade mode for multi-chips can be downloaded the code at the same time. It is useful for mass production.

Step 1: To download the target code to each ISP Writer U2. Please reference “
Reference “[4.1 Download the target code to ISP Programmer or ISP Writer U2](#)”

Step 2: To use the cable cascade each ISP Writer U2 in series as showed in following.
Please note 4 of “ISP Writer U2” in series is suggested.



Step 3: Put the target IC into socket, and then press one of “ISP-Key” to download multi-chip at one time.
To check the LED indicators to know the download result.

5 Information Zone

When the H/W option *LOCK* or *SB* is enabled for code security, there is no way to read out the contents of the target by neither a universal programmer nor the ISP Programmer. For the purpose of user's product failure analysis in the future, a special Flash area called **Information Zone** is defined to be readable by only the ISP Programmer even the target is locked or scrambled. The user may put some useful product information there for future failure analysis, such as Product version, F/W version, manufacturing date code, .. and etc.

Note:

The *Information Zone* is just the name of the range where the ISP Programmer can read out data even the target is locked or scrambled.

5.1 Definition of the Information Zone

The **Information zone** is defined in the 256 bytes just prior to the ISP-memory,

An example of the **Information zone** of MPC89L(E)54/58/515:

0000f640h:	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	BF	BE	BD	BC	BB	BA	;
0000f650h:	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	AF	AE	AD	AC	AB	AA	;
0000f660h:	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	9F	9E	9D	9C	9B	9A	;
0000f670h:	99	98	97	96	95	94	93	92	91	90	8F	8E	8D	8C	8B	8A	;
0000f680h:	89	88	87	86	85	84	83	82	81	80	7F	7E	7D	7C	7B	7A	;
0000f690h:	79	78	77	76	75	74	73	72	71	70	6F	6E	6D	6C	6B	6A	;
0000f6a0h:	69	68	67	66	65	64	63	62	61	60	5F	5E	5D	5C	5B	5A	;
0000f6b0h:	59	58	57	56	55	54	53	52	51	50	4F	4E	4D	4C	4B	4A	;
0000f6c0h:	49	48	47	46	45	44	43	42	41	40	3F	3E	3D	3C	3B	3A	;
0000f6d0h:	39	38	37	36	35	34	33	32	31	30	2F	2E	2D	2C	2B	2A	;
0000f6e0h:	29	28	27	26	25	24	23	22	21	20	1F	1E	1D	1C	1B	1A	;
0000f6f0h:	19	18	17	16	15	14	13	12	11	10	0F	0E	0D	0C	0B	0A	;
0000f700h:	2D	2D	2D	2D	2D	2D	2D	2D	2D	2D	2D	2D	2D	2D	2D	2D	-----
0000f710h:	49	6E	66	6F	72	6D	61	74	69	6F	6E	3A	20	20	20	20	; Information:
0000f720h:	31	29	20	50	72	6F	64	75	63	74	20	54	79	70	65	3A	; 1) Product Type:
0000f730h:	3D	3E	20	55	52	43	5F	52	35	20	20	20	20	20	20	20	; => URC_R5
0000f740h:	32	29	20	4D	66	67	2E	20	50	6C	61	6E	74	3A	20	20	; 2) Mfg. Plant:
0000f750h:	3D	3E	20	47	75	6D	69	2F	4B	6F	72	65	61	20	20	20	; => Gumi/Korea
0000f760h:	33	29	20	4D	66	67	2E	20	44	61	74	65	3A	20	20	20	; 3) Mfg. Date:
0000f770h:	3D	3E	20	32	30	30	36	2F	30	31	2F	30	31	20	20	20	; => 2006/01/01
0000f780h:	34	29	20	46	2F	57	20	56	65	72	73	69	6F	6E	3A	20	; 4) F/W Version:
0000f790h:	3D	3E	20	31	2E	30	30	20	20	20	20	20	20	20	20	20	; => 1.00
0000f7a0h:	2E	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	; .
0000f7b0h:	2E	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	; .
0000f7c0h:	2E	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	; .
0000f7d0h:	4D	43	55	20	54	79	70	65	3A	20	20	20	20	20	20	20	; MCU Type:
0000f7e0h:	4D	65	67	61	77	69	6E	20	20	20	20	20	20	20	20	20	; Megawin
0000f7f0h:	4D	50	43	38	39	4C	35	34	2F	35	38	2F	35	31	35	20	; MPC89L54/58/515

User can use any HEX editor to edit his Information Data.

Information Data

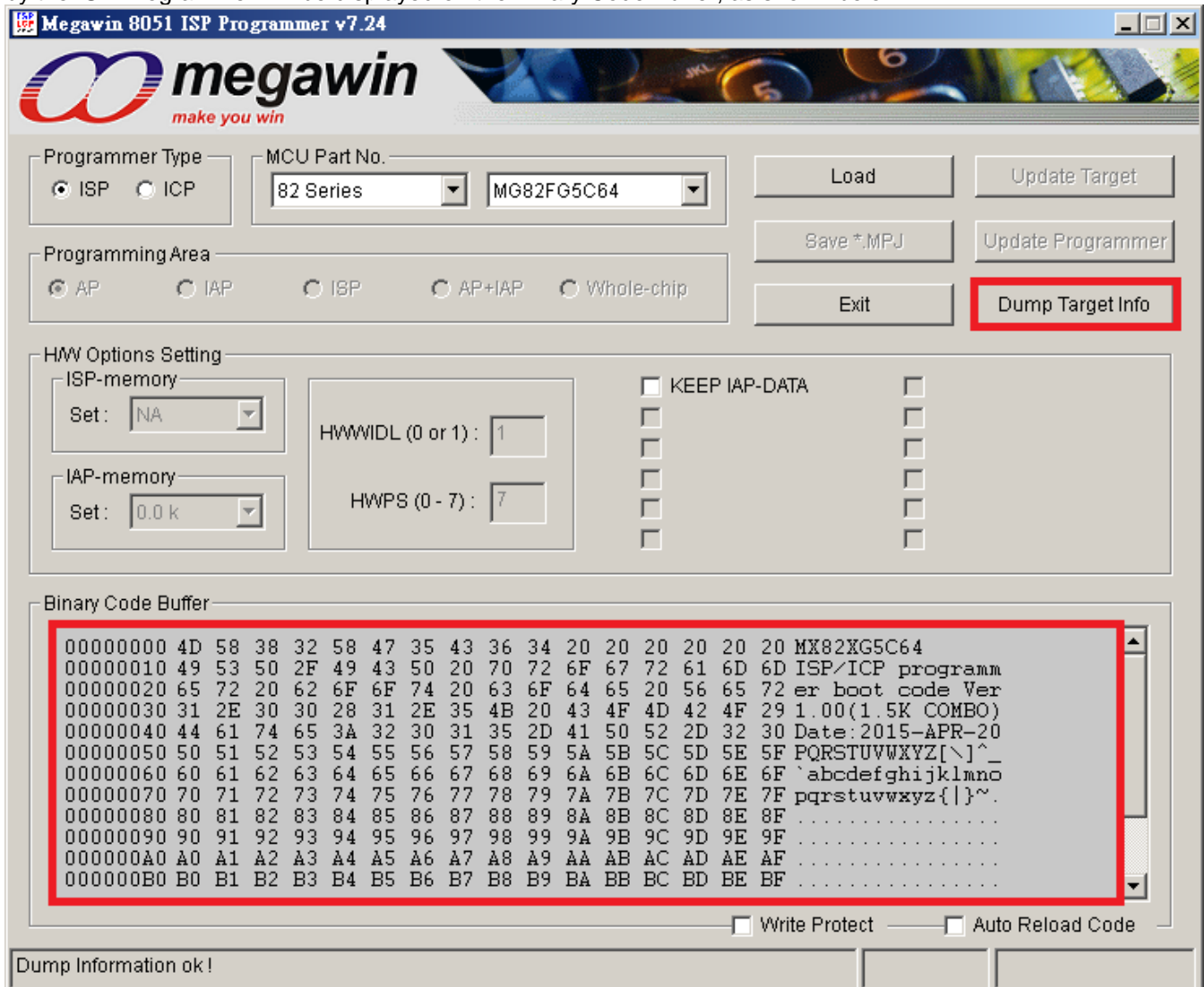
Address

ASCII type

Text type

5.2 Dump the Information Data

To view the Information Data in the Information Zone, click **"Dump Target Info"**. Now, the Information Data read by the ISP Programmer will be displayed on the Binary Code Buffer, as shown below.



Megawin 8051 ISP Programmer v7.24

Programmer Type: ☒ ISP ☐ ICP

MCU Part No.: 82 Series **MG82FG5C64**

Programming Area: ☒ AP ☐ IAP ☐ ISP ☐ AP+IAP ☐ Whole-chip

Buttons: Load, Update Target, Save *.MPJ, Update Programmer, Exit, **Dump Target Info**

HW Options Setting:

ISP-memory: Set: NA

IAP-memory: Set: 0.0 k

HW Options: HWWIDL (0 or 1): 1, HWPS (0 - 7): 7

KEEP IAP-DATA: ☐

Binary Code Buffer:

```

00000000 4D 58 38 32 58 47 35 43 36 34 20 20 20 20 20 20 MX82XG5C64
00000010 49 53 50 2F 49 43 50 20 70 72 6F 67 72 61 6D 6D ISP/ICP programm
00000020 65 72 20 62 6F 6F 74 20 63 6F 64 65 20 56 65 72 er boot code Ver
00000030 31 2E 30 30 28 31 2E 35 4B 20 43 4F 4D 42 4F 29 1.00(1.5K COMBO)
00000040 44 61 74 65 3A 32 30 31 35 2D 41 50 52 2D 32 30 Date:2015-APR-20
00000050 50 51 52 53 54 55 56 57 58 59 5A 5B 5C 5D 5E 5F PQRSTUVWXYZ[\]^_
00000060 60 61 62 63 64 65 66 67 68 69 6A 6B 6C 6D 6E 6F `abcdefghijklmnop
00000070 70 71 72 73 74 75 76 77 78 79 7A 7B 7C 7D 7E 7F pqrstuvwxyz{|}~.
00000080 80 81 82 83 84 85 86 87 88 89 8A 8B 8C 8D 8E 8F .....
00000090 90 91 92 93 94 95 96 97 98 99 9A 9B 9C 9D 9E 9F .....
000000A0 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 AA AB AC AD AE AF .....
000000B0 B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 BA BB BC BD BE BF .....
  
```

Write Protect: ☐ **Auto Reload Code:** ☐

Dump Information ok!

6 Special Notes for ISP

For the ISP operation, the Target MCU's **P3.1** pin is used as the **DTA** pin. The best case is that P3.1 dedicates itself to the ISP operation. However, P3.1 can have its normal function while not in ISP operation as long as the user follows the rule:

When the ISP Programmer is not connected, the state on P3.1 must be logic-1 when the MCU is just powered on.

It is because when the MCU is powered on and boots from ISP-memory, the MCU will check P3.1's state to determine which action will be taken: (1) keep running the ISP code, or (2) re-boot to run user's application code. If logic-0 is read, it means ISP operation is requested by the user, and the MCU will take action (1) for further ISP processing. If logic-1 is read, the MCU will take action (2). During ISP processing, P3.1 functions for bi-directional data transfer. It may output logic-1 or logic-0, and also, the ISP Programmer may send it logic-1 or logic-0. So, the user should check if it is harmful to the device/component which is connected to P3.1.

The following figures show the restriction on typical applications of P3.1 if P3.1 also functions for DTA-pin of ISP.

Figure 1:
P3.1 is used to drive an NPN transistor.

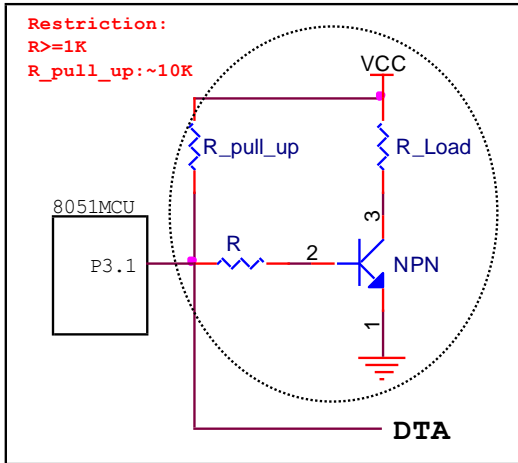


Figure 2:
P3.1 is used to drive a PNP transistor.

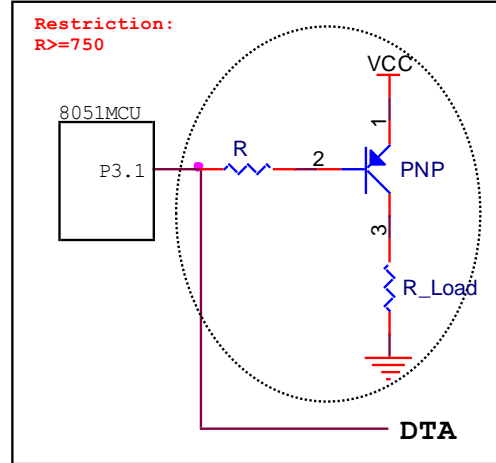


Figure 3:
P3.1 is used to drive an LED.

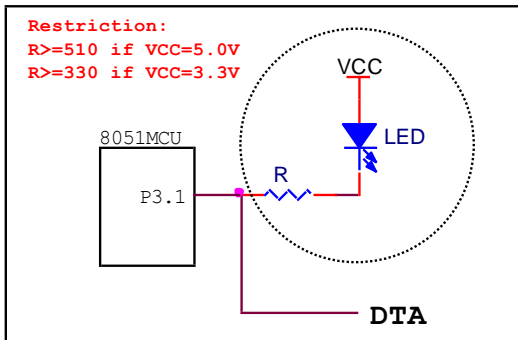


Figure 4:
P3.1 is used as its original TXD function.

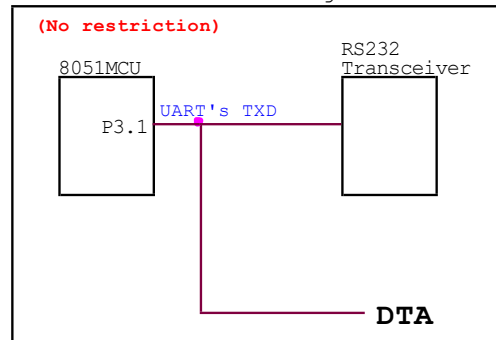


Figure 5:
P3.1 is pulled low.

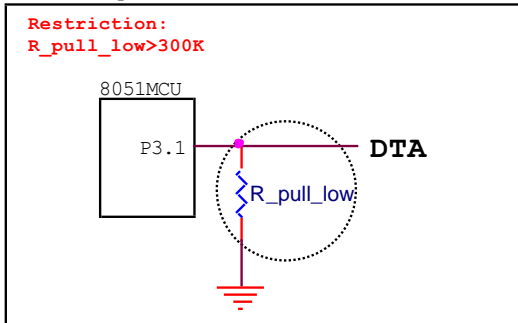
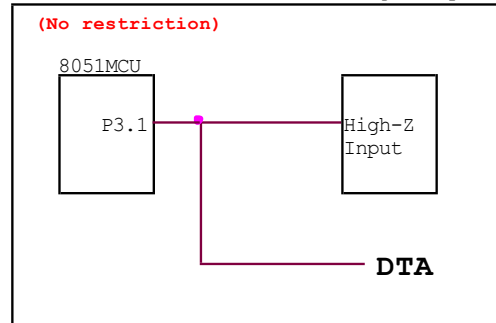
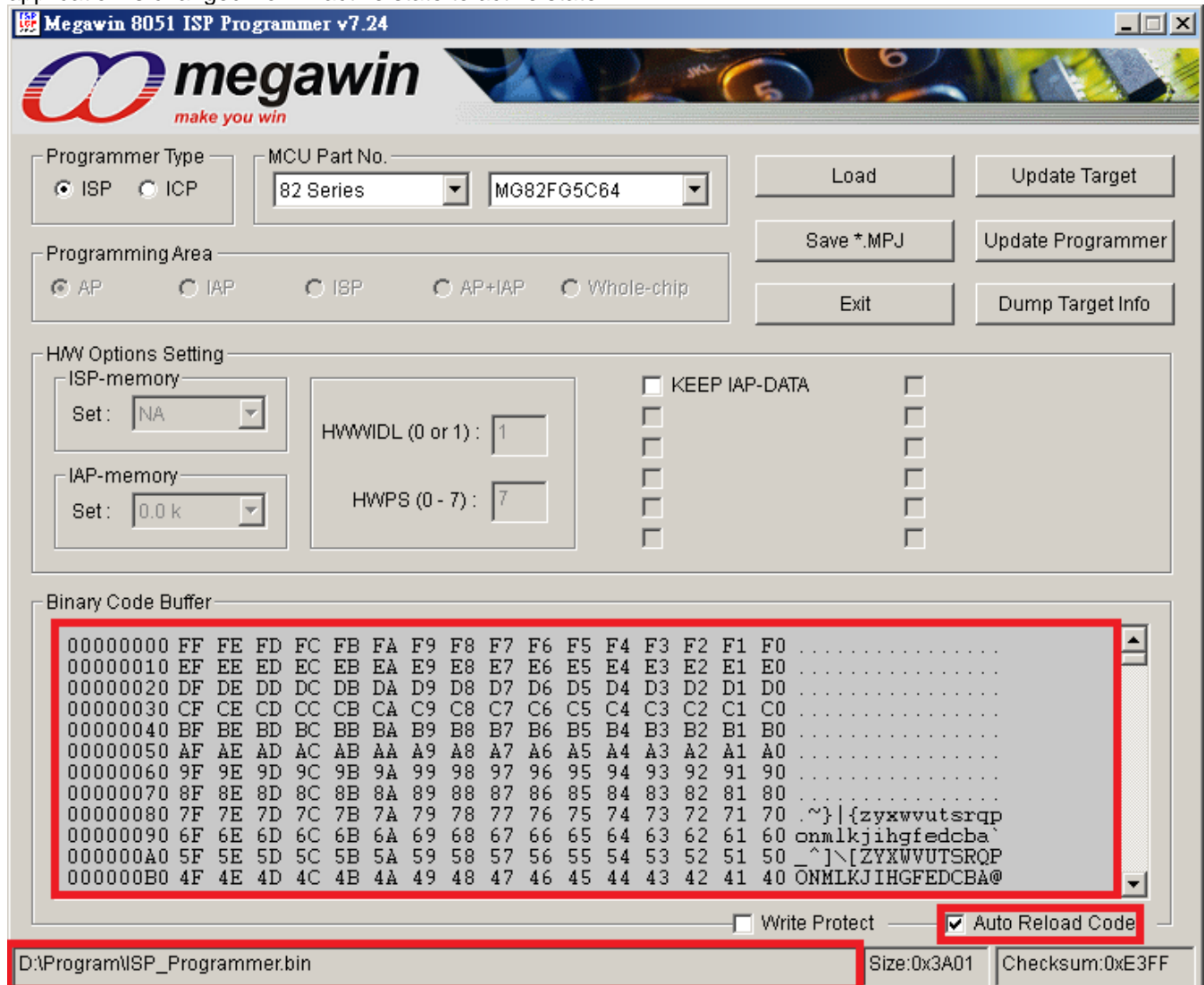


Figure 6:
P3.1 is used to drive a high-impedance input.



7 Special Notes for “Auto Reload Code”

Enable this function, the contents of the Binary Code Buffer will be reloaded according to the file path once the application is changed from inactive state to active state.



Megawin 8051 ISP Programmer v7.24

megawin
make you win

Programmer Type: ☒ ISP ☐ ICP

MCU Part No.: 82 Series MG82FG5C64

Load Update Target

Save *.MPJ Update Programmer

Exit Dump Target Info

Programming Area: ☒ AP ☐ IAP ☐ ISP ☐ AP+IAP ☐ Whole-chip

HW Options Setting

ISP-memory Set: NA

IAP-memory Set: 0.0 k

HWWIDL (0 or 1): 1

HWPS (0 - 7): 7

☐ KEEP IAP-DATA

Binary Code Buffer

```

00000000 FF FE FD FC FB FA F9 F8 F7 F6 F5 F4 F3 F2 F1 F0 .....
00000010 EF EE ED EC EB EA E9 E8 E7 E6 E5 E4 E3 E2 E1 E0 .....
00000020 DF DE DD DC DB DA D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 .....
00000030 CF CE CD CC CB CA C9 C8 C7 C6 C5 C4 C3 C2 C1 C0 .....
00000040 BF BE BD BC BB BA B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 .....
00000050 AF AE AD AC AB AA A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 .....
00000060 9F 9E 9D 9C 9B 9A 99 98 97 96 95 94 93 92 91 90 .....
00000070 8F 8E 8D 8C 8B 8A 89 88 87 86 85 84 83 82 81 80 .....
00000080 7F 7E 7D 7C 7B 7A 79 78 77 76 75 74 73 72 71 70 .~}|{zyxwvutsrqp
00000090 6F 6E 6D 6C 6B 6A 69 68 67 66 65 64 63 62 61 60 onmlkjihgfedcba`
000000A0 5F 5E 5D 5C 5B 5A 59 58 57 56 55 54 53 52 51 50 _^]\ZYXWVUTSRQP
000000B0 4F 4E 4D 4C 4B 4A 49 48 47 46 45 44 43 42 41 40 ONMLKJIHGFCDBA@
  
```

☐ Write Protect ☒ Auto Reload Code

D:\Program\ISP_Programmer.bin Size:0x3A01 Checksum:0xE3FF

Revision History

Revision	Description	Date
v5.30	(1) Fix the AP bug: Firmware upgrade will fail if host uses OHCI chip set. (2) For ICP Programmer, the user can select whether to update the hardware option or not.	2007/10/05
v5.30a	(1) Fix the AP bug: Wrong display in the H/W Option area when "MPC89E58.MPJ" is loaded. (2) Modify description for HWENW. (Section 3-3-3 & 3-3-4) (3) Correct description for ENLVRO, from 3.8V to 3.7V. (Section 3-3-3) (4) Update Section 2.1.	2008/01/24
v5.40	Add support for MG87FL51/52 and MG87FE51/52 in the ISP Programmer.	2008/07/09
V5.41	(1) In the Programming Area, the radio button name of "AP+IAP+ISP" changes to "Whole-chip." (2) When operate "Update Target" and "Update Programmer" functions, the only default option of "Update H/W Option" is "Yes."	2008/11/13
V5.42	Add support for MG87FL(E)2051/4051/6051 in the ISP Programmer.	2009/01/06
V5.43	Add support for MG82FG216/232/248 in the ISP Programmer.	2009/02/04
V5.44	(1) Add the "Set Max count " variable in Update Programmer function. (2) Add the "8051 ISP Writer U2" tool description	2009/02/27
V5.45	MG82FG216, MG82FG232, and MG82FG248 now have following option bit available for user to configure: ENLVRC, ENLVRO, OSCDN, ENROSC, HWENW	2009/03/16
V5.50	Add support for MG87FL(E)04 and MG82FL(E)308/316 in the ISP Programmer.	2009/09/01
V5.51	1. Supported the Multi-Load file function. 2. Available in Windows 7 operation system.	2010/01/20
V5.60	Add support for MG82FL(E)532/564 in the ISP Programmer.	2010/03/26
V5.61	Special Release	2010/06/02
V5.70	Add support for MG82FE216 in the ISP Programmer.	2010/07/05
V5.80	Add support for MG82FE632/664 in the ISP Programmer.	2010/12/22
V5.81	Modify auto-upgrade function for the firmware of the Programmer's MCU.	2011/01
V5.82	The ISP-ICP programmer supports Serial Number function when operate in Mode-3	2011/02
V5.83	Correct the IAP setting error on ICP programmer	2011/04
V5.90	1. Add support for MG86FL(E)104 in the ISP Programmer. 2. Remove the MG84FL516 in ISP and ICP Programmer.	2011/05
V5.91	Support new function on U2 Writer	2012/05
V6.00	Add support for MG86FL(E)508 in the ISP Programmer.	2012/07
V6.01	1. Add "Auto Reload Code" function. 2. Add version information on the title of the main window.	2012/09
V6.01a	Fix a bug on tip function when load MPJ file	2012/09/11
V6.02	Fix a bug on "Auto Reload Code" function.	2012/10/23
V6.10	Add support MG82FG5A64 in ISP Programmer.	2012/12/06
V6.20	Update "PC-site Driver " support Windows 8	2013/06/14
V6.30	1. Add support MG82FG5B(32/16) in ISP Programmer. 2. Add support MG20FL(E)809 in ISP Programmer.	2013/11/15
V6.40	Add support MG82FG5B(24/08) in ISP Programmer.	2014/04/09
V7.00	Support new H/W, TH079F	2014/06/01

V7.01	Fix a bug on TH079E	2014/07/01
V7.02	Support new H/W, TH064F	2014/09/24
V7.03	Fix a bug on Stand-Alone Operation	2014/12/01
V7.10	Add support MG82FG5C(64/32) in ISP Programmer.	2015/05/15
V7.11	Reduce the voltage of program level	2016/05/20
V7.20	Add support MG82FG5D(08/16) in ISP Programmer.	2017/06/09
V7.21	Fix load MPJ file error	2018/03/19
V7.22	Add support MG82G5E32 in ISP Programmer. Remove support MG82FG5D08 in ISP Programmer.	2018/06/11
V7.23	Fix program error when crystal 22M up & EN6T enable for 89 series	2018/11/16
V7.24	Support MG82F6D17	2019/03/25
V7.26	Automatically determine if there is external storage	2020/01/15
V7.27	Update Driver files	2020/02/07
V7.28	Fix load MPJ file error in SC version	2020/02/25
V7.29.0.0	Support MG82F6D64/6D32	2020/04/17
V7.30.0.0	Support MG82F6D16	2021/02/22
V7.32.0.0	Support MG82F5Bxx Support MG82F6B08/001/104 Remove MPJ function	2022/05/30
V7.32.0.1	Support MG87FL(E)04	2022/11/22
V7.4.0.0	Debug : MG82FG5Bxx, MA82F5Bxx info	2023/06/20
v7.5.0.0	Add Support MGEQ1C064	2023/08/21
v7.6.0.0	Add Support MG82F6P32	2024/08/27