Megawin

8051 Writer U1

User Manual

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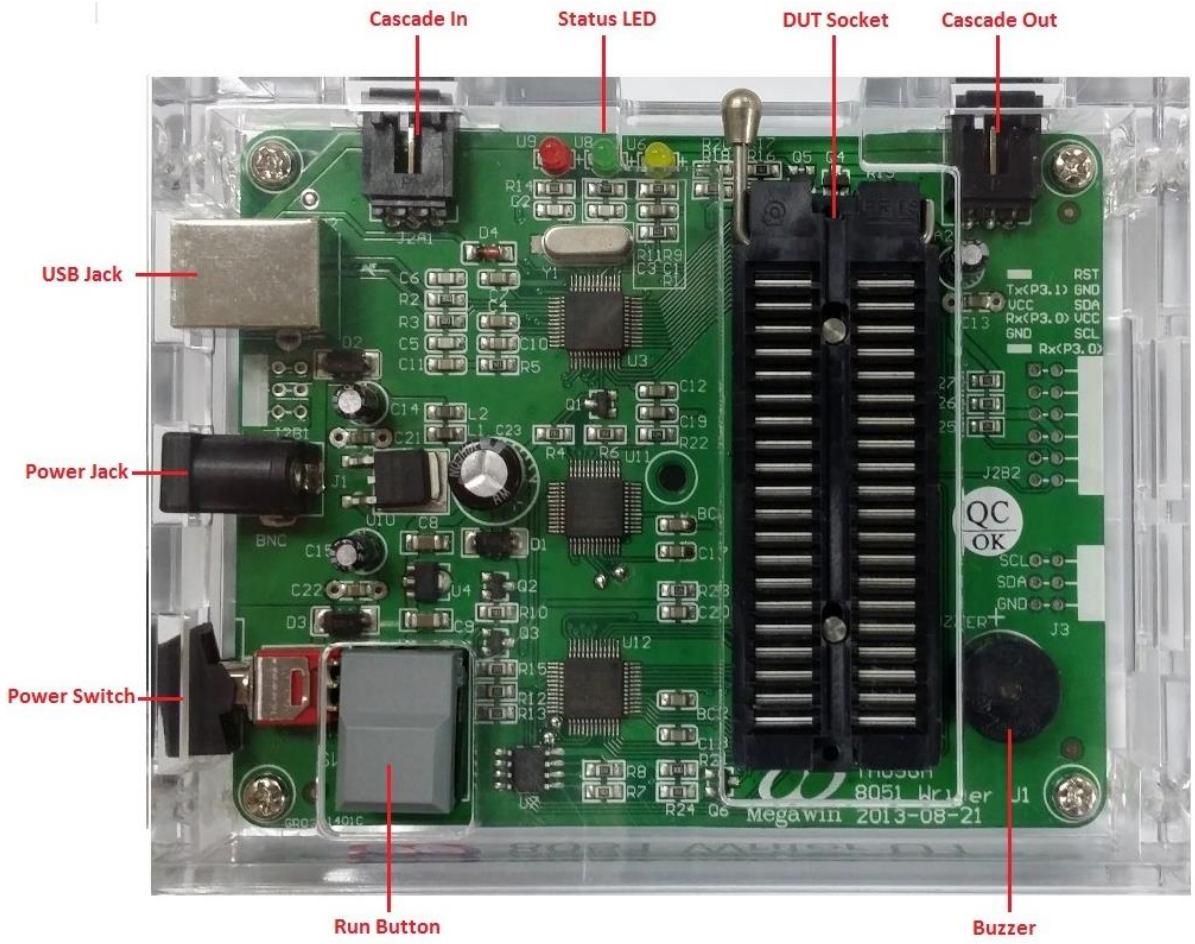
1. Introduction

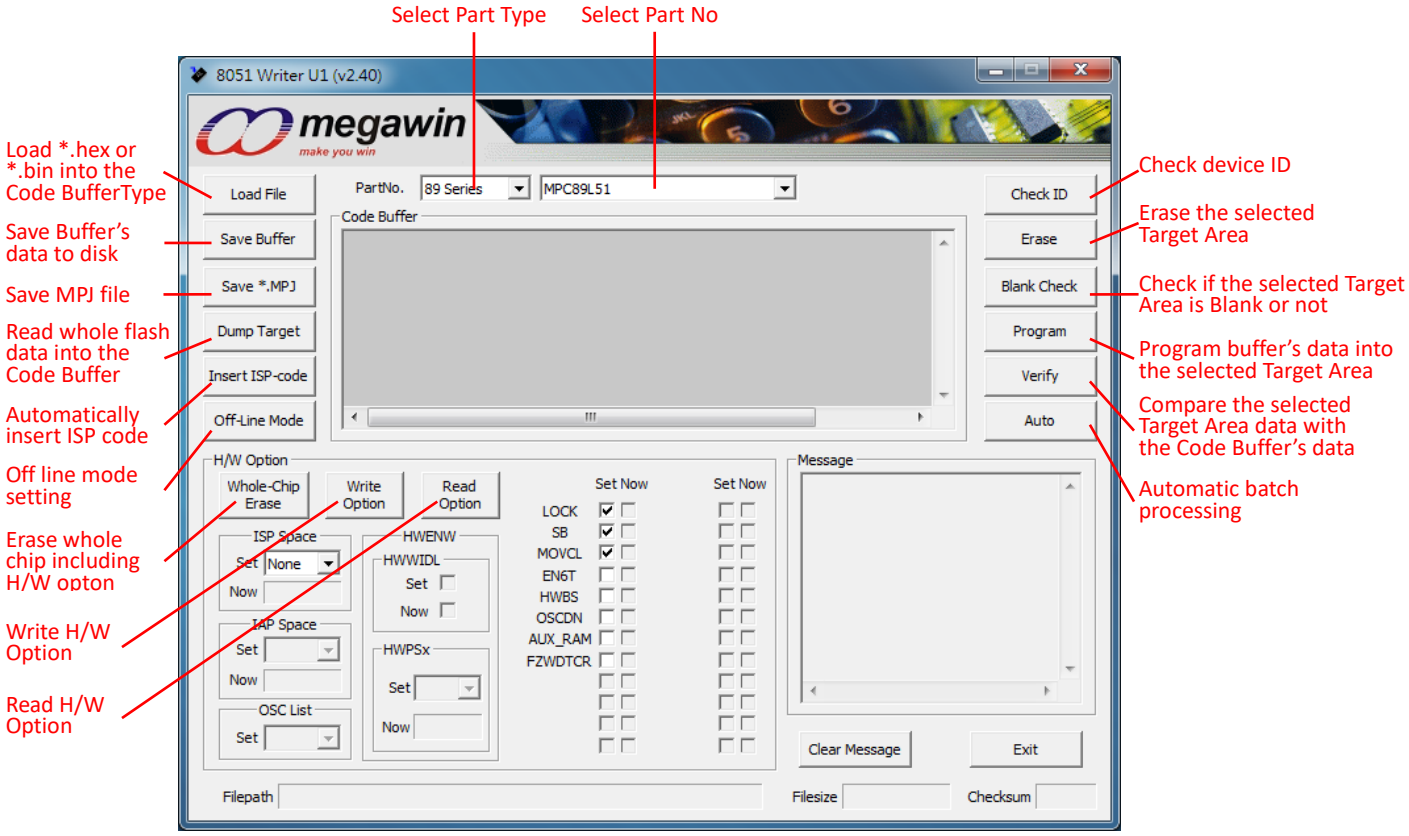
The “Megawin 8051 Writer U1” is a proprietary programmer designed for all Megawin’s 8051 MCU products. And there are two operating modes for the Writer. One is “On-line Programming Operation”, which functions as a universal Programmer. The other is “Off-line Copying Operation”, which functions as a copying machine for mass production.

Picture of the “Megawin 8051 Writer U1”

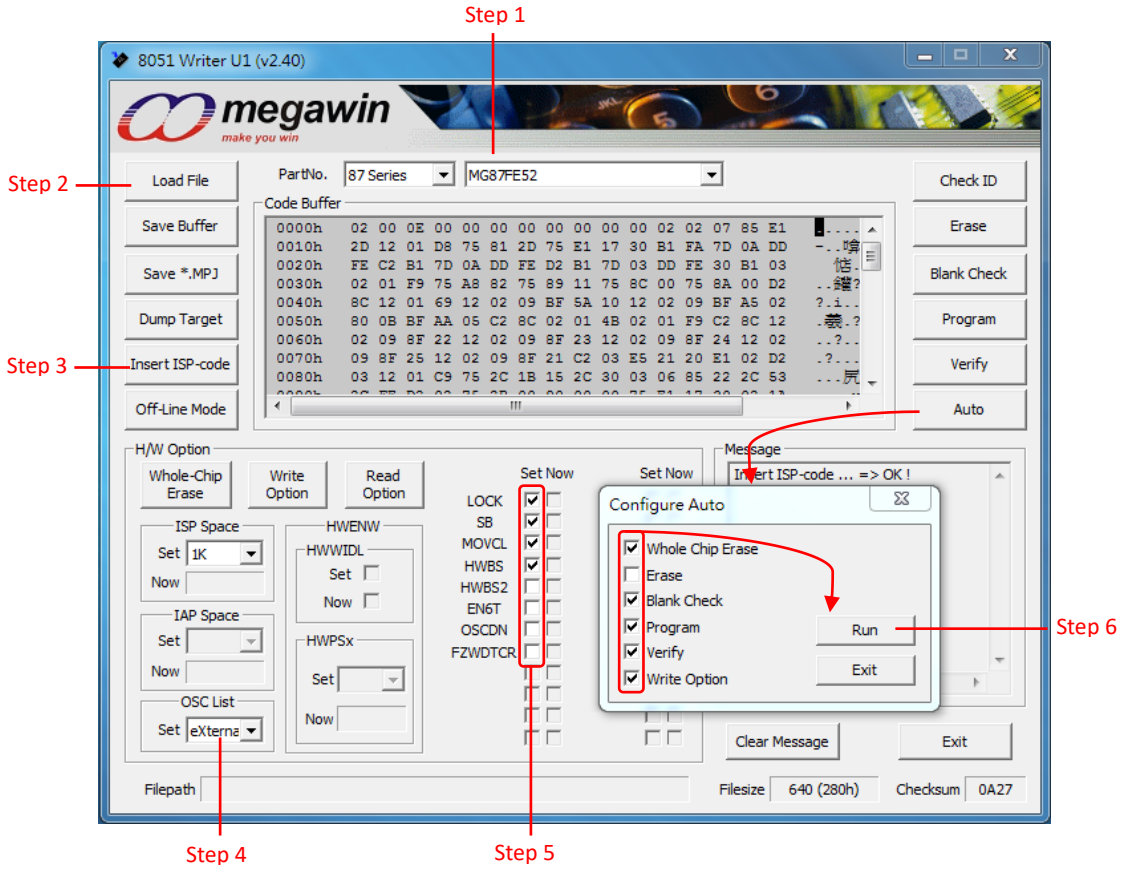


2. Easy-to-Use Writer

The following figure shows the GUI (Graphic User Interface) of the PC-site application program. The following sections will demonstrate how this Writer can be used very easily.



2.1 On-line Programming Operation



Follow the steps listed below for on-line programming (Example: MG87FE52)

Step 1: Select Part No.

Step 2: Load File.

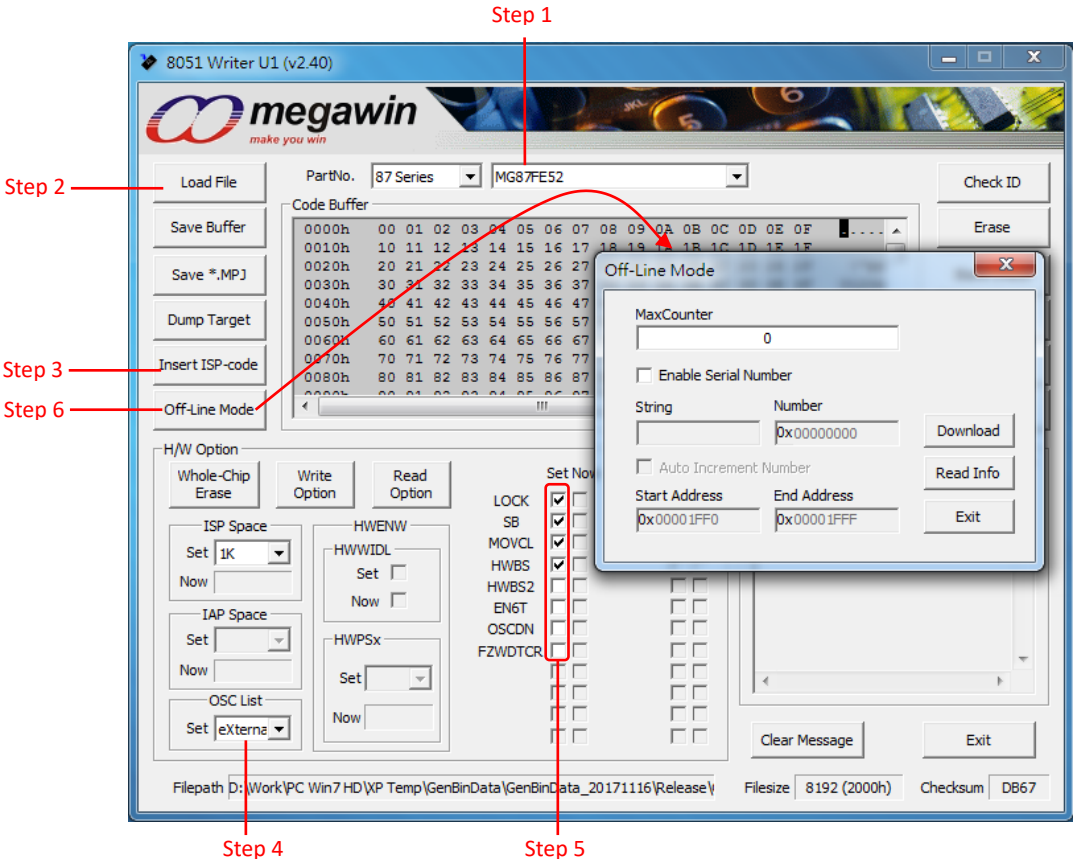
Step 3: Insert ISP code (This step may be omitted). The user could use ISP code provided by Megawin or developed by the user.

Step 4: Select system clock on OSC List. There are external crystal oscillator and internal oscillator of 6MHz, 11.059MHz, 12MHz, 22.118MHz, 24MHz & 24.576MHz.

Step 5: Enable H/W option bit. On most conditions, user will need to enable LOCK bit.

Step 6: Auto & Run. Enable the sub function to process the Programming Operation. The programming status will be shown on the message window.

2.2 Off-line Copying Operation



Follow the steps listed below for off-line Copying (Example: MG87FE52 & Gang2 Mode)

Step 1: Select Part No.

Step 2: Load File.

Step 3: Insert ISP code (This step may be omitted). The user could use ISP code provided by Megawin or developed by the user.

Step 4: Select system clock on OSC List. The user could use ISP code provided by Megawin or developed by the user.

Step 5: Enable H/W option bit. On most conditions, user need to enable LOCK bit.

Step 6: Off-Line Mode Setting

- MaxCounter: maximum number of devices programmed, zero for no limits.
- Enable Serial Number: Refer to the following section of "**How to use the Serial Number**" for details.
- Download: Download the contents from code buffer and all settings (Step 4, Step 5 and Serial Number if the function is enabled) into the Writer.

Step 7: Plug out the writer from PC, repeat "Download" at Step 6 for another Writer.

Step 8: Connect the two writers as shown on the following figure.

Step 9: Press the RUN button to process the Off-line Copying operation, and then the LEDs will indicate

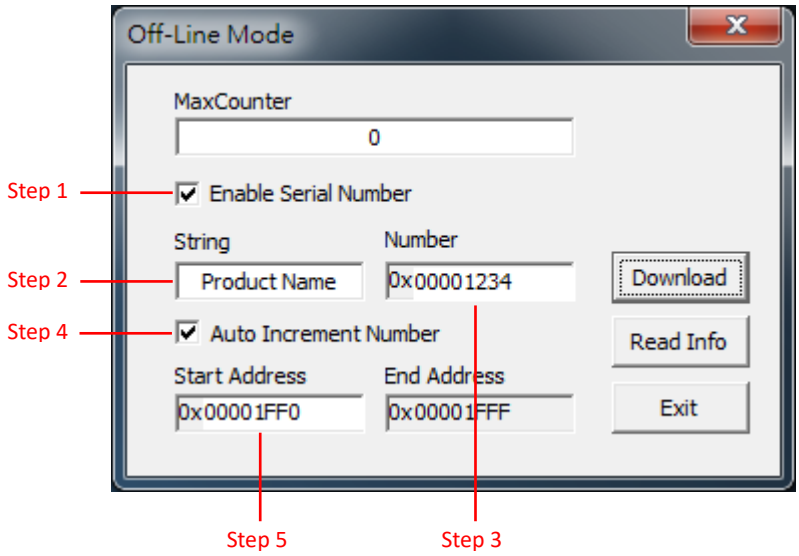
the programming status:

Orange - the device is under programming.

Green - the operation is completed and passed.

Red - the operation is failed.

3. How to use the Serial Number



Step 1: Enable the Serial Number function and totally 16 bytes (12 bytes for String and 4 bytes for Number) will be used.

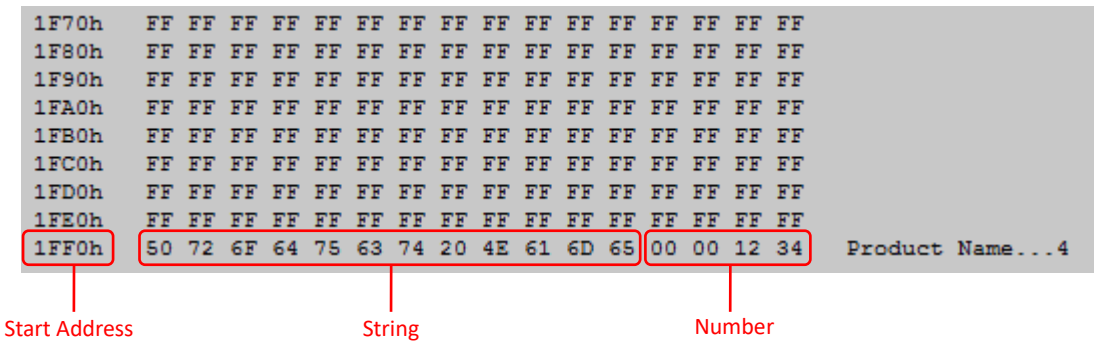
Step 2: Totally 12 bytes for the String and it could be used for Manufactory or Product string

Step 3: Totally 4 bytes for the Number and the value could be from 0x00000000 to 0xFFFFFFFF

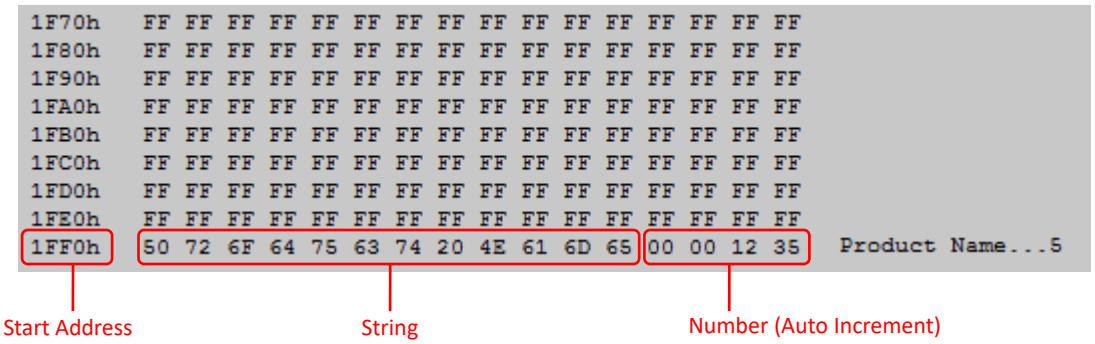
Step 4: The Number (as set in step 3) will be automatically added one when finish the “RUN” (Refer to the Step 9 in **Off-line Copying Operation**) process.

Step 5: Start Address for the Serial Number. It is limited from the chip size minus sixteen (For example, the limited Start Address for MG87FE52 is 0x00001FF0), and please make sure this range from start to end is unused..

After 1’st RUN process



After 2'nd RUN process



4. H/W Option

- **LOCK**

  Enable : Code dumped on a Writer is locked to 0xFF for security

  Disable : Code dumped on a Writer is not locked

- **SB**

  Enable : Code dumped on a Writer is scrambled for security

  Disable : Code dumped on a Writer is not scrambled

- **MOVCL**

  Enable : MOVC instruction executed from external program memory is disabled for security.

  Disable : MOVC is always enabled.

- **EN6T**

  Enable : MCU runs at 6T mode (each machine-cycle has 6 clocks).

  Disable : MCU runs at 12T mode (each machine-cycle has 12 clocks)

- **HWBS**

  Enable : When power-on, MCU will boot from ISP-memory if ISP-memory exists

  Disable : (No action)

- **OSCDN**

  Enable : Used under 16MHz for EMI reduction. (The gain of oscillating amplifier is reduced.)

  Disable : The gain of crystal oscillator is enough for higher Fosc oscillating

- **AUX_RAM**

  Enable : The internal auxiliary RAM access is disabled when the ERAM bit =0 (AUXR.bit1) and when ERAM bit =1 the internal auxiliary RAM access is enable

  Disable : The internal auxiliary RAM access is enable when the ERAM bit =0 (AUXR.bit1) and when ERAM bit =1 the internal auxiliary RAM access is disabled

- **FZWDTCR**

  Enable : The WDTCR register will be initialized to its reset value only by power-on reset

  Disable : The WDTCR register will be initialized to its reset value by all reset (including power-on, H/W, S/W and WDT reset)

- **ENLVR**

  Enable : Enable Low-Voltage Reset (LVR) , the LVR is around 2.4V for 3.3V device and 3.7V @12MHz for 5.0V device

  Disable : Disable LVR

- **LVFWP**

  Enable : Enable LVFWP (Low-Voltage Flash-Write Protection) while IAP or ISP programming

  Disable : Disable LVFWP

- **ENROSC**

Enable : MCU will used the internal 6MHz oscillator

Disable : MCU will used the external oscillator

- **HWENW**

  Enable : Automatically enable Watch-dog Timer by hardware when MCU is powered up

  Disable : (No action)

- **WDSFWP**

  Enable : To Write the WDTCR will be deny

  Disable : To Write the WDTCR will be accept

- **HWBS2**

  Enable : In addition to power-up, the reset from RST-pin will also force MCU to boot from ISP-memory, if ISP-memory is configured

  Disable : Where MCU boots from is determined by **HWBS**

- **ENLVRO**

  Enable : Enable Low-Voltage Reset (LVR) when Vdd less then 3.7V

  Disable : Disable LVR

- **ENLVRC**

  Enable : Enable Low-Voltage Reset (LVR) when Vdd less then 2.5V

  Disable : Disable LVR

- **BODRE**

  Enable : Enable Low-Voltage Reset (LVR)

  Disable : Disable LVR

- **BODWP**

  Enable : Enable LVFWP (Low-Voltage Flash-Write Protection) while IAP or ISP programming

  Disable : Disable LVFWP

- **P40IOE**

  Enable : Enable the P4.0 is in “Input Only mode” after Power On Reset

  Disable : The P4.0 is in default “Quasi-Bidirectional mode”

- **P41IOE**

  Enable : Enable the P4.1 is in “Input Only mode” after Power On Reset

  Disable : The P4.1 is in default “Quasi-Bidirectional mode”

- **{BO1S1O,BO1S0O}**

  {0, 0} : BOD1 detects the level at 2.0V on VDD

  {0, 1} : BOD1 detects the level at 2.4V on VDD

  {1, 0} : BOD1 detects the level at 3.7V on VDD

  {1, 0} : BOD1 detects the level at 4.2V on VDD

- **BO0REO**

Enable : BOD0 will trigger a RESET event to CPU on AP program start address

Disable : BOD0 can not trigger a RESET to CPU

- **BO1REO**

  Enable : BOD1 will trigger a RESET event to CPU on AP program start address

  Disable : BOD1 can not trigger a RESET to CPU

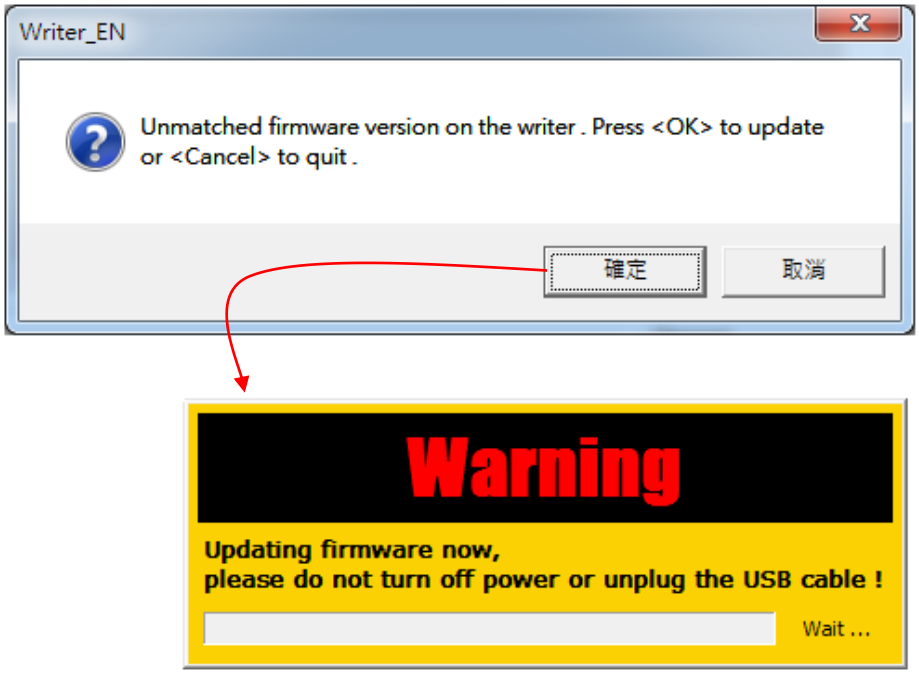
- **NSWDT**

  Enable : Enable the WDT to run in power down mode

  Disable : Disable the WDT to run in power down mode

5. Special Note

When the following message shows up that means the U1 writer needs to be updated firmware. Please make sure the USB cable should **NOT** unplug during the updating process. Otherwise, The U1 writer will cause unrecoverable damaged.



6. Revision History

Revision	Description	Date
v1.10	Release version	2008/11/20
v1.11	Special Release	2008/12/01
v1.12	Special Release	2008/12/25
v1.13	1. The default of “Target Area” is “AP+IAP+ISP.” 2. The size of “Erase” and “Blank Check” function set by “Load File”	2009/01/10
v1.14	Support MG87FL(E)2051/4051/6051 body.	2009/02/05
v1.15	The option bit of AUX_RAM is available to configure	2009/03/05
v1.16	Speed up the over all production time.	2009/03/23
v1.17	Support Serial Number Function	2009/05/25
v1.18	Special Release	2009/07/28
v1.20	1. Support MG82FL(E)308/316. 2. Separate the “PartNo” into several series. 3. Add an item “Erase” to the function of “Auto” 4. Support the MPJ file which created by “ Megawin 8051 writer “ or early version of “ Megawin 8051 writer U1”	2009/10/01
v1.30	1. Support MG82FL(E)532/564 2. Supported the Multi-Load file function	2010/03/26
v1.31	Special Release	2010/5/20
v1.32	Speed up the over all production time.	2010/07/05
v1.40	Support MG82FL(E)632/664	2010/12/24
v1.42	Special Release	2011/02/14
v1.50	Support MG84FG516 and MG86FL(E)104	2011/05/02
v1.61	Support MG86FL(E)508	2012/08/16
v1.70	1. Support MG82FG5A64 2. Update ISP CODE for MG84FG516	2012/12/11
v1.71	Modify the Whole-Chip Erase timing for 82/84/86/87 series	2013/01/07
v1.72	Update programming flow for MG84FL54	2013/06/13
v1.80	1. Support MG82FG5B(32/16) 2. Support MG20FL(E)809	2013/11/15
v1.81	Support MG82FG5B(24/08)	2014/04/09
v1.90	Support MG82FG5C(64/32)	2015/04/15
v2.00	Support MG82FG5D(16/08)	2017/06/09

v2.10	Support MG82G5E32 and remove MG82FG5D08	2018/06/11
v2.20	1. Update the figures. 2. Add H/W Option description	2018/08/21
v2.40	Support MG82F6D17	2019/03/11
v2.41	Support MA818-48	2019/06/25
v2.50	1. Support MG82F6D64, MG82F6D32, Remove MA818-48 2. Fix HWPsx Item on MG84FG516, MG86FL(E)104, MG82_FG5A(64/32), MG82FG5BSeries, MG82FG5C(64/32)	2020/04/17
v2.51	Modify power control on MG82F6D64, MG82F6D32 and MG82F6D17	2020/09/24
v2.70	Support MG82F6D16	2021/01/19
v2.90	1. Support MG82F5Bxx Series, 2. Update MG84FG516 ISP Code	2022/03/11
V3.00	Modify Request Form description	2022/04/22
V4.00	Support Burst Mode for MG82F6D32/6D64	2022/06/12